TAA5242 118dB のダイナミック レンジ、低消費電力、高性能 ステレオ オーディオ ADC

1 特長

- ADC チャネル
  - ステレオ高性能 ADC
  - 性能:
    - ライン差動入力のダイナミック レンジ:118dB
    - マイクロフォン差動入力のダイナミック レンジ:118dB
    - THD+N:-95dB
  - 入力電圧:
    - 差動、$2V_{RMS}$ フルスケール入力
    - シングルエンド、$1V_{RMS}$ フルスケール入力
  - 入力ミックス / マルチプレクサ オプション
  - サンプル レート (f_S) = 8kHz～768kHz
  - プログラム可能なマイクロフォン バイアス (最大 3V)
- 共通機能
  - 構成可能な HPF
  - ピン制御
  - オーディオ シリアル インターフェイス
    - フォーマット:TDM、I^2S、または左揃え
    - ワード長:16、20、24 または 32 ビット
  - プログラム可能な PLL による柔軟なクロック供給
  - 低消費電力モード
    - レコードの未定 mW
  - 単電源動作 1.8V または 3.3V
  - I/O 電源動作:1.2V、1.8V、または 3.3V
  - 温度グレード 1:-40℃ ≤ T_A ≤ +125℃

2 アプリケーション

- 陸上モバイル無線
- IP ネットワーク カメラ
- IP 電話
- テレビ会議システム
- 業務用オーディオ ミキサ / 制御卓

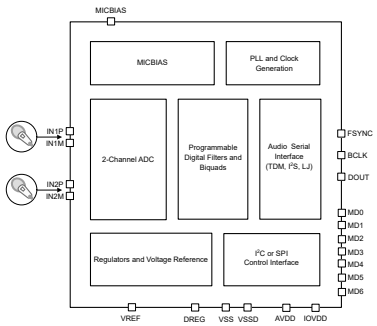
3 概要

TAA5242 は、$2V_{RMS}$ 差動入力、118dB ADC を備えた高性能 ステレオ ADC です。TAA5242 は、差動入力とシングルエンド入力の両方をサポートしています。このデバイスは、マイクロフォンとライン入力の両方の入力を、ADC チャネルで AC および DC 結合オプションによりサポートしています。TAA5242 は、、デジタル音量制御、低ジッタの位相ロック ループ (PLL)、構成可能なハイパス フィルタ (HPF) を内蔵しており、最高 768kHz のサンプル レートに対応できます。TAA5242 は時分割多重化 (TDM)、I^2S、または左揃え (LJ) オーディオ フォーマットに対応しており、ピン制御で制御できます。これらの高性能な機能を搭載し、単一電源で動作するので、TAA5242 はスペースの制約が厳しいオーディオ アプリケーションに最適です。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TAA5242	WQFN (28)	4mm × 4mm、0.5mm ピッチ

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略ブロック図

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2022	*	Initial Release

5 Pin Configuration and Functions

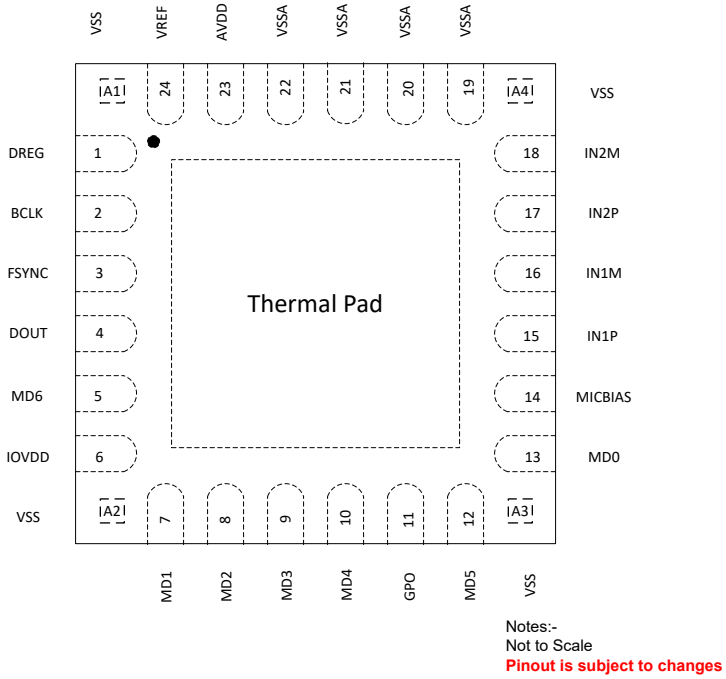


図 5-1. 28-Pin QFN With Exposed Thermal Pad, Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VSS	A1	Ground	Short directly to board Ground Plane.
DREG	1	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.5 V, nominal)
BCLK	2	Digital I/O	Audio serial data interface bus bit clock
FSYNC	3	Digital I/O	Audio serial data interface bus frame synchronization signal
DOUT	4	Digital Output	Audio serial data interface bus output
MD6	5	Digital Input	TDM Mode: MD6= DAISY_DIN
			I2S/LJ Mode: MD6=0: Stereo ADC Enabled; MD6=1: Mono Channel 1
IOVDD	6	Digital Supply	Digital I/O power supply (1.8 V or 3.3 V, nominal)
VSS	A2	Ground	Short directly to board Ground Plane.
MD1	7	Digital Input	Controller Mode: Frame Rate and BCLK frequency selection
			Target Mode: AVDD Supply and Word Length selection
MD2	8	Digital Input	Controller Mode: Frame Rate and BCLK frequency selection
			Target Mode: AVDD Supply and Word Length selection
MD3	9	Digital Input	Controller Mode: Controller Clock Input
			Target Mode: Digital HPF and Data Slot selection
MD4	10	Digital Input	ADC mode selection
GPO	11	Digital Output	Interrupt Output

ADVANCE INFORMATION

表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
MD5	12	Digital Input	ADC mode selection
VSS	A3	Ground	Short directly to board Ground Plane.
MD0	13	Analog Input	Multi-Level Analog input for Controller/Target and I^2S/TDM/LJ selection
MICBIAS	14	Analog	MICBIAS Output (Porgrammable output upto 11V)
IN1P	15	Analog Input	Analog Input 1P Pin
IN1M	16	Analog Input	Analog Input 1M Pin
IN2P	17	Analog Input	Analog Input 2P Pin
IN2M	18	Analog Input	Analo Input 2M Pin
VSS	A4	Ground	Short directly to board Ground Plane.
OUT1M	19	Analog Output	Analog Output 1M Pin
OUT1P	20	Analog Output	Analog Output 1P Pin
OUT2P	21	Analog Output	Analog Output 2P Pin
OUT2M	22	Analog Output	Analog Output 2M Pin
AVDD	23	Analog Supply	Analog power (3.3 V, nominal)
VREF	24	Analog	Analog reference voltage filter output

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
Supply voltage	IOVDD to VSS (thermal pad)	–0.3	3.9	V
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	5.656	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Functional ambient, T_A	-55	125	°C
	Operating ambient, T_A	–40	125	
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD(1)	Analog supply voltage to AVSS AVDD-3.3V Operation	3.0	3.3	3.6	V
AVDD(1)	Analog supply voltage to AVSS - AVDD 1.8V operation	1.65	1.8	1.95	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 1.2-V operation	1.08	1.2	1.32	V
INPUTS					
INxx	Analog input pins voltage to AVSS for line-in recording	0		AVDD	V
INxx	Analog input pins voltage to AVSS for microphone recording	0.1		MICBIAS – 0.1	V
	Digital input pins voltage to VSS (thermal pad)	0		IOVDD	V
MD0	MD0 pin w.r.t AVSS	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

ADVANCE INFORMATION

		MIN	NOM	MAX	UNIT
OTHERS					
	MD3 used as MCLK input clock frequency			36.864(2)	MHz
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2 V.
(2) MCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5 ns. For better audio noise performance, MCLK input must be used with low jitter.

6.4 Thermal Information

THERMAL METRIC(1)		TAA5242 RGE (WQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application report.

6.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC PERFORMANCE FOR INPUT RECORDING						
	Differential input full-scale AC signal voltage	AC-coupled input		2		V_{RMS}
	Single-ended input full-scale AC signal voltage	AC-coupled input		1		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		118		dB
SNR	Signal-to-noise ratio, A-weighted(1) (2)	IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain, Device in Hign Common Mode Tolerance Mode		110		dB
SNR	Signal-to-noise ratio, A-weighted(1) (2)	1.8V AVDD Operation:IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		110		dB
		1.8V AVDD Operation:IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		104		
DR	Dynamic range, A-weighted(2)	IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		118		dB
		IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		110		
DR	Dynamic range, A-weighted(2)	1.8V AVDD Operation: IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain	106	110		dB
		1.8V AVDD Operation: IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		104		

ADVANCE INFORMATION

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
THD+N	Total harmonic distortion(2)	IN1 differential AC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain			–95	TBD	dB
		IN1 differential DC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain			–95		
ADC OTHER PARAMETERS							
	Input impedance	Differential input, between INxP and INxM, 5kΩ Mode			5.5		kΩ
	Input impedance	Single-ended input, between INxP and INxM, 5kΩ Mode			2.75		kΩ
	Offset	Shorted Input.			TBD		mV
	Digital volume control range	Programmable 0.5-dB steps		–80		47	dB
	Input Signal Bandwidth	Upto 192KSPS FS Rate			0.46		FS
		>192KSPS			90		kHz
	Output data sample rate	Programmable		3.675		768	kHz
	Output data sample word length	Programmable		16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter			2		Hz
	Interchannel isolation	–1-dB full-scale AC signal line-in input to non measurement channel			–134		dB
	Interchannel gain mismatch	–6-dB full-scale AC signal line-in input, 0-dB channel gain			0.1		dB
	Interchannel phase mismatch	1-kHz sinusoidal signal			0.01		Degrees
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain			92		dB
MICROPHONE BIAS							
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS			2		$µV_{RMS}$
	MICBIAS voltage	AVDD=1.8V			1.375		V
	MICBIAS voltage	AVDD=3.3V			2.75		V
DIGITAL I/O							
V_{IL}	Low-level digital input logic voltage threshold	All digital pins, IOVDD 1.8-V operation		–0.3		0.35 × IOVDD	V
		All digital pins, IOVDD 3.3-V operation		–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins, IOVDD 1.8-V operation		0.65 × IOVDD		IOVDD + 0.3	V
		All digital pins, IOVDD 3.3-V operation		2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8-V operation				0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3-V operation				0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8-V operation		IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3-V operation		2.4			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0 V		–5	0.1	5	µA

ADVANCE INFORMATION

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in sleep mode (software shutdown mode)	All device external clocks stopped		TBD		µA
I_{IOVDD}				1		
I_{AVDD}	Current consumption when MICBIAS ON, MICBIAS voltage 10 V, 30 mA load, ADC off	f_S = 48 kHz, BCLK = 256 × f_S		TBD		mA
I_{IOVDD}				0.01		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 16-kHz, MICBIAS off, PLL on, BCLK = 512 × f_S			TBD		mA
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 48-kHz, MICBIAS on, PLL off, BCLK = 512 × f_S			TBD		mA
I_{IOVDD}				0.1		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

6.6 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		18			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		18			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time			10	ns

(1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

6.7 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of SDOUT, IOVDD = 3.3 V			14	
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of FSYNC to 50% of SDOUT, IOVDD = 3.3 V			14	

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(BCLK)}$	BCLK output clock frequency; master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{L(BCLK)}$	BCLK low pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{d(FSYNC)}$	BCLK to FSYNC delay; master mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3 V			14	
$t_{r(BCLK)}$	BCLK rise time; master mode	10% - 90% rise time, IOVDD = 1.8 V			10	ns
		10% - 90% rise time, IOVDD = 3.3 V			10	
$t_{f(BCLK)}$	BCLK fall time; master mode	90% - 10% fall time, IOVDD = 1.8 V			8	ns
		90% - 10% fall time, IOVDD = 3.3 V			8	

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

ADVANCE INFORMATION

7 Parameter Measurement Information

8 Detailed Description

8.1 Overview

The TAA5242 is from a scalable family of devices. As part of the extended family of devices, the TAA5242 consists of a high-performance, low-power, flexible, mono/stereo, audio analog-to-digital converter (ADC). This device is intended for applications such as ruggedized communication equipment, IP network camera, Professional Audio and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration registers across extended family make this device well suited for scalable system designs.

The TAA5242 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma (ΔΣ) ADCs
- Configurable single-ended or differential audio inputs with 2Vrms signal swing
- Low-noise microphone bias output
- Decimation filters with linear-phase
- High-pass filter (HPF)
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I^2S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

8.2 Functional Block Diagram

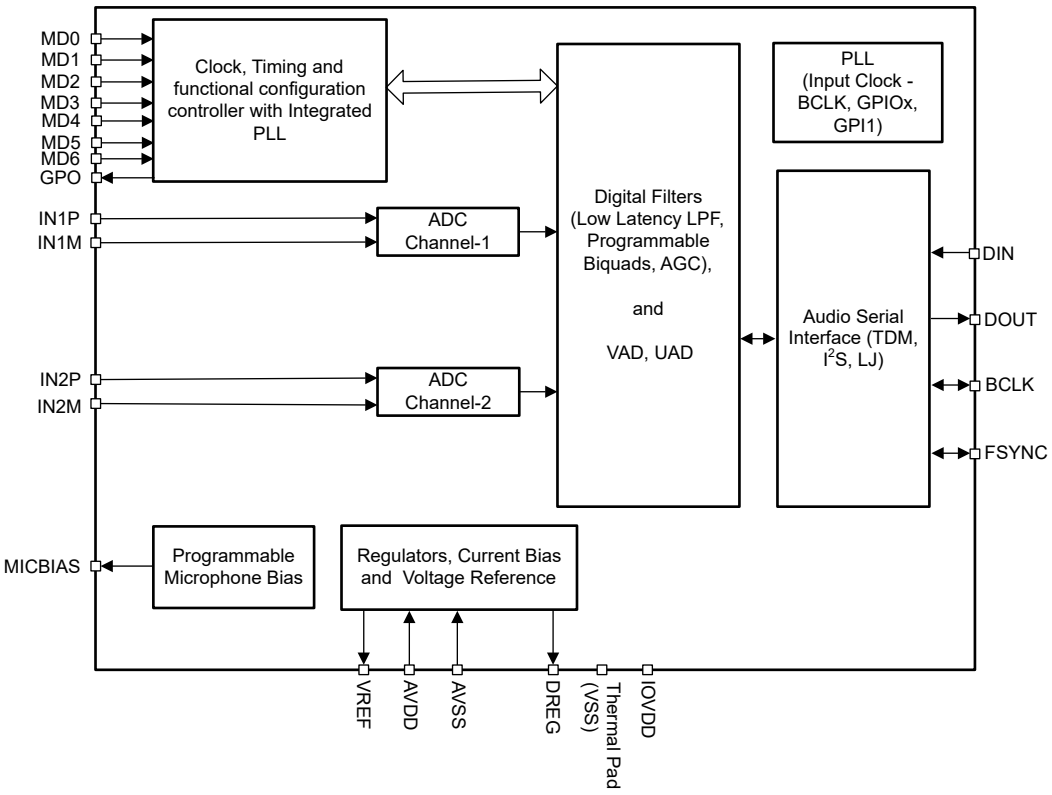


図 8-1. Functional Block Diagram

8.3 Feature Description

ADVANCE INFORMATION

8.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system. The MD0 to MD6 pins allow the device to be controlled by either pullup or pulldown resistors.

8.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAA5242 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for the I^2S and LJF, and the pin-selectable controller-target configurability for bus clock lines.

The device supports an audio bus controller or target mode of operation using the hardware pin MD0. In target mode, FSYNC and BCLK work as input pins whereas in controller mode, FSYNC and BCLK work as output pins generated by the device. 表 8-1 shows the master and slave mode selection using the MD0 pin.

表 8-1. Controller and Target Mode Selection

MD0	CONTROLLER AND TARGET SELECTION
Short to Ground	Target I2S Mode
Short to Ground with 4.7K Ohms	Target TDM Mode
Short to AVDD	Controller I2S Mode
Short to AVDD with 4.7K Ohms	Controller TDM Mode
Short to AVDD with 22K Ohms	Target LJ Mode

The word length for audio serial interface (ASI) in TAA5242 can be selected through MD1 and MD2 Pins in target mode of operation. In controller mode, fixed word length of 32 bits is supported. The TAA5242 also supports 1.8V AVDD operation in target mode with 32 bit word length. 表 8-2 shows the configuration table for setting word length and AVDD supply voltage

表 8-2. Word Length and Supply Mode Selection

MD1	MD2	CONTROLLER AND TARGET SELECTION
Low	Low	Word Length=32 AVDD=3.3V
Low	High	Word Length=32 AVDD=1.8V
High	Low	Word Length=24 AVDD=3.3V
High	High	Word Length=16 AVDD=3.3V

The TAA5242 offers daisy chain configuration for target TDM mode of operation. This can be selected through MD3 pin when MD0 is configured in target TDM mode. In this mode, MD6 can be used as Daisy chain data input. 表 8-3 shows the daisy chain configuration in Target TDM mode of operation based on MD3 pin.

表 8-3. Daisy Chain Selection for Target TDM Mode

MD3	Daisy Chain
Low	Disable
High	Enable

ADVANCE INFORMATION

8.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. 図 8-2 and 図 8-3 show the protocol timing for TDM operation with various configurations.

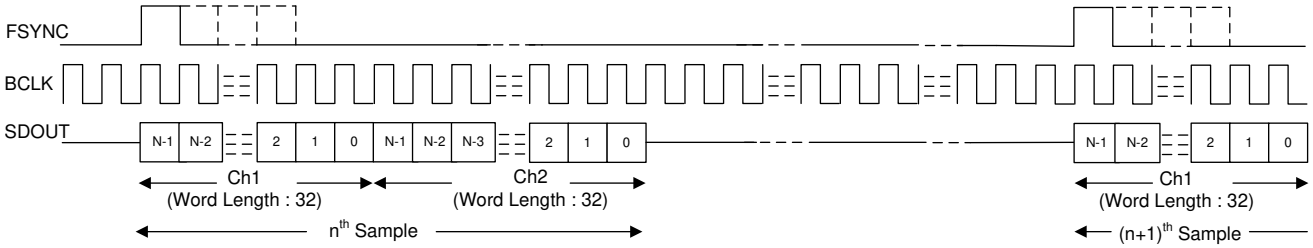


図 8-2. TDM Mode Protocol Timing (MD0 shorted to ground with 4.7K Ohms) In Target Mode

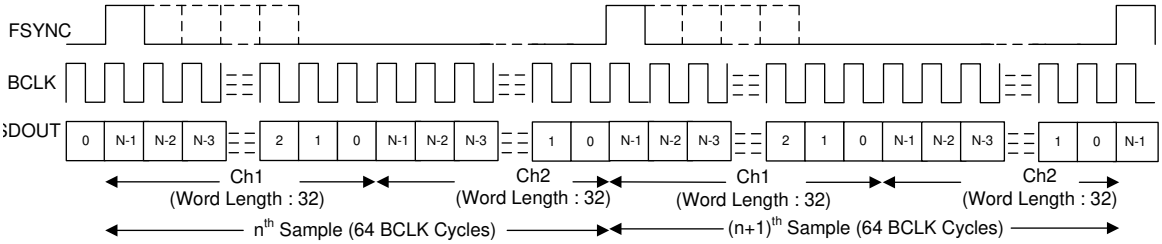


図 8-3. TDM Mode Protocol Timing (MD0 shorted to AVDD with 4.7K Ohms) In Controller Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the 32-bits word length of the output channel data. The device transmits a zero data value on SDOUT for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

8.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In master mode, FSYNC is transmitted on the rising edge of BCLK. 図 8-4 and 図 8-5 show the protocol timing for I^2S operation in slave and master mode of operation.

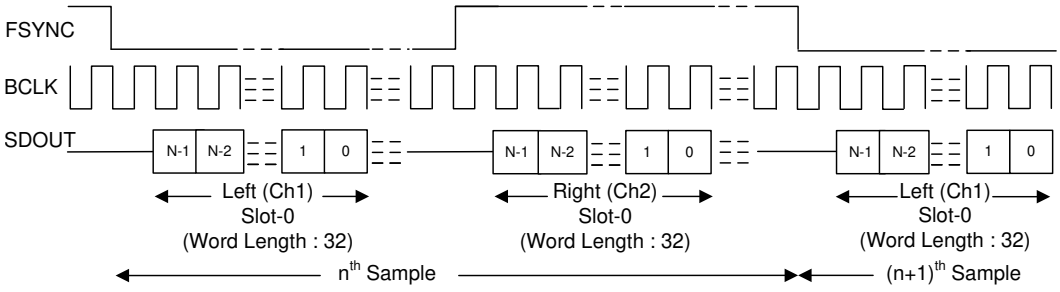


図 8-4. I^2S Mode Protocol Timing (MD0 shorted to ground) in Target Mode

ADVANCE INFORMATION

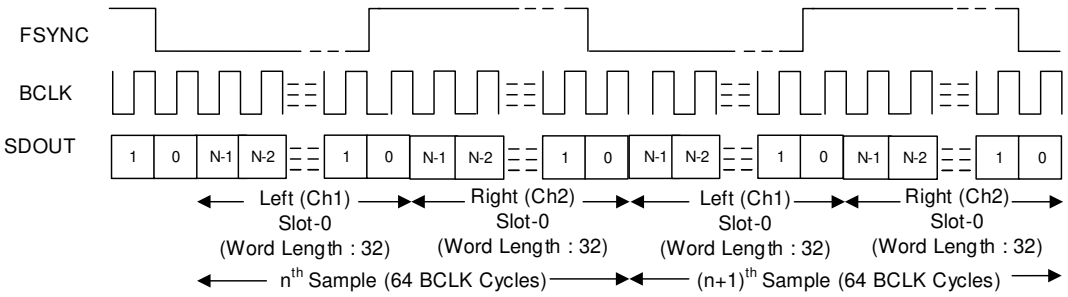


図 8-5. I²S Protocol Timing (MD0 shorted to AVDD) In Controller Mode

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the 32-bits word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the 32-bits data word length. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the 32-bits data word length. The device transmit zero data value on SDOUT for the extra unused bit clock cycles.

8.3.3 Analog Input Configurations

The device supports simultaneous recording of up to two channels using the high-performance stereo ADC. The device consists of two pairs of analog input pins (INxP and INxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for the analog pins can be from electret condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs can be capacitively coupled (AC-coupled) or DC-coupled to the device. For best distortion performance, use of low-voltage coefficient capacitors for AC-coupling is recommended. The typical input impedance for the TAA5242 is 5 kΩ for the INxP or INxM pins. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has a quick charge scheme to speed up the charging of the coupling capacitor at power-up. Quick-charge time for the device is configured using MD3 pin along with digital HPF.

表 8-4 shows the analog input configuration modes available with MD4 and MD5 configuration

表 8-4. Analog Input Configurations

MD4	MD5	ANALOG INPUT CONFIGURATION
Low	Low	Differential input; AC-Coupled only
Low	High	Differential input; AC or DC-Coupled
High	Low	Single Ended Input on INxP
High	High	Differential input; AC or DC-Coupled; Low Power Mode

8.3.4 Reference Voltage

All audio data converters require a DC reference voltage. The TAA5242 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to analog ground (VSS). The value of this reference voltage, VREF, is set to 2.75 V(for 3.3V AVDD) or 1.375V(for 1.8V AVDD), which in turn supports a 2-V_{RMS} differential full-scale input and 2-V_{RMS} differential full-scale output to the device. Do not connect any external load to a VREF pin.

8.4 Device Functional Modes

ADVANCE INFORMATION

8.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. Configure all hardware control pins (MD0, MD1, MD2, MD3, MD4, MD5 and MD6) for the device desired mode of operation before enabling clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up all ADC channels and starts transmitting and playing data over the audio serial interface. If the clocks are stopped, then the device auto powers down the ADC channels.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TAA5242 is a stereo, high-performance audio ADC that supports sample rates of up to 192 kHz. The device can be configured by controlling the Pins MD0 to MD6 and can support 1.8/3.3V AVDD along with flexible Digital interfaces of I2S/TDM/LJF. The device supports stereo high dynamic range ADC with differential and single ended input capabilities.

9.2 Typical Application

9.2.1 Application

図 9-1 shows a typical configuration of the TAA5242 for an application using two channel MEMS microphone in AC coupled mode with an I^2S target audio data target interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

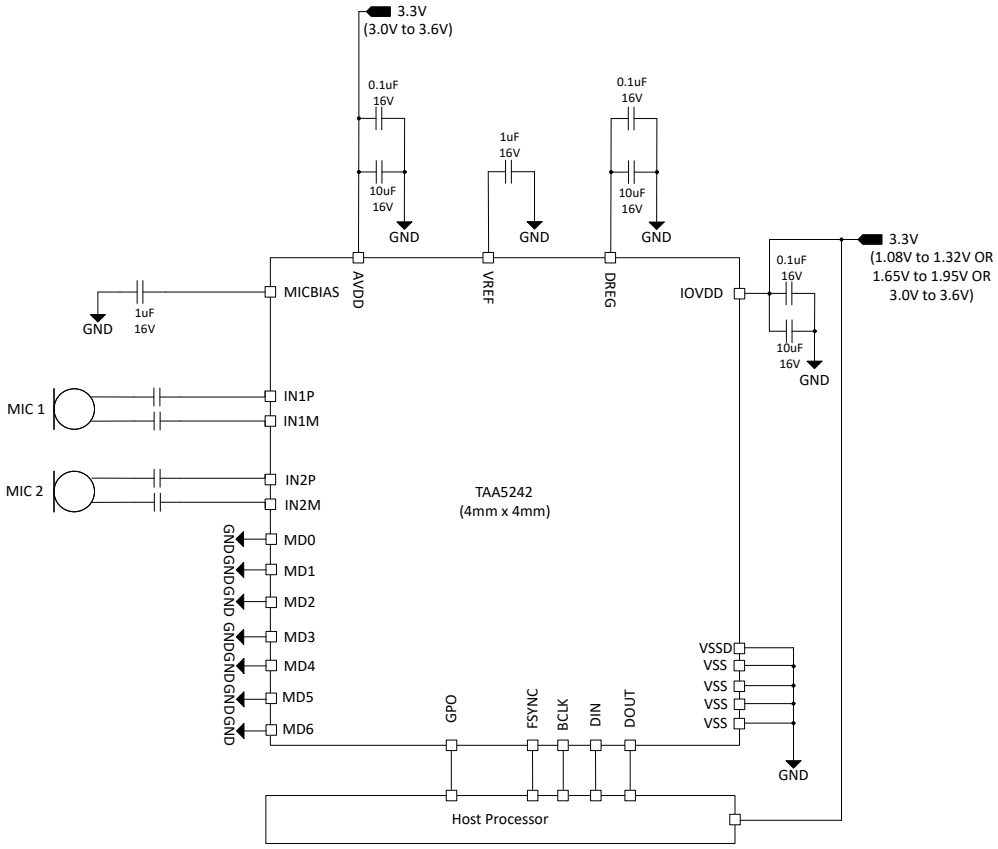


図 9-1. Stereo MEMS Microphone Block Diagram

9.2.2 Design Requirements

表 9-1 lists the design parameters for this application.

表 9-1. Design Parameters

PARAMETER	VALUE
AVDD	3.3 V
IOVDD	1.2 V or 1.8 V or 3.3 V
AVDD supply current consumption	TBD
IOVDD supply current consumption	TBD
Maximum MICBIAS current	5 mA

9.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAA5242 for this specific application.

1. Apply power to the device:
   a. Power up the IOVDD and AVDD power supplies
   b. Wait for at least 1ms to allow the device to initialize the internal registers.
   c. The device now goes into sleep mode (low-power mode < 10 µA)
2. Configure the Mode Pins as per the system requirements:
   a. Select the ASI Mode by pulling up to AVDD or down to VSS; MD0 Pin. MD0 should be grounded for this use case.
   b. Pull Up to IOVDD or Pull down to VSS on MD1 to MD6 Pin as per the reuqired configuration. All the Pins are grounded for this use case.
3. Applying the ASI Clocks will wake up the device (BCLK and FSYNC)
4. To put the device back in sleep mode, Stop the clocks:
   a. Wait at least 100 ms to allow the device to complete the shutdown sequence
   b. Change the Mode configuration by changing MD0 to MD5 as per requirement
5. Repeat step 3 and step 4 as required for mode transitions

ADVANCE INFORMATION

ADVANCE INFORMATION

10 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, after all Mode pins are stable, then only initiate the clocks to initialize the device.

For the supply power-up requirement, t_1, t_2 and t_3 must be at least 2 ms to allow the device to initialize the internal registers. See the *セクション 8.4* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_4, t_5 and t_6 must be at least 10 ms. This timing (as shown in 図 10-1) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into low power mode.

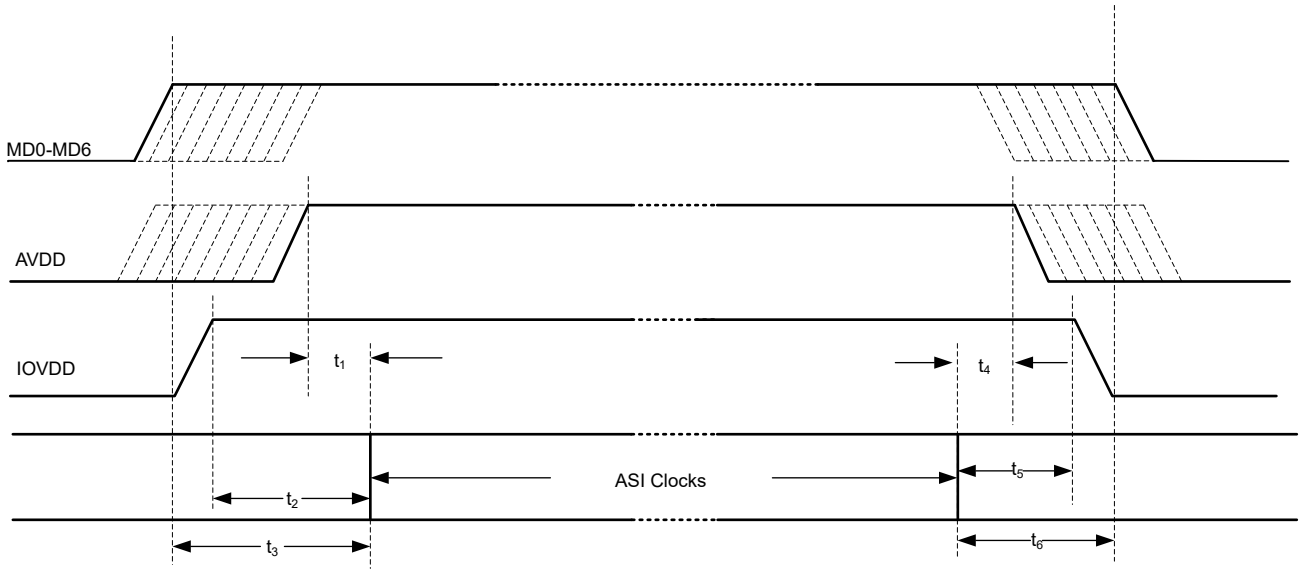


図 10-1. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100 ms.

The TAA5242 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

11.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

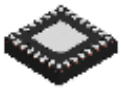
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

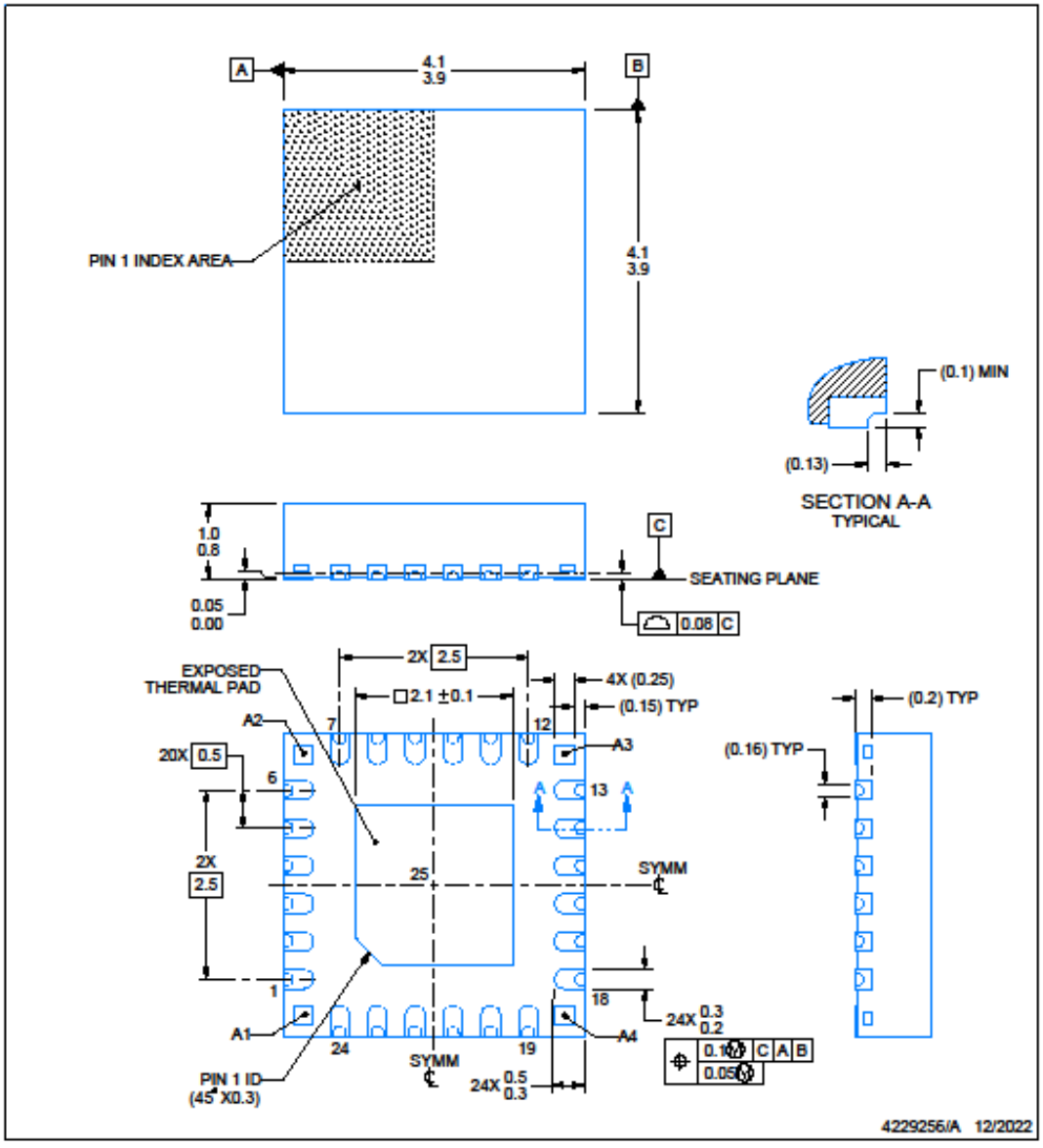
RGE0024W



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

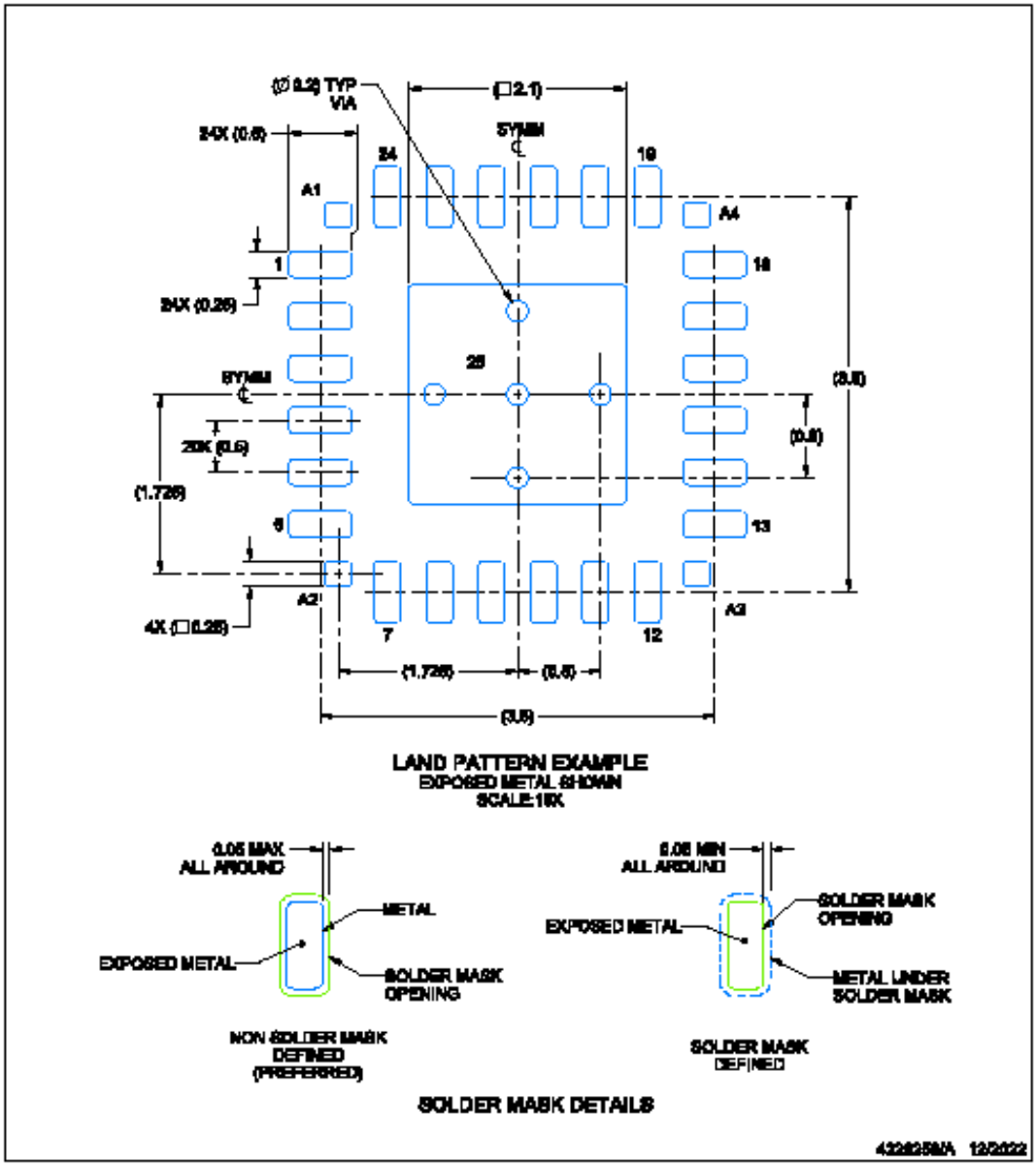
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

RGE0024W — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Texas Instruments
www.ti.com

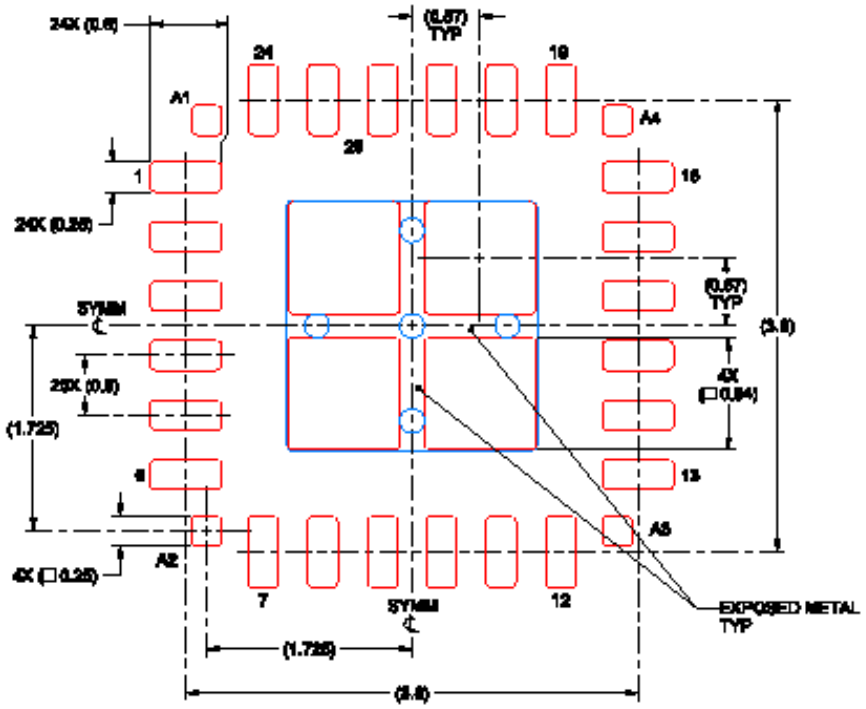
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGE0024W — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 28:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTAA5242IRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

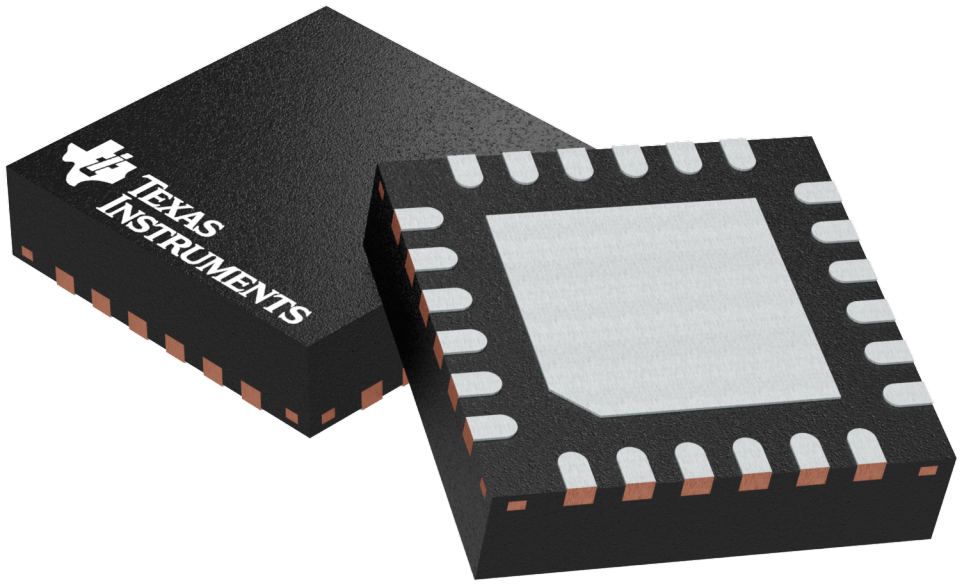
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265