

TAC5212 高性能、ステレオ オーディオ コーデック、ダイナミックレンジが 118dB の ADC およびダイナミックレンジが 119dB の DAC 搭載

1 特長

- ADC チャンネル
 - 高性能ステレオ ADC
 - 性能：
 - ライン差動入力のダイナミックレンジ：118dB
 - マイクフォン差動入力のダイナミックレンジ：118dB
 - THD+N：-95dB
 - チャンネル加算モードで高 SNR をサポート
 - 入力電圧：
 - 差動、 $2V_{RMS}$ フルスケール入力
 - シングルエンド、 $1V_{RMS}$ フルスケール入力
 - 入力ミックス / マルチプレクサのオプション
 - サンプルレート (f_s)：8kHz~768kHz
 - プログラム可能なマイクフォンバイアス (最大 3V)
- DAC チャンネル
 - 高性能ステレオ DAC
 - DAC 性能：
 - DAC からライン出力までのダイナミックレンジ：119dB
 - DAC から HP 出力までのダイナミックレンジ：115dB
 - THD+N：-95dB
 - ヘッドホン / ライン出力の出力電圧：
 - 差動、 $2V_{RMS}$ フルスケール
 - シングルエンド、 $1V_{RMS}$ フルスケール
 - DAC サンプルレート (f_s)：8KHz~768KHz
- 共通機能
 - 最大 4 個のレコード チャンネル
 - アナログ 2 チャンネル + デジタル 2 チャンネル
 - アナログ 1 チャンネル + デジタル 3 チャンネル
 - デジタル 4 チャンネル
 - アナログ入力から出力へのバイパス
 - 音声アクティビティ検出
 - バッテリ保護
 - 信号歪みリミッタ
 - サーマル フォールドバック
 - 低レイテンシ フィルタの選択
 - HPF およびバイカッド フィルタをプログラム可能
 - I²C および SPI 制御インターフェイス
 - オーディオシリアル インターフェイス
 - フォーマット：TDM、I²S、左揃え
 - ワード長：16、20、24 または 32 ビット
 - 柔軟なクロック供給のためのプログラム可能な PLL

- 低消費電力モード
 - 再生時：未定 mW
 - 録音時：未定 mW
- 単一電源動作：1.8V または 3.3V
- I/O 電源動作：1.2V、1.8V または 3.3V
- 温度グレード 1：-40°C ≤ T_A ≤ +125°C

2 アプリケーション

- 陸上モバイル無線
- IP ネットワーク カメラ
- IP 電話
- テレビ会議システム
- 業務用オーディオ ミキサ / 制御卓

3 概要

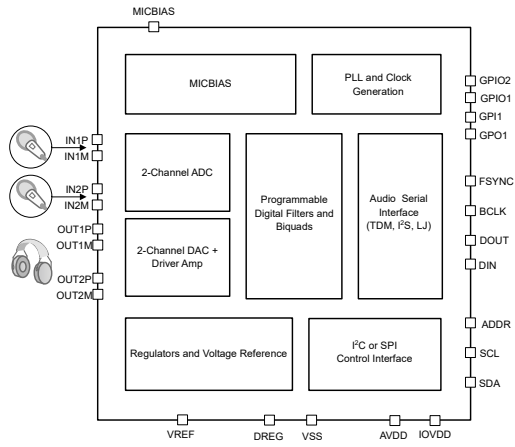
TAC5212 は、 $2V_{RMS}$ の差動入力、118dB のステレオ ADC および $2V_{RMS}$ のステレオ DAC を備えた、高性能なステレオ コーデックです。TAC5212 は、差動入出力とシングルエンド入出力の両方をサポートしています。このデバイスは、ADC チャンネルでマイクフォン入力とライン入力の両方をサポートしています。DAC 出力は、ライン出力またはヘッドホン負荷のいずれかに構成できます。TAC5212 は、ヘッドホン負荷に最大 62.5mW を駆動できます。TAC5212 は、プログラム可能なチャンネル ゲイン、デジタル音量制御、低ジッタの位相ロック ループ (PLL)、プログラム可能なハイパス フィルタ (HPF)、プログラム可能な EQ およびバイカッド フィルタ、低レイテンシのフィルタ モードを内蔵しており、最高 768kHz のサンプルレートに対応できます。TAC5212 は時分割多重化 (TDM)、I²S、左揃え (LJ) オーディオ フォーマットに対応しており、I²C または SPI で制御できます。これらの高性能な機能を内蔵し、単一電源で動作するため、TAC5212 はスペースに制約のあるオーディオ アプリケーションにとって最適な選択肢となります。

製品情報

| 部品番号 | パッケージ ⁽¹⁾ | 本体サイズ (公称) |
|---------|----------------------|---------------------|
| TAC5212 | WQFN (28) | 4mm × 4mm、0.5mm ピッチ |

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。





概略ブロック図

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4 Device Comparison Table

| FEATURE | TAC5212 | TAC5112 | TAC5211 | TAC5111 | TAC5242 | TAC5142 |
|--------------------------------|---|---------|---|---------|---|---------|
| Control interface | I ² C or SPI | | | | Pin control | |
| Digital audio serial interface | TDM or I ² S or left-justified (LJ) | | | | TDM or I ² S | |
| Audio ADC channel | 2 | | 1 | | 2 | |
| Digital microphone channel | 4 | | 2 | | Not available (N/A) | |
| Programmable MICBIAS voltage | Yes | | | | Yes (Fixed Voltage) | |
| ADC Dynamic range | 118 dB | 100 dB | 118 dB | 100 dB | 118 dB | 100 dB |
| Audio DAC Channel | 2 | | 1 | | 2 | |
| DAC Dynamic Range | 119 dB | 106dB | 119 dB | 106 dB | 119 dB | 106 dB |
| Compatibility | Pin-to-pin, package, and control registers compatible; drop-in replacements of each other | | Pin-to-pin, package, and control registers compatible; drop-in replacements of each other | | Pin-to-pin, package, drop-in replacements of each other | |
| Package | QFN , 28-pin, 4.00 mm × 4.00 mm (0.5-mm pitch) | | | | | |

5 Pin Configuration and Functions

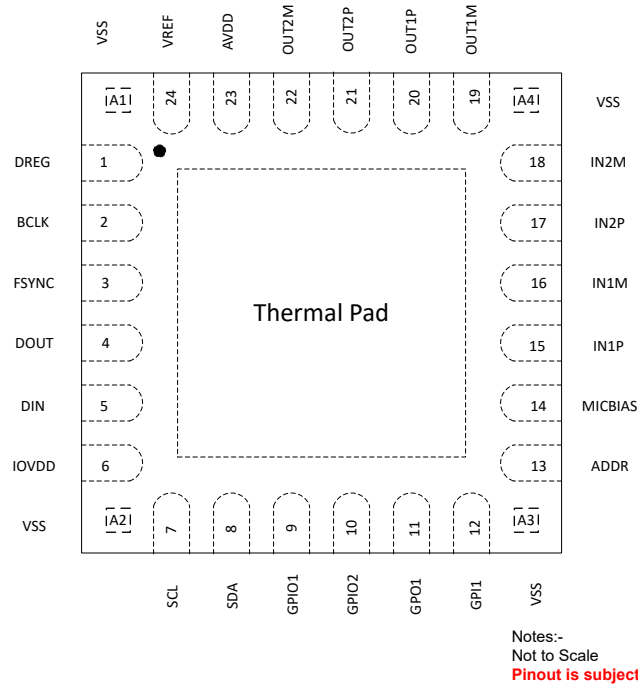


図 5-1. 28-Pin QFN With Exposed Thermal Pad, Top View

表 5-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|-----|---------------------|---|
| NAME | NO. | | |
| DREG | 1 | Digital Supply | Digital on-chip regulator output voltage for digital supply (1.5 V, nominal) |
| BCLK | 2 | Digital I/O | Audio serial data interface bus bit clock |
| FSYNC | 3 | Digital I/O | Audio serial data interface bus frame synchronization signal |
| DOUT | 4 | Digital I/O | Audio serial data interface bus output |
| DIN | 5 | Digital Input | Audio serial data interface bus input |
| IOVDD | 6 | Digital Supply | Digital I/O power supply (1.8 V or 3.3 V, nominal) |
| VSS | A2 | Ground | Ground Pin. Short directly to board Ground Plane. |
| SCL | 7 | Digital Input | Clock for I ² C Control Interface |
| SDA | 8 | Digital Input | Data for I ² C Control Interface |
| GPIO1 | 9 | Digital I/O | General-purpose digital input/output 0 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so forth) |
| GPIO2 | 10 | Digital I/O | General-purpose digital input/output 1 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so forth) |
| GPO1 | 11 | Digital Output | General-purpose digital output 1 (multipurpose functions such as audio data output, interrupt, and so forth) |
| GPI1 | 12 | Digital Input | General-purpose digital input 1 (multipurpose functions such as daisy-chain input, PLL input clock source, and so forth) |

表 5-1. Pin Functions (続き)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|---------|-----|---------------------|---|
| NAME | NO. | | |
| VSS | A3 | Ground | Ground Pin. Short directly to board Ground Plane. |
| ADDR | 13 | Analog Input | I2C Address |
| MICBIAS | 14 | Analog | MICBIAS Output (Programmable output upto 3V) |
| IN1P | 15 | Analog Input | Analog Input 1P Pin |
| IN1M | 16 | Analog Input | Analog Input 1M Pin |
| IN2P | 17 | Analog Input | Analog Input 2P Pin |
| IN2M | 18 | Analog Input | Analog Input 2M Pin |
| VSS | A4 | Ground | Ground Pin. Short directly to board Ground Plane. |
| OUT1M | 19 | Analog Output | Analog Output 1M Pin |
| OUT1P | 20 | Analog Output | Analog Output 1P Pin |
| OUT2P | 21 | Analog Output | Analog Output 2P Pin |
| OUT2M | 22 | Analog Output | Analog Output 2M Pin |
| AVDD | 23 | Analog Supply | Analog power (3.3 V, nominal) |
| VREF | 24 | Analog | Analog reference voltage filter output |
| VSS | A1 | Ground | Ground Pin. Short directly to board Ground Plane. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------------|---|------|-------------|------|
| Supply voltage | AVDD to AVSS | -0.3 | 3.9 | V |
| Supply voltage | IOVDD to VSS (thermal pad) | -0.3 | 3.9 | V |
| Ground voltage differences | AVSS to VSS (thermal pad) | -0.3 | 0.3 | V |
| Analog input voltage | Analog input pins voltage to AVSS | -0.3 | 5.656 | V |
| Digital input voltage | Digital input pins voltage to VSS (thermal pad) | -0.3 | IOVDD + 0.3 | V |
| Temperature | Functional ambient, T _A | -55 | 125 | °C |
| | Operating ambient, T _A | -40 | 125 | |
| | Junction, T _J | -40 | 150 | |
| | Storage, T _{stg} | -65 | 150 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V |
| V _(ESD) | Electrostatic discharge | Charged-device model (CDM), per AEC Q100-011 | ±500 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT | |
|---------------------|--|---|------|---------------|------|----|
| POWER | | | | | | |
| AVDD ⁽¹⁾ | Analog supply voltage to AVSS AVDD-3.3V Operation | | 3.0 | 3.3 | 3.6 | V |
| AVDD ⁽¹⁾ | Analog supply voltage to AVSS - AVDD 1.8V operation | | 1.65 | 1.8 | 1.95 | V |
| IOVDD | IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation | | 3.0 | 3.3 | 3.6 | V |
| | IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation | | 1.65 | 1.8 | 1.95 | |
| IOVDD | IO supply voltage to VSS (thermal pad) - IOVDD 1.2-V operation | | 1.08 | 1.2 | 1.32 | V |
| INPUTS | | | | | | |
| INxx | Analog input pins voltage to AVSS for line-in recording | Analog input pins voltage to AVSS for line-in recording | | 0 | 5.6 | V |
| INxx | Analog input pins voltage to AVSS for microphone recording | | 0.1 | MICBIAS – 0.1 | | V |
| | Digital input pins voltage to VSS (thermal pad) | | 0 | IOVDD | | V |
| ADDR | ADDR pin w.r.t AVSS | | 0 | AVDD | | V |
| TEMPERATURE | | | | | | |
| T _A | Operating ambient temperature | | -40 | | 125 | °C |

| | | MIN | NOM | MAX | UNIT |
|----------------|---|-----|-----|-----------------------|------|
| OTHERS | | | | | |
| | GPIOx or GPIx (used as MCLK input) clock frequency | | | 36.864 ⁽²⁾ | MHz |
| C _b | SCL and SDA bus capacitance for I ² C interface supports standard-mode and fast-mode | | | 400 | pF |
| | SCL and SDA bus capacitance for I ² C interface supports fast-mode plus | | | 550 | |
| C _L | Digital output load capacitance | | 20 | 50 | pF |

- (1) AVSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2 V.
 (2) MCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5 ns. For better audio noise performance, MCLK input must be used with low jitter.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TAC5212 | | UNIT |
|-------------------------------|--|------------|--|------|
| | | RGE (WQFN) | | |
| | | 28 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 38.4 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 26.3 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 15.9 | | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.5 | | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 15.8 | | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 13.8 | | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [spra953](#) application report.

6.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--|--|---|-----|-----|------------------|
| ADC PERFORMANCE FOR INPUT RECORDING | | | | | |
| | Differential input full-scale AC signal voltage | AC-coupled input | 2 | | V _{RMS} |
| | | DC-coupled input | 4 | | V _{RMS} |
| | Single-ended input full-scale AC signal voltage | AC-coupled input | 1 | | V _{RMS} |
| | | DC-coupled input | 2 | | V _{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 118 | dB |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | IN1 differential AC-coupled input selected and AC signal shorted to ground, 12-dB channel gain | | 103 | dB |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain, Device in High Common Mode Tolerance Mode (ADC_CH1_CM_TOL and ADC_CH2_CM_TOL=2'b10) | | 110 | dB |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | IN1 differential DC-coupled input selected and AC signal shorted to ground, 12-dB channel gain, Device in High Common Mode Tolerance Mode (ADC_CH1_CM_TOL and ADC_CH2_CM_TOL=2'b10) | | 98 | dB |
| SNR | Signal-to-noise ratio, A-weighted ^{(1) (2)} | Wideband Mode: IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (Integrated till 20KHz A-Weighted) | | | dB |

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $IOVDD = 3.3\text{ V}$, $f_{IN} = 1\text{-kHz}$ sinusoidal signal, $f_S = 48\text{ kHz}$, 32-bit audio data, $BCLK = 256 \times f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|-----------|---|---|-----|-----|-----|------|
| SNR | Signal-to-noise ratio ⁽¹⁾ ⁽²⁾ | Wideband Mode: IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain (Integrated till 100KHz) | | 91 | | dB |
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ ⁽²⁾ | Power Tune Mode: IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 106 | | dB |
| | | Power Tune Mode: IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 106 | | |
| | | Power Tune Mode: IN1 differential DC-coupled input selected and AC signal shorted to ground, 12-dB channel gain | | 94 | | |
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ ⁽²⁾ | 1.8V AVDD Operation: IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 110 | | dB |
| | | 1.8V AVDD Operation: IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 104 | | |
| | | 1.8V AVDD Operation: IN1 differential DC-coupled input selected and AC signal shorted to ground, 12-dB channel gain | | 92 | | |
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ ⁽²⁾ | 1.8V AVDD Operation + Power Tune Mode: IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 104 | | dB |
| | | 1.8V AVDD Operation + Power Tune Mode: IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain | | 100 | | |
| | | 1.8V AVDD Operation + Power Tune Mode: IN1 differential DC-coupled input selected and AC signal shorted to ground, 12-dB channel gain | | 88 | | |
| DR | Dynamic range, A-weighted ⁽²⁾ | IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 118 | | dB |
| | | IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 110 | | |
| | | IN1 differential DC-coupled input selected and –72-dB full-scale AC signal input, 12-dB channel gain | | 98 | | |
| DR | Dynamic range, A-weighted ⁽²⁾ | Power Tune Mode: IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 106 | | dB |
| | | Power Tune Mode: IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 106 | | |
| | | Power Tune Mode: IN1 differential DC-coupled input selected and –72-dB full-scale AC signal input, 12-dB channel gain | | 94 | | |

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $IOVDD = 3.3\text{ V}$, $f_{IN} = 1\text{-kHz}$ sinusoidal signal, $f_S = 48\text{ kHz}$, 32-bit audio data, $BCLK = 256 \times f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|--|---|-------|------|-----|------|
| DR | Dynamic range, A-weighted ⁽²⁾ | 1.8V AVDD Operation: IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | 106 | 110 | | dB |
| | | 1.8V AVDD Operation: IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 104 | | |
| | | 1.8V AVDD Operation: IN1 differential DC-coupled input selected and –72-dB full-scale AC signal input, 12-dB channel gain | | 92 | | |
| DR | Dynamic range, A-weighted ⁽²⁾ | 1.8V AVDD Operation + Power Tune Mode: IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 104 | | dB |
| | | 1.8V AVDD Operation + Power Tune Mode: IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain | | 100 | | |
| | | 1.8V AVDD Operation + Power Tune Mode: IN1 differential DC-coupled input selected and –72-dB full-scale AC signal input, 12-dB channel gain | | 88 | | |
| THD+N | Total harmonic distortion ⁽²⁾ | IN1 differential AC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain | | –95 | TBD | dB |
| | | IN1 differential DC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain | | –95 | | |
| | | IN1 differential DC-coupled input selected and –13-dB full-scale AC signal input, 12-dB channel gain | | –91 | | |
| ADC OTHER PARAMETERS | | | | | | |
| Input impedance | | Differential input, between INxP and INxM, 5kΩ Mode | | 5.5 | | kΩ |
| | | Differential input, between INxP and INxM, 10kΩ Mode | | 11 | | |
| | | Differential input, between INxP and INxM, 40kΩ Mode | | 44 | | |
| | | Single-ended input, between INxP and INxM, 5kΩ Mode | | 2.75 | | |
| | | Single-ended input, between INxP and INxM, 10kΩ Mode | | 5.5 | | |
| | | Single-ended input, between INxP and INxM, 40kΩ Mode | | 22 | | |
| Offset | | Shorted Input. | | TBD | | mV |
| Digital volume control range | | Programmable 0.5-dB steps | –80 | | 47 | dB |
| Input Signal Bandwidth | | Upto 192KSPS FS Rate | | 0.46 | | FS |
| | | >192KSPS | | 90 | | kHz |
| Output data sample rate | | Programmable | 3.675 | | 768 | kHz |
| Output data sample word length | | Programmable | 16 | | 32 | Bits |
| Digital high-pass filter cutoff frequency | | First-order IIR filter with programmable coefficients, –3-dB point (default setting) | | 2 | | Hz |
| Interchannel isolation | | –1-dB full-scale AC signal line-in input to non measurement channel | | –134 | | dB |
| Interchannel gain mismatch | | –6-dB full-scale AC signal line-in input, 0-dB channel gain | | 0.1 | | dB |

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $IOVDD = 3.3\text{ V}$, $f_{IN} = 1\text{-kHz}$ sinusoidal signal, $f_S = 48\text{ kHz}$, 32-bit audio data, $BCLK = 256 \times f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|--|---|---|-----------|-----|-------|-----|----------------------------|
| | Interchannel phase mismatch | 1-kHz sinusoidal signal | | | 0.01 | | Degrees |
| PSRR | Power-supply rejection ratio | 100-mV _{PP} , 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain | | | 92 | | dB |
| CMRR | Common-mode rejection ratio | Differential microphone input selected, 0-dB channel gain, 1-V _{RMS} AC input, 1-kHz signal on both pins and measure level at output, ADC_CHx_CFG0 D3-2 register bits set to 2b'10 to configure device in high CMRR performance mode | | | 80 | | dB |
| MICROPHONE BIAS | | | | | | | |
| | MICBIAS noise | BW = 20 Hz to 20 kHz, A-weighted, 1- μF capacitor between MICBIAS and AVSS | | | 2 | | μV_{RMS} |
| | MICBIAS voltage | Bypass to AVDD | | | AVDD | | V |
| | MICBIAS voltage | AVDD=1.8V | | | 1.375 | | V |
| | MICBIAS voltage | AVDD=3.3V | | | 2.75 | | V |
| Analog Bypass to Line Out/Head Phone Amplifier | | | | | | | |
| | Input impedance | Differential input, between INxP and INxM | | | 8.8 | | k Ω |
| | | Single-ended input, between INxP and INxM | | | 4.4 | | |
| | | Differential input, between INxP and INxM, 40k Mode | | | 40k | | |
| | | Single-ended input, between INxP and INxM, 40k Mode | | | 20k | | |
| | Single Ended Full Scale Output | AVDD=3.3V | AVDD=3.3V | | 1 | | V _{rms} |
| | Differential Full Scale Output | AVDD=3.3V | | | 2 | | V _{rms} |
| | | AVDD=1.8V | | | 1 | | V _{rms} |
| | Gain Error | | | | 0.1 | | dB |
| | Noise, A-Weighted | Idle Channel, AC Coupled Input Shorted to Ground, Fully Differential output | | | 4.5 | | μV_{RMS} |
| | Noise, A-Weighted | Idle Channel, AC Coupled Input Shorted to Ground, Single Ended output | | | 6.3 | | μV_{RMS} |
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ ⁽²⁾ | Idle Channel, AC Coupled Input Shorted to Ground, Fully Differential output, AVDD=3.3V | | | 113 | | dB |
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ ⁽²⁾ | Idle Channel, AC Coupled Input Shorted to Ground, Single Ended output, AVDD=3.3V | | | 104 | | dB |
| THD+N | Total harmonic distortion ⁽²⁾ | IN1 differential AC-coupled input selected and -1-dB full-scale AC signal input, 0-dB channel gain | | | -104 | | dB |
| DAC Performance for Line Output/Head Phone Playback | | | | | | | |
| | Full Scale Output Voltage | Differential output between OUTxP and OUTxM, AVDD=3.3V | | | 2 | | V _{RMS} |
| | | Differential Output between OUTxP and OUTxM, AVDD=1.8V | | | 1 | | |
| | | Single-ended Output, AVDD=3.3V | | | 1 | | |
| | | Single-ended Output, AVDD=1.8V | | | 0.5 | | |
| | | Pseudo Differential Output between OUTxP and OUTxM, AVDD=3.3V | | | 1 | | |
| | | Pseudo Differential Output between OUTxP and OUTxM, AVDD=1.8V | | | 0.5 | | |

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $IOVDD = 3.3\text{ V}$, $f_{IN} = 1\text{-kHz}$ sinusoidal signal, $f_S = 48\text{ kHz}$, 32-bit audio data, $BCLK = 256 \times f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|-------------------------------------|---|---|-----|-----|-----|----------|
| SNR | Signal-to-noise ratio, A-weighted ⁽¹⁾ ⁽²⁾ | Differential Output, 0dBFS Signal, AVDD=3.3V | | 119 | | dB |
| | | Single Ended Output, 0dBFS Signal, AVDD=3.3V | | 111 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V | | 110 | | |
| | | Differential Output, 0dBFS Signal, AVDD=1.8V | | 114 | | |
| | | Single Ended Output, 0dBFS Signal, AVDD=1.8V | | 105 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=1.8V | | 104 | | |
| | | Differential Output, 0dBFS Signal, AVDD=3.3V, 0dBFS Signal, Power Tune Mode | | 112 | | |
| | | Single Ended Output, 0dBFS Signal, AVDD=3.3V, Power Tune Mode | | 102 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V, Power Tune Mode | | 101 | | |
| | | Differential Output, 0dBFS Signal, AVDD=1.8V, Power Tune Mode | | 108 | | |
| | | Single Ended Output, 0dBFS Signal, AVDD=1.8V, Power Tune Mode | | 97 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=1.8V, Power Tune Mode | | 96 | | |
| DR | Dynamic range, A-weighted ⁽²⁾ | Differential Output, -60dBFS Signal, AVDD=3.3V | | 119 | | dB |
| | | Single Ended Output, -60dBFS Signal, AVDD=3.3V | | 111 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V | | 110 | | |
| | | Differential Output, -60dBFS Signal, AVDD=1.8V | | 114 | | |
| | | Single Ended Output, -60dBFS Signal, AVDD=1.8V | | 105 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=1.8V | | 104 | | |
| | | Differential Output, -60dBFS Signal, AVDD=3.3V, 0dBFS Signal, Power Tune Mode | | 112 | | |
| | | Single Ended Output, -60dBFS Signal, AVDD=3.3V, Power Tune Mode | | 102 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V, Power Tune Mode | | 101 | | |
| | | Differential Output, -60dBFS Signal, AVDD=1.8V, Power Tune Mode | | 108 | | |
| | | Single Ended Output, -60dBFS Signal, AVDD=1.8V, Power Tune Mode | | 97 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=1.8V, Power Tune Mode | | 96 | | |
| THD+N | Total harmonic distortion ⁽²⁾ | | | -95 | | dB |
| | Head Phone Load Range | | | 16 | | Ω |
| | Line Out Load Range | | 600 | | | Ω |
| | Channel gain control range | Programmable 1-dB steps | -6 | | 12 | dB |
| DAC Channel OTHER PARAMETERS | | | | | | |
| | Output Offset | 0 Input, Fully Differential Output | | 0.5 | | mV |

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $IOVDD = 3.3\text{ V}$, $f_{IN} = 1\text{-kHz}$ sinusoidal signal, $f_S = 48\text{ kHz}$, 32-bit audio data, $BCLK = 256 \times f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|---|---|---|--------------|--------------|---------|----|
| Output Offset | 0 Input, Pseudo Differential Output | | 0.4 | | mV | |
| Output Common Mode | Common Mode Level for OUTxP and OUTxM AVDD=1.8V (Register Configurable) | | 0.9 | | V | |
| Output Common Mode | Common Mode Level for OUTxP and OUTxM AVDD=3.3V (Register Configurable) | | 1.65 | | V | |
| Common Mode Error | DC Error in Common Mode Voltage | | ±20 | | mV | |
| Digital volume control range | Programmable 0.5-dB steps | -120 | | 42 | dB | |
| Output Signal Bandwidth | Upto 192KSPS FS Rate | | 0.46 | | FS | |
| | >192KSPS | | 100 | | kHz | |
| Input data sample rate | Programmable | 3.675 | | 768 | kHz | |
| Input data sample word length | Programmable | 16 | | 32 | Bits | |
| Digital high-pass filter cutoff frequency | First-order IIR filter with programmable coefficients, -3-dB point (default setting) | | 2 | | Hz | |
| Interchannel isolation | | | -134 | | dB | |
| Interchannel gain mismatch | | | 0.1 | | dB | |
| Interchannel phase mismatch | 1-kHz sinusoidal signal | | 0.01 | | Degrees | |
| PSRR | Power-supply rejection ratio | 100-mV _{PP} , 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain | | 100 | | dB |
| | Mute Attenuation | | | -130 | | dB |
| P _{out} | Output Power Delivery | Single ended/Pseudo Differential R _L =16 Ohms, THD+N<1% | | 62.5 | | mW |
| DIGITAL I/O | | | | | | |
| V _{IL(SHDNZ)} | Low-level digital input logic voltage threshold | SHDNZ pin | -0.3 | 0.25 × IOVDD | V | |
| V _{IH(SHDNZ)} | High-level digital input logic voltage threshold | SHDNZ pin | 0.75 × IOVDD | IOVDD + 0.3 | V | |
| V _{IL} | Low-level digital input logic voltage threshold | All digital pins except SDA and SCL, IOVDD 1.8-V operation | -0.3 | 0.35 × IOVDD | V | |
| | | All digital pins except SDA and SCL, IOVDD 3.3-V operation | -0.3 | 0.8 | | |
| V _{IH} | High-level digital input logic voltage threshold | All digital pins except SDA and SCL, IOVDD 1.8-V operation | 0.65 × IOVDD | IOVDD + 0.3 | V | |
| | | All digital pins except SDA and SCL, IOVDD 3.3-V operation | 2 | IOVDD + 0.3 | | |
| V _{OL} | Low-level digital output voltage | All digital pins except SDA and SCL, I _{OL} = -2 mA, IOVDD 1.8-V operation | | 0.45 | V | |
| | | All digital pins except SDA and SCL, I _{OL} = -2 mA, IOVDD 3.3-V operation | | 0.4 | | |
| V _{OH} | High-level digital output voltage | All digital pins except SDA and SCL, I _{OH} = 2 mA, IOVDD 1.8-V operation | IOVDD - 0.45 | | V | |
| | | All digital pins except SDA and SCL, I _{OH} = 2 mA, IOVDD 3.3-V operation | 2.4 | | | |
| V _{IL(I2C)} | Low-level digital input logic voltage threshold | SDA and SCL | -0.5 | 0.3 × IOVDD | V | |
| V _{IH(I2C)} | High-level digital input logic voltage threshold | SDA and SCL | 0.7 × IOVDD | IOVDD + 0.5 | V | |

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $IOVDD = 3.3\text{ V}$, $f_{IN} = 1\text{-kHz}$ sinusoidal signal, $f_S = 48\text{ kHz}$, 32-bit audio data, $BCLK = 256 \times f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|----------------|---|--|-----|-----|--------------------|---------------|
| $V_{OL1(I2C)}$ | Low-level digital output voltage | SDA, $I_{OL(I2C)} = -3\text{ mA}$, $IOVDD > 2\text{ V}$ | | | 0.4 | V |
| $V_{OL2(I2C)}$ | Low-level digital output voltage | SDA, $I_{OL(I2C)} = -2\text{ mA}$, $IOVDD \leq 2\text{ V}$ | | | $0.2 \times IOVDD$ | V |
| $I_{OL(I2C)}$ | Low-level digital output current | SDA, $V_{OL(I2C)} = 0.4\text{ V}$, standard-mode or fast-mode | 3 | | | mA |
| | | SDA, $V_{OL(I2C)} = 0.4\text{ V}$, fast-mode plus | 20 | | | |
| I_{IL} | Input logic-low leakage for digital inputs | All digital pins, input = 0 V | -5 | 0.1 | 5 | μA |
| I_{IH} | Input logic-high leakage for digital inputs | All digital pins, input = $IOVDD$ | -5 | 0.1 | 5 | μA |
| C_{IN} | Input capacitance for digital inputs | All digital pins | | 5 | | pF |
| R_{PD} | Pulldown resistance for digital I/O pins when asserted on | | | 20 | | k Ω |

TYPICAL SUPPLY CURRENT CONSUMPTION

| | | | | | | |
|-------------|---|---|------|--|--|---------------|
| I_{AVDD} | Current consumption in sleep mode (software shutdown mode) | All device external clocks stopped | TBD | | | μA |
| I_{IOVDD} | | | 1 | | | |
| I_{AVDD} | Current consumption when MICBIAS ON, MICBIAS voltage 10 V, 30 mA load, ADC off | $f_S = 48\text{ kHz}$, $BCLK = 256 \times f_S$ | TBD | | | mA |
| I_{IOVDD} | | | 0.01 | | | |
| I_{AVDD} | Current consumption with ADC 2-channel operation at f_S 16-kHz, MICBIAS off, PLL on, $BCLK = 512 \times f_S$ | | TBD | | | mA |
| I_{IOVDD} | | | 0.1 | | | |
| I_{AVDD} | Current consumption with ADC 2-channel operation at f_S 48-kHz, MICBIAS on, PLL off, $BCLK = 512 \times f_S$ | | TBD | | | mA |
| I_{IOVDD} | | | 0.1 | | | |
| I_{AVDD} | Current consumption with DAC to HP 2-channel operation at f_S 16-kHz, MICBIAS off, PLL on, $BCLK = 512 \times f_S$ | | TBD | | | mA |
| I_{IOVDD} | | | 0.2 | | | |
| I_{AVDD} | Current consumption with DAC to HP 2-channel operation at f_S 48-kHz, MICBIAS off, PLL off, $BCLK = 512 \times f_S$ | | TBD | | | mA |
| I_{IOVDD} | | | TBD | | | |

- (1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
- (2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

6.6 Timing Requirements: I²C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see TBD for timing diagram

| | | MIN | NOM | MAX | UNIT |
|-----------------------|--|------|----------------------------|------|------|
| STANDARD-MODE | | | | | |
| f _{SCL} | SCL clock frequency | 0 | | 100 | kHz |
| t _{HD,STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4 | | | μs |
| t _{LOW} | Low period of the SCL clock | 4.7 | | | μs |
| t _{HIGH} | High period of the SCL clock | 4 | | | μs |
| t _{SU,STA} | Setup time for a repeated START condition | 4.7 | | | μs |
| t _{HD,DAT} | Data hold time | 0 | | 3.45 | μs |
| t _{SU,DAT} | Data setup time | 250 | | | ns |
| t _r | SDA and SCL rise time | | | 1000 | ns |
| t _f | SDA and SCL fall time | | | 300 | ns |
| t _{SU,STO} | Setup time for STOP condition | 4 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 4.7 | | | μs |
| FAST-MODE | | | | | |
| f _{SCL} | SCL clock frequency | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6 | | | μs |
| t _{LOW} | Low period of the SCL clock | 1.3 | | | μs |
| t _{HIGH} | High period of the SCL clock | 0.6 | | | μs |
| t _{SU,STA} | Setup time for a repeated START condition | 0.6 | | | μs |
| t _{HD,DAT} | Data hold time | 0 | | 0.9 | μs |
| t _{SU,DAT} | Data setup time | 100 | | | ns |
| t _r | SDA and SCL rise time | 20 | | 300 | ns |
| t _f | SDA and SCL fall time | | 20 × (IOVDD / 5.5 V) | 300 | ns |
| t _{SU,STO} | Setup time for STOP condition | 0.6 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 1.3 | | | μs |
| FAST-MODE PLUS | | | | | |
| f _{SCL} | SCL clock frequency | 0 | | 1000 | kHz |
| t _{HD,STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26 | | | μs |
| t _{LOW} | Low period of the SCL clock | 0.5 | | | μs |
| t _{HIGH} | High period of the SCL clock | 0.26 | | | μs |
| t _{SU,STA} | Setup time for a repeated START condition | 0.26 | | | μs |
| t _{HD,DAT} | Data hold time | 0 | | | μs |
| t _{SU,DAT} | Data setup time | 50 | | | ns |
| t _r | SDA and SCL Rise Time | | | 120 | ns |
| t _f | SDA and SCL Fall Time | | 20 × (IOVDD / 5.5 V) | 120 | ns |
| t _{SU,STO} | Setup time for STOP condition | 0.26 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 0.5 | | | μs |

6.7 Switching Characteristics: I²C Interface

 at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see TBD for timing diagram

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|------------------|-----------------|-----|-----|------|------|
| t _d (SDA) | SCL to SDA delay | Standard-mode | 200 | | 1250 | ns |
| | | Fast-mode | 200 | | 850 | ns |
| | | Fast-mode plus | | | 400 | ns |

6.8 Timing Requirements: SPI Interface

 at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

| | | MIN | NOM | MAX | UNIT |
|-------------------------|---------------------------|---------------------|-----|-----|------|
| t _i (SCLK) | SCLK period | 40 | | | ns |
| t _H (SCLK) | SCLK high pulse duration | 18 | | | ns |
| t _L (SCLK) | SCLK low pulse duration | 18 | | | ns |
| t _{LEAD} | Enable lead time | 16 | | | ns |
| t _{TRAIL} | Enable trail time | 16 | | | ns |
| t _{DSEQ} | Sequential transfer delay | 20 | | | ns |
| t _{SU} (PICO) | PICO data setup time | 8 | | | ns |
| t _{HLD} (PICO) | PICO data hold time | 8 | | | ns |
| t _r (SCLK) | SCLK rise time | 10% - 90% rise time | | 6 | ns |
| t _f (SCLK) | SCLK fall time | 90% - 10% fall time | | 6 | ns |

6.9 Switching Characteristics: SPI Interface

 at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--------------------|---|-----|-----|-----|------|
| t _a (MISO) | MISO access time | IOVDD = 1.8 V | | | 18 | ns |
| | | IOVDD = 3.3 V | | | 14 | |
| t _d (MISO) | SCLK to MISO delay | 50% of SCLK to 50% of MISO, IOVDD = 1.8 V | | | 19 | ns |
| | | 50% of SCLK to 50% of MISO, IOVDD = 3.3 V | | | 15 | |
| t _{dis} (MISO) | MISO disable time | IOVDD = 1.8 V | | | 18 | ns |
| | | IOVDD = 3.3 V | | | 14 | |

6.10 Timing Requirements: TDM, I²S or LJ Interface

 at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

| | | MIN | NOM | MAX | UNIT |
|--------------------------|---|---------------------|-----|-----|------|
| t _i (BCLK) | BCLK period | 40 | | | ns |
| t _H (BCLK) | BCLK high pulse duration ⁽¹⁾ | 18 | | | ns |
| t _L (BCLK) | BCLK low pulse duration ⁽¹⁾ | 18 | | | ns |
| t _{SU} (FSYNC) | FSYNC setup time | 8 | | | ns |
| t _{HLD} (FSYNC) | FSYNC hold time | 8 | | | ns |
| t _{SU} (DIN) | DIN setup time | 8 | | | ns |
| t _{HLD} (DIN) | DIN hold time | 8 | | | ns |
| t _r (BCLK) | BCLK rise time | 10% - 90% rise time | | 10 | ns |
| t _f (BCLK) | BCLK fall time | 90% - 10% fall time | | 10 | ns |

- (1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

6.11 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|---|-----|--------|------|
| t _d (SDOUT-BCLK) | BCLK to SDOUT delay | 50% of BCLK to 50% of SDOUT, IOVDD = 1.8 V | | 18 | ns |
| | | 50% of BCLK to 50% of SDOUT, IOVDD = 3.3 V | | 14 | |
| t _d (SDOUT-FSYNC) | FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0) | 50% of FSYNC to 50% of SDOUT, IOVDD = 1.8 V | | 18 | ns |
| | | 50% of FSYNC to 50% of SDOUT, IOVDD = 3.3 V | | 14 | |
| f _(BCLK) | BCLK output clock frequency; master mode (1) | | | 24.576 | MHz |
| t _H (BCLK) | BCLK high pulse duration; master mode | IOVDD = 1.8 V | 14 | | ns |
| | | IOVDD = 3.3 V | 14 | | |
| t _L (BCLK) | BCLK low pulse duration; master mode | IOVDD = 1.8 V | 14 | | ns |
| | | IOVDD = 3.3 V | 14 | | |
| t _d (FSYNC) | BCLK to FSYNC delay; master mode | 50% of BCLK to 50% of FSYNC, IOVDD = 1.8 V | | 18 | ns |
| | | 50% of BCLK to 50% of FSYNC, IOVDD = 3.3 V | | 14 | |
| t _r (BCLK) | BCLK rise time; master mode | 10% - 90% rise time, IOVDD = 1.8 V | | 10 | ns |
| | | 10% - 90% rise time, IOVDD = 3.3 V | | 10 | |
| t _f (BCLK) | BCLK fall time; master mode | 90% - 10% fall time, IOVDD = 1.8 V | | 8 | ns |
| | | 90% - 10% fall time, IOVDD = 3.3 V | | 8 | |

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

6.12 Timing Requirements: PDM Digital Microphone Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------------|-------------------|-----|-----|-----|------|
| t _{SU} (PDMINx) | PDMINx setup time | 30 | | | ns |
| t _{HLD} (PDMINx) | PDMINx hold time | TBD | | | ns |

6.13 Switching Characteristics: PDM Digital Microphone Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|----------------------------|---------------------|-----|-------|------|
| f _(PDMCLK) | PDMCLK clock frequency | 0.768 | | 6.144 | MHz |
| t _H (PDMCLK) | PDMCLK high pulse duration | 72 | | | ns |
| t _L (PDMCLK) | PDMCLK low pulse duration | 72 | | | ns |
| t _r (PDMCLK) | PDMCLK rise time | 10% - 90% rise time | | 8 | ns |
| t _f (PDMCLK) | PDMCLK fall time | 90% - 10% fall time | | 8 | ns |

6.14 Timing Diagrams

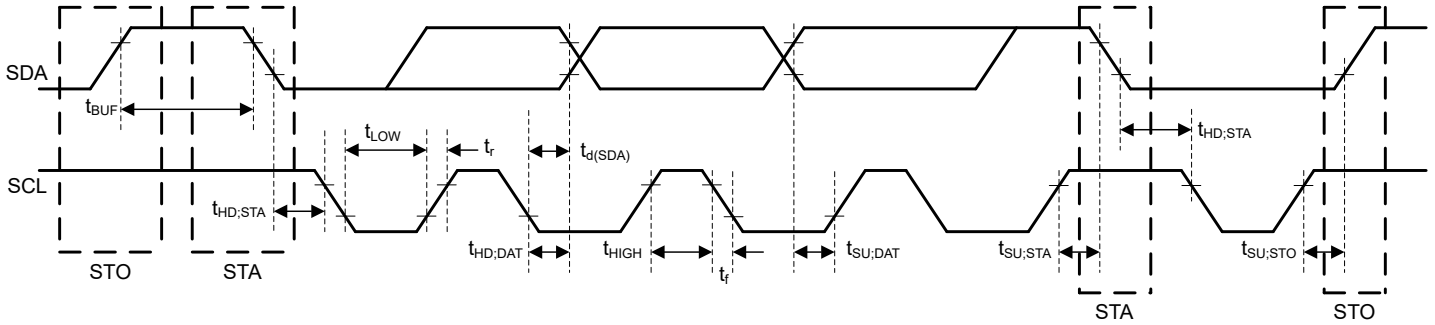


图 6-1. I²C Interface Timing Diagram

ADVANCE INFORMATION

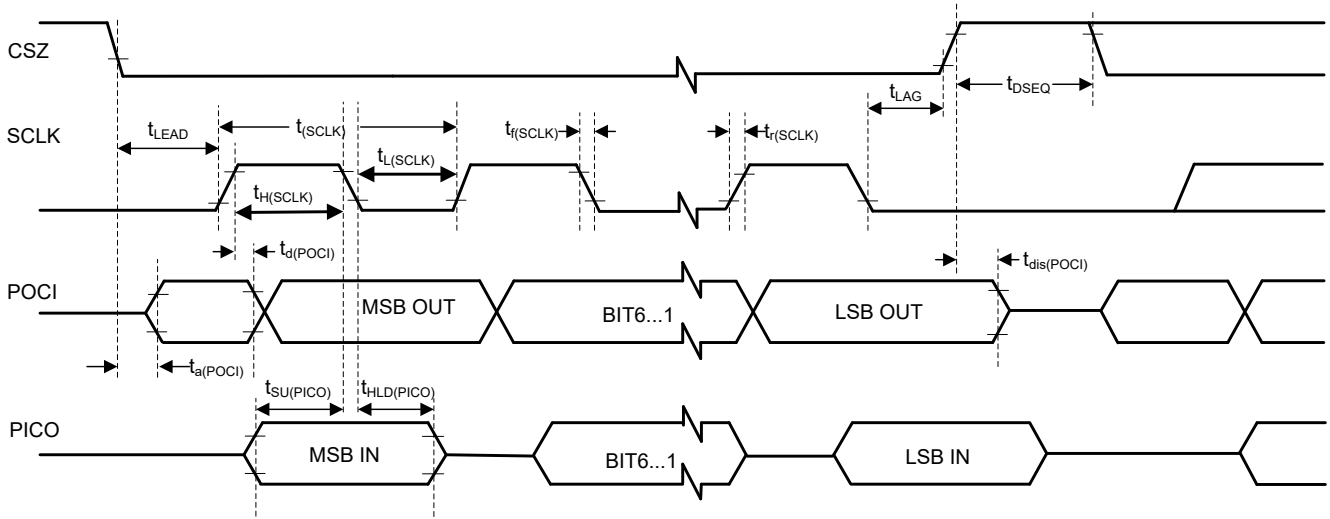


图 6-2. SPI Interface Timing Diagram

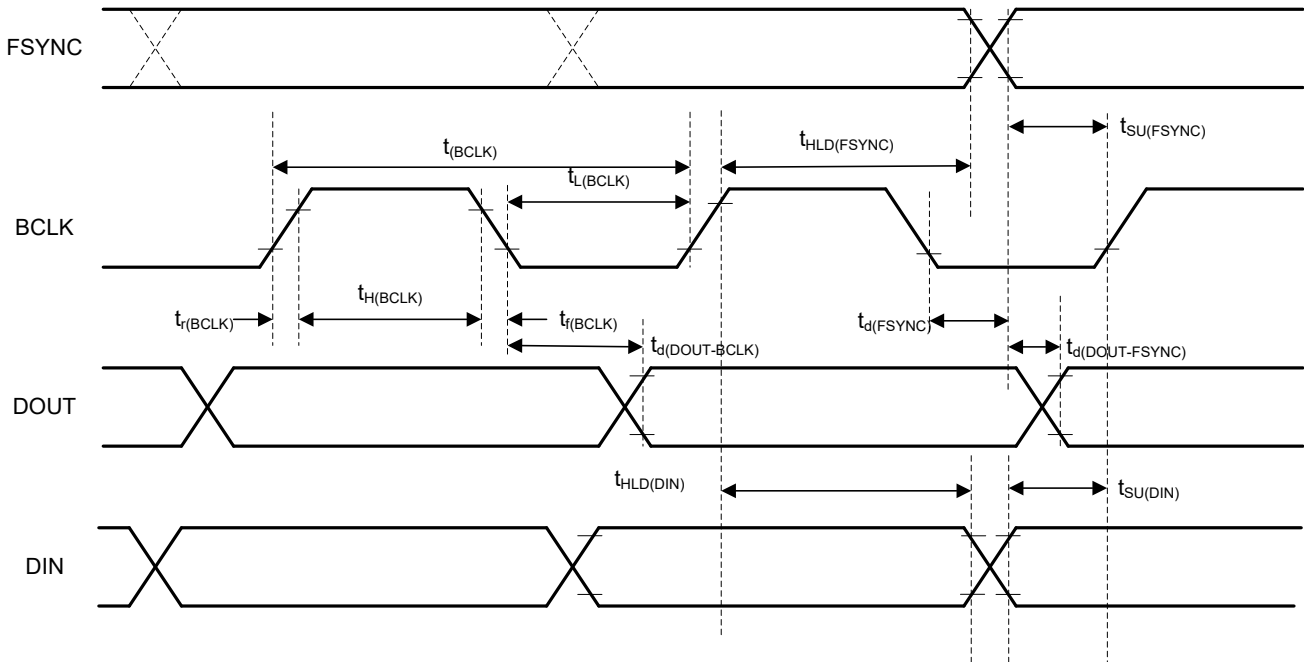


図 6-3. TDM (With BCLK_POL = 1), I²S, and LJ Interface Timing Diagram

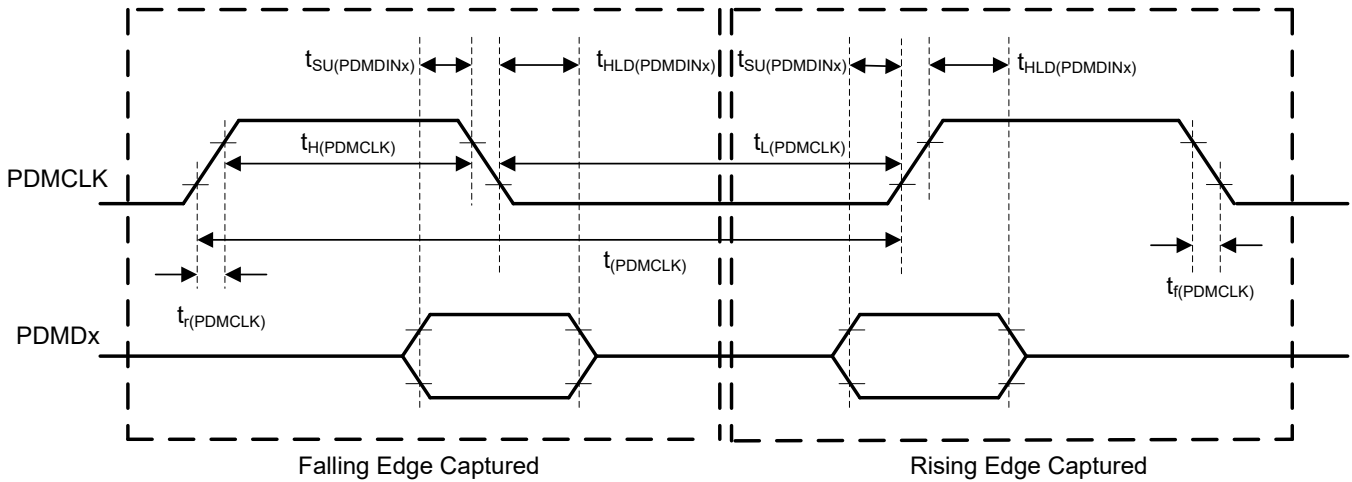


図 6-4. PDM Digital Microphone Interface Timing Diagram

7 Detailed Description

7.1 Overview

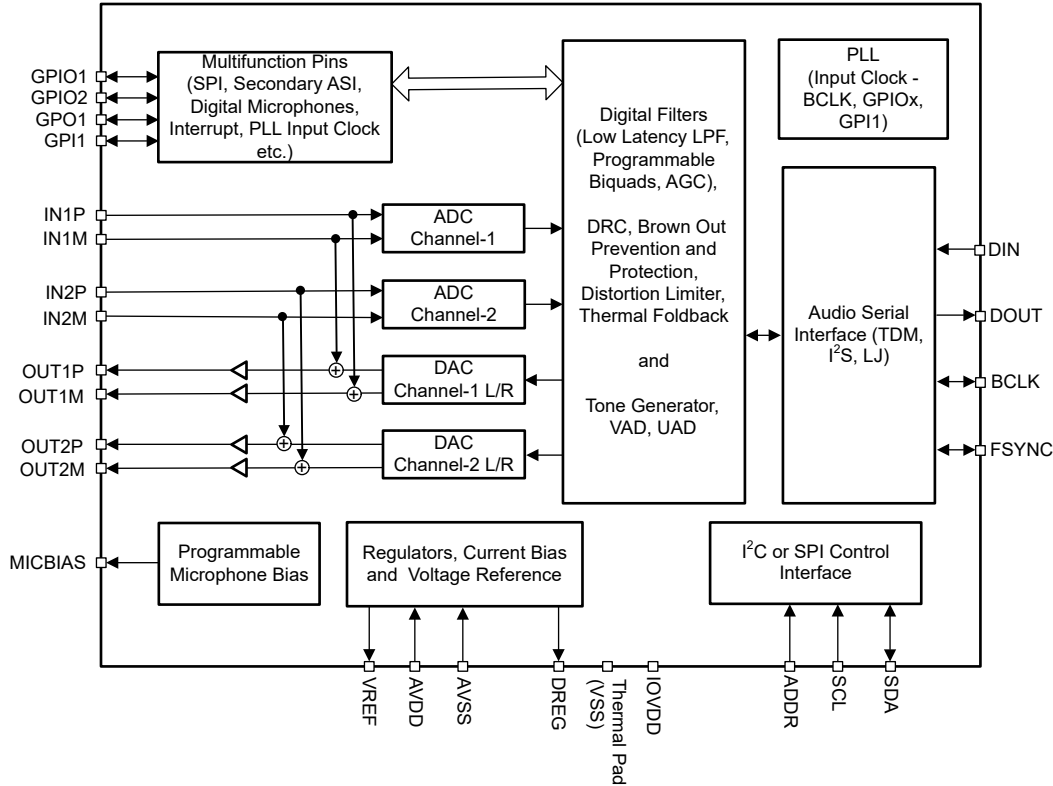
The TAC5212 is from a scalable family of devices. As part of the extended family of devices, the TAC5212 consists of a high-performance, low-power, flexible, mono/stereo, audio analog-to-digital converter (ADC) and audio digital-to-analog converter (DAC) with extensive feature integration. This device is intended for automotive applications such as ruggedized communication equipment, IP network cameras, Professional Audio, and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration registers across extended families make this device well-suited for scalable system designs.

The TAC5212 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma ($\Delta\Sigma$) ADCs
- Configurable single-ended or differential audio inputs with 2Vrms signal swing
- Low-noise programmable microphone bias output
- 2-channel, multibit, high-performance delta-sigma ($\Delta\Sigma$) DACs
- Configurable single-ended, differential, or pseudo-differential audio outputs
- Over Current Diagnostics and Protection for MICBIAS and analog outputs
- Automatic gain controller (AGC)
- Advanced Thermal foldback and protection
- Advanced Battery guard and distortion limiter
- Programmable decimation filters with linear-phase or low-latency filter
- Programmable channel gain, volume control, and biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF) and digital channel mixer
- Pulse density modulation (PDM) digital microphone interface with a high-performance decimation filter
- Dual I²S or TDM Interface with Independent Sample Rate(Synchronous)
- Synchronous Sample Rate Converter(SRC)
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the TAC5212 for configuring the control registers is supported using an I²C and SPI interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I²S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

7.2 Functional Block Diagram



☒ 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

7.3.1.1 Control Serial Interfaces

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. All these registers can be accessed using either I²C or SPI communication to the device. For more information, see the [セクション 7.5](#) section.

7.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAC5212 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I²S or left-justified protocols format, programmable data length options, very flexible controller-target configurability for bus clock lines, and the ability to communicate with multiple devices within a system directly.

The TAC5212 supports up to two ASI Interfaces. Secondary ASI Clock and Data Pins can be configured by setting GPIO's. Frame Sync of two ASI's must be synchronous. See the for more details on Secondary ASI.

The bus protocol TDM, I²S, or left-justified (LJ) format can be selected for primary ASI by using the PASI_FORMAT[1:0], P0_R26_D[7:6] register bits. As shown in 表 7-1 and 表 7-2, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the PASI_WLEN[1:0], P0_R26_D[5:4] register bits.

表 7-1. Primary Audio Serial Interface Format

| P0_R26_D[7:6] : PASI_FORMAT[1:0] | PRIMARY AUDIO SERIAL INTERFACE FORMAT |
|----------------------------------|--|
| 00 (default) | Time-division multiplexing (TDM) mode |
| 01 | Inter IC sound (I ² S) mode |
| 10 | Left-justified (LJ) mode |
| 11 | Reserved (do not use this setting) |

表 7-2. Primary Audio Serial Interface Data Word-Length

| P0_R7_D[5:4] : PASI_WLEN[1:0] | PRIMARY AUDIO OUTPUT CHANNEL DATA WORD-LENGTH |
|-------------------------------|---|
| 00 | Data word-length set to 16 bits |
| 01 | Data word-length set to 20 bits |
| 10 | Data word-length set to 24 bits |
| 11 (default) | Data word-length set to 32 bits |

The frame sync pin, FSYNC, is used in this audio bus protocol to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit-clock cycles in a frame must accommodate multiple device active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 32) to allow all input/output channel audio data transmissions to be completed on the audio bus by a device or multiple devices sharing the same audio bus. The device supports up to eight input channels and eight output channels that can be configured on the primary ASI bus to place their audio data on bus slot 0 to slot 31. 表 7-3 lists the output channel-1 slot configuration settings. In I²S and LJ mode, the slots are divided into two sets, left-channel slots, and right-channel slots, as described in the セクション 7.3.1.2.2 and セクション 7.3.1.2.3 sections.

表 7-3. Output Channel-1 Slot Assignment Settings

| P0_R30_D[4:0] : PASI_TX_CH1_SLOT[4:0] | OUTPUT CHANNEL 1 SLOT ASSIGNMENT |
|---------------------------------------|---|
| 0 0000 = 0d (default) | Slot 0 for TDM or left slot 0 for I ² S, LJ. |
| 0 0001 = 1d | Slot 1 for TDM or left slot 1 for LJ. |
| ... | ... |
| 0 1111 = 15d | Slot 15 for TDM or left slot 15 for LJ. |
| 1 0000 = 32d | Slot 16 for TDM or right slot 0 for I ² S, LJ. |
| ... | ... |
| 1 1110 = 30d | Slot 30 for TDM or right slot 14 for LJ. |
| 1 1111 = 31d | Slot 31 for TDM or right slot 15 for LJ. |

Similarly, the slot assignment setting for output channel 2 to channel 8 can be done using the PASI_TX_CH2_SLOT (P0_R31) to PASI_TX_CH8_SLOT (P0_R37) registers and for input channel 1 to channel 8 by using the PASI_RX_CH1_SLOT (P0_R40) to PAS_RX_CH8_SLOT (P0_R47), respectively.

The slot word length is the same as the primary ASI channel word length set for the device. The output channel data word length must be set to the same value for all TAC5212 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.

The device also includes a feature that offsets the start of the slot data transfer concerning the frame sync by up to 31 cycles of the bit clock. Offset can be configured independently for input and output data paths. 表 7-4 and 表 7-5 lists the programmable offset configuration settings for transmission and receive paths respectively.

表 7-4. Programmable Offset Settings for the ASI Slot Start for transmission

| P0_R28_D[4:0] : PASI_TX_OFFSET[4:0] | PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START |
|-------------------------------------|---|
| 0 0000 = 0d (default) | The device follows the standard protocol timing without any offset. |
| 0 0001 = 1d | Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I ² S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing. |
| | |
| 1 1110 = 30d | Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I ² S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. |
| 1 1111 = 31d | Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I ² S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. |

表 7-5. Programmable Offset Settings for the ASI Slot Start for Receive

| P0_R38_D[4:0] : PASI_RX_OFFSET[4:0] | PROGRAMMABLE OFFSET SETTING FOR SLOT DATA RECEIVE START |
|-------------------------------------|---|
| 0 0000 = 0d (default) | The device follows the standard protocol timing without any offset. |
| 0 0001 = 1d | Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I ² S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing. |
| | |
| 1 1110 = 30d | Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I ² S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. |
| 1 1111 = 31d | Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I ² S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. |

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the PASI_FSYNC_POL, P0_R26_D3 register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the PASI_BCLK_POL, P0_R26_D2 register bit.

In addition, the word clock and bit clock can be independently configured in either Controller or Target mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

7.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. 図 7-2 to 図 7-5 illustrate the protocol timing for TDM operation with various configurations.

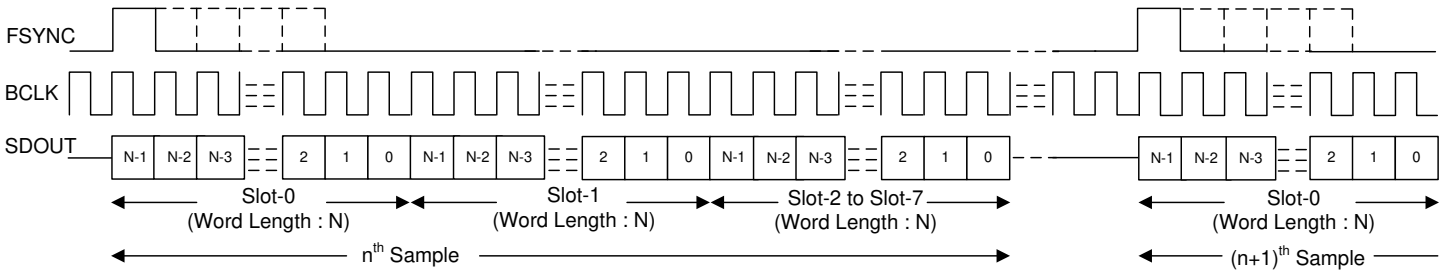


図 7-2. TDM Mode Standard Protocol Timing ($PASI_TX_OFFSET = 0$)

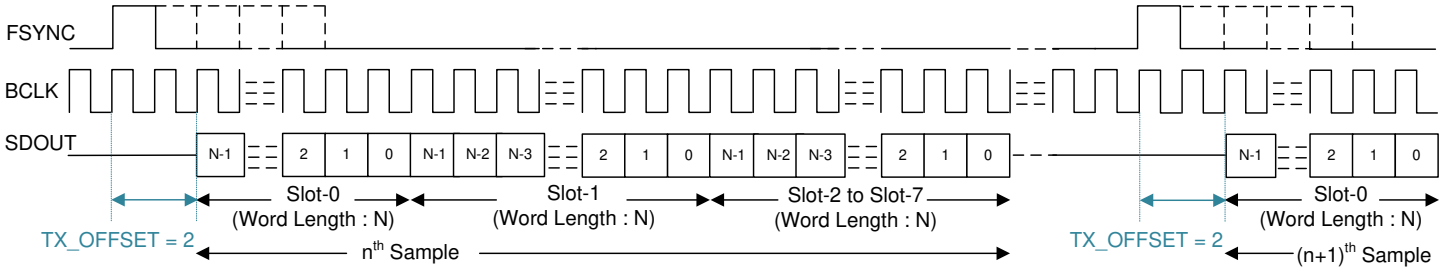


図 7-3. TDM Mode Protocol Timing ($PASI_TX_OFFSET = 2$)

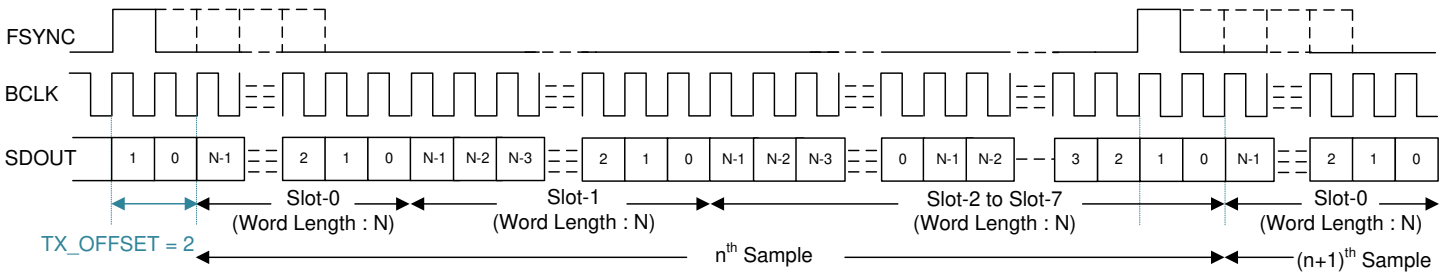


図 7-4. TDM Mode Protocol Timing (No Idle BCLK Cycles, $PASI_TX_OFFSET = 2$)

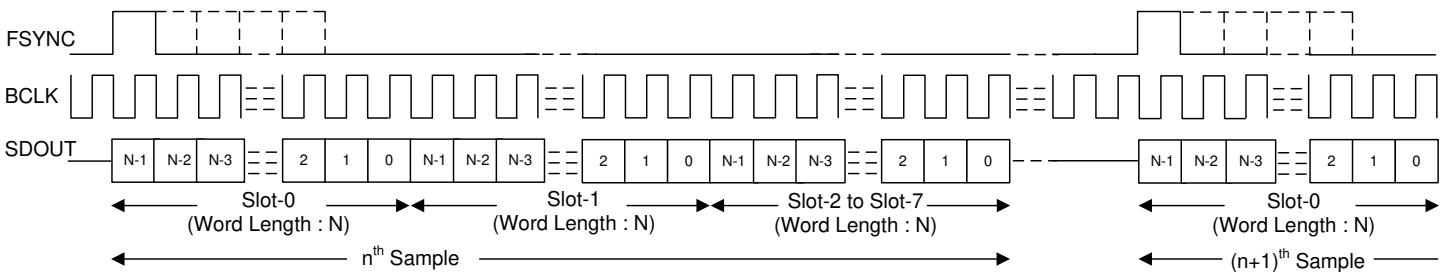


図 7-5. TDM Mode Protocol Timing ($PASI_TX_OFFSET = 0$ and $PASI_BCLK_POL = 1$)

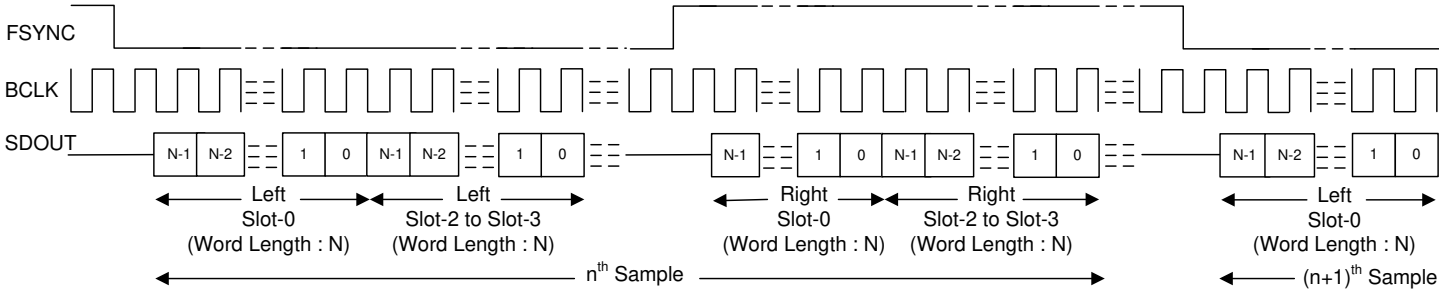
For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a $PASI_TX_OFFSET$ value higher than 0 is recommended.

7.3.1.2.2 Inter IC Sound (I²S) Interface

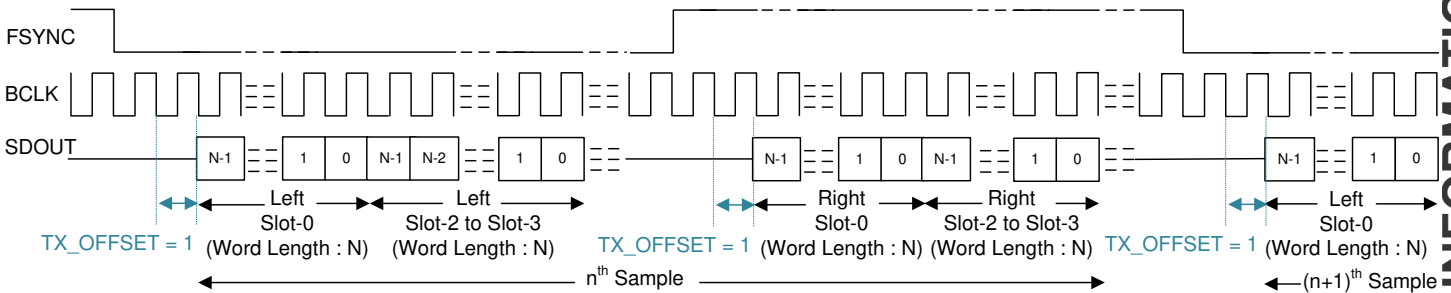
The standard I²S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I²S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the falling edge of FSYNC. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of

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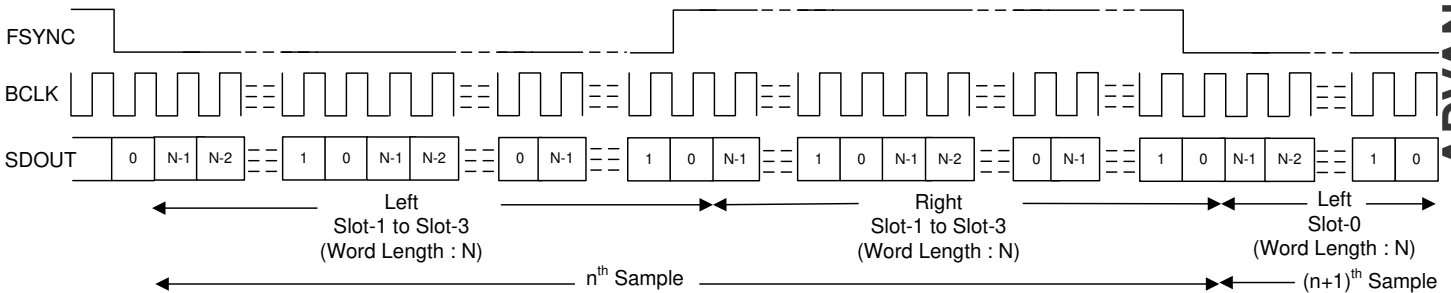
BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. 7-6 to 7-9 illustrate the protocol timing for I²S operation with various configurations.



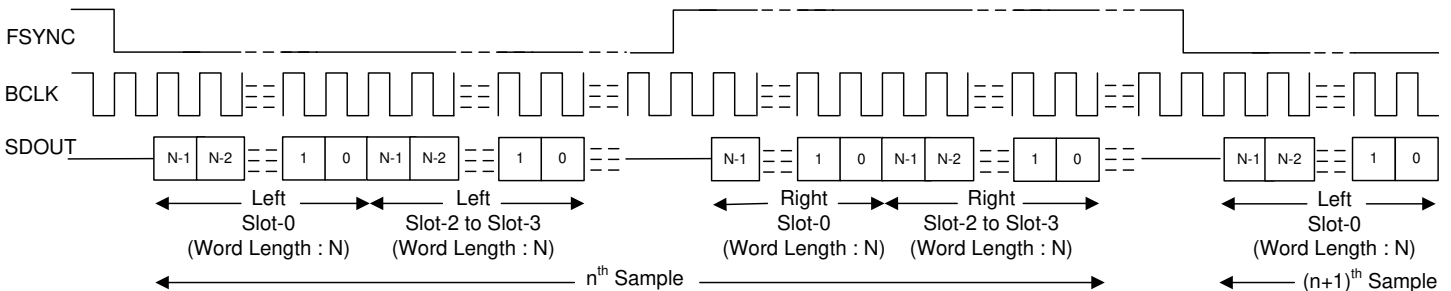
7-6. I²S Mode Standard Protocol Timing (PASI_TX_OFFSET = 0)



7-7. I²S Protocol Timing (PASI_TX_OFFSET = 1)



7-8. I²S Protocol Timing (No Idle BCLK Cycles, PASI_TX_OFFSET = 0)




7-9. I²S Protocol Timing (PASI_TX_OFFSET = 0 and PASI_BCLK_POL = 1)

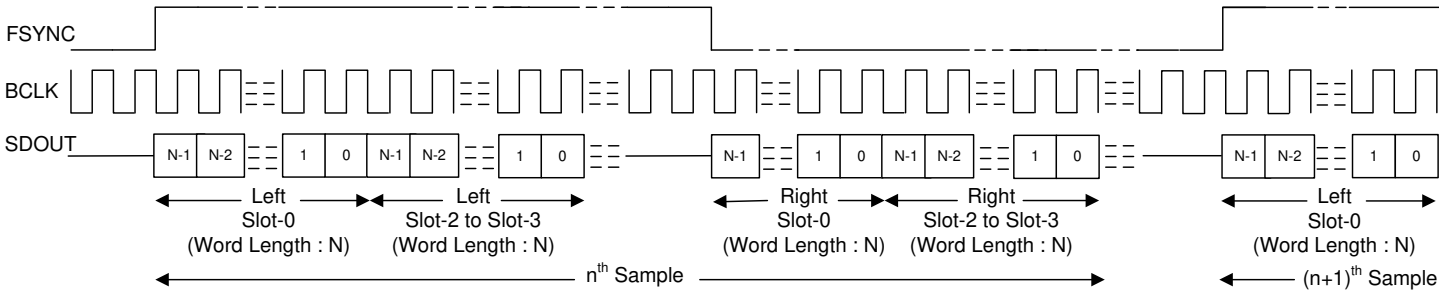
For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be several BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high pulse

must be several BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

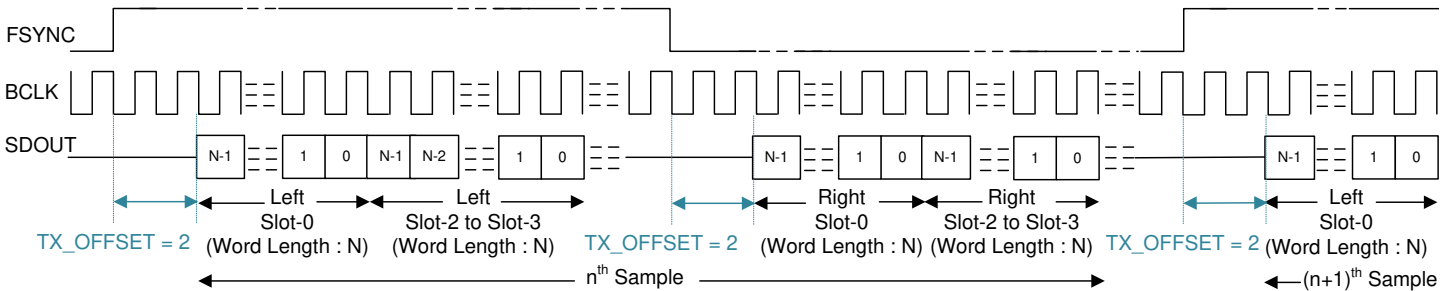
7.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK.  illustrate the protocol timing for LJ operation with various configurations.

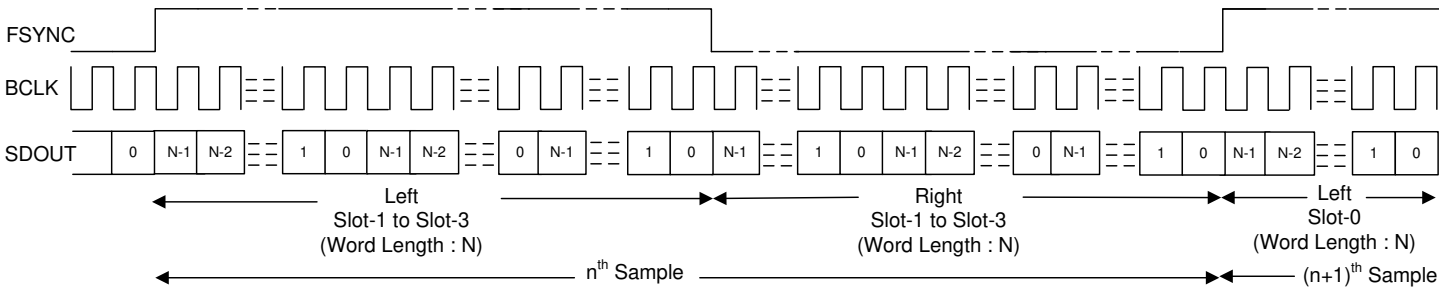
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 7-10. LJ Mode Standard Protocol Timing (TX_OFFSET = 0)



 7-11. LJ Protocol Timing (TX_OFFSET = 2)



 7-12. LJ Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

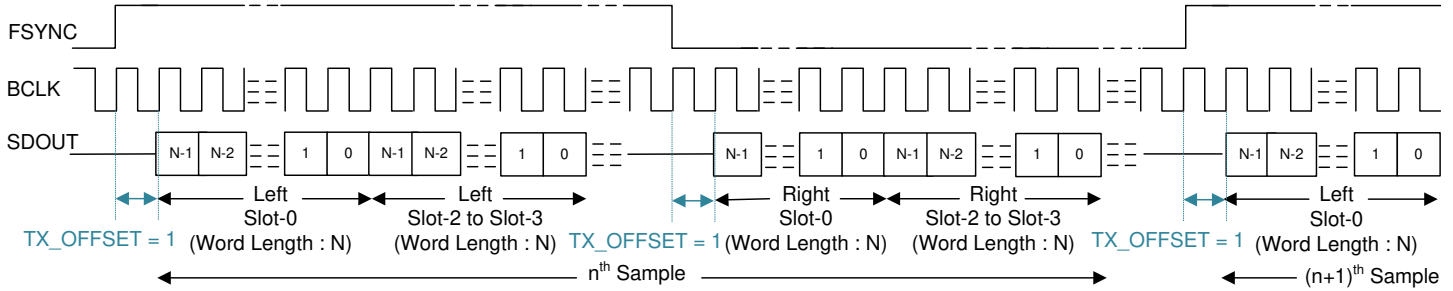


Figure 7-13. LJ Protocol Timing (TX_OFFSET = 1 and BCLK_POL = 1)

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be several BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be several BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX_OFFSET value higher than 0 is recommended.

7.3.1.3 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect multiple TAC5212 devices by sharing a single common I²C or SPI control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone or speaker array for beam-forming operation, audio conferencing, noise cancellation, and so forth. Figure 7-14 shows a diagram of multiple TAC5212 devices in a configuration where the control and audio data buses are shared.

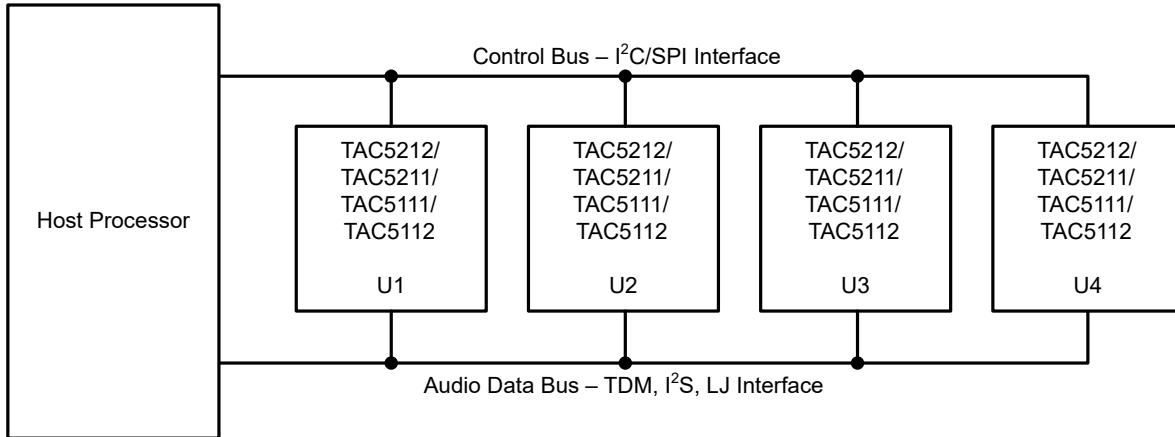


Figure 7-14. Multiple TAC5212 Devices With Shared Control and Audio Data Buses

The TAC5212 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:

- Supports up to four pin-programmable I²C target addresses
- I²C broadcast simultaneously writes to (or triggers) all TAC5212 devices
- Supports up to 32 configuration input/output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIOx, GPI1 or GPO1 pin can be configured as a secondary input/output data lane or as a secondary audio serial interface
- The GPIOx, GPI1 or GPO1 pin can be used in a daisy-chain configuration of multiple TAC5212 devices

- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable controller and target options for both primary and secondary audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices
- Inter Channel Gain Alignment(ICGA) feature to align the DAC Channel gain across devices.

See the [Multiple TAC5x1x Devices With a Shared TDM and I²C/SPI Bus application report](#) for further details.

7.3.2 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the ADC and DAC modulators and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signals on the audio buses.

The device supports the various data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. 表 7-6 and 表 7-7 list the supported FSYNC and BCLK frequencies.

表 7-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

| BCLK TO FSYNC RATIO | BCLK (MHz) | | | | | | | | |
|---------------------|---------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|
| | FSYNC (8 kHz) | FSYNC (16 kHz) | FSYNC (24 kHz) | FSYNC (32 kHz) | FSYNC (48 kHz) | FSYNC (96 kHz) | FSYNC (192 kHz) | FSYNC (384 kHz) | FSYNC (768 kHz) |
| 16 | Reserved | 0.256 | 0.384 | 0.512 | 0.768 | 1.536 | 3.072 | 6.144 | 12.288 |
| 24 | Reserved | 0.384 | 0.576 | 0.768 | 1.152 | 2.304 | 4.608 | 9.216 | 18.432 |
| 32 | 0.256 | 0.512 | 0.768 | 1.024 | 1.536 | 3.072 | 6.144 | 12.288 | 24.576 |
| 48 | 0.384 | 0.768 | 1.152 | 1.536 | 2.304 | 4.608 | 9.216 | 18.432 | Reserved |
| 64 | 0.512 | 1.024 | 1.536 | 2.048 | 3.072 | 6.144 | 12.288 | 24.576 | Reserved |
| 96 | 0.768 | 1.536 | 2.304 | 3.072 | 4.608 | 9.216 | 18.432 | Reserved | Reserved |
| 128 | 1.024 | 2.048 | 3.072 | 4.096 | 6.144 | 12.288 | 24.576 | Reserved | Reserved |
| 192 | 1.536 | 3.072 | 4.608 | 6.144 | 9.216 | 18.432 | Reserved | Reserved | Reserved |
| 256 | 2.048 | 4.096 | 6.144 | 8.192 | 12.288 | 24.576 | Reserved | Reserved | Reserved |
| 384 | 3.072 | 6.144 | 9.216 | 12.288 | 18.432 | Reserved | Reserved | Reserved | Reserved |
| 512 | 4.096 | 8.192 | 12.288 | 16.384 | 24.576 | Reserved | Reserved | Reserved | Reserved |
| 1024 | 8.192 | 16.384 | 24.576 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 2048 | 16.384 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

表 7-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

| BCLK TO FSYNC RATIO | BCLK (MHz) | | | | | | | | |
|---------------------|------------------|------------------|-------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|
| | FSYNC (7.35 kHz) | FSYNC (14.7 kHz) | FSYNC (22.05 kHz) | FSYNC (29.4 kHz) | FSYNC (44.1 kHz) | FSYNC (88.2 kHz) | FSYNC (176.4 kHz) | FSYNC (352.8 kHz) | FSYNC (705.6 kHz) |
| 16 | Reserved | Reserved | 0.3528 | 0.4704 | 0.7056 | 1.4112 | 2.8224 | 5.6448 | 11.2896 |
| 24 | Reserved | 0.3528 | 0.5292 | 0.7056 | 1.0584 | 2.1168 | 4.2336 | 8.4672 | 16.9344 |
| 32 | Reserved | 0.4704 | 0.7056 | 0.9408 | 1.4112 | 2.8224 | 5.6448 | 11.2896 | 22.5792 |
| 48 | 0.3528 | 0.7056 | 1.0584 | 1.4112 | 2.1168 | 4.2336 | 8.4672 | 16.9344 | Reserved |
| 64 | 0.4704 | 0.9408 | 1.4112 | 1.8816 | 2.8224 | 5.6448 | 11.2896 | 22.5792 | Reserved |
| 96 | 0.7056 | 1.4112 | 2.1168 | 2.8224 | 4.2336 | 8.4672 | 16.9344 | Reserved | Reserved |
| 128 | 0.9408 | 1.8816 | 2.8224 | 3.7632 | 5.6448 | 11.2896 | 22.5792 | Reserved | Reserved |
| 192 | 1.4112 | 2.8224 | 4.2336 | 5.6448 | 8.4672 | 16.9344 | Reserved | Reserved | Reserved |
| 256 | 1.8816 | 3.7632 | 5.6448 | 7.5264 | 11.2896 | 22.5792 | Reserved | Reserved | Reserved |
| 384 | 2.8224 | 5.6448 | 8.4672 | 11.2896 | 16.9344 | Reserved | Reserved | Reserved | Reserved |
| 512 | 3.7632 | 7.5264 | 11.2896 | 15.0528 | 22.5792 | Reserved | Reserved | Reserved | Reserved |
| 1024 | 7.5264 | 15.0528 | 22.5792 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 2048 | 15.0528 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

The TAC5212 also supports non-Audio sample rates beyond those listed in prior tables. Refer to [Configuring Non-Audio Sample Rates for TAC5x1x devices](#) for more details.

The TAC5212 sample rate can be configured using registers CLK_DET0 (P0_R62) and CLK_DET1 (P0_R63) for primary and secondary ASI respectively. These registers also capture the device auto-detect result for

the FSYNC frequency in auto-detection mode. The registers CLK_DET2 (P0_R64) and CLK_DET3 (P0_R65) capture the BCLK to FSYNC ratio detected by the device. If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock error interrupt and mutes all the channels accordingly.

The TAC5212 also supports enabling channels while ADC or DAC channels are already in operation. This requires a pre-configuration before power to describe the maximum number of channels that can be enabled while in operation to ensure proper clock generation and use. This can be configured by using register DYN_PUPD_CFG (P0_R119). ADC_DYN_PUPD_EN and DAC_DYN_PUPD_EN bits can be used to independently enable ADC or DAC Channels' dynamic power up. Several channels can be configured using ADC_DYN_MAXCH_SEL and DAC_DYN_MAXCH_SEL bits.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the modulators and digital filter engine, as well as other control blocks. The device also supports an option to use BCLK, GPIOx, or the GPI1 pin (as CCLK) as the audio clock source without using the PLL to reduce power consumption. However, the ADC performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications. More details and information on how to configure and use the device in low-power mode without using the PLL are discussed in the [TAC5x1x Power Consumption Matrix Across Various Usage Scenarios application report](#).

The device also supports an audio bus controller mode operation using the GPIOx or GPI1 pin (as CCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on controller mode configuration and operation are discussed in the [Configuring and Operating TAC5x1x as an Audio Bus Controller application report](#).

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks but can be disabled using the IGNORE_CLK_ERR (P0_R4_D6) and CUSTOM_CLK_CFG (P0_R50_D0) register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto-detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the [TAC5212EVM-PDK Evaluation module user's guide](#) and the [PurePath™ console graphical development suite](#).

7.3.3 Input Channel Configurations

The device consists of two pairs of analog input pins (INxP and INxM) that can be configured as differential inputs or single-ended inputs for the recording channel. The device supports simultaneous recording of up to two channels using the high-performance multichannel ADC. The input source for the analog pins can be from electret condenser analog microphones, microelectrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board. Analog inputs support differential input, single-ended inputs (two pin and one-pin) with AC and DC coupling options. Additionally, if the application uses digital PDM microphones for the recording, GPIO, GPI and GPO pins can be reconfigured in the device to support up to four channels for the digital microphone recording. TAC5212 supports incremental mode of ADC where analog input channels can be used for DC measurements. This can be configured by setting IADC_EN (P0_R81_D7). [表 7-8](#) shows the input source selection for the record channel.

表 7-8. Input Source Selection for the Record Channel

| P0_R80_D[7:6] : ADC_CH1_INSRC[1:0] | INPUT CHANNEL 1 RECORD SOURCE SELECTION |
|------------------------------------|---|
| 00 (default) | Analog differential input for channel 1 |
| 01 | Analog single-ended Input for channel 1 (Signal on one input pin and Ground on other pin) |
| 10 | Analog single-ended Input on IN1P |
| 11 | Analog single-ended Input on IN1M |

Similarly, the input source selection setting for input channel 2 can be configured using the ADC_CH2_INSRC[1:0] (P0_R85_D[7:6]) register bits.

Typically, voice or audio signal inputs are capacitively coupled (AC-coupled) to the device; however, the device also supports an option for DC-coupled inputs to save board space. This configuration can be done independently for each channel by setting the input common mode tolerance in ADC_CH1_CM_TOL (P0_R60_D[3:2]), ADC_CH2_CM_TOL (P0_R85_D[3:2]) register bits. The INM pin can be directly grounded in Rail to Rail Common Mode (see [Figure 7-15](#)), but the INM pin must be grounded after the AC-coupling capacitor whenever ADC_CHx_INSRC is set to 2'b01 and ADC_CHx_CM_TOL is set to 2'b01 (see [Figure 7-16](#)) for the single-ended input configuration. For the best dynamic range performance, the differential AC-coupled input must be used.

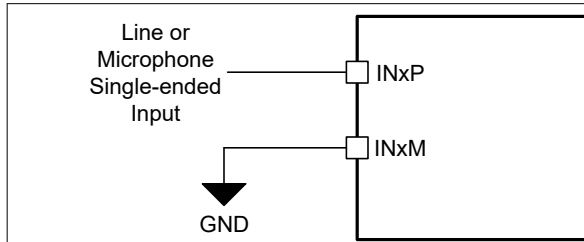


Figure 7-15. Single-Ended DC-Coupled Input Connection

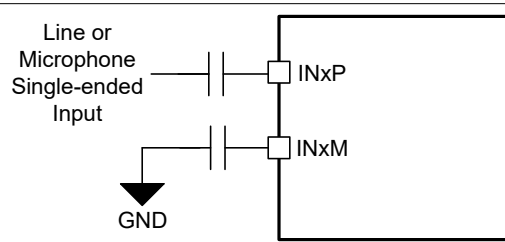


Figure 7-16. Single-Ended AC-Coupled Input Connection

The device allows for flexibility in choosing the typical input impedance on INxP or INxM from 5 kΩ (default), 10 kΩ, and 40 kΩ based on the input source impedance. The higher input impedance results in slightly higher noise or lower dynamic range. [Table 7-9](#) lists the configuration register settings for the input impedance for the record channel.

Table 7-9. Input Impedance Selection for the Record Channel

| P0_R80_D[5:4] : ADC_CH1_IMP[1:0] | CHANNEL 1 INPUT IMPEDANCE SELECTION |
|----------------------------------|--|
| 00 (default) | Channel 1 input impedance typical value is 5 kΩ on INxP or INxM |
| 01 | Channel 1 input impedance typical value is 10 kΩ on INxP or INxM |
| 10 | Channel 1 input impedance typical value is 40 kΩ on INxP or INxM |
| 11 | Reserved (do not use this setting) |

Similarly, the input impedance selection setting for input channel 2 can be configured using the ADC_CH2_IMP[1:0] (P0_R85_D[5:4]).

The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has modes to speed up the charging of the coupling capacitor. The default value of the quick-charge timing is set for a coupling capacitor up to 1 μF. However, if a higher-value capacitor is used in the system, then the quick-charging timing can be increased by using the INCAP_QCHG (P0_R5_D[7:6]) register bits. For best distortion performance, use the low-voltage coefficient capacitors for AC coupling.

7.3.4 Output Channel Configurations

The device consists of two pairs of analog output pins (OUTxP and OUTxM) that can be configured as differential inputs or single-ended outputs for playback channels. The device supports simultaneous playback of up to four channels of single-ended output or up to two channel differential output using the high-performance multichannel DAC. [Table 7-10](#) shows the input source selection for the playback channels.

Table 7-10. Input Source Selection for the Playback Channel

| P0_R100_D[7:5] : OUT1x_SRC[2:0] | OUT1P/OUT1M Source Selection |
|---------------------------------|------------------------------|
| 000 (default) | Output driver disabled |
| 001 | DAC signal chain |

表 7-10. Input Source Selection for the Playback Channel (続き)

| P0_R100_D[7:5] : OUT1x_SRC[2:0] | OUT1P/OUT1M Source Selection |
|---------------------------------|---|
| 010 | Analog bypass signal chain |
| 011 | Mixing of DAC and analog bypass signal chains |
| 100 | OUT1P for DAC and OUT1M for analog bypass signal chain |
| 101 | OUT1P for analog bypass and OUT1M for DAC signal chain. |
| 11x | Reserved. Do not use this setting. |

Similarly, the input source selection setting for output channel 2 can be configured using the OUT2x_SRC[2:0] (P0_R107_D[7:5]) register bits.

The TAC5212 supports up to 2-channel differential output, up to 2-channel pseudo-differential output, and up to 4-channel single-ended output. Each of the output channels can be independently configured for differential or single-ended output.

表 7-11 shows the configuration modes for the output pins

表 7-11. Output Pin Configuration for the Playback Channel

| P0_R100_D[4:2] : OUT1x_CFG[2:0] | OUT1P/OUT1M Pin Configuration |
|---------------------------------|---|
| 000 (default) | OUT1P/OUT1M as a differential pair |
| 001 | OUT1P and OUT1M as independent single-ended outputs |
| 010 | Mono Single Ended output on OUT1P only |
| 011 | Mono Single Ended output on OUT1M only |
| 100 | Pseudo-differential output with OUT1P as signal and OUT1M as VCOM |
| 101 | Pseudo differential output with OUT1P as signal, OUT1M as VCOM and OUT2M as VCOM sense. |
| 110 | Pseudo differential output with OUT1M as signal and OUT1P as VCOM |
| 111 | Reserved. Do not use this setting. |

Similarly, the output pin configuration for output channel 2 can be done using the OUT2x_CFG[2:0] (P0_R107_D[4:2]) register bits.

The TAC5212 can support a variety of loads including headphone, lineout, and receiver amplifiers. Load drive configurations are available for each pin independently. OUT1P_DRIVE[1:0] (OUT1x_CFG[7:6]) configures the load drive capability for the OUT1P pin. OUT1M_DRIVE[1:0], OUT2P_DRIVE[1:0], OUT2M_DRIVE[1:0] are the output drive control for OUT1M, OUT2P and OUT2M respectively.

7.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TAC5212 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1- μ F capacitor connected from the VREF pin to the analog ground (VSS).

The value of this reference voltage can be configured using the P0_R77_D[1:0] register bits and must be set to an appropriate value based on the desired full-scale input for the device and the AVDD supply voltage available in the system. The default VREF value is set to 2.75 V, which in turn supports a 2- V_{RMS} differential full-scale input to the device. The required minimum AVDD voltage for this mode is 3 V. The TAC5212 also supports double swing mode with 4- V_{RMS} differential swing which can be enabled by setting ADC_CHx_FULLSCALE_VAL to 1. 表 7-12 lists the various VREF settings supported along with the required AVDD range and the supported full-scale input signal for that configuration.

表 7-12. VREF Programmable Settings

| P0_R77_D[1:0]: VREF[1:0] | VREF OUTPUT VOLTAGE | DIFFERENTIAL FULL- SCALE INPUT SUPPORTED | SINGLE-ENDED FULL- SCALE INPUT SUPPORTED | AVDD RANGE REQUIREMENT |
|-----------------------------|------------------------|---|--|---------------------------|
| 00 (default) | 2.75 V | 2 V _{RMS} (4 V _{RMS} supported in high swing mode) | 1 V _{RMS} | 3 V to 3.6 V |
| 01 | 2.5 V | 1.818 V _{RMS} | 0.909 V _{RMS} | 2.8 V to 3.6 V |
| 10 | 1.375 V | 1 V _{RMS} | 0.5 V _{RMS} | 1.7 V to 1.9 V |
| 11 | Reserved | Reserved | Reserved | Reserved |

To achieve low power consumption, this audio reference block is powered down as described in the Device Functional Modes section. When exiting sleep mode, the audio reference block is powered up using the internal fast-charge scheme and the VREF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5 ms when using a 1-μF decoupling capacitor. If a higher-value decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF_QCHG (P0_R2_D[4:3]) register bits, which support options of 3.5 ms (default), 10 ms, 50 ms, or 100 ms.

7.3.6 Programmable Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The integrated bias amplifier supports up to 10 mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine-tuned for specific microphone combinations.

When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. 表 7-13 shows the available microphone bias programmable options.

表 7-13. MICBIAS Programmable Settings

| P0_R77_D[3:2] : MICBIAS_VAL[1:0] | P0_R77_D[1:0] : VREF_FSCALE[1:0] | MICBIAS OUTPUT VOLTAGE |
|----------------------------------|----------------------------------|--------------------------------------|
| 00 (default) | 00 (default) | 2.75 V (same as the VREF output) |
| | 01 | 2.5 V (same as the VREF output) |
| | 10 | 1.375 V (same as the VREF output) |
| | 11 | Reserved (do not use these settings) |
| 01 | 00 (default) | 1.375 V (0.5 times the VREF output) |
| | 01 | 1.250 V (0.5 times the VREF output) |
| | 10 or 11 | Reserved (do not use these settings) |
| 10 | XX | Reserved (do not use these settings) |
| 11 | XX | Same as AVDD |

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS_PDZ, P0_R120_D5 register bit. Additionally, the device provides an option to configure the GPIO1 or GPIx pin to directly control the microphone bias output powering on or off. This feature is useful to control the microphone directly without engaging the host for I²C or SPI communication. The MICBIAS_PDZ, P0_R120_D5 register bit value is ignored if the GPIO1 or GPIx pin is configured to set the microphone bias on or off.

7.3.7 Signal-Chain Processing

The TAC5212 signal chain is comprised of very low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package make the TAC5212 is optimized for a variety of end-equipments and applications that require multichannel audio capture and playback. [セクション 7.3.7.1](#) and [セクション 7.3.7.2](#) describes key components in ADC and DAC signal chain further.

7.3.7.1 ADC Signal-Chain

Figure 7-17 shows the key components of the record path signal chain.

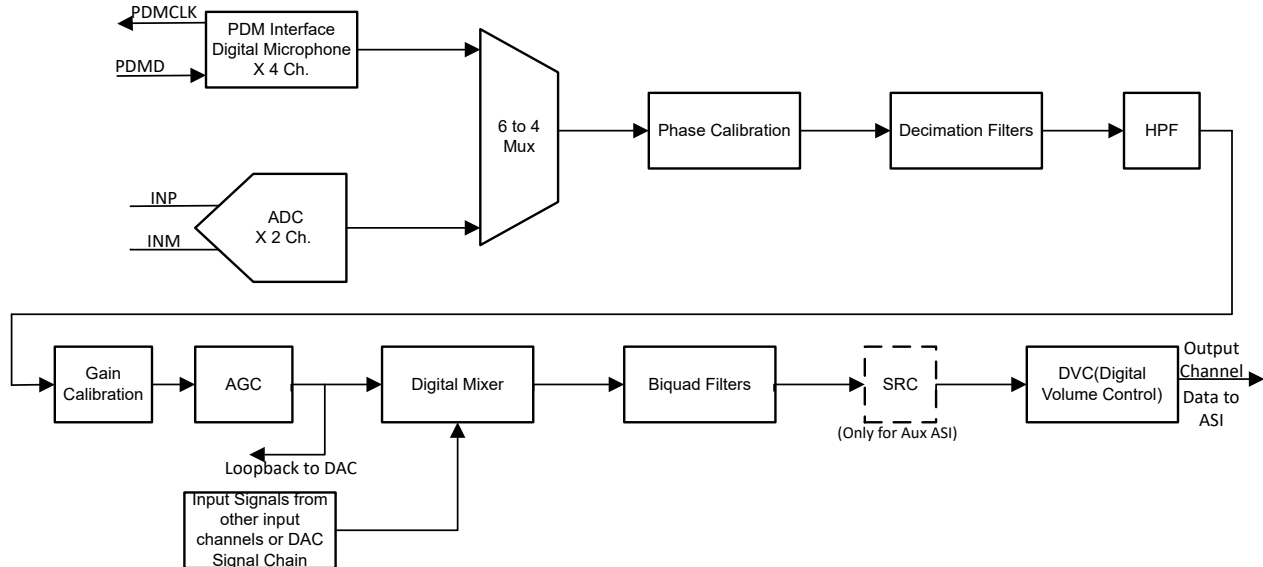


Figure 7-17. ADC Signal-Chain Processing Flowchart

The front-end ADC is very low noise, with a 115-dB dynamic range performance. This low-noise and low-distortion, multibit, delta-sigma ADC enables the TAC5212 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device also has an integrated programmable biquad filter that allows for custom low-pass, high-pass, or any other desired frequency shaping. Thus, the overall signal chain architecture removes the requirement to add external components for antialiasing low-pass filtering and thus saves drastically on the external system component cost and board space. See the [TAC5212 Integrated Analog Antialiasing Filter and Flexible Digital Filter application report](#) for further details.

The signal chain also consists of various highly programmable digital processing blocks such as phase calibration, gain calibration, high-pass filter, digital summer or mixer, biquad filters, synchronous sample rate converter, and volume control. The details of these processing blocks are discussed further in this section. The device also supports up to four digital PDM microphone recording channels when the analog recording channels are not used.

The desired input channels for recording can be enabled or disabled by using the CH_EN (P0_R118) register, and the output channels for the audio serial interface can be enabled or disabled by using the ASI_TX_CHx_CFG register. In general, the device supports simultaneous power-up and power-down of all active channels for simultaneous recording. However, based on the application needs, if some channels must be powered up or powered down dynamically when the other channel recording is on, then that use case is supported by setting the DYN_PUPD_CFG register.

The device supports an input signal bandwidth up to 100 kHz, which allows the high-frequency non-audio signal to be recorded by using a 216-kHz (or higher) sample rate. Wide bandwidth mode can be enabled or disabled by setting ADC_CHx_BW_MODE bit.

For sample rates of 48 kHz or lower, the device supports all features and various programmable processing blocks. However, for sample rates higher than 48 kHz, there are limitations in the number of simultaneous

channel recordings and playback supported and the number of biquad filters and such. See the [TAC5212 Sampling Rates and Programmable Processing Blocks Supported application report](#) for further details.

7.3.7.1.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each input channel that can be set to the appropriate value based on the maximum input signal expected in the system and the ADC VREF setting used (see the [セクション 7.3.5](#) section), which determines the ADC full-scale signal level.

The device has a programmable digital volume control with a range from –80 dB to 47 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically while the ADC channel is powered up and recorded. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the ADC_DSP_DISABLE_SOFT_STEP (P0_R114_D1) register bit.

The digital volume control setting is independently available for each output channel, including the digital microphone record channel. However, the device also supports an option to gang up the volume control setting for all channels together using the channel 1 digital volume control setting, regardless if channel 1 is powered up or powered down. This gang-up can be enabled using the ADC_DSP_DVOL_GANG (P0_R114_D0) register bit.

表 7-14 shows the programmable options available for the digital volume control.

表 7-14. Digital Volume Control (DVC) Programmable Settings

| P0_R82_D[7:0] : ADC_CH1_DVOL[7:0] | DVC SETTING FOR OUTPUT CHANNEL 1 |
|-----------------------------------|---|
| 0000 0000 = 0d | Output channel 1 DVC is set to mute |
| 0000 0001 = 1d | Output channel 1 DVC is set to –80 dB |
| 0000 0010 = 2d | Output channel 1 DVC is set to –79.5 dB |
| 0000 0011 = 3d | Output channel 1 DVC is set to –79 dB |
| ... | ... |
| 1010 0000 = 160d | Output channel 1 DVC is set to –0.5 dB |
| 1010 0001 = 161d (default) | Output channel 1 DVC is set to 0 dB |
| 1010 0010 = 162d | Output channel 1 DVC is set to 0.5 dB |
| ... | ... |
| 1111 1101 = 253d | Output channel 1 DVC is set to 46 dB |
| 1111 1110 = 254d | Output channel 1 DVC is set to 46.5 dB |
| 1111 1111 = 255d | Output channel 1 DVC is set to 47 dB |

Similarly, the digital volume control setting for output channel 2 to channel 4 can be configured using the CH2_DVOL (P0_R87) to CH4_DVOL (P0_R95) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the record channel. This feature can also be entirely disabled using the ADC_DSP_DISABLE_SOFT_STEP (P0_R114_D1) register bit.

7.3.7.1.2 Programmable Channel Gain Calibration

Along with the digital volume control, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of –0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from external components and microphone sensitivity. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. 表 7-15 shows the programmable options available for the channel gain calibration.

表 7-15. Channel Gain Calibration Programmable Settings

| P0_R83_D[7:4] : ADC_CH1_FGAIN[3:0] | CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1 |
|------------------------------------|--|
| 0000 = 0d | Input channel 1 gain calibration is set to -0.8 dB |
| 0001 = 1d | Input channel 1 gain calibration is set to -0.7 dB |
| ... | ... |
| 1000 = 8d (default) | Input channel 1 gain calibration is set to 0 dB |
| ... | ... |
| 1110 = 14d | Input channel 1 gain calibration is set to 0.6 dB |
| 1111 = 15d | Input channel 1 gain calibration is set to 0.7 dB |

Similarly, the channel gain calibration setting for input channel 2 to channel 4 can be configured using the ADC_CH2_CFG3 (P0_R88) to ADC_CH4_CFG3 (P0_R96) register bits, respectively.

7.3.7.1.3 Programmable Channel Phase Calibration

In addition to the gain calibration, the phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 255 for the phase error. The modulator clock, the same clock used for ADC_MOD_CLK, is 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz) or 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz) irrespective of the analog microphone or digital microphone use case. This feature is very useful for many applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones. 表 7-16 shows the available programmable options for channel phase calibration.

表 7-16. Channel Phase Calibration Programmable Settings

| P0_R64_D[7:0] : CH1_PCAL[7:0] | CHANNEL PHASE CALIBRATION SETTING FOR INPUT CHANNEL 1 |
|-------------------------------|---|
| 0000 0000 = 0d (default) | Input channel 1 phase calibration with no delay |
| 0000 0001 = 1d | Input channel 1 phase calibration delay is set to one cycle of the modulator clock |
| 0000 0010 = 2d | Input channel 1 phase calibration delay is set to two cycles of the modulator clock |
| ... | ... |
| 1111 1110 = 254d | Input channel 1 phase calibration delay is set to 254 cycles of the modulator clock |
| 1111 1111 = 255d | Input channel 1 phase calibration delay is set to 255 cycles of the modulator clock |

Similarly, the channel phase calibration setting for input channel 2 to channel 8 can be configured using the CH2_PCAL (P0_R69) to CH8_PCAL (P0_R99) register bits, respectively.

The phase calibration feature must not be used when the analog input and PDM input are used together for simultaneous conversion.

7.3.7.1.4 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter and is efficient enough to filter out possible DC components of the signal. 表 7-17 shows the predefined -3-dB cutoff frequencies available that can be set by using the ADC_DSP_HP_SEL[1:0] register bits of P0_R114. Additionally, to achieve a custom -3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the HPF_SEL[1:0] register bits are set to 2'b00. The inability to set a frequency response plot for the HPF filter.

表 7-17. HPF Programmable Settings

| P0_R107_D[1:0] : HPF_SEL[1:0] | -3-dB CUTOFF FREQUENCY SETTING | -3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE | -3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE |
|-------------------------------|-----------------------------------|--|--|
| 00 | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter |
| 01 (default) | $0.00002 \times f_s$ | 0.25 Hz | 1 Hz |

表 7-17. HPF Programmable Settings (続き)

| P0_R107_D[1:0] : HPF_SEL[1:0] | -3-dB CUTOFF FREQUENCY SETTING | -3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE | -3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE |
|----------------------------------|-----------------------------------|---|---|
| 10 | $0.00025 \times f_S$ | 4 Hz | 12 Hz |
| 11 | $0.002 \times f_S$ | 32 Hz | 96 Hz |

図 7-18. HPF Filter Frequency Response Plot

式 1 gives the transfer function for the first-order programmable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (1)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in 表 7-18 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If HPF_SEL[1:0] is set to 2'b00, the host device must write these coefficient values for the desired frequency response before powering-up any ADC channel for recording. 表 7-18 shows the filter coefficients for the first-order IIR filter.

表 7-18. 1st-Order IIR Filter Coefficients

| FILTER | FILTER COEFFICIENT | DEFAULT COEFFICIENT VALUE | COEFFICIENT REGISTER MAPPING |
|---|-----------------------|---------------------------|---------------------------------|
| Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter) | N_0 | 0x7FFFFFFF | P4_R72-R75 |
| | N_1 | 0x00000000 | P4_R76-R79 |
| | D_1 | 0x00000000 | P4_R80-R83 |

7.3.7.1.5 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters available for ADC signal chain limited to 3/channel. These highly efficient filters achieve the desired frequency response. The TAC5212 also supports on-the-fly programmable Biquad filters for two-channel record use cases. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. 式 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}} \quad (2)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for low-pass, high-pass, or any other desired frequency shaping. The programmable coefficients for the mixer operation are located in the and sections. If biquad filtering is required, then the host device must write these coefficient values before powering up any ADC channels for recording. In two-channel use case, the TAC5212 also supports on-the-fly programmable filters. In this case, the Device uses two banks of filters for one channel with a switch bit to perform the switch from one filter bank to the other. As described in 表 7-19, these biquad filters can be allocated for each output channel based on the ADC_DSP_BQ_CFG[1:0] register setting of P0_R114. By setting BIQUAD_CFG[1:0] to 2'b00, the biquad filtering for all record channels is disabled and the host device can choose this setting if no additional

filtering is required for the system application. See the [TAC5212 Programmable Biquad Filter Configuration and Applications application report](#) for further details.

表 7-19. Biquad Filter Allocation to the Record Output Channel

| PROGRAMMABLE BIQUAD FILTER | RECORD OUTPUT CHANNEL ALLOCATION USING P0_R114_D[3:2] REGISTER SETTING | | |
|----------------------------|--|---|--|
| | ADC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel) | ADC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel) | ADC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel) |
| Biquad filter 1 | Allocated to output channel 1 | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 2 | Allocated to output channel 2 | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 3 | Allocated to output channel 3 | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 4 | Allocated to output channel 4 | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 5 | Not used | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 6 | Not used | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 7 | Not used | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 8 | Not used | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 9 | Not used | Not used | Allocated to output channel 1 |
| Biquad filter 10 | Not used | Not used | Allocated to output channel 2 |
| Biquad filter 11 | Not used | Not used | Allocated to output channel 3 |
| Biquad filter 12 | Not used | Not used | Allocated to output channel 4 |

表 7-20 shows the biquad filter coefficients mapping to the register space.

表 7-20. Biquad Filter Coefficients Register Mapping

| PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING | PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING |
|----------------------------|---|----------------------------|---|
| Biquad filter 1 | P8_R8-R27 | Biquad filter 7 | P9_R8-R27 |
| Biquad filter 2 | P8_R28-R47 | Biquad filter 8 | P9_R28-R47 |
| Biquad filter 3 | P8_R48-R67 | Biquad filter 9 | P9_R48-R67 |
| Biquad filter 4 | P8_R68-R87 | Biquad filter 10 | P9_R68-R87 |
| Biquad filter 5 | P8_R88-R107 | Biquad filter 11 | P9_R88-R107 |
| Biquad filter 6 | P8_R108-R127 | Biquad filter 12 | P9_R108-R127 |

7.3.7.1.6 Programmable Channel Summer and Digital Mixer

For applications that require an even higher SNR than that supported for each channel, the device's digital summing mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise.

The device supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. 図 7-19 shows a block diagram that describes the mixer 1 operation to generate output channel 1. The programmable coefficients for the mixer operation are located in the section.

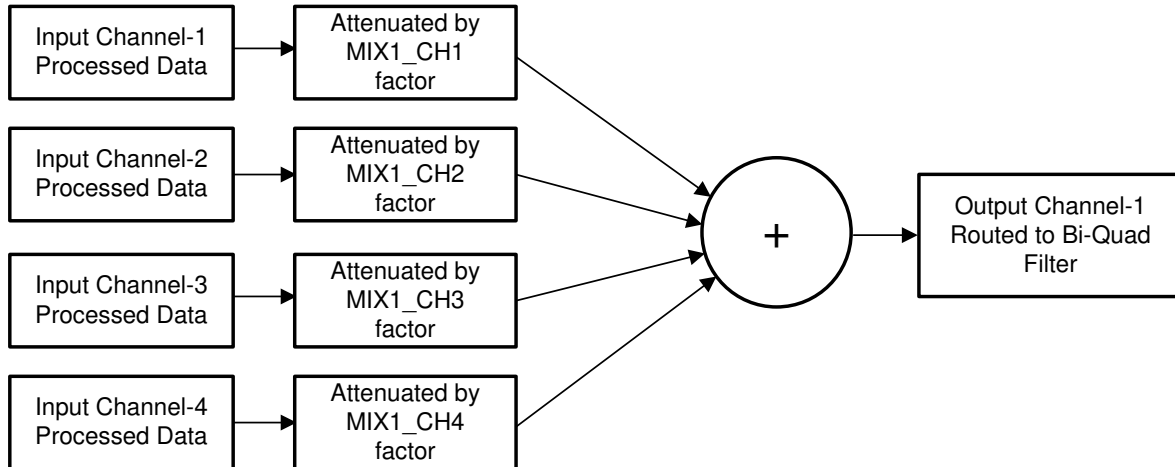


図 7-19. Programmable Digital Mixer Block Diagram

A similar mixer operation is performed by mixer 2, mixer 3, and mixer 4 to generate output channel 2, channel 3, and channel 4, respectively.

7.3.7.1.7 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range and a built-in digital decimation filter to process the oversampled data from the multibit delta-sigma ($\Delta\Sigma$) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. As illustrated in [図 7-17](#), this decimation filter can also be used for processing the oversampled PDM stream from the digital microphone. The decimation filter can be chosen from four different types, depending on the required frequency response, group delay, power consumption, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by configuring the ADC_DSP_DECI_FILT, P0_R114_D[7:6] register bits. Low power filter can be configured by setting ADC_LOW_PWR_FILT, P0_R78_D2 bit. [表 7-21](#) shows the configuration register setting for the decimation filter mode selection for the record channel.

表 7-21. Decimation Filter Mode Selection for the Record Channel

| P0_R78_D2 : ADC_LOW_PWR_FILT | P0_R114_D[7:6] : ADC_DSP_DECI_FILT[1:0] | DECIMATION FILTER MODE SELECTION |
|---------------------------------|--|---|
| 0 | 00 (default) | Linear phase filters are used for the decimation |
| 0 | 01 | Low latency filters are used for the decimation |
| 0 | 10 | Ultra-low latency filters are used for the decimation |
| 0 | 11 | Reserved (do not use this setting) |
| 1 | x | Low power filters are used for the decimation |

7.3.7.1.7.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

7.3.7.1.7.1.1 Sampling Rate: 16 kHz or 14.7 kHz

図 7-20 and 図 7-21 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. 表 7-22 lists the specifications for a decimation filter with a 16-kHz or 14.7-kHz sampling rate.

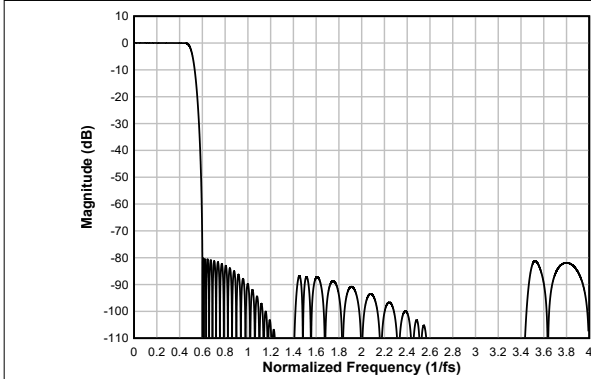


図 7-20. Linear Phase Decimation Filter Magnitude Response

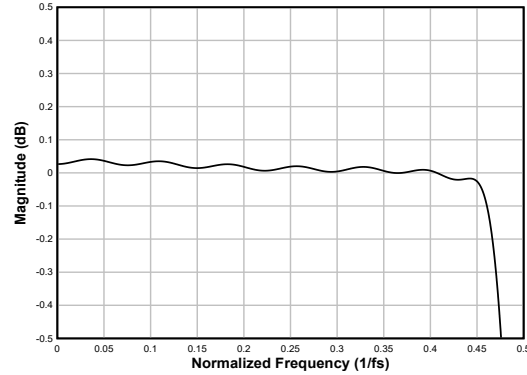


図 7-21. Linear Phase Decimation Filter Pass-Band Ripple

表 7-22. Linear Phase Decimation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|-------|------|------|------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_s$ | -0.05 | | 0.05 | dB |
| Stop-band attenuation | Frequency range is $0.6 \times f_s$ to $4 \times f_s$ | 80.2 | | | |
| | Frequency range is $4 \times f_s$ onwards | 84.7 | | | dB |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_s$ | | 16.1 | | |

7.3.7.1.7.1.2 Sampling Rate: 24 kHz or 22.05 kHz

図 7-22 and 図 7-23 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. 表 7-23 lists the specifications for a decimation filter with an 24-kHz or 22.05-kHz sampling rate.

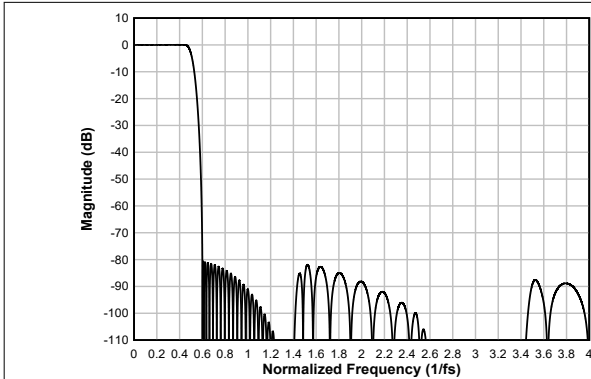


図 7-22. Linear Phase Decimation Filter Magnitude Response

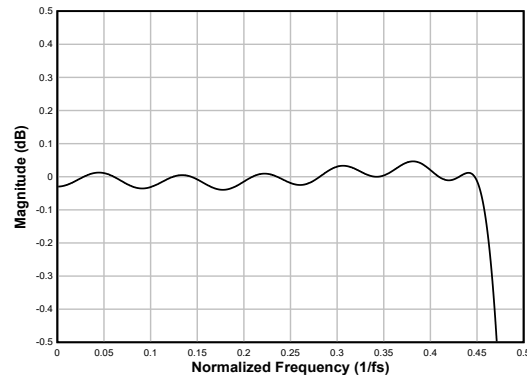


図 7-23. Linear Phase Decimation Filter Pass-Band Ripple

表 7-23. Linear Phase Decimation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|-------|-----|------|------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_s$ | -0.05 | | 0.05 | dB |
| Stop-band attenuation | Frequency range is $0.6 \times f_s$ to $4 \times f_s$ | 80.6 | | | |
| | Frequency range is $4 \times f_s$ onwards | 92.9 | | | dB |

表 7-23. Linear Phase Decimation Filter Specifications (続き)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-----|------|-----|---------|
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 14.7 | | $1/f_S$ |

7.3.7.1.7.1.3 Sampling Rate: 32 kHz or 29.4 kHz

図 7-24 and 図 7-25 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. 表 7-24 lists the specifications for a decimation filter with an 32-kHz or 29.4-kHz sampling rate.

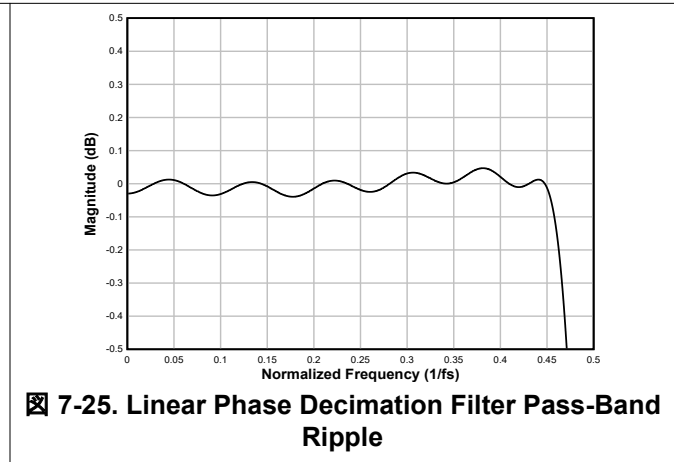
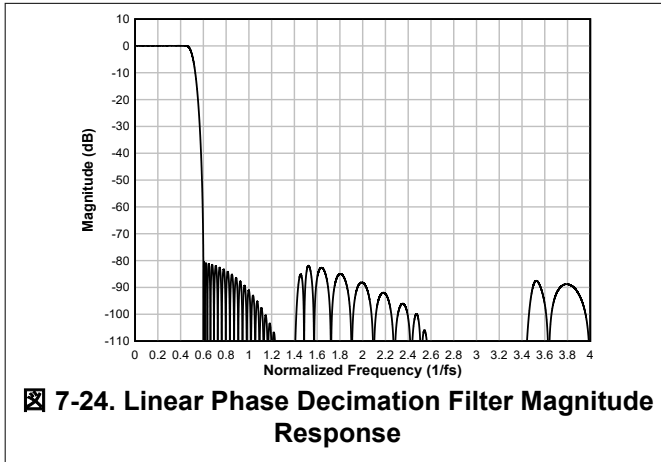


表 7-24. Linear Phase Decimation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_S$ | -0.05 | | 0.05 | dB |
| Stop-band attenuation | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 80.6 | | | dB |
| | Frequency range is $4 \times f_S$ onwards | 92.9 | | | |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 14.7 | | $1/f_S$ |

7.3.7.1.7.1.4 Sampling Rate: 48 kHz or 44.1 kHz

図 7-26 and 図 7-27 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. 表 7-25 lists the specifications for a decimation filter with an 48-kHz or 44.1-kHz sampling rate.

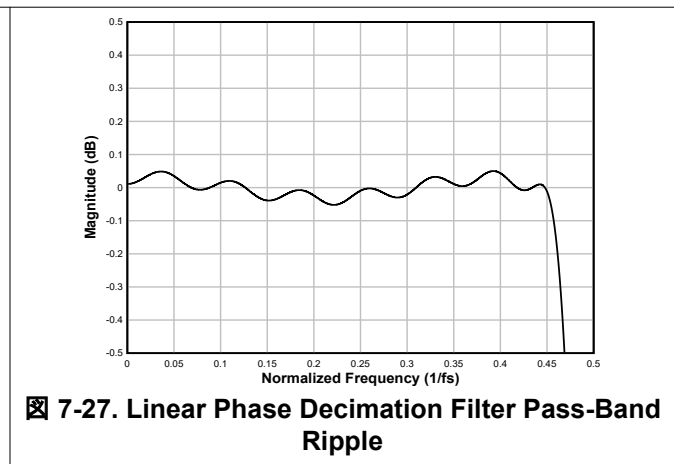
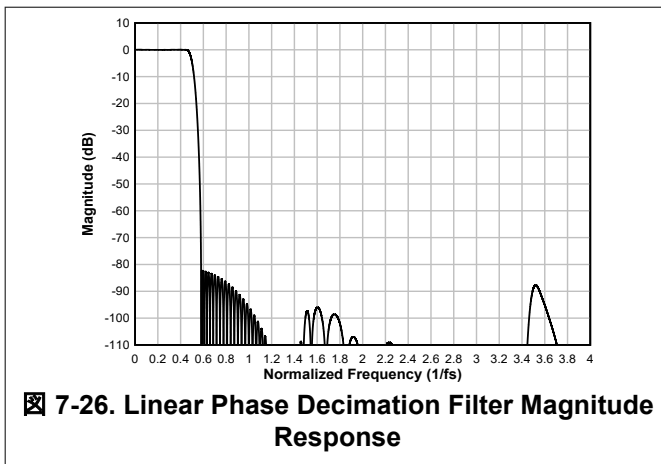


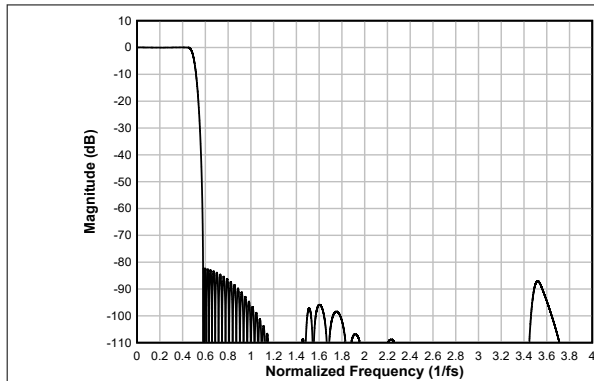


表 7-25. Linear Phase Decimation Filter Specifications

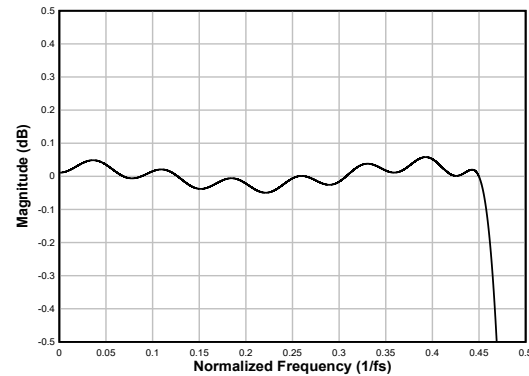
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|--------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_S$ | -0.052 | | 0.05 | dB |
| Stop-band attenuation | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 82.2 | | | dB |
| | Frequency range is $4 \times f_S$ onwards | 97.9 | | | |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 17.0 | | $1/f_S$ |

7.3.7.1.7.1.5 Sampling Rate: 96 kHz or 88.2 kHz

 7-28 and  7-29 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. 表 7-26 lists the specifications for a decimation filter with an 96-kHz or 88.2-kHz sampling rate.



 7-28. Linear Phase Decimation Filter Magnitude Response





 7-29. Linear Phase Decimation Filter Pass-Band Ripple

表 7-26. Linear Phase Decimation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-------|------|-------|---------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_S$ | -0.05 | | 0.058 | dB |
| Stop-band attenuation | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 82.2 | | | dB |
| | Frequency range is $4 \times f_S$ onwards | 96.9 | | | |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 16.9 | | $1/f_S$ |

7.3.7.1.7.1.6 Sampling Rate: 384 kHz or 352.8 kHz

 7-30 and  7-31 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 384 kHz or 352.8 kHz. 表 7-27 lists the specifications for a decimation filter with an 384-kHz or 352.8-kHz sampling rate.

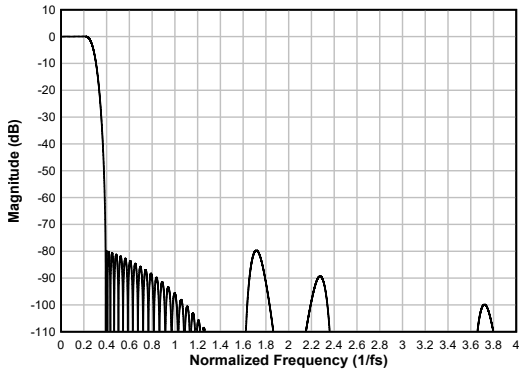


図 7-30. Linear Phase Decimation Filter Magnitude Response

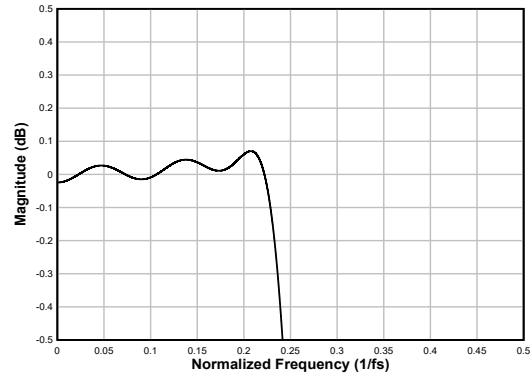


図 7-31. Linear Phase Decimation Filter Pass-Band Ripple

表 7-27. Linear Phase Decimation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|-------|-------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.227 \times f_S$ | -0.07 | | 0.07 | dB |
| Stop-band attenuation | Frequency range is $0.391 \times f_S$ to $2 \times f_S$ | 79.7 | | | dB |
| | Frequency range is $2 \times f_S$ onwards | 89.3 | | | |
| Group delay or latency | Frequency range is 0 to $0.212 \times f_S$ | | 11.45 | | $1/f_S$ |

7.3.7.2 DAC Signal-Chain

Figure 7-32 shows the key components of the playback signal chain.

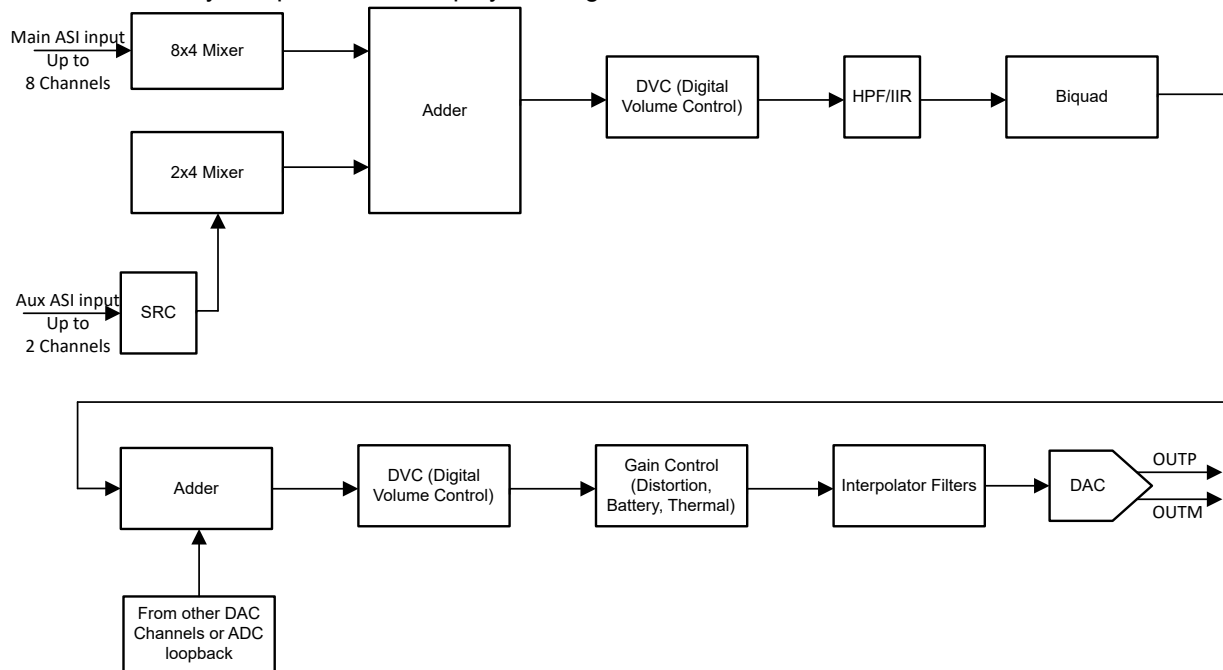


Figure 7-32. DAC Signal-Chain Processing Flowchart

The DAC signal chain offers a highly flexible low-noise playback path for low-noise and high-fidelity audio applications. This low-noise and low-distortion, multibit, delta-sigma DAC enables the TAC5212 to achieve 120 dB dynamic range in very low power. Moreover, the DAC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. Further on in the signal chain, an integrated, high-performance multistage digital interpolation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The signal chain also consists of various highly programmable digital processing blocks such as biquad filters, phase calibration, gain calibration, high-pass filter, digital summer or mixer, synchronous sample rate converter, distortion limiter, thermal foldback, brownout prevention, and volume control. The details of these processing blocks are discussed further in this section. The device also supports up to four channel single-ended output modes and an analog bypass option from ADC input to DAC output.

The output channels for playback can be enabled or disabled by using the CH_EN (P0_R118) register, and the input channels for the audio serial interface can be enabled or disabled by using the PASI_RX_CHx_CFG or SASI_RX_CHx_CFG bits. The device supports simultaneous power-up and power-down of all active channels for simultaneous playback. However, based on the application needs, if some channels must be powered-up or powered-down dynamically when the other channel playback is on, then that use case is supported by setting the DYN_PUPD_CFG register.

The device supports multiple data mixing options where up to 8 Input Channels from Main ASI, 2 Input Channels from Aux ASI, ADC loopback data, and tone generator can be mixed with flexible gain options for each path before playback on DAC output. By default, these mixers are disabled and channels are configured for only one channel of data. Mixers can be configured by setting ASI_DIN_Mixers on Page 17.

The device supports an output signal bandwidth of up to 100 kHz, which allows the high-frequency non-audio signal to be played by using a 216 kHz (or higher) sample rate. Wideband mode can be enabled or disabled by using the DAC_CHx_BW_Mode bit.

For sample rates of 48 kHz or lower, the device supports all features and various programmable processing blocks. However, for sample rates higher than 48 kHz, there are limitations in the number of simultaneous channel recordings and playback supported and the number of biquad filters and such. See the [TAC5212 Sampling Rates and Programmable Processing Blocks Supported application report](#) for further details.

7.3.7.2.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each output channel that can be set to the appropriate value based on the maximum input signal expected in the system. This can be done by configuring OUT1x_LVL_CTRL and OUT2x_LVL_CTRL bits. Coarse gain configuration from -6dB to +24dB is available with these controls in steps of 6dB. .

The device has a programmable digital volume control with a range from -100 dB to 27 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically while the DAC channel is powered-up and playing. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DAC_DSP_DISABLE_SOFT_STEP (P0_R115_D1) register bit.

The digital volume control setting is independently available for each of the 4 single-ended output channels. In the case of 2 Channel Differential DAC, Only settings for DAC_CH1A and DAC_CH2A are applicable. The device also supports an option to gang up the volume control setting for all channels together using the channel 1 A digital volume control setting, regardless if channel 1A is powered up or powered down. This gang-up can be enabled using the DAC_DSP_DVOL_GANG (P0_R115_D0) register bit.

表 7-28 shows the programmable options available for the digital volume control.

表 7-28. Digital Volume Control (DVC) Programmable Settings

| P0_R103_D[7:0] : DAC_CH1A_DVOL[7:0] | DVC SETTING FOR OUTPUT CHANNEL 1A |
|-------------------------------------|---|
| 0000 0000 = 0d | Output channel 1 DVC is set to mute |
| 0000 0001 = 1d | Output channel 1 DVC is set to -100 dB |
| 0000 0010 = 2d | Output channel 1 DVC is set to -99.5 dB |
| 0000 0011 = 3d | Output channel 1 DVC is set to -99 dB |
| ... | ... |
| 1100 1000 = 200d | Output channel 1 DVC is set to -0.5 dB |
| 1100 1001 = 201d (default) | Output channel 1 DVC is set to 0 dB |
| 1100 1010 = 202d | Output channel 1 DVC is set to 0.5 dB |
| ... | ... |
| 1111 1101 = 253d | Output channel 1 DVC is set to 26 dB |
| 1111 1110 = 254d | Output channel 1 DVC is set to 26.5 dB |
| 1111 1111 = 255d | Output channel 1 DVC is set to 27 dB |

Similarly, the digital volume control setting for output channels 1B,2A, and 2B can be configured using the CH1B_DVOL (P0_R103) to CH2B_DVOL (P0_R112) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the playback channel which can cause audible artifacts. This feature can also be entirely disabled using the DAC_DSP_DISABLE_SOFT_STEP (P0_R115_D1) register bit.

7.3.7.2.2 Programmable Channel Gain Calibration

Along with the digital volume control, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of -0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from transducer sensitivity and load impedance mismatch. This feature, in combination with the regular digital volume control,

allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. 表 7-29 shows the programmable options available for the channel gain calibration.

表 7-29. DAC Channel Gain Calibration Programmable Settings

| P0_R104_D[7:4] : DAC_CH1A_FGAIN[3:0] | CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1A |
|--------------------------------------|---|
| 0000 = 0d | Input channel 1 gain calibration is set to -0.8 dB |
| 0001 = 1d | Input channel 1 gain calibration is set to -0.7 dB |
| ... | ... |
| 1000 = 8d (default) | Input channel 1 gain calibration is set to 0 dB |
| ... | ... |
| 1110 = 14d | Input channel 1 gain calibration is set to 0.6 dB |
| 1111 = 15d | Input channel 1 gain calibration is set to 0.7 dB |

Similarly, the channel gain calibration setting for input channel 1B,2A and 2B can be configured using the DAC_CH1B_CFG1 (P0_R106), DAC_CH2A_CFG1 (P0_R111), and DAC_CH2B_CFG1 (P0_R113) register bits, respectively.

7.3.7.2.3 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all DAC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. 表 7-30 shows the predefined -3-dB cutoff frequencies available that can be set by using the DAC_DSP_HP_SEL[1:0] register bits of P0_R115. Additionally, to achieve a custom -3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the DAC_DSP_HP_SEL[1:0] register bits are set to 2'b00. 図 7-33 illustrates a frequency response plot for the HPF filter.

表 7-30. HPF Programmable Settings

| P0_R115_D[5:4] : DAC_DSP_HP_SEL[1:0] | -3-dB CUTOFF FREQUENCY SETTING | -3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE | -3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE |
|--------------------------------------|-----------------------------------|--|--|
| 00 | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter |
| 01 (default) | $0.00002 \times f_s$ | 0.25 Hz | 1 Hz |
| 10 | $0.00025 \times f_s$ | 4 Hz | 12 Hz |
| 11 | $0.002 \times f_s$ | 32 Hz | 96 Hz |

図 7-33. HPF Filter Frequency Response Plot

式 3 gives the transfer function for the first-order programmable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (3)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in 表 7-31 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If DAC_DSP_HP_SEL[1:0] are set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any DAC channel for playback. 表 7-31 shows the filter coefficients for the first-order IIR filter.

表 7-31. 1st-Order IIR Filter Coefficients

| FILTER | FILTER COEFFICIENT | DEFAULT COEFFICIENT VALUE | COEFFICIENT REGISTER MAPPING |
|---|--------------------|---------------------------|------------------------------|
| Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter) | N ₀ | 0x7FFFFFFF | P17_R120-R124 |
| | N ₁ | 0x00000000 | P17_R125-R128 |
| | D ₁ | 0x00000000 | P18_R8-R11 |

7.3.7.2.4 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters available for DAC signal chain limited to 3/channel. These highly efficient filters achieve the desired frequency response. The TAC5212 also supports on the fly programmable Biquad filters for two channel playback use case. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. 式 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1z^{-1} + N_2z^{-2}}{2^{31} - 2D_1z^{-1} - D_2z^{-2}} \quad (4)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. The programmable coefficients for the mixer operation are located in the and sections. If biquad filtering is required, then the host device must write these coefficients values before powering up any ADC channels for recording. In two channel use case, the TAC5212 also supports on the fly programmable filters. In this case, Device uses two banks of filters for one channel with a switch bit to perform the switch from one filter bank to the other. As described in 表 7-32, these biquad filters can be allocated for each output channel based on the DAC_DSP_BQ_CFG[1:0] register setting of P0_R115. By setting DAC_DSP_BQ_CFG[1:0] to 2'b00, the biquad filtering for all playback channels are disabled and the host device can choose this setting if no additional filtering is required for the system application. See the [TAC5212 Programmable Biquad Filter Configuration and Applications application report](#) for further details.

表 7-32. Biquad Filter Allocation to the Record Output Channel

| PROGRAMMABLE BIQUAD FILTER | RECORD OUTPUT CHANNEL ALLOCATION USING P0_R115_D[3:2] REGISTER SETTING | | |
|----------------------------|--|---|--|
| | DAC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel) | DAC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel) | DAC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel) |
| Biquad filter 1 | Allocated to output channel 1 | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 2 | Allocated to output channel 2 | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 3 | Allocated to output channel 3 | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 4 | Allocated to output channel 4 | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 5 | Not used | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 6 | Not used | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 7 | Not used | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 8 | Not used | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 9 | Not used | Not used | Allocated to output channel 1 |
| Biquad filter 10 | Not used | Not used | Allocated to output channel 2 |
| Biquad filter 11 | Not used | Not used | Allocated to output channel 3 |
| Biquad filter 12 | Not used | Not used | Allocated to output channel 4 |

表 7-33 shows the biquad filter coefficients mapping to the register space.

表 7-33. Biquad Filter Coefficients Register Mapping

| PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING | PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING |
|----------------------------|---|----------------------------|---|
| Biquad filter 1 | P16_R8-R27 | Biquad filter 7 | P17_R8-R27 |
| Biquad filter 2 | P16_R28-R47 | Biquad filter 8 | P17_R28-R47 |
| Biquad filter 3 | P16_R48-R67 | Biquad filter 9 | P17_R48-R67 |
| Biquad filter 4 | P16_R68-R87 | Biquad filter 10 | P17_R68-R87 |
| Biquad filter 5 | P16_R88-R107 | Biquad filter 11 | P17_R88-R107 |
| Biquad filter 6 | P16_R108-R127 | Biquad filter 12 | P17_R108-R127 |

7.3.7.2.5 Programmable Digital Mixer

The device supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. [図 7-19](#) shows a block diagram that describes the mixer 1 operation to generate output channel 1. The programmable coefficients for the mixer operation are located in the section.

A similar mixer operation is performed by mixer 2, mixer 3, and mixer 4 to generate output channel 2, channel 3, and channel 4, respectively.

7.3.7.2.6 Configurable Digital Interpolation Filters

The device playback channel includes a high dynamic range, built-in digital interpolation filter to process the input data stream to generate digital data stream for multibit delta-sigma ($\Delta\Sigma$) modulator. The interpolation filter can be chosen from four different types, depending on the required frequency response, group delay, power consumption, and phase linearity requirements for the target application. The selection of the interpolation filter option can be done by configuring the DAC_DSP_INTX_FILT, P0_R115_D[7:6] register bits. Low power filter can be configured by setting DAC_LOW_PWR_FILT, P0_R79_D2 bit. [表 7-34](#) shows the configuration register setting for the decimation filter mode selection for the record channel.

表 7-34. Interpolation Filter Mode Selection for the Playback Channel

| P0_R79_D2 : DAC_LOW_PWR_FILT | P0_R115_D[7:6] : DAC_DSP_INTX_FILT[1:0] | INTERPOLATION FILTER MODE SELECTION |
|---------------------------------|--|--|
| 0 | 00 (default) | Linear phase filters are used for the interpolation |
| 0 | 01 | Low latency filters are used for the interpolation |
| 0 | 10 | Ultra-low latency filters are used for the interpolation |
| 0 | 11 | Reserved (do not use this setting) |
| 1 | x | Low power filters are used for the interpolation |

7.3.7.2.6.1 Linear Phase Filters

The linear phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

7.3.7.2.6.1.1 Sampling Rate: 16 kHz or 14.7 kHz

図 7-34 and 図 7-35 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 16 kHz or 14.7 kHz. 表 7-35 lists the specifications for a interpolation filter with an 16-kHz or 14.7-kHz sampling rate.

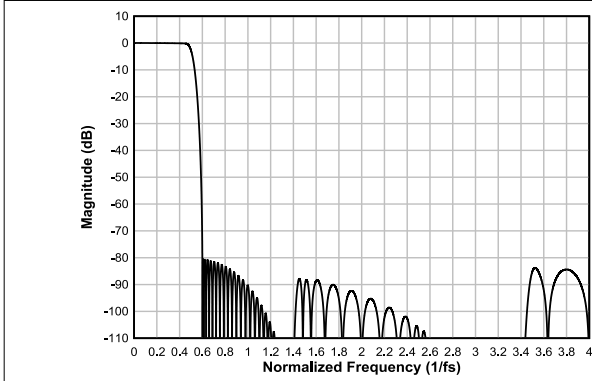


図 7-34. Linear Phase Interpolation Filter Magnitude Response

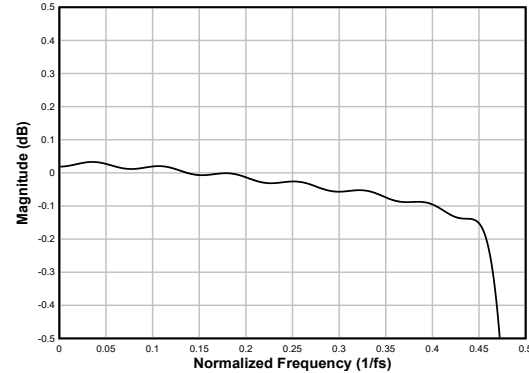


図 7-35. Linear Phase Interpolation Filter Pass-Band Ripple

表 7-35. Linear Phase Interpolation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_s$ | -0.17 | | 0.03 | dB |
| Stop-band attenuation | Frequency range is $0.6 \times f_s$ to $4 \times f_s$ | 80.4 | | | dB |
| | Frequency range is $4 \times f_s$ to $7.43 \times f_s$ | 86.9 | | | |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_s$ | | 16.0 | | $1/f_s$ |

7.3.7.2.6.1.2 Sampling Rate: 24 kHz or 22.05 kHz

図 7-36 and 図 7-37 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 24 kHz or 22.05 kHz. 表 7-36 lists the specifications for a interpolation filter with an 24-kHz or 22.05-kHz sampling rate.

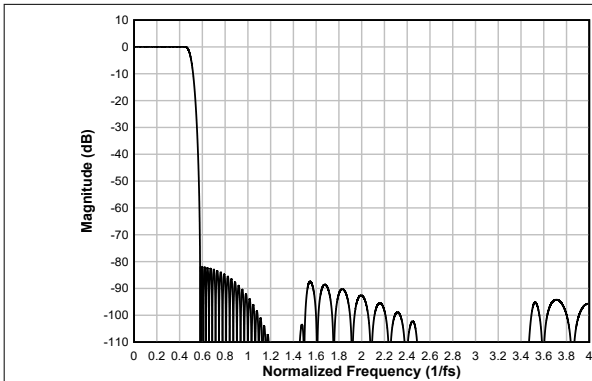


図 7-36. Linear Phase Interpolation Filter Magnitude Response

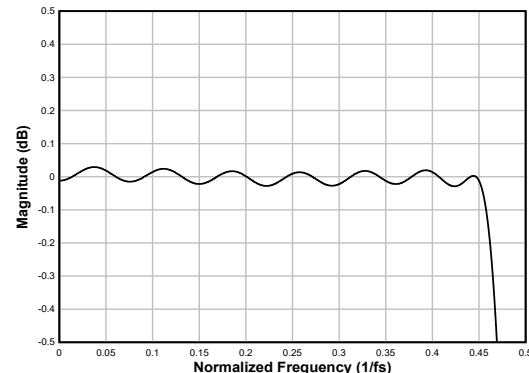


図 7-37. Linear Phase Interpolation Filter Pass-Band Ripple

表 7-36. Linear Phase Interpolation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|-------|-----|------|------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_s$ | -0.05 | | 0.03 | dB |
| Stop-band attenuation | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 81.9 | | | dB |
| | Frequency range is $4 \times f_s$ to $15.42 \times f_s$ | 87.6 | | | |

表 7-36. Linear Phase Interpolation Filter Specifications (続き)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-----|------|-----|---------|
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 17.6 | | $1/f_S$ |

7.3.7.2.6.1.3 Sampling Rate: 32 kHz or 29.4 kHz

図 7-38 and 図 7-39 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 32 kHz or 29.4 kHz. 表 7-37 lists the specifications for a interpolation filter with an 32-kHz or 29.4-kHz sampling rate.

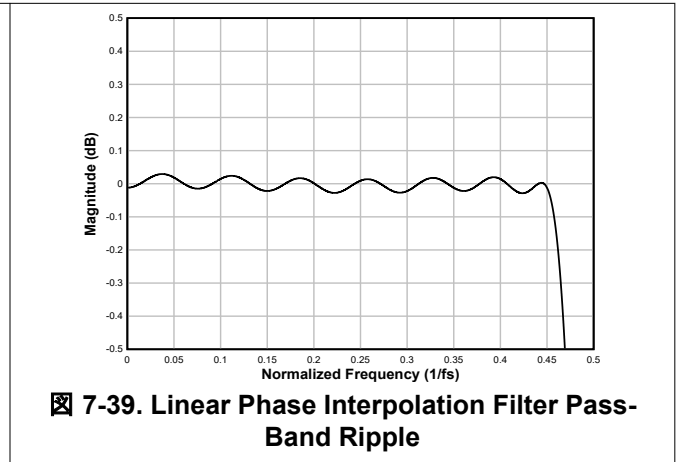
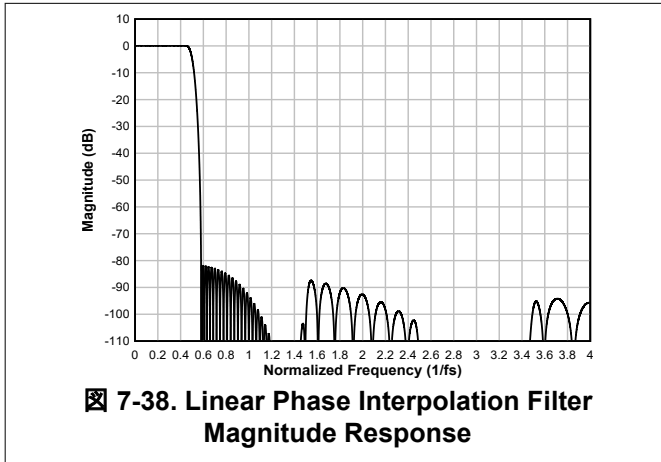
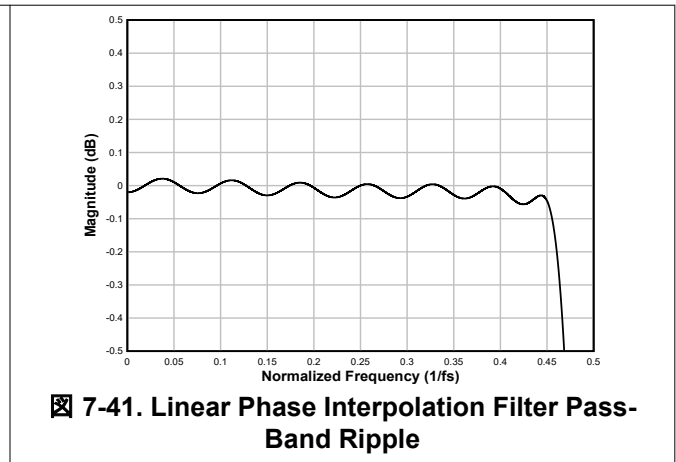
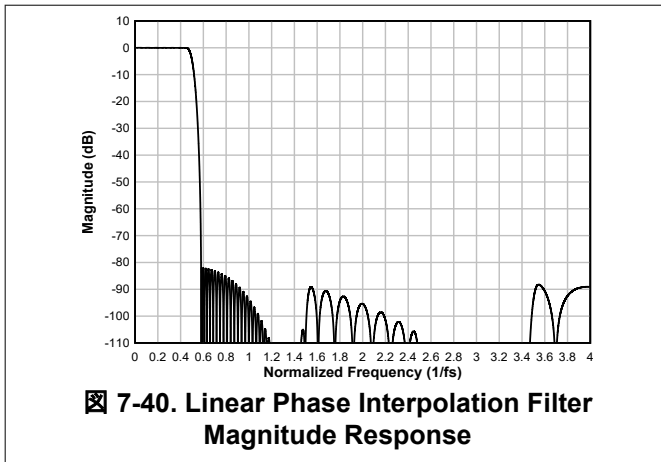


表 7-37. Linear Phase Interpolation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_S$ | -0.05 | | 0.03 | dB |
| Stop-band attenuation | Frequency range is $0.586 \times f_S$ to $4 \times f_S$ | 81.9 | | | |
| | Frequency range is $4 \times f_S$ to $15.42 \times f_S$ | 87.6 | | | |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 17.6 | | $1/f_S$ |

7.3.7.2.6.1.4 Sampling Rate: 48 kHz or 44.1 kHz

図 7-40 and 図 7-41 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 48 kHz or 44.1 kHz. 表 7-38 lists the specifications for a interpolation filter with an 48-kHz or 44.1-kHz sampling rate.





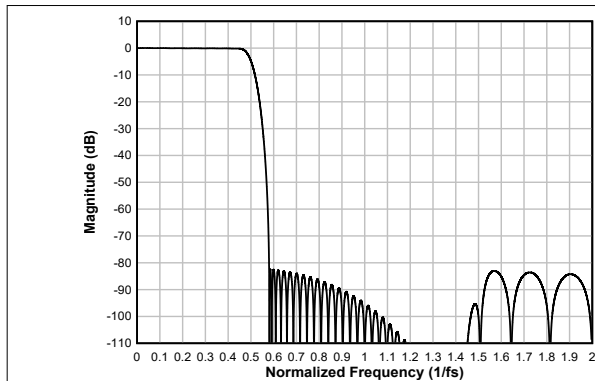
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表 7-38. Linear Phase Interpolation Filter Specifications

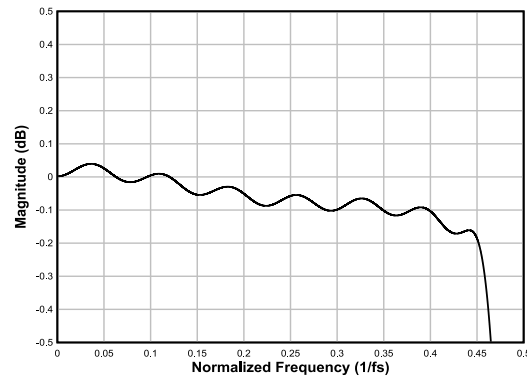
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.454 \times f_S$ | -0.08 | | 0.02 | dB |
| Stop-band attenuation | Frequency range is $0.585 \times f_S$ to $4 \times f_S$ | 82.0 | | | dB |
| | Frequency range is $4 \times f_S$ to $7.42 \times f_S$ onwards | 89.0 | | | |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 17.3 | | $1/f_S$ |

7.3.7.2.6.1.5 Sampling Rate: 96 kHz or 88.2 kHz

 7-42 and  7-43 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 96 kHz or 88.2 kHz. 表 7-39 lists the specifications for a interpolation filter with an 96-kHz or 88.2-kHz sampling rate.



 7-42. Linear Phase Interpolation Filter Magnitude Response





 7-43. Linear Phase Interpolation Filter Pass-Band Ripple

表 7-39. Linear Phase Interpolation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.452 \times f_S$ | -0.2 | | 0.04 | dB |
| Stop-band attenuation | Frequency range is $0.58 \times f_S$ to $3.42 \times f_S$ | 82.4 | | | dB |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$ | | 16.7 | | $1/f_S$ |

7.3.7.2.6.1.6 Sampling Rate: 384 kHz or 352.8 kHz

 7-44 and  7-45 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 384 kHz or 352.8 kHz. 表 7-40 lists the specifications for a interpolation filter with an 384-kHz or 352.8-kHz sampling rate.

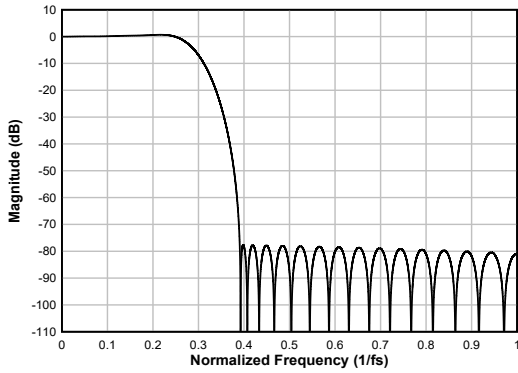


図 7-44. Linear Phase Interpolation Filter Magnitude Response

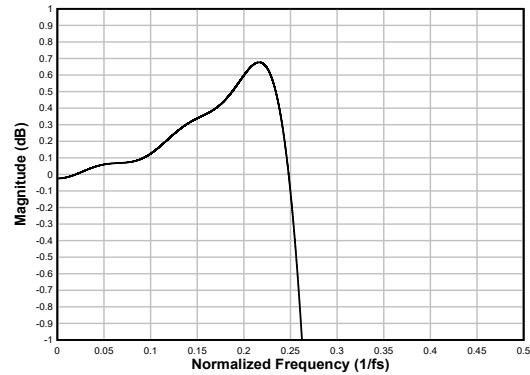


図 7-45. Linear Phase Interpolation Filter Pass-Band Ripple

表 7-40. Linear Phase Interpolation Filter Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple | Frequency range is 0 to $0.245 \times f_s$ | -0.03 | | 0.67 | dB |
| Stop-band attenuation | Frequency range is $0.391 \times f_s$ to $1.61 \times f_s$ | 77.6 | | | dB |
| Group delay or latency | Frequency range is 0 to $0.212 \times f_s$ | | 10.7 | | $1/f_s$ |

7.3.8 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device require host processor intervention and can be used to trigger interrupts to the host processor. One such event is an audio serial interface (ASI) bus error. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

- Invalid FSYNC frequency
- Invalid SBCLK to FSYNC ratio
- Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down all the record and playback channels as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the audio. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT_MASK0[7] (P1_R47_D7) is set low. The clock fault is also available for readback in the latched fault status register bit INT_LTCH0 (P1_R52), which is a read-only register. Reading the latched fault status register, INT_LTCH0, clears all latched fault status. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIOx or GPO1 pins and also can be configured as open-drain outputs so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as active low or active high polarity by setting the INT_POL (P0_R66_D7) register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT_EVENT[1:0] (P0_R66_D[6:5]) register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live-status registers to determine if the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in the DEV_STS0 (P0_R121) and DEV_STS1 (P0_R122) register bits.

The device has a multifunctional GPIO1 pin that can be configured for a desired specific function. 表 7-41 lists all possible allocations of these multifunctional pins for the various features.

表 7-41. Multifunction Pin Assignments

| ROW | PIN FUNCTION | GPIO1 | GPIO2 | GPO1 | GPI1 |
|-----|----------------------------------|------------------|-------------|-------------|-------------------|
| — | — | GPIO1_CFG | GPO2_CFG | GPO1_CFG | GPI1_CFG |
| — | — | P0_R10[7:4] | P0_R11[7:4] | P0_R12[7:4] | P0_R13[1] |
| A | Pin disabled | S ⁽¹⁾ | S (default) | S (default) | S (default) |
| B | General-purpose output (GPO) | S | S | S | NS ⁽²⁾ |
| C | Interrupt output (IRQ) | S (default) | S | S | NS |
| D | Power down for all ADC channels | S | S | NS | S |
| E | Power down for all DAC channels | S | S | NS | S |
| F | PDM clock output (PDMCLK) | S | S | S | NS |
| G | MiCBIAS on/off input (BIASEN) | S | S | NS | S |
| H | General-purpose input (GPI) | S | S | NS | S |
| I | Controller clock input (CCLK) | S | S | S | S |
| J | ASI daisy-chain input | S | S | NS | S |
| K | PDM data input 1 (PDMIN1) | S | S | NS | S |
| L | PDM data input 2 (PDMIN2) | S | S | NS | S |
| M | ASI DOUT | S | S | S | NS |
| N | ASI BCLK | S | S | S | S |
| O | ASI FSYNC | S | S | S | S |
| P | General Purpose Clock Out | S | S | S | NS |
| Q | ASI daisy-chain output | S | S | S | NS |
| R | Incremental ADC Conversion Start | S | S | NS | S |

- (1) S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.
 (2) NS means the feature mentioned in this row is *not supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.

Each GPOx or GPIOx pin can be independently set for the desired drive configurations setting using the GPIOx_DRV[2:0] or GPO1_DRV[2:0] register bits. 表 7-42 lists the drive configuration settings.

表 7-42. GPIO or GPOx Pins Drive Configuration Settings

| P0_R10_D[2:0] : GPIO1_DRV[2:0] | GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1 |
|--------------------------------|--|
| 000 | The GPIO1 pin is set to high impedance (floated) |
| 001 | The GPIO1 pin is set to be driven active low or active high |
| 010 (default) | The GPIO1 pin is set to be driven active low or weak high (on-chip pullup) |
| 011 | The GPIO1 pin is set to be driven active low or Hi-Z (floated) |
| 100 | The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high |
| 101 | The GPIO1 pin is set to be driven Hi-Z (floated) or active high |
| 110 and 111 | Reserved (do not use these settings) |

Similarly, the GPO1 pin can be configured using the GPO1_DRV(P0_R12) register bits.

When configured as a general-purpose output (GPO), the GPIOx or GPO1 pin values can be driven by writing the GPO_GPI_VAL (P0_R14) registers. The GPIO_MON bits (P0_R14_D[3:1]) can be used to readback the status of the GPIOx or GPI1 pin when configured as a general-purpose input (GPI).

7.4 Device Functional Modes

7.5 Register Maps

This section describes the control registers for the device in detail. All these registers are eight bits in width and allocated to device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using either I²C or SPI communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, page 1 and page 3. Page 0 is the default page setting at power up (and after a software reset). The device current page can be switch to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data N to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data M to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

7.5.1 TAC5212 Registers

表 7-43 lists the memory-mapped registers for the TAC5212 registers. All register offset addresses not listed in 表 7-43 should be considered as reserved locations and the register contents should not be modified.

表 7-43. TAC5212 Registers

| Address | Acronym | Register Name | Reset Value | Section |
|---------|----------------|------------------------------------|-------------|--|
| 0x0 | PAGE_CFG | Device page register | 0x00 | PAGE_CFG Register (Address = 0x0) [Reset = 0x00] |
| 0x1 | SW_RESET | Software reset register | 0x00 | SW_RESET Register (Address = 0x1) [Reset = 0x00] |
| 0x2 | VREF_CFG | | 0x00 | VREF_CFG Register (Address = 0x2) [Reset = 0x00] |
| 0x3 | AVDD_IOVDD_STS | | 0x00 | AVDD_IOVDD_STS Register (Address = 0x3) [Reset = 0x00] |
| 0x4 | MISC_CFG | | 0x00 | MISC_CFG Register (Address = 0x4) [Reset = 0x00] |
| 0x5 | MISC_CFG1 | | 0x15 | MISC_CFG1 Register (Address = 0x5) [Reset = 0x15] |
| 0x6 | DAC_CFG_A0 | DAC DEPOP configuration register | 0x55 | DAC_CFG_A0 Register (Address = 0x6) [Reset = 0x55] |
| 0x7 | MISC_CFG0 | Misc. configuration register | 0x00 | MISC_CFG0 Register (Address = 0x7) [Reset = 0x00] |
| 0xA | GPIO1_CFG0 | GPIO1 configuration register 0 | 0x32 | GPIO1_CFG0 Register (Address = 0xA) [Reset = 0x32] |
| 0xB | GPIO2_CFG0 | GPIO2 configuration register 0 | 0x00 | GPIO2_CFG0 Register (Address = 0xB) [Reset = 0x00] |
| 0xC | GPO1_CFG0 | GPO1 configuration register 0 | 0x00 | GPO1_CFG0 Register (Address = 0xC) [Reset = 0x00] |
| 0xD | GPI_CFG | GPI1 configuration register 0 | 0x00 | GPI_CFG Register (Address = 0xD) [Reset = 0x00] |
| 0xE | GPO_GPI_VAL | GPIO, GPO output value register | 0x00 | GPO_GPI_VAL Register (Address = 0xE) [Reset = 0x00] |
| 0xF | INTF_CFG0 | Interface configuration register 0 | 0x00 | INTF_CFG0 Register (Address = 0xF) [Reset = 0x00] |
| 0x10 | INTF_CFG1 | Interface configuration register 1 | 0x52 | INTF_CFG1 Register (Address = 0x10) [Reset = 0x52] |
| 0x11 | INTF_CFG2 | Interface configuration register 2 | 0x80 | INTF_CFG2 Register (Address = 0x11) [Reset = 0x80] |
| 0x12 | INTF_CFG3 | Interface configuration register 3 | 0x00 | INTF_CFG3 Register (Address = 0x12) [Reset = 0x00] |

表 7-43. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|-----------------|--|-------------|--|
| 0x13 | INTF_CFG4 | Interface configuration register 3 | 0x00 | INTF_CFG4 Register (Address = 0x13) [Reset = 0x00] |
| 0x14 | INTF_CFG5 | Interface configuration register 4 | 0x00 | INTF_CFG5 Register (Address = 0x14) [Reset = 0x00] |
| 0x15 | INTF_CFG6 | Interface configuration register 5 | 0x00 | INTF_CFG6 Register (Address = 0x15) [Reset = 0x00] |
| 0x18 | ASI_CFG0 | ASI configuration register 0 | 0x40 | ASI_CFG0 Register (Address = 0x18) [Reset = 0x40] |
| 0x19 | ASI_CFG1 | ASI configuration register 1 | 0x00 | ASI_CFG1 Register (Address = 0x19) [Reset = 0x00] |
| 0x1A | PASI_CFG0 | Primary ASI configuration register 0 | 0x30 | PASI_CFG0 Register (Address = 0x1A) [Reset = 0x30] |
| 0x1B | PASI_TX_CFG0 | PASI TX configuration register 0 | 0x00 | PASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00] |
| 0x1C | PASI_TX_CFG1 | PASI TX configuration register 1 | 0x00 | PASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00] |
| 0x1D | PASI_TX_CFG2 | PASI TX configuration register 2 | 0x00 | PASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00] |
| 0x1E | PASI_TX_CH1_CFG | PASI TX Channel 1 configuration register | 0x20 | PASI_TX_CH1_CFG Register (Address = 0x1E) [Reset = 0x20] |
| 0x1F | PASI_TX_CH2_CFG | PASI TX Channel 2 configuration register | 0x21 | PASI_TX_CH2_CFG Register (Address = 0x1F) [Reset = 0x21] |
| 0x20 | PASI_TX_CH3_CFG | PASI TX Channel 3 configuration register | 0x02 | PASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02] |
| 0x21 | PASI_TX_CH4_CFG | PASI TX Channel 4 configuration register | 0x03 | PASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03] |
| 0x22 | PASI_TX_CH5_CFG | PASI TX Channel 5 configuration register | 0x04 | PASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04] |
| 0x23 | PASI_TX_CH6_CFG | PASI TX Channel 6 configuration register | 0x05 | PASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05] |
| 0x24 | PASI_TX_CH7_CFG | PASI TX Channel 7 configuration register | 0x06 | PASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06] |
| 0x25 | PASI_TX_CH8_CFG | PASI TX Channel 8 configuration register | 0x07 | PASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07] |

表 7-43. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|-----------------|--|-------------|--|
| 0x26 | PASI_RX_CFG0 | PASI RX configuration register 0 | 0x00 | PASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00] |
| 0x27 | PASI_RX_CFG1 | PASI RX configuration register 1 | 0x00 | PASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00] |
| 0x28 | PASI_RX_CH1_CFG | PASI RX Channel 1 configuration register | 0x20 | PASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x20] |
| 0x29 | PASI_RX_CH2_CFG | PASI RX Channel 2 configuration register | 0x21 | PASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x21] |
| 0x2A | PASI_RX_CH3_CFG | PASI RX Channel 3 configuration register | 0x02 | PASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02] |
| 0x2B | PASI_RX_CH4_CFG | PASI RX Channel 4 configuration register | 0x03 | PASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03] |
| 0x2C | PASI_RX_CH5_CFG | PASI RX Channel 5 configuration register | 0x04 | PASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04] |
| 0x2D | PASI_RX_CH6_CFG | PASI RX Channel 6 configuration register | 0x05 | PASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05] |
| 0x2E | PASI_RX_CH7_CFG | PASI RX Channel 7 configuration register | 0x06 | PASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06] |
| 0x2F | PASI_RX_CH8_CFG | PASI RX Channel 8 configuration register | 0x07 | PASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07] |
| 0x32 | CLK_CFG0 | Clock configuration register 0 | 0x00 | CLK_CFG0 Register (Address = 0x32) [Reset = 0x00] |
| 0x33 | CLK_CFG1 | Clock configuration register 1 | 0x00 | CLK_CFG1 Register (Address = 0x33) [Reset = 0x00] |
| 0x34 | CLK_CFG2 | Clock configuration register 2 | 0x40 | CLK_CFG2 Register (Address = 0x34) [Reset = 0x40] |
| 0x35 | CNT_CLK_CFG0 | controller mode clock configuration register 0 | 0x00 | CNT_CLK_CFG0 Register (Address = 0x35) [Reset = 0x00] |
| 0x36 | CNT_CLK_CFG1 | controller mode clock configuration register 1 | 0x00 | CNT_CLK_CFG1 Register (Address = 0x36) [Reset = 0x00] |
| 0x37 | CNT_CLK_CFG2 | controller mode clock configuration register 2 | 0x20 | CNT_CLK_CFG2 Register (Address = 0x37) [Reset = 0x20] |

表 7-43. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|------------------|--|-------------|---|
| 0x38 | CNT_CLK_CFG3 | controller mode clock configuration register 3 | 0x00 | CNT_CLK_CFG3 Register (Address = 0x38) [Reset = 0x00] |
| 0x39 | CNT_CLK_CFG4 | controller mode clock configuration register 4 | 0x00 | CNT_CLK_CFG4 Register (Address = 0x39) [Reset = 0x00] |
| 0x3A | CNT_CLK_CFG5 | controller mode clock configuration register 5 | 0x00 | CNT_CLK_CFG5 Register (Address = 0x3A) [Reset = 0x00] |
| 0x3B | CNT_CLK_CFG6 | controller mode clock configuration register 6 | 0x00 | CNT_CLK_CFG6 Register (Address = 0x3B) [Reset = 0x00] |
| 0x3C | CLK_ERR_STS0 | Clock error and status register 0 | 0x00 | CLK_ERR_STS0 Register (Address = 0x3C) [Reset = 0x00] |
| 0x3D | CLK_ERR_STS1 | Clock error and status register 1 | 0x00 | CLK_ERR_STS1 Register (Address = 0x3D) [Reset = 0x00] |
| 0x3E | CLK_DET_STS0 | Clock ratio detection register 0 | 0x00 | CLK_DET_STS0 Register (Address = 0x3E) [Reset = 0x00] |
| 0x3F | CLK_DET_STS1 | Clock ratio detection register 1 | 0x00 | CLK_DET_STS1 Register (Address = 0x3F) [Reset = 0x00] |
| 0x40 | CLK_DET_STS2 | Clock ratio detection register 2 | 0x00 | CLK_DET_STS2 Register (Address = 0x40) [Reset = 0x00] |
| 0x41 | CLK_DET_STS3 | Clock ratio detection register 3 | 0x00 | CLK_DET_STS3 Register (Address = 0x41) [Reset = 0x00] |
| 0x42 | INT_CFG | Interrupt configuration register | 0x00 | INT_CFG Register (Address = 0x42) [Reset = 0x00] |
| 0x43 | DAC_FLT_CFG | Interrupt configuration register | 0x50 | DAC_FLT_CFG Register (Address = 0x43) [Reset = 0x50] |
| 0x4B | ADC_DAC_MISC_CFG | ADC overload Response configuration register | 0x00 | ADC_DAC_MISC_CFG Register (Address = 0x4B) [Reset = 0x00] |
| 0x4C | IADC_CFG | IADC configuration register | 0x5C | IADC_CFG Register (Address = 0x4C) [Reset = 0x5C] |
| 0x4D | VREF_CFG | Power tune configuration register 0 | 0x00 | VREF_CFG Register (Address = 0x4D) [Reset = 0x00] |
| 0x4E | PWR_TUNE_CFG0 | Power tune configuration register 0 | 0x00 | PWR_TUNE_CFG0 Register (Address = 0x4E) [Reset = 0x00] |
| 0x4F | PWR_TUNE_CFG1 | Power tune configuration register 1 | 0x00 | PWR_TUNE_CFG1 Register (Address = 0x4F) [Reset = 0x00] |

表 7-43. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|--------------|--|-------------|---|
| 0x50 | ADC_CH1_CFG0 | ADC Channel 1 configuration register 0 | 0x00 | ADC_CH1_CFG0 Register (Address = 0x50) [Reset = 0x00] |
| 0x51 | ADC_CH_CFG | ADC Channel configuration register | 0x00 | ADC_CH_CFG Register (Address = 0x51) [Reset = 0x00] |
| 0x52 | ADC_CH1_CFG2 | ADC Channel 1 configuration register 2 | 0xA1 | ADC_CH1_CFG2 Register (Address = 0x52) [Reset = 0xA1] |
| 0x53 | ADC_CH1_CFG3 | ADC Channel 1 configuration register 3 | 0x80 | ADC_CH1_CFG3 Register (Address = 0x53) [Reset = 0x80] |
| 0x54 | ADC_CH1_CFG4 | ADC Channel 1 configuration register 4 | 0x00 | ADC_CH1_CFG4 Register (Address = 0x54) [Reset = 0x00] |
| 0x55 | ADC_CH2_CFG0 | ADC Channel 2 configuration register 0 | 0x00 | ADC_CH2_CFG0 Register (Address = 0x55) [Reset = 0x00] |
| 0x57 | ADC_CH2_CFG2 | Channel 2 configuration register 2 | 0xA1 | ADC_CH2_CFG2 Register (Address = 0x57) [Reset = 0xA1] |
| 0x58 | ADC_CH2_CFG3 | ADC Channel 2 configuration register 3 | 0x80 | ADC_CH2_CFG3 Register (Address = 0x58) [Reset = 0x80] |
| 0x59 | ADC_CH2_CFG4 | ADC Channel 2 configuration register 4 | 0x00 | ADC_CH2_CFG4 Register (Address = 0x59) [Reset = 0x00] |
| 0x5A | ADC_CH3_CFG0 | ADC Channel 3 configuration register 0 | 0x00 | ADC_CH3_CFG0 Register (Address = 0x5A) [Reset = 0x00] |
| 0x5B | ADC_CH3_CFG2 | ADC Channel 3 configuration register 2 | 0xA1 | ADC_CH3_CFG2 Register (Address = 0x5B) [Reset = 0xA1] |
| 0x5C | ADC_CH3_CFG3 | ADC Channel 3 configuration register 3 | 0x80 | ADC_CH3_CFG3 Register (Address = 0x5C) [Reset = 0x80] |
| 0x5D | ADC_CH3_CFG4 | ADC Channel 3 configuration register 4 | 0x00 | ADC_CH3_CFG4 Register (Address = 0x5D) [Reset = 0x00] |
| 0x5E | ADC_CH4_CFG0 | ADC Channel 4 configuration register 0 | 0x00 | ADC_CH4_CFG0 Register (Address = 0x5E) [Reset = 0x00] |
| 0x5F | ADC_CH4_CFG2 | Channel 4 configuration register 2 | 0xA1 | ADC_CH4_CFG2 Register (Address = 0x5F) [Reset = 0xA1] |
| 0x60 | ADC_CH4_CFG3 | ADC Channel 4 configuration register 3 | 0x80 | ADC_CH4_CFG3 Register (Address = 0x60) [Reset = 0x80] |

表 7-43. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------------|---|-------------|--|
| 0x61 | ADC_CH4_CFG4 | ADC Channel 4 configuration register 4 | 0x00 | ADC_CH4_CFG4 Register (Address = 0x61) [Reset = 0x00] |
| 0x62 | ADC_CFG1 | ADC configuration register | 0x00 | ADC_CFG1 Register (Address = 0x62) [Reset = 0x00] |
| 0x64 | OUT1x_CFG0 | Channel OUT1x configuration register 0 | 0x20 | OUT1x_CFG0 Register (Address = 0x64) [Reset = 0x20] |
| 0x65 | OUT1x_CFG1 | Channel OUT1x configuration register 1 | 0x20 | OUT1x_CFG1 Register (Address = 0x65) [Reset = 0x20] |
| 0x66 | OUT1x_CFG2 | Channel OUT2x configuration register 2 | 0x20 | OUT1x_CFG2 Register (Address = 0x66) [Reset = 0x20] |
| 0x67 | DAC_CH1A_CFG0 | DAC Channel 1A configuration register 0 | 0xC9 | DAC_CH1A_CFG0 Register (Address = 0x67) [Reset = 0xC9] |
| 0x68 | DAC_CH1A_CFG1 | DAC Channel 1A configuration register 1 | 0x80 | DAC_CH1A_CFG1 Register (Address = 0x68) [Reset = 0x80] |
| 0x69 | DAC_CH1B_CFG0 | DAC Channel 1B configuration register 0 | 0xC9 | DAC_CH1B_CFG0 Register (Address = 0x69) [Reset = 0xC9] |
| 0x6A | DAC_CH1B_CFG1 | DAC Channel 1B configuration register 1 | 0x80 | DAC_CH1B_CFG1 Register (Address = 0x6A) [Reset = 0x80] |
| 0x6B | OUT2x_CFG0 | Channel OUT2x configuration register 0 | 0x20 | OUT2x_CFG0 Register (Address = 0x6B) [Reset = 0x20] |
| 0x6C | OUT2x_CFG1 | Channel OUT2x configuration register 1 | 0x20 | OUT2x_CFG1 Register (Address = 0x6C) [Reset = 0x20] |
| 0x6D | OUT2x_CFG2 | Channel OUT2x configuration register 2 | 0x20 | OUT2x_CFG2 Register (Address = 0x6D) [Reset = 0x20] |
| 0x6E | DAC_CH2A_CFG0 | DAC Channel 2A configuration register 0 | 0xC9 | DAC_CH2A_CFG0 Register (Address = 0x6E) [Reset = 0xC9] |
| 0x6F | DAC_CH2A_CFG1 | DAC Channel 2A configuration register 1 | 0x80 | DAC_CH2A_CFG1 Register (Address = 0x6F) [Reset = 0x80] |
| 0x70 | DAC_CH2B_CFG0 | DAC Channel 2B configuration register 0 | 0xC9 | DAC_CH2B_CFG0 Register (Address = 0x70) [Reset = 0xC9] |
| 0x71 | DAC_CH2B_CFG1 | DAC Channel 2B configuration register 1 | 0x80 | DAC_CH2B_CFG1 Register (Address = 0x71) [Reset = 0x80] |

表 7-43. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|--------------|---------------------------------------|-------------|--|
| 0x72 | DSP_CFG0 | DSP configuration register 0 | 0x18 | DSP_CFG0 Register (Address = 0x72) [Reset = 0x18] |
| 0x73 | DSP_CFG1 | DSP configuration register 0 | 0x18 | DSP_CFG1 Register (Address = 0x73) [Reset = 0x18] |
| 0x76 | CH_EN | Channel enable configuration register | 0xCC | CH_EN Register (Address = 0x76) [Reset = 0xCC] |
| 0x77 | DYN_PUPD_CFG | Power up configuration register | 0x00 | DYN_PUPD_CFG Register (Address = 0x77) [Reset = 0x00] |
| 0x78 | PWR_CFG | Power up configuration register | 0x00 | PWR_CFG Register (Address = 0x78) [Reset = 0x00] |
| 0x79 | DEV_STS0 | Device status value register 0 | 0x00 | DEV_STS0 Register (Address = 0x79) [Reset = 0x00] |
| 0x7A | DEV_STS1 | Device status value register 1 | 0x80 | DEV_STS1 Register (Address = 0x7A) [Reset = 0x80] |
| 0x7E | I2C_CKSUM | I ² C checksum register | 0x00 | I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00] |

7.5.1.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in 表 7-44.

Return to the [Summary Table](#).

The device memory map is divided into pages. This register sets the page.

表 7-44. PAGE_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-----------|--|
| 7-0 | PAGE[7:0] | R/W | 00000000b | These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255 |

7.5.1.2 SW_RESET Register (Address = 0x1) [Reset = 0x00]

SW_RESET is shown in 表 7-45.

Return to the [Summary Table](#).

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

表 7-45. SW_RESET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|----------|---------------------------------------|
| 7-1 | RESERVED | R | 0000000b | Reserved bits; Write only reset value |

表 7-45. SW_RESET Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 0 | SW_RESET | R/W | 0b | Software reset. This bit is self clearing. 0d = Do not reset 1d = Reset all registers to their reset values |

7.5.1.3 VREF_CFG Register (Address = 0x2) [Reset = 0x00]

VREF_CFG is shown in 表 7-46.

Return to the [Summary Table](#).

表 7-46. VREF_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-6 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 5-4 | VREF_QCHG[1:0] | R/W | 00b | The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω. 0d = VREF quick-charge duration of 3.5 ms (typical) 1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical) |
| 3 | SLEEP_EXIT_VREF_EN | R/W | 0b | Sleep mode exit configuration 0d = Only DREG Enabled 1d = DREG and VREF enabled |
| 2 | AVDD_MODE | R/W | 0b | AVDD mode configuration. 0d = Internal AREG regulator is used (Should be used for AVDD > 2V) 1d = AVDD 1.8V used directly for AREG (Strictly use this setting for AVDD 1.7V-1.9V) |
| 1 | IOVDD_IO_MODE | R/W | 0b | IOVDD mode configuration. 0d = IOVDD at 3.3V / 1.8V / 1.2V (speed limitation applicable for 1.8V and 1.2V) 1d = IOVDD at 1.8V / 1.2V only (no speed limitation - Strictly don't use this setting for IOVDD > 2V). |
| 0 | SLEEP_ENZ | R/W | 0b | Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode |

7.5.1.4 AVDD_IOVDD_STS Register (Address = 0x3) [Reset = 0x00]

AVDD_IOVDD_STS is shown in 表 7-47.

Return to the [Summary Table](#).

表 7-47. AVDD_IOVDD_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7 | AVDD_MODE_STS | R | 0b | AVDD mode status flag register. 0d = AVDD_MODE as per configured 1d = AVDD > 2V (AVDD_MODE forced to 0d) |
| 6 | IOVDD_IO_MODE_STS | R | 0b | IOVDD mode status flag register. 0d = IOVDD_MODE as per configured 1d = IOVDD > 2V (IOVDD_IO_MODE forced to 0d) |
| 5-2 | RESERVED | R | 0000b | Reserved bits; Write only reset values |
| 1 | BRWNOUT_SHDN_STS | R | 0b | Brwnout shutdown status 0d = No brwnout shutdown 1d = Brwnout shutdown |

表 7-47. AVDD_IOVDD_STS Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 0 | BRWNOUT_SHDN_EXIT_SLEEP | R/W | 0b | Brwnout shutdown sleep exit config 0d = Stay in sleep mode 1d = Exit sleep mode |

7.5.1.5 MISC_CFG Register (Address = 0x4) [Reset = 0x00]

MISC_CFG is shown in 表 7-48.

Return to the [Summary Table](#).

表 7-48. MISC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | I2C_BRDCAST_EN | R/W | 0b | I ² C broadcast addressing setting. 0d = I ² C broadcast mode disabled 1d = I ² C broadcast mode enabled; the I ² C target address is fixed with pin-controlled LSB bits as '0' |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.1.6 MISC_CFG1 Register (Address = 0x5) [Reset = 0x15]

MISC_CFG1 is shown in 表 7-49.

Return to the [Summary Table](#).

表 7-49. MISC_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-6 | INCAP_QCHG[1:0] | R/W | 00b | The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800 Ω. 0d = INxP, INxM quick-charge duration of 2.5 ms (typical) 1d = INxP, INxM quick-charge duration of 12.5 ms (typical) 2d = INxP, INxM quick-charge duration of 25 ms (typical) 3d = INxP, INxM quick-charge duration of 50 ms (typical) |
| 5-4 | SHDN_CFG[1:0] | R/W | 01b | Shutdown configuration. 0d = DREG is powered down immediately after IOVDD is deasserted 1d = DREG remains active to enable a clean shut down until a time-out(DREG_KA_TIME) is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved; Don't use |
| 3-2 | DREG_KA_TIME[1:0] | R/W | 01b | These bits set how long DREG remains active after IOVDD is deasserted. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) |
| 1-0 | RESERVED | R/W | 01b | Reserved bits; Write only reset values |

7.5.1.7 DAC_CFG_A0 Register (Address = 0x6) [Reset = 0x55]

DAC_CFG_A0 is shown in [表 7-50](#).

Return to the [Summary Table](#).

This register configures the device DAC DEPOP

表 7-50. DAC_CFG_A0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|---|
| 7-4 | RSERIES_DE_POP[3:0] | R/W | 0101b | HP Amp series resistor select config. 0d = Open 1d = 1K 2d = 2.5K 3d = 0.715k 4d = 10K 5d = 0.91k 6d = 2K 7d = 0.667k 8d = 20K Dont use Dont use Dont use Dont use Dont use Dont use Dont use |
| 3-0 | PWR_UP_TIME_DE_PO P[3:0] | R/W | 0101b | HP Amp external cap charging time config. 0d = 2ms 1d = 4ms 2d = 8ms 3d = 16ms 4d = 50ms 5d = 100ms 6d = 250ms 7d = 500ms 8d = 1s 9d = 5s 10d-15d = Reserved |

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7.5.1.8 MISC_CFG0 Register (Address = 0x7) [Reset = 0x00]

MISC_CFG0 is shown in [表 7-51](#).

Return to the [Summary Table](#).

This register configures the device Misc.

表 7-51. MISC_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7 | DAC_ST_W_CAP_DIS | R/W | 0b | DAC start with dc blocking capacitor discharge sequence. 0d = disable 1d = enable |
| 6 | DAC_DLYD_PWRUP | R/W | 0b | DAC power up delayed config. 0d = disable 1d = enable (Delay power-up by based on DAC_DLYD_PWRUP_TIME config) |
| 5 | DAC_DLYD_PWRUP_TIM E | R/W | 0b | DAC power up delayed time config. 0d = 128ms 1d = 512ms |

表 7-51. MISC_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | HW_RESET_ON_CLK_S TOP_EN | R/W | 0b | Assertion of Hard Reset when clock selected by CLK_SRC_SEL is not available for 2ms config 0d = disable 1d = enable |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset values |

7.5.1.9 GPIO1_CFG0 Register (Address = 0xA) [Reset = 0x32]

GPIO1_CFG0 is shown in 表 7-52.

Return to the [Summary Table](#).

This register is the GPIO1 configuration register 0.

表 7-52. GPIO1_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7-4 | GPIO1_CFG[3:0] | R/W | 0011b | GPIO1 configuration. 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose input (GPI) or any other input function 2d = GPIO1 is configured as a general-purpose output (GPO) 3d = GPIO1 is configured as a chip interrupt output (IRQ) 4d = GPIO1 is configured as a PDM clock output (PDMCLK) 5d = GPIO1 is configured as primary ASI DOUT 6d = GPIO1 is configured as primary ASI DOUT2 7d = GPIO1 is configured as secondary ASI DOUT 8d = GPIO1 is configured as secondary ASI DOUT2 9d = GPIO1 is configured as secondary ASI BCLK output 10d = GPIO1 is configured as secondary ASI FSYNC output 11d = GPIO1 is configured as general purpose CLKOUT 12d = GPIO1 is configured as PASI DOUT and SASI DOUT muxed 13d = GPIO1 is configured as DAISY_OUT for DIN Daisy 14d to 15d = Reserved |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2-0 | GPIO1_DRV[2:0] | R/W | 010b | GPIO1 output drive configuration. (Not valid if GPIO1_CFG configured as I ² S out) 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use |

7.5.1.10 GPIO2_CFG0 Register (Address = 0xB) [Reset = 0x00]

GPIO2_CFG0 is shown in 表 7-53.

Return to the [Summary Table](#).

This register is the GPIO2 configuration register 0.

表 7-53. GPIO2_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7-4 | GPIO2_CFG[3:0] | R/W | 0000b | GPIO2 configuration. 0d = GPIO2 is disabled 1d = GPIO2 is configured as a general-purpose input (GPI) or any other input function 2d = GPIO2 is configured as a general-purpose output (GPO) 3d = GPIO2 is configured as a chip interrupt output (IRQ) 4d = GPIO2 is configured as a PDM clock output (PDMCLK) 5d = GPIO2 is configured as primary ASI DOUT 6d = GPIO2 is configured as primary ASI DOUT2 7d = GPIO2 is configured as secondary ASI DOUT 8d = GPIO2 is configured as secondary ASI DOUT2 9d = GPIO2 is configured as secondary ASI BCLK output 10d = GPIO2 is configured as secondary ASI FSYNC output 11d = GPIO2 is configured as general purpose CLKOUT 12d = GPIO2 is configured as PASI DOUT and SASI DOUT muxed 13d = GPIO2 is configured as DAISY_OUT for DIN Daisy 14d to 15d = Reserved |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2-0 | GPIO2_DRV[2:0] | R/W | 000b | GPIO2 output drive configuration. (Not valid if GPIO2_CFG configured as I ² S out) 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use |

7.5.1.11 GPO1_CFG0 Register (Address = 0xC) [Reset = 0x00]

GPO1_CFG0 is shown in 表 7-54.

Return to the [Summary Table](#).

This register is the GPO1 configuration register 0.

表 7-54. GPO1_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7-4 | GPO1_CFG[3:0] | R/W | 0000b | GPO1 configuration. (For SPI mode, this pin act as DO and the below configuration settings are not applicable) 0d = GPO1 is disabled 1d = Reserved 2d = GPO1 is configured as a general-purpose output (GPO) 3d = GPO1 is configured as a chip interrupt output (IRQ) 4d = GPO1 is configured as a PDM clock output (PDMCLK) 5d = GPO1 is configured as primary ASI DOUT 6d = GPO1 is configured as primary ASI DOUT2 7d = GPO1 is configured as secondary ASI DOUT 8d = GPO1 is configured as secondary ASI DOUT2 9d = GPO1 is configured as secondary ASI BCLK output 10d = GPO1 is configured as secondary ASI FSYNC output 11d = GPO1 is configured as general purpose CLKOUT 12d = GPO1 is configured as PASI DOUT and SASI DOUT muxed 13d = GPO1 is configured as DAISY_OUT for DIN Daisy 14d to 15d = Reserved |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

表 7-54. GPO1_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 2-0 | GPO1_DRV[2:0] | R/W | 000b | GPO1 output drive configuration. (Not valid if GPO1_CFG configured as I ² S out) 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use |

7.5.1.12 GPI_CFG Register (Address = 0xD) [Reset = 0x00]

GPI_CFG is shown in 表 7-55.

Return to the [Summary Table](#).

This register is the GPI1 configuration register 0.

表 7-55. GPI_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|---------|---|
| 7-2 | RESERVED | R | 000000b | Reserved bits; Write only reset values |
| 1 | GPI1_CFG | R/W | 0b | GPI1 configuration.(For SPI mode, this pin act as CSZ and the below configuration settings are not applicable) 0d = GPI1 is disabled 1d = GPI1 is configured as a general-purpose input (GPI) or any other input function |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.1.13 GPO_GPI_VAL Register (Address = 0xE) [Reset = 0x00]

GPO_GPI_VAL is shown in 表 7-56.

Return to the [Summary Table](#).

This register is the GPIO and GPO output value register.

表 7-56. GPO_GPI_VAL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | GPIO1_VAL | R/W | 0b | GPIO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1 |
| 6 | GPIO2_VAL | R/W | 0b | GPIO2 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1 |
| 5 | GPO1_VAL | R/W | 0b | GPO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1 |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | GPIO1_MON | R | 0b | GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1 |
| 2 | GPIO2_MON | R | 0b | GPIO2 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1 |
| 1 | GPI1_MON | R | 0b | GPI1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1 |

表 7-56. GPO_GPI_VAL Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--------------------------------------|
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.14 INTF_CFG0 Register (Address = 0xF) [Reset = 0x00]

INTF_CFG0 is shown in [表 7-57](#).

Return to the [Summary Table](#).

This register is the interface configuration register 0.

表 7-57. INTF_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | CCLK_SEL[1:0] | R/W | 00b | CCLK select configuration. 0d = CCLK is disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 |
| 4-2 | PASI_DIN2_SEL[2:0] | R/W | 000b | Primary ASI DIN2 select configuration. 0d = Primary ASI DIN2 is disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = DOUT 5d = Primary ASI DIN 6d to 7d = Reserved |
| 1 | PASI_BCLK_SEL | R/W | 0b | Primary ASI BCLK select configuration. 0d = Primary ASI BCLK is BCLK 1d = Primary ASI BCLK is Secondary ASI BCLK |
| 0 | PASI_FSYNC_SEL | R/W | 0b | Primary ASI FSYNC select configuration. 0d = Primary ASI FSYNC is FSYNC 1d = Primary ASI FSYNC is Secondary ASI FSYNC |

7.5.1.15 INTF_CFG1 Register (Address = 0x10) [Reset = 0x52]

INTF_CFG1 is shown in [表 7-58](#).

Return to the [Summary Table](#).

This register is the interface configuration register 1.

表 7-58. INTF_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-4 | DOUT_SEL[3:0] | R/W | 0101b | DOUT select configuration. 0d = DOUT is disabled 1d = DOUT is configured as input 2d = DOUT is configured as a general-purpose output (GPO) 3d = DOUT is configured as a chip interrupt output (IRQ) 4d = DOUT is configured as a PDM clock output (PDMCLK) 5d = DOUT is configured as primary ASI DOUT 6d = DOUT is configured as primary ASI DOUT2 7d = DOUT is configured as secondary ASI DOUT 8d = DOUT is configured as secondary ASI DOUT2 9d = DOUT is configured as secondary ASI BCLK output 10d = DOUT is configured as secondary ASI FSYNC output 11d = DOUT is configured as general purpose CLKOUT 12d = DOUT is configured as PASI DOUT and SASI DOUT muxed 13d = DOUT is configured as DAISY_OUT for DIN Daisy 14d = DOUT is configured as DIN(LOOPBACK) 15d = Reserved |
| 3 | DOUT_VAL | R/W | 0b | DOUT output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1 |
| 2-0 | DOUT_DRV[2:0] | R/W | 010b | DOUT output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use |

7.5.1.16 INTF_CFG2 Register (Address = 0x11) [Reset = 0x80]

INTF_CFG2 is shown in 表 7-59.

Return to the [Summary Table](#).

This register is the interface configuration register 2.

表 7-59. INTF_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7 | PASI_DIN_EN | R/W | 1b | Primary ASI DIN enable configuration. 0d = Primary ASI DIN is disabled 1d = Primary ASI DIN is enabled |
| 6-4 | SASI_FSYNC_SEL[2:0] | R/W | 000b | Secondary ASI FSYNC select configuration. 0d = Secondary ASI disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = Reserved 5d = Primary ASI FSYNC 6d to 7d = Reserved |
| 3-1 | SASI_BCLK_SEL[2:0] | R/W | 000b | Secondary ASI BCLK select configuration. 0d = Secondary ASI disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = Reserved 5d = Primary ASI BCLK 6d to 7d = Reserved |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.17 INTF_CFG3 Register (Address = 0x12) [Reset = 0x00]

INTF_CFG3 is shown in [表 7-60](#).

Return to the [Summary Table](#).

This register is the interface configuration register 3.

表 7-60. INTF_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-5 | SASI_DIN_SEL[2:0] | R/W | 000b | Secondary ASI DIN select configuration. 0d = Secondary ASI DIN is disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = DOUT 5d = Primary ASI DIN 6d to 7d = Reserved |
| 4-2 | SASI_DIN2_SEL[2:0] | R/W | 000b | Secondary ASI DIN2 select configuration. 0d = Secondary ASI DIN2 is disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = DOUT 5d = Primary ASI DIN 6d to 7d = Reserved |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

7.5.1.18 INTF_CFG4 Register (Address = 0x13) [Reset = 0x00]

INTF_CFG4 is shown in [表 7-61](#).

Return to the [Summary Table](#).

This register is the interface configuration register 3.

表 7-61. INTF_CFG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7 | PDM_CH1_SEL | R/W | 0b | PDM select configuration for channel 1 of record path. 0d = Channel 1 is analog (ADC) type on the record path 1d = Channel 1 is digital (PDM) type on the record path |
| 6 | PDM_CH2_SEL | R/W | 0b | PDM select configuration for channel 2 of record path. 0d = Channel 2 is analog (ADC) type on the record path 1d = Channel 2 is digital (PDM) type on the record path |
| 5 | PDMDIN1_EDGE | R/W | 0b | PDMCLK latching edge used for channel 1 and channel 2 data. 0d = Channel 1 data are latched on the negative edge, channel 2 data are latched on the positive edge 1d = Channel 1 data are latched on the positive edge, channel 2 data are latched on the negative edge |
| 4 | PDMDIN2_EDGE | R/W | 0b | PDMCLK latching edge used for channel 3 and channel 4 data. 0d = Channel 3 data are latched on the negative edge, channel 4 data are latched on the positive edge 1d = Channel 3 data are latched on the positive edge, channel 4 data are latched on the negative edge |
| 3-2 | PDM_DIN1_SEL[1:0] | R/W | 00b | PDM data channels 1 and 2 select configuration. 0d = PDM data channels 1 and 2 are disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 |

表 7-61. INTF_CFG4 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 1-0 | PDM_DIN2_SEL[1:0] | R/W | 00b | PDM data channels 3 and 4 select configuration. 0d = PDM data channels 3 and 4 are disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 |

7.5.1.19 INTF_CFG5 Register (Address = 0x14) [Reset = 0x00]

INTF_CFG5 is shown in 表 7-62.

Return to the [Summary Table](#).

This register is the interface configuration register 4.

表 7-62. INTF_CFG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7 | PDM_DIN_SEL_OVRD | R/W | 0b | PDM data channels (1 and 2)/(3 and 4) select configuration override. 0d = No Override 1d = PDM_DIN1/2_SEL if configured as GPI1 will be overridden as DIN |
| 6 | DOOUT_WITH_DIN | R/W | 0b | DOOUT used as both ASI OUT and ASI IN 0d = DOOUT based on DOOUT_SEL 1d = DOOUT used as both ASI OUT and ASI DIN |
| 5-4 | PD_ADC_GPIO[1:0] | R/W | 00b | Power down ADC using GPIO select configuration.(ADC powered down if any one of the PD_ADC_GPIO/ADC_PDZ is configured power down) 0d = Power down ADC using GPIO is disabled 1d = Power down ADC using GPIO1 2d = Power down ADC using GPIO2 3d = Power down ADC using GPI1 |
| 3-2 | PD_DAC_GPIO[1:0] | R/W | 00b | Power down DAC using GPIO select configuration.(DAC powered down if any one of the PD_DAC_GPIO/DAC_PDZ is configured power down) 0d = Power down DAC using GPIO is disabled 1d = Power down DAC using GPIO1 2d = Power down DAC using GPIO2 3d = Power down DAC using GPI1 |
| 1 | PLIM_GPIO | R/W | 0b | PLIM using GPIO1 configuration. 0d = PLIM using GPIO1 is disabled 1d = PLIM using GPIO1 |
| 0 | GPA_GPIO | R/W | 0b | GPA using GPIO1 configuration. 0d = GPA using GPIO1 is disabled 1d = GPA using GPIO1 |

7.5.1.20 INTF_CFG6 Register (Address = 0x15) [Reset = 0x00]

INTF_CFG6 is shown in 表 7-63.

Return to the [Summary Table](#).

This register is the interface configuration register 5.

表 7-63. INTF_CFG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 7-6 | EN_MBIAS_GPIO[1:0] | R/W | 00b | Enable MICBIAS using GPIO select configuration. 0d = Enable MICBIAS using GPIO is disabled 1d = Enable MICBIAS using GPIO1 2d = Enable MICBIAS using GPIO2 3d = Enable MICBIAS using GPI1 |
| 5-4 | IADC_CONVST_GPIO[1:0]] | R/W | 00b | IADC conversion start using GPIO select configuration. 0d = Enable IADC using GPIO is disabled 1d = Enable IADC using GPIO1 2d = Enable IADC using GPIO2 3d = Enable IADC using GPI1 |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.21 ASI_CFG0 Register (Address = 0x18) [Reset = 0x40]

ASI_CFG0 is shown in 表 7-64.

Return to the [Summary Table](#).

This register is the ASI configuration register 0.

表 7-64. ASI_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7 | PASI_DIS | R/W | 0b | Disable or enable primary ASI (PASI). 0d = Primary ASI enabled 1d = Primary ASI disabled |
| 6 | SASI_DIS | R/W | 1b | Disable or enable secondary ASI (SASI). 0d = Secondary ASI enabled 1d = Secondary ASI disabled |
| 5 | SASI_CFG_GANG | R/W | 0b | All configurations of secondary ASI ganged with primary ASI. 0d = Secondary ASI has independent configurations 1d = Secondary ASI configurations same as primary ASI |
| 4-3 | DAISY_EN[1:0] | R/W | 00b | Daisy chain feature enable (only 1 ASI with 1 DOUT AND DIN available) 0d = Daisy chain disabled 1d = PASI daisy chain enabled (Secondary ASI not available) 2d = SASI daisy chain enabled (Primary ASI not available) 3d = Reserved; Don't use |
| 2-0 | DAISY_IN_SEL[2:0] | R/W | 000b | Daisy input select configuration. 0d = Daisy input disabled 1d = GPIO1 2d = GPIO2 3d = GPI1 4d = Reserved 5d = DIN 6d to 7d = Reserved |

7.5.1.22 ASI_CFG1 Register (Address = 0x19) [Reset = 0x00]

ASI_CFG1 is shown in 表 7-65.

Return to the [Summary Table](#).

This register is the ASI configuration register 1.

表 7-65. ASI_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-6 | ASI_DOUT_CFG[1:0] | R/W | 00b | ASI data output configuration. 0d = 1 data output for Primary ASI and 1 data output for Secondary ASI 1d = 2 data outputs for Primary ASI 2d = 2 data outputs for Secondary ASI 3d = Reserved; Don't use |
| 5-4 | ASI_DIN_CFG[1:0] | R/W | 00b | ASI data input configuration. 0d = 1 data input for Primary ASI and 1 data input for Secondary ASI 1d = 2 data inputs for Primary ASI 2d = 2 data inputs for Secondary ASI 3d = Reserved; Don't use |
| 3 | DAISY_DIR | R/W | 0b | Daisy direction configuration. 0d = ASI DOUT daisy 1d = ASI DIN daisy |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.23 PASI_CFG0 Register (Address = 0x1A) [Reset = 0x30]

PASI_CFG0 is shown in 表 7-66.

Return to the [Summary Table](#).

This register is the ASI configuration register 0.

表 7-66. PASI_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-6 | PASI_FORMAT[1:0] | R/W | 00b | Primary ASI protocol format. 0d = TDM mode 1d = I ² S mode 2d = LJ (left-justified) mode 3d = Reserved; Don't use |
| 5-4 | PASI_WLEN[1:0] | R/W | 11b | Primary ASI word or slot length. 0d = 16 bits (Recommended: This setting to be used with 10-kΩ input impedance configuration) 1d = 20 bits 2d = 24 bits 3d = 32 bits |
| 3 | PASI_FSYNC_POL | R/W | 0b | ASI FSYNC polarity (for PASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol |
| 2 | PASI_BCLK_POL | R/W | 0b | ASI BCLK polarity (for PASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol |
| 1 | PASI_BUS_ERR | R/W | 0b | ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection |
| 0 | PASI_BUS_ERR_RCOV | R/W | 0b | ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until host configures the device |

7.5.1.24 PASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00]

PASI_TX_CFG0 is shown in 表 7-67.

Return to the [Summary Table](#).

This register is the PASI TX configuration register 0.

表 7-67. PASI_TX_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7 | PASI_TX_EDGE | R/W | 0b | Primary ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 6 | PASI_TX_FILL | R/W | 0b | Primary ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles |
| 5 | PASI_TX_LSB | R/W | 0b | Primary ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle |
| 4-3 | PASI_TX_KEEPER[1:0] | R/W | 00b | Primary ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles |
| 2 | PASI_TX_USE_INT_FSYNC | R/W | 0b | Primary ASI uses internal FSYNC for output data generation in Controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data generation 1d = Use internal FSYNC for ASI protocol data generation |
| 1 | PASI_TX_USE_INT_BCLK | R/W | 0b | Primary ASI uses internal BCLK for output data generation in Controller mode configuration. 0d = Use external BCLK for ASI protocol data generation 1d = Use internal BCLK for ASI protocol data generation |
| 0 | PASI_TDM_PULSE_WIDTH | R/W | 0b | Primary ASI fsync pulse width in TDM format. (Valid for Controller mode) 0d = Fsync pulse is 1 bclk period wide 1d = Fsync pulse is 2 bclk period wide |

7.5.1.25 PASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00]

PASI_TX_CFG1 is shown in [表 7-68](#).

Return to the [Summary Table](#).

This register is the PASI TX configuration register 1.

表 7-68. PASI_TX_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-5 | RESERVED | R | 000b | Reserved bits; Write only reset values |

表 7-68. PASI_TX_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|--------|---|
| 4-0 | PASI_TX_OFFSET[4:0] | R/W | 00000b | Primary ASI output data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

7.5.1.26 PASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00]

PASI_TX_CFG2 is shown in 表 7-69.

Return to the [Summary Table](#).

This register is the PASI TX configuration register 2.

表 7-69. PASI_TX_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7 | PASI_TX_CH8_SEL | R/W | 0b | Primary ASI output channel 8 select. 0d = Primary ASI channel 8 output is on DOUT 1d = Primary ASI channel 8 output is on DOUT2 |
| 6 | PASI_TX_CH7_SEL | R/W | 0b | Primary ASI output channel 7 select. 0d = Primary ASI channel 7 output is on DOUT 1d = Primary ASI channel 7 output is on DOUT2 |
| 5 | PASI_TX_CH6_SEL | R/W | 0b | Primary ASI output channel 6 select. 0d = Primary ASI channel 6 output is on DOUT 1d = Primary ASI channel 6 output is on DOUT2 |
| 4 | PASI_TX_CH5_SEL | R/W | 0b | Primary ASI output channel 5 select. 0d = Primary ASI channel 5 output is on DOUT 1d = Primary ASI channel 5 output is on DOUT2 |
| 3 | PASI_TX_CH4_SEL | R/W | 0b | Primary ASI output channel 4 select. 0d = Primary ASI channel 4 output is on DOUT 1d = Primary ASI channel 4 output is on DOUT2 |
| 2 | PASI_TX_CH3_SEL | R/W | 0b | Primary ASI output channel 3 select. 0d = Primary ASI channel 3 output is on DOUT 1d = Primary ASI channel 3 output is on DOUT2 |
| 1 | PASI_TX_CH2_SEL | R/W | 0b | Primary ASI output channel 2 select. 0d = Primary ASI channel 2 output is on DOUT 1d = Primary ASI channel 2 output is on DOUT2 |
| 0 | PASI_TX_CH1_SEL | R/W | 0b | Primary ASI output channel 1 select. 0d = Primary ASI channel 1 output is on DOUT 1d = Primary ASI channel 1 output is on DOUT2 |

7.5.1.27 PASI_TX_CH1_CFG Register (Address = 0x1E) [Reset = 0x20]

PASI_TX_CH1_CFG is shown in 表 7-70.

Return to the [Summary Table](#).

This register is the PASI TX Channel 1 configuration register.

表 7-70. PASI_TX_CH1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_TX_CH1_CFG | R/W | 1b | Primary ASI output channel 1 configuration. 0d = Primary ASI channel 1 output is in a tri-state condition 1d = Primary ASI channel 1 output corresponds to ADC/PDM Channel 1 data |
| 4-0 | PASI_TX_CH1_SLOT_NUM[4:0] | R/W | 00000b | Primary ASI output channel 1 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.28 PASI_TX_CH2_CFG Register (Address = 0x1F) [Reset = 0x21]

PASI_TX_CH2_CFG is shown in 表 7-71.

Return to the [Summary Table](#).

This register is the PASI TX Channel 2 configuration register.

表 7-71. PASI_TX_CH2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_TX_CH2_CFG | R/W | 1b | Primary ASI output channel 2 configuration. 0d = Primary ASI channel 2 output is in a tri-state condition 1d = Primary ASI channel 2 output corresponds to ADC/PDM Channel 2 data |
| 4-0 | PASI_TX_CH2_SLOT_NUM[4:0] | R/W | 00001b | Primary ASI output channel 2 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.29 PASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02]

PASI_TX_CH3_CFG is shown in 表 7-72.

Return to the [Summary Table](#).

This register is the PASI TX Channel 3 configuration register.

表 7-72. PASI_TX_CH3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--------------------------------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |

表 7-72. PASI_TX_CH3_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 6-5 | PASI_TX_CH3_CFG[1:0] | R/W | 00b | Primary ASI output channel 3 configuration. 0d = Primary ASI channel 3 output is in a tri-state condition 1d = Primary ASI channel 3 output corresponds to PDM Channel 3 data 2d = Primary ASI channel 3 output corresponds to VBAT data 3d = Reserved |
| 4-0 | PASI_TX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Primary ASI output channel 3 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.30 PASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03]

PASI_TX_CH4_CFG is shown in [表 7-73](#).

Return to the [Summary Table](#).

This register is the PASI TX Channel 4 configuration register.

表 7-73. PASI_TX_CH4_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_TX_CH4_CFG[1:0] | R/W | 00b | Primary ASI output channel 4 configuration. 0d = Primary ASI channel 4 output is in a tri-state condition 1d = Primary ASI channel 4 output corresponds to PDM Channel 4 data 2d = Primary ASI channel 4 output corresponds to TEMP data 3d = Reserved |
| 4-0 | PASI_TX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Primary ASI output channel 4 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.31 PASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04]

PASI_TX_CH5_CFG is shown in [表 7-74](#).

Return to the [Summary Table](#).

This register is the PASI TX Channel 5 configuration register.

表 7-74. PASI_TX_CH5_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--------------------------------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |

表 7-74. PASI_TX_CH5_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 6-5 | PASI_TX_CH5_CFG[1:0] | R/W | 00b | Primary ASI output channel 5 configuration. 0d = Primary ASI channel 5 output is in a tri-state condition 1d = Primary ASI channel 5 output corresponds to ASI Input Channel 1 loopback data 2d = Primary ASI channel 5 output corresponds to echo reference Channel 1 data 3d = Reserved |
| 4-0 | PASI_TX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Primary ASI output channel 5 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.32 PASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05]

PASI_TX_CH6_CFG is shown in 表 7-75.

Return to the [Summary Table](#).

This register is the PASI TX Channel 6 configuration register.

表 7-75. PASI_TX_CH6_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_TX_CH6_CFG[1:0] | R/W | 00b | Primary ASI output channel 6 configuration. 0d = Primary ASI channel 6 output is in a tri-state condition 1d = Primary ASI channel 6 output corresponds to ASI Input Channel 2 loopback data 2d = Primary ASI channel 6 output corresponds to echo reference Channel 2 data 3d = Reserved |
| 4-0 | PASI_TX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Primary ASI output channel 6 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.33 PASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06]

PASI_TX_CH7_CFG is shown in 表 7-76.

Return to the [Summary Table](#).

This register is the PASI TX Channel 7 configuration register.

表 7-76. PASI_TX_CH7_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--------------------------------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |

表 7-76. PASI_TX_CH7_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 6-5 | PASI_TX_CH7_CFG[1:0] | R/W | 00b | Primary ASI output channel 7 configuration. 0d = Primary ASI channel 7 output is in a tri-state condition 1d = Primary ASI channel 7 output corresponds to {VBAT_WLby2, TEMP_WLby2} 2d = Primary ASI channel 7 output corresponds to {echo_ref_ch1, echo_ref_ch2} 3d = Reserved |
| 4-0 | PASI_TX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Primary ASI output channel 7 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.34 PASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07]

PASI_TX_CH8_CFG is shown in 表 7-77.

Return to the [Summary Table](#).

This register is the PASI TX Channel 8 configuration register.

表 7-77. PASI_TX_CH8_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_TX_CH8_CFG | R/W | 0b | Primary ASI output channel 8 configuration. 0d = Primary ASI channel 8 output is in a tri-state condition 1d = Primary ASI channel 8 output corresponds to ICLA data |
| 4-0 | PASI_TX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Primary ASI output channel 8 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.35 PASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00]

PASI_RX_CFG0 is shown in 表 7-78.

Return to the [Summary Table](#).

This register is the PASI RX configuration register 0.

表 7-78. PASI_RX_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | PASI_RX_EDGE | R/W | 0b | Primary ASI data input (on the primary and secondary data pin) receive edge. 0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting |

表 7-78. PASI_RX_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|--------|--|
| 6 | PASI_RX_USE_INT_FSYNC | R/W | 0b | Primary ASI uses internal FSYNC for input data latching in Controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data latching 1d = Use internal FSYNC for ASI protocol data latching |
| 5 | PASI_RX_USE_INT_BCLK | R/W | 0b | Primary ASI uses internal BCLK for input data latching in Controller mode configuration. 0d = Use external BCLK for ASI protocol data latching 1d = Use internal BCLK for ASI protocol data latching |
| 4-0 | PASI_RX_OFFSET[4:0] | R/W | 00000b | Primary ASI data input MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

7.5.1.36 PASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00]

PASI_RX_CFG1 is shown in 表 7-79.

Return to the [Summary Table](#).

This register is the PASI RX configuration register 1.

表 7-79. PASI_RX_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | PASI_RX_CH8_SEL | R/W | 0b | Primary ASI input channel 8 select. 0d = Primary ASI channel 8 input is on DIN 1d = Primary ASI channel 8 input is on DIN2 |
| 6 | PASI_RX_CH7_SEL | R/W | 0b | Primary ASI input channel 7 select. 0d = Primary ASI channel 7 input is on DIN 1d = Primary ASI channel 7 input is on DIN2 |
| 5 | PASI_RX_CH6_SEL | R/W | 0b | Primary ASI input channel 6 select. 0d = Primary ASI channel 6 input is on DIN 1d = Primary ASI channel 6 input is on DIN2 |
| 4 | PASI_RX_CH5_SEL | R/W | 0b | Primary ASI input channel 5 select. 0d = Primary ASI channel 5 input is on DIN 1d = Primary ASI channel 5 input is on DIN2 |
| 3 | PASI_RX_CH4_SEL | R/W | 0b | Primary ASI input channel 4 select. 0d = Primary ASI channel 4 input is on DIN 1d = Primary ASI channel 4 input is on DIN2 |
| 2 | PASI_RX_CH3_SEL | R/W | 0b | Primary ASI input channel 3 select. 0d = Primary ASI channel 3 input is on DIN 1d = Primary ASI channel 3 input is on DIN2 |
| 1 | PASI_RX_CH2_SEL | R/W | 0b | Primary ASI input channel 2 select. 0d = Primary ASI channel 2 input is on DIN 1d = Primary ASI channel 2 input is on DIN2 |
| 0 | PASI_RX_CH1_SEL | R/W | 0b | Primary ASI input channel 1 select. 0d = Primary ASI channel 1 input is on DIN 1d = Primary ASI channel 1 input is on DIN2 |

7.5.1.37 PASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x20]

 PASI_RX_CH1_CFG is shown in [表 7-80](#).

 Return to the [Summary Table](#).

This register is the PASI RX Channel 1 configuration register.

表 7-80. PASI_RX_CH1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH1_CFG | R/W | 1b | Primary ASI input channel 1 configuration. 0d = Primary ASI channel 1 input is disabled 1d = Primary ASI channel 1 input corresponds to DAC Channel 1 data |
| 4-0 | PASI_RX_CH1_SLOT_NUM[4:0] | R/W | 00000b | Primary ASI input channel 1 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.38 PASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x21]

 PASI_RX_CH2_CFG is shown in [表 7-81](#).

 Return to the [Summary Table](#).

This register is the PASI RX Channel 2 configuration register.

表 7-81. PASI_RX_CH2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH2_CFG | R/W | 1b | Primary ASI input channel 2 configuration. 0d = Primary ASI channel 2 input is disabled 1d = Primary ASI channel 2 input corresponds to DAC Channel 2 data |
| 4-0 | PASI_RX_CH2_SLOT_NUM[4:0] | R/W | 00001b | Primary ASI input channel 2 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.39 PASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02]

 PASI_RX_CH3_CFG is shown in [表 7-82](#).

 Return to the [Summary Table](#).

This register is the PASI RX Channel 3 configuration register.

表 7-82. PASI_RX_CH3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |

表 7-82. PASI_RX_CH3_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 5 | PASI_RX_CH3_CFG | R/W | 0b | Primary ASI input channel 3 configuration. 0d = Primary ASI channel 3 input is disabled 1d = Primary ASI channel 3 input corresponds to DAC Channel 3 data |
| 4-0 | PASI_RX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Primary ASI input channel 3 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.40 PASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03]

PASI_RX_CH4_CFG is shown in [表 7-83](#).

Return to the [Summary Table](#).

This register is the PASI RX Channel 4 configuration register.

表 7-83. PASI_RX_CH4_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH4_CFG | R/W | 0b | Primary ASI input channel 4 configuration. 0d = Primary ASI channel 4 input is disabled 1d = Primary ASI channel 4 input corresponds to DAC Channel 4 data |
| 4-0 | PASI_RX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Primary ASI input channel 4 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.41 PASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04]

PASI_RX_CH5_CFG is shown in [表 7-84](#).

Return to the [Summary Table](#).

This register is the PASI RX Channel 5 configuration register.

表 7-84. PASI_RX_CH5_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH5_CFG[1:0] | R/W | 00b | Primary ASI input channel 5 configuration. 0d = Primary ASI channel 5 input is disabled 1d = Primary ASI channel 5 input corresponds to DAC Channel 5 data 2d = Primary ASI channel 5 input corresponds to ADC Channel 1 output loopback 3d = Reserved |

表 7-84. PASI_RX_CH5_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 4-0 | PASI_RX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Primary ASI input channel 5 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.42 PASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05]

PASI_RX_CH6_CFG is shown in 表 7-85.

Return to the [Summary Table](#).

This register is the PASI RX Channel 6 configuration register.

表 7-85. PASI_RX_CH6_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH6_CFG[1:0] | R/W | 00b | Primary ASI input channel 6 configuration. 0d = Primary ASI channel 6 input is disabled 1d = Primary ASI channel 6 input corresponds to DAC Channel 6 data 2d = Primary ASI channel 6 input corresponds to ADC Channel 2 output loopback 3d = Primary ASI channel 6 input corresponds to ICLA device 1 data |
| 4-0 | PASI_RX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Primary ASI input channel 6 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.43 PASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06]

PASI_RX_CH7_CFG is shown in 表 7-86.

Return to the [Summary Table](#).

This register is the PASI RX Channel 7 configuration register.

表 7-86. PASI_RX_CH7_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH7_CFG[1:0] | R/W | 00b | Primary ASI input channel 7 configuration. 0d = Primary ASI channel 7 input is disabled 1d = Primary ASI channel 7 input corresponds to DAC Channel 7 data 2d = Primary ASI channel 7 input corresponds to ADC Channel 3 output loopback 3d = Primary ASI channel 7 input corresponds to ICLA device 2 data |

表 7-86. PASI_RX_CH7_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 4-0 | PASI_RX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Primary ASI input channel 7 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.44 PASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07]

PASI_RX_CH8_CFG is shown in 表 7-87.

Return to the [Summary Table](#).

This register is the PASI RX Channel 8 configuration register.

表 7-87. PASI_RX_CH8_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH8_CFG[1:0] | R/W | 00b | Primary ASI input channel 8 configuration. 0d = Primary ASI channel 8 input is disabled 1d = Primary ASI channel 8 input corresponds to DAC Channel 8 data 2d = Primary ASI channel 8 input corresponds to ADC Channel 4 output loopback 3d = Primary ASI channel 8 input corresponds to ICLA device 3 data |
| 4-0 | PASI_RX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Primary ASI input channel 8 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.1.45 CLK_CFG0 Register (Address = 0x32) [Reset = 0x00]

CLK_CFG0 is shown in 表 7-88.

Return to the [Summary Table](#).

This register is the clock configuration register 0.

表 7-88. CLK_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|---------|---|
| 7-2 | PASI_SAMP_RATE[5:0] | R/W | 000000b | Primary ASI sample rate configuration. -Typical (Allowed Range) 0d = Primary ASI sampling rate auto detected in the device 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved |
| 1 | PASI_FS_RATE_NO_LIM | R/W | 0b | Limit sampling rate to standard audio sample rates only. 0d = Standard audio rates with 1% tolerance supported using auto mode 1d = Standard audio rates with 5% tolerance supported using auto mode |
| 0 | CUSTOM_CLK_CFG | R/W | 0b | Custom clock configuration enable, all dividers and mux selects need to be manually configured. 0d = Auto clock configuration 1d = Custom clock configuration |

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7.5.1.46 CLK_CFG1 Register (Address = 0x33) [Reset = 0x00]

CLK_CFG1 is shown in 表 7-89.

Return to the [Summary Table](#).

This register is the clock configuration register 1.

表 7-89. CLK_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|---------|---|
| 7-2 | SASI_SAMP_RATE[5:0] | R/W | 000000b | Secondary ASI sample rate configuration. -Typical (Range) 0d = Secondary ASI sampling rate auto detected in the device 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved |
| 1 | SASI_FS_RATE_NO_LIM | R/W | 0b | Limit sampling rate to standard audio sample rates only. 0d = Standard audio rates with 1% tolerance supported using auto mode 1d = Standard audio rates with 5% tolerance supported using auto mode |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.47 CLK_CFG2 Register (Address = 0x34) [Reset = 0x40]

CLK_CFG2 is shown in 表 7-90.

Return to the [Summary Table](#).

This register is the clock configuration register 2.

表 7-90. CLK_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7 | PLL_DIS | R/W | 0b | Custom/Auto clock mode PLL setting. 0d = PLL is always enabled in custom clk mode/PLL is enabled based on DSP MIPS requirement in auto clock mode 1d = PLL is disabled |
| 6 | AUTO_PLL_FR_ALLOW | R/W | 1b | Allow the PLL to operate in fractional mode of operation. 0d = PLL fractional mode disabled 1d = PLL fractional mode allowed |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3-1 | CLK_SRC_SEL[2:0] | R/W | 000b | Input clock source select. 0d = Primary ASI BCLK is the input clock source 1d = CCLK synchronized with Primary ASI FSYNC is the input clock source 2d = Secondary ASI BCLK is the input clock source 3d = CCLK synchronized with Secondary ASI FSYNC is the input clock source 4d = Fixed CCLK frequency (used only in controller mode configuration) 5d = Internal oscillator clock is the input clock source 6d to 7d = Reserved |
| 0 | RATIO_CLK_EDGE | R/W | 0b | Edge selection for clock source ratio detection. 0d = Use rising edge of clock source to check ratio with primary or secondary FSYNC 1d = Use falling edge of clock source to check ratio with primary or secondary FSYNC |

7.5.1.48 CNT_CLK_CFG0 Register (Address = 0x35) [Reset = 0x00]

CNT_CLK_CFG0 is shown in [表 7-91](#).

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 0.

表 7-91. CNT_CLK_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|---------|--|
| 7-6 | PDM_CLK_CFG[1:0] | R/W | 00b | PDM_CLK configurattion. 0d = PDM_CLK is 2.8224 MHz or 3.072 MHz 1d = PDM_CLK is 1.4112 MHz or 1.536 MHz 2d = PDM_CLK is 705.6 kHz or 768 kHz 3d = PDM_CLK is 5.6448 MHz or 6.144 MHz |
| 5-0 | CCLK_FS_RATIO_MSB[5:0] | R/W | 000000b | Most significant bits for selecting the ratio between CCLK and primary/secondary ASI FSYNC with which CCLK is synchronized. 0d = Auto detect the ratio (assumption is CCLK is synchronized with primary/secondary FSYNC) 1d to 16383d = Ratio as per configuration |

7.5.1.49 CNT_CLK_CFG1 Register (Address = 0x36) [Reset = 0x00]

CNT_CLK_CFG1 is shown in [表 7-92](#).

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 1.

表 7-92. CNT_CLK_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-----------|--|
| 7-0 | CCLK_FS_RATIO_LSB[7:0] | R/W | 00000000b | LSB's for selecting the ratio between CCLK and primary/secondary ASI FSYNC with which CCLK is synchronized. 0d = Auto detect the ratio (assumption is CCLK is synchronized with primary/secondary FSYNC) 1d to 16383d = Ratio as per configuration |

7.5.1.50 CNT_CLK_CFG2 Register (Address = 0x37) [Reset = 0x20]

CNT_CLK_CFG2 is shown in 表 7-93.

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 2.

表 7-93. CNT_CLK_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7-5 | CCLK_FREQ_SEL[2:0] | R/W | 001b | These bits select the CCLK input frequency (used only in controller mode configuration). 0d = 12 MHz 1d = 12.288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 19.2 MHz 5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz |
| 4 | PASI_CNT_CFG | R/W | 0b | Primary ASI controller or target configuration 0d = Primary ASI in target configuration 1d = Primary ASI in controller configuration |
| 3 | SASI_CNT_CFG | R/W | 0b | Secondary ASI controller or target configuration 0d = Secondary ASI in target configuration 1d = Secondary ASI in controller configuration |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | FS_MODE | R/W | 0b | Sample rate setting (valid when the device is in controller mode). This is applicable for both PASI and SASI. 0d = sampling rate is a multiple (or submultiple) of 48 kHz 1d = sampling rate is a multiple (or submultiple) of 44.1 kHz |

7.5.1.51 CNT_CLK_CFG3 Register (Address = 0x38) [Reset = 0x00]

CNT_CLK_CFG3 is shown in 表 7-94.

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 3.

表 7-94. CNT_CLK_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------------|------|-------|---|
| 7 | PASI_USE_INT_BCLK_F OR_FSYNC | R/W | 0b | Use internal BCLK for FSYNC generation in PASI during controller mode configuration. 0d = Use external BCLK for FSYNC generation 1d = Use internal BCLK for FSYNC generation |
| 6 | PASI_INV_BCLK_FOR_F SYNC | R/W | 0b | Invert PASI BCLK polarity only for PASI FSYNC generation in controller mode configuration. 0d = Do not invert PASI BCLK polarity for PASI FSYNC generation 1d = Invert PASI BCLK polarity for PASI FSYNC generation |

表 7-94. CNT_CLK_CFG3 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|---------|--|
| 5-0 | PASI_BCLK_FS_RATIO_MSB[5:0] | R/W | 000000b | MSB bits for primary ASI BCLK to FSYNC ratio in controller mode. |

7.5.1.52 CNT_CLK_CFG4 Register (Address = 0x39) [Reset = 0x00]

CNT_CLK_CFG4 is shown in 表 7-95.

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 4.

表 7-95. CNT_CLK_CFG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-----------|--|
| 7-0 | PASI_BCLK_FS_RATIO_LSB[7:0] | R/W | 00000000b | LSB byte for primary ASI BCLK to FSYNC ratio in controller mode. |

7.5.1.53 CNT_CLK_CFG5 Register (Address = 0x3A) [Reset = 0x00]

CNT_CLK_CFG5 is shown in 表 7-96.

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 5.

表 7-96. CNT_CLK_CFG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|---------|---|
| 7 | SASI_USE_INT_BCLK_FOR_FSYNC | R/W | 0b | Use internal BCLK for FSYNC generation in SASI during controller mode configuration. 0d = Use external BCLK for FSYNC generation 1d = Use internal BCLK for FSYNC generation |
| 6 | SASI_INV_BCLK_FOR_FSYNC | R/W | 0b | Invert SASI BCLK polarity only for SASI FSYNC generation in controller mode configuration. 0d = Do not invert SASI BCLK polarity for SASI FSYNC generation 1d = Invert SASI BCLK polarity for SASI FSYNC generation |
| 5-0 | SASI_BCLK_FS_RATIO_MSB[5:0] | R/W | 000000b | MSB bits for secondary ASI BCLK to FSYNC ratio in controller mode. |

7.5.1.54 CNT_CLK_CFG6 Register (Address = 0x3B) [Reset = 0x00]

CNT_CLK_CFG6 is shown in 表 7-97.

Return to the [Summary Table](#).

This register is the controller mode clock configuration register 6.

表 7-97. CNT_CLK_CFG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-----------|--|
| 7-0 | SASI_BCLK_FS_RATIO_LSB[7:0] | R/W | 00000000b | LSB byte for secondary ASI BCLK to FSYNC ratio in controller mode. |

7.5.1.55 CLK_ERR_STS0 Register (Address = 0x3C) [Reset = 0x00]

CLK_ERR_STS0 is shown in 表 7-98.

Return to the [Summary Table](#).

This register is the clock error and status register 0.

表 7-98. CLK_ERR_STS0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|--|
| 7 | DSP_CLK_ERR | R | 0b | Flag indicating ratio error between FSYNC and selected clock source. 0d = No ratio error 1d = Ratio error between primary or secondary ASI FSYNC and selected clock source |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | SRC_RATIO_ERR | R | 0b | Flag indicating that SRC m:n ratio is unsupported. (not valid for custom m/n ratio config). 0d = m:n ratio supported 1d = Unsupported m:n ratio error |
| 3 | DEM_RATE_ERR | R | 0b | Flag indicating that clock configuration does not allow valid DEM rate. 0d = No DEM clock rate error 1d = DEM clock rate error in selected clock configuration |
| 2 | PDM_CLK_ERR | R | 0b | Flag indicating that clock configuration does not allow valid PDM clock generation. 0d = No PDM clock generation error 1d = PDM clock generation error in selected clock configuration |
| 1 | RESET_ON_CLK_STOP_DET_STS | R | 0b | Flag indicating that audio clock source stopped for atleast 1ms. 0d = No audio clock source error 1d = Audio clock source stopped for atleast 1ms |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.56 CLK_ERR_STS1 Register (Address = 0x3D) [Reset = 0x00]

CLK_ERR_STS1 is shown in 表 7-99.

Return to the [Summary Table](#).

This register is the clock error and status register 1.

表 7-99. CLK_ERR_STS1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|---|
| 7 | PASI_BCLK_FS_RATIO_ERR | R | 0b | Flag indicating PASI bclk fsync ratio error. 0d = No PASI bclk fsync ratio error 1d = PASI bclk fsync ratio error in selected clock configuration |
| 6 | SASI_BCLK_FS_RATIO_ERR | R | 0b | Flag indicating SASI bclk fsync ratio error. 0d = No SASI bclk fsync ratio error 1d = SASI bclk fsync ratio error in selected clock configuration |
| 5 | CCLK_FS_RATIO_ERR | R | 0b | Flag indicating CCLK fsync ratio error. 0d = No CCLK fsync ratio error 1d = CCLK fsync ratio error |
| 4 | PASI_FS_ERR | R | 0b | Flag indicating PASI FS rate change or halt error. 0d = No PASI FS error 1d = PASI FS rate change or halt detected |
| 3 | SASI_FS_ERR | R | 0b | Flag indicating SASI FS rate change or halt error. 0d = No SASI FS error 1d = SASI FS rate change or halt detected |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset values |

7.5.1.57 CLK_DET_STS0 Register (Address = 0x3E) [Reset = 0x00]

 CLK_DET_STS0 is shown in [表 7-100](#).

 Return to the [Summary Table](#).

This register is the clock ratio detection register 0.

表 7-100. CLK_DET_STS0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|---------|---|
| 7-2 | PASI_SAMP_RATE_STS[5:0] | R | 000000b | Primary ASI Sample rate detected status. 0d = Reserved 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved |
| 1-0 | PLL_MODE_STS[1:0] | R | 00b | PLL usage status. 0d = PLL used in integer mode 1d = PLL used in fractional mode 2d = PLL not used 3d = Reserved |

7.5.1.58 CLK_DET_STS1 Register (Address = 0x3F) [Reset = 0x00]

 CLK_DET_STS1 is shown in [表 7-101](#).

 Return to the [Summary Table](#).

This register is the clock ratio detection register 1.

表 7-101. CLK_DET_STS1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|---------|---|
| 7-2 | SASI_SAMP_RATE_STS[5:0] | R | 000000b | Secondary ASI Sample rate detected status. 0d = Reserved 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

7.5.1.59 CLK_DET_STS2 Register (Address = 0x40) [Reset = 0x00]

CLK_DET_STS2 is shown in 表 7-102.

Return to the [Summary Table](#).

This register is the clock ratio detection register 2.

表 7-102. CLK_DET_STS2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------------|------|---------|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5-0 | FS_CLKSRC_RATIO_DETECT_MSB_STS[5:0] | R | 000000b | MSB bits for primary ASI or secondary ASI FSYNC to clock source ratio detected. |

7.5.1.60 CLK_DET_STS3 Register (Address = 0x41) [Reset = 0x00]

CLK_DET_STS3 is shown in [表 7-103](#).

Return to the [Summary Table](#).

This register is the clock ratio detection register 3.

表 7-103. CLK_DET_STS3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------------|------|-----------|---|
| 7-0 | FS_CLKSRC_RATIO_DETECT_LSB_STS[7:0] | R | 00000000b | LSB byte for primary ASI or secondary ASI FSYNC to clock source ratio detected. |

7.5.1.61 INT_CFG Register (Address = 0x42) [Reset = 0x00]

INT_CFG is shown in [表 7-104](#).

Return to the [Summary Table](#).

This register is the interrupt configuration register.

表 7-104. INT_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7 | INT_POL | R/W | 0b | Interrupt polarity. 0b = Active low (IRQZ) 1b = Active high (IRQ) |
| 6-5 | INT_EVENT[1:0] | R/W | 00b | Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event 1d = INT asserts on any unmasked live interrupts event 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event |
| 4-3 | PD_ON_FLT_CFG[1:0] | R/W | 00b | Powerdown configuration during fault for chx and micbias. 0d = Faults are not considered for power down 1d = Only unmasked faults are considered for power down 2d = All faults are considered for powerdown 3d = Reserved |
| 2 | LTCH_READ_CFG | R/W | 0b | Interrupt latch registers readback configuration. 0b = All interrupts can be read through the LTCH registers 1b = Only unmasked interrupts can be read through the LTCH registers |
| 1 | PD_ON_FLT_RCV_CFG | R/W | 0b | Configuration for Powerdown ADC channels on fault 0b = Auto recovery, ADC channels are re-powered up when fault goes away 1b = Manual recovery, ADC channels are not re-powered up when fault goes away |
| 0 | LTCH_CLR_ON_READ | R/W | 0b | Cfgn for clearing LTCH register bits 0 = LTCH reg bits are cleared on reg read only if live status is zero 1 = LTCH reg bits are cleared on reg read irrespective of live status |

7.5.1.62 DAC_FLT_CFG Register (Address = 0x43) [Reset = 0x50]

DAC_FLT_CFG is shown in [表 7-105](#).

Return to the [Summary Table](#).

This register is the interrupt configuration register.

表 7-105. DAC_FLT_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | DAC_PD_ON_FLT_CFG[1:0] | R/W | 10b | Powerdown configuration during fault for DAC . 0d = Faults are not considered for power down 1d = Only unmasked faults are considered for power down 2d = All faults are considered for powerdown 3d = Reserved |
| 4 | DAC_PD_ON_FLT_RCV_CFG | R/W | 1b | Configuration for Powerdown DAC channels on fault 0b = Auto recovery, DAC channels are re-powered up when fault goes away 1b = Manual recovery, DAC channels are not re-powered up when fault goes away |
| 3 | OUT_CHx_PD_FLT_STS | R | 0b | Status for PD on OUTxx faults 0d = No DAC Channel is Powered Down due to fault/s 1d = Some DAC Channel is Powered Down due to fault/s |
| 2 | DAC_DIS_PD_W_PU | R/W | 0b | Disable power down on DRVR VG fault while powering up DAC 0b = Power down DAC on DRVR VG fault while power up 1b = Disable power down DAC on DRVR VG fault while power up |
| 1 | DAC_FLT_DET_DIS | R/W | 0b | DAC vg_fault/sc_fault detect config 0b = enable 1b = disable |
| 0 | AREG_SC_FLAG_DET_DIS | R/W | 0b | AREG short circuit detect config 0b = enable 1b = disable |

7.5.1.63 ADC_DAC_MISC_CFG Register (Address = 0x4B) [Reset = 0x00]

ADC_DAC_MISC_CFG is shown in [表 7-106](#).

Return to the [Summary Table](#).

Option to Mute ADC Channel in Overload Recovery Phase

表 7-106. ADC_DAC_MISC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | ADC_CH1_MUTE_ON_OVRLD | R/W | 0b | Mute ADC channel 1 while ADC1 is in Overload Recovery Phase 0b = Disable 1b = Enable |
| 3 | ADC_CH2_MUTE_ON_OVRLD | R/W | 0b | Mute ADC channel 2 while ADC2 is in Overload Recovery Phase 0b = Disable 1b = Enable |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset values |

7.5.1.64 IADC_CFG Register (Address = 0x4C) [Reset = 0x5C]

IADC_CFG is shown in [表 7-107](#).

Return to the [Summary Table](#).

This register is the IADC configuration register.

表 7-107. IADC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7-6 | IADC_NSkip_SEL[1:0] | R/W | 01b | IADC NSkip configuration. 0d = 384 mod clks 1d = 576 mod clks 2d = 896 mod clks 3d = 1024 mod clks 4d = 2048 mod clks 5d = 4096 mod clks 6d-7d = Reserved |
| 5-4 | IADC_NRESET_SEL[1:0] | R/W | 01b | IADC NRESET configuration. 0d = 50 mod clks 1d = 75 mod clks 2d = 100 mod clks 3d = 150 mod clks |
| 3-2 | IADC_OSR_SEL[1:0] | R/W | 11b | IADC OSR select configuration. 0d = 32 1d = 64 2d = 96 3d = 128 |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

7.5.1.65 PWR_TUNE_CFG0 Register (Address = 0x4E) [Reset = 0x00]

PWR_TUNE_CFG0 is shown in [表 7-108](#).

Return to the [Summary Table](#).

This register is configuration register for power tune configuration.

表 7-108. PWR_TUNE_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7 | ADC_CLK_BY2_MODE | R/W | 0b | ADC MOD CLK select configuration. 0d = MOD CLK 3MHz 1d = MOD CLK 1.5MHz |
| 6 | ADC_CIC_ORDER | R/W | 0b | ADC CIC order configuratoin. 0d = 5th order CIC 1d = 4th order CIC |
| 5 | ADC_FIR_BYPASS | R/W | 0b | ADC FIR bypass configuration. 0d = Bypass disable 1d = Bypass enable |
| 4-3 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 2 | ADC_LOW_PWR_FILTER | R/W | 0b | Low Power filter configuration for ADC 0d = Disable 1d = Enable |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

7.5.1.66 PWR_TUNE_CFG1 Register (Address = 0x4F) [Reset = 0x00]

PWR_TUNE_CFG1 is shown in [表 7-109](#).

Return to the [Summary Table](#).

This register is configuration register for power tune configuration.

表 7-109. PWR_TUNE_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7 | DAC_CLK_BY2_MODE | R/W | 0b | DAC MOD CLK select configuration. 0d = MOD CLK 3MHz 1d = MOD CLK 1.5MHz |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | DAC_FIR_SEG_BYPASS | R/W | 0b | DAC FIR and segmenter bypass configuration. 0d = Bypass disable 1d = Bypass enable |
| 4-3 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 2 | DAC_LOW_PWR_FILTER | R/W | 0b | Low Power Filter configuration for DAC 0d = Disable 1d = Enable |
| 1 | DAC_POWER_SCAL | R/W | 0b | DAC IREF select configuration. 0d = Vref/R 1d = Vref/2R |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.67 ADC_CH1_CFG0 Register (Address = 0x50) [Reset = 0x00]

ADC_CH1_CFG0 is shown in 表 7-110.

Return to the [Summary Table](#).

This register is configuration register 0 for ADC channel 1.

表 7-110. ADC_CH1_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 7-6 | ADC_CH1_INSRC[1:0] | R/W | 00b | ADC Channel 1 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Analog single-ended mux INP1 input 3d = Analog single-ended mux INM1 input |
| 5-4 | ADC_CH1_IMP[1:0] | R/W | 00b | ADC Channel 1 input impedance (applicable for the analog input). 0d = Typical 5-kΩ input impedance (For 4 Vrms case it will be 10-kΩ) 1d = Typical 10-kΩ input impedance 2d = Typical 40-kΩ input impedance 3d = Reserved |
| 3-2 | ADC_CH1_CM_TOL[1:0] | R/W | 00b | ADC Channel 1 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported 500 mVpp for single ended and 1 Vpp for differential configuration 2d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) 3d = Reserved |
| 1 | ADC_CH1_FULLSCALE_VAL | R/W | 0b | ADC Channel 1 Fullscale value for VREF=2.75 V (applicable for the analog input). 0d = 2 Vrms differential (1 Vrms for single ended operation) 1d = 4 Vrms differential (2 Vrms for single ended operation)(For AC-coupled configuration external biasing is required for input common mode, this mode supported with common mode variance tolerance rail to rail) (only 2.75 VREF supported, only supported in audio bandwidth mode) |

表 7-110. ADC_CH1_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 0 | ADC_CH1_BW_MODE | R/W | 0b | ADC Channel 1 band-width selection. coupling (applicable for the analog input). 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode) (Supported only for 40-kΩ input impedance case) |

7.5.1.68 ADC_CH_CFG Register (Address = 0x51) [Reset = 0x00]

ADC_CH_CFG is shown in 表 7-111.

Return to the [Summary Table](#).

This register is configuration register 0 for ADC channel .

表 7-111. ADC_CH_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 7 | IADC_EN | R/W | 0b | IADC enable configuration. 0d = IADC disabled 1d = IADC enabled |
| 6-5 | IADC_MODE[1:0] | R/W | 00b | IADC mode configuration. (for single channel mode channel select is controlled by ADC_INSRC SE_MUX config) 0d = One-shot single channel 1d = One-shot multi channel 2d = Sequential single channel 3d = Sequential multi channel |
| 4 | IADC_CONVST_ONESHOT | R/W | 0b | IADC conversion start one shor configuration. 0d = No conversion 1d = Start one shot conversion |
| 3 | IADC_STOP_SEQ_CONV | R/W | 0b | IADC stop sequential conversion configuration. 0d = Sequential conversion running 1d = Stop sequential conversion |
| 2 | IADC_ONESHOT_CONV_DONE_STS | R | 0b | IADC one shot conversion done configuration. 0d = Conversion not done 1d = One shot conversion done |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.1.69 ADC_CH1_CFG2 Register (Address = 0x52) [Reset = 0xA1]

ADC_CH1_CFG2 is shown in 表 7-112.

Return to the [Summary Table](#).

This register is configuration register 2 for ADC channel 1.

表 7-112. ADC_CH1_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|---|
| 7-0 | ADC_CH1_DVOL[7:0] | R/W | 10100001b | Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB |

7.5.1.70 ADC_CH1_CFG3 Register (Address = 0x53) [Reset = 0x80]

ADC_CH1_CFG3 is shown in 表 7-113.

Return to the [Summary Table](#).

This register is configuration register 3 for ADC channel 1.

表 7-113. ADC_CH1_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-4 | ADC_CH1_FGAIN[3:0] | R/W | 1000b | ADC channel 1 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.71 ADC_CH1_CFG4 Register (Address = 0x54) [Reset = 0x00]

ADC_CH1_CFG4 is shown in 表 7-114.

Return to the [Summary Table](#).

This register is configuration register 4 for ADC channel 1.

表 7-114. ADC_CH1_CFG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|---------|--|
| 7-2 | ADC_CH1_PCAL[5:0] | R/W | 000000b | ADC channel 1 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock |
| 1-0 | PCAL_ANA_DIG_SEL[1:0] | R/W | 00b | PCAL support configuration. 0d = Pcal for both Ana-Dig supported 1d = Pcal for only Ana 2d = Pcal for only Dig 3d = Reserved |

7.5.1.72 ADC_CH2_CFG0 Register (Address = 0x55) [Reset = 0x00]

ADC_CH2_CFG0 is shown in 表 7-115.

Return to the [Summary Table](#).

This register is configuration register 0 for ADC channel 2.

表 7-115. ADC_CH2_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-6 | ADC_CH2_INSRC[1:0] | R/W | 00b | ADC Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Analog single-ended mux IN2P input 3d = Analog single-ended mux IN2M input |

表 7-115. ADC_CH2_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 5-4 | ADC_CH2_IMP[1:0] | R/W | 00b | ADC Channel 2 input impedance (applicable for the analog input). 0d = Typical 5-kΩ input impedance (For 4 Vrms case it will be 10-kΩ) 1d = Typical 10-kΩ input impedance 2d = Typical 40-kΩ input impedance 3d = Reserved |
| 3-2 | ADC_CH2_CM_TOL[1:0] | R/W | 00b | ADC Channel 2 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported 500 mVpp for single ended and 1 Vpp for differential configuration 2d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) 3d = Reserved |
| 1 | ADC_CH2_FULLSCALE_VAL | R/W | 0b | ADC Channel 2 Fullscale value for VREF=2.75 V (applicable for the analog input). 0d = 2 Vrms differential (1 Vrms for single ended operation) 1d = 4 Vrms differential (2 Vrms for single ended operation)(For AC-coupled configuration external biasing is required for input common mode, this mode supported with common mode variance tolerance rail to rail) (only 2.75 VREF supported, only supported in audio band-width mode) |
| 0 | ADC_CH2_BW_MODE | R/W | 0b | ADC Channel 2 band-width selection. coupling (applicable for the analog input). 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode) (Supported only for 40-kΩ input impedance case) |

7.5.1.73 ADC_CH2_CFG2 Register (Address = 0x57) [Reset = 0xA1]

ADC_CH2_CFG2 is shown in 表 7-116.

Return to the [Summary Table](#).

This register is configuration register 2 for channel 2.

表 7-116. ADC_CH2_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|---|
| 7-0 | ADC_CH2_DVOL[7:0] | R/W | 10100001b | Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB |

7.5.1.74 ADC_CH2_CFG3 Register (Address = 0x58) [Reset = 0x80]

ADC_CH2_CFG3 is shown in 表 7-117.

Return to the [Summary Table](#).

This register is configuration register 3 for ADC Channel 2.

表 7-117. ADC_CH2_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-4 | ADC_CH2_FGAIN[3:0] | R/W | 1000b | ADC Channel 2 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.75 ADC_CH2_CFG4 Register (Address = 0x59) [Reset = 0x00]

ADC_CH2_CFG4 is shown in 表 7-118.

Return to the [Summary Table](#).

This register is configuration register 4 for ADC Channel 2.

表 7-118. ADC_CH2_CFG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|---------|--|
| 7-2 | ADC_CH2_PCAL[5:0] | R/W | 000000b | ADC Channel 2 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.1.76 ADC_CH3_CFG0 Register (Address = 0x5A) [Reset = 0x00]

ADC_CH3_CFG0 is shown in 表 7-119.

Return to the [Summary Table](#).

This register is configuration register 0 for ADC channel 3.

表 7-119. ADC_CH3_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|----------|---|
| 7 | ADC_CH3_CLONE | R/W | 0b | ADC Channel 3 input configuration. 0d = clone disabled 1d = Channel 3 Digital Filter Input is generated same as Channel 1 Digital Filter Input (Cloned Input) |
| 6-0 | RESERVED | R | 0000000b | Reserved bits; Write only reset value |

7.5.1.77 ADC_CH3_CFG2 Register (Address = 0x5B) [Reset = 0xA1]

ADC_CH3_CFG2 is shown in 表 7-120.

Return to the [Summary Table](#).

This register is configuration register 2 for ADC channel 3.

表 7-120. ADC_CH3_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|---|
| 7-0 | ADC_CH3_DVOL[7:0] | R/W | 10100001b | Channel 3 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB |

7.5.1.78 ADC_CH3_CFG3 Register (Address = 0x5C) [Reset = 0x80]

ADC_CH3_CFG3 is shown in 表 7-121.

Return to the [Summary Table](#).

This register is configuration register 3 for ADC channel 3.

表 7-121. ADC_CH3_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-4 | ADC_CH3_FGAIN[3:0] | R/W | 1000b | ADC channel 3 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.79 ADC_CH3_CFG4 Register (Address = 0x5D) [Reset = 0x00]

ADC_CH3_CFG4 is shown in 表 7-122.

Return to the [Summary Table](#).

This register is configuration register 4 for ADC channel 3.

表 7-122. ADC_CH3_CFG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|---------|--|
| 7-2 | ADC_CH3_PCAL[5:0] | R/W | 000000b | ADC channel 3 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.1.80 ADC_CH4_CFG0 Register (Address = 0x5E) [Reset = 0x00]

ADC_CH4_CFG0 is shown in 表 7-123.

Return to the [Summary Table](#).

This register is configuration register 0 for ADC Channel 4.

表 7-123. ADC_CH4_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|----------|---|
| 7 | ADC_CH4_CLONE | R/W | 0b | ADC Channel 4 input configuration. 0d = clone disabled 1d = Channel 4 Digital Filter Input is generated same as Channel 2 Digital Filter Input (Cloned Input) |
| 6-0 | RESERVED | R | 0000000b | Reserved bits; Write only reset value |

7.5.1.81 ADC_CH4_CFG2 Register (Address = 0x5F) [Reset = 0xA1]

ADC_CH4_CFG2 is shown in [表 7-124](#).

Return to the [Summary Table](#).

This register is configuration register 2 for channel 4.

表 7-124. ADC_CH4_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|---|
| 7-0 | ADC_CH4_DVOL[7:0] | R/W | 10100001b | Channel 4 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB |

7.5.1.82 ADC_CH4_CFG3 Register (Address = 0x60) [Reset = 0x80]

ADC_CH4_CFG3 is shown in [表 7-125](#).

Return to the [Summary Table](#).

This register is configuration register 3 for ADC Channel 4.

表 7-125. ADC_CH4_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 7-4 | ADC_CH4_FGAIN[3:0] | R/W | 1000b | ADC Channel 4 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.83 ADC_CH4_CFG4 Register (Address = 0x61) [Reset = 0x00]

ADC_CH4_CFG4 is shown in [表 7-126](#).

Return to the [Summary Table](#).

This register is configuration register 4 for ADC Channel 4.

表 7-126. ADC_CH4_CFG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|---------|--|
| 7-2 | ADC_CH4_PCAL[5:0] | R/W | 000000b | ADC Channel 4 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.1.84 ADC_CFG1 Register (Address = 0x62) [Reset = 0x00]

ADC_CFG1 is shown in [表 7-127](#).

Return to the [Summary Table](#).

This register is configuration register for ADC.

表 7-127. ADC_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 7-4 | ADC_PINCM_TRIM[3:0] | R/W | 0000b | Bit to tweak the Input common mode of the ADC channel in AC coupled mode, connects the following resistor from input pin to AVDD 0001 = 500k 0010 = 250k 0100 = 125k 1000 = 65k |
| 3 | ADC_QUANT_OFFSET_CAL_EN | R/W | 0b | Quantizer offset calibration mode |
| 2 | ADC_DATA_INVERT | R/W | 0b | Bit to Invert ADC Data |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.1.85 OUT1x_CFG0 Register (Address = 0x64) [Reset = 0x20]

OUT1x_CFG0 is shown in [表 7-128](#).

Return to the [Summary Table](#).

This register is configuration register 0 for Channel OUT1x.

表 7-128. OUT1x_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7-5 | OUT1x_SRC[2:0] | R/W | 001b | OUT1x Source Configuration. 0d = Output driver disabled 1d = Input from DAC signal chain 2d = Input from Analog bypass path 3d = Input from both DAC signal chain and Analog bypass path 4d = Independent input from both DAC signal chain and Analog bypass path (DAC -> OUT1P, IN1P -> OUT1M) 5d = Independent input from both DAC signal chain and Analog bypass path (IN1M -> OUT1P, DAC -> OUT1M) 6d-7d = Reserved; Don't use |

表 7-128. OUT1x_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 4-2 | OUT1x_CFG[2:0] | R/W | 000b | OUT1x DAC / Analog Bypass Routing Configuration. (Don't use if OUT1x_SRC configured 4d or 5d) 0d = Differential (DAC1AP + DAC1BP / IN1M -> OUT1P ; DAC1AM + DAC1BM / IN1P -> OUT1M) 1d = Stereo single-ended (DAC1A / IN1M -> OUT1P ; DAC1B / IN1P -> OUT1M) 2d = Mono single-ended with output at OUT1P only (DAC1A + DAC1B / IN1M-> OUT1P) 3d = Mono single-ended with output at OUT1M only (DAC1A + DAC1B / IN1P -> OUT1M) 4d = Pseudo differential with OUT1M as VCOM (DAC1A, DAC1B / IN1M -> OUT1P, VCOM -> OUT1M) 5d = Pseudo differential with OUT1M as VCOM and OUT2M for external sensing (DAC1A, DAC1B / IN1M -> OUT1P, VCOM -> OUT1M) 6d = Pseudo differential with OUT1P as VCOM (IN1P -> OUT1M, VCOM -> OUT1P) 7d = Reserved; Don't use |
| 1 | OUT1x_VCOM | R/W | 0b | Channel OUT1x VCOM configuration. 0d = $0.6 * V_{ref}$ (for 1.375V VREF mode alone as $0.654 * V_{ref}$) 1d = AVDD by 2 |
| 0 | OUT1x_LP_MODE | R/W | 0b | Low power mode of OUT1x channel. (only valid for OUT1x_SRC configured as DAC signal chain) (not valid for OUT1x_CFG configured as Stereo SE) 0d = Low power mode is disabled (3 dB higher perf) 1d = Low power mode is enabled |

7.5.1.86 OUT1x_CFG1 Register (Address = 0x65) [Reset = 0x20]

OUT1x_CFG1 is shown in 表 7-129.

Return to the [Summary Table](#).

This register is configuration register 1 for Channel OUT1x.

表 7-129. OUT1x_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7-6 | OUT1P_DRIVE[1:0] | R/W | 00b | Channel OUT1P drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug |
| 5-3 | OUT1P_LVL_CTRL[2:0] | R/W | 100b | Channel OUT1P level control configuration. 0d = 24 dB (only for DAC sigchain SE) 1d = 18 dB (only for DAC sigchain) 2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured) 3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured) 4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured) 5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured) 6d = -12 dB (available for Rin 4.4-k Ω only) 7d = Reserved; Don't use |
| 2 | AIN1M_BYP_IMP | R/W | 0b | AIN1M Analog Bypass input impedance. 0d = 4.4-k Ω 1d = 20-k Ω |
| 1 | AIN1x_BYP_CFG | R/W | 0b | IN1x Analog Bypass input config. 0d = FD / Pseudo Diff 1d = SE |

表 7-129. OUT1x_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 0 | DAC_CH1_BW_MODE | R/W | 0b | DAC Channel 1 band-width selection. 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode) |

7.5.1.87 OUT1x_CFG2 Register (Address = 0x66) [Reset = 0x20]

OUT1x_CFG2 is shown in 表 7-130.

Return to the [Summary Table](#).

This register is configuration register 2 for Channel OUT2x.

表 7-130. OUT1x_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7-6 | OUT1M_DRIVE[1:0] | R/W | 00b | Channel OUT1M drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug |
| 5-3 | OUT1M_LVL_CTRL[2:0] | R/W | 100b | Channel OUT1M level control configuration. 0d = 24 dB (only for DAC sigchain SE) 1d = 18 dB (only for DAC sigchain) 2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured) 3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured) 4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured) 5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured) 6d = -12 dB (available for Rin 4.4-kΩ only) 7d = Reserved; Don't use |
| 2 | AIN1P_BYP_IMP | R/W | 0b | AIN1P Analog Bypass input impedance. 0d = 4.4-kΩ 1d = 20-kΩ |
| 1 | DAC_CH1_FULLSCALE_VAL | R/W | 0b | DAC Channel 1 Fullscale value for VREF=2.75 V (applicable for the analog input). 0d = 2 Vrms differential (1 Vrms for single ended operation) 1d = 4 Vrms differential (2 Vrms for single ended operation) (For AC-coupled configuration external biasing is required for input common mode, this mode supported with common mode variance tolerance rail to rail) (only 2.75 VREF supported, only supported in audio band-width mode) |
| 0 | DAC_CH1_CM_TOL | R/W | 0b | DAC Channel 1 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) |

7.5.1.88 DAC_CH1A_CFG0 Register (Address = 0x67) [Reset = 0xC9]

DAC_CH1A_CFG0 is shown in 表 7-131.

Return to the [Summary Table](#).

This register is configuration register 0 for DAC channel 1A.

表 7-131. DAC_CH1A_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-----------|--|
| 7-0 | DAC_CH1A_DVOL[7:0] | R/W | 11001001b | Channel 1A digital volume control. 0d = Digital Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB |

7.5.1.89 DAC_CH1A_CFG1 Register (Address = 0x68) [Reset = 0x80]

DAC_CH1A_CFG1 is shown in 表 7-132.

Return to the [Summary Table](#).

This register is configuration register 1 for DAC channel 1A.

表 7-132. DAC_CH1A_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-4 | DAC_CH1A_FGAIN[3:0] | R/W | 1000b | DAC channel 1A fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.90 DAC_CH1B_CFG0 Register (Address = 0x69) [Reset = 0xC9]

DAC_CH1B_CFG0 is shown in 表 7-133.

Return to the [Summary Table](#).

This register is configuration register 0 for DAC channel 1B.

表 7-133. DAC_CH1B_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-----------|--|
| 7-0 | DAC_CH1B_DVOL[7:0] | R/W | 11001001b | Channel 1B digital volume control. 0d = Digital Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB |

7.5.1.91 DAC_CH1B_CFG1 Register (Address = 0x6A) [Reset = 0x80]

DAC_CH1B_CFG1 is shown in 表 7-134.

Return to the [Summary Table](#).

This register is configuration register 1 for DAC channel 1B.

表 7-134. DAC_CH1B_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-4 | DAC_CH1B_FGAIN[3:0] | R/W | 1000b | DAC channel 1B fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.92 OUT2x_CFG0 Register (Address = 0x6B) [Reset = 0x20]

OUT2x_CFG0 is shown in [表 7-135](#).

Return to the [Summary Table](#).

This register is configuration register 0 for Channel OUT2x.

表 7-135. OUT2x_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7-5 | OUT2x_SRC[2:0] | R/W | 001b | OUT2x Source Configuration. 0d = Output driver disabled 1d = Input from DAC signal chain 2d = Input from Analog bypass path 3d = Input from both DAC signal chain and Analog bypass path 4d = Independent input from both DAC signal chain and Analog bypass path (DAC -> OUT2P, IN2P -> OUT2M) 5d = Independent input from both DAC signal chain and Analog bypass path (IN2M -> OUT2P, DAC -> OUT2M) 6d-7d = Reserved; Don't use |
| 4-2 | OUT2x_CFG[2:0] | R/W | 000b | OUT2x DAC / Analog Bypass Routing Configuration. (Don't use if OUT1x_SRC configured 4d or 5d) 0d = Differential (DAC2AP + DAC2BP / IN2M -> OUT2P ; DAC2AM + DAC2BM / IN2P -> OUT2M) 1d = Stereo single-ended (DAC2A / IN2M -> OUT2P ; DAC2B / IN2P -> OUT2M) 2d = Mono single-ended with output at OUT2P only (DAC2A + DAC2B / IN2M -> OUT2P) 3d = Mono single-ended with output at OUT2M only (DAC2A + DAC2B / IN2P -> OUT2M) 4d = Pseudo differential with OUT2M as VCOM (DAC2A, DAC2B / IN2M -> OUT2P, VCOM -> OUT2M) 5d = Reserved; Don't use 6d = Pseudo differential with OUT2P as VCOM (IN2P -> OUT2M, VCOM -> OUT2P) 7d = Reserved; Don't use |
| 1 | OUT2x_VCOM | R/W | 0b | Channel OUT2x VCOM configuration. 0d = $0.6 * V_{ref}$ (for 1.375V VREF mode alone as $0.654 * V_{ref}$) 2d = AVDD by 2 |
| 0 | OUT2x_LP_MODE | R/W | 0b | Low power mode of OUT2x channel. (only valid for OUT2x_SRC configured as DAC signal chain) (not valid for OUT2x_CFG configured as Stereo SE) 0d = Low power mode is disabled (3 dB higher perf) 1d = Low power mode is enabled |

7.5.1.93 OUT2x_CFG1 Register (Address = 0x6C) [Reset = 0x20]

OUT2x_CFG1 is shown in [表 7-136](#).

Return to the [Summary Table](#).

This register is configuration register 1 for Channel OUT2x.

表 7-136. OUT2x_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-6 | OUT2P_DRIVE[1:0] | R/W | 00b | Channel OUT2P drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug |
| 5-3 | OUT2P_LVL_CTRL[2:0] | R/W | 100b | Channel OUT2P level control configuration 0d = 24 dB (only for DAC sigchain SE) 1d = 18 dB (only for DAC sigchain) 2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured) 3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured) 4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured) 5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured) 6d = -12 dB (available for Rin 4.4-kΩ only) 7d = Reserved; Don't use |
| 2 | AIN2M_BYP_IMP | R/W | 0b | AIN2M Analog Bypass input impedance. 0d = 4.4-kΩ 1d = 20-kΩ |
| 1 | AIN2x_BYP_CFG | R/W | 0b | IN2x Analog Bypass input config. 0d = FD / Pseudo Diff 1d = SE |
| 0 | DAC_CH2_BW_MODE | R/W | 0b | DAC Channel 2 band-width selection. 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode) |

7.5.1.94 OUT2x_CFG2 Register (Address = 0x6D) [Reset = 0x20]

OUT2x_CFG2 is shown in [表 7-137](#).

Return to the [Summary Table](#).

This register is configuration register 2 for Channel OUT2x.

表 7-137. OUT2x_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7-6 | OUT2M_DRIVE[1:0] | R/W | 00b | Channel OUT2M drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug |
| 5-3 | OUT2M_LVL_CTRL[2:0] | R/W | 100b | Channel OUT2M level control configuration. 0d = 24 dB (only for DAC sigchain SE) 1d = 18 dB (only for DAC sigchain) 2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured) 3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured) 4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured) 5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured) 6d = -12 dB (available for Rin 4.4-kΩ only) 7d = Reserved; Don't use |
| 2 | AIN2P_BYP_IMP | R/W | 0b | AIN2P Analog Bypass input impedance. 0d = 4.4-kΩ 1d = 20-kΩ |

表 7-137. OUT2x_CFG2 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 1 | DAC_CH2_FULLSCALE_VAL | R/W | 0b | DAC Channel 2 Fullscale value for VREF=2.75 V (applicable for the analog input). 0d = 2 Vrms differential (1 Vrms for single ended operation) 1d = 4 Vrms differential (2 Vrms for single ended operation) (For AC-coupled configuration external biasing is required for input common mode, this mode supported with common mode variance tolerance rail to rail) (only 2.75 VREF supported, only supported in audio bandwidth mode) |
| 0 | DAC_CH2_CM_TOL | R/W | 0b | DAC Channel 2 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) |

7.5.1.95 DAC_CH2A_CFG0 Register (Address = 0x6E) [Reset = 0xC9]

DAC_CH2A_CFG0 is shown in 表 7-138.

Return to the [Summary Table](#).

This register is configuration register 0 for DAC channel 2A.

表 7-138. DAC_CH2A_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-----------|--|
| 7-0 | DAC_CH2A_DVOL[7:0] | R/W | 11001001b | Channel 2A digital volume control. 0d = Digital Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB |

7.5.1.96 DAC_CH2A_CFG1 Register (Address = 0x6F) [Reset = 0x80]

DAC_CH2A_CFG1 is shown in 表 7-139.

Return to the [Summary Table](#).

This register is configuration register 1 for DAC channel 2A.

表 7-139. DAC_CH2A_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-4 | DAC_CH2A_FGAIN[3:0] | R/W | 1000b | DAC channel 2A fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.97 DAC_CH2B_CFG0 Register (Address = 0x70) [Reset = 0xC9]

DAC_CH2B_CFG0 is shown in [表 7-140](#).

Return to the [Summary Table](#).

This register is configuration register 0 for DAC channel 2B.

表 7-140. DAC_CH2B_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-----------|--|
| 7-0 | DAC_CH2B_DVOL[7:0] | R/W | 11001001b | Channel 2B digital volume control. 0d = Digital Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB |

7.5.1.98 DAC_CH2B_CFG1 Register (Address = 0x71) [Reset = 0x80]

DAC_CH2B_CFG1 is shown in [表 7-141](#).

Return to the [Summary Table](#).

This register is configuration register 1 for DAC channel 2B.

表 7-141. DAC_CH2B_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-4 | DAC_CH2B_FGAIN[3:0] | R/W | 1000b | DAC channel 2B fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.1.99 DSP_CFG0 Register (Address = 0x72) [Reset = 0x18]

DSP_CFG0 is shown in [表 7-142](#).

Return to the [Summary Table](#).

This register is the digital signal processor (DSP) configuration register 0.

表 7-142. DSP_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|--|
| 7-6 | ADC_DSP_DECI_FILT[1:0] | R/W | 00b | ADC channel decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved; Don't use |

表 7-142. DSP_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|--|
| 5-4 | ADC_DSP_HPF_SEL[1:0] | R/W | 01b | ADC channel high-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P10_R120-127 and P11_R8-11 set as the all-pass filter 1d = HPF with a cutoff of $0.00002 \times f_S$ (1 Hz at $f_S = 48$ kHz) is selected 2d = HPF with a cutoff of $0.00025 \times f_S$ (12 Hz at $f_S = 48$ kHz) is selected 3d = HPF with a cutoff of $0.002 \times f_S$ (96 Hz at $f_S = 48$ kHz) is selected |
| 3-2 | ADC_DSP_BQ_CFG[1:0] | R/W | 10b | Number of biquads per ADC channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel |
| 1 | ADC_DSP_DISABLE_SOFT_STEP | R/W | 0b | ADC Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled |
| 0 | ADC_DSP_DVOL_GANG | R/W | 0b | DVOL control ganged across ADC channels. 0d = Each channel has its own DVOL CTRL settings as programmed in the ADC_CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (ADC_CH1_DVOL) irrespective of whether channel 1 is turned on or not |

7.5.1.100 DSP_CFG1 Register (Address = 0x73) [Reset = 0x18]

DSP_CFG1 is shown in 表 7-143.

Return to the [Summary Table](#).

This register is the digital signal processor (DSP) configuration register 0.

表 7-143. DSP_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|--|
| 7-6 | DAC_DSP_INTX_FILTER[1:0] | R/W | 00b | DAC channel decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved; Don't use |
| 5-4 | DAC_DSP_HPF_SEL[1:0] | R/W | 01b | DAC channel high-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P17_R120-127 and P18_R8-11 set as the all-pass filter 1d = HPF with a cutoff of $0.00002 \times f_S$ (1 Hz at $f_S = 48$ kHz) is selected 2d = HPF with a cutoff of $0.00025 \times f_S$ (12 Hz at $f_S = 48$ kHz) is selected 3d = HPF with a cutoff of $0.002 \times f_S$ (96 Hz at $f_S = 48$ kHz) is selected |
| 3-2 | DAC_DSP_BQ_CFG[1:0] | R/W | 10b | Number of biquads per DAC channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel |
| 1 | DAC_DSP_DISABLE_SOFT_STEP | R/W | 0b | DAC Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled |

表 7-143. DSP_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 0 | DAC_DSP_DVOL_GANG | R/W | 0b | DVOL control ganged across DAC channels. 0d = Each DAC channel has its own DVOL CTRL settings as programmed in the DAC_CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (DAC_CH1_DVOL) irrespective of whether channel 1 is turned on or not |

7.5.1.101 CH_EN Register (Address = 0x76) [Reset = 0xCC]

CH_EN is shown in [表 7-144](#).

Return to the [Summary Table](#).

This register is the channel enable configuration register.

表 7-144. CH_EN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7 | IN_CH1_EN | R/W | 1b | Input channel 1 enable setting. 0d = Input channel 1 is disabled 1d = Input channel 1 is enabled |
| 6 | IN_CH2_EN | R/W | 1b | Input channel 2 enable setting. 0d = Input channel 2 is disabled 1d = Input channel 2 is enabled |
| 5 | IN_CH3_EN | R/W | 0b | Input channel 3 enable setting. 0d = Input channel 3 is disabled 1d = Input channel 3 is enabled |
| 4 | IN_CH4_EN | R/W | 0b | Input channel 4 enable setting. 0d = Input channel 4 is disabled 1d = Input channel 4 is enabled |
| 3 | OUT_CH1_EN | R/W | 1b | Output channel 1 enable setting. 0d = Output channel 1 is disabled 1d = Output channel 1 is enabled |
| 2 | OUT_CH2_EN | R/W | 1b | Output channel 2 enable setting. 0d = Output channel 2 is disabled 1d = Output channel 2 is enabled |
| 1 | OUT_CH3_EN | R/W | 0b | Output channel 3 enable setting. 0d = Output channel 3 is disabled 1d = Output channel 3 is enabled |
| 0 | OUT_CH4_EN | R/W | 0b | Output channel 4 enable setting. 0d = Output channel 4 is disabled 1d = Output channel 4 is enabled |

7.5.1.102 DYN_PUPD_CFG Register (Address = 0x77) [Reset = 0x00]

DYN_PUPD_CFG is shown in [表 7-145](#).

Return to the [Summary Table](#).

This register is the power-up configuration register.

表 7-145. DYN_PUPD_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7 | ADC_DYN_PUPD_EN | R/W | 0b | Dynamic channel power-up, power-down enable for record path. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on |

表 7-145. DYN_PUPD_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|---|
| 6 | ADC_DYN_MAXCH_SEL | R/W | 0b | Dynamic mode maximum channel select configuration for record path. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled |
| 5 | DAC_DYN_PUPD_EN | R/W | 0b | Dynamic channel power-up, power-down enable for playback path. 0d = Channel power-up, power-down is not supported if any channel playback is on 1d = Channel can be powered up or down individually, even if channel playback is on |
| 4 | DAC_DYN_MAXCH_SEL | R/W | 0b | Dynamic mode maximum channel select configuration for playback path. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled |
| 3 | DYN_PUPD_ADC_PDM_DIFF_CLK | R/W | 0b | Dynamic power-up power-down with different adc mod clock and pdm clock configuration. 0d = Same ADC MOD CLK and PDM CLK in dynamic pupd 1d = Different ADC MOD CLK and PDM CLK in dynamic pupd |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset value |

7.5.1.103 PWR_CFG Register (Address = 0x78) [Reset = 0x00]

PWR_CFG is shown in 表 7-146.

Return to the [Summary Table](#).

This register is the power-up configuration register.

表 7-146. PWR_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | ADC_PDZ | R/W | 0b | Power control for ADC and PDM channels. 0d = Power down all ADC and PDM channels 1d = Power up all enabled ADC and PDM channels |
| 6 | DAC_PDZ | R/W | 0b | Power control for DAC channels. 0d = Power down all DAC channels 1d = Power up all enabled DAC channels |
| 5 | MICBIAS_PDZ | R/W | 0b | Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | UAD_EN | R/W | 0b | Enable ultrasound activity detection (UAD) algorithm. 0d = UAD is disabled 1d = UAD is enabled |
| 2 | VAD_EN | R/W | 0b | Enable voice activity detection (VAD) algorithm. 0d = VAD is disabled 1d = VAD is enabled |
| 1 | UAG_EN | R/W | 0b | Enable ultrasound activity detection (UAG) algorithm. 0d = UAG is disabled 1d = UAG is enabled |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.1.104 DEV_STS0 Register (Address = 0x79) [Reset = 0x00]

DEV_STS0 is shown in [表 7-147](#).

Return to the [Summary Table](#).

This register is the device status value register 0.

表 7-147. DEV_STS0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | IN_CH1_STATUS | R | 0b | ADC or PDM channel 1 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up |
| 6 | IN_CH2_STATUS | R | 0b | ADC or PDM channel 2 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up |
| 5 | IN_CH3_STATUS | R | 0b | ADC or PDM channel 1 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up |
| 4 | IN_CH4_STATUS | R | 0b | ADC or PDM channel 2 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up |
| 3 | OUT_CH1_STATUS | R | 0b | DAC channel 1 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up |
| 2 | OUT_CH2_STATUS | R | 0b | DAC channel 2 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up |
| 1 | OUT_CH3_STATUS | R | 0b | DAC channel 3 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up |
| 0 | OUT_CH4_STATUS | R | 0b | DAC channel 4 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up |

7.5.1.105 DEV_STS1 Register (Address = 0x7A) [Reset = 0x80]

DEV_STS1 is shown in [表 7-148](#).

Return to the [Summary Table](#).

This register is the device status value register 1.

表 7-148. DEV_STS1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-5 | MODE_STS[2:0] | R | 100b | Device mode status. 0-3d = Reserved 4d = Device is in sleep mode or software shutdown mode 5d = Reserved 6d = Device is in active mode with all record and playback channels turned off 7d = Device is in active mode with at least one record or playback channel turned on |
| 4 | PLL_STS | R | 0b | PLL status. 0d = PLL is not enabled 1d = PLL is enabled |
| 3 | MICBIAS_STS | R | 0b | MICBIAS status. 0d = MICBIAS is disabled 1d = MICBIAS is enabled |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |

表 7-148. DEV_STS1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 1 | CHx_PD_FLT_STS | R | 0b | Status for PD on INxx Analog inputs faults 0d = No ADC Channel is Powered Down due to fault/s on Analog inputs INxx 1d = Some ADC Channel is Powered Down due to fault/s on Analog inputs INxx |
| 0 | ALL_CHx_PD_FLT_STS | R | 0b | Status for PD on Micbias faults 0d = No ADC Channel is Powered Down due to fault/s related to Micbias 1d = All ADC Channels are Powered Down due to fault/s related to Micbias |

7.5.1.106 I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00]

I2C_CKSUM is shown in [表 7-149](#).

Return to the [Summary Table](#).

This register returns the I²C transactions checksum value.

表 7-149. I2C_CKSUM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-----------|--|
| 7-0 | I2C_CKSUM[7:0] | R/W | 00000000b | These bits return the I ² C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages. |

7.5.2 TAC5212 Registers

表 7-150 lists the memory-mapped registers for the TAC5212 registers. All register offset addresses not listed in 表 7-150 should be considered as reserved locations and the register contents should not be modified.

表 7-150. TAC5212 Registers

| Address | Acronym | Register Name | Reset Value | Section |
|---------|----------------|---|-------------|---|
| 0x0 | PAGE_CFG | Device page register | 0x00 | PAGE_CFG Register (Address = 0x0) [Reset = 0x00] |
| 0x3 | DSP_CFG0 | | 0x00 | DSP_CFG0 Register (Address = 0x3) [Reset = 0x00] |
| 0xD | CLK_CFG0 | | 0x00 | CLK_CFG0 Register (Address = 0xD) [Reset = 0x00] |
| 0xE | CHANNEL_CFG1 | | 0x00 | CHANNEL_CFG1 Register (Address = 0xE) [Reset = 0x00] |
| 0xF | CHANNEL_CFG2 | | 0x00 | CHANNEL_CFG2 Register (Address = 0xF) [Reset = 0x00] |
| 0x17 | SRC_CFG0 | SRC configuration register 1 | 0x00 | SRC_CFG0 Register (Address = 0x17) [Reset = 0x00] |
| 0x18 | SRC_CFG1 | SRC configuration register 2 | 0x00 | SRC_CFG1 Register (Address = 0x18) [Reset = 0x00] |
| 0x19 | JACK_DET_CFG0 | JACK DET configuration register 0 | 0x00 | JACK_DET_CFG0 Register (Address = 0x19) [Reset = 0x00] |
| 0x1A | JACK_DET_CFG1 | JACK DET configuration register 1 | 0x00 | JACK_DET_CFG1 Register (Address = 0x1A) [Reset = 0x00] |
| 0x1B | JACK_DET_CFG2 | JACK DET configuration register 2 | 0x00 | JACK_DET_CFG2 Register (Address = 0x1B) [Reset = 0x00] |
| 0x1C | JACK_DET_CFG3 | JACK DET configuration register 3 | 0x00 | JACK_DET_CFG3 Register (Address = 0x1C) [Reset = 0x00] |
| 0x1E | LPAD_CFG1 | LPAD | 0x20 | LPAD_CFG1 Register (Address = 0x1E) [Reset = 0x20] |
| 0x1F | LPSG_CFG1 | LPSG | 0x80 | LPSG_CFG1 Register (Address = 0x1F) [Reset = 0x80] |
| 0x20 | LPAD_LPSG_CFG1 | LPAD and LPSG common configuration register 1 | 0x00 | LPAD_LPSG_CFG1 Register (Address = 0x20) [Reset = 0x00] |
| 0x23 | LIMITER_CFG | Limiter configuration register 2 | 0x00 | LIMITER_CFG Register (Address = 0x23) [Reset = 0x00] |
| 0x24 | AGC_DRC_CFG | AGC_DRC configuration register 2 | 0x00 | AGC_DRC_CFG Register (Address = 0x24) [Reset = 0x00] |

表 7-150. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|--------------|---------------------------------------|-------------|---|
| 0x2B | PLIM_CFG0 | PLIM configuration register 0 | 0x00 | PLIM_CFG0 Register (Address = 0x2B) [Reset = 0x00] |
| 0x2C | MIXER_CFG0 | MISC configuration register 0 | 0x00 | MIXER_CFG0 Register (Address = 0x2C) [Reset = 0x00] |
| 0x2D | MISC_CFG0 | MISC configuration register 0 | 0x00 | MISC_CFG0 Register (Address = 0x2D) [Reset = 0x00] |
| 0x2E | BRWNOUT | | 0xBF | BRWNOUT Register (Address = 0x2E) [Reset = 0xBF] |
| 0x2F | INT_MASK0 | Interrupt Mask Register-0 | 0xFF | INT_MASK0 Register (Address = 0x2F) [Reset = 0xFF] |
| 0x32 | INT_MASK4 | Interrupt Mask Register-3 | 0x00 | INT_MASK4 Register (Address = 0x32) [Reset = 0x00] |
| 0x33 | INT_MASK5 | Interrupt Mask Register-3 | 0x30 | INT_MASK5 Register (Address = 0x33) [Reset = 0x30] |
| 0x34 | INT_LTCH0 | Latched Interrupt Readback Register-0 | 0x00 | INT_LTCH0 Register (Address = 0x34) [Reset = 0x00] |
| 0x35 | CHx_LTCH | Summary of Diagnostics | 0x00 | CHx_LTCH Register (Address = 0x35) [Reset = 0x00] |
| 0x38 | OUT_CH1_LTCH | | 0x00 | OUT_CH1_LTCH Register (Address = 0x38) [Reset = 0x00] |
| 0x39 | OUT_CH2_LTCH | | 0x00 | OUT_CH2_LTCH Register (Address = 0x39) [Reset = 0x00] |
| 0x3A | INT_LTCH1 | Latched Interrupt Readback Register-0 | 0x00 | INT_LTCH1 Register (Address = 0x3A) [Reset = 0x00] |
| 0x3B | INT_LTCH2 | Latched Interrupt Readback Register-3 | 0x00 | INT_LTCH2 Register (Address = 0x3B) [Reset = 0x00] |
| 0x3C | INT_LIVE0 | Live Interrupt Readback Register-0 | 0x00 | INT_LIVE0 Register (Address = 0x3C) [Reset = 0x00] |
| 0x3D | CHx_LIVE | Summary of Diagnostics | 0x00 | CHx_LIVE Register (Address = 0x3D) [Reset = 0x00] |
| 0x40 | OUT_CH1_LIVE | | 0x00 | OUT_CH1_LIVE Register (Address = 0x40) [Reset = 0x00] |
| 0x41 | OUT_CH2_LIVE | | 0x00 | OUT_CH2_LIVE Register (Address = 0x41) [Reset = 0x00] |

表 7-150. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|--------------------|---------------------------------------|-------------|---|
| 0x42 | INT_LIVE1 | Latched Interrupt Readback Register-0 | 0x00 | INT_LIVE1 Register (Address = 0x42) [Reset = 0x00] |
| 0x43 | INT_LIVE2 | Latched Interrupt Readback Register-3 | 0x00 | INT_LIVE2 Register (Address = 0x43) [Reset = 0x00] |
| 0x4E | DIAG_CFG8 | | 0xBA | DIAG_CFG8 Register (Address = 0x4E) [Reset = 0xBA] |
| 0x4F | DIAG_CFG9 | | 0x4B | DIAG_CFG9 Register (Address = 0x4F) [Reset = 0x4B] |
| 0x54 | DIAG_CFG14 | | 0x48 | DIAG_CFG14 Register (Address = 0x54) [Reset = 0x48] |
| 0x55 | DIAGDATA_CFG | | 0x00 | DIAGDATA_CFG Register (Address = 0x55) [Reset = 0x00] |
| 0x58 | DIAG_MON_MSB_MBIAS | | 0x00 | DIAG_MON_MSB_ MBIAS Register (Address = 0x58) [Reset = 0x00] |
| 0x59 | DIAG_MON_LSB_MBIAS | | 0x01 | DIAG_MON_LSB_M BIAS Register (Address = 0x59) [Reset = 0x01] |
| 0x62 | DIAG_MON_MSB_OUT1P | | 0x00 | DIAG_MON_MSB_ OUT1P Register (Address = 0x62) [Reset = 0x00] |
| 0x63 | DIAG_MON_LSB_OUT1P | | 0x06 | DIAG_MON_LSB_O UT1P Register (Address = 0x63) [Reset = 0x06] |
| 0x64 | DIAG_MON_MSB_OUT1M | | 0x00 | DIAG_MON_MSB_ OUT1M Register (Address = 0x64) [Reset = 0x00] |
| 0x65 | DIAG_MON_LSB_OUT1M | | 0x07 | DIAG_MON_LSB_O UT1M Register (Address = 0x65) [Reset = 0x07] |
| 0x66 | DIAG_MON_MSB_OUT2P | | 0x00 | DIAG_MON_MSB_ OUT2P Register (Address = 0x66) [Reset = 0x00] |
| 0x67 | DIAG_MON_LSB_OUT2P | | 0x08 | DIAG_MON_LSB_O UT2P Register (Address = 0x67) [Reset = 0x08] |
| 0x68 | DIAG_MON_MSB_OUT2M | | 0x00 | DIAG_MON_MSB_ OUT2M Register (Address = 0x68) [Reset = 0x00] |

表 7-150. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|-------------------------|---------------|-------------|--|
| 0x69 | DIAG_MON_LSB_OUT2M | | 0x09 | DIAG_MON_LSB_OUT2M Register (Address = 0x69) [Reset = 0x09] |
| 0x6A | DIAG_MON_MSB_TEMP | | 0x00 | DIAG_MON_MSB_TEMP Register (Address = 0x6A) [Reset = 0x00] |
| 0x6B | DIAG_MON_LSB_TEMP | | 0x0A | DIAG_MON_LSB_TEMP Register (Address = 0x6B) [Reset = 0x0A] |
| 0x6C | DIAG_MON_MSB_MBIAS_LOAD | | 0x00 | DIAG_MON_MSB_MBIAS_LOAD Register (Address = 0x6C) [Reset = 0x00] |
| 0x6D | DIAG_MON_LSB_MBIAS_LOAD | | 0x0B | DIAG_MON_LSB_MBIAS_LOAD Register (Address = 0x6D) [Reset = 0x0B] |
| 0x6E | DIAG_MON_MSB_AVDD | | 0x00 | DIAG_MON_MSB_AVDD Register (Address = 0x6E) [Reset = 0x00] |
| 0x6F | DIAG_MON_LSB_AVDD | | 0x0C | DIAG_MON_LSB_AVDD Register (Address = 0x6F) [Reset = 0x0C] |
| 0x70 | DIAG_MON_MSB_GPA | | 0x00 | DIAG_MON_MSB_GPA Register (Address = 0x70) [Reset = 0x00] |
| 0x71 | DIAG_MON_LSB_GPA | | 0x0D | DIAG_MON_LSB_GPA Register (Address = 0x71) [Reset = 0x0D] |

ADVANCE INFORMATION

7.5.2.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in 表 7-151.

Return to the [Summary Table](#).

The device memory map is divided into pages. This register sets the page.

表 7-151. PAGE_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-----------|--|
| 7-0 | PAGE[7:0] | R/W | 00000000b | These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255 |

7.5.2.2 DSP_CFG0 Register (Address = 0x3) [Reset = 0x00]

DSP_CFG0 is shown in 表 7-152.

Return to the [Summary Table](#).

表 7-152. DSP_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | DIS_DVOL_OTF_CHG | R/W | 0b | Disable run-time changes to DVOL settings. 0d = Digital volume control changes supported while ADC is powered-on 1d = Digital volume control changes not supported while ADC is powered-on. |
| 0 | EN_BQ_OTF_CHG | R/W | 0b | Enable run-time changes to Biquad settings. 0d = Disable on the fly biquad changes 1d = Enable on the fly biquad changes |

7.5.2.3 CLK_CFG0 Register (Address = 0xD) [Reset = 0x00]

CLK_CFG0 is shown in 表 7-153.

Return to the [Summary Table](#).

表 7-153. CLK_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7 | CNT_TGT_CFG_OVR_PASI | R/W | 0b | ASI controller target Config Override Register 0d = controller-target Config as per PASI_CNT_CFG bit. 1d = Override the standard behavior of the PASI_CNT_CFG. In this case the clock auto detect feature is not available. PASI_CNT_CFG = 0 : BCLK is input but FSYNC is output. PASI_CNT_CFG = 1 : BCLK is output but FSYNC in input. |
| 6 | CNT_TGT_CFG_OVR_SASI | R/W | 0b | ASI controller target Config Override Register 0d = controller-target Config as per SASI_CNT_CFG bit. 1d = Override the standard behavior of the SASI_CNT_CFG. In this case the clock auto detect feature is not available. SASI_CNT_CFG = 0 : BCLK is input but FSYNC is output. SASI_CNT_CFG = 1 : BCLK is output but FSYNC in input. |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4-3 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 2 | PASI_USE_INT_FSYNC | R/W | 0b | For Primary use internal FSYNC in controller mode configuration. 0d = Use external FSYNC 1d = Use internal FSYNC |
| 1 | SASI_USE_INT_FSYNC | R/W | 0b | For Secondary use internal FSYNC in controller mode configuration. 0d = Use external FSYNC 1d = Use internal FSYNC |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.2.4 CHANNEL_CFG1 Register (Address = 0xE) [Reset = 0x00]

CHANNEL_CFG1 is shown in 表 7-154.

Return to the [Summary Table](#).

表 7-154. CHANNEL_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 7 | FORCE_DYN_MODE_CUST_MAX_CH | R/W | 0b | ADC Force dynamic mode custom max channel 0d = In Dynamic mode, Max channel is based on ADC_DYN_MAXCH_SEL 1d = In Dynamic mode, max channel is custom as DYN_MODE_CUST_MAX_CH |
| 6-3 | DYN_MODE_CUST_MAX_CH[3:0] | R/W | 0000b | ADC Dynamic mode custom max channel configuration [3]->CH4_EN [2]->CH3_EN [1]->CH2_EN [0]->CH1_EN |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset values |

7.5.2.5 CHANNEL_CFG2 Register (Address = 0xF) [Reset = 0x00]

CHANNEL_CFG2 is shown in [表 7-155](#).

Return to the [Summary Table](#).

表 7-155. CHANNEL_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|--|
| 7 | DAC_FORCE_DYN_MODE_CUST_MAX_CH | R/W | 0b | DAC Force dynamic mode custom max channel 0d = In Dynamic, Max channel is based on DAC_DYN_MAXCH_SEL 1d = In Dynamic mode, max channel is custom as per DAC_DYN_MODE_CUST_MAX_CH |
| 6-3 | DAC_DYN_MODE_CUST_MAX_CH[3:0] | R/W | 0000b | DAC Dynamic mode custom max channel configuration ([3]->CH4_EN, [2]->CH3_EN, [1]->CH2_EN, [0]->CH1_EN) [3]->CH4_EN [2]->CH3_EN [1]->CH2_EN [0]->CH1_EN |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset values |

7.5.2.6 SRC_CFG0 Register (Address = 0x17) [Reset = 0x00]

SRC_CFG0 is shown in [表 7-156](#).

Return to the [Summary Table](#).

This register is configuration register 1 for SRC.

表 7-156. SRC_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|---------|---|
| 7 | SRC_EN | R/W | 0b | SRC enable config 0b = SRC disable 1b = SRC enable |
| 6 | DIS_AUTO_SRC_DET | R/W | 0b | SRC auto detect config 0b = SRC auto detect enabled 1b = SRC auto detect disabled |
| 5-0 | RESERVED | R | 000000b | Reserved bits; Write only reset value |

7.5.2.7 SRC_CFG1 Register (Address = 0x18) [Reset = 0x00]

SRC_CFG1 is shown in [表 7-157](#).

Return to the [Summary Table](#).

This register is configuration register 2 for SRC.

表 7-157. SRC_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------------|------|-------|---|
| 7 | MAIN_FS_CUSTOM_CFG | R/W | 0b | Main Fs custom config 0b = Main Fs is auto inferred 1b = Main Fs need to be selected from MAIN_FS_SELECT_CFG |
| 6 | MAIN_FS_SELECT_CFG | R/W | 0b | Main Fs select config 0b = PASI Fs shall be used as Main Fs 1b = SASI Fs shall be used as Main Fs |
| 5-3 | MAIN_AUX_RATIO_M_C USTOM_CFG[2:0] | R/W | 000b | Main and Aux Fs Ratio m:n config 0d = m is auto inferred 1d = 1 2d = 2 3d = 3 4d = 4 5d = Reserved 6d = 6 7d = Reserved |
| 2-0 | MAIN_AUX_RATIO_N_C USTOM_CFG[2:0] | R/W | 000b | Main and Aux Fs Ratio m:n config 0d = n is auto inferred 1d = 1 2d = 2 3d = 3 4d = 4 5d = Reserved 6d = 6 7d = Reserved |

7.5.2.8 JACK_DET_CFG0 Register (Address = 0x19) [Reset = 0x00]

JACK_DET_CFG0 is shown in [表 7-158](#).

Return to the [Summary Table](#).

This register is the JACK DET configuration register 0.

表 7-158. JACK_DET_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|---|
| 7-6 | JACK_DET_MONITOR_F REQ[1:0] | R/W | 00b | Headset Detection Pulse Frequency 0d = 0.5 Hz 1d = 1 Hz 2d = 7.5 Hz 3d = 15 Hz |
| 5 | JACK_DET_PULSE_WID TH | R/W | 0b | Detector Pulse High Width 0d = 4ms (MICBIAS PIN Cap = 1 uF) 1d = 32ms (MICBIAS PIN Cap = 10 uF) |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2-1 | HPDET_CLOCK_SEL[1:0] | R/W | 00b | Headphone Detection Clock Timeperiod Select 0d = 1ms 1d = 2ms 2d = 4ms 3d = Reserved |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.2.9 JACK_DET_CFG1 Register (Address = 0x1A) [Reset = 0x00]

JACK_DET_CFG1 is shown in [表 7-159](#).

Return to the [Summary Table](#).

This register is the JACK DET configuration register 1.

表 7-159. JACK_DET_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|--|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | JACK_DET_COMP_CTRL 2 | R/W | 0b | Hook Press Threshold Control in Fixed External Resistance case, controls the choice of Lowest Microphone impedance to be supported or Highest Hook button Impedance to be supported 0d = Minimum Microphone resistance supported, R_Mic = 800 Ωs and Max Hook button impedance supported, R_Hook = 320 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_hook = 150 Ωs) 1d = Max Hook button impedance supported, R_hook = 680 Ωs and Minimum Microphone resistance supported, R_Mic = 1350 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_Mic = 1750 Ωs) |
| 5-4 | JACK_DET_COMP_CTRL 3[1:0] | R/W | 00b | Hook Pressed Jack Insertion support, valid only for External Resistor Type P0_R25_D4 = 0 else Don't care. 0d = supports minimum Hook button impedance of 150 Ωs for Hook Pressed Jack Insertion detection 1d = supports minimum Hook button impedance of 100 Ωs for Hook Pressed Jack Insertion detection 2d = supports minimum Hook button impedance of 50 Ωs for Hook Pressed Jack Insertion detection 3d = Reserved |
| 3 | HPDET_COUPLING | R/W | 0b | Headphone detect coupling 0d = AC coupled 1d = DC coupled |
| 2 | HPDET_USE_2x_CURR | R/W | 0b | Headset detect current sel config 0d = 2x current for headphone detection disabled 1d = 2x current for headphone detection enabled |
| 1 | JACK_DET_EN | R/W | 0b | Headset Detection Enable 0d = Headset Detection Disabled 1d = Headset Detection Enabled |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.10 JACK_DET_CFG2 Register (Address = 0x1B) [Reset = 0x00]

JACK_DET_CFG2 is shown in [表 7-160](#).

Return to the [Summary Table](#).

This register is the JACK DET configuration register 2.

表 7-160. JACK_DET_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | HPDET_DEB | R/W | 0b | Headphone Detection Debounce Programmability 0d = No Debounce 1d = Debounce of 3 detections |

表 7-160. JACK_DET_CFG2 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|--|
| 5-3 | JACK_DET_DEB_INSERT[2:0] | R/W | 000b | Headset Insert Detection Debounce Programmability 0d = Debounce Time = 16ms 1d = Debounce Time = 32ms 2d = Debounce Time = 64ms 3d = Debounce Time = 128ms 4d = Debounce Time = 256ms 5d = Debounce Time = 512ms 6d = Reserved. Don not use 7d = No Debounce |
| 2 | JACK_DET_DEB_REMOVE | R/W | 0b | Headset Removal Detection Debounce Programmability 0d = Debounce of 5 detections 1d = Debounce of 3 detections |
| 1-0 | JACK_DET_DEB_HOOK_PRESS[1:0] | R/W | 00b | Hook Press Debounce config 0d = No Debounce 1d = No Debounce 2d = Debounce of 2 detections 3d = Debounce of 3 detections |

7.5.2.11 JACK_DET_CFG3 Register (Address = 0x1C) [Reset = 0x00]

JACK_DET_CFG3 is shown in 表 7-161.

Return to the [Summary Table](#).

This register is the JACK DET configuration register 3.

表 7-161. JACK_DET_CFG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 7-6 | JACK_TYPE_FLAG[1:0] | R | 00b | Headset Jack type flag 0d = Jack is not inserted 1d = Jack is inserted without Microphone 2d = Reserved. Do not use 3d = Jack is inserted with Microphone |
| 5-4 | HEADSET_TYPE_DET[1:0] | R | 00b | Headset type 0d = Headset is not inserted 1d = Jack is inserted with mono-HS (RIGHT) 2d = Jack is inserted with mono-HS (LEFT) 3d = Jack is inserted with stereo-HS |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.2.12 LPAD_CFG1 Register (Address = 0x1E) [Reset = 0x20]

LPAD_CFG1 is shown in 表 7-162.

Return to the [Summary Table](#).

Low Power Activity Detection. Voice activity detection or Ultrasonic Activity detection configuration register 1

表 7-162. LPAD_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7-6 | LPAD_MODE[1:0] | R/W | 00b | Auto ADC power up / power down configuration selection. 0d = User initiated ADC power-up and ADC power-down 1d = VAD/UAD interrupt based ADC power up and ADC power down 2d = VAD/UAD interrupt based ADC power up but user initiated ADC power down Dont use |

表 7-162. LPAD_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 5-4 | LPAD_CH_SEL[1:0] | R/W | 10b | VAD channel select. 0d = Channel 1 is monitored for VAD/UAD activity 1d = Channel 2 is monitored for VAD/UAD activity 2d = Channel 3 is monitored for VAD/UAD activity 3d = Channel 4 is monitored for VAD/UAD activity |
| 3 | LPAD_SDOOUT_INT_CFG | R/W | 0b | SDOUT interrupt configuration. 0d = SDOUT pin is not enabled for interrupt function 1d = SDOUT pin is enabled to support interrupt output when channel data in not being recorded |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | LPAD_PD_DET_EN | R/W | 0b | Enable ASI output data during VAD/UAD activity. 0d = VAD/UAD processing is not enabled during ADC recording 1d = VAD/UAD processing is enabled during ADC recording and VAD interrupts are generated as configured |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.2.13 LPSG_CFG1 Register (Address = 0x1F) [Reset = 0x80]

LPSG_CFG1 is shown in 表 7-163.

Return to the [Summary Table](#).

Low Power Signal Generation configuration register 1

表 7-163. LPSG_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|--------|---|
| 7-6 | LPSG_CH_SEL[1:0] | R/W | 10b | LPSG channel select.- UAG 0d = UAG activity is generated on channel 1 1d = UAG activity is generated on channel 2 2d = UAG activity is generated on channel 3 3d = UAG activity is generated on channel 4 |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4-0 | RESERVED | R | 00000b | Reserved bits; Write only reset values |

7.5.2.14 LPAD_LPSG_CFG1 Register (Address = 0x20) [Reset = 0x00]

LPAD_LPSG_CFG1 is shown in 表 7-164.

Return to the [Summary Table](#).

This register is configuration register 1 for VAD/UAD/UAG.

表 7-164. LPAD_LPSG_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 7-6 | LPAD_LPSG_CLK_CFG[1:0] | R/W | 00b | Clock select for VAD/UAD/UAG 0d = VAD/UAD/UAG processing using internal oscillator clock 1d = VAD/UAD/UAG processing using external clock on BCLK input 2d = VAD/UAD/UAG processing using external clock on CCLK input 3d = Custom clock configuration based on CNT_CFG, CLK_SRC and CLKGEN_CFG registers in page 0 |
| 5-4 | LPAD_LPSG_EXT_CLK_CFG[1:0] | R/W | 00b | Clock configuration using external clock for VAD/UAD/UAG 0d = External clock is 24.576 MHz 1d = External clock is 6.144 MHz 2d = External clock is 12.288 MHz 3d = External clock is 18.432 MHz |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

表 7-164. LPAD_LPSG_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 2 | LPAD_PH1_EN | R/W | 0b | Enable LPAD Phase 1 detection through Jack Detection comparator. 0d = LPAD phase 1 disabled 1d = LPAD phase 1 enabled |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

7.5.2.15 LIMITER_CFG Register (Address = 0x23) [Reset = 0x00]

LIMITER_CFG is shown in 表 7-165.

Return to the [Summary Table](#).

This register is configuration register 2 for Limiter.

表 7-165. LIMITER_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7-6 | LIMITER_INP_SEL[1:0] | R/W | 00b | Limiter input select config 0d = max(dacin_ch0, dacin_ch1) 1d = dacin_ch1 2d = dacin_ch0 3d = avg(dacin_ch0, dacin_ch1) |
| 5-4 | LIMITER_OUT_SEL[1:0] | R/W | 00b | Limiter output select config 0d = applied on both 1d = dacin_ch1 2d = dacin_ch0 3d = applied none |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset values |

7.5.2.16 AGC_DRC_CFG Register (Address = 0x24) [Reset = 0x00]

AGC_DRC_CFG is shown in 表 7-166.

Return to the [Summary Table](#).

This register is configuration register 2 for AGC_DRC.

表 7-166. AGC_DRC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|--|
| 7 | AGC_CH1_EN | R/W | 0b | AGC Channel 1 enable config 0d = disable 1d = enable |
| 6 | AGC_CH2_EN | R/W | 0b | AGC Channel 2 enable config 0d = disable 1d = enable |
| 5 | AGC_CH3_EN | R/W | 0b | AGC Channel 3 enable config 0d = disable 1d = enable |
| 4 | AGC_CH4_EN | R/W | 0b | AGC Channel 4 enable config 0d = disable 1d = enable |
| 3 | DRC_CH1_EN | R/W | 0b | DRC Channel 1 enable config 0d = disable 1d = enable |
| 2 | DRC_CH2_EN | R/W | 0b | DRC Channel 2 enable config 0d = disable 1d = enable |

表 7-166. AGC_DRC_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|--|
| 1 | DRC_CH3_EN | R/W | 0b | DRC Channel 3 enable config 0d = disable 1d = enable |
| 0 | DRC_CH4_EN | R/W | 0b | DRC Channel 4 enable config 0d = disable 1d = enable |

7.5.2.17 PLIM_CFG0 Register (Address = 0x2B) [Reset = 0x00]

PLIM_CFG0 is shown in 表 7-167.

Return to the [Summary Table](#).

This register is configuration register 0 for PLIM.

表 7-167. PLIM_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7 | EN_PLIM | R/W | 0b | Enable PLIM 0d = Disable 1d = Enable |
| 6-4 | PLIM_ATTEN_VAL[2:0] | R/W | 000b | PLIM attenuation factor 0d = 0dB 1d = -6dB 2d = -12dB 3d = -18dB 4d = -24dB 5d = -30dB 6d = -36dB 7d = -42dB |
| 3 | PLIM_BY_SAR_GPA | R/W | 0b | PLIM attenuation value source 0d = Plimit attenuation based on GPIO and reg_plimi_attn_val 1d = Plimit attenuation based on GPA Analog voltage. LUT will map SAR ADC data to Attenuation factor |
| 2 | PLIM_RECOVERY | R/W | 0b | PLIM attenuation recovery 0d = Plimit func doesn't recover. It stays at same attenuation level or can apply more attenuation if required 1d = Plimit func recovers (reduces the attenuation) if "gpio_val=0" or "sar_adc_gpa" data suggest that Battery Voltage has recovered then we can reduce the attenuation being applied |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.2.18 MIXER_CFG0 Register (Address = 0x2C) [Reset = 0x00]

MIXER_CFG0 is shown in 表 7-168.

Return to the [Summary Table](#).

This register is the MISC configuration register 0.

表 7-168. MIXER_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7 | EN_DAC_ASI_MIXER | R/W | 0b | Enable DAC ASI Mixer 0b = Disabled 1b = Enabled |
| 6 | EN_SIDE_CHAIN_MIXER | R/W | 0b | Enable Side Chain Mixer 0b = Disabled 1b = Enabled |

表 7-168. MIXER_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 5 | EN_ADC_CHANNEL_MIXER | R/W | 0b | Enable ADC Channel Mixer 0b = Disabled 1b = Enabled |
| 4 | EN_LOOPBACK_MIXER | R/W | 0b | Enable Loopback Mixer 0b = Disabled 1b = Enabled |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.2.19 MISC_CFG0 Register (Address = 0x2D) [Reset = 0x00]

MISC_CFG0 is shown in [表 7-169](#).

Return to the [Summary Table](#).

This register is the MISC configuration register 0.

表 7-169. MISC_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|------|-------|--|
| 7 | EN_DISTORTION | R/W | 0b | Distortion Limiter enable config 0b = Distortion Limiter disable 1b = Distortion Limiter enable |
| 6 | EN_BOP | R/W | 0b | BOP enable config 0b = BOP disable 1b = BOP enable |
| 5 | EN_THERMAL_FOLDBACK | R/W | 0b | Thermal Foldback enable config 0b = Thermal Foldback disable 1b = Thermal Foldback enable |
| 4 | EN_DRC | R/W | 0b | DRC enable config 0b = DRC disable 1b = DRC enable |
| 3 | DAC_SIGNAL_GENERATOR_1_ENABLE | R/W | 0b | DAC signal generator 1 enable config 0b = Signal generator disabled 1b = Signal generator enabled |
| 2 | DAC_SIGNAL_GENERATOR_2_ENABLE | R/W | 0b | DAC signal generator 2 enable config 0b = Signal generator disabled 1b = Signal generator enabled |
| 1 | DSP_VBAT_AVDD_SEL | R/W | 0b | SAR data source select for DSP Limiter, BOP, DRC 0b = SAR VBAT data to DSP 1b = SAR AVDD data to DSP |
| 0 | BRWNOUT_EN | R/W | 0b | Brownout enable config 0b = Brownout disable 1b = Brownout enable |

7.5.2.20 BRWNOUT Register (Address = 0x2E) [Reset = 0xBF]

BRWNOUT is shown in [表 7-170](#).

Return to the [Summary Table](#).

表 7-170. BRWNOUT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|---|
| 7-0 | BRWNOUT_THRS[7:0] | R/W | 10111111b | Threshold for brownout shutdown (IF P1_R45_D1->DSP_VBAT_AVDD_SEL=1) Default = 7.8V (~2.7V) Nd = ((0.9×(N*16)/4095)-0.211764)×17 (V) (((0.9×(N*16)/4095)-0.225)×6 (V)) |

7.5.2.21 INT_MASK0 Register (Address = 0x2F) [Reset = 0xFF]

INT_MASK0 is shown in 表 7-171.

Return to the [Summary Table](#).

Interrupt masks.

表 7-171. INT_MASK0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | INT_MASK0 | R/W | 1b | Clock error interrupt mask. 0b = Don't Mask 1b = Mask |
| 6 | INT_MASK0 | R/W | 1b | PLL Lock interrupt mask. 0b = Don't Mask 1b = Mask |
| 5 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |

7.5.2.22 INT_MASK4 Register (Address = 0x32) [Reset = 0x00]

INT_MASK4 is shown in 表 7-172.

Return to the [Summary Table](#).

Interrupt masks.

表 7-172. INT_MASK4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | INT_MASK4 | R/W | 0b | OUT Short Circuit Fault Interrupt Mask. 0b = Don't Mask 1b = Mask |
| 4 | INT_MASK4 | R/W | 0b | DRVR Virtual Ground Fault Interrupt Mask. 0b = Don't Mask 1b = Mask |
| 3 | INT_MASK4 | R/W | 0b | Headset insert detection interrupt mask. 0b = Don't Mask 1b = Mask |
| 2 | INT_MASK4 | R/W | 0b | Headset remove detection interrupt mask. 0b = Don't Mask 1b = Mask |

表 7-172. INT_MASK4 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 1 | INT_MASK4 | R/W | 0b | Headset detection hook(button) interrupt mask. 0b = Don't Mask 1b = Mask |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.2.23 INT_MASK5 Register (Address = 0x33) [Reset = 0x30]

INT_MASK5 is shown in [表 7-173](#).

Return to the [Summary Table](#).

Interrupt masks.

表 7-173. INT_MASK5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | INT_MASK5 | R/W | 0b | GPA up threshold fault mask. 0b = Don't Mask 1b = Mask |
| 6 | INT_MASK5 | R/W | 0b | GPA low threshold fault mask. 0b = Don't Mask 1b = Mask |
| 5 | INT_MASK5 | R/W | 1b | VAD power up detect interrupt mask. 0b = Don't Mask 1b = Mask |
| 4 | INT_MASK5 | R/W | 1b | VAD power down detect interrupt mask. 0b = Don't Mask 1b = Mask |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.2.24 INT_LTCH0 Register (Address = 0x34) [Reset = 0x00]

INT_LTCH0 is shown in [表 7-174](#).

Return to the [Summary Table](#).

Latched interrupt readback.

表 7-174. INT_LTCH0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | INT_LTCH0 | R | 0b | Interrupt due to clock error (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 6 | INT_LTCH0 | R | 0b | Interrupt due to PLL Lock (self clearing bit) 0b = No interrupt 1b = Interrupt |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |

表 7-174. INT_LTCH0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--------------------------------------|
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.25 CHx_LTCH Register (Address = 0x35) [Reset = 0x00]

CHx_LTCH is shown in 表 7-175.

Return to the [Summary Table](#).

Channel level Diagnostics Latched Status

表 7-175. CHx_LTCH Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | STS_CHx_LTCH | R | 0b | Status of Input CH1_LTCH. 0b = No faults occurred in input channel 1 1b = Fault or Faults have occurred in input channel 1 |
| 6 | STS_CHx_LTCH | R | 0b | Status of Input CH2_LTCH. 0b = No faults occurred in input channel 2 1b = Fault or Faults have occurred in input channel 2 |
| 5 | STS_CHx_LTCH | R | 0b | Status of Output CH1_LTCH. 0b = No faults occurred in output channel 1 1b = Fault or Faults have occurred in output channel 1 |
| 4 | STS_CHx_LTCH | R | 0b | Status of Output CH2_LTCH. 0b = No faults occurred in output channel 2 1b = Fault or Faults have occurred in output channel 2 |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.26 OUT_CH1_LTCH Register (Address = 0x38) [Reset = 0x00]

OUT_CH1_LTCH is shown in 表 7-176.

Return to the [Summary Table](#).

表 7-176. OUT_CH1_LTCH Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7 | OUT_CH1_LTCH | R | 0b | OUT1P Short Circuit Fault (self clearing bit). 0b = No short circuit fault 1b = Short circuit fault |
| 6 | OUT_CH1_LTCH | R | 0b | OUT1M Short Circuit Fault (self clearing bit). 0b = No short circuit fault 1b = Short circuit fault |
| 5 | OUT_CH1_LTCH | R | 0b | Channel 1 DRVRP Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault |
| 4 | OUT_CH1_LTCH | R | 0b | Channel 1 DRVRM Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault |
| 3 | MASK_ADC_CH1_OVRLD_FLAG | R/W | 0b | ADC CH1 OVRLD fault mask. 0b = Don't Mask 1b = Mask |
| 2 | MASK_ADC_CH2_OVRLD_FLAG | R/W | 0b | ADC CH2 OVRLD fault mask. 0b = Don't Mask 1b = Mask |

表 7-176. OUT_CH1_LTCH Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---------------------------------------|
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

7.5.2.27 OUT_CH2_LTCH Register (Address = 0x39) [Reset = 0x00]

OUT_CH2_LTCH is shown in [表 7-177](#).

Return to the [Summary Table](#).

表 7-177. OUT_CH2_LTCH Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7 | OUT_CH2_LTCH | R | 0b | OUT2P Short Circuit Fault (self clearing bit). 0b = No short circuit fault 1b = Short circuit fault |
| 6 | OUT_CH2_LTCH | R | 0b | OUT2M Short Circuit Fault (self clearing bit). 0b = No short circuit fault 1b = Short circuit fault |
| 5 | OUT_CH2_LTCH | R | 0b | Channel 2 DRVRP Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault |
| 4 | OUT_CH2_LTCH | R | 0b | Channel 2 DRVRM Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault |
| 3-2 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 1 | MASK_AREG_SC_FLAG | R/W | 0b | AREG SC fault mask. 0b = Don't Mask 1b = Mask |
| 0 | AREG_SC_FLAG_LTCH | R | 0b | AREG SC fault (self clearing bit). 0b = No AREG short circuit fault 1b = AREG short circuit fault |

7.5.2.28 INT_LTCH1 Register (Address = 0x3A) [Reset = 0x00]

INT_LTCH1 is shown in [表 7-178](#).

Return to the [Summary Table](#).

Latched interrupt readback.

表 7-178. INT_LTCH1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | INT_LTCH1 | R | 0b | Interrupt due to Headset Insert Detection (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 2 | INT_LTCH1 | R | 0b | Interrupt due to Headset Remove Detection (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 1 | INT_LTCH1 | R | 0b | Interrupt due to Headset hook(button) (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.29 INT_LTCH2 Register (Address = 0x3B) [Reset = 0x00]

INT_LTCH2 is shown in [表 7-179](#).

Return to the [Summary Table](#).

Latched interrupt readback.

表 7-179. INT_LTCH2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | INT_LTCH2 | R | 0b | Interrupt due to GPA up threshold fault (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 6 | INT_LTCH2 | R | 0b | Interrupt due to GPA low threshold fault (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 5 | INT_LTCH2 | R | 0b | Interrupt due to VAD power up detect (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 4 | INT_LTCH2 | R | 0b | Interrupt due to VAD power down detect (self clearing bit). 0b = No interrupt 1b = Interrupt |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.30 INT_LIVE0 Register (Address = 0x3C) [Reset = 0x00]

INT_LIVE0 is shown in [表 7-180](#).

Return to the [Summary Table](#).

Latched interrupt readback.

表 7-180. INT_LIVE0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | INT_LIVE0 | R | 0b | Interrupt due to clock error . 0b = No interrupt 1b = Interrupt |
| 6 | INT_LIVE0 | R | 0b | Interrupt due to PLL Lock 0b = No interrupt 1b = Interrupt |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.31 CHx_LIVE Register (Address = 0x3D) [Reset = 0x00]

CHx_LIVE is shown in [表 7-181](#).

Return to the [Summary Table](#).

Channel level Diagnostics Live Status

表 7-181. CHx_LIVE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | STS_CHx_LIVE | R | 0b | Status of Input CH1_LIVE. 0b = No faults occurred in input channel 1 1b = Fault or Faults have occurred in input channel 1 |
| 6 | STS_CHx_LIVE | R | 0b | Status of Input CH2_LIVE. 0b = No faults occurred in input channel 2 1b = Fault or Faults have occurred in input channel 2 |
| 5 | STS_CHx_LIVE | R | 0b | Status of Output CH1_LIVE. 0b = No faults occurred in output channel 1 1b = Fault or Faults have occurred in output channel 1 |
| 4 | STS_CHx_LIVE | R | 0b | Status of Output CH2_LIVE. 0b = No faults occurred in output channel 2 1b = Fault or Faults have occurred in output channel 2 |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.32 OUT_CH1_LIVE Register (Address = 0x40) [Reset = 0x00]

OUT_CH1_LIVE is shown in 表 7-182.

Return to the [Summary Table](#).

表 7-182. OUT_CH1_LIVE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | OUT_CH1_LIVE | R | 0b | OUT1P Short Circuit Fault . 0b = No short circuit fault 1b = Short circuit fault |
| 6 | OUT_CH1_LIVE | R | 0b | OUT1M Short Circuit Fault . 0b = No short circuit fault 1b = Short circuit fault |
| 5 | OUT_CH1_LIVE | R | 0b | Channel 1 DRVRP Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault |
| 4 | OUT_CH1_LIVE | R | 0b | Channel 1 DRVRM Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.2.33 OUT_CH2_LIVE Register (Address = 0x41) [Reset = 0x00]

OUT_CH2_LIVE is shown in 表 7-183.

Return to the [Summary Table](#).

表 7-183. OUT_CH2_LIVE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | OUT_CH2_LIVE | R | 0b | OUT2P Short Circuit Fault . 0b = No short circuit fault 1b = Short circuit fault |
| 6 | OUT_CH2_LIVE | R | 0b | OUT2M Short Circuit Fault . 0b = No short circuit fault 1b = Short circuit fault |

表 7-183. OUT_CH2_LIVE Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 5 | OUT_CH2_LIVE | R | 0b | Channel 2 DRVRP Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault |
| 4 | OUT_CH2_LIVE | R | 0b | Channel 2 DRVRM Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault |
| 3-1 | RESERVED | R | 000b | Reserved bits; Write only reset value |
| 0 | AREG_SC_FLAG_LIVE | R | 0b | AREG SC fault . 0b = No AREG short circuit fault 1b = AREG short circuit fault |

7.5.2.34 INT_LIVE1 Register (Address = 0x42) [Reset = 0x00]

INT_LIVE1 is shown in 表 7-184.

Return to the [Summary Table](#).

Live interrupt readback.

表 7-184. INT_LIVE1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | INT_LIVE1 | R | 0b | Interrupt due to Headset Insert Detection . 0b = No interrupt 1b = Interrupt |
| 2 | INT_LIVE1 | R | 0b | Interrupt due to Headset Remove Detection . 0b = No interrupt 1b = Interrupt |
| 2 | INT_LIVE1 | R | 0b | Interrupt due to Headset hook(button) . 0b = No interrupt 1b = Interrupt |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | |

7.5.2.35 INT_LIVE2 Register (Address = 0x43) [Reset = 0x00]

INT_LIVE2 is shown in 表 7-185.

Return to the [Summary Table](#).

Live interrupt readback.

表 7-185. INT_LIVE2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7 | INT_LIVE2 | R | 0b | Interrupt due to GPA up threshold fault . 0b = No interrupt 1b = Interrupt |
| 6 | INT_LIVE2 | R | 0b | Interrupt due to GPA low threshold fault 0b = No interrupt 1b = Interrupt |

表 7-185. INT_LIVE2 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 5 | INT_LIVE2 | R | 0b | Interrupt due to VAD power up detect . 0b = No interrupt 1b = Interrupt |
| 4 | INT_LIVE2 | R | 0b | Interrupt due to VAD power down detect . 0b = No interrupt 1b = Interrupt |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.2.36 DIAG_CFG8 Register (Address = 0x4E) [Reset = 0xBA]

DIAG_CFG8 is shown in 表 7-186.

Return to the [Summary Table](#).

表 7-186. DIAG_CFG8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-----------|--|
| 7-0 | GPA_UP_THRS_FLT_TH RES[7:0] | R/W | 10111010b | General Purpose Analog High Threshold Default = ~ 2.6V $nd = ((0.9 \times (N \times 16) / 4095) - 0.225) \times 6 \text{ (V)}$ |

7.5.2.37 DIAG_CFG9 Register (Address = 0x4F) [Reset = 0x4B]

DIAG_CFG9 is shown in 表 7-187.

Return to the [Summary Table](#).

表 7-187. DIAG_CFG9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-----------|---|
| 7-0 | GPA_LOW_THRS_FLT_T HRES[7:0] | R/W | 01001011b | General Purpose Analog Low Threshold Default = ~ 0.2V $nd = ((0.9 \times (N \times 16) / 4095) - 0.225) \times 6 \text{ (V)}$ |

7.5.2.38 DIAG_CFG14 Register (Address = 0x54) [Reset = 0x48]

DIAG_CFG14 is shown in 表 7-188.

Return to the [Summary Table](#).

表 7-188. DIAG_CFG14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | AVDD_FILT_SEL[1:0] | R/W | 10b | AVDD filter select 0d = 3.5MHz 1d = 200kHz 2d = 100kHz 3d = No filter |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

表 7-188. DIAG_CFG14 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 3-2 | VBAT_FILT_SEL[1:0] | R/W | 10b | VBAT filter select 0d = 3.5MHz 1d = 200kHz 2d = 100kHz 3d = No filter |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

7.5.2.39 DIAGDATA_CFG Register (Address = 0x55) [Reset = 0x00]

DIAGDATA_CFG is shown in 表 7-189.

Return to the [Summary Table](#).

表 7-189. DIAGDATA_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|---|
| 7-4 | RESERVED | R/W | 0000b | Reserved bits; Write only reset values |
| 3 | IADC_DATA_IN_DIAG_REGS | R/W | 0b | IADC channel data in diagnostics channel data registers 0b= Disabled 1b= Enabled |
| 2 | HOLD_IADC_DATA | R/W | 0b | Hold IADC data update during register readback 0b= Data update is not held, Data register is continuously updated 1b= Data update is held, Data register readback can be done |
| 1 | OVRD_VBAT_TEMP_DATA | R/W | 0b | Override VBAT and TEMP data 0b= Override Disabled 1b= Override Enabled |
| 0 | HOLD_SAR_DATA | R/W | 0b | Hold SAR data update during register readback 0b= Data update is not held, Data register is continuously updated 1b= Data update is held, Data register readback can be done |

7.5.2.40 DIAG_MON_MSB_MBIAS Register (Address = 0x58) [Reset = 0x00]

DIAG_MON_MSB_MBIAS is shown in 表 7-190.

Return to the [Summary Table](#).

表 7-190. DIAG_MON_MSB_MBIAS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-----------|--|
| 7-0 | DIAG_MON_MSB_MBIAS[7:0] | R | 00000000b | D diagnostic SAR Monitor Data MSB Byte |

7.5.2.41 DIAG_MON_LSB_MBIAS Register (Address = 0x59) [Reset = 0x01]

DIAG_MON_LSB_MBIAS is shown in 表 7-191.

Return to the [Summary Table](#).

表 7-191. DIAG_MON_LSB_MBIAS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_MBIAS[3:0] | R | 0000b | D diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 0001b | Channel ID |

7.5.2.42 DIAG_MON_MSB_OUT1P Register (Address = 0x62) [Reset = 0x00]

DIAG_MON_MSB_OUT1P is shown in [表 7-192](#).

Return to the [Summary Table](#).

表 7-192. DIAG_MON_MSB_OUT1P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_OUT_CH1P[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.43 DIAG_MON_LSB_OUT1P Register (Address = 0x63) [Reset = 0x06]

DIAG_MON_LSB_OUT1P is shown in [表 7-193](#).

Return to the [Summary Table](#).

表 7-193. DIAG_MON_LSB_OUT1P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_OUT_C_H1P[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 0110b | Channel ID |

7.5.2.44 DIAG_MON_MSB_OUT1M Register (Address = 0x64) [Reset = 0x00]

DIAG_MON_MSB_OUT1M is shown in [表 7-194](#).

Return to the [Summary Table](#).

表 7-194. DIAG_MON_MSB_OUT1M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_OUT_CH1N[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.45 DIAG_MON_LSB_OUT1M Register (Address = 0x65) [Reset = 0x07]

DIAG_MON_LSB_OUT1M is shown in [表 7-195](#).

Return to the [Summary Table](#).

表 7-195. DIAG_MON_LSB_OUT1M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_OUT_C_H1N[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 0111b | Channel ID |

7.5.2.46 DIAG_MON_MSB_OUT2P Register (Address = 0x66) [Reset = 0x00]

DIAG_MON_MSB_OUT2P is shown in [表 7-196](#).

Return to the [Summary Table](#).

表 7-196. DIAG_MON_MSB_OUT2P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_OUT_CH2P[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.47 DIAG_MON_LSB_OUT2P Register (Address = 0x67) [Reset = 0x08]

 DIAG_MON_LSB_OUT2P is shown in [表 7-197](#).

 Return to the [Summary Table](#).

表 7-197. DIAG_MON_LSB_OUT2P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_OUT_C H2P[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1000b | Channel ID |

7.5.2.48 DIAG_MON_MSB_OUT2M Register (Address = 0x68) [Reset = 0x00]

 DIAG_MON_MSB_OUT2M is shown in [表 7-198](#).

 Return to the [Summary Table](#).

表 7-198. DIAG_MON_MSB_OUT2M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_OUT_ CH2N[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.49 DIAG_MON_LSB_OUT2M Register (Address = 0x69) [Reset = 0x09]

 DIAG_MON_LSB_OUT2M is shown in [表 7-199](#).

 Return to the [Summary Table](#).

表 7-199. DIAG_MON_LSB_OUT2M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_OUT_C H2N[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1001b | Channel ID |

7.5.2.50 DIAG_MON_MSB_TEMP Register (Address = 0x6A) [Reset = 0x00]

 DIAG_MON_MSB_TEMP is shown in [表 7-200](#).

 Return to the [Summary Table](#).

表 7-200. DIAG_MON_MSB_TEMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_TEMP[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.51 DIAG_MON_LSB_TEMP Register (Address = 0x6B) [Reset = 0x0A]

 DIAG_MON_LSB_TEMP is shown in [表 7-201](#).

 Return to the [Summary Table](#).

表 7-201. DIAG_MON_LSB_TEMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_TEMP[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |

表 7-201. DIAG_MON_LSB_TEMP Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-------------|
| 3-0 | Channel[3:0] | R | 1010b | Channel ID |

7.5.2.52 DIAG_MON_MSB_MBIAS_LOAD Register (Address = 0x6C) [Reset = 0x00]

DIAG_MON_MSB_MBIAS_LOAD is shown in [表 7-202](#).

Return to the [Summary Table](#).

表 7-202. DIAG_MON_MSB_MBIAS_LOAD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_MBIAS_LOAD[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.53 DIAG_MON_LSB_MBIAS_LOAD Register (Address = 0x6D) [Reset = 0x0B]

DIAG_MON_LSB_MBIAS_LOAD is shown in [表 7-203](#).

Return to the [Summary Table](#).

表 7-203. DIAG_MON_LSB_MBIAS_LOAD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_MBIAS_LOAD[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1011b | Channel ID |

7.5.2.54 DIAG_MON_MSB_AVDD Register (Address = 0x6E) [Reset = 0x00]

DIAG_MON_MSB_AVDD is shown in [表 7-204](#).

Return to the [Summary Table](#).

表 7-204. DIAG_MON_MSB_AVDD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_AVDD[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.55 DIAG_MON_LSB_AVDD Register (Address = 0x6F) [Reset = 0x0C]

DIAG_MON_LSB_AVDD is shown in [表 7-205](#).

Return to the [Summary Table](#).

表 7-205. DIAG_MON_LSB_AVDD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_AVDD[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1100b | Channel ID |

7.5.2.56 DIAG_MON_MSB_GPA Register (Address = 0x70) [Reset = 0x00]

DIAG_MON_MSB_GPA is shown in [表 7-206](#).

Return to the [Summary Table](#).

表 7-206. DIAG_MON_MSB_GPA Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-----------|--------------------------------------|
| 7-0 | DIAG_MON_MSB_GPA[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

7.5.2.57 DIAG_MON_LSB_GPA Register (Address = 0x71) [Reset = 0x0D]

DIAG_MON_LSB_GPA is shown in [表 7-207](#).

Return to the [Summary Table](#).

表 7-207. DIAG_MON_LSB_GPA Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7-4 | DIAG_MON_LSB_GPA[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1101b | Channel ID |

7.5.3 TAC5212 Registers

表 7-208 lists the memory-mapped registers for the TAC5212 registers. All register offset addresses not listed in 表 7-208 should be considered as reserved locations and the register contents should not be modified.

表 7-208. TAC5212 Registers

| Address | Acronym | Register Name | Reset Value | Section |
|---------|-----------------|--|-------------|--|
| 0x0 | PAGE_CFG | Device page register | 0x00 | PAGE_CFG Register (Address = 0x0) [Reset = 0x00] |
| 0x1A | SASI_CFG0 | Secondary ASI configuration register 0 | 0x30 | SASI_CFG0 Register (Address = 0x1A) [Reset = 0x30] |
| 0x1B | SASI_TX_CFG0 | SASI TX configuration register 0 | 0x00 | SASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00] |
| 0x1C | SASI_TX_CFG1 | SASI TX configuration register 1 | 0x00 | SASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00] |
| 0x1D | SASI_TX_CFG2 | SASI TX configuration register 2 | 0x00 | SASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00] |
| 0x1E | SASI_TX_CH1_CFG | SASI TX Channel 1 configuration register | 0x00 | SASI_TX_CH1_CFG Register (Address = 0x1E) [Reset = 0x00] |
| 0x1F | SASI_TX_CH2_CFG | SASI TX Channel 2 configuration register | 0x01 | SASI_TX_CH2_CFG Register (Address = 0x1F) [Reset = 0x01] |
| 0x20 | SASI_TX_CH3_CFG | SASI TX Channel 3 configuration register | 0x02 | SASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02] |
| 0x21 | SASI_TX_CH4_CFG | SASI TX Channel 4 configuration register | 0x03 | SASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03] |
| 0x22 | SASI_TX_CH5_CFG | SASI TX Channel 5 configuration register | 0x04 | SASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04] |
| 0x23 | SASI_TX_CH6_CFG | SASI TX Channel 6 configuration register | 0x05 | SASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05] |
| 0x24 | SASI_TX_CH7_CFG | SASI TX Channel 7 configuration register | 0x06 | SASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06] |
| 0x25 | SASI_TX_CH8_CFG | SASI TX Channel 8 configuration register | 0x07 | SASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07] |
| 0x26 | SASI_RX_CFG0 | SASI RX configuration register 0 | 0x00 | SASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00] |

表 7-208. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|-----------------|--|-------------|--|
| 0x27 | SASI_RX_CFG1 | SASI RX configuration register 1 | 0x00 | SASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00] |
| 0x28 | SASI_RX_CH1_CFG | SASI RX Channel 1 configuration register | 0x00 | SASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x00] |
| 0x29 | SASI_RX_CH2_CFG | SASI RX Channel 2 configuration register | 0x01 | SASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x01] |
| 0x2A | SASI_RX_CH3_CFG | SASI RX Channel 3 configuration register | 0x02 | SASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02] |
| 0x2B | SASI_RX_CH4_CFG | SASI RX Channel 4 configuration register | 0x03 | SASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03] |
| 0x2C | SASI_RX_CH5_CFG | SASI RX Channel 5 configuration register | 0x04 | SASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04] |
| 0x2D | SASI_RX_CH6_CFG | SASI RX Channel 6 configuration register | 0x05 | SASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05] |
| 0x2E | SASI_RX_CH7_CFG | SASI RX Channel 7 configuration register | 0x06 | SASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06] |
| 0x2F | SASI_RX_CH8_CFG | SASI RX Channel 8 configuration register | 0x07 | SASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07] |
| 0x32 | CLK_CFG12 | Clock configuration register 12 | 0x00 | CLK_CFG12 Register (Address = 0x32) [Reset = 0x00] |
| 0x33 | CLK_CFG13 | | 0x00 | CLK_CFG13 Register (Address = 0x33) [Reset = 0x00] |
| 0x34 | CLK_CFG14 | Clock configuration register 14 | 0x10 | CLK_CFG14 Register (Address = 0x34) [Reset = 0x10] |
| 0x35 | CLK_CFG15 | Clock configuration register 15 | 0x01 | CLK_CFG15 Register (Address = 0x35) [Reset = 0x01] |
| 0x36 | CLK_CFG16 | Clock configuration register 16 | 0x00 | CLK_CFG16 Register (Address = 0x36) [Reset = 0x00] |
| 0x37 | CLK_CFG17 | Clock configuration register 17 | 0x00 | CLK_CFG17 Register (Address = 0x37) [Reset = 0x00] |
| 0x38 | CLK_CFG18 | Clock configuration register 18 | 0x08 | CLK_CFG18 Register (Address = 0x38) [Reset = 0x08] |

表 7-208. TAC5212 Registers (続き)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------------|------------------------------------|-------------|--|
| 0x39 | CLK_CFG19 | Clock configuration register 19 | 0x20 | CLK_CFG19 Register (Address = 0x39) [Reset = 0x20] |
| 0x3A | CLK_CFG20 | Clock configuration register 20 | 0x04 | CLK_CFG20 Register (Address = 0x3A) [Reset = 0x04] |
| 0x3B | CLK_CFG21 | Clock configuration register 21 | 0x00 | CLK_CFG21 Register (Address = 0x3B) [Reset = 0x00] |
| 0x3C | CLK_CFG22 | Clock configuration register 18 | 0x01 | CLK_CFG22 Register (Address = 0x3C) [Reset = 0x01] |
| 0x3D | CLK_CFG23 | Clock configuration register 18 | 0x01 | CLK_CFG23 Register (Address = 0x3D) [Reset = 0x01] |
| 0x3E | CLK_CFG24 | Clock configuration register 21 | 0x01 | CLK_CFG24 Register (Address = 0x3E) [Reset = 0x01] |
| 0x44 | CLK_CFG30 | | 0x00 | CLK_CFG30 Register (Address = 0x44) [Reset = 0x00] |
| 0x45 | CLK_CFG31 | | 0x00 | CLK_CFG31 Register (Address = 0x45) [Reset = 0x00] |
| 0x46 | CLKOUT_CFG1 | CLKOUT configuration register 1 | 0x00 | CLKOUT_CFG1 Register (Address = 0x46) [Reset = 0x00] |
| 0x47 | CLKOUT_CFG2 | CLKOUT configuration register 2 | 0x01 | CLKOUT_CFG2 Register (Address = 0x47) [Reset = 0x01] |
| 0x49 | SARCLK_CFG1 | SAR clock configuration register 1 | 0x00 | SARCLK_CFG1 Register (Address = 0x49) [Reset = 0x00] |
| 0x5B | ADC_OVRD_FLAG | | 0x00 | ADC_OVRD_FLAG Register (Address = 0x5B) [Reset = 0x00] |

7.5.3.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in [表 7-209](#).

Return to the [Summary Table](#).

The device memory map is divided into pages. This register sets the page.

表 7-209. PAGE_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-----------|--|
| 7-0 | PAGE[7:0] | R/W | 00000000b | These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255 |

7.5.3.2 SASI_CFG0 Register (Address = 0x1A) [Reset = 0x30]

SASI_CFG0 is shown in [表 7-210](#).

Return to the [Summary Table](#).

This register is the ASI configuration register 0.

表 7-210. SASI_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7-6 | SASI_FORMAT[1:0] | R/W | 00b | Secondary ASI protocol format. 0d = TDM mode 1d = I ² S mode 2d = LJ (left-justified) mode 3d = Reserved; Don't use |
| 5-4 | SASI_WLEN[1:0] | R/W | 11b | Secondary ASI word or slot length. 0d = 16 bits (Recommended this setting to be used with 10-kΩ input impedance configuration) 1d = 20 bits 2d = 24 bits 3d = 32 bits |
| 3 | SASI_FSYNC_POL | R/W | 0b | ASI FSYNC polarity (for SASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol |
| 2 | SASI_BCLK_POL | R/W | 0b | ASI BCLK polarity (for SASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol |
| 1 | SASI_BUS_ERR | R/W | 0b | ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection |
| 0 | SASI_BUS_ERR_RCOV | R/W | 0b | ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until host configures the device |

7.5.3.3 SASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00]

SASI_TX_CFG0 is shown in [表 7-211](#).

Return to the [Summary Table](#).

This register is the SASI TX configuration register 0.

表 7-211. SASI_TX_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | SASI_TX_EDGE | R/W | 0b | Secondary ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in SASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting |

表 7-211. SASI_TX_CFG0 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 6 | SASI_TX_FILL | R/W | 0b | Secondary ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles |
| 5 | SASI_TX_LSB | R/W | 0b | Secondary ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle |
| 4-3 | SASI_TX_KEEPER[1:0] | R/W | 00b | Secondary ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles |
| 2 | SASI_TX_USE_INT_FSYNC | R/W | 0b | Secondary ASI uses internal FSYNC for output data generation in controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data generation 1d = Use internal FSYNC for ASI protocol data generation |
| 1 | SASI_TX_USE_INT_BCLK | R/W | 0b | Secondary ASI uses internal BCLK for output data generation in controller mode configuration. 0d = Use external BCLK for ASI protocol data generation 1d = Use internal BCLK for ASI protocol data generation |
| 0 | SASI_TDM_PULSE_WIDTH | R/W | 0b | Secondary ASI fsync pulse width in TDM format. 0d = Fsync pulse is 1 bclk period wide 1d = Fsync pulse is 2 bclk period wide |

7.5.3.4 SASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00]

SASI_TX_CFG1 is shown in 表 7-212.

Return to the [Summary Table](#).

This register is the SASI TX configuration register 1.

表 7-212. SASI_TX_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|--------|---|
| 7-5 | RESERVED | R | 000b | Reserved bits; Write only reset value |
| 4-0 | SASI_TX_OFFSET[4:0] | R/W | 00000b | Secondary ASI output data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

7.5.3.5 SASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00]

SASI_TX_CFG2 is shown in [表 7-213](#).

Return to the [Summary Table](#).

This register is the SASI TX configuration register 2.

表 7-213. SASI_TX_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7 | SASI_TX_CH8_SEL | R/W | 0b | Secondary ASI output channel 8 select. 0d = Secondary ASI channel 8 output is on DOUT 1d = Secondary ASI channel 8 output is on DOUT2 |
| 6 | SASI_TX_CH7_SEL | R/W | 0b | Secondary ASI output channel 7 select. 0d = Secondary ASI channel 7 output is on DOUT 1d = Secondary ASI channel 7 output is on DOUT2 |
| 5 | SASI_TX_CH6_SEL | R/W | 0b | Secondary ASI output channel 6 select. 0d = Secondary ASI channel 6 output is on DOUT 1d = Secondary ASI channel 6 output is on DOUT2 |
| 4 | SASI_TX_CH5_SEL | R/W | 0b | Secondary ASI output channel 5 select. 0d = Secondary ASI channel 5 output is on DOUT 1d = Secondary ASI channel 5 output is on DOUT2 |
| 3 | SASI_TX_CH4_SEL | R/W | 0b | Secondary ASI output channel 4 select. 0d = Secondary ASI channel 4 output is on DOUT 1d = Secondary ASI channel 4 output is on DOUT2 |
| 2 | SASI_TX_CH3_SEL | R/W | 0b | Secondary ASI output channel 3 select. 0d = Secondary ASI channel 3 output is on DOUT 1d = Secondary ASI channel 3 output is on DOUT2 |
| 1 | SASI_TX_CH2_SEL | R/W | 0b | Secondary ASI output channel 2 select. 0d = Secondary ASI channel 2 output is on DOUT 1d = Secondary ASI channel 2 output is on DOUT2 |
| 0 | SASI_TX_CH1_SEL | R/W | 0b | Secondary ASI output channel 1 select. 0d = Secondary ASI channel 1 output is on DOUT 1d = Secondary ASI channel 1 output is on DOUT2 |

7.5.3.6 SASI_TX_CH1_CFG Register (Address = 0x1E) [Reset = 0x00]

SASI_TX_CH1_CFG is shown in [表 7-214](#).

Return to the [Summary Table](#).

This register is the SASI TX Channel 1 configuration register.

表 7-214. SASI_TX_CH1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_TX_CH1_CFG | R/W | 0b | Secondary ASI output channel 1 configuration. 0d = Secondary ASI channel 1 output is in a tri-state condition 1d = Secondary ASI channel 1 output corresponds to ADC Channel 1 data |
| 4-0 | SASI_TX_CH1_SLOT_NUM[4:0] | R/W | 00000b | Secondary ASI output channel 1 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.7 SASI_TX_CH2_CFG Register (Address = 0x1F) [Reset = 0x01]

SASI_TX_CH2_CFG is shown in 表 7-215.

Return to the [Summary Table](#).

This register is the SASI TX Channel 2 configuration register.

表 7-215. SASI_TX_CH2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_TX_CH2_CFG | R/W | 0b | Secondary ASI output channel 2 configuration. 0d = Secondary ASI channel 2 output is in a tri-state condition 1d = Secondary ASI channel 2 output corresponds to ADC Channel 2 data |
| 4-0 | SASI_TX_CH2_SLOT_NUM[4:0] | R/W | 00001b | Secondary ASI output channel 2 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.8 SASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02]

SASI_TX_CH3_CFG is shown in 表 7-216.

Return to the [Summary Table](#).

This register is the SASI TX Channel 3 configuration register.

表 7-216. SASI_TX_CH3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH3_CFG[1:0] | R/W | 00b | Secondary ASI output channel 3 configuration. 0d = Secondary ASI channel 3 output is in a tri-state condition 1d = Secondary ASI channel 3 output corresponds to ADC Channel 3 data 2d = Secondary ASI channel 3 output corresponds to VBAT data 3d = Reserved |
| 4-0 | SASI_TX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Secondary ASI output channel 3 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.9 SASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03]

SASI_TX_CH4_CFG is shown in 表 7-217.

Return to the [Summary Table](#).

This register is the SASI TX Channel 4 configuration register.

表 7-217. SASI_TX_CH4_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH4_CFG[1:0] | R/W | 00b | Secondary ASI output channel 4 configuration. 0d = Secondary ASI channel 4 output is in a tri-state condition 1d = Secondary ASI channel 4 output corresponds to ADC Channel 4 data 2d = Secondary ASI channel 4 output corresponds to TEMP data 3d = Reserved |
| 4-0 | SASI_TX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Secondary ASI output channel 4 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.10 SASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04]

SASI_TX_CH5_CFG is shown in [表 7-218](#).

Return to the [Summary Table](#).

This register is the SASI TX Channel 5 configuration register.

表 7-218. SASI_TX_CH5_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH5_CFG[1:0] | R/W | 00b | Secondary ASI output channel 5 configuration. 0d = Secondary ASI channel 5 output is in a tri-state condition 1d = Secondary ASI channel 5 output corresponds to ASI Input Channel 1 loopback data 2d = Secondary ASI channel 5 output corresponds to echo reference channel 1 data 3d = Reserved |
| 4-0 | SASI_TX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Secondary ASI output channel 5 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.11 SASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05]

SASI_TX_CH6_CFG is shown in [表 7-219](#).

Return to the [Summary Table](#).

This register is the SASI TX Channel 6 configuration register.

表 7-219. SASI_TX_CH6_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--------------------------------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |

表 7-219. SASI_TX_CH6_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 6-5 | SASI_TX_CH6_CFG[1:0] | R/W | 00b | Secondary ASI output channel 6 configuration. 0d = Secondary ASI channel 6 output is in a tri-state condition 1d = Secondary ASI channel 6 output corresponds to ASI Input Channel 2 loopback data 2d = Secondary ASI channel 6 output corresponds to echo reference channel 2 data 3d = Reserved |
| 4-0 | SASI_TX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Secondary ASI output channel 6 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.12 SASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06]

SASI_TX_CH7_CFG is shown in 表 7-220.

Return to the [Summary Table](#).

This register is the SASI TX Channel 7 configuration register.

表 7-220. SASI_TX_CH7_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH7_CFG[1:0] | R/W | 00b | Secondary ASI output channel 7 configuration. 0d = Secondary ASI channel 7 output is in a tri-state condition 1d = Secondary ASI channel 7 output corresponds to {VBAT_WLby2, TEMP_WLby2} 2d = Secondary ASI channel 7 output corresponds to {echo_ref_ch1_wlby2, echo_ref_ch2_wlby2} 3d = Reserved |
| 4-0 | SASI_TX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Secondary ASI output channel 7 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.13 SASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07]

SASI_TX_CH8_CFG is shown in 表 7-221.

Return to the [Summary Table](#).

This register is the SASI TX Channel 8 configuration register.

表 7-221. SASI_TX_CH8_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_TX_CH8_CFG | R/W | 0b | Secondary ASI output channel 8 configuration. 0d = Secondary ASI channel 8 output is in a tri-state condition 1d = Secondary ASI channel 8 output corresponds to ICLA data |

表 7-221. SASI_TX_CH8_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|---|
| 4-0 | SASI_TX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Secondary ASI output channel 8 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.14 SASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00]

SASI_RX_CFG0 is shown in 表 7-222.

Return to the [Summary Table](#).

This register is the SASI RX configuration register 0.

表 7-222. SASI_RX_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|--------|--|
| 7 | SASI_RX_EDGE | R/W | 0b | Secondary ASI data input (on the primary and secondary data pin) receive edge. 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 6 | SASI_RX_USE_INT_FSYNC | R/W | 0b | Secondary ASI uses internal FSYNC for input data latching in controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data latching 1d = Use internal FSYNC for ASI protocol data latching |
| 5 | SASI_RX_USE_INT_BCLK | R/W | 0b | Secondary ASI uses internal BCLK for input data latching in controller mode configuration. 0d = Use external BCLK for ASI protocol data latching 1d = Use internal BCLK for ASI protocol data latching |
| 4-0 | SASI_RX_OFFSET[4:0] | R/W | 00000b | Secondary ASI data input MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I ² S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

7.5.3.15 SASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00]

SASI_RX_CFG1 is shown in 表 7-223.

Return to the [Summary Table](#).

This register is the SASI RX configuration register 1.

表 7-223. SASI_RX_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7 | SASI_RX_CH8_SEL | R/W | 0b | Secondary ASI input channel 8 select. 0d = Secondary ASI channel 8 input is on DIN 1d = Secondary ASI channel 8 input is on DIN2 |
| 6 | SASI_RX_CH7_SEL | R/W | 0b | Secondary ASI input channel 7 select. 0d = Secondary ASI channel 7 input is on DIN 1d = Secondary ASI channel 7 input is on DIN2 |
| 5 | SASI_RX_CH6_SEL | R/W | 0b | Secondary ASI input channel 6 select. 0d = Secondary ASI channel 6 input is on DIN 1d = Secondary ASI channel 6 input is on DIN2 |
| 4 | SASI_RX_CH5_SEL | R/W | 0b | Secondary ASI input channel 5 select. 0d = Secondary ASI channel 5 input is on DIN 1d = Secondary ASI channel 5 input is on DIN2 |
| 3 | SASI_RX_CH4_SEL | R/W | 0b | Secondary ASI input channel 4 select. 0d = Secondary ASI channel 4 input is on DIN 1d = Secondary ASI channel 4 input is on DIN2 |
| 2 | SASI_RX_CH3_SEL | R/W | 0b | Secondary ASI input channel 3 select. 0d = Secondary ASI channel 3 input is on DIN 1d = Secondary ASI channel 3 input is on DIN2 |
| 1 | SASI_RX_CH2_SEL | R/W | 0b | Secondary ASI input channel 2 select. 0d = Secondary ASI channel 2 input is on DIN 1d = Secondary ASI channel 2 input is on DIN2 |
| 0 | SASI_RX_CH1_SEL | R/W | 0b | Secondary ASI input channel 1 select. 0d = Secondary ASI channel 1 input is on DIN 1d = Secondary ASI channel 1 input is on DIN2 |

7.5.3.16 SASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x00]

SASI_RX_CH1_CFG is shown in [表 7-224](#).

Return to the [Summary Table](#).

This register is the SASI RX Channel 1 configuration register.

表 7-224. SASI_RX_CH1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH1_CFG | R/W | 0b | Secondary ASI input channel 1 configuration. 0d = Secondary ASI channel 1 input is disabled 1d = Secondary ASI channel 1 input corresponds to DAC Channel 1 data |
| 4-0 | SASI_RX_CH1_SLOT_NUM[4:0] | R/W | 00000b | Secondary ASI input channel 1 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.17 SASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x01]

SASI_RX_CH2_CFG is shown in [表 7-225](#).

Return to the [Summary Table](#).

This register is the SASI RX Channel 2 configuration register.

表 7-225. SASI_RX_CH2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH2_CFG | R/W | 0b | Secondary ASI input channel 2 configuration. 0d = Secondary ASI channel 2 input is disabled 1d = Secondary ASI channel 2 input corresponds to DAC Channel 2 data |
| 4-0 | SASI_RX_CH2_SLOT_NUM[4:0] | R/W | 00001b | Secondary ASI input channel 2 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.18 SASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02]

SASI_RX_CH3_CFG is shown in 表 7-226.

Return to the [Summary Table](#).

This register is the SASI RX Channel 3 configuration register.

表 7-226. SASI_RX_CH3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH3_CFG | R/W | 0b | Secondary ASI input channel 3 configuration. 0d = Secondary ASI channel 3 input is disabled 1d = Secondary ASI channel 3 input corresponds to DAC Channel 3 data |
| 4-0 | SASI_RX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Secondary ASI input channel 3 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.19 SASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03]

SASI_RX_CH4_CFG is shown in 表 7-227.

Return to the [Summary Table](#).

This register is the SASI RX Channel 4 configuration register.

表 7-227. SASI_RX_CH4_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH4_CFG | R/W | 0b | Secondary ASI input channel 4 configuration. 0d = Secondary ASI channel 4 input is disabled 1d = Secondary ASI channel 4 input corresponds to DAC Channel 4 data |

表 7-227. SASI_RX_CH4_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 4-0 | SASI_RX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Secondary ASI input channel 4 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.20 SASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04]

SASI_RX_CH5_CFG is shown in 表 7-228.

Return to the [Summary Table](#).

This register is the SASI RX Channel 5 configuration register.

表 7-228. SASI_RX_CH5_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH5_CFG[1:0] | R/W | 00b | Secondary ASI input channel 5 configuration. 0d = Secondary ASI channel 5 input is disabled 1d = Secondary ASI channel 5 input corresponds to DAC Channel 5 data 2d = Secondary ASI channel 5 input corresponds to ADC Channel 1 output loopback 3d = Reserved |
| 4-0 | SASI_RX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Secondary ASI input channel 5 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.21 SASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05]

SASI_RX_CH6_CFG is shown in 表 7-229.

Return to the [Summary Table](#).

This register is the SASI RX Channel 6 configuration register.

表 7-229. SASI_RX_CH6_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH6_CFG[1:0] | R/W | 00b | Secondary ASI input channel 6 configuration. 0d = Secondary ASI channel 6 input is disabled 1d = Secondary ASI channel 6 input corresponds to DAC Channel 6 data 2d = Secondary ASI channel 6 input corresponds to ADC Channel 2 output loopback 3d = Secondary ASI channel 6 input corresponds to ICLA device 1 data |

表 7-229. SASI_RX_CH6_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 4-0 | SASI_RX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Secondary ASI input channel 6 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.22 SASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06]

SASI_RX_CH7_CFG is shown in 表 7-230.

Return to the [Summary Table](#).

This register is the SASI RX Channel 7 configuration register.

表 7-230. SASI_RX_CH7_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH7_CFG[1:0] | R/W | 00b | Secondary ASI input channel 7 configuration. 0d = Secondary ASI channel 7 input is disabled 1d = Secondary ASI channel 7 input corresponds to DAC Channel 7 data 2d = Secondary ASI channel 7 input corresponds to ADC Channel 3 output loopback 3d = Secondary ASI channel 7 input corresponds to ICLA device 2 data |
| 4-0 | SASI_RX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Secondary ASI input channel 7 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.23 SASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07]

SASI_RX_CH8_CFG is shown in 表 7-231.

Return to the [Summary Table](#).

This register is the SASI RX Channel 8 configuration register.

表 7-231. SASI_RX_CH8_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH8_CFG[1:0] | R/W | 00b | Secondary ASI input channel 8 configuration. 0d = Secondary ASI channel 8 input is disabled 1d = Secondary ASI channel 8 input corresponds to DAC Channel 8 data 2d = Secondary ASI channel 8 input corresponds to ADC Channel 4 output loopback 3d = Secondary ASI channel 8 input corresponds to ICLA device 3 data |

表 7-231. SASI_RX_CH8_CFG Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|--------|--|
| 4-0 | SASI_RX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Secondary ASI input channel 8 slot assignment. 0d = TDM is slot 0 or I ² S, LJ is left slot 0 1d = TDM is slot 1 or I ² S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I ² S, LJ is left slot 15 16d = TDM is slot 16 or I ² S, LJ is right slot 0 17d = TDM is slot 17 or I ² S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I ² S, LJ is right slot 15 |

7.5.3.24 CLK_CFG12 Register (Address = 0x32) [Reset = 0x00]

CLK_CFG12 is shown in 表 7-232.

Return to the [Summary Table](#).

This register is the clock configuration register 12.

表 7-232. CLK_CFG12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 7-6 | PDIV_CLKSRC_SEL[1:0] | R/W | 00b | Source clock selection for PLL PDIV Divider. 0d = PLL_PDIV_IN_CLK is Primary ASI BCLK 1d = PLL_PDIV_IN_CLK is Secondary ASI BCLK 2d = PLL_PDIV_IN_CLK is CCLK 3d = PLL_PDIV_IN_CLK is internal Oscillator Clock |
| 5-3 | PASI_BCLK_DIV_CLK_SEL[2:0] | R/W | 000b | Primary ASI BCLK divider clock source selection. 0d = Primary ASI BCLK divider clock source is PLL output 1d = Reserved 2d = Primary ASI BCLK divider clock source is secondary ASI BCLK 3d = Primary ASI BCLK divider clock source is CCLK 4d = Primary ASI BCLK divider clock source is internal oscillator clock 5d = Primary ASI BCLK divider clock source is DSP clock 6d to 7d = Reserved |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset value |

7.5.3.25 CLK_CFG13 Register (Address = 0x33) [Reset = 0x00]

CLK_CFG13 is shown in 表 7-233.

Return to the [Summary Table](#).

表 7-233. CLK_CFG13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-4 | SASI_BCLK_DIV_CLK_SEL[2:0] | R/W | 000b | Secondary ASI BCLK divider clock source selection. 0d = Secondary ASI BCLK divider clock source is PLL output 1d = Secondary ASI BCLK divider clock source is primary ASI BCLK 2d = Reserved 3d = Secondary ASI BCLK divider clock source is CCLK 4d = Secondary ASI BCLK divider clock source is internal oscillator clock 5d = Secondary ASI BCLK divider clock source is DSP clock 6d to 7d = Reserved |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

7.5.3.26 CLK_CFG14 Register (Address = 0x34) [Reset = 0x10]

CLK_CFG14 is shown in 表 7-234.

Return to the [Summary Table](#).

This register is the clock configuration register 14.

表 7-234. CLK_CFG14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 7-6 | DIG_NM_DIV_CLK_SRC_SEL[1:0] | R/W | 00b | Source clock selection for DIG NMDIV CLK clock. 0d = DIG NM divider input clock is Primary ASI BCLK 1d = DIG NM divider input clock is Secondary ASI BCLK 2d = DIG NM divider input clock is CCLK 3d = DIG NM divider input clock is internal oscillator clock |
| 5-4 | ANA_NM_DIV_CLK_SRC_SEL[1:0] | R/W | 01b | Source clock selection for NMDIV CLK clock. 0d = NM divider input clock is PLL Output 1d = NM divider input clock is PLL Output 2d = NM divider input clock is DIG NM Divider Clock Source 3d = NM divider input clock is Primary ASI BCLK (Low Jitter Path) |
| 3-2 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 1-0 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |

7.5.3.27 CLK_CFG15 Register (Address = 0x35) [Reset = 0x01]

CLK_CFG15 is shown in 表 7-235.

Return to the [Summary Table](#).

This register is the clock configuration register 15.

表 7-235. CLK_CFG15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|----------|---|
| 7-0 | PLL_PDIV[7:0] | R/W | 0000001b | PLL pre-scaler P-divider value (Don't care when auto detection is enabled) 0d = PLL PDIV value is 256 1d = PLL PDIV value is 1 2d = PLL PDIV value is 2 3d to 254d = PLL PDIV value is as per configuration 255d = PLL PDIV value is 255 |

7.5.3.28 CLK_CFG16 Register (Address = 0x36) [Reset = 0x00]

CLK_CFG16 is shown in 表 7-236.

Return to the [Summary Table](#).

This register is the clock configuration register 16.

表 7-236. CLK_CFG16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|---------|--|
| 7 | PLL_JMUL_MSB | R/W | 0b | PLL integer portion J-multiplier value MSB bit. (Don't care when auto detection is enabled) |
| 6 | PLL_DIV_CLK_DIV_BY_2 | R/W | 0b | PLL DIV clock divide by 2 configuration 0d = No divide/2 inside PLL 1d = PLL does a divide/2 |
| 5-0 | PLL_DMUL_MSB[5:0] | R/W | 000000b | PLL fractional portion D-multiplier value MSB bits. (Don't care when auto detection is enabled) |

7.5.3.29 CLK_CFG17 Register (Address = 0x37) [Reset = 0x00]

CLK_CFG17 is shown in [表 7-237](#).

Return to the [Summary Table](#).

This register is the clock configuration register 17.

表 7-237. CLK_CFG17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|---|
| 7-0 | PLL_DMUL_LSB[7:0] | R/W | 00000000b | PLL fractional portion D-multiplier value LSB byte. Above D-multiplier value MSB bits (PLL_DMUL_MSB) along with this LSB byte (PLL_DMUL_LSB) is concatenated to determine final D-multiplier value. (Don't care when auto detection is enabled) 0d = PLL DMUL value is 0 1d = PLL DMUL value is 1 2d = PLL DMUL value is 2 3d to 9998d = PLL JMUL value is as per configuration 9999d = PLL JMUL value is 9999 10000d to 16383d = Reserved; Don't use |

7.5.3.30 CLK_CFG18 Register (Address = 0x38) [Reset = 0x08]

CLK_CFG18 is shown in [表 7-238](#).

Return to the [Summary Table](#).

This register is the clock configuration register 18.

表 7-238. CLK_CFG18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-----------|--|
| 7-0 | PLL_JMUL_LSB[7:0] | R/W | 00001000b | PLL integer portion J-multiplier value LSB byte. Above J-multiplier value MSB bit (PLL_JMUL_MSB) along with this LSB byte (PLL_JMUL_LSB) is concatenated to determine final J-multiplier value. (Don't care when auto detection is enabled) 0d = Reserved; Don't use 1d = PLL JMUL value is 1 2d = PLL JMUL value is 2 3d to 510d = PLL JMUL value is as per configuration 511d = PLL JMUL value is 511 |

7.5.3.31 CLK_CFG19 Register (Address = 0x39) [Reset = 0x20]

CLK_CFG19 is shown in [表 7-239](#).

Return to the [Summary Table](#).

This register is the clock configuration register 19.

表 7-239. CLK_CFG19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-5 | NDIV[2:0] | R/W | 001b | NDIV divider value. (Don't care when auto detection is enabled) 0d = NDIV value is 8 1d = NDIV value is 1 2d = NDIV value is 2 3d to 6d = NDIV value is as per configuration 7d = NDIV value is 7 |

表 7-239. CLK_CFG19 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 4-2 | PDM_DIV[2:0] | R/W | 000b | PDM divider value. (Don't care when auto detection is enabled) 0d = PDM_DIV value is 1 1d = PDM_DIV value is 2 2d = PDM_DIV value is 4 3d = PDM_DIV value is 8 4d = PDM_DIV value is 16 5d-7d Reserved |
| 1-0 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |

7.5.3.32 CLK_CFG20 Register (Address = 0x3A) [Reset = 0x04]

CLK_CFG20 is shown in [表 7-240](#).

Return to the [Summary Table](#).

This register is the clock configuration register 20.

表 7-240. CLK_CFG20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|---------|--|
| 7-2 | MDIV[5:0] | R/W | 000001b | MDIV divider value. (Don't care when auto detection is enabled) 0d = MDIV value is 64 1d = MDIV value is 1 2d = MDIV value is 2 3d to 62d = MDIV value is as per configuration 63d = MDIV value is 63 |
| 1-0 | DIG_ADC_MODCLK_DIV[1:0] | R/W | 00b | ADC modulator clock divider value. (Don't care when auto detection is enabled) 0d = DIG_ADC_MODCLK_DIV value is 1 1d = DIG_ADC_MODCLK_DIV value is 2 2d = DIG_ADC_MODCLK_DIV value is 4 3d = Reserved |

7.5.3.33 CLK_CFG21 Register (Address = 0x3B) [Reset = 0x00]

CLK_CFG21 is shown in [表 7-241](#).

Return to the [Summary Table](#).

This register is the clock configuration register 21.

表 7-241. CLK_CFG21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 7-6 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 5-4 | DIG_DAC_MODCLK_DIV[1:0] | R/W | 00b | DAC modulator clock divider value. (Don't care when auto detection is enabled) 0d = DIG_DAC_MODCLK_DIV value is 1 1d = DIG_DAC_MODCLK_DIV value is 2 2d = DIG_DAC_MODCLK_DIV value is 4 3d = Reserved |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | PASI_BDIV_MSB | R/W | 0b | Primary ASI BCLK divider value MSB bit. (Don't care when auto detection is enabled) |
| 1 | SASI_BDIV_MSB | R/W | 0b | Secondary ASI BCLK divider value MSB bit. (Don't care when auto detection is enabled) |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

7.5.3.34 CLK_CFG22 Register (Address = 0x3C) [Reset = 0x01]

CLK_CFG22 is shown in 表 7-242.

Return to the [Summary Table](#).

This register is the clock configuration register 18.

表 7-242. CLK_CFG22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-----------|---|
| 7-0 | PASI_BDIV_LSB[7:0] | R/W | 00000001b | Secondary ASI BCLK divider value. (Don't care when auto detection is enabled) 0d = SASI BCLK divider value is 512 1d = SASI BCLK divider value is 1 2d = SASI BCLK divider value is 2 3d to 62d = SASI BCLK divider value is as per configuration 63d = SASI BCLK divider value is 511 |

7.5.3.35 CLK_CFG23 Register (Address = 0x3D) [Reset = 0x01]

CLK_CFG23 is shown in 表 7-243.

Return to the [Summary Table](#).

This register is the clock configuration register 18.

表 7-243. CLK_CFG23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-----------|---|
| 7-0 | SASI_BDIV_LSB[7:0] | R/W | 00000001b | Secondary ASI BCLK divider value. (Don't care when auto detection is enabled) 0d = SASI BCLK divider value is 512 1d = SASI BCLK divider value is 1 2d = SASI BCLK divider value is 2 3d to 62d = SASI BCLK divider value is as per configuration 63d = SASI BCLK divider value is 511 |

7.5.3.36 CLK_CFG24 Register (Address = 0x3E) [Reset = 0x01]

CLK_CFG24 is shown in 表 7-244.

Return to the [Summary Table](#).

This register is the clock configuration register 21.

表 7-244. CLK_CFG24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|---------|--|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5-0 | ANA_NM_DIV[5:0] | R/W | 000001b | Analog N-M DIV divider value. (Don't care when auto detection is enabled) 0d = ANA_NM_DIV value is 64 1d = ANA_NM_DIV value is 1 2d = ANA_NM_DIV value is 2 3d to 62d = ANA_NM_DIV value is as per configuration 63d = NDIV value is 63 |

7.5.3.37 CLK_CFG30 Register (Address = 0x44) [Reset = 0x00]

CLK_CFG30 is shown in 表 7-245.

Return to the [Summary Table](#).

表 7-245. CLK_CFG30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|--------|--|
| 7-3 | RESERVED | R | 00000b | Reserved bits; Write only reset value |
| 2 | NDIV_EN | R/W | 0b | NDIV divider enable 0d = divider disabled 1d = divider enabled |
| 1 | MDIV_EN | R/W | 0b | MDIV divider enable 0d = divider disabled 1d = divider enabled |
| 0 | PDM_DIV_EN | R/W | 0b | PDM divider enable 0d = divider disabled 1d = divider enabled |

7.5.3.38 CLK_CFG31 Register (Address = 0x45) [Reset = 0x00]

CLK_CFG31 is shown in 表 7-246.

Return to the [Summary Table](#).

表 7-246. CLK_CFG31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | DIG_ADC_MODCLK_DIV_EN | R/W | 0b | ADC MODCLK divider enable 0d = divider disabled 1d = divider enabled |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | DIG_DAC_MODCLK_DIV_EN | R/W | 0b | DAC MODCLK divider enable 0d = divider disabled 1d = divider enabled |
| 3 | PASI_BDIV_EN | R/W | 0b | PASI BDIV divider enable 0d = divider disabled 1d = divider enabled |
| 2 | SASI_BDIV_EN | R/W | 0b | SASI BDIV divider enable 0d = divider disabled 1d = divider enabled |
| 1 | PASI_FSYNC_DIV_EN | R/W | 0b | PASI FSYNC DIV divider enable 0d = divider disabled 1d = divider enabled |
| 0 | SASI_FSYNC_DIV_EN | R/W | 0b | SASI FSYNC DIV divider enable 0d = divider disabled 1d = divider enabled |

7.5.3.39 CLKOUT_CFG1 Register (Address = 0x46) [Reset = 0x00]

CLKOUT_CFG1 is shown in 表 7-247.

Return to the [Summary Table](#).

This register is the CLKOUT configuration register 1.

表 7-247. CLKOUT_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|--------|---------------------------------------|
| 7-3 | RESERVED | R | 00000b | Reserved bits; Write only reset value |

表 7-247. CLKOUT_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 2-0 | CLKOUT_CLK_SEL[2:0] | R/W | 000b | General Purpose CLKOUT divider clock source selection. 0d = Source clock is PLL output 1d = Source clock is primary ASI BCLK 2d = Source clock is secondary ASI BCLK 3d = Source clock is CCLK 4d = Source clock is internal oscillator clock 5d = Source clock is DSP clock 6d to 7d = Reserved |

7.5.3.40 CLKOUT_CFG2 Register (Address = 0x47) [Reset = 0x01]

CLKOUT_CFG2 is shown in 表 7-248.

Return to the [Summary Table](#).

This register is the CLKOUT configuration register 2.

表 7-248. CLKOUT_CFG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|----------|--|
| 7 | CLKOUT_DIV_EN | R/W | 0b | CLKOUT divider enable. 0d = CLKOUT divider disabled 1d = CLKOUT divider enabled |
| 6-0 | CLKOUT_DIV[6:0] | R/W | 0000001b | CLKOUT DIV divider value. 0d = CLKOUT_DIV value is 128 1d = CLKOUT_DIV value is 1 2d = CLKOUT_DIV value is 2 3d to 126d = CLKOUT_DIV value is as per configuration 127d = CLKOUT_DIV value is 127 |

7.5.3.41 SARCLK_CFG1 Register (Address = 0x49) [Reset = 0x00]

SARCLK_CFG1 is shown in 表 7-249.

Return to the [Summary Table](#).

This register is the SAR clock configuration register 1

表 7-249. SARCLK_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|---|
| 7-6 | SAR_CLK_FREQ_SEL[1:0] | R/W | 00b | SAR clock frequency mode 0d = SAR clock frequency is ~6MHz 1d = SAR clock frequency is ~3MHz 2d = SAR clock frequency is ~1.5MHz 3d = SAR clock frequency is ~12MHz (valid only when SAR clock is generated directly using internal oscillator clock) |
| 5 | SAR_CLK_SRC_AUTO_DISABLE | R/W | 0b | SAR divider source clock auto selection disable 0d = SAR divider source clock auto-selection based on clock detection scheme 1d = SAR divider source clock auto-selection disabled and selected based on BST_CLK_SRC_SEL |
| 4 | SAR_CLK_SRC_MANUAL_SEL | R/W | 0b | SAR clock source manual selection (don't care in auto mode) 0d = SAR clock generated based on Audio clock available for ADC/DAC 1d = SAR clock generated based on internal oscillator clock |
| 3 | SAR_CLK_EN_AUTO_DISABLE | R/W | 0b | SAR divider source clock auto selection disable 0d = SAR divider auto-enabled 1d = SAR divider enabled/disabled based on manual control using BST_CLK_EN |

表 7-249. SARCLK_CFG1 Register Field Descriptions (続き)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 2 | SAR_CLK_MANUAL_EN | R/W | 0b | SAR divider manual enable (don't care in auto mode) 0d = SAR divider disabled 1d = SAR divider enabled |
| 1-0 | SAR_CLK_MANUAL_DIV[1:0] | R/W | 00b | SAR divider value (don't care in auto mode) 0d = SAR divider value is 1 1d = SAR divider value is 2 2d = SAR divider value is 4 3d = SAR divider value is 8 |

7.5.3.42 ADC_OVRD_FLAG Register (Address = 0x5B) [Reset = 0x00]

ADC_OVRD_FLAG is shown in [表 7-250](#).

Return to the [Summary Table](#).

表 7-250. ADC_OVRD_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 7 | ADC_CH1_OVRD_LTCH | R | 0b | ADC CH1 OVRD fault (self clearing bit). 0b = No ADC CH1 OVRD fault 1b = ADC CH1 OVRD fault |
| 6 | ADC_CH2_OVRD_LTCH | R | 0b | ADC CH2 OVRD fault (self clearing bit). 0b = No ADC CH2 OVRD fault 1b = ADC CH2 OVRD fault |
| 5 | ADC_CH1_OVRD_LIVE | R | 0b | ADC CH1 OVRD fault (self clearing bit). 0b = No ADC CH1 OVRD fault 1b = ADC CH1 OVRD fault |
| 4 | ADC_CH2_OVRD_LIVE | R | 0b | ADC CH2 OVRD fault (self clearing bit). 0b = No ADC CH2 OVRD fault 1b = ADC CH2 OVRD fault |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TAC5212 is a stereo, high-performance audio codec that supports sample rates of up to 768 kHz. The device supports up to a total of 4 microphones for simultaneous recording which can be selected from up to 2 analog microphones or 4 digital pulse density modulation (PDM) microphones. The device also supports up to 4 channel simultaneous playback which can be configured as a 2 channel differential or psuedo differential output or up to 4 channel single-ended output with options for headphone and lineout drive capabilities.

Communication to the TAC5212 for configuration of the control registers is supported using an I²C or SPI interface. The device supports a highly flexible, audio serial interface (TDM, I²S, and LJ) to transmit audio data seamlessly in the system across devices.

8.2 Typical Application

8.2.1 Application

☒ 8-1 shows a typical configuration of the TAC5212 for an application using two analog ECM microphones for simultaneous recording and two channel lineout operation with an I²C control interface and a time-division multiplexing (TDM) audio data target interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

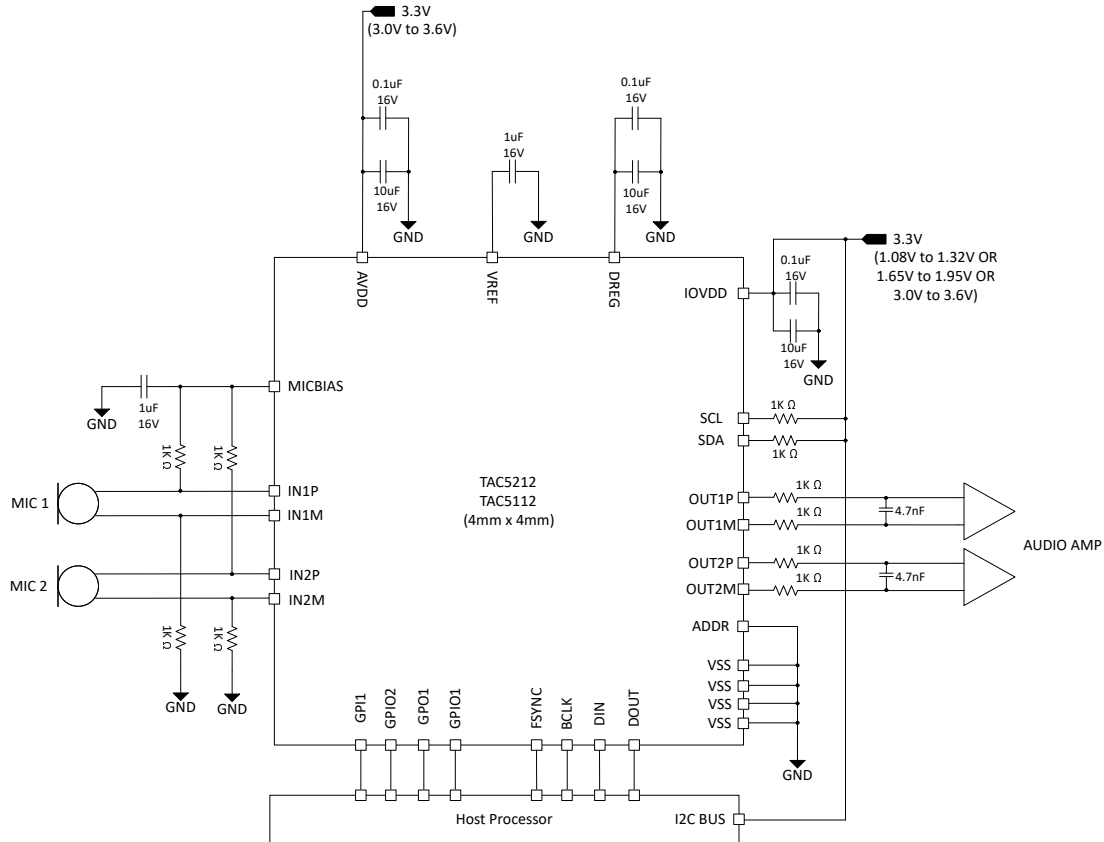


図 8-1. Stereo Microphone with Stereo Lineout Block Diagram

8.2.2 Design Requirements

表 8-1a lists the design parameters for this application.

表 8-1. Design Parameters

| PARAMETER | VALUE |
|------------------------------------|-------------------------|
| AVDD | 3.3 V |
| IOVDD | 1.2 V or 1.8 V or 3.3 V |
| AVDD supply current consumption | TBD |
| IOVDD supply current consumption | TBD |
| Maximum MICBIAS current | 5 mA |
| Load on OUT1M, OUT1P, OUT2M, OUT2P | >600 ohms |

8.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAC5212 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
 - a. Power up the IOVDD and AVDD power supplies
 - b. Wait for at least 1ms to allow the device to initialize the internal registers.
 - c. The device now goes into sleep mode (low-power mode < 10 μ A)
2. Transition from sleep mode to active mode whenever required for the operation:
 - a. Wake up the device by writing to P0_R2 to disable sleep mode
 - b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence

- c. Override the default configuration registers or programmable coefficients value as required (this step is optional)
- d. Enable all desired input channels by writing to P0_R118
- e. Enable all desired audio serial interface input/output channels by writing to P0_R40 to P0_R47 for DAC and P0_R30 to P0_R37 for ADC
- f. Power-up the ADC, DAC and MICBIAS by writing to P0_R120
- g. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

This specific step can be done at any point in the sequence after step a.

See the [セクション 7.3.2](#) section for supported sample rates and the BCLK to FSYNC ratio.

- h. The device recording data is now sent to the host processor using the TDM audio serial data bus and playback data from TDM is now played on the lineout
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
 - a. Enter sleep mode by writing to P0_R2 to enable sleep mode
 - b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
 - c. Read P0_R122 to check the device shutdown and sleep mode status
 - d. If the device P0_R122_D[7:5] status bit is 3'b100 then stop FSYNC and BCLK in the system
 - e. The device now goes into sleep mode (low-power mode < 10 μ A) and retains all register values
 4. Transition from sleep mode to active mode (again) as required for the recording operation:
 - a. Wake up the device by writing to P0_R2 to disable sleep mode
 - b. Wait at least 1 ms to allow the device to complete the internal wake-up sequence
 - c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
 - d. The device recording data is now sent to the host processor using the TDM audio serial data bus and playback data from TDM is now played on the lineout
 5. Repeat step 4 and step 5 as required for mode transitions

9 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, after all supplies are stable, then only initiate the I²C or SPI transactions to initialize the device.

For the supply power-up requirement, t_1 , t_2 must be at least 2 ms to allow the device to initialize the internal registers. See the [セクション 7.4](#) section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, t_4 , t_5 and t_6 must be at least 10 ms. This timing (as shown in [図 9-1](#)) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into shutdown mode. The device can also be immediately put into shutdown mode by ramping down power supplies, but doing so causes an abrupt shutdown.

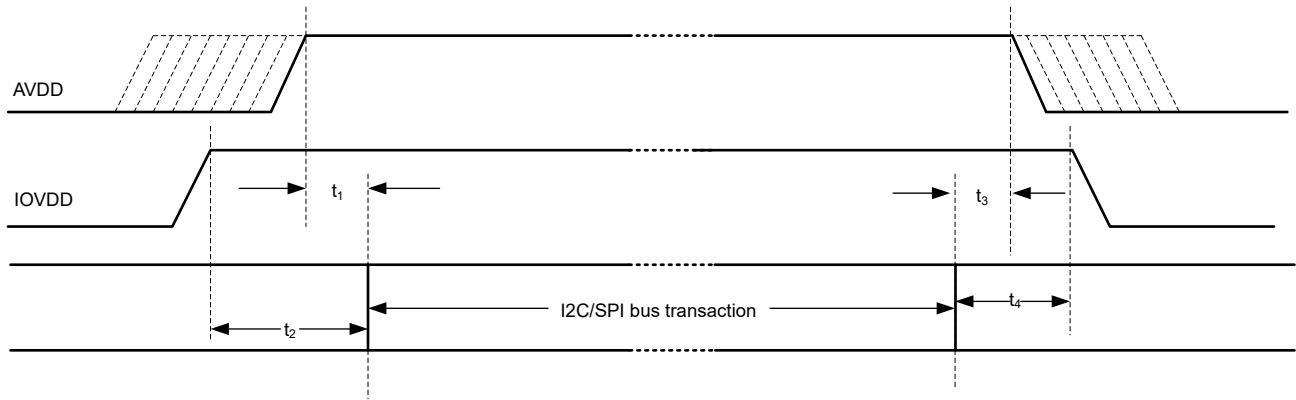


図 9-1. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/ μ s and that the wait time between a power-down and a power-up event is at least 100 ms. For supply ramp rate slower than 0.1 V/ms, host device must apply a software reset as first transaction before doing any device configuration. Make sure all digital input pins are at valid input levels and not toggling during supply sequencing.

The TAC5212 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[\[通知\]](#) をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

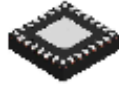
11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| December 2023 | * | Initial Release |

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

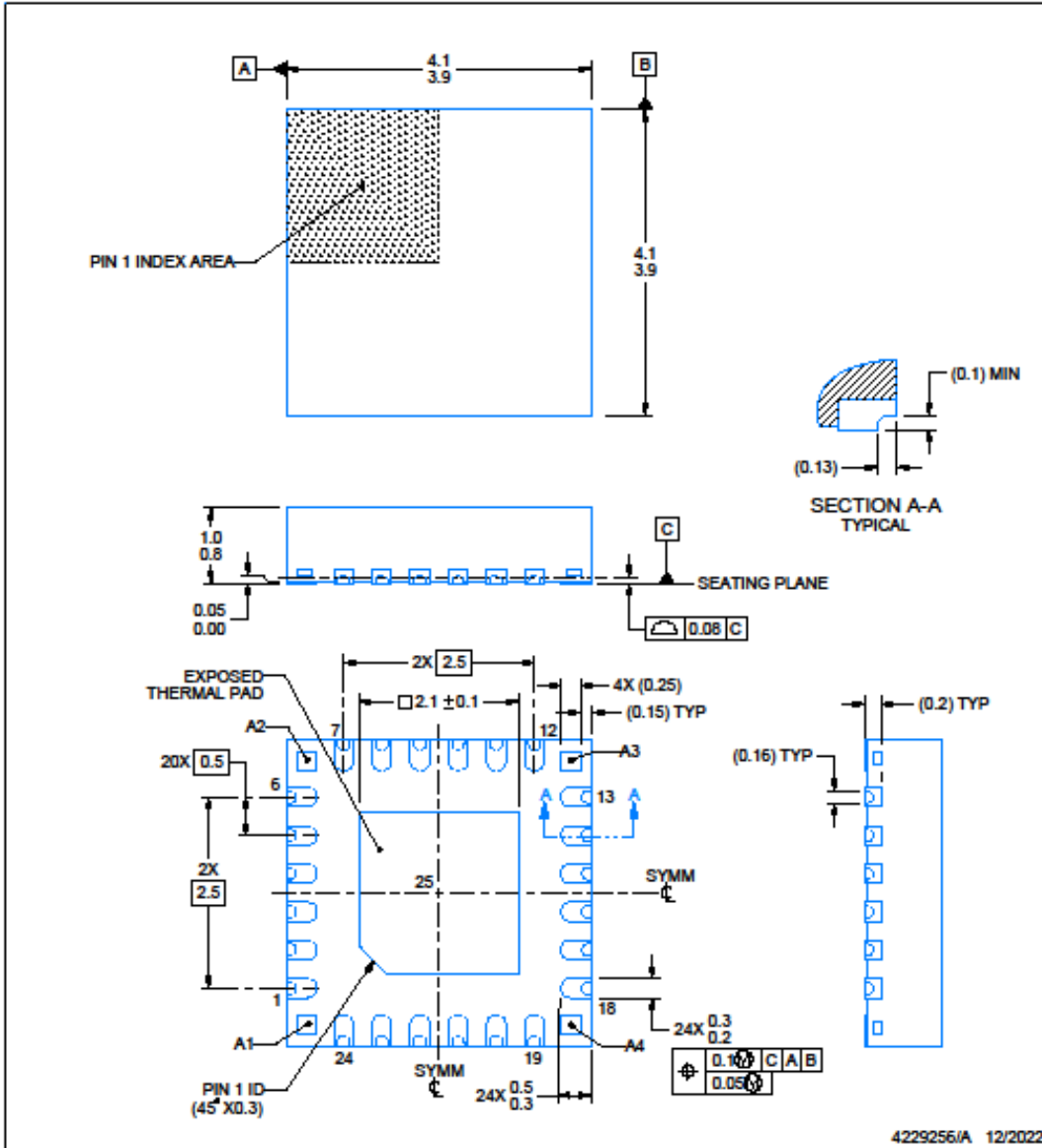


RGE0024W

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

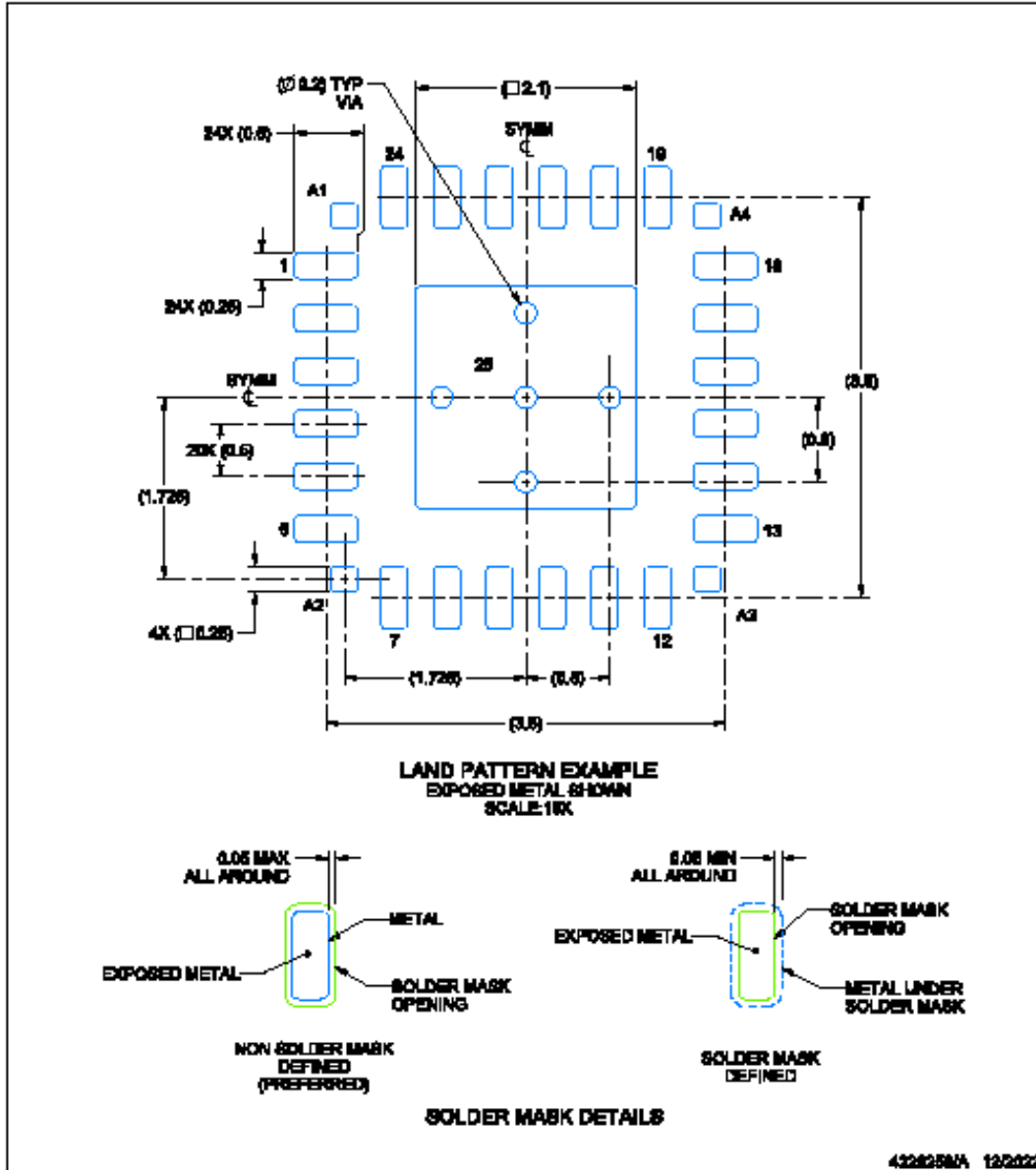


EXAMPLE BOARD LAYOUT

RGED024W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continues)

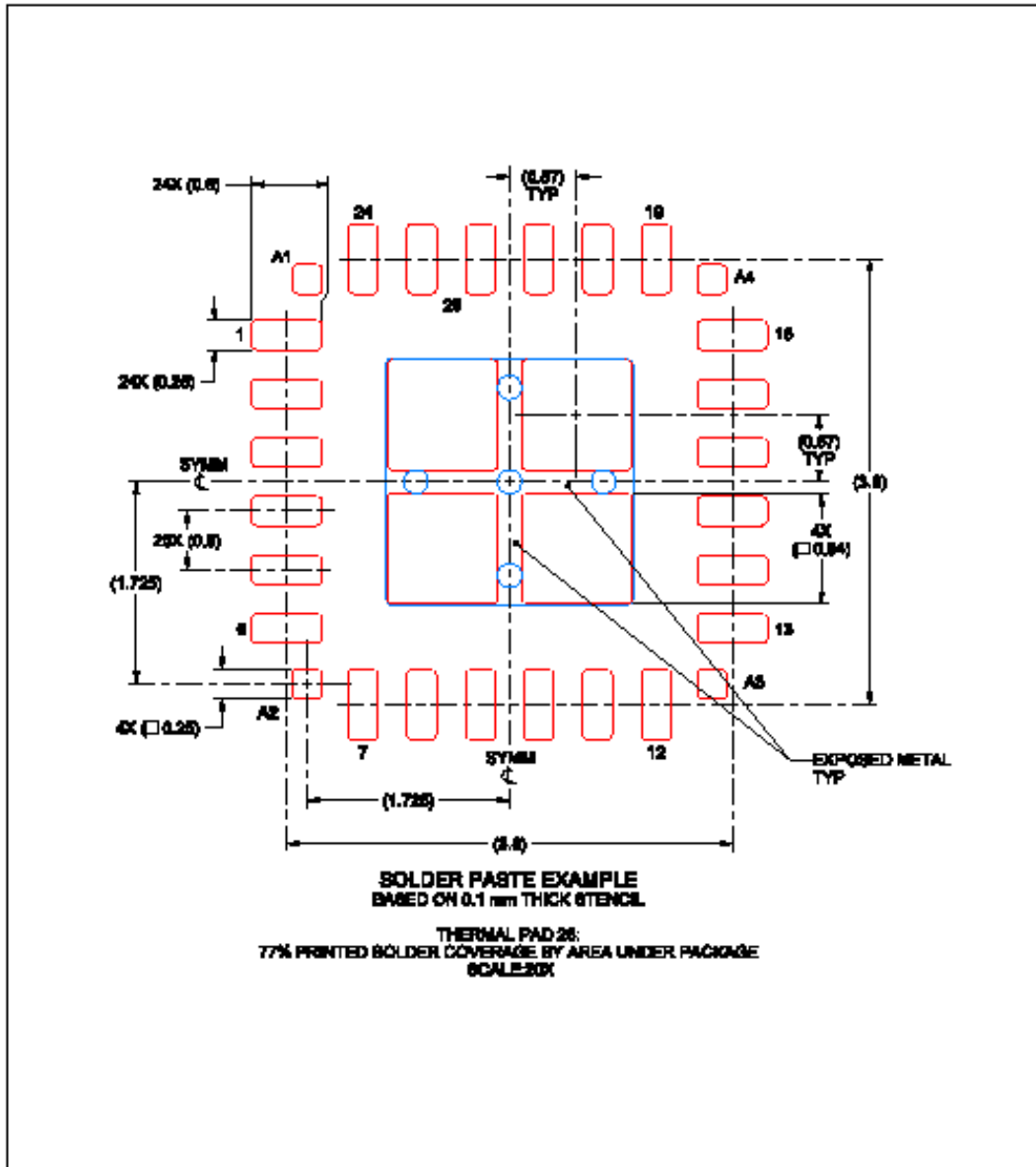
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments Solderability number SL10A271 (www.ti.com/lit/sls10a271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGED024W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

1. Laser cutting spawners with trapezoidal walls and rounded corners may offer better paste release. IPC-7535 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| XTAC5212IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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RGE 24

GENERIC PACKAGE VIEW

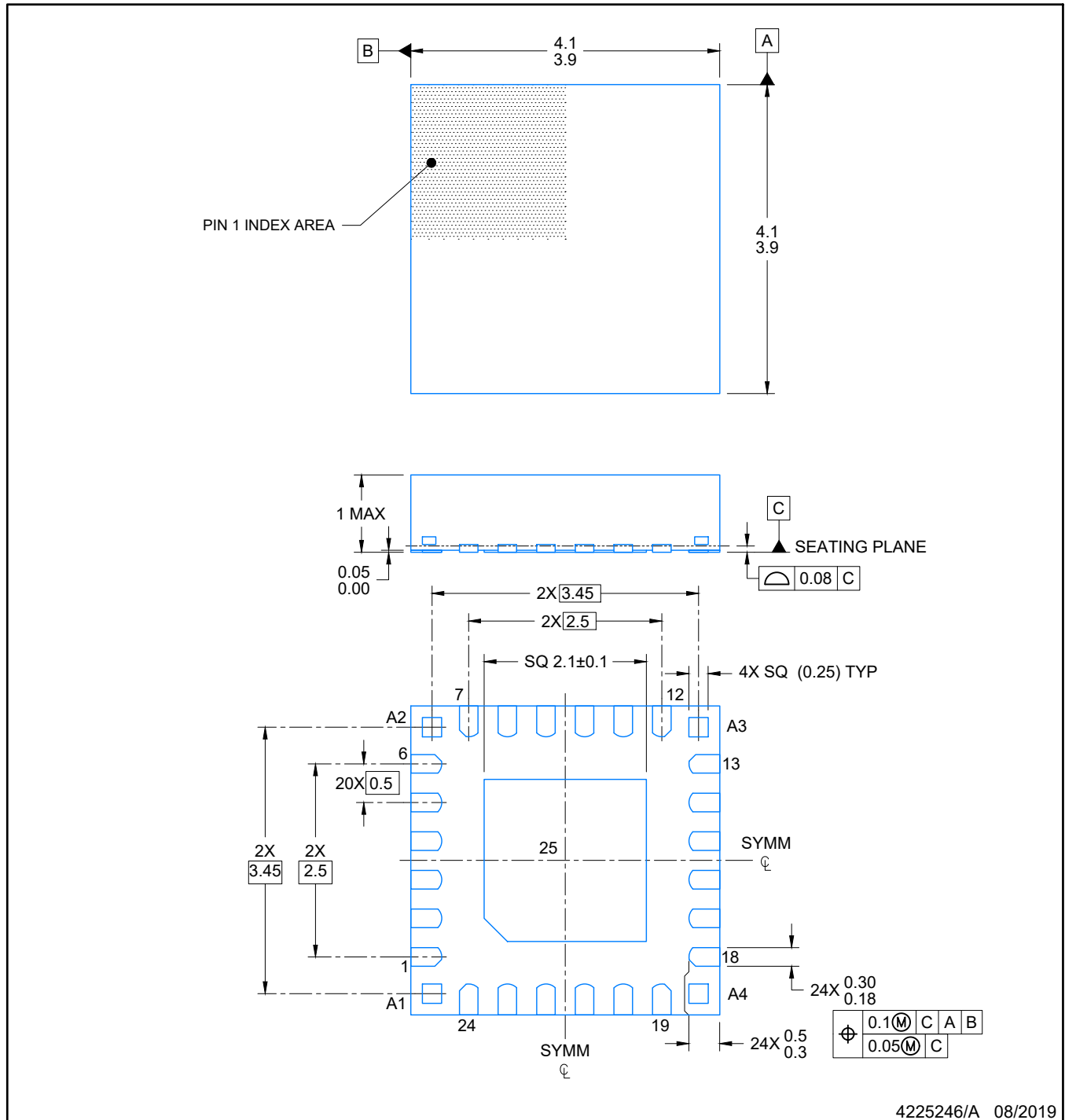
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



NOTES:

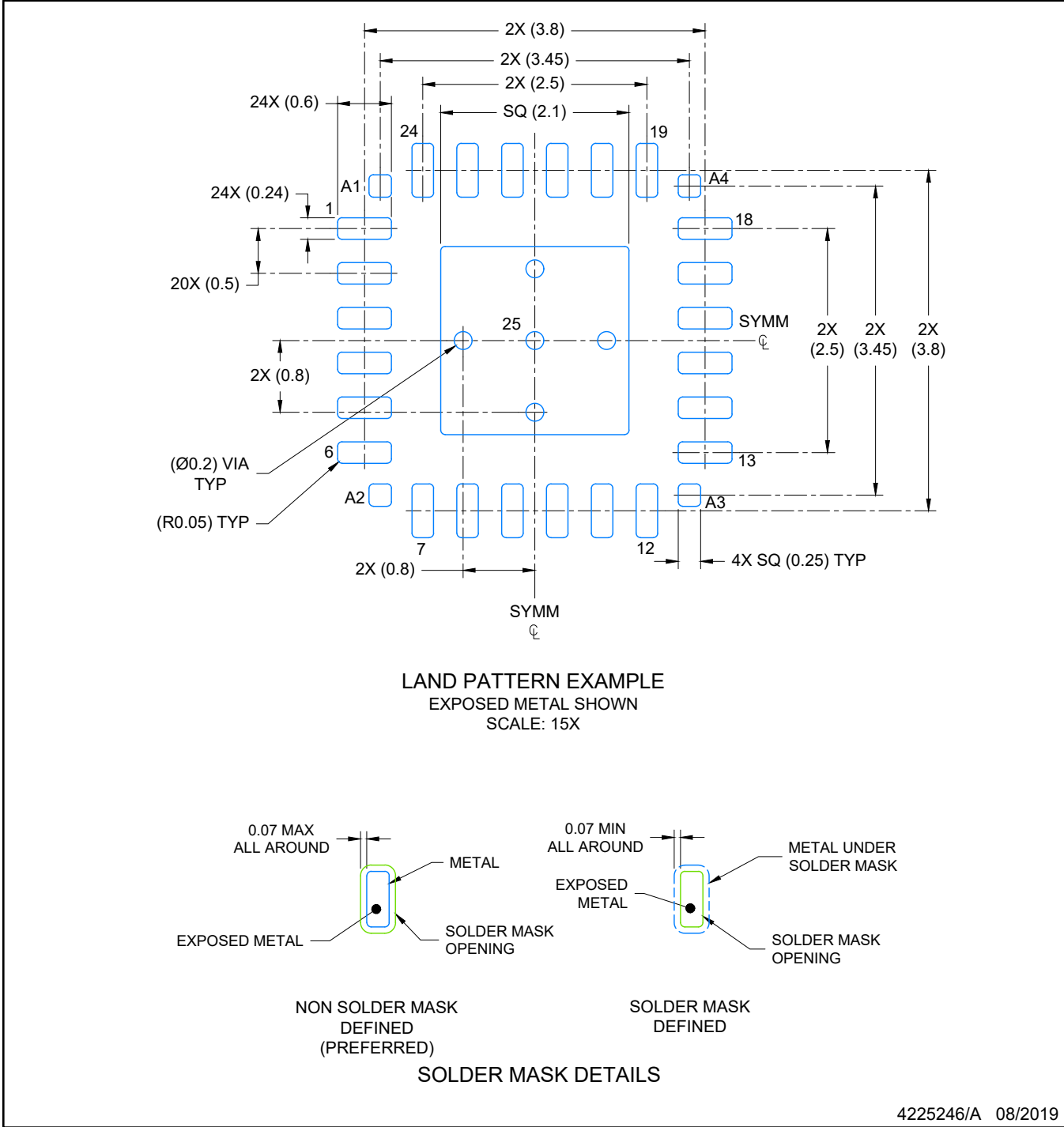
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGE0024R

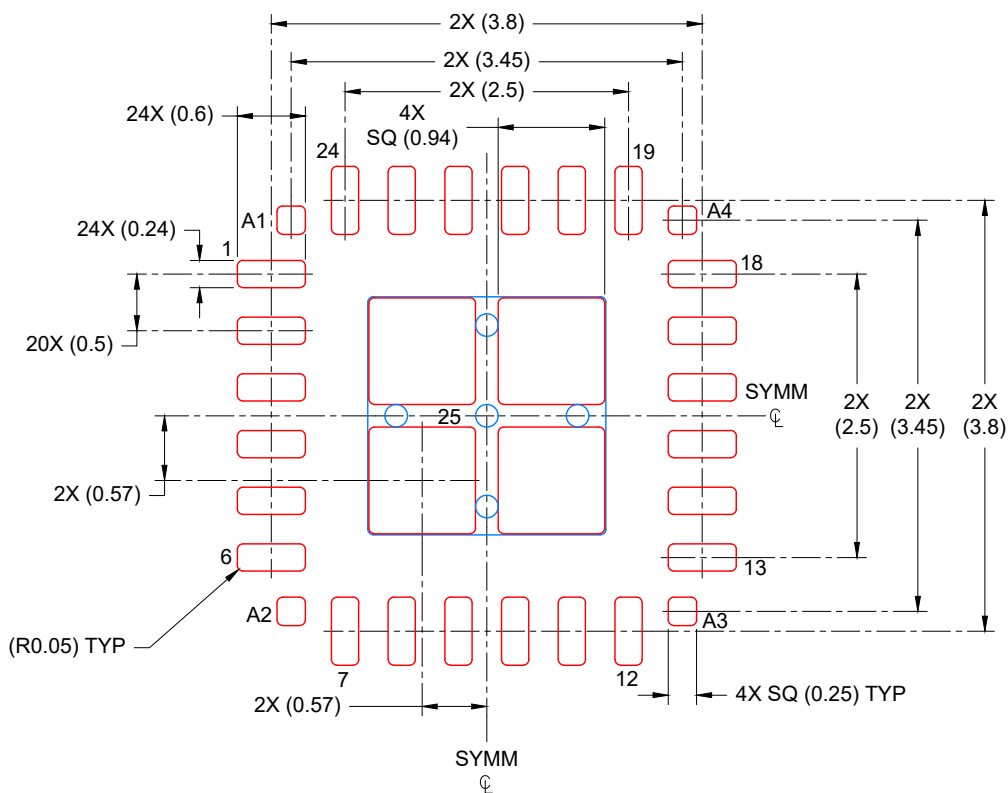
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 80% PRINTED COVERAGE BY AREA
 SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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