

# TAS5806M 高度な処理機能を備えた、低消費電力、インダクタレス、デジタル入力、ステレオ、閉ループ、23W Class-D オーディオ・アンプ

## 1 特長

- 複数の出力構成をサポート
  - 2.0 モードで  $2 \times 23\text{W}$  ( $8\Omega$ ,  $21\text{V}$ ,  $\text{THD+N}=1\%$ )
  - モノラル・モードで  $45\text{W}$  ( $4\Omega$ ,  $21\text{V}$ ,  $\text{THD+N}=1\%$ )
- 優れたオーディオ性能
  - $1\text{W}$ ,  $1\text{kHz}$ ,  $\text{PVDD} = 12\text{V}$  で  $\text{THD+N} \leq 0.03\%$
  - $\text{SNR} \geq 107\text{dB}$  (A 特性)、ノイズ・レベル  $< 40\mu\text{V}_{\text{RMS}}$
- ハイブリッド変調による低い静止電流
  - $16.5\text{mA}$  ( $\text{PVDD} = 13.5\text{V}$ ,  $22\mu\text{H} + 0.68\mu\text{F}$  フィルタの場合)
- 柔軟な電源構成
  - $\text{PVDD}$ :  $4.5\text{V} \sim 26.4\text{V}$
  - $\text{DVDD}$ とI/O:  $1.8\text{V} \sim 3.3\text{V}$
- 柔軟なオーディオ I/O
  - I<sup>2</sup>S, LJ, RJ, TDM, 3 線式デジタル・オーディオ・インターフェイス (MCLK 不要)
  - 32, 44.1, 48, 88.2, 96kHz のサンプル・レートをサポート
  - オーディオ・モニタ、サブチャンネル、エコー・キャンセルのための SDOUT
- 高度なオーディオ処理
  - マルチバンドの高度な DRC および AGL
  - 2x15 BQ、サーマル・フォールドバック、DC ブロッキング
  - 入力ミキサー、出力クロスオーバー、レベル・メータ
  - 5 BQ + 1 バンド DRC + サブウーファー・チャンネル用の THD マネージャ
- 自己保護機能内蔵
  - 隣接ピン間で短絡が発生してもデバイスが損傷しない
  - 過電流エラー (OCE)
  - 過熱警告 (OTW)
  - 過熱エラー (OTE)
  - 低電圧/過電圧誤動作防止 (UVLO/OVLO)
- システム統合が簡単
  - I<sup>2</sup>C ソフトウェア制御
  - ソリューション・サイズの低減
    - 開ループ・デバイスと比べて少ない受動部品数
    - $\text{PVDD} \leq 14\text{V}$  のほとんどの場合、インダクタレスで動作 (フェライト・ビーズ)
- TAS5806MD とピン互換

## 2 アプリケーション

- LCD TV、OLED TV
- ワイヤレス・スピーカー、音声アシスタント付きのスマート・スピーカー
- サウンドバー、有線スピーカー
- デスクトップ PC、ノート PC
- AV レシーバー、スマート・ホームおよび IoT 家電

## 3 概要

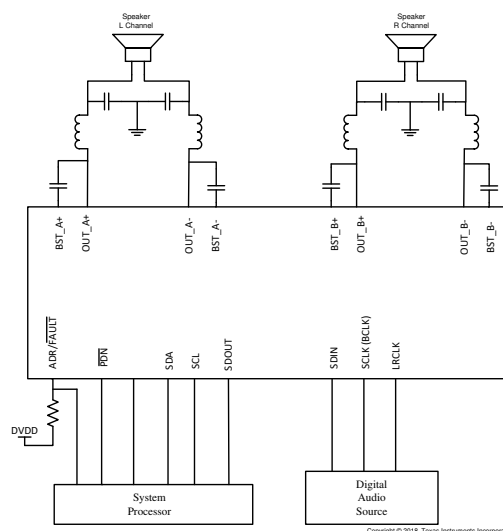
TAS5806M は、低消費電力と高音質を兼ね備えた低コスト・デジタル入力ソリューションを提供する高効率ステレオ閉ループ Class-D アンプです。このデバイスの内蔵オーディオ・プロセッサと 96kHz アーキテクチャは、SRC、チャンネルごとに 15 の BQ、音量制御、オーディオ・ミキシング、3 バンド 4 次 DRC、フルバンド AGL、THD マネージャ、レベル・メータを含む先進のオーディオ処理フローをサポートしています。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
TAS5806M	TSSOP (38) DCP	9.70mmx4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### ブロック概略図



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019年5月	*	初版

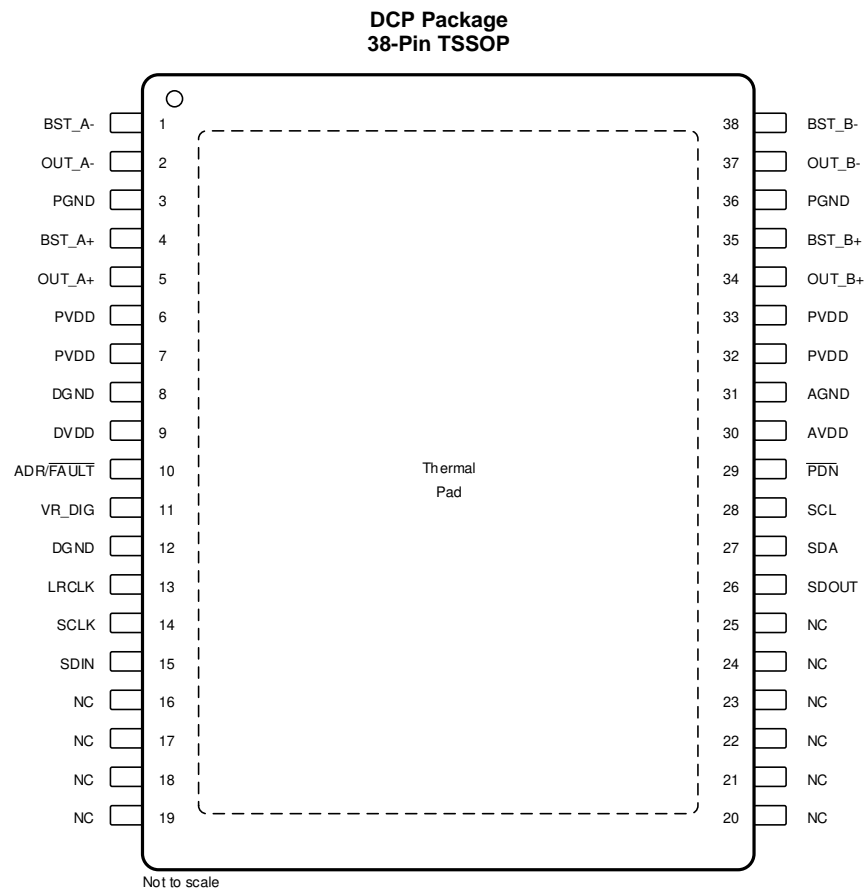
## 5 概要 (続き)

TAS5806M は、TI 独自のハイブリッド変調方式を採用しているため、静止電流が非常に小さく (13.5V の PVDD で 16.5mA)、携帯用オーディオ・アプリケーションのバッテリー動作時間を延長できます。先進の EMI 抑制テクノロジーにより、10W 未満のアプリケーションでは安価なフェライト・ビーズ・フィルタを活用して基板面積とシステム・コストを低減できます。

## 6 Device Comparison Table

ORDERABLE PART NUMBER	RECOMMENDED PVDD RANGE	R <sub>DS(ON)</sub> OPTION	Package	Headphone/Line Driver integrated
TAS5806M	4.5 V to 26.4 V	180 mΩ	TSSOP38 (DCP)	NO
TAS5805M	4.5 V to 26.4 V	180 mΩ	TSSOP28 (PWP)	NO
TAS5806MD	4.5 V to 26.4 V	180 mΩ	TSSOP38 (DCP)	YES
TAS5825M	4.5 V to 26.4 V	90 mΩ	QFN32 (RHB)	NO

## 7 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
DGND	8,12	G	Digital ground
DVDD	9	P	3.3-V or 1.8-V digital power supply
VR_DIG	11	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
ADR/ $\overline{\text{FAULT}}$	10	DIO	Different I <sup>2</sup> C device address can be set by selecting different pull up resistor to DVDD, see Table 3 for details. After power up, ADR/ $\overline{\text{FAULT}}$ can be redefine as $\overline{\text{FAULT}}$ , go to Page0, Book0, set register 0x61 = 0x0b first, then set register 0x60 = 0x01
LRCLK	13	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I <sup>2</sup> S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)

**Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
SCLK	14	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
SDIN	15	DI	Data line to the serial data port
SDOUT	26	DO	Serial Audio data output, the source data can select as Pre-DSP or Post DSP, by setting the register 0x30h.
SDA	27	DI/O	I2C serial control data interface input/output
SCL	28	DI	I2C serial control clock input
$\overline{\text{PDN}}$	29	DI	Power Down, active-low. $\overline{\text{PDN}}$ place the amplifier in Shutdown, turn off all internal regulators. Low, Power Down Device; High, Enable Device.
AVDD	30	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices
AGND	31	G	Analog ground
PVDD	6	P	PVDD voltage input
	7	P	
	32	P	
	33	P	
PGND	3	G	Ground reference for power device circuitry. Connect this pin to system ground.
	36	G	
OUT_A+	5	AO	Positive pin for differential speaker amplifier output A+
BST_A+	4	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
OUT_A-	2	AO	Negative pin for differential speaker amplifier output A-
BST_A-	1	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
BST_B-	38	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
OUT_B-	37	AO	Negative pin for differential speaker amplifier output B
BST_B+	35	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
OUT_B+	34	AO	Positive pin for differential speaker amplifier output B+
NC	16-25		Not connected inside the device (all "no connect" pins should be connected to ground for best thermal performance, however they can be used as routing channels if required.)
PowerPAD™	-	G	Connect to the system Ground

## 8 Specifications

### 8.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	-0.3	3.9	V
PVDD	PVDD supply	-0.3	30	V
V <sub>I(DigIn)</sub>	DVDD referenced digital inputs <sup>(2)</sup>	-0.5	V <sub>DVDD</sub> + 0.5	V
V <sub>I(SPK_OUT.xx)</sub>	Voltage at speaker output pins	-0.3	32	V
T <sub>A</sub>	Ambient operating temperature	-25	85	°C
T <sub>stg</sub>	Storage temperature	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) DVDD referenced digital pins include: ADR/FAULT, LRCLK, SCLK, SCL, SDA, SDIN,PDN

### 8.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>(POWER)</sub>	Power supply inputs	DVDD	1.62		3.63	V
		PVDD	4.5		26.4	
R <sub>SPK</sub>	Minimum speaker load	BTL Mode (4.5V ≤ PVDD ≤ 16V)	3.2			Ω
		BTL Mode (16V < PVDD ≤ 24V)	4.8			Ω
R <sub>SPK</sub>	Minimum speaker load	PBTL Mode (4.5V ≤ PVDD ≤ 16V)	1.6			Ω
		PBLT Mode (16V < PVDD ≤ 24V)	2.4			Ω
L <sub>OUT</sub>	Minimum inductor value in LC filter under short-circuit condition		1	4.7		μH

### 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TSSOP (DCP) 38 PINS			UNIT
		JEDEC STANDARD 2-LAYER PCB	JEDEC STANDARD 4-LAYER PCB	TAS5806MEVM-4 4-LAYER PCB	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	N/A	29	23.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	N/A	18.5	N/A	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	N/A	9.2	N/A	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	N/A	0.5	1.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	N/A	9.2	8.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	2.3	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 8.5 Electrical Characteristics

Free-air room temperature 25°C ,DVDD=3.3V,1SPW mode with LC filter, BD mode with Ferrite bead filter (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL I/O</b>						
$ I_{IH} $	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	$\mu A$
$ I_{IL} $	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = 0 V$			-10	$\mu A$
$V_{IH(DigIn)}$	Input logic high threshold for DVDD referenced digital inputs		70%			$V_{DVDD}$
$V_{IL(DigIn)}$	Input logic low threshold for DVDD referenced digital inputs				30%	$V_{DVDD}$
$V_{OH(DigIn)}$	Output logic high voltage level	$I_{OH} = 2 mA$	80%			$V_{DVDD}$
$V_{OL(DigIn)}$	Output logic low voltage level	$I_{OH} = -2 mA$			20%	$V_{DVDD}$
<b>I<sup>2</sup>C CONTROL PORT</b>						
$C_L(I2C)$	Allowable load capacitance for each I <sup>2</sup> C line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
<b>SERIAL AUDIO PORT</b>						
$t_{DLY}$	Required LRCLK/FS to SCLK rising edge delay		5			ns
$D_{SCLK}$	Allowable SCLK duty cycle		40%		60%	
$f_s$	Supported input sample rates		32		96	kHz
$f_{SCLK}$	Supported SCLK frequencies		32		64	$f_s$
$f_{SCLK}$	SCLK frequency				24.576	MHz
<b>SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS)</b>						
$I_{cc}$	Quiescent supply current on DVDD	$\overline{PDN}=2V, DVDD=3.3V, Play mode$		18		mA
$I_{cc}$	Quiescent supply current on DVDD	$\overline{PDN}=2V, DVDD=3.3V, Sleep mode$		0.75		mA
$I_{cc}$	Quiescent supply current on DVDD	$\overline{PDN}=2V, DVDD=3.3V, Deep Sleep mode$		0.75		mA
$I_{cc}$	Quiescent supply current on DVDD	$\overline{PDN}=0V, DVDD=3.3V, Shutdown mode$		5.5		$\mu A$
$I_{cc}$	Quiescent supply current on PVDD	$\overline{PDN}=2V, V_{PVDD}=13.5V, LC filter=10\mu H+0.68\mu F, F_{sw}=768kHz, BD Modulation, Play mode,BTL mode$		32.5		mA
$I_{cc}$	Quiescent supply current on PVDD	$\overline{PDN}=2V, V_{PVDD}=13.5V, LC filter=22\mu H+0.68\mu F, F_{sw}=384kHz, Hybrid Modulation, Play mode,BTL mode$		16.5		mA
$I_{cc}$	Quiescent supply current on PVDD	$\overline{PDN}=2V, V_{PVDD}=13.5V, Output Hiz Mode$		10.4		mA
$I_{cc}$	Quiescent supply current on PVDD	$\overline{PDN}=2V, V_{PVDD}=13.5V, Sleep Mode$		7.2		mA
$I_{cc}$	Quiescent supply current on PVDD	$\overline{PDN}=2V, V_{PVDD}=13.5V, Deep Sleep Mode$		120		$\mu A$
$I_{cc}$	Quiescent supply current on PVDD	$\overline{PDN}=0V, V_{PVDD}=13.5V, Shutdown Mode$		7.2		$\mu A$
$t_{off}$	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SP_K\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD. Measured at 0 dB input(1FS)	4.95		29.5	V
$\Delta A_{V(SP_K\_AMP)}$	Amplifier gain error	Gain = 29.5 Vp/FS		0.5		dB
$f_{SP_K\_AMP}$	Switching frequency of the speaker amplifier			384		kHz
				768		kHz

### Electrical Characteristics (continued)

Free-air room temperature 25°C ,DVDD=3.3V,1SPW mode with LC filter, BD mode with Ferrite bead filter (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>DS(on)</sub>	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization		180		mΩ
OCE <sub>THRES</sub>	Over-Current Error Threshold	OUTxx Overcurrent Error Threshold		5		A
OVE <sub>THRES(PVDD)</sub>	PVDD over voltage error threshold			28		V
UVE <sub>THRES(PVDD)</sub>	PVDD under voltage error threshold			4.2		V
OTE <sub>THRES</sub>	Over temperature error threshold			160		°C
OTE <sub>Hysteresis</sub>	Over temperature error hysteresis			10		°C
OTW <sub>THRES</sub>	Over temperature warning level	Read by register 0x73 bit3		135		°C
<b>SPEAKER AMPLIFIER (STEREO BTL)</b>						
V <sub>OS</sub>	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 Vp gain, V <sub>PVDD</sub> = 12 V, BD Mode	-6.5		6.5	mV
P <sub>O(SPK)</sub>	Continuous Output power (per channel)	V <sub>PVDD</sub> = 21V, R <sub>SPK</sub> = 8 Ω, f = 1 kHz, THD+N = 1%, 1SPW Mode		23		W
		V <sub>PVDD</sub> = 21 V, R <sub>SPK</sub> = 8 Ω, f = 1 kHz, THD+N = 10%, 1SPW Mode		27.5		W
		V <sub>PVDD</sub> = 18 V, R <sub>SPK</sub> = 6 Ω, f = 1 kHz, THD+N = 1%, BD Mode		21		W
		V <sub>PVDD</sub> = 18 V, R <sub>SPK</sub> = 6 Ω, f = 1 kHz, THD+N = 10%, BD Mode		25		W
		V <sub>PVDD</sub> = 12 V, R <sub>SPK</sub> = 6 Ω, f = 1 kHz THD+N = 1%, BD Mode		9.9		W
		V <sub>PVDD</sub> = 12 V, R <sub>SPK</sub> = 6 Ω, f = 1 kHz THD+N = 10%, BD Mode		12		W
		V <sub>PVDD</sub> = 13.5 V, R <sub>SPK</sub> = 6 Ω, f = 1 kHz THD+N = 1%, BD Mode		12		W
		V <sub>PVDD</sub> = 13.5 V, R <sub>SPK</sub> = 6 Ω, f = 1 kHz THD+N = 10%, BD Mode		15		W
THD+N <sub>SPK</sub>	Total harmonic distortion and noise (P <sub>O</sub> = 1 W, f = 1 KHz, R <sub>SPK</sub> = 6 Ω)	V <sub>PVDD</sub> = 12 V, Fsw=768kHz, LC-filter, BD Mode		0.03%		
		V <sub>PVDD</sub> = 18 V, Fsw=768kHz, LC-filter, BD Mode		0.03%		
I <sub>CN(SPK)</sub>	Idle channel noise(A-weighted)	V <sub>PVDD</sub> = 12 V, Fsw=768kHz, LC-filter, Load=6 Ω		37		μVrms
		V <sub>PVDD</sub> = 18 V, Fsw=768kHz, LC-filter, Load=6 Ω		38		
DR	Dynamic range	A-Weighted, -60 dBFS method. V <sub>PVDD</sub> = 24 V, SPK_GAIN = 29.5 Vp/FS		106		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N output level, V <sub>PVDD</sub> =24V		111		dB
		A-Weighted, referenced to 1% THD+N output level, V <sub>PVDD</sub> =13.5V		107.5		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 V <sub>rms</sub> , V <sub>PVDD</sub> = 12 V, input audio signal = digital zero		72		dB
X-talk <sub>SPK</sub>	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 kHz		100		dB
<b>SPEAKER AMPLIFIER (MONO PBTL)</b>						
V <sub>OS</sub>	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.5 Vp gain, V <sub>PVDD</sub> = 12 V, BD Mode	-8		8	mV



## Electrical Characteristics (continued)

Free-air room temperature 25°C ,DVDD=3.3V,1SPW mode with LC filter, BD mode with Ferrite bead filter (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>O(SPK)</sub>	Continuous Output Power	V <sub>PVDD</sub> = 12 V, R <sub>SPK</sub> = 4 Ω, f = 1kHz, THD+N = 1%, BD Mode		15.4		W
		V <sub>PVDD</sub> = 12 V, R <sub>SPK</sub> = 4 Ω, f = 1kHz, THD+N = 10%, BD Mode		18.5		W
		V <sub>PVDD</sub> = 18V, R <sub>SPK</sub> = 4 Ω, f = 1kHz, THD+N = 1%, BD Mode		33.6		W
		V <sub>PVDD</sub> = 18 V, R <sub>SPK</sub> = 4 Ω, f = 1kHz, THD+N = 10%, BD Mode		41		W
THD+N <sub>SPK</sub>	Total harmonic distortion and noise (P <sub>O</sub> = 1 W, f = 1 kHz)	V <sub>PVDD</sub> = 12 V, 4.7uH + 0.68uF filter, R <sub>SPK</sub> = 4 Ω, BD Mode		0.06%		
		V <sub>PVDD</sub> = 24 V, 4.7uH + 0.68uF filter, R <sub>SPK</sub> = 4 Ω, 1SPW Mode		0.07%		
DR	Dynamic range	A-Weighted, -60 dBFS method, V <sub>PVDD</sub> = 24V, SPK_GAIN = 29.5 Vp/FS		106		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N output level, V <sub>PVDD</sub> =13.5V		107.7		dB
		A-Weighted, referenced to 1% THD+N output level, V <sub>PVDD</sub> =24V		111		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 V <sub>rms</sub> , V <sub>PVDD</sub> = 19 V, input audio signal = digital zero		72		dB

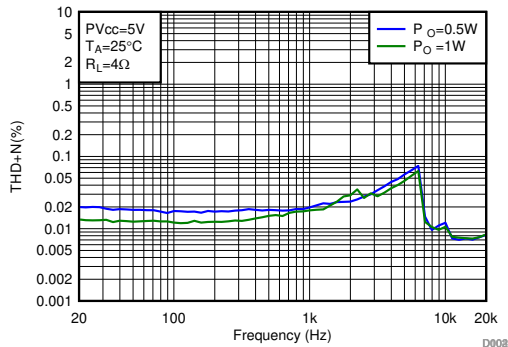
## 8.6 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>Serial Audio Port Timing</b>					
$f_{\text{SCLK}}$	SCLK frequency	1.024			MHz
$t_{\text{SCLK}}$	SCLK period	40			ns
$t_{\text{SCLKL}}$	SCLK pulse width, low	16			ns
$t_{\text{SCLKH}}$	SCLK pulse width, high	16			ns
$t_{\text{SL}}$	SCLK rising to LRCK/FS edge	8			ns
$t_{\text{LS}}$	LRCK/FS Edge to SCLK rising edge	8			ns
$t_{\text{SU}}$	Data setup time, before SCLK rising edge	8			ns
$t_{\text{DH}}$	Data hold time, after SCLK rising edge	8			ns
$t_{\text{DFS}}$	Data delay time from SCLK falling edge			15	ns
<b>I<sup>2</sup>C Bus Timing – Standard</b>					
$f_{\text{SCL}}$	SCL clock frequency			100	kHz
$t_{\text{BUF}}$	Bus free time between a STOP and START condition	4.7			$\mu\text{s}$
$t_{\text{LOW}}$	Low period of the SCL clock	4.7			$\mu\text{s}$
$t_{\text{HI}}$	High period of the SCL clock	4			$\mu\text{s}$
$t_{\text{RS-SU}}$	Setup time for (repeated) START condition	4.7			$\mu\text{s}$
$t_{\text{S-HD}}$	Hold time for (repeated) START condition	4			$\mu\text{s}$
$t_{\text{D-SU}}$	Data setup time	250			ns
$t_{\text{D-HD}}$	Data hold time	0		900	ns
$t_{\text{SCL-R}}$	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
$t_{\text{SCL-R1}}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
$t_{\text{SCL-F}}$	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
$t_{\text{SDA-R}}$	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
$t_{\text{SDA-F}}$	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
$t_{\text{P-SU}}$	Setup time for STOP condition	4			$\mu\text{s}$
<b>I<sup>2</sup>C Bus Timing – Fast</b>					
$f_{\text{SCL}}$	SCL clock frequency			400	kHz
$t_{\text{BUF}}$	Bus free time between a STOP and START condition	1.3			$\mu\text{s}$
$t_{\text{LOW}}$	Low period of the SCL clock	1.3			$\mu\text{s}$
$t_{\text{HI}}$	High period of the SCL clock	600			ns
$t_{\text{RS-SU}}$	Setup time for (repeated)START condition	600			ns
$t_{\text{RS-HD}}$	Hold time for (repeated)START condition	600			ns
$t_{\text{D-SU}}$	Data setup time	100			ns
$t_{\text{D-HD}}$	Data hold time	0		900	ns
$t_{\text{SCL-R}}$	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
$t_{\text{SCL-R1}}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
$t_{\text{SCL-F}}$	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
$t_{\text{SDA-R}}$	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
$t_{\text{SDA-F}}$	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
$t_{\text{P-SU}}$	Setup time for STOP condition	600			ns
$t_{\text{SP}}$	Pulse width of spike suppressed			50	ns

## 8.7 Typical Characteristics

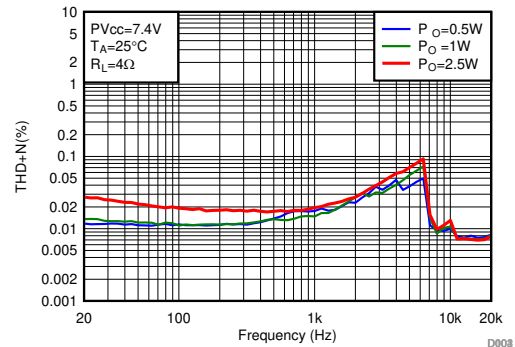
### 8.7.1 Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5806MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM Modulation mode set to 1 SPW mode with Class D Bandwidth = 120 kHz for 576 kHz F<sub>sw</sub> and Class D Bandwidth = 175 kHz for 768 kHz F<sub>sw</sub> (Listed in Register 0x53) unless otherwise noted.



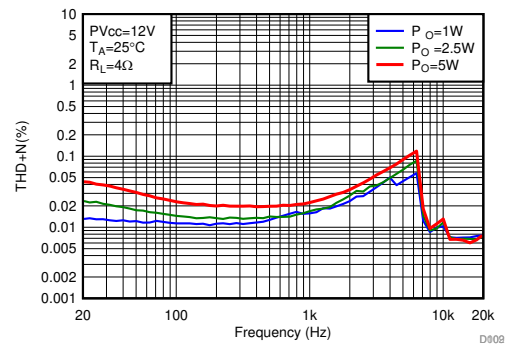
PVDD = 5 V      4.7μH+0.68μF  
F<sub>SW</sub> = 576 kHz      1SPW Modulation      Load=4Ω

图 1. THD+N vs Frequency-BTL



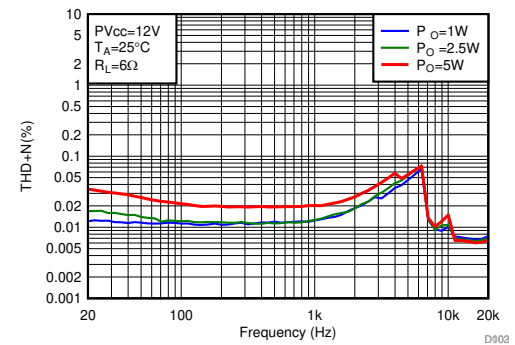
PVDD = 7.4 V      4.7 μH + 0.68 μF  
F<sub>SW</sub> = 576 kHz      1 SPW Modulation      Load = 4 Ω

图 2. THD+N vs Frequency-BTL



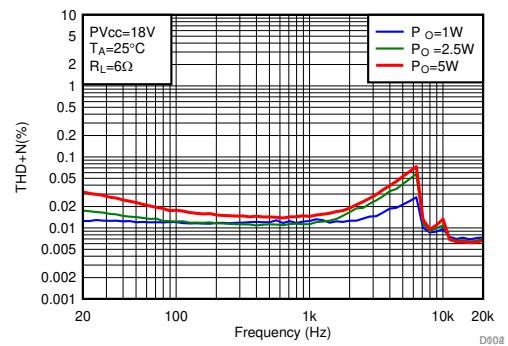
PVDD = 12 V      4.7 μH + 0.68 μF  
F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load= 4 Ω

图 3. THD+N vs Frequency-BTL



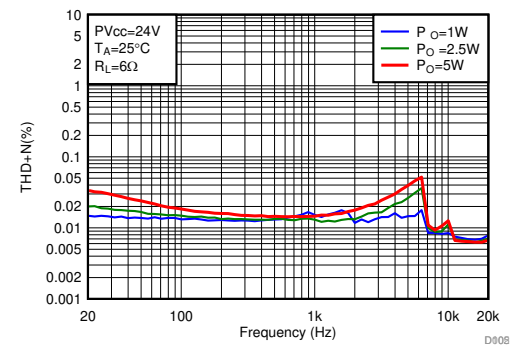
PVDD = 12 V      4.7 μH + 0.68 μF  
F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 6 Ω

图 4. THD+N vs Frequency-BTL



PVDD = 18 V      10 μH + 0.68 μF  
F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 6 Ω

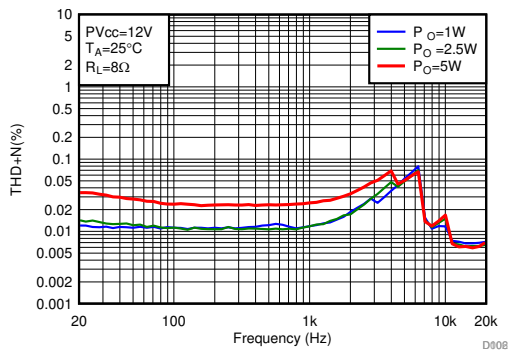
图 5. THD+N vs Frequency-BTL



PVDD = 24 V      10 μH + 0.68 μF  
F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 6 Ω

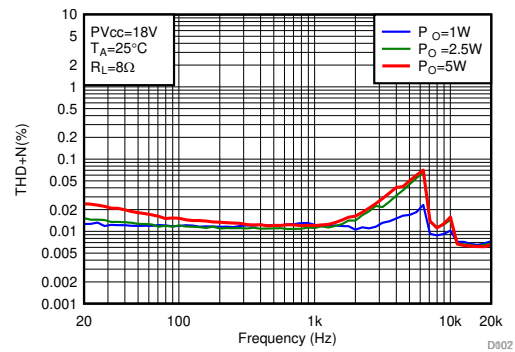
图 6. THD+N vs Frequency-BTL

### Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (continued)



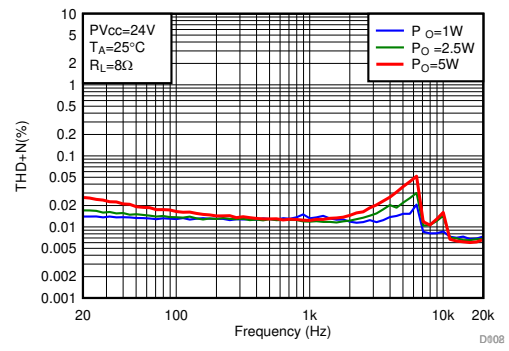
PVDD = 12 V    4.7  $\mu$ H + 0.68  $\mu$ F  
 $F_{SW}$  = 768 kHz    1 SPW Modulation    Load = 8  $\Omega$

Fig. 7. THD+N vs Frequency-BTL



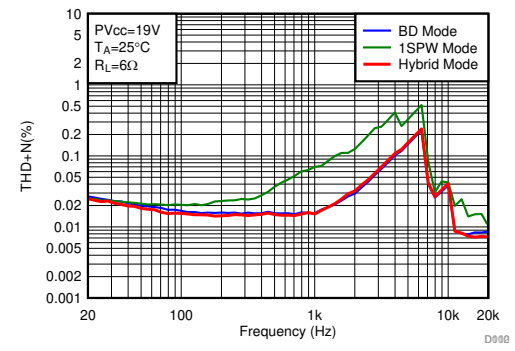
PVDD = 18 V    10  $\mu$ H + 0.68  $\mu$ F  
 $F_{SW}$  = 768 kHz    1 SPW Modulation    Load = 8  $\Omega$

Fig. 8. THD+N vs Frequency-BTL



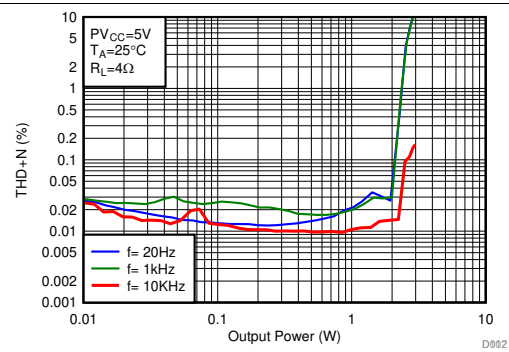
PVDD = 24 V    10  $\mu$ H + 0.68  $\mu$ F  
 $F_{SW}$  = 768 kHz    1 SPW Modulation    Load = 8  $\Omega$

Fig. 9. THD+N vs Frequency-BTL



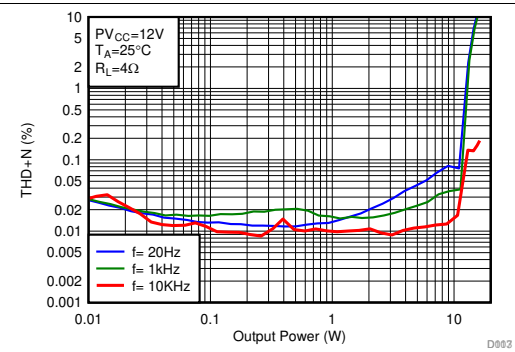
PVDD = 19 V    10  $\mu$ H + 0.68  $\mu$ F     $P_O$  = 5 W  
 $F_{SW}$  = 384 kHz    Hybrid/BD, 1 SPW Modulation    Load = 6  $\Omega$

Fig. 10. THD+N vs Frequency-BTL



PVDD = 5 V    4.7  $\mu$ H + 0.68  $\mu$ F  
 $F_{SW}$  = 768 kHz    1 SPW Modulation    Load = 4  $\Omega$

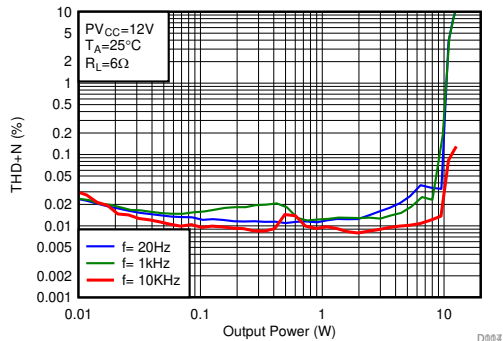
Fig. 11. THD+N vs Output Power-BTL



PVDD = 12 V    4.7  $\mu$ H + 0.68  $\mu$ F  
 $F_{SW}$  = 768 kHz    1 SPW Modulation    Load = 4  $\Omega$

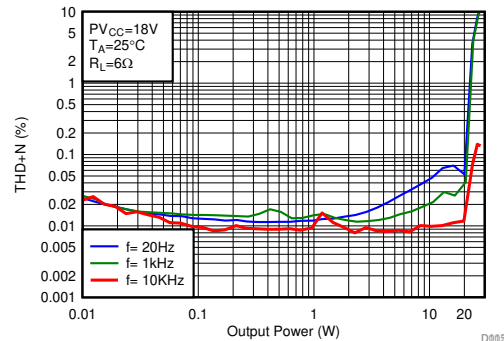
Fig. 12. THD+N vs Output Power-BTL

Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (continued)



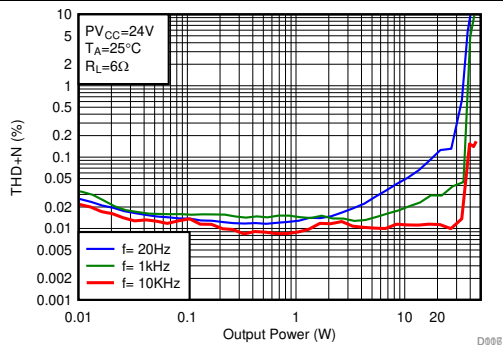
PVDD = 12 V    4.7  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 768 kHz    1 SPW Modulation    Load = 6  $\Omega$

图 13. THD+N vs Output Power-BTL



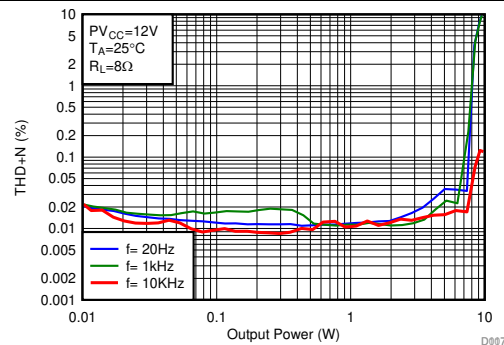
PVDD = 18 V    10  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 768 kHz    1 SPW Modulation    Load = 6  $\Omega$

图 14. THD+N vs Output Power-BTL



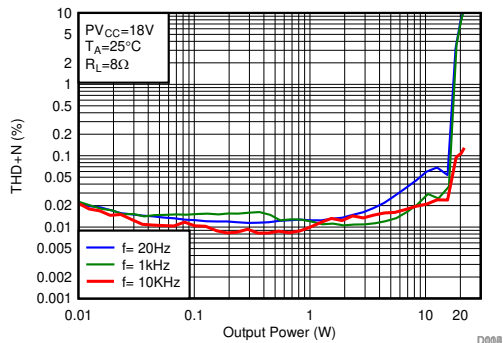
PVDD = 24 V    10  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 768 kHz    1 SPW Modulation    Load = 6  $\Omega$

图 15. THD+N vs Output Power-BTL



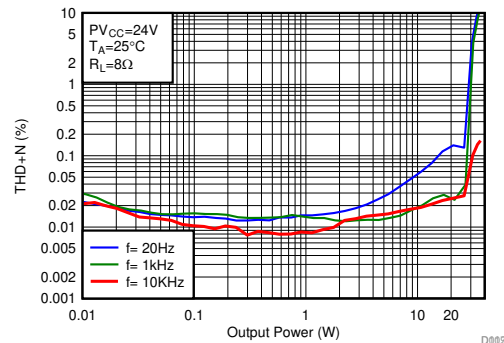
PVDD = 12 V    10  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 768 kHz    1 SPW Modulation    Load = 8  $\Omega$

图 16. THD+N vs Output Power-BTL



PVDD = 18 V    10  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 768 kHz    1 SPW Modulation    Load = 8  $\Omega$

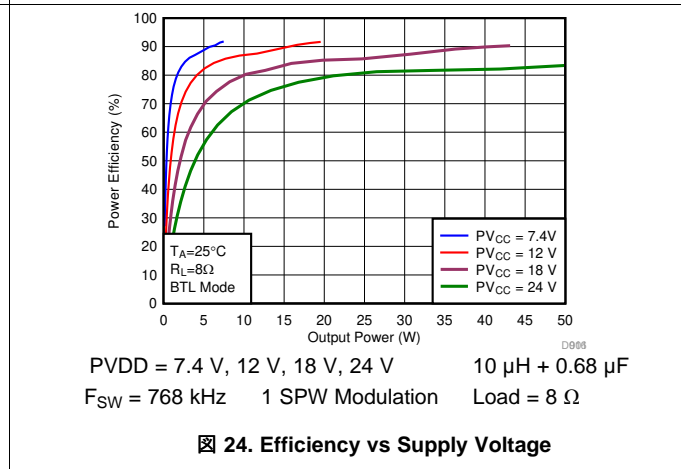
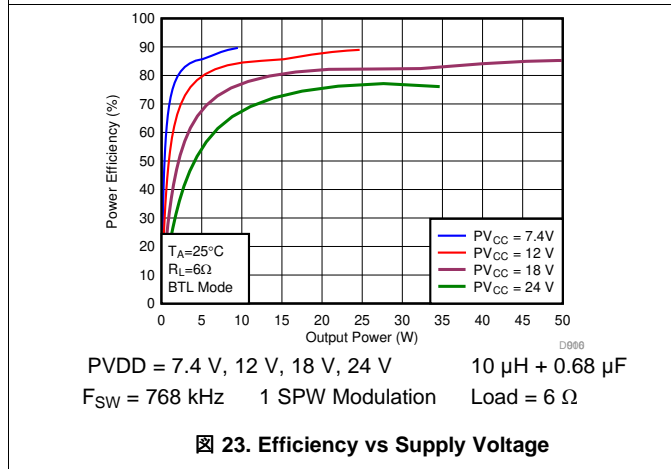
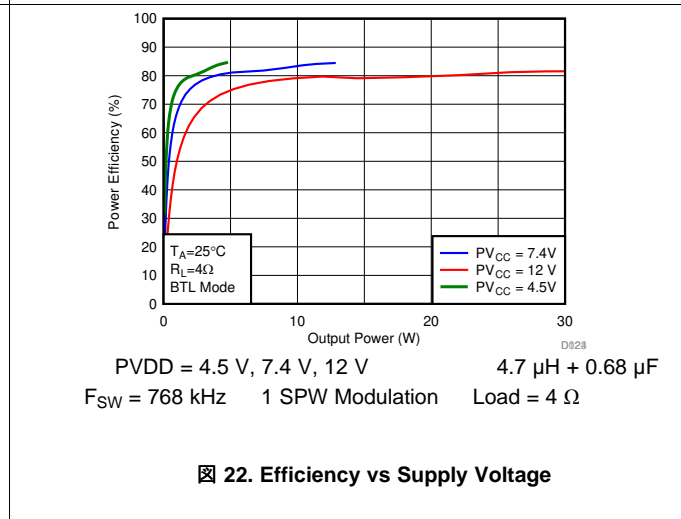
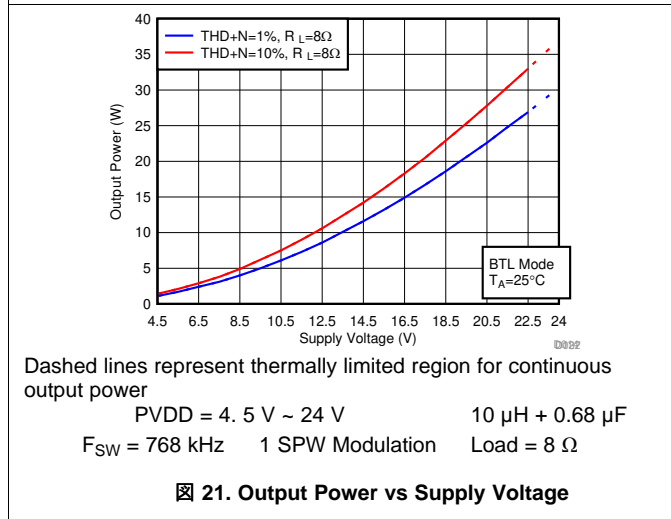
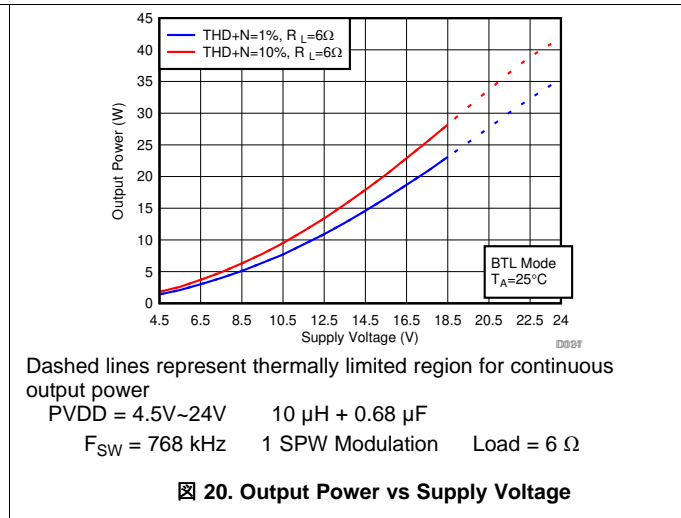
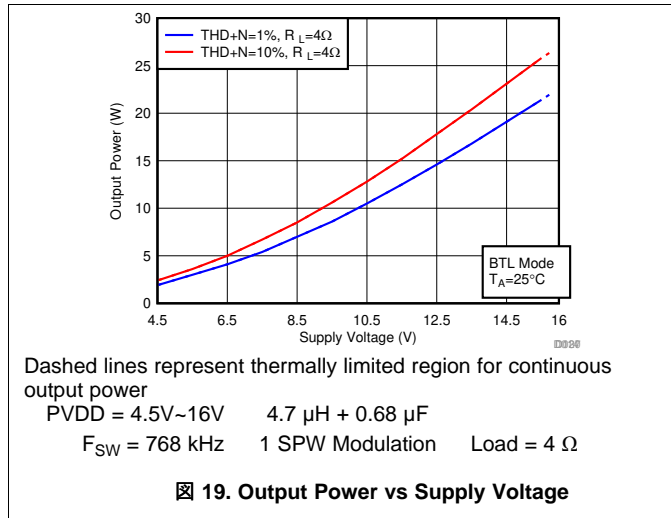
图 17. THD+N vs Output Power-BTL



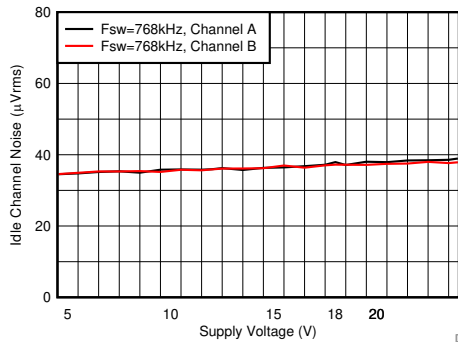
PVDD = 24 V    10  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 768 kHz    1 SPW Modulation    Load = 8  $\Omega$

图 18. THD+N vs Output Power-BTL

### Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (continued)

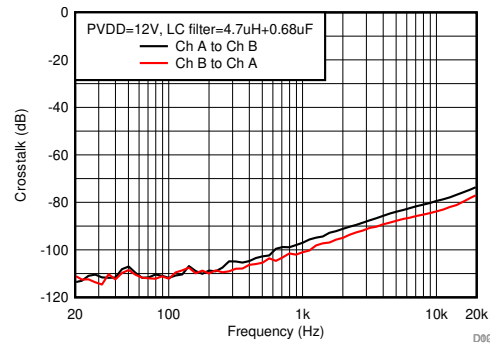


Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (continued)



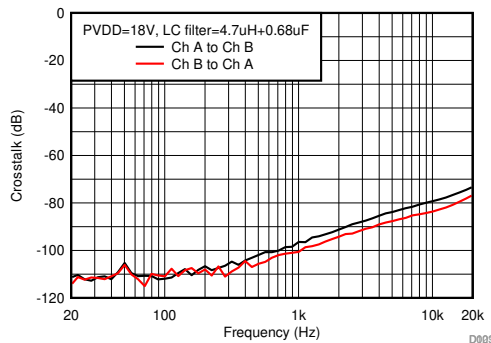
PVDD = 7.4 V ~ 24 V      10 µH + 0.68 µF  
 F<sub>SW</sub> = 768 kHz      1SPW Modulation      Load = 8 Ω

图 25. Idle Channel Noise vs Supply Voltage



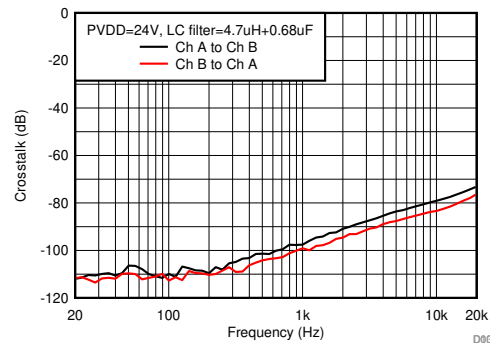
PVDD = 12 V      4.7 µH + 0.68 µF      P<sub>O</sub> = 1 W  
 F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 6 Ω

图 26. Crosstalk



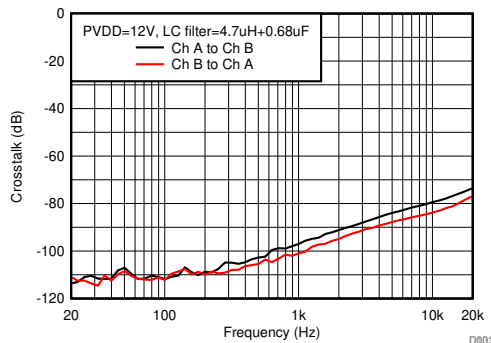
PVDD = 18 V      4.7 µH + 0.68 µF      P<sub>O</sub> = 1 W  
 F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 6 Ω

图 27. Crosstalk



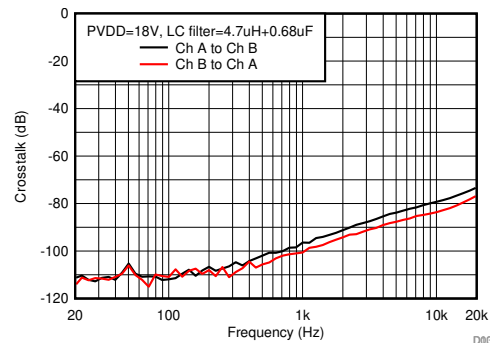
PVDD = 24 V      4.7 µH + 0.68 µF      P<sub>O</sub> = 1 W  
 F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 6 Ω

图 28. Crosstalk



PVDD = 12 V      4.7 µH + 0.68 µF      P<sub>O</sub> = 1 W  
 F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 8 Ω

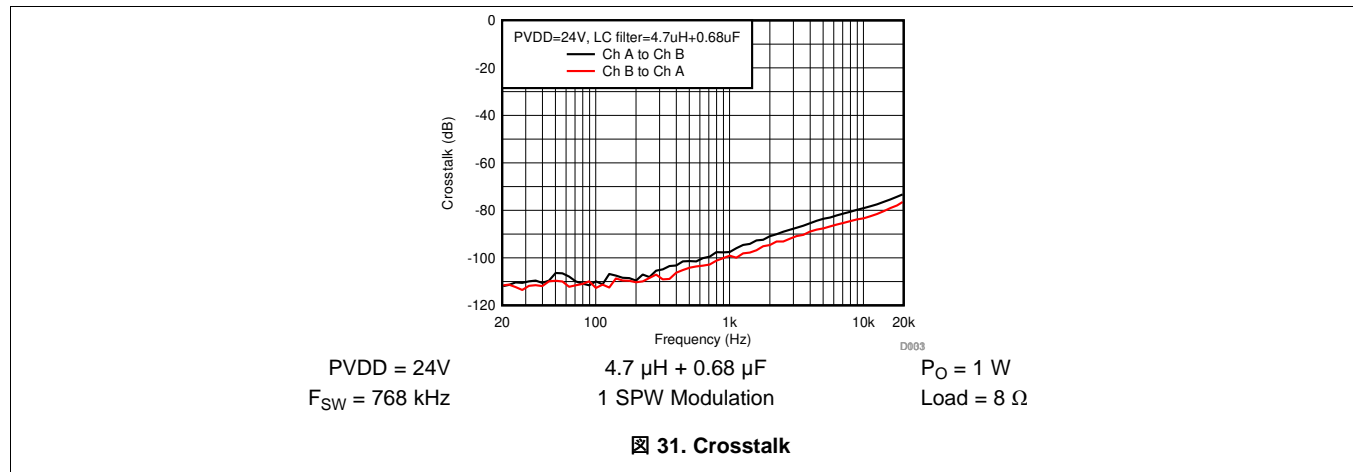
图 29. Crosstalk



PVDD = 18 V      4.7 µH + 0.68 µF      P<sub>O</sub> = 1 W  
 F<sub>SW</sub> = 768 kHz      1 SPW Modulation      Load = 8 Ω

图 30. Crosstalk

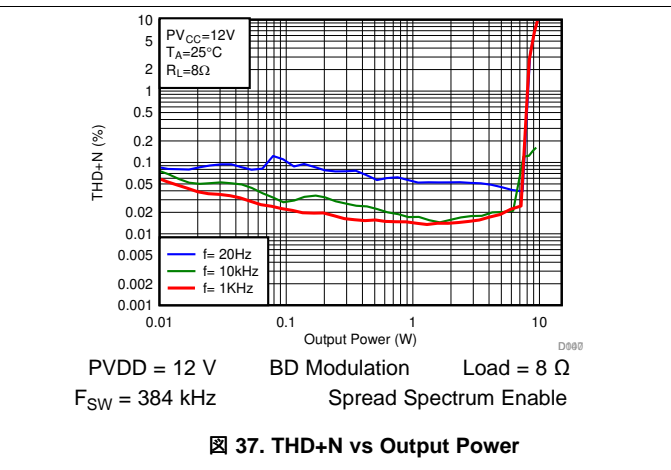
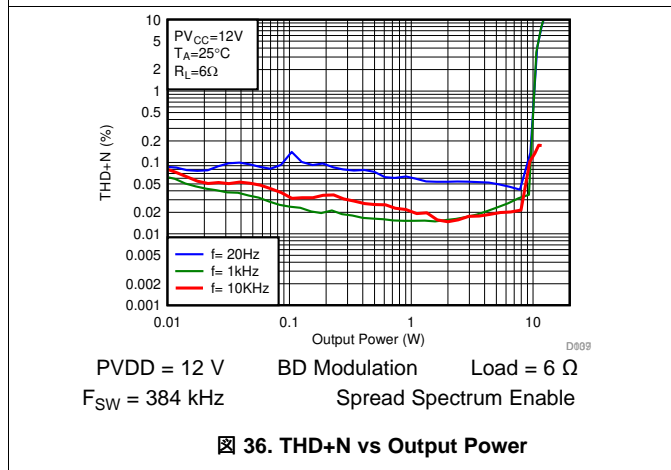
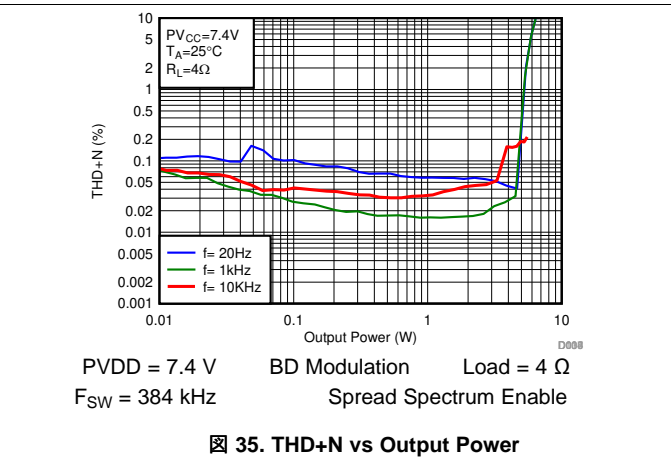
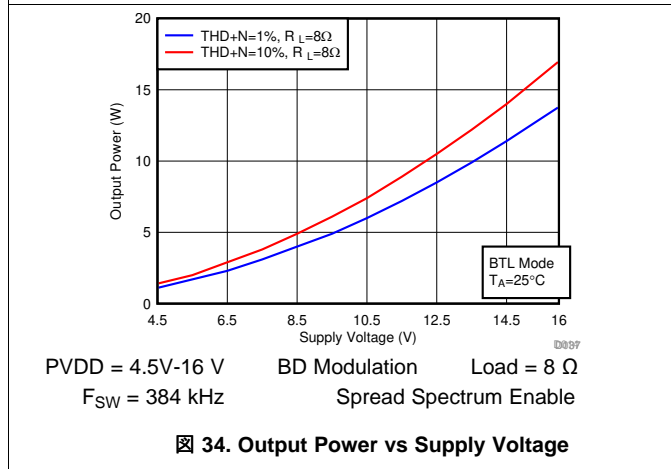
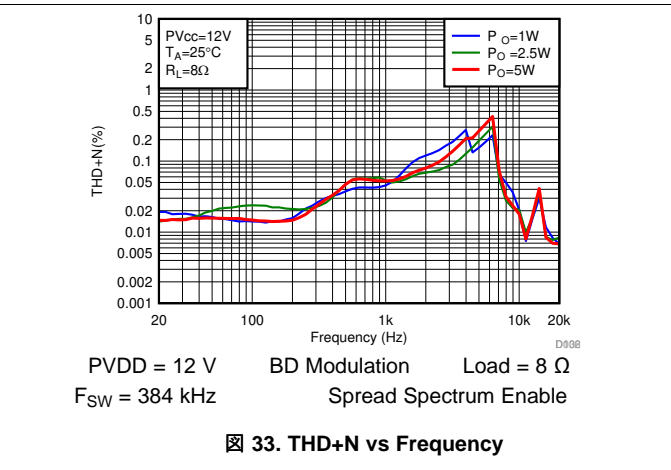
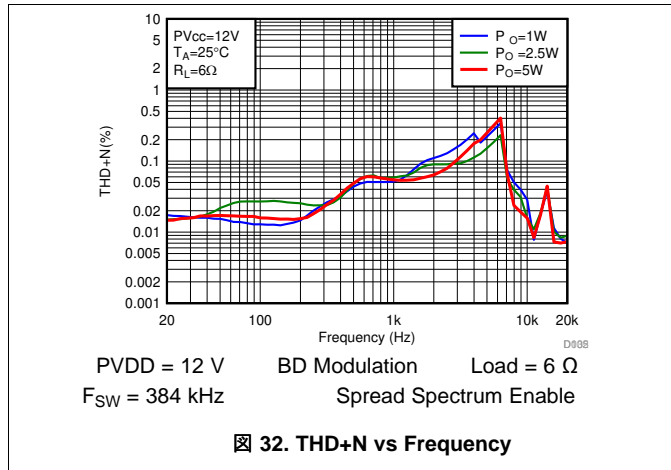
**Bridge Tied Load (BTL) Configuration Curves with 1 SPW Mode (continued)**



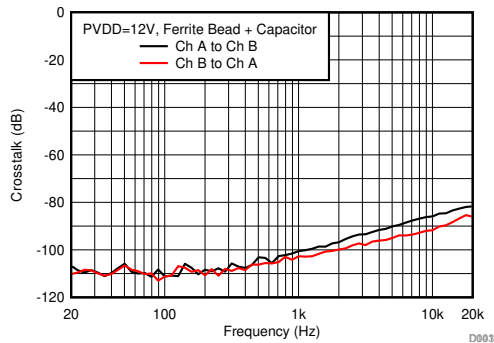


### 8.7.2 Bridge Tied Load (BTL) Configuration Curves

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS806MDEV board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, with Class D Bandwidth = 80 kHz (Listed in Register 0x53), Spread Spectrum Enable, Ferrite bead + Capacitor as the output filter, BD Modulation, unless otherwise noted.

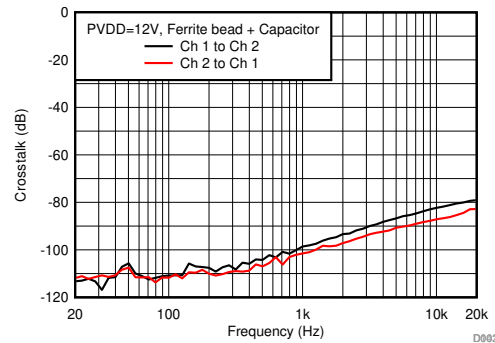


Bridge Tied Load (BTL) Configuration Curves (continued)



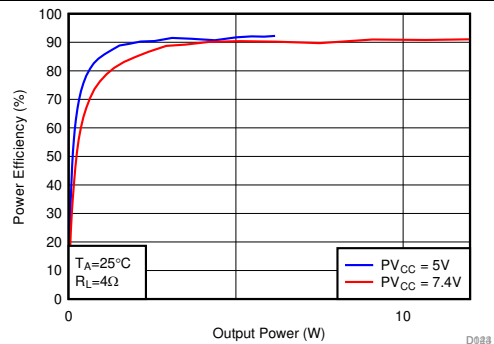
PVDD = 12 V BD Modulation Load = 6 Ω  
 F<sub>SW</sub> = 384 kHz Spread Spectrum Enable P<sub>O</sub> = 1 W

38. Crosstalk



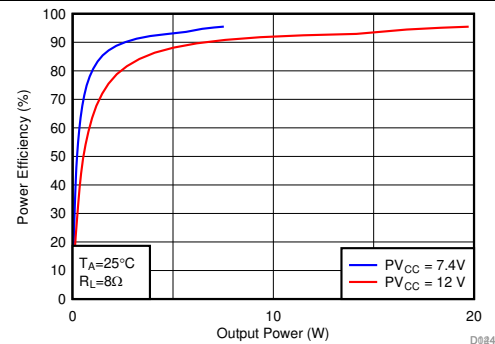
PVDD = 12 V BD Modulation Load = 8 Ω  
 F<sub>SW</sub> = 384 kHz Spread Spectrum Enable P<sub>O</sub> = 1 W

39. Crosstalk



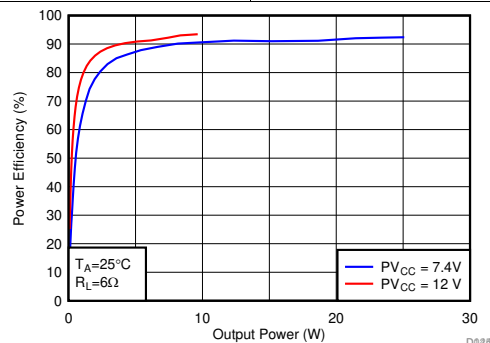
PVDD = 5V/7.4V BD Modulation Load = 4 Ω  
 F<sub>SW</sub> = 384 kHz Spread Spectrum Enable

40. Efficiency vs Output Power



PVDD = 7.4 V, 12 V BD Modulation Load = 8 Ω  
 F<sub>SW</sub> = 384 kHz Spread Spectrum Enable

41. Efficiency vs Output Power



PVDD = 7.4 V, 12 V BD Modulation Load = 6 Ω  
 F<sub>SW</sub> = 384 kHz Spread Spectrum Enable

42. Efficiency vs Output Power

### 8.7.3 Parallel Bridge Tied Load (PBTB) Configuration

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5806MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 576 kHz, the LC filter used was 4.7 μH / 0.68 μF, 1SPW modulation with Class D Bandwidth = 120 kHz (Listed in Register 0x53) unless otherwise noted.

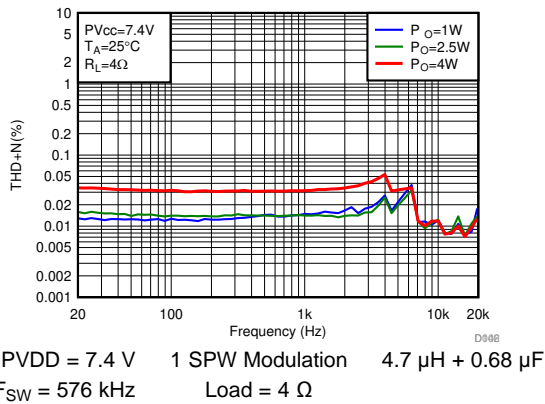


Figure 43. THD+N vs Frequency

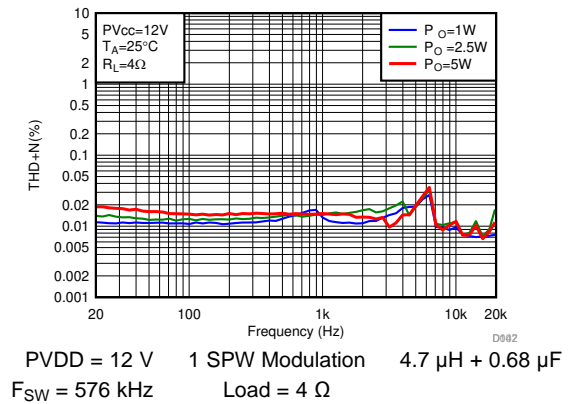


Figure 44. THD+N vs Frequency

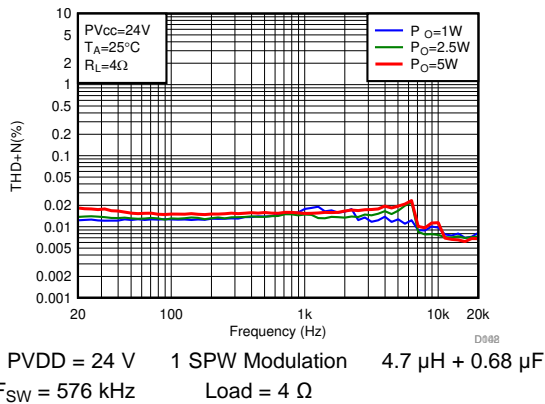


Figure 45. THD+N vs Frequency

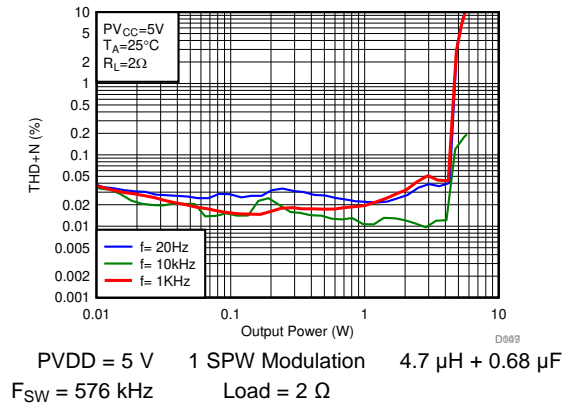


Figure 46. THD+N vs Output Power

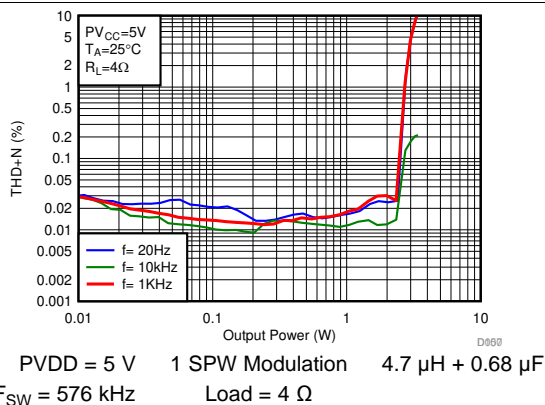


Figure 47. THD+N vs Output Power

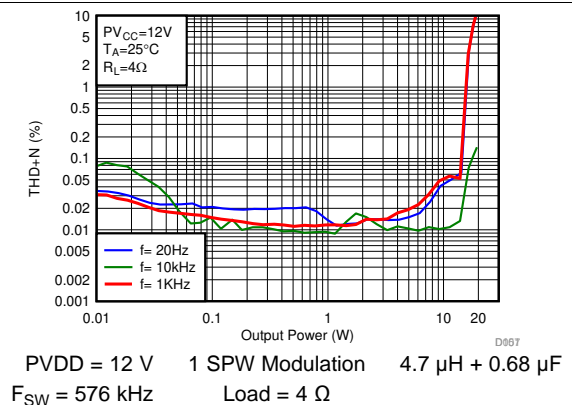
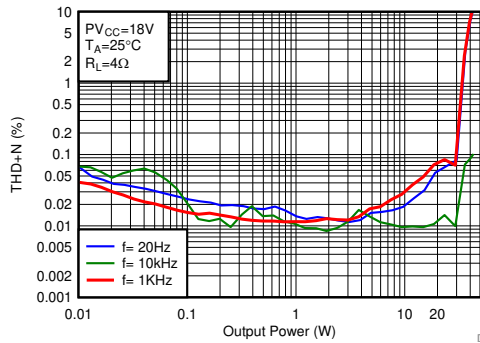


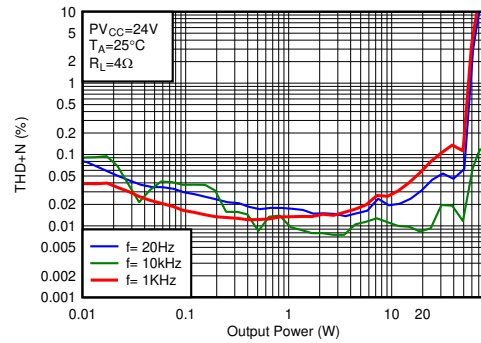
Figure 48. THD+N vs Output Power

Parallel Bridge Tied Load (PBTL) Configuration (continued)



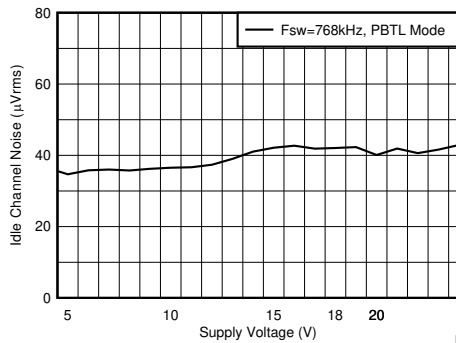
PVDD = 18 V 1 SPW Modulation 4.7  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 576 kHz Load = 4  $\Omega$

图 49. THD+N vs Output Power



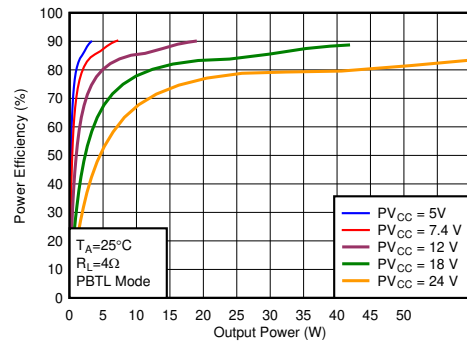
PVDD = 24 V 1 SPW Modulation 4.7  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 576 kHz Load = 4  $\Omega$

图 50. THD+N vs Output Power



PVDD = 4.5–24V 1 SPW Modulation 4.7  $\mu$ H + 0.68  $\mu$ F  
 F<sub>SW</sub> = 576 kHz Load = 4  $\Omega$

图 51. Idle Channel Noise vs Supply Voltage



PVDD = 5 V, 7.4 V, 12 V, 18 V, 24 V 1 SPW Modulation  
 F<sub>SW</sub> = 576 kHz Load = 4  $\Omega$  4.7  $\mu$ H + 0.68  $\mu$ F

图 52. Efficiency vs Output Power

## 9 Parametric Measurement Information

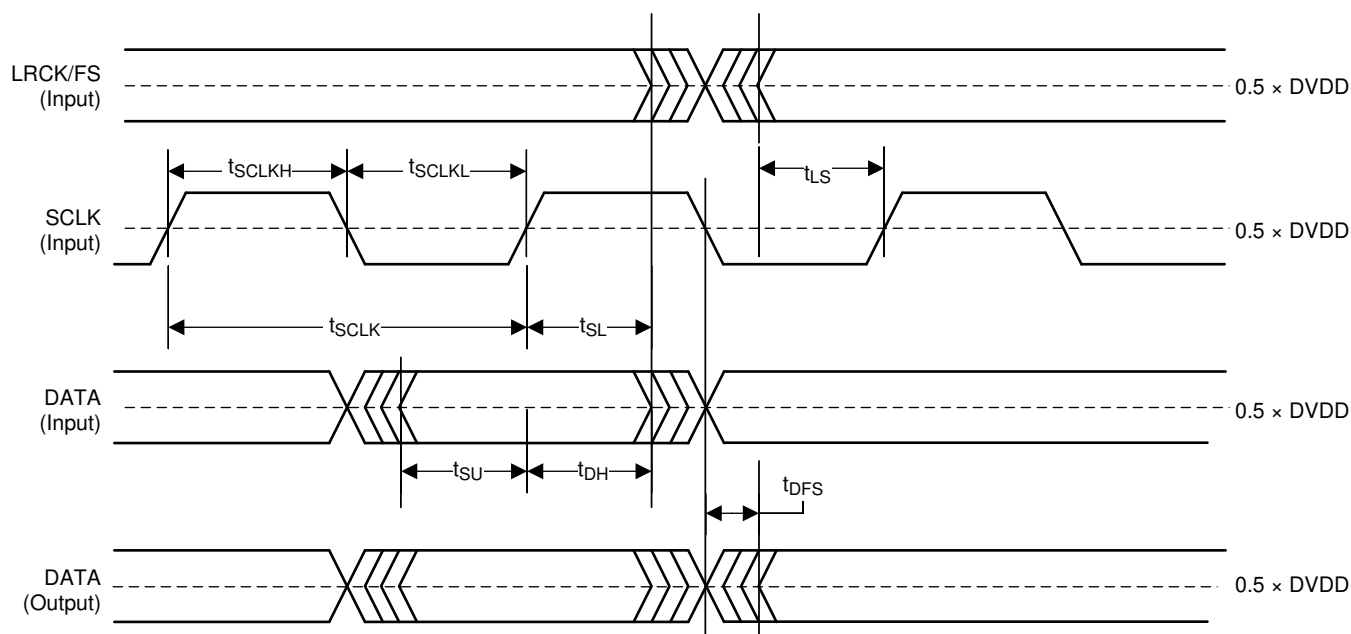


图 53. Serial Audio Port Timing in Slave Mode

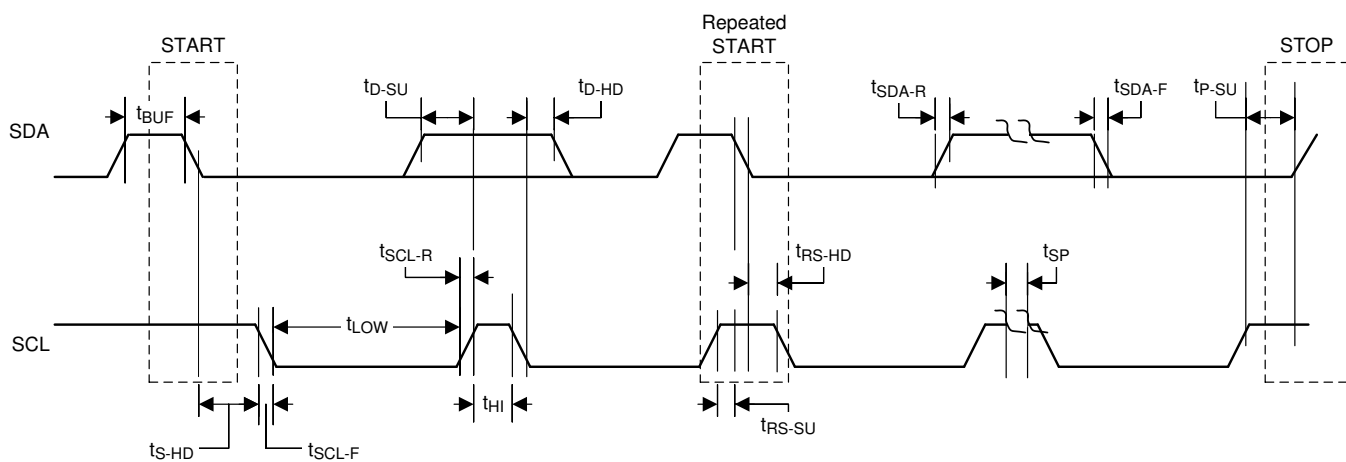


图 54. I<sup>2</sup>C Communication Port Timing Diagram

## 10 Detailed Description

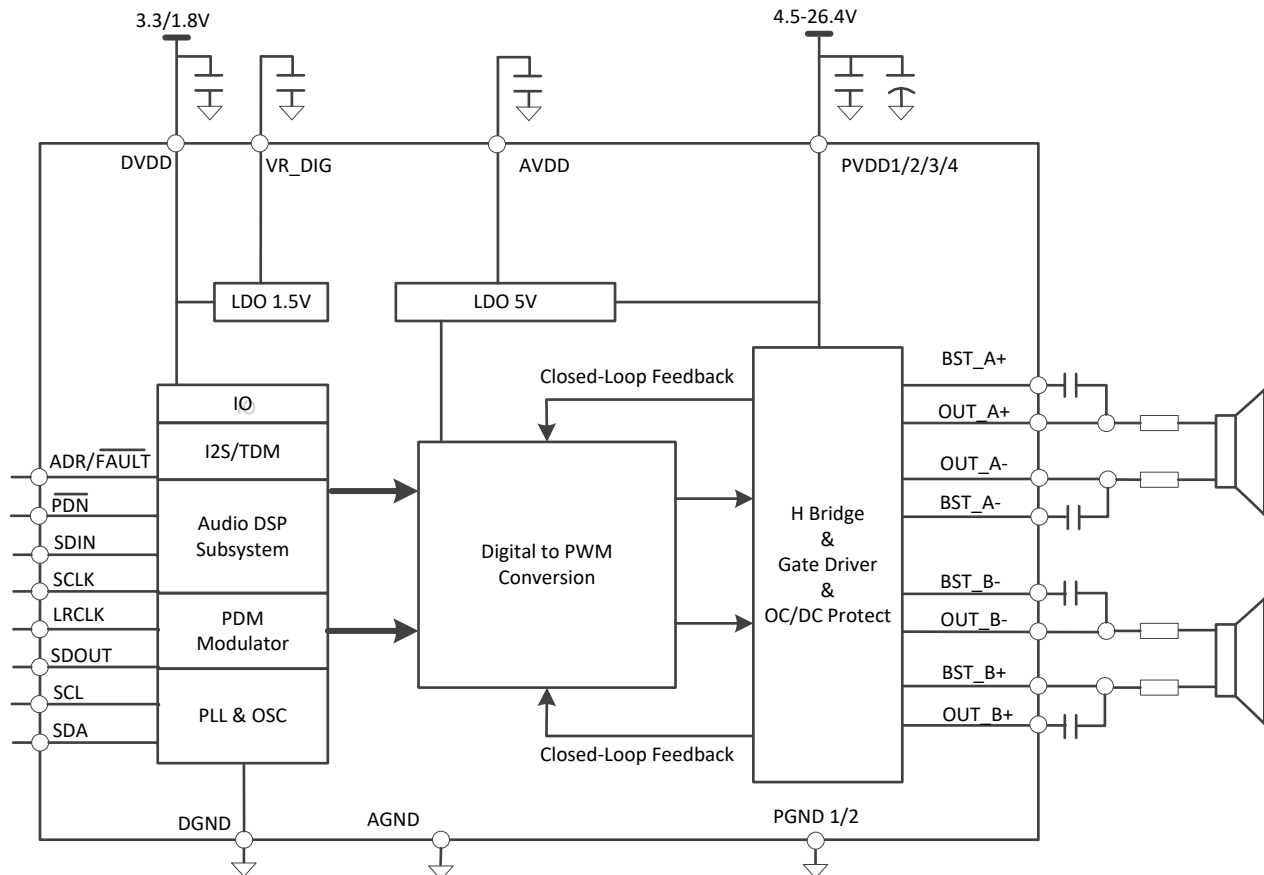
### 10.1 Overview

The TAS5806M device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. These 4 main building blocks are listed as follows:

1. A stereo audio DAC.
2. An Audio DSP subsystem.
3. A flexible close-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
4. An I<sup>2</sup>C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, PVDD, is required to provide power to the output stage of the audio amplifier. One internal LDO converts PVDD to 5 V for internal GVDD and AVDD, another LDO converts DVDD to 1.5V for internal digital core.

### 10.2 Functional Block Diagram



## 10.3 Feature Description

### 10.3.1 Power Supplies

To facilitate system design, TAS5806M needs only a 3.3-V or 1.8-V supply in addition to the (typical) 12 V or 24 V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST\_x). The gate drive voltages (AVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST\_x) to the power-stage output pin (OUT\_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (AVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

### 10.3.2 Device Clocking

The TAS5806M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

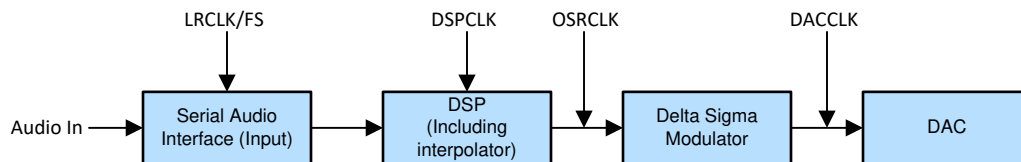


Fig 55. Audio Flow with Respective Clocks

Fig 55 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left/Right Word Clock and Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The TAS5806M device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32 kHz, 44.1kHz – 48 kHz, 88.2 kHz – 96 kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

### 10.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5806M device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Feature Description (continued)

表 1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (fs)
I <sup>2</sup> S/LJ/RJ	32, 24, 20, 16	32 to 96	64, 32
TDM	32, 24, 20, 16	32	128
		44.1,48	128,256,512
		96	128,256

Before DSP register initialize with I<sup>2</sup>C during the startup , TAS5806M requires stable I<sup>2</sup>S ready. When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

10.3.4 Clock Halt Auto-recovery

As some of host processor will Halt the I<sup>2</sup>S clock when there is no audio playing. When Clock halt, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). After audio clocks recovery, the device automatically returns to the previous state.

10.3.5 Sample Rate on the Fly Change

TAS5806M supports LRCLK(FS) rate on the fly change. For example, change LCRLK from 32kHz to 48kHz or 96kHz, Host processor needs to put the LRCLK(FS)/SCLK to Halt state at least 100us before changing to the new sample rate.

10.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (P0-R51-D[5:4]). If the high width of LRCK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (P0-R51-D[3:2]) should set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in 表 1. The data formats are detailed in 图 56 through 图 60. The word length are selected via Register (P0-R51-D[1:0]). The offsets of data are selected via Register (P0-R51-D[7]) and Register (P0-R52-D[7:0]). Default setting is I2S and 24 bit word length.

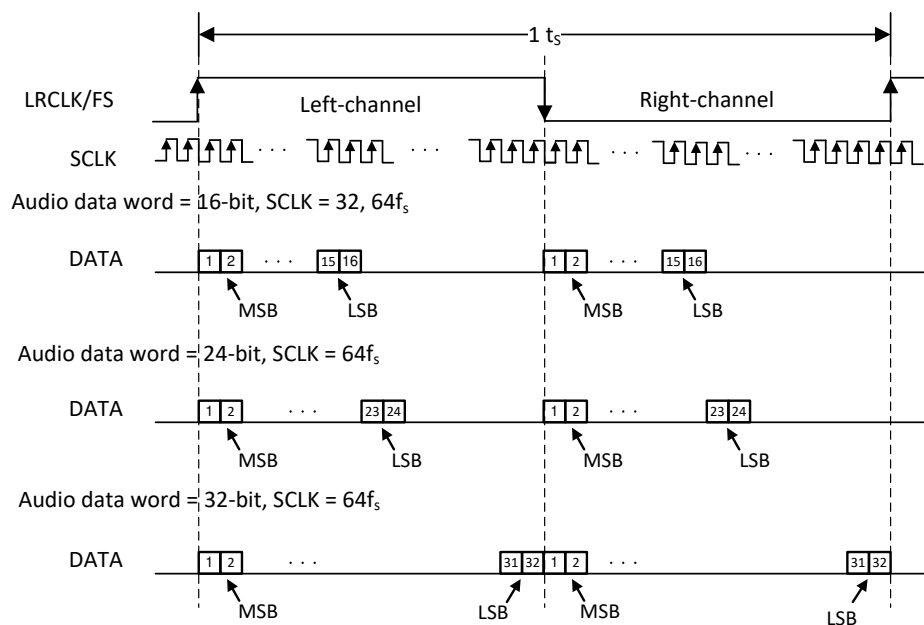
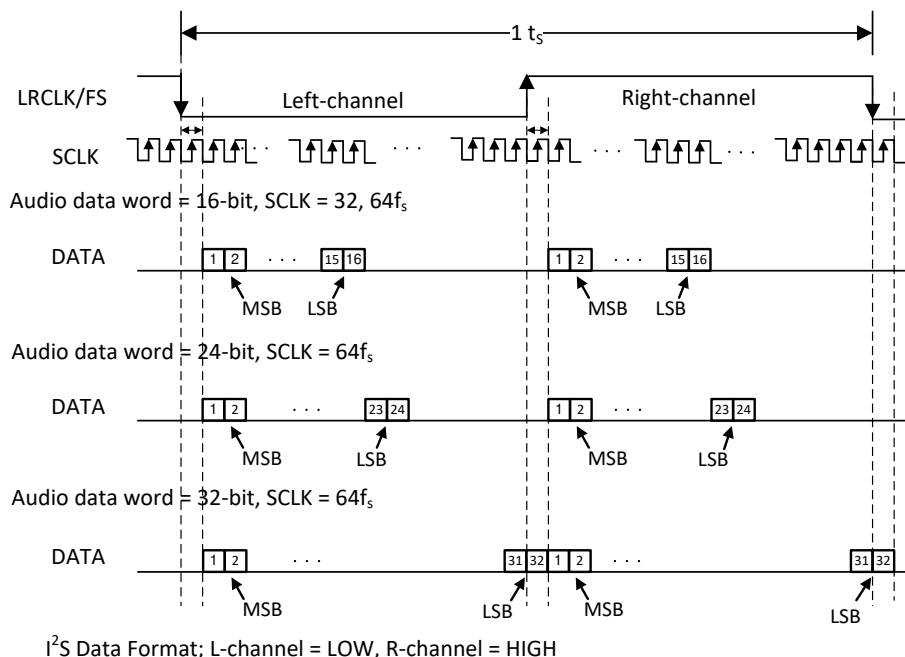


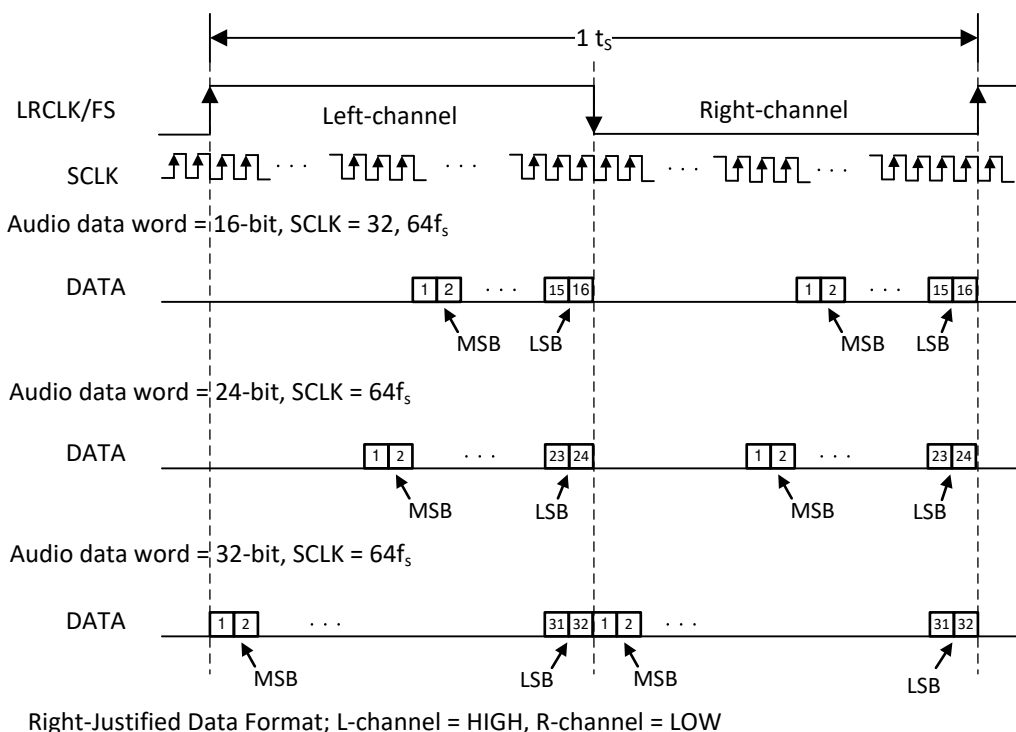
图 56. Left Justified Audio Data Format





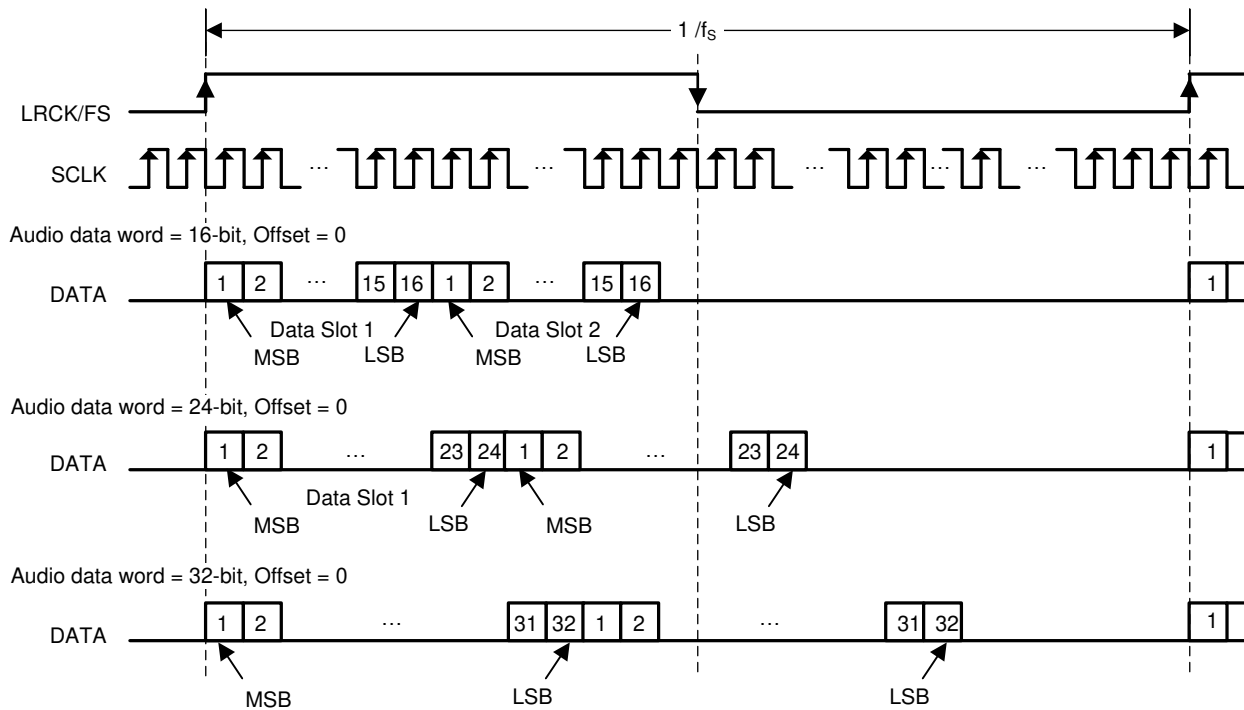
I<sup>2</sup>S Data Format; L-channel = LOW, R-channel = HIGH

图 57. I<sup>2</sup>S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

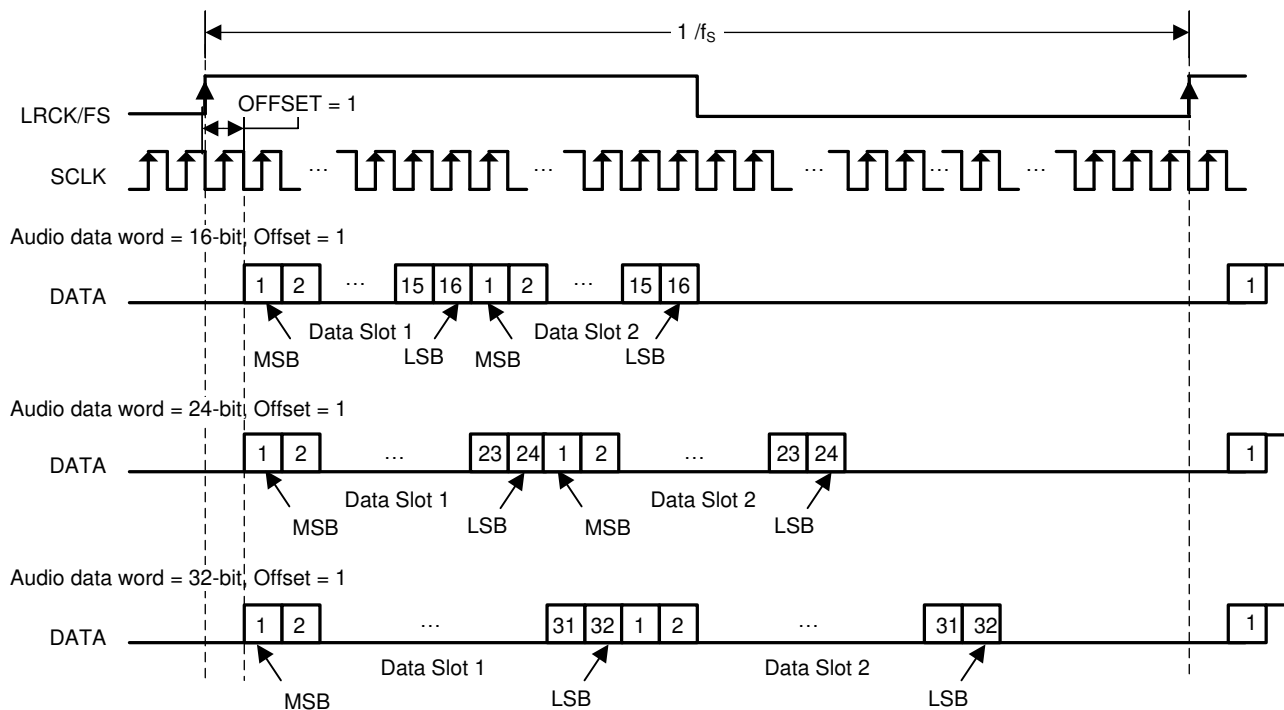
图 58. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

59. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

60. TDM 2 Audio Data Format

### 10.3.7 Digital Audio Processing

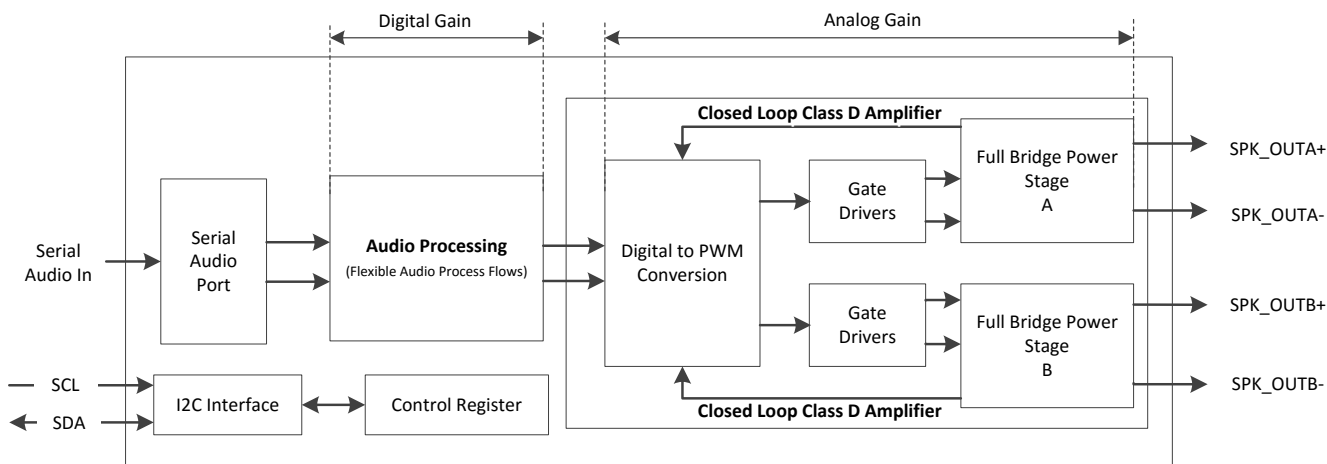
TAS5806M DSP has a flexible process flows for different applications, refer to application note, [TAS5805M Process Flows](#) for details.

### 10.3.8 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

#### 10.3.8.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in [Figure 61](#), the audio path of the TAS5806M consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.



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**Figure 61. Speaker Amplifier Gain**

As shown in [Figure 61](#), the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default, it does not change. For all settings of the register 0x54, AGAIN[4:0], the digital boost block remains at 0 dB. These gain settings ensure that the output signal is not clipping at different PVDD levels. 0 dBFS output is 29.5-V peak output voltage

**Table 2. Analog Gain Setting**

AGAIN <4:0>	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V)
00000	0	29.5
00001	-0.5	27.85
.....	.....	.....
11111	-15.5	4.95

## 10.4 Device Functional Modes

### 10.4.1 Software Control

The TAS5806M device is configured via an I<sup>2</sup>C communication port.

The I<sup>2</sup>C Communication Protocol is detailed in the I<sup>2</sup>C Communication Port section. The I<sup>2</sup>C timing requirements are described in the I<sup>2</sup>C Bus Timing – Standard and I<sup>2</sup>C Bus Timing – Fast sections.

### 10.4.2 Speaker Amplifier Operating Modes

The TAS5806M device can be used in two different amplifier configurations:

1. BTL Mode
2. PBTL Mode

#### 10.4.2.1 BTL Mode

The familiar BTL mode of operation uses the TAS5806M device to amplify two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT\_A+ and OUT\_A-, the amplified right signal is presented on differential output pair shown as OUT\_B+ and OUT\_B-.

#### 10.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5806M device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5806M device, the input signal to the PBTL amplifier is left frame of I<sup>2</sup>S or TDM data.

### 10.4.3 Low EMI Modes

TAS5806M employs several modes to minimize EMI during playing audio, and they can be used based on different applications.

#### 10.4.3.1 Minimize EMI with Spread Spectrum

This device supports spread spectrum with triangle mode, Spread spectrum is used to minimize the EMI noise.

User need configure register SS\_CTRL0 (0x6B) to Enable triangle mode and enable spread spectrum, and select spread spectrum frequency and range with SS\_CTRL1 (0x6C). For 384kHz FSW which configured by DEVICE\_CTRL1 (0x02), the spread spectrum frequency and range are described in Table 3.

**表 3. Spread Spectrum Setting**

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example-Central Switching Frequency is 384kHz, Triangle Frequency is 24kHz, take I<sup>2</sup>C device address 0x58 as an example:

w 58 6b 03 //Enable Spread Spectrum.

w 58 6c 03 //SS\_TRI\_CTRL[3:0]0011, Triangle Frequency = 24 kHz, Spread Spectrum Range should be 25% (336 kHz ~ 432 kHz).

### 10.4.3.2 Channel to Channel Phase shift

This device support channel to channel 180 degree PWM phase shift to minimize the EMI. Bit 0 of Register 0x53 can be used to disable or enable the phase shift.

### 10.4.3.3 Multi-Devices PWM Phase Synchronization

This device support up to 4 phases selection for the multi devices application system. For example, when a system integrated 4 devices, user can select phase 0/1/2/3 for each device by register PHASE\_CTRL (0x6A), which means there is a 45 degree phase shift between each device to minimize the EMI.

Recommend to do the Phase Synchronization with I<sup>2</sup>S clock during the Startup Phase.

1. Halt I<sup>2</sup>S clock.
2. Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A = 0x03 for device 0; Register 0x6A = 0x07 for device 1; Register 0x6A = 0x0B for device 2; Register 0x6A = 0x0F for device 3. There should be a 45 degree PWM phase shift between each device to minimize the EMI.
3. Configure each device into HIZ mode.
4. Provide I<sup>2</sup>S to each device. Phase synchronization for all 4 devices will be automatically done by internal sequence.
5. Initialize the DSP code. (This step can be skipped if only need to do the PWM Phase Synchronization).
6. Device to Device PWM phase shift should be fixed with 45 degree.

### 10.4.4 Thermal Foldback

The Thermal Foldback (TFB), is designed to protect TAS5806M from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the TAS5806M to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (135C typ), an internal AGL (Automatic Gain Limiter) will reduce the digital gain automatically. Once the die temperature drops below the OTW, the device digital gain gradually returns to the former setting. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed (attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5806M App in PurePath™ Console3.

### 10.4.5 Device State Control

TAS5806M has 5 states with different power dissipation which listed in the Electrical Characteristics Table.

- Shutdown Mode. With PDN pin pull down to GND. All internal LDOs (1.5V for digital core, 5V for analog) are disabled, all registers will be cleared to default value.

---

**注**

Exit from Shutdown Mode and re-enter into Play mode, need reload all register configurations (which generated by PurePath Console3) again.

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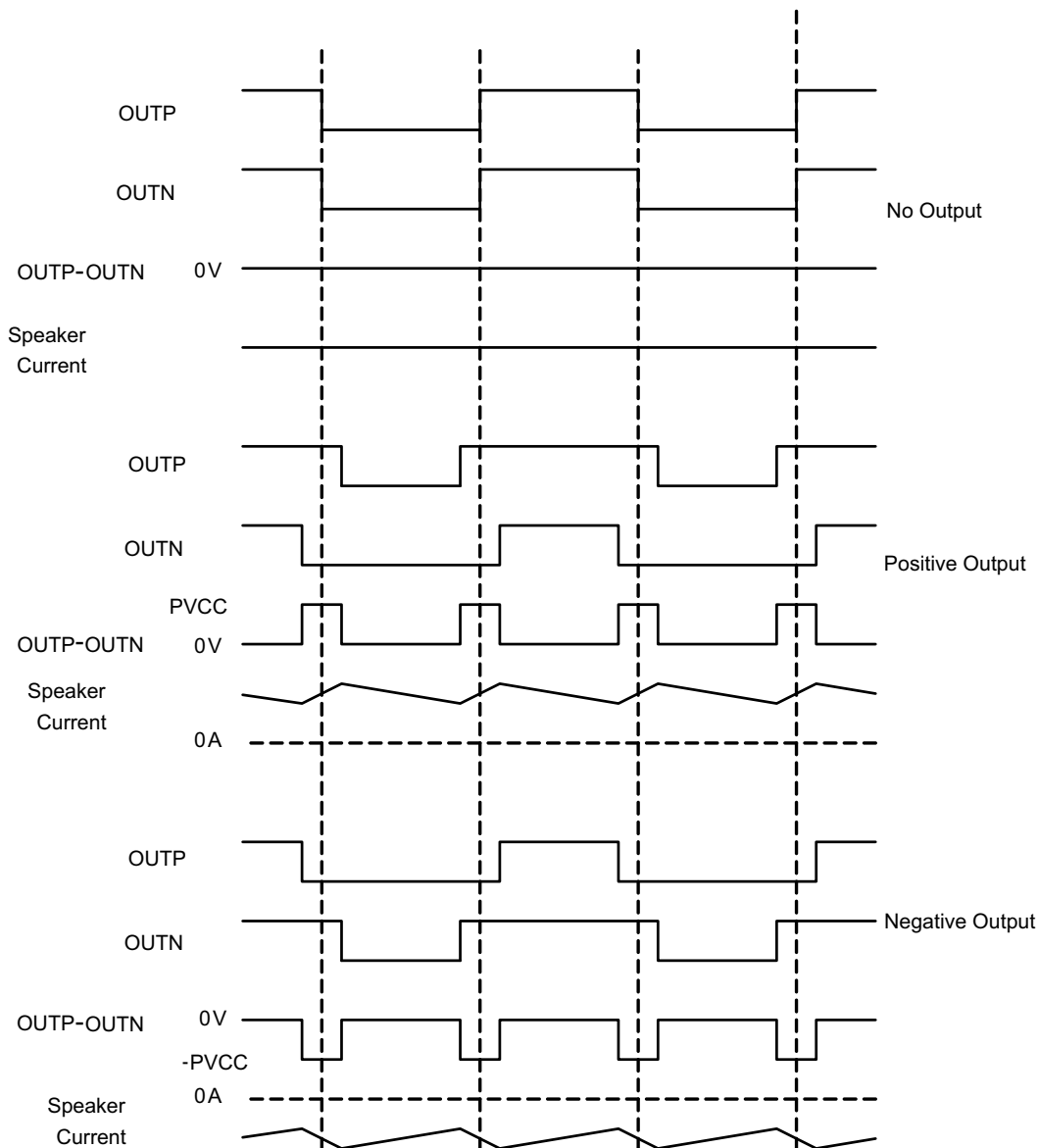
- Deep Sleep Mode. Deep Sleep Mode. Register 0x03h -D[1:0]=00, device stays in Deep Sleep Mode. In this mode, I<sup>2</sup>C block and 1.5V LDO for digital core still working, but internal 5V LDO (For AVDD and MOSFET gate driver) is disabled for low power dissipation. This mode can be used to extend the battery life in some portable speaker applications. If the host processor stops playing audio for a long time, TAS5806M can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. Unlike the Shutdown Mode (Pulling PDN Low), entering or exiting Deep Sleep Mode, the DSP keeps active.
- Sleep Mode. Register 0x03h -D[1:0]=01, device stays in Sleep Mode. In this mode, I<sup>2</sup>C block, Digital core, DSP Memory, 5V Analog LDO are stilling working. Unlike the Shutdown Mode (Pull PDN Low), enter or exit Sleep Mode, DSP is kept active. Exit from this mode and re-enter into play mode, only need to set Register 0x03h -D[1:0]=11.
- Output Hiz Mode. Register 0x03h -D[1:0]=10, device stays in Hiz Mode. In this mode, only output driver is set to be Hi-Z state, all other block operate normally. Exit from this mode and re-enter into play mode, only need to set Register 0x03h -D[1:0]=11.
- Play Mode. Register 0x03h -D[1:0]=11, device stays in Play Mode.

## 10.4.6 Device Modulation

TAS5806M has 3 modulation schemes: BD Modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for TAS5806M with Register 0x02 [1:0]-DAMP\_MOD.

### 10.4.6.1 BD Modulation

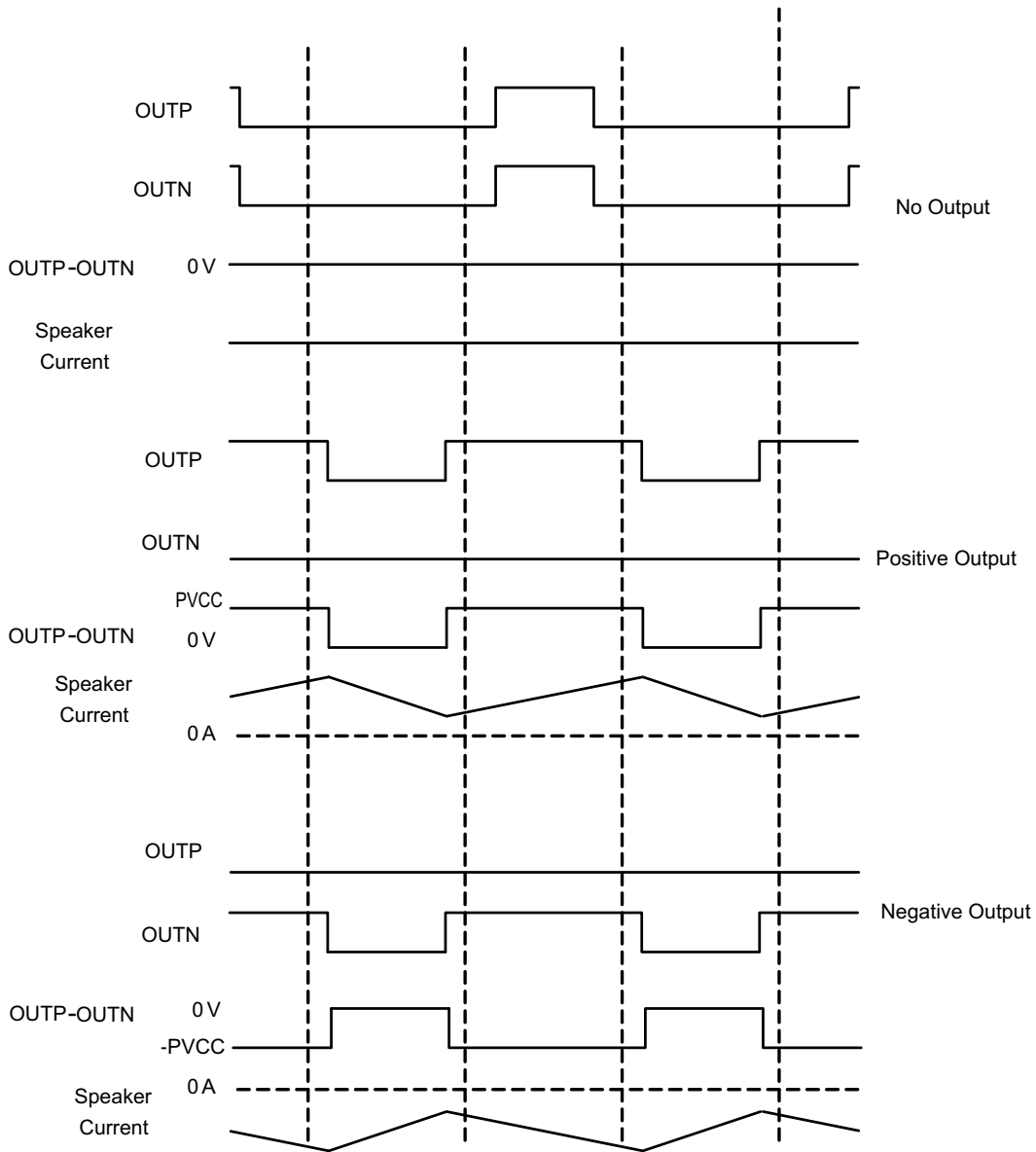
This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I<sup>2</sup>R losses in the load.



⊗ 62. BD Mode Modulation

**10.4.6.2 1SPW Modulation**

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at ~17% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.



**FIG 63. 1SPW Mode Modulation**

**10.4.6.3 Hybrid Modulation**

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5806MD will detect the input signal level and adjust PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the Hybrid Modulation.

注

To use the Hybrid Modulation, users need to enter the system's PVDD value on the TAS5806M PPC3 App.

## 10.5 Programming and Control

### 10.5.1 I<sup>2</sup>C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the Inter IC (I<sup>2</sup>C) bus protocol and supports 100 and 400-kHz data transfer rates for random and sequential write and read operations as a slave device. Because the TAS5806M register map and DSP memory spans multi pages, the user should change from page to page before writing individual register or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255.

### 10.5.2 Slave Address

The TAS5806M device has 7 bits for the slave address. The first five bits (MSBs) of the slave address are factory preset to 01011(0x5x). The next two bits of address byte are the device select bits which can be user-defined by ADR/ $\overline{\text{FAULT}}$  pin in 表 4.

表 4. I<sup>2</sup>C Slave Address Configuration

ADR/ $\overline{\text{FAULT}}$ PIN Configuration	MSBs					User Define		LSB
4.7k $\Omega$ to DVDD	0	1	0	1	1	0	0	R/ $\overline{\text{W}}$
15k $\Omega$ to DVDD	0	1	0	1	1	0	1	R/ $\overline{\text{W}}$
47k $\Omega$ to DVDD	0	1	0	1	1	1	0	R/ $\overline{\text{W}}$
120k $\Omega$ to DVDD	0	1	0	1	1	1	1	R/ $\overline{\text{W}}$

#### 10.5.2.1 Random Write

As shown in 图 64, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I<sup>2</sup>C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

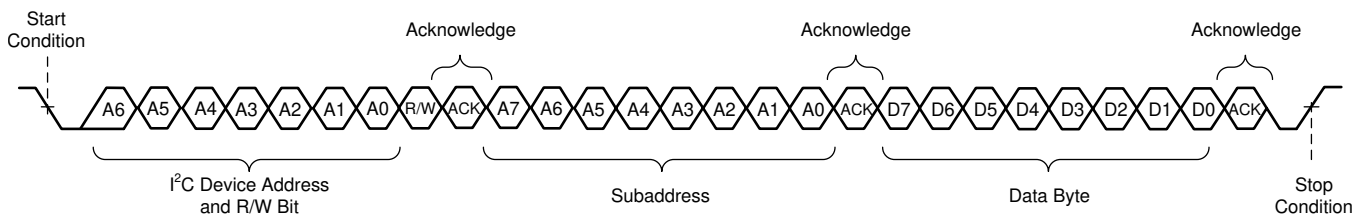


图 64. Random Write Transfer

#### 10.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in 图 65. After receiving each data byte, the device responds with an acknowledge bit and the I<sup>2</sup>C sub-address is automatically incremented by one.



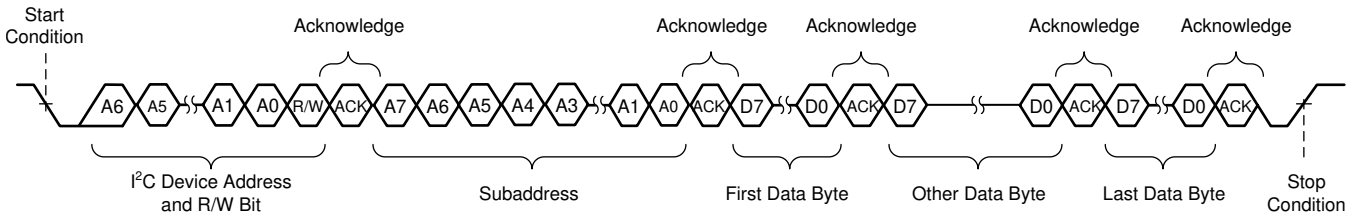


FIG 65. Sequential Write Transfer

### 10.5.2.3 Random Read

As shown in FIG 66, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

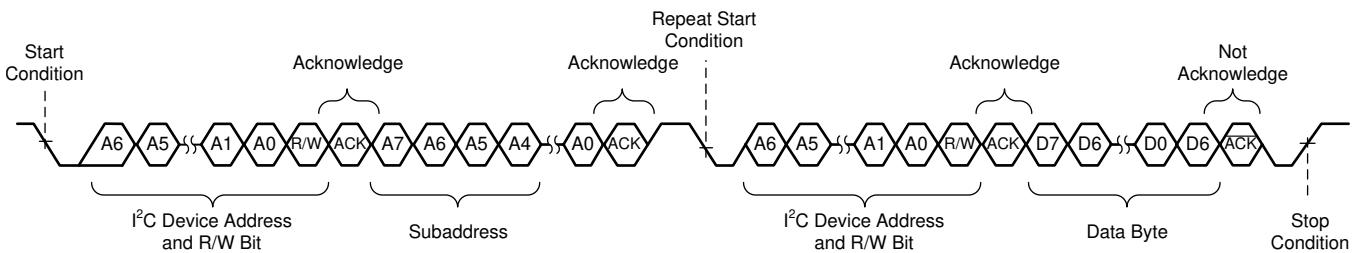
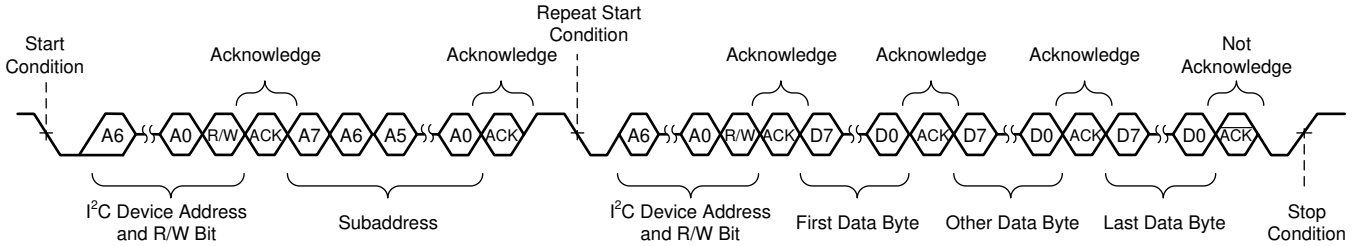
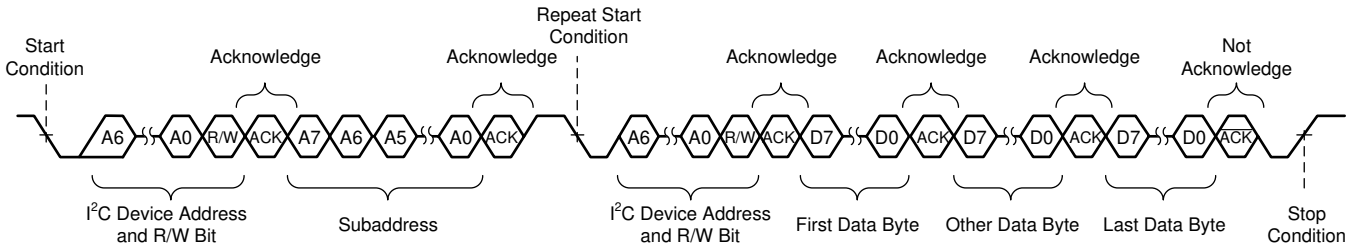


FIG 66. Random Read Transfer

### 10.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in . Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I<sup>2</sup>C sub address by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.



 **67. Sequential Read Transfer**

### 10.5.2.5 DSP Memory Book, Page and BQ update

The TAS5806M device supports the I<sup>2</sup>C serial bus and the data transmission protocol for standard and fast mode as a slave device.

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

Because the TAS5806M register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes.

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in Book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest.

All DSP/Audio Process Flow Related Register are listed in Application Note, TAS5805M Process Flows

### 10.5.2.6 Example Use

Example 1, The following is a sample script for configuring a device on I<sup>2</sup>C slave address 0x58 and set the device switching frequency to 768 kHz with Class D loop bandwidth to 175 kHz, 1SPW Modulation:

```
w 58 00 00 #Go to Page0
w 58 7f 00 #Change the Book to 0x00
w 58 00 00 #Go to Page 0x00
w 58 02 01 #Set switching frequency to 768kHz with 1SPW Modulation
w 58 53 60 #Set Class D Loop Bandwidth to 175kHz
```

Example 2, The following is a sample script for configuring a device on I<sup>2</sup>C slave address 0x58 and using the DSP host memory to change the digital volume to the default value of 0dB:

```
w 58 00 00 #Go to Page 0
w 58 7f 8c #Change the Book to 0x8C
w 58 00 2a #Go to Page 0x2a
w 58 24 00 80 00 00 #change digital volume to 0dB
```

### 10.5.2.7 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

#### 10.5.2.7.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation,  $(1 + x^1 + x^2 + x^8)$ ). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I<sup>2</sup>C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B\_x, Page\_0, Reg\_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

#### 10.5.2.7.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B\_140, Page\_0, Reg\_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

### 10.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

#### 10.5.3.1 Startup Procedures

1. Configure  $\overline{\text{ADR/FAULT}}$  pin with proper setting for I<sup>2</sup>C device address.
2. Bring up power supplies (it does not matter if PVDD/AVDD or DVDD comes up first).
3. Once power supplies are stable, bring up  $\overline{\text{PDN}}$  to high and wait at least 5 ms, then start SCLK, LRCLK.
4. Once I<sup>2</sup>S clock are stable, set the device into HiZ state and enable DSP via the I<sup>2</sup>C control port.
5. Wait at least 5 ms. Then initialize the DSP Coefficient, then set the device to Play state.
6. The device is now in normal operation.

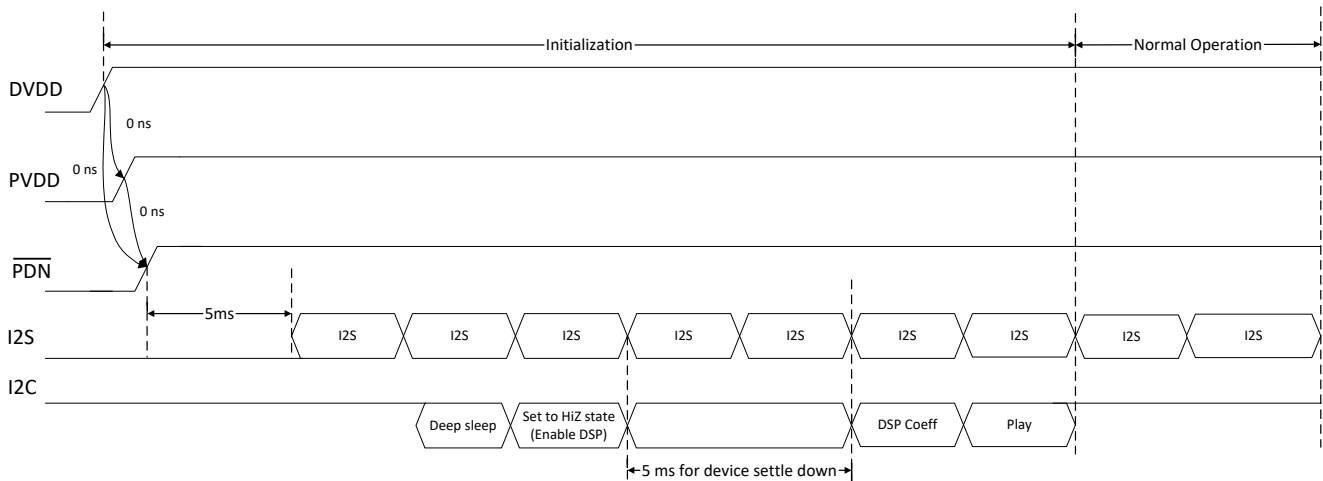
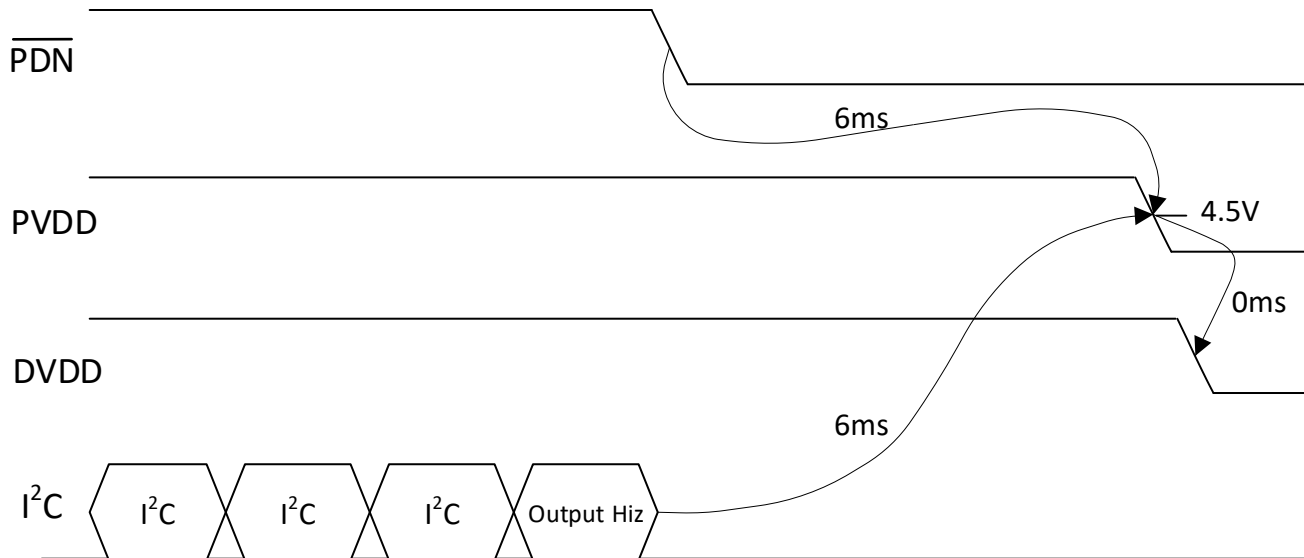


图 68. Start-up Sequence

#### 10.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register 0x03h -D[1:0]=10 (HiZ) via the I<sup>2</sup>C control port or Pull  $\overline{\text{PDN}}$  low.
3. Wait at least 6ms (this time depends on the LRCLK rate, digital volume and digital volume ramp down rate).
4. Bring down power supplies.
5. The device is now fully shutdown and powered off.



- (1) Before PVDD/DVDD power down, Class D Output driver needs to be disabled by  $\overline{\text{PDN}}$  or by I<sup>2</sup>C.
- (2) At least 6 ms delay needed based on LRCLK (Fs) = 48 kHz. Digital volume ramp down update every sample period, decreased by 0.5 dB for each update, digital volume = 24 dB. Change the value of register 0x4C and 0x4E or change the LRCLK rate, the delay changes.

⊠ 69. Power-down Sequence

### 10.5.3.3 Protection and Monitoring

#### 10.5.3.3.1 Over-current Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100 ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user may restart the affected channel via I<sup>2</sup>C. An OCSD event activates the fault pin, and the I<sup>2</sup>C fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OSCD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

#### 10.5.3.3.2 DC Detect

If the TAS5806M device measures a DC offset in the output voltage, the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault.

## 10.6 Register Maps

### 10.6.1 CONTROL PORT Registers

Table 5 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

**Table 5. CONTROL PORT Registers**

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	<a href="#">Go</a>
2h	DEVICE_CTRL_1	Register 2	<a href="#">Go</a>
3h	DEVICE_CTRL_2	Register 3	<a href="#">Go</a>
Fh	I2C_PAGE_AUTO_INC	Register 15	<a href="#">Go</a>
28h	SIG_CH_CTRL	Register 40	<a href="#">Go</a>
29h	CLOCK_DET_CTRL	Register 41	<a href="#">Go</a>
30h	SDOUT_SEL	Register 48	<a href="#">Go</a>
31h	I2S_CTRL	Register 49	<a href="#">Go</a>
33h	SAP_CTRL1	Register 51	<a href="#">Go</a>
34h	SAP_CTRL2	Register 52	<a href="#">Go</a>
35h	SAP_CTRL3	Register 53	<a href="#">Go</a>
37h	FS_MON	Register 55	<a href="#">Go</a>
38h	BCK_MON	Register 56	<a href="#">Go</a>
39h	CLKDET_STATUS	Register 57	<a href="#">Go</a>
40h	CHANNEL_FORCE_HIZ	Register 58	<a href="#">Go</a>
4Ch	DIG_VOL_CTRL	Register 76	<a href="#">Go</a>
4Eh	DIG_VOL_CTRL2	Register 78	<a href="#">Go</a>
4Fh	DIG_VOL_CTRL3	Register 79	<a href="#">Go</a>
50h	AUTO_MUTE_CTRL	Register 80	<a href="#">Go</a>
51h	AUTO_MUTE_TIME	Register 81	<a href="#">Go</a>
53h	ANA_CTRL	Register 83	<a href="#">Go</a>
54h	AGAIN	Register 84	<a href="#">Go</a>
5Ch	BQ_WR_CTRL1	Register 92	<a href="#">Go</a>
5Dh	DAC_CTRL	Register 93	<a href="#">Go</a>
60h	ADR_PIN_CTRL	Register 96	<a href="#">Go</a>
61h	ADR_PIN_CONFIG	Register 97	<a href="#">Go</a>
66h	DSP_MISC	Register 102	<a href="#">Go</a>
67h	DIE_ID	Register 103	<a href="#">Go</a>
68h	POWER_STATE	Register 104	<a href="#">Go</a>
69h	AUTOMUTE_STATE	Register 105	<a href="#">Go</a>
6Ah	PHASE_CTRL	Register 106	<a href="#">Go</a>
6Bh	SS_CTRL0	Register 107	<a href="#">Go</a>
6Ch	SS_CTRL1	Register 108	<a href="#">Go</a>
6Dh	SS_CTRL2	Register 109	<a href="#">Go</a>
6Eh	SS_CTRL3	Register 110	<a href="#">Go</a>
6Fh	SS_CTRL4	Register 111	<a href="#">Go</a>
70h	CHAN_FAULT	Register 112	<a href="#">Go</a>
71h	GLOBAL_FAULT1	Register 113	<a href="#">Go</a>
72h	GLOBAL_FAULT2	Register 114	<a href="#">Go</a>
73h	OT WARNING	Register 115	<a href="#">Go</a>
74h	PIN_CONTROL1	Register 116	<a href="#">Go</a>
75h	PIN_CONTROL2	Register 117	<a href="#">Go</a>

**Table 5. CONTROL PORT Registers (continued)**

Offset	Acronym	Register Name	Section
76h	MISC_CONTROL	Register 118	<a href="#">Go</a>
78h	FAULT_CLEAR	Register 120	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 6](#) shows the codes that are used for access types in this section.

**Table 6. CONTROL PORT Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

**10.6.1.1 RESET\_CTRL Register (Offset = 1h) [reset = 0x00]**

 RESET\_CTRL is shown in [Figure 70](#) and described in [Table 7](#).

 Return to [Summary Table](#).

**Figure 70. RESET\_CTRL Register**

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
R/W			W	R			W

**Table 7. RESET\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	RST_MOD	W	0	WRITE CLEAR BIT Reset Modules WRITE CLEAR BIT Reset full digital core This bit resets full digital signal chain (Include DSP and Control Port Registers). Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. 0: Normal 1: Reset modules
3-1	RESERVED	R	000	This bit is reserved
0	RST_CONTROL_REG	W	0	WRITE CLEAR BIT Reset Registers This bit resets the control port registers back to their initial values. The RAM content is not cleared. 0: Normal 1: Reset control port registers



### 10.6.1.2 DEVICE\_CTRL\_1 Register (Offset = 2h) [reset = 0x00]

DEVICE\_CTRL\_1 is shown in [Figure 71](#) and described in [Table 8](#).

Return to [Summary Table](#).

**Figure 71. DEVICE\_CTRL\_1 Register**

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	DAMP_PBTB	DAMP_MOD	
R/W	R/W			R/W	R/W	R/W	

**Table 8. DEVICE\_CTRL\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	FSW_SEL	R/W	000	SELECT FSW 000:768K 001:384K 011:480K 100:576K 010:Reserved 101:Reserved 110:Reserved 111:Reserved
3	RESERVED	R/W	0	This bit is reserved
2	DAMP_PBTB	R/W	0	0: SET DAMP TO BTL MODE 1: SET DAMP TO PBTB MODE
1-0	DAMP_MOD	R/W	00	00:BD MODE 01:1SPW MODE 10:HYBRID MODE

**10.6.1.3 DEVICE\_CTRL\_2 Register (Offset = 3h) [reset = 0x10]**

 DEVICE\_CTRL\_2 is shown in [Figure 72](#) and described in [Table 9](#).

 Return to [Summary Table](#).

**Figure 72. DEVICE\_CTRL\_2 Register**

7	6	5	4	3	2	1	0
RESERVED			DIS_DSP	MUTE	RESERVED	CTRL_STATE	
R/W			R/W	R/W	R/W	R/W	

**Table 9. DEVICE\_CTRL\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	DIS_DSP	R/W	1	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute Both Left /Right Channel This bit issues soft mute request for the left/right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	RESERVED	R/W	0	This bit is reserved
1-0	CTRL_STATE	R/W	00	Device state control register 00: Deep Sleep 01: Sleep 10: Hiz (Set both A channel and B channel to Hiz) Notes: For separate channel Hiz, see details in <a href="#">Table 21</a> 11: PLAY

#### 10.6.1.4 I2C\_PAGE\_AUTO\_INC Register (Offset = Fh) [reset = 0x00]

I2C\_PAGE\_AUTO\_INC is shown in [Figure 73](#) and described in [Table 10](#).

Return to [Summary Table](#).

**Figure 73. I2C\_PAGE\_AUTO\_INC Register**

7	6	5	4	3	2	1	0
RESERVED				PAGE_AUTOINC_REG	RESERVED		
R/W				R/W	R/W		

**Table 10. I2C\_PAGE\_AUTO\_INC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3	PAGE_AUTOINC_REG	R/W	0	Page auto increment disable Disable page auto increment mode for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	000	This bit is reserved

#### 10.6.1.5 SIG\_CH\_CTRL Register (Offset = 28h) [reset = 0x00]

SIG\_CH\_CTRL is shown in [Figure 74](#) and described in [Table 11](#).

Return to [Summary Table](#).

**Figure 74. SIG\_CH\_CTRL Register**

7	6	5	4	3	2	1	0
BCK_RATIO_CONFIGURE				FS_MODE			
R/W				R/W			

**Table 11. SIG\_CH\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	BCK_RATIO_CONFIGURE	R/W	0000	These bits indicate the configured BCK ratio, the number of BCK clocks in one audio frame. 0011: 32FS 0101: 64FS 0111: 128FS 1001: 256FS 1011: 512FS
3-0	FS_MODE	R/W	0000	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. 0000: Auto detection 0110: 32KHz 1000: 44.1KHz 1001: 48KHz 1010: 88.2KHz 1011: 96KHz Others Reserved

**10.6.1.6 CLOCK\_DET\_CTRL Register (Offset = 29h) [reset = 0x00]**

 CLOCK\_DET\_CTRL is shown in [Figure 75](#) and described in [Table 12](#).

 Return to [Summary Table](#).

**Figure 75. CLOCK\_DET\_CTRL Register**

7	6	5	4	3	2	1	0
RESERVED	DIS_DET_PLL	DIS_DET_BCLK_RANGE	DIS_DET_FS	DIS_DET_BCLK	DIS_DET_MISS	RESERVED	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 12. CLOCK\_DET\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL overrate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. 0: Regard PLL overrate detection 1: Ignore PLL overrate detection
5	DIS_DET_BCLK_RANGE	R/W	0	Ignore BCK Range Detection This bit controls whether to ignore the BCK range detection. The BCK must be stable between 256KHz and 50MHz or an error will be reported. When ignored, a BCK range error will not cause a clock error. 0: Regard BCK Range detection 1: Ignore BCK Range detection
4	DIS_DET_FS	R/W	0	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error. But CLKDET_STATUS will report fs error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_BCLK	R/W	0	Ignore BCK Detection This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error. 0: Regard BCK detection 1: Ignore BCK detection
2	DIS_DET_MISS	R/W	0	Ignore BCK Missing Detection This bit controls whether to ignore the BCK missing detection. When ignored an BCK missing will not cause a clock error. 0: Regard BCK missing detection 1: Ignore BCK missing detection
1	RESERVED	R/W	0	This bit is reserved
0	RESERVED	R/W	0	This bit is reserved

**10.6.1.7 SDOUT\_SEL Register (Offset = 30h) [reset = 0h]**

 SDOUT\_SEL is shown in [Figure 76](#) and described in [Table 13](#).

 Return to [Summary Table](#).

**Figure 76. SDOUT\_SEL Register**

7	6	5	4	3	2	1	0
RESERVED							SDOUT_SEL
							R/W

**Table 13. SDOUT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	RESERVED		0	This bit is reserved
0	SDOUT_SEL	R	0	SDOUT Select. This bit selects what is being output as SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

**10.6.1.8 I2S\_CTRL Register (Offset = 31h) [reset = 0x00]**

 I2S\_CTRL is shown in [Figure 77](#) and described in [Table 14](#).

 Return to [Summary Table](#).

**Figure 77. I2S\_CTRL Register**

7	6	5	4	3	2	1	0
RESERVED		BCK_INV	RESERVED		RESERVED		RESERVED
R/W		R/W	R/W	R	R		R/W

**Table 14. I2S\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	BCK_INV	R/W	0	BCK Polarity This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. 0: Normal BCK mode 1: Inverted BCK mode
4-0	RESERVED	R/W	00000	This bit is reserved

**10.6.1.9 SAP\_CTRL1 Register (Offset = 33h) [reset = 0x02]**

SAP\_CTRL1 is shown in Figure 78 and described in Table 15.

Return to [Summary Table](#).

**Figure 78. SAP\_CTRL1 Register**

7	6	5	4	3	2	1	0
I2S_SHIFT_MSB	RESERVED	DATA_FORMAT		I2S_LRCLK_PULSE		WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

**Table 15. SAP\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	I2S_SHIFT_MSB	R/W	0	I2S Shift MSB
6	RESERVED	R/W	0	This bit is reserved
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: Ircclk pulse < 8 SCLK. If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, these two bits need set to 01.
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

**10.6.1.10 SAP\_CTRL2 Register (Offset = 34h) [reset = 0x00]**

SAP\_CTRL2 is shown in Figure 79 and described in Table 16.

Return to [Summary Table](#).

**Figure 79. SAP\_CTRL2 Register**

7	6	5	4	3	2	1	0
I2S_SHIFT							
R/W							

**Table 16. SAP\_CTRL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 00000000: offset = 0 BCK (no offset) 00000001: offset = 1 BCK 00000010: offset = 2 BCKs and 11111111: offset = 512 BCKs

**10.6.1.11 SAP\_CTRL3 Register (Offset = 35h) [reset = 0x11]**

SAP\_CTRL3 is shown in [Figure 80](#) and described in [Table 17](#).

Return to [Summary Table](#).

**Figure 80. SAP\_CTRL3 Register**

7	6	5	4	3	2	1	0
RESERVED		LEFT_DAC_DPATH		RESERVED		RIGHT_DAC_DPATH	
R/W		R/W		R/W		R/W	

**Table 17. SAP\_CTRL3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	LEFT_DAC_DPATH	R/W	01	Left DAC Data Path. These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3-2	RESERVED	R/W	00	This bit is reserved
1-0	RIGHT_DAC_DPATH	R/W	01	Right DAC Data Path. These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)



### 10.6.1.12 FS\_MON Register (Offset = 37h) [reset = 0x00]

FS\_MON is shown in [Figure 81](#) and described in [Table 18](#).

Return to [Summary Table](#).

**Figure 81. FS\_MON Register**

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH			FS		
R/W		R			R		

**Table 18. FS\_MON Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	BCLK_RATIO_HIGH	R	00	2 msbs of detected BCK ratio
3-0	FS	R	0000	These bits indicate the currently detected audio sampling rate. 0000: FS Error 0110: 32KHz 1000: Reserved 1001: 48KHz 1011: 96KHz Others Reserved

### 10.6.1.13 BCK\_MON Register (Offset = 38h) [reset = 0x00]

BCK\_MON is shown in [Figure 82](#) and described in [Table 19](#).

Return to [Summary Table](#).

**Figure 82. BCK\_MON Register**

7	6	5	4	3	2	1	0
BCLK_RATIO_LOW							
R							

**Table 19. BCK\_MON Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO_LOW	R	00000000	These bits indicate the currently detected BCK ratio, the number of BCK clocks in one audio frame. BCK = 32 FS~512 FS

**10.6.1.14 CLKDET\_STATUS Register (Offset = 39h) [reset = 0x00]**

 CLKDET\_STATUS is shown in [Figure 83](#) and described in [Table 20](#).

 Return to [Summary Table](#).

**Figure 83. CLKDET\_STATUS Register**

7	6	5	4	3	2	1	0
RESERVED		DET_STATUS					
R/W		R					

**Table 20. CLKDET\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	DET_STATUS	R	0	This bit indicates whether the BCLK is overrate or underrate
4	DET_STATUS	R	0	This bit indicates whether the PLL is overrate
3	DET_STATUS	R	0	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled.
2	DET_STATUS	R	0	This bit indicates whether the BCK is missing or not.
1	DET_STATUS	R	0	This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-512FS to be valid.
0	DET_STATUS	R	0	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid or not. In non auto detection mode(reg_fsmode!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag will be also asserted.

**10.6.1.15 CHANNEL\_FORCE\_HIZ Register (Offset = 40h) [reset = 0x01]**

CHANNEL\_FORCE\_HIZ is shown in [Figure 84](#) and described in [Table 21](#).

Return to [Summary Table](#).

**Figure 84. CHANNEL\_FORCE\_HIZ Register**

7	6	5	4	3	2	1	0
RESERVED			CH_A_HIZ	CH_B_HIZ	RESERVED		
R/W			R/W	R/W	R/W		

**Table 21. CHANNEL\_FORCE\_HIZ Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	These bits are reserved
4	CH_A_HIZ	R/W	0	1: Force Channel A (L channel) to Hiz mode. 0: Exit Force Hi-Z mode, Channel A is now controlled by Register 0x03, see <a href="#">Table 9</a> . Notes: If channel has been forced to Hiz, only method to exit Force Hi-Z mode is set this bit to 0. This function is disabled in PBTL mode.
3	CH_B_HIZ	R/W	0	1: Force Channel B (R channel) to Hiz mode. 0: Exit Force Hi-Z mode, Channel B is now controlled by Register 0x03, see <a href="#">Table 9</a> . Notes: If channel has been forced to Hiz, only method to exit Force Hi-Z mode is set this bit to 0. This function is disabled in PBTL mode.
2-0	RESERVED	R/W	001	These bits are reserved.

**10.6.1.16 DIG\_VOL\_CTL Register (Offset = 4Ch) [reset = 30h]**

DIG\_VOL\_CTL is shown in [Figure 85](#) and described in [Table 22](#).

Return to [Summary Table](#).

**Figure 85. DIG\_VOL\_CTL Register**

7	6	5	4	3	2	1	0
PGA							
R/W							

**Table 22. DIG\_VOL\_CTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PGA	R/W	00110000	Digital Volume These bits control both left and right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB ..... and 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ..... 11111110: -103 dB 11111111: Mute

**10.6.1.17 DIG\_VOL\_CTRL2 Register (Offset = 4Eh) [reset = 0x33]**

 DIG\_VOL\_CTRL2 is shown in [Figure 86](#) and described in [Table 23](#).

 Return to [Summary Table](#).

**Figure 86. DIG\_VOL\_CTRL2 Register**

7	6	5	4	3	2	1	0
PGA_RAMP_DOWN_SPEED		PGA_RAMP_DOWN_STEP		PGA_RAMP_UP_SPEED		PGA_RAMP_UP_STEP	
R/W		R/W		R/W		R/W	

**Table 23. DIG\_VOL\_CTRL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	PGA_RAMP_DOWN_STEP	R/W	11	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	PGA_RAMP_UP_SPEED	R/W	00	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	PGA_RAMP_UP_STEP	R/W	11	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

**10.6.1.18 DIG\_VOL\_CTRL3 Register (Offset = 4Fh) [reset = 0x30]**

DIG\_VOL\_CTRL3 is shown in [Figure 87](#) and described in [Table 24](#).

Return to [Summary Table](#).

**Figure 87. DIG\_VOL\_CTRL3 Register**

7	6	5	4	3	2	1	0
FAST_RAMP_DOWN_SPEED		FAST_RAMP_DOWN_STEP		RESERVED			
R/W		R/W		R/W			

**Table 24. DIG\_VOL\_CTRL3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	FAST_RAMP_DOWN_STEP	R/W	11	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	RESERVED	R/W	0000	This bit is reserved

**10.6.1.19 AUTO\_MUTE\_CTRL Register (Offset = 50h) [reset = 0x07]**

AUTO\_MUTE\_CTRL is shown in [Figure 88](#) and described in [Table 25](#).

Return to [Summary Table](#).

**Figure 88. AUTO\_MUTE\_CTRL Register**

7	6	5	4	3	2	1	0
RESERVED					REG_AUTO_MUTE_CTRL		
R/W					R/W		

**Table 25. AUTO\_MUTE\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2	REG_AUTO_MUTE_CTRL	R/W	1	0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted
1	REG_AUTO_MUTE_CTRL	R/W	1	0: Disable right channel auto mute 1: Enable right channel auto mute
0	REG_AUTO_MUTE_CTRL	R/W	1	0: Disable left channel auto mute 1: Enable left channel auto mute bit2: .

**10.6.1.20 AUTO\_MUTE\_TIME Register (Offset = 51h) [reset = 0x00]**

 AUTO\_MUTE\_TIME is shown in [Figure 89](#) and described in [Table 26](#).

 Return to [Summary Table](#).

**Figure 89. AUTO\_MUTE\_TIME Register**

7	6	5	4	3	2	1	0
RESERVED	AUTOMUTE_TIME_LEFT			RESERVED	AUTOMUTE_TIME_RIGHT		
R/W	R/W			R/W	R/W		

**Table 26. AUTO\_MUTE\_TIME Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	AUTOMUTE_TIME_LEFT	R/W	000	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0	This bit is reserved
2-0	AUTOMUTE_TIME_RIGHT	R/W	000	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

**10.6.1.21 ANA\_CTRL Register (Offset = 53h) [reset = 0x00]**

ANA\_CTRL is shown in [Figure 90](#) and described in [Table 27](#).

Return to [Summary Table](#).

**Figure 90. ANA\_CTRL Register**

7	6	5	4	3	2	1	0
ANA_CTRL							
R/W							

**Table 27. ANA\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	ANA_CTRL	R/W	00	Class-D bandwidth control. 00: 80kHz; 01: 100kHz; 10: 120kHz; 11: 175kHz. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance. With Fsw=384kHz, bandwidth should ≤ 120kHz.
4-0	RESERVED	R/W	0000	These bits are reserved

**10.6.1.22 AGAIN Register (Offset = 54h) [reset = 0x00]**

 AGAIN is shown in [Figure 91](#) and described in [Table 28](#).

 Return to [Summary Table](#).

**Figure 91. AGAIN Register**

7	6	5	4	3	2	1	0
RESERVED				ANA_GAIN			
R/W				R/W			

**Table 28. AGAIN Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control , with 0.5dB one step This bit controls the analog gain. 00000: 0 dB (29.5V peak voltage) 00001: -0.5db 11111: -15.5 dB

**10.6.1.23 BQ\_WR\_CTRL1 Register (Offset = 5Ch) [reset = 0x00]**

 BQ\_WR\_CTRL1 is shown in [Figure 92](#) and described in [Table 29](#).

 Return to [Summary Table](#).

**Figure 92. BQ\_WR\_CTRL1 Register**

7	6	5	4	3	2	1	0
RESERVED							BQ_WR_FIRST_COEF
R/W							R/W

**Table 29. BQ\_WR\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	BQ_WR_FIRST_COEF	R/W	0	Indicate the first coefficient of a BQ is starting to write.



**10.6.1.24 DAC\_CTRL Register (Offset = 5Dh) [reset = 0xF8]**

DAC\_CTRL is shown in Figure 93 and described in Table 30.

Return to [Summary Table](#).

**Figure 93. DAC\_CTRL Register**

7	6	5	4	3	2	1	0
DAC_FREQUE NCY_SEL	DAC_DITHER_EN		DAC_DITHER			DAC_CTRL_DEM_SEL	
R/W	R/W		R/W			R/W	

**Table 30. DAC\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DAC_FREQUENCY_SEL	R/W	1	DAC Frequency Select 0: 6.144MHz 1: 3.072MHz
6-5	DAC_DITHER_EN	R/W	11	DITHER_EN, 00: disable both stage dither 01: enable main stage dither 10: enable second stage dither 11: enable both stage dither
4-2	DAC_DITHER	R/W	110	Dither level 100: -2 <sup>-7</sup> 101: -2 <sup>-8</sup> 110: -2 <sup>-9</sup> 111: -2 <sup>-10</sup> 000: -2 <sup>-13</sup> 001: -2 <sup>-14</sup> 010: -2 <sup>-15</sup> 011: -2 <sup>-16</sup>
1-0	DAC_CTRL_DEM_SEL	R/W	00	00: Enable DEM 11: Disable DEM

**10.6.1.25 ADR\_PIN\_CTRL Register (Offset = 60h) [reset = 0h]**

ADR\_PIN\_CTRL is shown in Figure 94 and described in Table 31.

Return to [Summary Table](#).

**Figure 94. ADR\_PIN\_CTRL Register**

7	6	5	4	3	2	1	0
RESERVED							ADR_OE
							R/W - 0x0

**Table 31. ADR\_PIN\_CTRL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	ADR_OE	R/W	0	ADR Output Enable This bit sets the direction of the ADR pin 0: ADR is input 1: ADR is output

**10.6.1.26 ADR\_PIN\_CONFIG Register (Offset = 61h) [reset = 0x00]**

 ADR\_PIN\_CONFIG is shown in [Figure 95](#) and described in [Table 32](#).

 Return to [Summary Table](#).

**Figure 95. ADR\_PIN\_CONFIG Register**

7	6	5	4	3	2	1	0
RESERVED			ADR_PIN_CONFIG				
R/W							

**Table 32. ADR\_PIN\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	These bits are reserved
4-0	ADR_PIN_CONFIG	R/W	00000	00000: off (low) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 0101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock missing) 00111: Reserved 01001: Reserved 01011: ADR as FAULTZ output

**10.6.1.27 DSP\_MISC Register (Offset = 66h) [reset = 0h]**

 DSP\_MISC is shown in [Figure 96](#) and described in [Table 33](#).

 Return to [Summary Table](#).

**Figure 96. DSP\_MISC Register**

7	6	5	4	3	2	1	0
BYPASS_CONTROL							
R/W							

**Table 33. DSP\_MISC Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	These bits are reserved
3	BYPASS CONTROL	R/W	0	1: Left and Right will have use unique coef 0->Right channel will share left channel coefficient
2	BYPASS CONTROL	R/W	0	1: bypass 128 tap FIR
1	BYPASS CONTROL	R/W	0	1: bypass DRC (Only bypass DRC in L/R channel)
0	BYPASS CONTROL	R/W	0	1: bypass EQ (Only bypass EQs in L/R channel)

**10.6.1.28 DIE\_ID Register (Offset = 67h) [reset = 0h]**

 DIE\_ID is shown in [Figure 97](#) and described in [Table 34](#).

 Return to [Summary Table](#).

**Figure 97. DIE\_ID Register**

7	6	5	4	3	2	1	0
DIE_ID							
R-0h							

**Table 34. DIE\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	0h	DIE ID

**10.6.1.29 POWER\_STATE Register (Offset = 68h) [reset = 0x00]**

POWER\_STATE is shown in [Figure 98](#) and described in [Table 35](#).

Return to [Summary Table](#).

**Figure 98. POWER\_STATE Register**

7	6	5	4	3	2	1	0
STATE_RPT							
R							

**Table 35. POWER\_STATE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	STATE_RPT	R	00000000	0: Deep sleep 1: Sleep 2: HIZ 3: Play Others: reserved

**10.6.1.30 AUTOMUTE\_STATE Register (Offset = 69h) [reset = 0x00]**

 AUTOMUTE\_STATE is shown in [Figure 99](#) and described in [Table 36](#).

 Return to [Summary Table](#).

**Figure 99. AUTOMUTE\_STATE Register**

7	6	5	4	3	2	1	0
RESERVED						ZERO_RIGHT_ MON	ZERO_LEFT_ MON
R						R	R

**Table 36. AUTOMUTE\_STATE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	ZERO_RIGHT_MON	R	0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
0	ZERO_LEFT_MON	R	0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

**10.6.1.31 PHASE\_CTRL Register (Offset = 6Ah) [reset = 0x00]**

 PHASE\_CTRL is shown in [Figure 100](#) and described in [Table 37](#).

 Return to [Summary Table](#).

**Figure 100. PHASE\_CTR Register**

7	6	5	4	3	2	1	0
RESERVED				RAMP_PHASE_SEL		PHASE_SYNC_SEL	PHASE_SYNC_EN
R/W				R/W		R/W	R/W

**Table 37. PHASE\_CTR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-2	RAMP_PHASE_SEL	R/W	00	Select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recommended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. 00: phase0 01: phase1 10: phase2 11: phase3
1	I2S_SYNC_EN	R/W	0	Use I2S to synchronize output PWM phase 0: Disable 1: Enable
0	PHASE_SYNC_EN	R/W	0	0: RAMP phase sync disable 1: RAMP phase sync enable

**10.6.1.32 SS\_CTRL0 Register (Offset = 6Bh) [reset = 0x00]**

SS\_CTRL0 is shown in [Figure 101](#) and described in [Table 38](#).

Return to [Summary Table](#).

**Figure 101. SS\_CTRL0 Register**

7	6	5	4	3	2	1	0
RESERVED	RESERVED	SS_PRE_DIV_SEL	SS_MANUAL_MODE	RESERVED		SS_RDM_EN	SS_TRI_EN
R/W	R/W	R/W	R/W	R/W		R/W	R/W

**Table 38. SS\_CTRL0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	RESERVED	R/W	0	This bit is reserved
5	SS_PRE_DIV_SEL	R/W	0	Select pll clock divide 2 as source clock in manual mode
4	SS_MANUAL_MODE	R/W	0	Set ramp ss controller to manual mode
3-2	RESERVED	R/W	0	This bit is reserved
1	SS_RDM_EN	R/W	0	Random SS enable
0	SS_TRI_EN	R/W	0	Triangle SS enable

**10.6.1.33 SS\_CTRL1 Register (Offset = 6Ch) [reset = 0x00]**

SS\_CTRL1 is shown in [Figure 102](#) and described in [Table 39](#).

Return to [Summary Table](#).

**Figure 102. SS\_CTRL1 Register**

7	6	5	4	3	2	1	0
RESERVED	SS_RDM_CTRL			SS_TRI_CTRL			
R/W	R/W			R/W			

**Table 39. SS\_CTRL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	SS_RDM_CTRL	R/W	000	Random SS range control
3-0	SS_TRI_CTRL	R/W	0000	Triangle SS frequency and range control

**10.6.1.34 SS\_CTRL2 Register (Offset = 6Dh) [reset = 0x50]**

 SS\_CTRL2 is shown in [Figure 103](#) and described in [Table 40](#).

 Return to [Summary Table](#).

**Figure 103. SS\_CTRL2 Register**

7	6	5	4	3	2	1	0
TM_FREQ_CTRL							
R/W							

**Table 40. SS\_CTRL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	TM_FREQ_CTRL	R/W	01010000	Control ramp frequency in manual mode, F=61440000/N

**10.6.1.35 SS\_CTRL3 Register (Offset = 6Eh) [reset = 0x11]**

 SS\_CTRL3 is shown in [Figure 104](#) and described in [Table 41](#).

 Return to [Summary Table](#).

**Figure 104. SS\_CTRL3 Register**

7	6	5	4	3	2	1	0
TM_DSTEP_CTRL				TM_USTEP_CTRL			
R/W				R/W			

**Table 41. SS\_CTRL3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	SS_TM_DSTEP_CTRL	R/W	0001	Control triangle mode spread spectrum fall step in ramp ss manual mode
3-0	SS_TM_USTEP_CTRL	R/W	0001	Control triangle mode spread spectrum rise step in ramp ss manual mode

**10.6.1.36 SS\_CTRL4 Register (Offset = 6Fh) [reset = 0x24]**

 SS\_CTRL4 is shown in [Figure 105](#) and described in [Table 42](#).

 Return to [Summary Table](#).

**Figure 105. SS\_CTRL4 Register**

7	6	5	4	3	2	1	0
RESERVED	TM_AMP_CTRL		SS_TM_PERIOD_BOUNDRY				
R/W	R/W		R/W				

**Table 42. SS\_CTRL4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	TM_AMP_CTRL	R/W	01	Control ramp amp ctrl in ramp ss manual model
4-0	SS_TM_PERIOD_BOUNDRY	R/W	00100	Control triangle mode spread spectrum boundary in ramp ss manual mode



**10.6.1.37 CHAN\_FAULT Register (Offset = 70h) [reset = 0x00]**

CHAN\_FAULT is shown in [Figure 106](#) and described in [Table 43](#).

Return to [Summary Table](#).

**Figure 106. CHAN\_FAULT Register**

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

**Table 43. CHAN\_FAULT Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	Left channel DC fault
2	CH2_DC_1	R	0	Right channel DC fault
1	CH1_OC_I	R	0	Left channel over current fault
0	CH2_OC_I	R	0	Right channel over current fault

**10.6.1.38 GLOBAL\_FAULT1 Register (Offset = 71h) [reset = 0h]**

GLOBAL\_FAULT1 is shown in [Figure 107](#) and described in [Table 44](#).

Return to [Summary Table](#).

**Figure 107. GLOBAL\_FAULT1 Register**

7	6	5	4	3	2	1	0
OTP_CRC_ER ROR	BQ_WR_ERRO R				CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R				R	R	R

**Table 44. GLOBAL\_FAULT1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0h	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0h	The recent BQ is written failed
5-3	RESERVED	R	0h	This bit is reserved
2	CLK_FAULT_I	R	0h	Clock fault
1	PVDD_OV_I	R	0h	PVDD OV fault
0	PVDD_UV_I	R	0h	PVDD UV fault

**10.6.1.39 GLOBAL\_FAULT2 Register (Offset = 72h) [reset = 0h]**

 GLOBAL\_FAULT2 is shown in [Figure 108](#) and described in [Table 45](#).

 Return to [Summary Table](#).

**Figure 108. GLOBAL\_FAULT2 Register**

7	6	5	4	3	2	1	0
RESERVED				RESERVED		OTSD_I	
R				R		R	

**Table 45. GLOBAL\_FAULT2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000	This bit is reserved
0	OTSD_I	R	0	Over temperature shut down fault

**10.6.1.40 OT\_WARNING Register (Offset = 73h) [reset = 0x00]**

 OT\_WARNING is shown in [Figure 109](#) and described in [Table 46](#).

 Return to [Summary Table](#).

**Figure 109. OT\_WARNING Register**

7	6	5	4	3	2	1	0
RESERVED		RESERVED			OTW	RESERVED	
R		R			R	R	

**Table 46. OT\_WARNING Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	This bit is reserved
5-3	RESERVED	R	000	This bit is reserved
2	OTW	R	0	Over temperature warning ,135C
1-0	RESERVED	R	00	This bit is reserved

### 10.6.1.41 PIN\_CONTROL1 Register (Offset = 74h) [reset = 0x00]

PIN\_CONTROL1 is shown in [Figure 110](#) and described in [Table 47](#).

Return to [Summary Table](#).

**Figure 110. PIN\_CONTROL1 Register**

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDD_UV	MASK_DVDD_OV	MASK_CLK_F AULT	MASK_PVDD_UV	MASK_PVDD_OV	MASK_DC	MASK_OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 47. PIN\_CONTROL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0	Mask OTSD fault report
6	MASK_DVDD_UV	R/W	0	Mask DVDD UV fault report
5	MASK_DVDD_OV	R/W	0	Mask DVDD OV fault report
4	MASK_CLK_FAULT	R/W	0	Mask clock fault report
3	MASK_PVDD_UV	R/W	0	Mask PVDD UV fault report
2	MASK_PVDD_OV	R/W	0	Mask PVDD OV fault report
1	MASK_DC	R/W	0	Mask DC fault report
0	MASK_OC	R/W	0	Mask OC fault report

### 10.6.1.42 PIN\_CONTROL2 Register (Offset = 75h) [reset = 0xF8]

PIN\_CONTROL2 is shown in [Figure 111](#) and described in [Table 48](#).

Return to [Summary Table](#).

**Figure 111. PIN\_CONTROL2 Register**

7	6	5	4	3	2	1	0
RESERVED		CLKFLT_LATC H_EN	OTSD_LATCH _EN	OTW_LATCH_ EN	MASK_OTW	RESERVED	
		R/W	R/W	R/W	R/W		

**Table 48. PIN\_CONTROL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	11	This bit is reserved
5	CLKFLT_LATCH_EN	R/W	1	Enable clock fault latch
4	OTSD_LATCH_EN	R/W	1	Enable OTSD fault latch
3	OTW_LATCH_EN	R/W	1	Enable OT warning latch
2	MASK_OTW	R/W	0	Mask OT warning report
1-0	RESERVED	R/W	00	This bit is reserved

**10.6.1.43 MISC\_CONTROL Register (Offset = 76h) [reset = 0x00]**

 MISC\_CONTROL is shown in [Figure 112](#) and described in [Table 49](#).

 Return to [Summary Table](#).

**Figure 112. MISC\_CONTROL Register**

7	6	5	4	3	2	1	0
DET_STATUS_LATCH	RESERVED		OTSD_AUTO_REC_EN	RESERVED			
R/W	R/W		R/W	R/W			

**Table 49. MISC\_CONTROL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	DET_STATUS_LATCH	R/W	0	1:Latch clock detection status 0:Don't latch clock detection status
6-5	RESERVED	R/W	00	This bit is reserved
4	OTSD_AUTO_REC_EN	R/W	0	OTSD auto recovery enable
3-0	RESERVED	R/W	0000	This bit is reserved

**10.6.1.44 FAULT\_CLEAR Register (Offset = 78h) [reset = 0x00]**

 FAULT\_CLEAR is shown in [Figure 113](#) and described in [Table 50](#).

 Return to [Summary Table](#).

**Figure 113. FAULT\_CLEAR Register**

7	6	5	4	3	2	1	0
ANALOG_FAULT_CLEAR		RESERVED					
W		R/W					

**Table 50. FAULT\_CLEAR Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	W	0	WRITE CLEAR BIT. Once write this bit to 1, device will clear analog fault
6-0	RESERVED	R/W	0000000	This bit is reserved

## 11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 11.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5806M device into the larger system.

#### 11.1.1 Bootstrap Capacitors

The output stage of the TAS5806M uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22-μF capacitors to connect the appropriate output pin (OUT\_X) to the bootstrap pin (BST\_X). For example, connect a 0.22-μF capacitor between OUT\_A and BST\_A for bootstrapping the A channel. Similarly, connect another 0.22-μF capacitor between the OUT\_B and BST\_B pins for the B channel inverting output.

#### 11.1.2 Inductor Selections

It is required that the peak current is smaller than the OCP (Over current protection) value which is 5A, there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to  $\theta$ .

$$I_{peak\_power\_up} \approx PVDD \times \sqrt{C/L} \times \sin(1/\sqrt{L \times C} \times \theta / F_{sw}) \tag{1}$$

注

$\theta=0.5$  (BD Modulation), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation)

表 51. Peak current during power up

PWM Modulation	PVDD	L (uH)	C (uF)	Fsw (kHz)	I <sub>peak_power_up</sub>	Comments
BD Modulation (θ=0.5)	24	4.7	0.68	384 (80kHz BW)	6.07A (>5A OCP)	1. Lower Switching Frequency only permits low Class D Loop Bandwidth, which cause worse THD+N. 2. Lower Switching Frequency cause higher startup peak current, which needs Inductor supports higher saturation current. 3. BD Mode has more switching loss than 1SPW mode, so the thermal performance is worse with high PVDD, recommend 1SPW mode for high PVDD case (Typical >16V case). 4. Saturation current of Inductor needs >I <sub>peak_power_up</sub> .
	24	10	0.68	384 (80kHz BW)	3A	
	12	4.7	0.68	384 (80kHz BW)	3.32A	
	12	10	0.68	384 (80kHz BW)	1.55A	
	24	4.7	0.68	768 (175kHz BW)	3.25A	
	24	10	0.68	768 (175kHz BW)	1.55A	

**Application Information (continued)**
**表 51. Peak current during power up (continued)**

PWM Modulation	PVDD	L (uH)	C (uF)	Fsw (kHz)	I <sub>peak_power_up</sub>	Comments
1SPW Modulation (θ=0.14)	24	4.7	0.68	384 (80kHz BW)	1.84A	1. 1SPW mode with smaller duty cycle during start up cause smaller I <sub>peak_power_up</sub>
	24	10	0.68	384 (80kHz BW)	0.87A	
	12	4.7	0.68	384 (80kHz BW)	0.92A	
	12	10	0.68	384 (80kHz BW)	0.44A	
	12	4.7	0.68	768 (175kHz BW)	0.46A	1. Even with same Inductor value, higher switching frequency cause smaller I <sub>peak_power_up</sub> which means some lower cost inductor with less saturation current is permitted. 2. 768kHz switching frequency, 175kHz Loop Bandwidth with 1SPW mode is a good balance for both thermal and audio performance.
	24	4.7	0.68	768 (175kHz BW)	0.93A	
	24	10	0.68	768 (175kHz BW)	0.87A	

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping will cause PWM duty cycle increase dramatically. This is the worst case and it rarely happens.

$$I_{peak\_clipping} \approx PVDD \times (1 - \theta) / (F_{sw} \times L) \quad (2)$$

**表 52. Peak current during PVDD clipping with Burst**

PWM Modulation	PVDD	L (uH)	Fsw (kHz)	I <sub>peak_clipping</sub>	Comments
1SPW	24	10	768	2.68A	For high PVDD case, 1SPW mode is a good option to improve thermal performance, but switching frequency can't be too low.
	24	10	576	3.58A	
	24	10	384	5.37A (>5A OCP)	
	12	10	768	1.34A	
	12	4.7	768	2.86A	
BD	24	10	768	1.56	
	24	10	384	3.12	
	12	10	768	0.78	
	12	4.7	768	1.66	

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor here.

$$I_{peak\_output\_power} \approx \sqrt{2 \times Max\_Output\_Power / R_{speaker\_Load}} \quad (3)$$

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. It is suggested that inductor saturation current I<sub>SAT</sub>, is larger than the amplifier's peak current during power-up and play audio.

$$I_{SAT} \geq \max(I_{peak\_power\_up}, I_{peak\_clipping}, I_{peak\_output\_power}) \quad (4)$$

In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in [表 53](#) to meet datasheet specifications. The minimum inductance is given in [表 53](#).

**表 53. LC filter recommendation**

PVDD (V)	Switching Frequency (kHz)	Modulation Scheme	Recommended Minimum Inductance (uH) for LC filter design
≤12	384	BD	4.7uH + 0.68uF
>12			10uH + 0.68uF
≤12	384	1SPW/Hybrid	10uH + 0.68uF
>12			15uH + 0.68uF

For higher switching frequency (Fsw), select inductors with minimum inductance to be  $384\text{kHz}/\overline{F_{sw}} \times L$ .

### 11.1.3 Power Supply Decoupling

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22 μF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1-μF or 0.1-μF capacitors as close as possible to the PVDD pins of the device.

### 11.1.4 Output EMI Filtering

The TAS5806M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

## 11.2 Typical Applications

### 11.2.1 2.0 (Stereo BTL) System

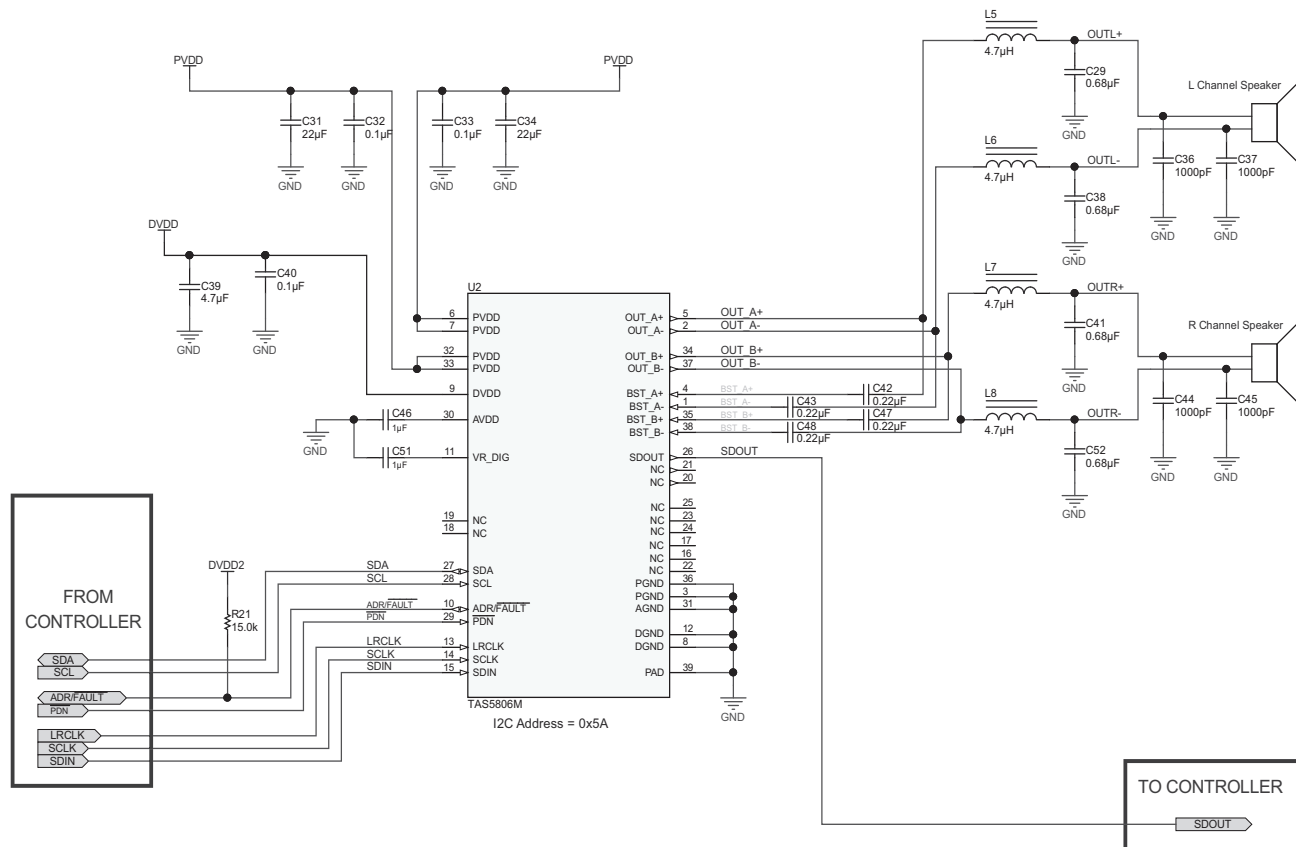
In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

 [114](#) shows the 2.0 (Stereo BTL) system application.

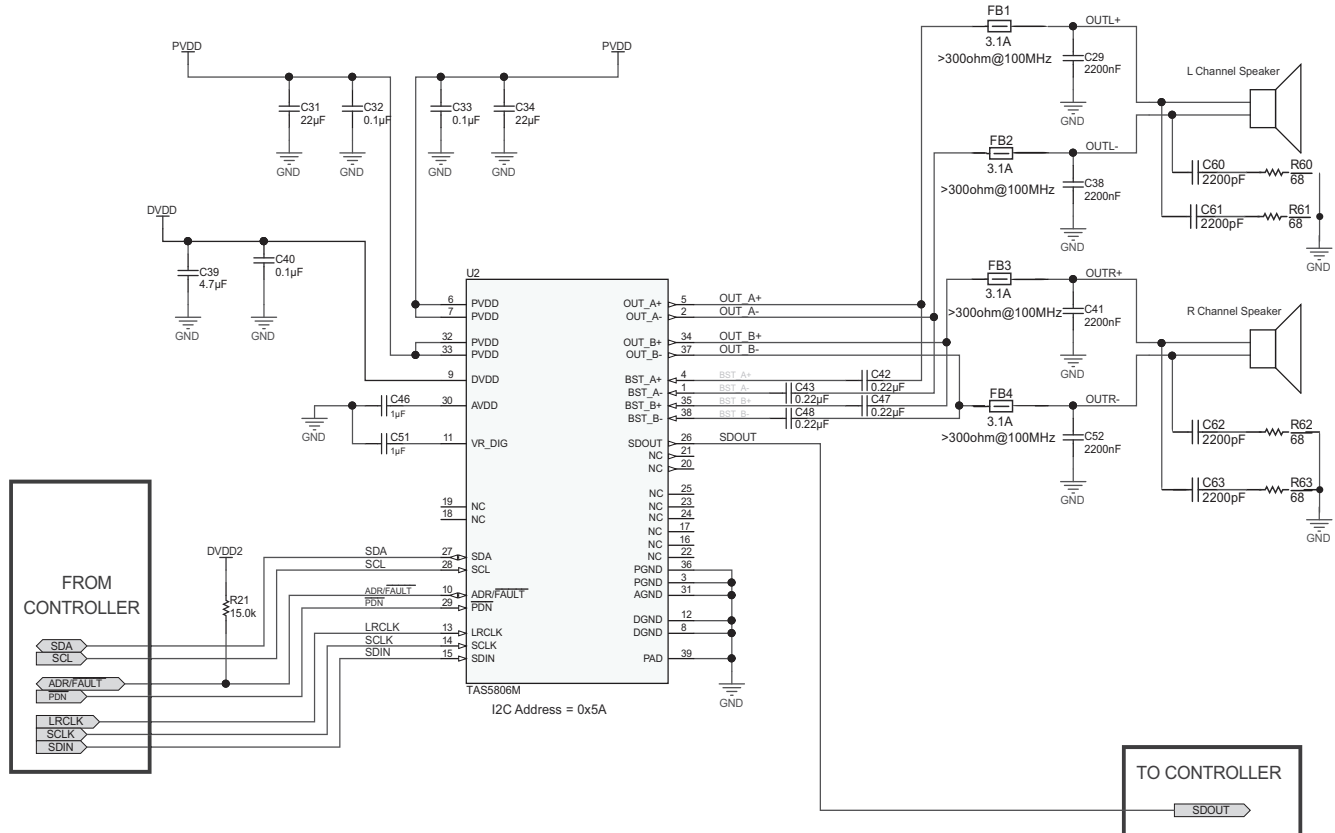


Typical Applications (continued)



114. 2.0 (Stereo BTL with Inductor as output filter) System Application Schematic

Typical Applications (continued)



115. 2.0 (Stereo BTL with Ferrite bead as output filter) System Application Schematic

11.2.2 Design Requirements

- Power supplies:
  - 3.3-V or 1.8-V supply for DVDD.
  - 4.5-V to 24-V supply for PVDD.
- Communication: host processor serving as I<sup>2</sup>C compliant master.
- External memory (Such as EEPROM or FLASH) used for coefficients.

11.2.3 Detailed Design Procedure

The design procedure can be used for Stereo 2.0, Mono, 2.1 system

11.2.3.1 Step1:Hardware Integration

- Use the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Follow the recommended component placement, board layout, and routing given in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals, all of which go to the serial audio port. Constructing these signals to ensure they

### Typical Applications (continued)

are given precedent as design trade-offs are made is recommended.

- For questions and support, go to the E2E forums (E2E.ti.com). If deviating from the recommended layout is necessary, go to the E2E forum to request a layout review.

#### 11.2.3.2 Step2: Speaker Tuning

Use the TAS5806MEVM board and the TAS5806M tuning software to configure the desired device settings.

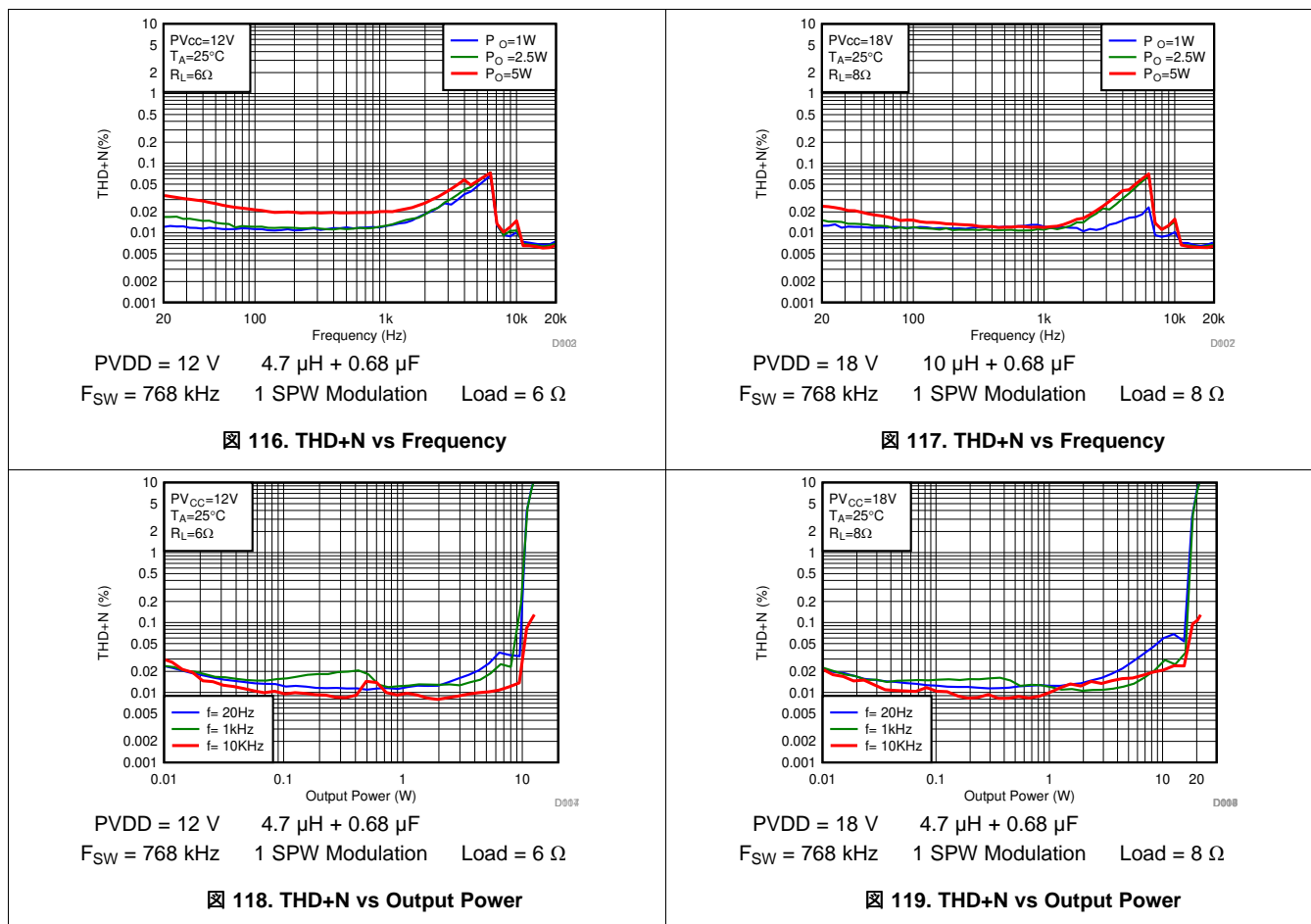
#### 11.2.3.3 Software Integration

Use the End System Integration feature of the TAS5806M tuning software app to generate a baseline configuration file.

Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.

Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

#### 11.2.3.4 Application Curves



Typical Applications (continued)

11.2.4 Mono (PBTL) system

In MONO application, TAS5806M can be used as PBTL mode to drive sub-woofer with more output power.

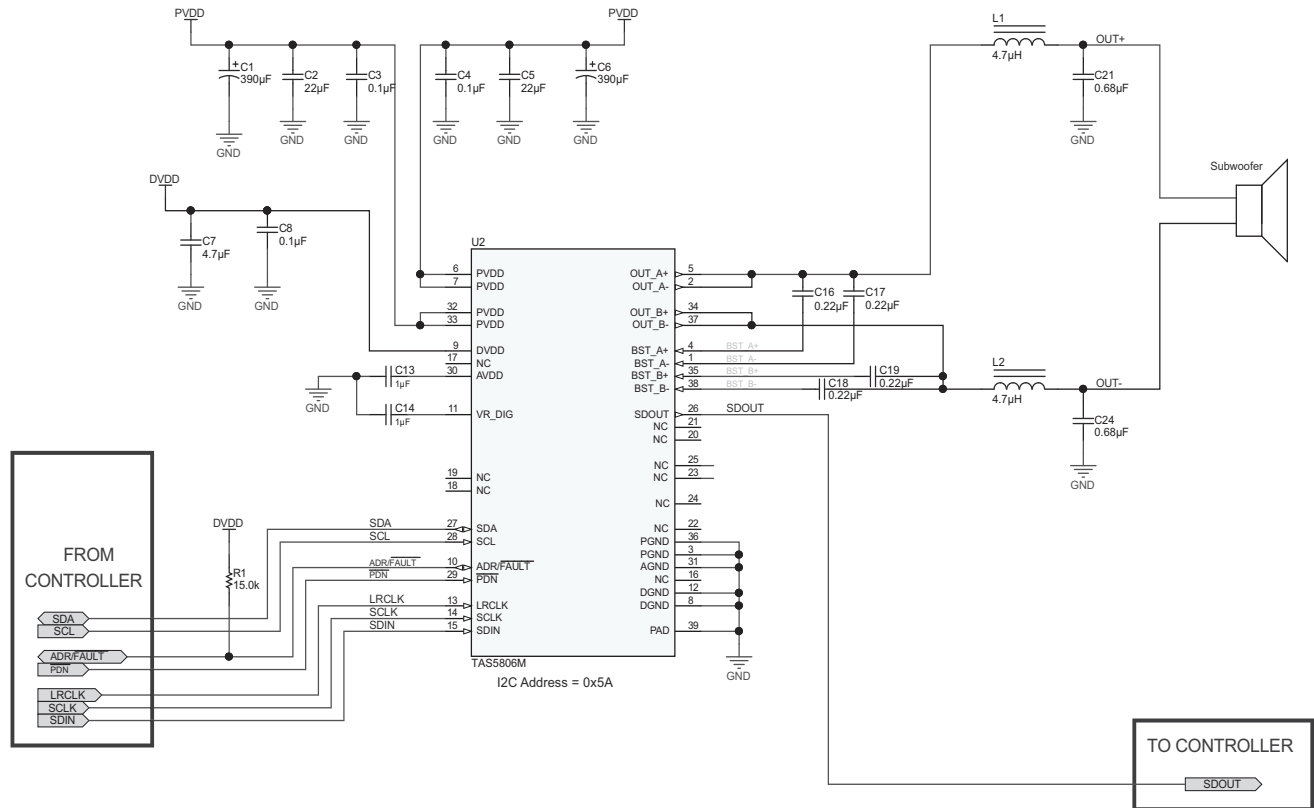
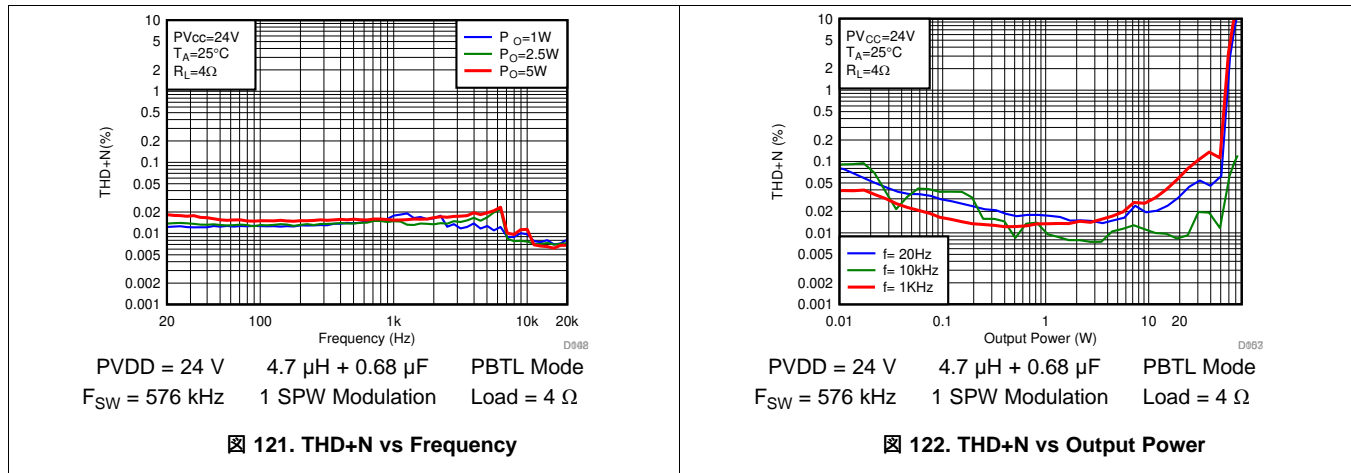


FIG 120. Mono (PBTL) System Application Schematic

**Typical Applications (continued)**

**11.2.5 Application Curves**



## 12 Power Supply Recommendations

The TAS5806M device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. One low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the *Recommended Operating Conditions* table. These two power supplies do not have a required power-up sequence. The power supplies can be powered on in any order. But once the device has been initialized, PVDD must keep within the normal operation voltage. Once PVDD lower than 3.5V, all registers need re-initialize again. Recommends waiting 1 ms to 5 ms for the DVDD power supplies to stabilize before starting I<sup>2</sup>C communication and providing stable I<sup>2</sup>S clock before enabling the device outputs.

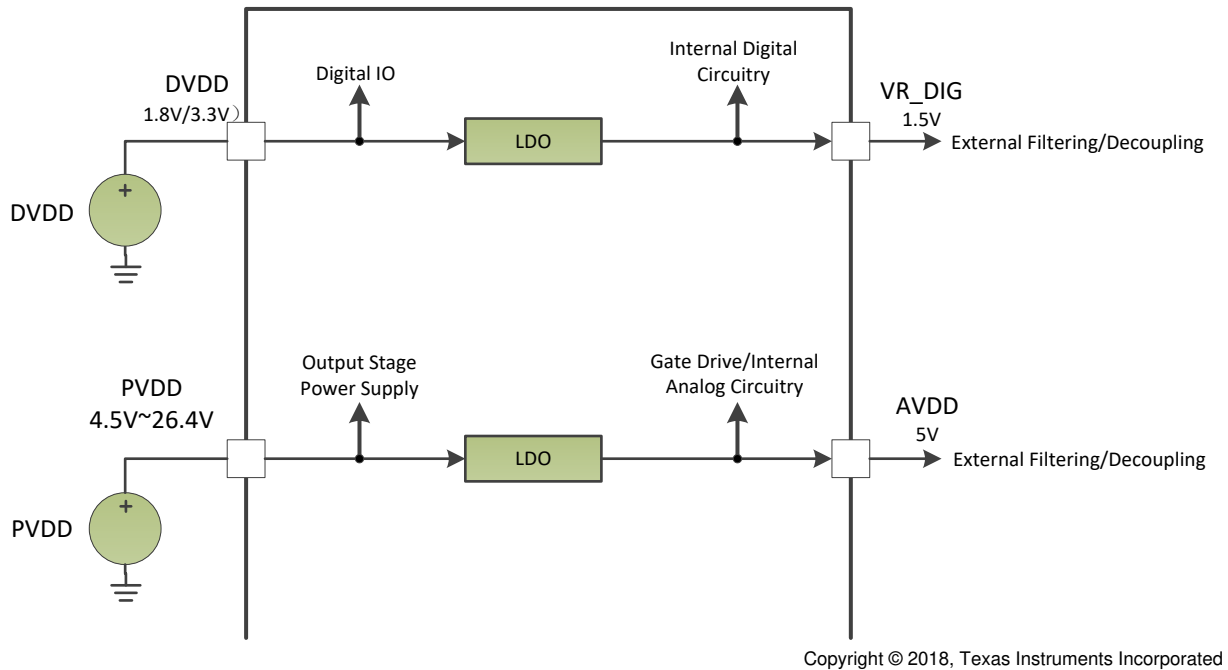


Fig 123. Power Supply Function Block Diagram

### 12.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in Fig 123, it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *Application and Implementation* section and the *Layout Example* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5806M device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the VR\_DIG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

## 12.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5806MEVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5806M device [Application and Implementation](#). Lack of proper decoupling, like that shown in the [Application and Implementation](#), results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. An AVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5806M internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

## 13 Layout

### 13.1 Layout Guidelines

#### 13.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the [Layout Example](#) section. These examples represent exemplary baseline balance of the engineering trade-offs involved with laying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the [Layout Example](#) section and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

#### 13.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD and PVDD. However, the capacitors on the PVDD net for the TAS5806M device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only does placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5806M device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the [Layout Example](#) section.

#### 13.1.3 Optimizing Thermal Performance

Follow the layout example shown in the [Figure 124](#) to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

##### 13.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5806M device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5806M device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5806M device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5806M device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane



## Layout Guidelines (continued)

from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

### 13.1.3.2 Stencil Pattern

The recommended drawings for the TAS5806M device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

---

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

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#### 13.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5806M device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5806M device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5806M device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the [Layout Example](#) section, this interface can benefit from improved thermal performance.

---

注

Vias can obstruct heat flow if they are not constructed properly.

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More notes on the construction and placement of vias are as follows:

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drill must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the [Layout Example](#) section.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5806M device to open up the current path to and from the device.

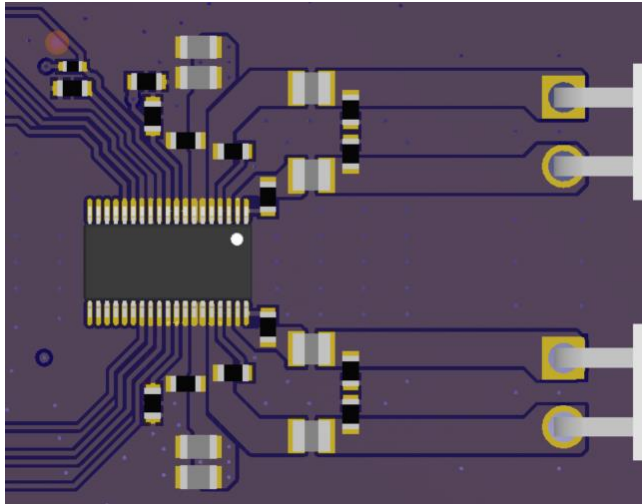
#### 13.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to

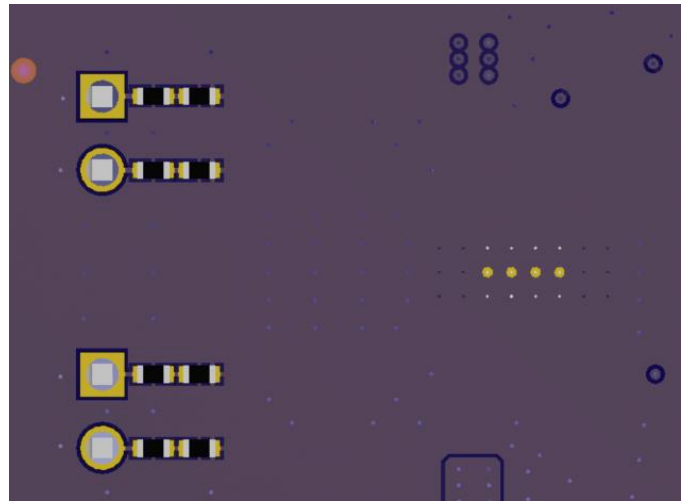
### Layout Guidelines (continued)

manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

### 13.2 Layout Example



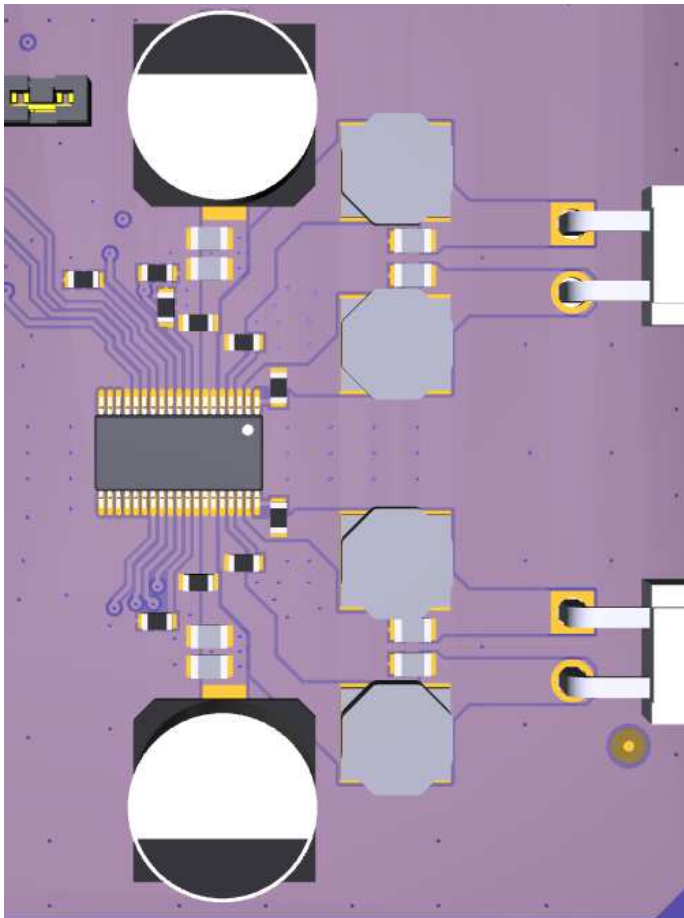
Top Layer 3D layout  
(Output Filter = Ferrite Bead + Capacitor)



Bot Layer 3D layout  
(Output Filter = Ferrite Bead + Capacitor)

✕ 124. 2.0 (Stereo BTL with Ferrite bead as the output filter) 3-D View

**Layout Example (continued)**



Top Layer 3D layout  
(Output Filter = Inductor + Capacitor)



Bot Layer 3D layout  
(Output Filter = Inductor + Capacitor)

**图 125. 2.0 (Stereo BTL with Inductor as the output filter) 3-D View**

## 14 デバイスおよびドキュメントのサポート

### 14.1 ドキュメントのサポート

#### 14.1.1 関連資料

関連資料については、以下を参照してください。

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#### 14.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 14.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 14.4 商標

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#### 14.5 静電気放電に関する注意事項



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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

#### 14.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5806MDCPR	ACTIVE	HTSSOP	DCP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5806M	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5806MDCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5806MDCPR	HTSSOP	DCP	38	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

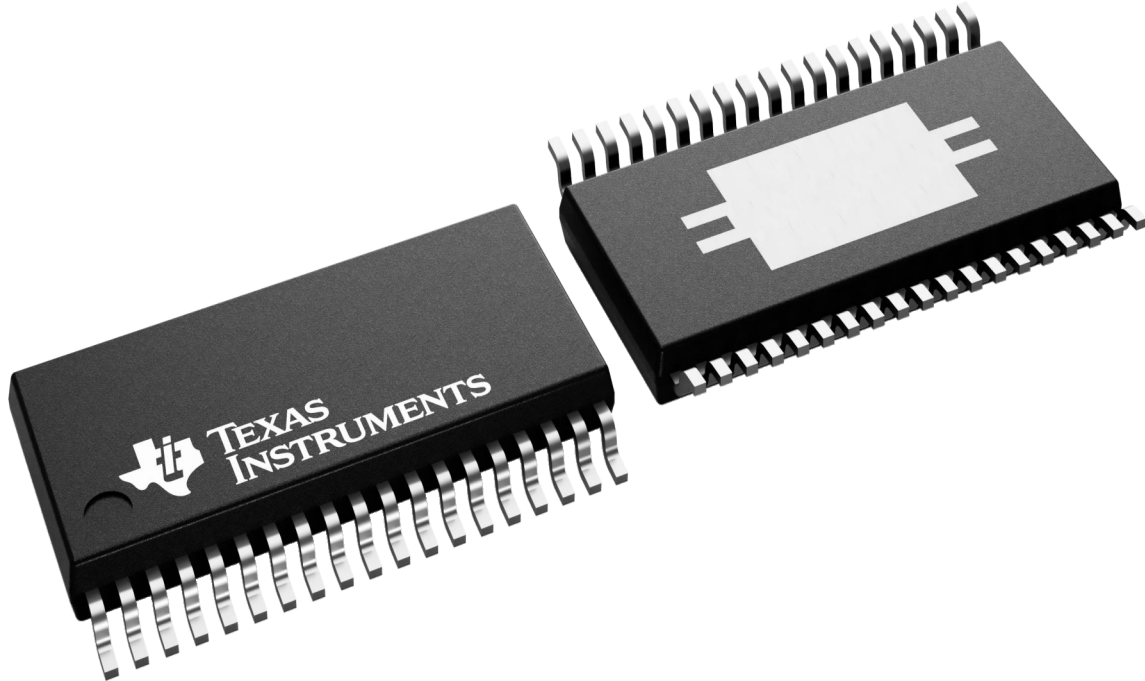
**DCP 38**

**PowerPAD TSSOP - 1.2 mm max height**

4.4 x 9.7, 0.5 mm pitch

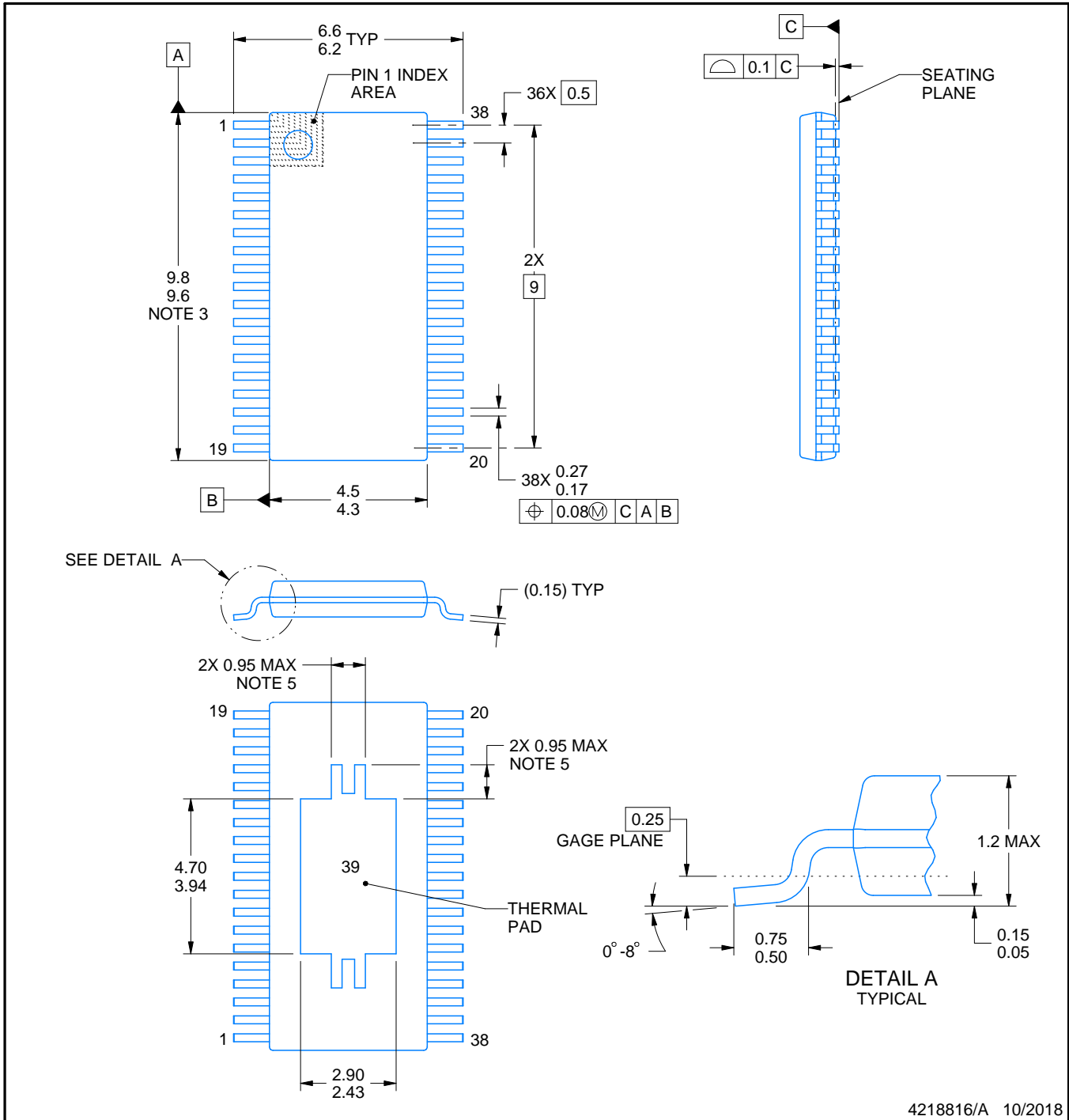
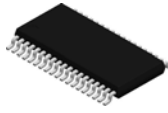
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224560/B





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NOTES:

PowerPAD is a trademark of Texas Instruments.

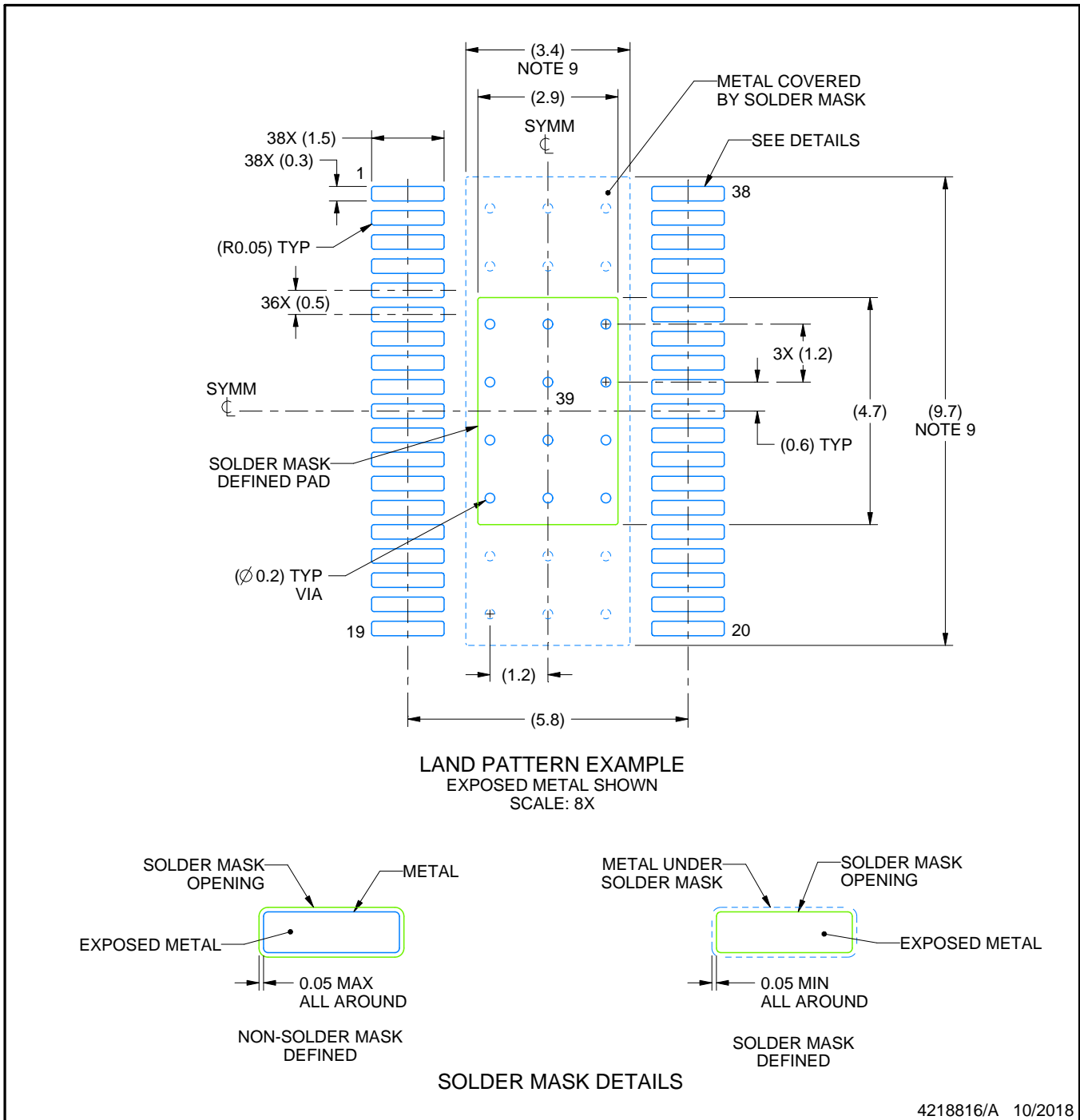
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

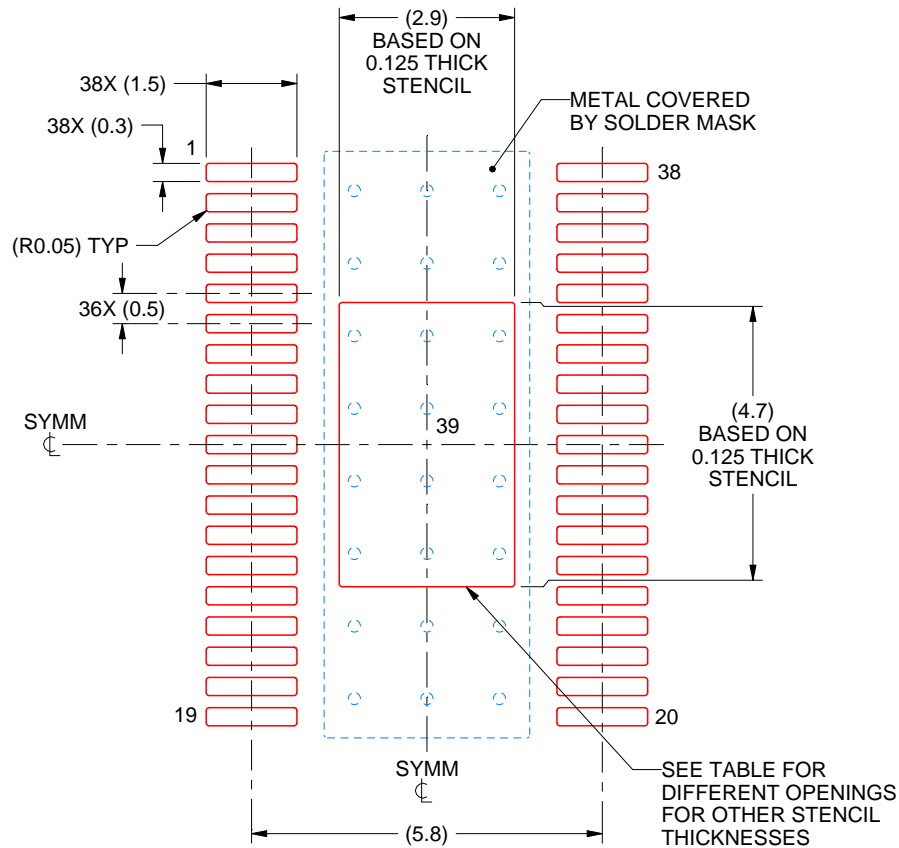
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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