

TCA9617B レベル変換 FM+ I²C バス リピータ

1 特長

- 2 チャンネルの双方向 I²C バッファ
- Standard Mode、Fast Mode (400kHz)、Fast Mode+ (1MHz) の I²C 動作をサポート
- A 側の動作電源電圧範囲: 0.8V~5.5V
- B 側の動作電源電圧範囲: 2.2V~5.5V
- 0.8V から 5.5V および 2.2V から 5.5V への電圧レベル変換
- フットプリントと機能において TCA9517 を代替可能
- アクティブ HIGH のリピータ イネーブル入力
- オープンドレインの I²C I/O
- 5.5V 許容の I²C およびイネーブル入力に対応
- ロックアップの発生しない動作
- 電源オフ時に高インピーダンスになる I²C バスピン
- デバイス全体で、クロック ストレッチングと複数マスタの調停をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
 - 人体モデルで 4000V
 - 荷電デバイス モデルで 1500V

2 アプリケーション

- サーバー
- ルーター (テレコム スイッチング機器)
- 産業用機器
- 多くの I²C ターゲットや長い PCB 配線を持つ製品

3 概要

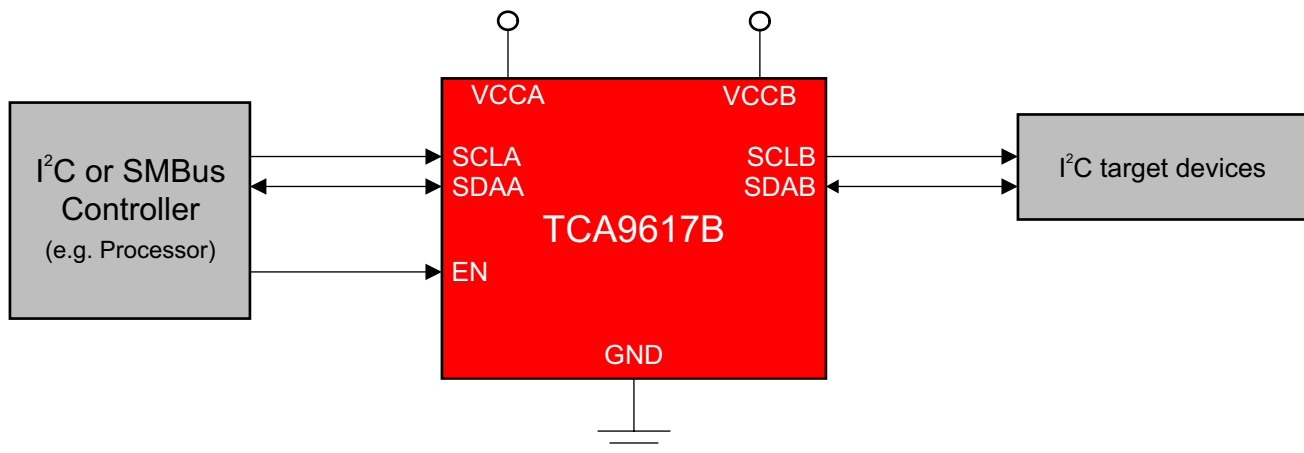
TCA9617B は、BiCMOS のデュアル双方向バッファで、I²C バスおよび SMBus システム用に設計されています。混在モード アプリケーションで、低電圧 (最低 0.8V) とより高い電圧 (2.2V~5.5V) との間の双方向電圧レベル変換 (昇圧変換/降圧変換) を行います。このデバイスにより、I²C および同様のバス システムを拡張でき、レベル シフト時にも性能劣化を防ぐことができます。

TCA9617B は、I²C バス上でシリアル データ (SDA) 信号とシリアル クロック (SCL) 信号の両方をバッファするため、容量が 550pF の 2 つのバスを、I²C アプリケーション内で接続できます。このデバイスを使って電圧や容量のバスを 2 つに分離することもできます。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
TCA9617B	VSSOP (8)	3mm×3mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



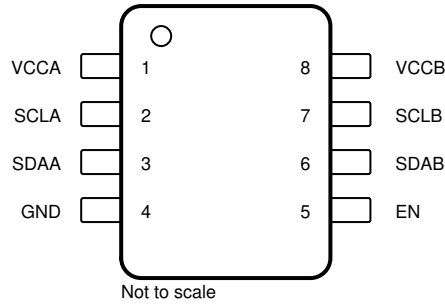
概略回路図



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4 Pin Configuration and Functions




**4-1. DGK Package, 8-Pin VSSOP
(Top View)**

表 4-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
VCCA	1	A-side supply voltage (0.8V to 5.5V)
SCLA	2	I ² C SCL line, A side. Connect to V _{CCA} through a pull-up resistor.
SDAA	3	I ² C SDA line, A side. Connect to V _{CCA} through a pull-up resistor.
GND	4	Supply ground
EN	5	Active-high repeater enable input. Internally connected to V _{CCB} through a weak pull-up resistor.
SDAB	6	I ² C SDA line, B side. Connect to V _{CCB} through a pull-up resistor.
SCLB	7	I ² C SCL line, B side. Connect to V _{CCB} through a pull-up resistor.
VCCB	8	B-side and device supply voltage (2.2V to 5.5V)

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CCB}	Supply voltage range		-0.5	6.5	V
V _{CCA}	Supply voltage range		-0.5	6.5	V
V _I	Enable input voltage range ⁽²⁾		-0.5	6.5	V
V _{IO}	I ² C bus voltage range ⁽²⁾		-0.5	6.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CCA}	Supply voltage, A-side bus		0.8	V _{CCB}	V
V _{CCB}	Supply voltage, B-side bus		2.2	5.5	V
I _{OLA}	Low-level output current			30	mA
I _{OLB}	Low-level output current		0.1	30	mA
T _A	Ambient temperature		-40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DGK	UNIT
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	171.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	77.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	107.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	105.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

V_{CCB} = 2.2V to 5.5V, GND = 0V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V _{CCB}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IK}	Input clamp voltage		I _I = -18mA	2.2V to 5.5V	-1.2		0	V	
V _{OL}	Low-level output voltage	SDAB, SCLB	I _{OL} = 100μA or 30mA, V _{ILA} = 0V	2.2V to 5.5V	0.48	0.53	0.58	V	
		SDAA, SCLA	I _{OL} = 30mA				0.1		0.23
V _{IH}	High-level input voltage	SDAA, SCLA		2.2V to 5.5V	0.7 × V _{CCA}		5.5	V	
		SDAB, SCLB					0.7 × V _{CCA}		5.5
		EN					0.7 × V _{CCB}		5.5
V _{IL}	Low-level input voltage	SDAA, SCLA		2.2V to 5.5V			0.3 × V _{CCA}	V	
		SDAB, SCLB					0.4		
		EN					0.3 × V _{CCB}		
I _{CCA}	Quiescent supply current for V _{CCA}		Both channels low, SDAA = SCLA = GND and I _{OLB} = 100μA, or SDAA = SCLA = open and SDAB = SCLB = GND	2.2V to 5.5V			13	μA	
I _{CCB}	Quiescent supply current		Both Channels high, SDAA = SCLA = V _{CCA} B-side pulled up to V _{CCB} with pull-up resistors	2.2V to 5.5V		4.5	7	mA	
			Both channels low, SDAA = SCLA = GND, I _{OLB} = 100μA	5.5V		5.7	8.1		

5.5 Electrical Characteristics (続き)

$V_{CCB} = 2.2V$ to $5.5V$, $GND = 0V$, $T_A = -40^\circ C$ to $85^\circ C$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current	SDAB, SCLB	$V_I = V_{CCB}$	2.2V to 5.5V	-1		1	μA
			$V_I = 0.2V, EN = 0$		-10		10	
			$V_I = V_{CCB} - 0.2V$		-1		1	
			$V_I = 5.5V, V_{CCA} = 0V$	0V	-10		10	
		SDAA, SCLA	$V_I = V_{CCA}$	2.2V to 5.5V	-1		1	
			$V_I = 0.2V, EN = 0$		-10		10	
			$V_I = V_{CCA} - 0.2V$		-1		1	
			$V_I = 5.5V, V_{CCA} = 0V$	0V	-10		10	
		EN	$V_I = V_{CCB}$		-1		1	
			$V_I = 0.2V$		-25			
C_I	Input capacitance	EN	$V_I = 3V$ or $0V$	3.3V			7	pF
C_{IO}	Input/output capacitance	SCLA, SDAA	$V_I = 3V$ or $0V$	3.3V			9	pF
			$V_I = 3V$ or $0V$	0V			9	
		SCLB, SDAB	$V_I = 3V$ or $0V$	3.3V			14	
			$V_I = 3V$ or $0V$	0V			14	

(1) All typical values are at $T_A = 25^\circ C$.

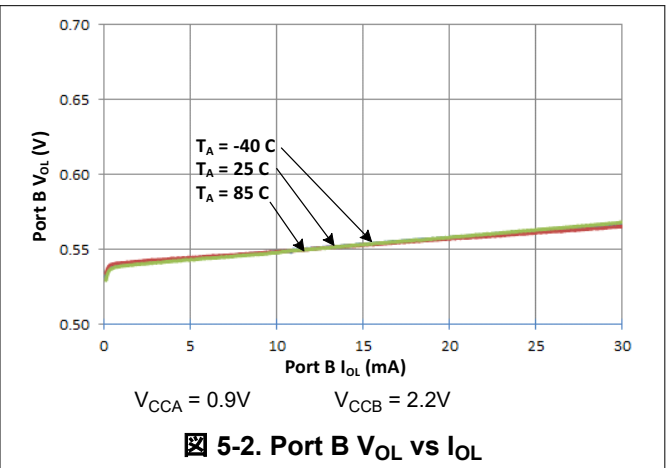
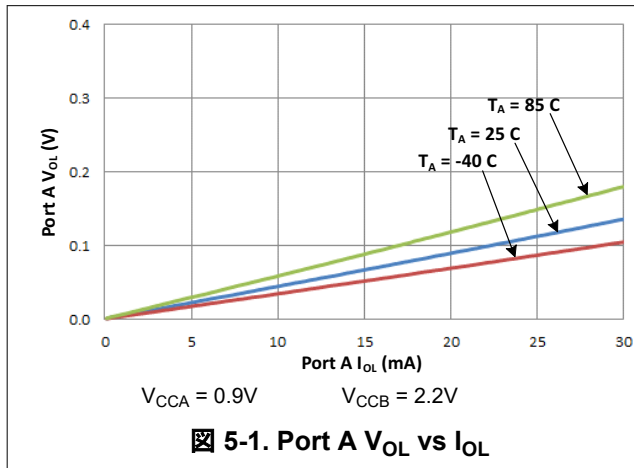
5.6 Timing Requirements

$V_{CCA} = 0.8V$ to $5.5V$, $V_{CCB} = 2.2V$ to $5.5V$, $GND = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ (unless otherwise noted)^{(1) (2) (3)}

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay	SDAB, SCLB	SDAA, SCLA		35		90	ns
t_{PLH}	Propagation delay	SDAA, SCLA	SDAB, SCLB	$V_{CCB} \leq 3V$	50		137	ns
t_{PLH}	Propagation delay	SDAA, SCLA	SDAB, SCLB	$V_{CCB} > 3V$	59		250	ns
t_{PHL}	Propagation delay	SDAB, SCLB	SDAA, SCLA		32		144	ns
t_{PHL}	Propagation delay	SDAA, SCLA	SDAB, SCLB		28		140	ns
$t_{TLH}^{(4)}$	Transition time	B side	30%	70%	88		ns	
		A side			37			
t_{THL}	Transition time	B side	70%	30%	5.40	32		ns
		A side			1.40	40		
$t_{su,en}^{(5)}$	Setup time, EN high before Start condition				100			ns

- Times are specified with loads of $240 \Omega \pm 1\%$ and $400 pF \pm 10\%$ on B-side and $240 \Omega \pm 1\%$ and $200 pF \pm 10\%$ on A-side. Different load resistance and capacitance alter the rise time, thereby changing the propagation delay and transition times.
- Times are specified with A-side signals pulled up to V_{CCA} and B-side signals pulled up to V_{CCB} .
- Typical values were measured with $V_{CCA} = 0.9 V$ and $V_{CCB} = 2.5 V$ at $T_A = 25^{\circ}C$, unless otherwise noted.
- t_{TLH} is determined by the pull-up resistance and load capacitance
- EN should change state only when the global bus and the repeater port are in an idle state

5.7 Typical Characteristics



Parameter Measurement Information

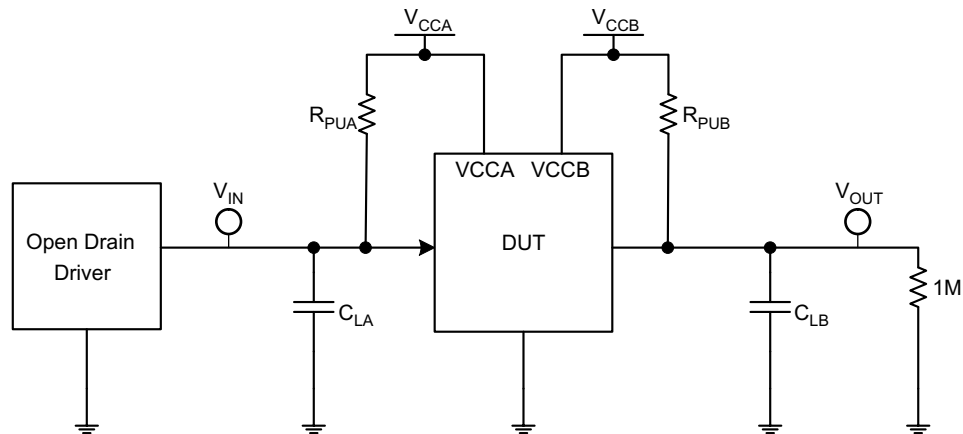


图 6-1. Test Circuit for Open-Drain Output from A to B

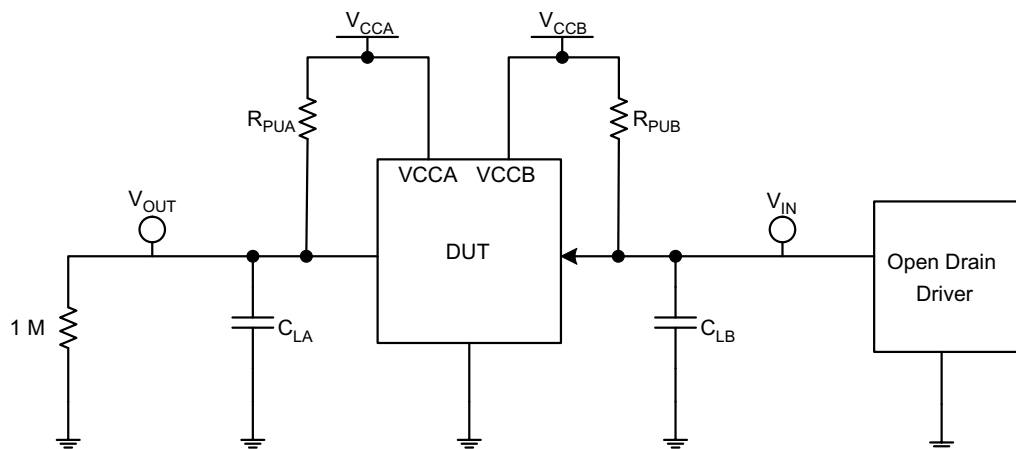


图 6-2. Test Circuit for Open-Drain Output from B to A

- $V_{CCA} = 0.9V$
- $V_{CCB} = 2.5V$
- $R_{PUA} = R_{PUB} = 240\Omega$ on the A-side and the B-side
- $C_{LA} = 200pF$ on A-side and $C_{LB} = 400pF$ on B-side (includes probe and jig capacitance)
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_O = 50\Omega$, $slew\ rate \geq 1V/ns$
- The outputs are measured one at a time, with one transition per measurement.

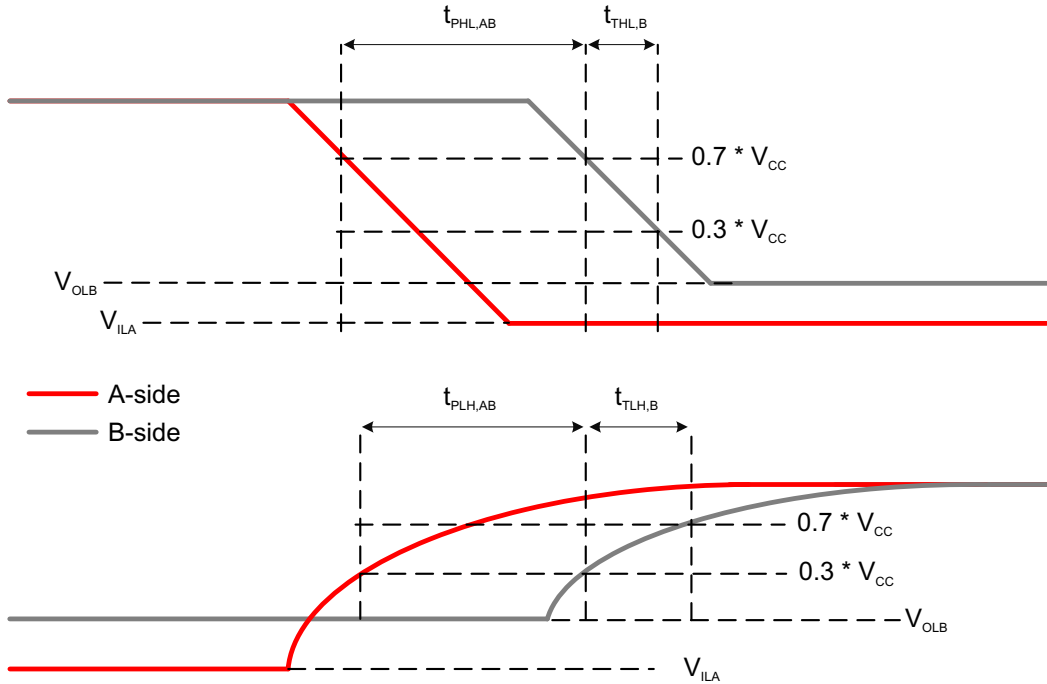


Figure 6-3. Propagation Delay And Transition Times (A to B)

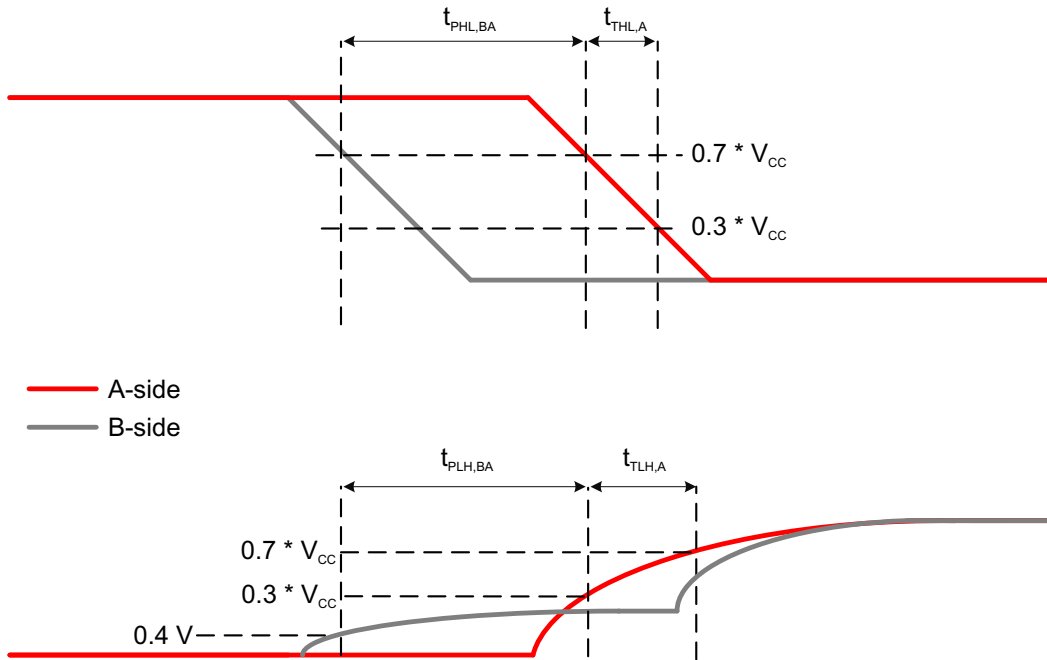


Figure 6-4. Propagation Delay And Transition Times (B to A)

6 Detailed Description

6.1 Overview

The TCA9617B is a BiCMOS dual bidirectional buffer intended for I²C bus and SMBus systems. As with the standard I²C system, pull-up resistors are required to provide the logic high levels on the buffered bus. The TCA9617B has standard open-drain configuration of the I²C bus. The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. The device is designed to work with Standard mode, Fast mode and Fast Mode+ I²C devices. The SCL and SDA lines shall be at high-impedance when either one of the supplies is powered off.

The TCA9617B B-side drivers operate from 2.2V to 5.5V. The output low level for this internal buffer is approximately 0.5V, but the input voltage must be below V_{IL} when the output is externally driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design on the B side prevents TCA9617B from being used in series with another TCA9617B B-side or other buffers that incorporate a static or dynamic offset voltage. This is because these devices do not recognize buffered low signals as a valid low and do not propagate the signal as a buffered low again.

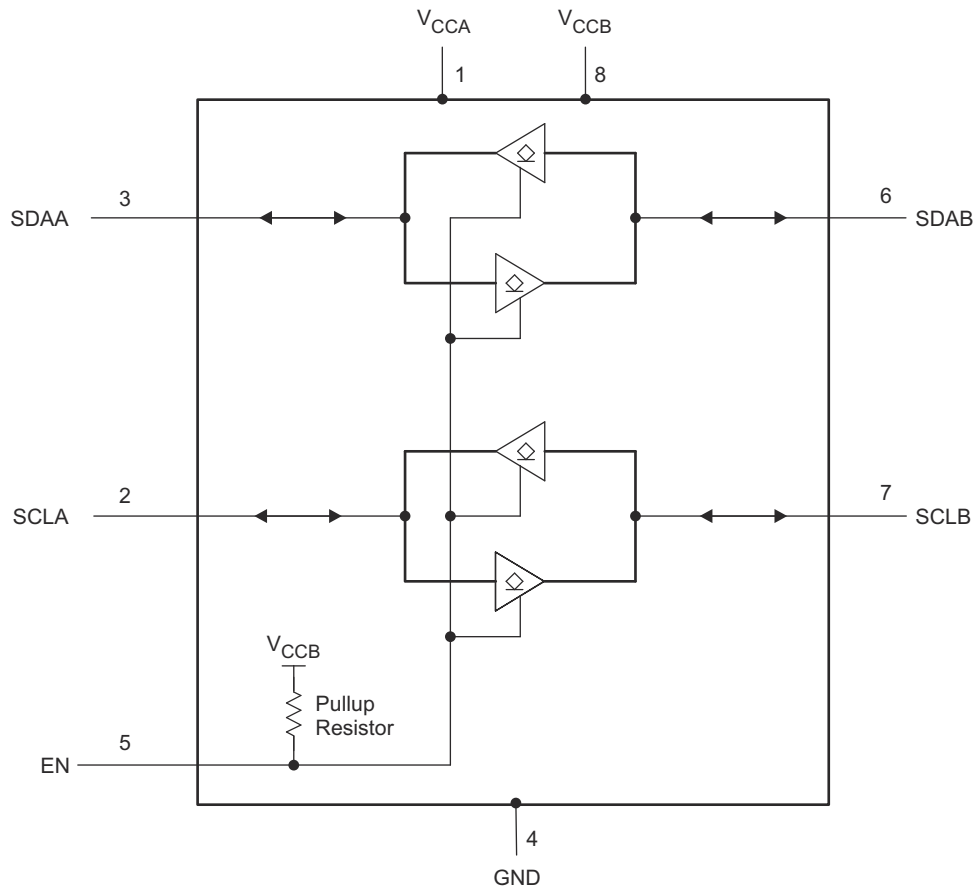
The TCA9617B A-side drivers operate from 0.8V to 5.5V and do not have the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0V low on the A side, which accommodates smaller voltage swings of low-voltage logic. The output pull-down on the A side drives a hard low, and the input level is set to 30% of V_{CCA} to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.8V.

The A side of two or more TCA9617B can be connected together to allow a star topology, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static or dynamic offset voltage. Multiple TCA9617B can be connected in series, A side to B side, with no buildup in offset voltage with only time-of-flight delays to consider.

The TCA9617B includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2V and V_{CCA} is above 0.7V. V_{CCA} is only used to provide references for the A-side input comparators and the power-good-detect circuit. The TCA9617B internal circuitry and all I/Os are powered by the V_{CCB} pin.

After power up and with the EN high, the A side falling below 30% of V_{CCA} turns on the corresponding B-side driver (either SDA or SCL) and drives the B-side down momentarily to 0V before settling to approximately 0.5V. When the A-side rises above 30% of V_{CCA} , the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. If the B side falls first and goes below 0.4V, the A-side driver is turned on and drives the A-side to 0V. When the B-side rises above 0.45V, the A-side pull-down driver is turned off and the external pull-up resistor pulls the pin high.

6.2 Functional Block Diagram





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6.3 Feature Description

6.3.1 Bidirectional Level Translation

The TCA9617B can provide bidirectional voltage level translation (up-translation and down-translation) between low voltages (down to 0.8V) and higher voltages (2.2V to 5.5V) in mixed-mode applications.

6.3.2 Low to High Transition Characteristics

 6-2 depicts the offset voltage on the B side of the device. As shown in  6-2 the target releases and the B-side rises, and rises to 0.5V and stays there until the A-side rises above 30% of V_{CCA} . This effect can cause the low level signal to have a *pedestal*. Once the voltage on the A-side crosses 30% of V_{CCA} , the B-side begins to rise to V_{CCB} .

Due to nature of the B-side pedestal and the static offset voltage, there is a slight overshoot as the B-side rises from being externally driven low to the 0.5V offset. The TCA9617B is designed to control this behavior provided the system is designed with rise times greater than 20ns. Therefore; care must be taken to limit the pull-up strength when devices with rise time accelerators are present on the B side. Excessive overshoot on the B-side pedestal can cause devices with rise time accelerators to trip prematurely if the overshoot is more than accelerator thresholds.

6.3.3 High-to-Low Transition Characteristics

When the A side of the bus is driven to 30% of V_{CCA} , the B side driver turns on. This drives the B-side to 0V for a short period (see Figure 6-2), and then the B-side rises to the static offset voltage of 0.5V (V_{OL} of TCA9617B). This effect, called an inverted pedestal, allows the B-side to drive to logic low much faster than driving to the static offset. Driving to the static offset voltage requires that the fall time be slowed to prevent ringing.

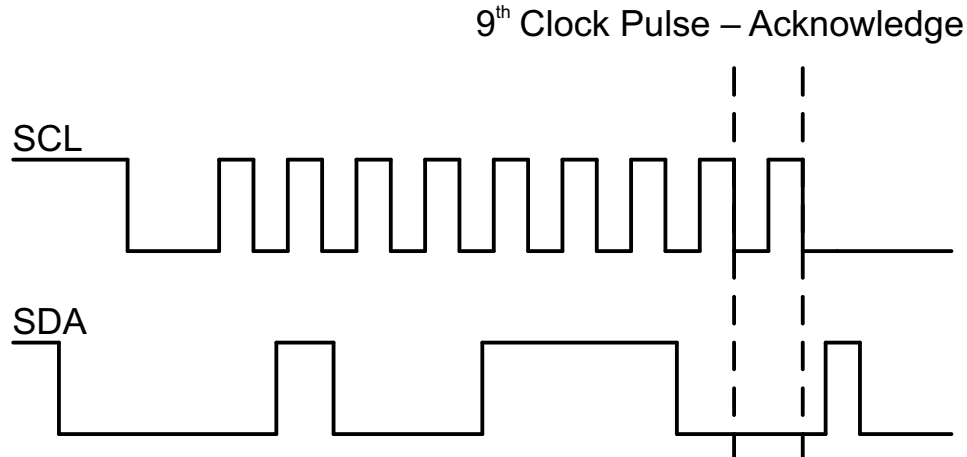


Figure 6-1. Bus A (0.8V to 5.5V Bus) Waveform

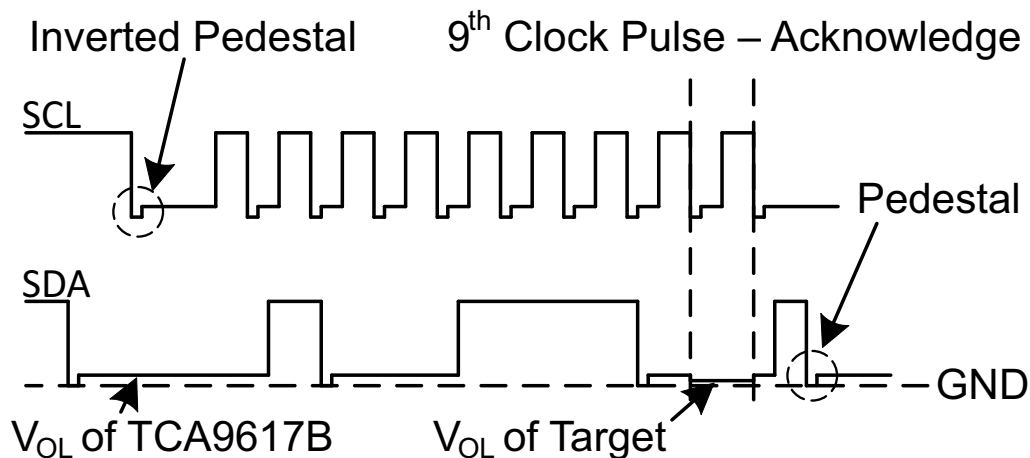


Figure 6-2. Bus B (2.2V to 5.5V Bus) Waveform

6.4 Device Functional Modes

The TCA9617B has an active-high enable (EN) input with an internal pull-up to V_{CCB} , which allows the user to select when the repeater is active. This can be used to separate a misbehaving target on power-up reset. The EN must never change state during an I²C operation. Disabling during a bus operation can hang the bus. Enabling part way through the bus cycles can confuse the I²C parts being enabled. The EN input must change state only when the global bus and repeater port are in the idle state to prevent system failures.

Table 6-1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

A typical application is shown in [図 7-1](#). In this example, the system controller is running on a 0.9V I²C bus, and the target is connected to a 2.5V bus. Both buses are running at 400kHz. Decoupling capacitors are required, but are not shown in [図 7-6](#) for simplicity.

The TCA9617B is 5V tolerant so no additional circuits are required to translate between 0.8V to 5.5V bus voltages and 2.7V to 5.5V bus voltages.

When the A side of the TCA9617B is pulled low by a driver on the I²C bus, a comparator detects the falling edge when the signal level goes below 30% of V_{CCA} and cause the internal driver on the B side to turn on. The B-side is first pulled down to 0V, and then settles to 0.5V. When the B side of the TCA9617B falls below 0.4V, the TCA9617B detects the falling edge, turn on the internal driver on the A side and pull the A-side pin down to ground.

On the B-side bus of the TCA9617B, the clock and data lines has a positive offset from ground equal to the V_{OL} of the TCA9617B. After the eighth clock pulse, the data line is pulled to the V_{OL} of the target device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver of the TCA9617B for a short delay (approximately 0.5V), while the A-side bus rises above 30% of V_{CCA} and then continues high.

Although the TCA9617B has a single application, the device can exist in multiple configurations. [図 7-1](#) shows the standard configuration for the TCA9617B. Multiple TCA9617Bs can be connected either in star configuration ([図 7-4](#)) or in series configuration ([図 7-5](#)). The design requirements, detailed design procedure, and application curves in [セクション 7.2.1](#) are valid for all three configurations.

7.2 Typical Application

7.2.1 Standard Application

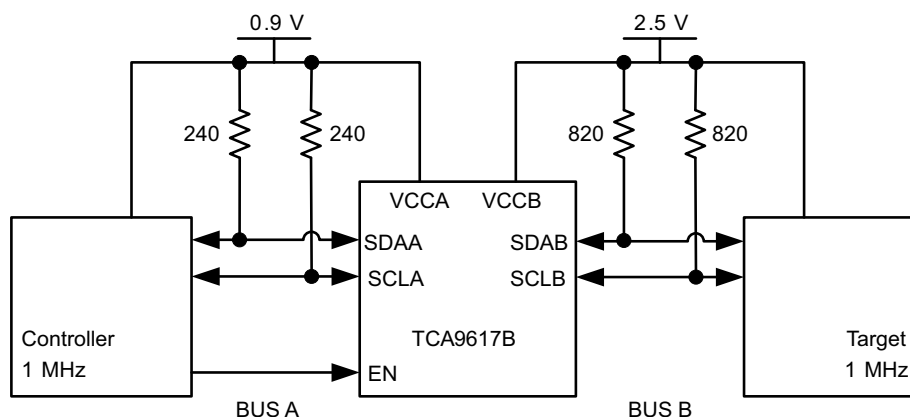


図 7-1. Bidirectional Voltage Level Translator

7.2.1.1 Design Requirements

For the level-translating application, the following must be true:

- $V_{CCA} = 0.8V$ to $5.5V$
- $V_{CCB} = 2.2V$ to $5.5V$
- $V_{CCA} \leq V_{CCB}$
- $I_{OL} > I_O$

7.2.1.2 Detailed Design Procedure

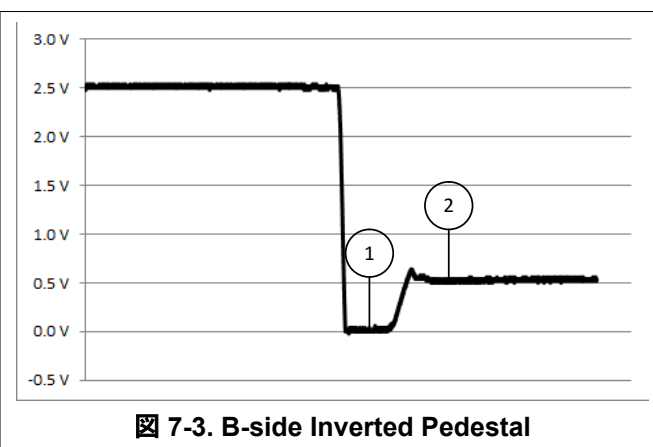
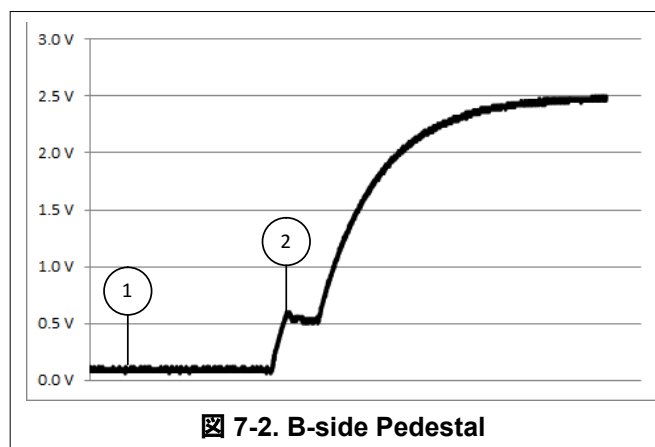
7.2.1.2.1 Pullup Resistor Sizing

For the TCA9617B to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level ($0.4V$). This means that the V_{OL} of any device on the B-side must be below $0.4V$ for proper operation.

The V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistor value. The pull-up resistor on the B-side must be carefully selected to make sure the logic levels are transferred correctly to the A-side.

The B-side pull-up resistor sizing must also make sure that the rise time is greater than $20ns$. Shorter rise times increase the pedestal overshoot shown in [Figure 7-2](#).

7.2.1.3 Application Curves



7.2.2 Star Application

Multiple A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

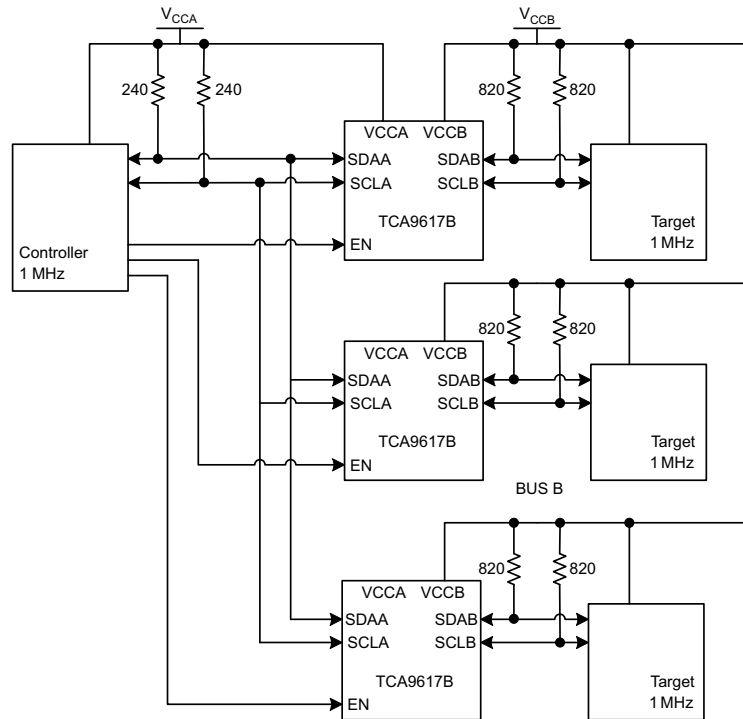


図 7-4. Typical Star Application

7.2.2.1 Design Requirements

Refer to [セクション 7.2.1.1](#).

7.2.2.2 Detailed Design Procedure

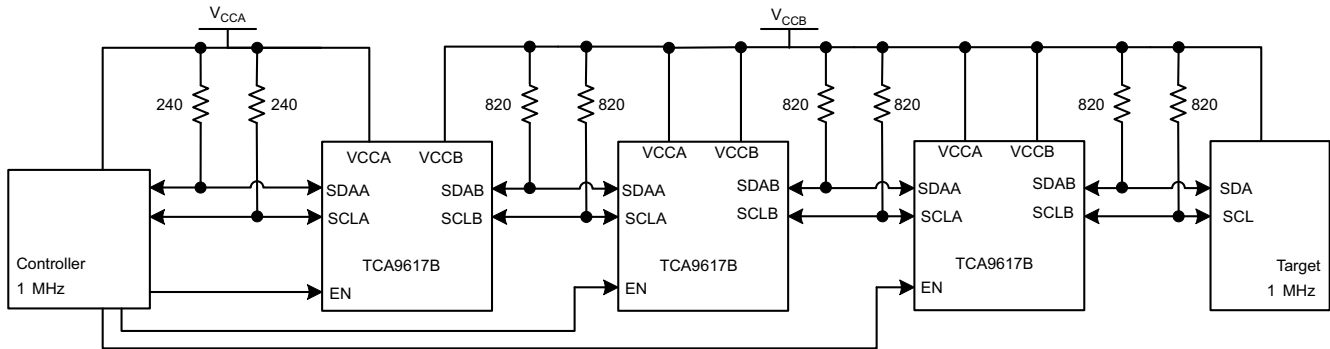
Refer to [セクション 7.2.1.2](#).

7.2.2.3 Application Curves

Refer to [セクション 7.2.1.3](#).

7.2.3 Series Application

Multiple TCA9617Bs can be connected in series as long as the A side is connected to the B side. I²C bus target devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.



7-5. Typical Series Application

7.2.3.1 Design Requirements

Refer to [セクション 7.2.1.1](#).

7.2.3.2 Detailed Design Procedure

Refer to [セクション 7.2.1.2](#).

7.2.3.3 Application Curves

Refer to [セクション 7.2.1.3](#).

7.3 Power Supply Recommendations

For VCCA, an 0.8V to 5.5V power supply is required. For VCCB, a 2.2V to 5.5V power supply is required.

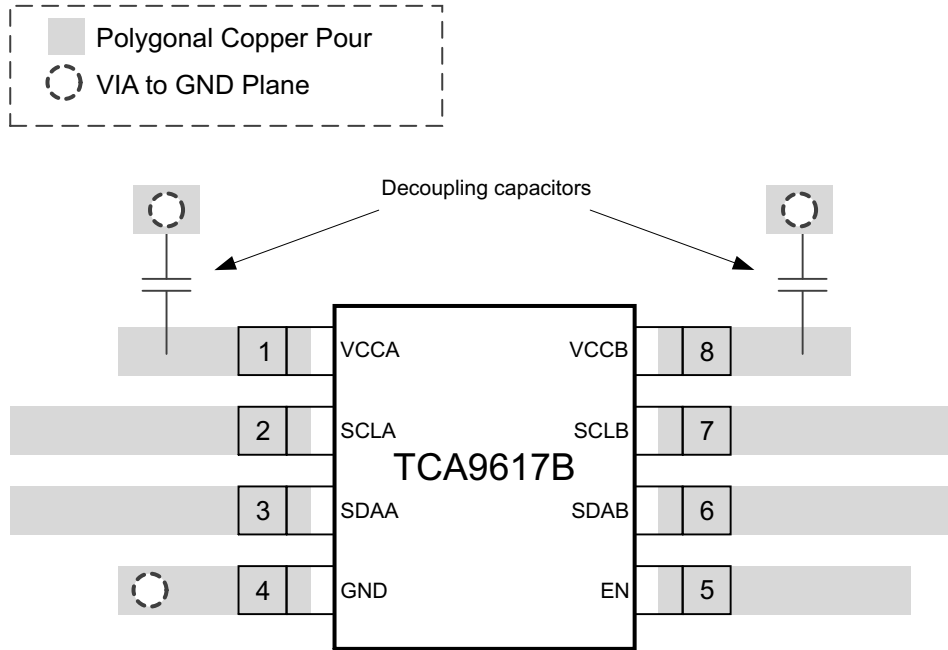
Standard decoupling capacitors are recommended. These capacitors typically range from 0.1 μ F to 1 μ F, but the value of the capacitance depends on the frequencies of noise from the power supply.

7.4 Layout

7.4.1 Layout Guidelines

The recommended decoupling capacitors must be placed as close to the VCCA and VCCB pins of the TCA9617B as possible.

7.4.2 Layout Example



☒ 7-6. Layout Schematic

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2024) to Revision E (October 2024)	Page
• Updated Tape and Reel Information W: 9.2mm to 12mm.....	20

Changes from Revision C (January 2024) to Revision D (September 2024)	Page
• Updated Tape and Reel Information.....	20

Changes from Revision B (December 2018) to Revision C (January 2024)	Page
• すべての古い用語をコントローラおよびターゲットに変更.....	1
• Added weak pull-up resistor information on pin EN	3
• Changed abs max voltages from 7V to 6.5V.....	4
• Changed the Thermal Information for 8 DGK.....	5
• Changed V_{IK} MAX value of -1.2V to a MIN value.....	5
• Changed T_{PLH} (B to A) by removing typical value.....	7
• Changed T_{PLH} (A to B) for $V_{CCB} \leq 3V$ by changing min value from 59ns to 50ns and removing typical value.....	7
• Changed T_{PLH} (A to B) for $V_{CCB} > 3V$ by removing typical value.....	7
• Changed T_{PHL} (B to A) by changing min value from 69ns to 32ns and removing typical value.....	7
• Changed T_{PHL} (A to B) by changing min value from 68ns to 28ns and removing typical value.....	7
• Changed T_{THL} (B side) by changing max value from 13.8ns to 32ns and removing typical value.....	7
• Changed T_{THL} (B side) by changing max value from 11.3ns to 40ns and removing typical value.....	7
• Changed $0.3V_{CCA}$ to: <i>30% of V_{CCA} in the Overview</i>	10
• Changed A side falling below $0.7V_{CCB}$ to: <i>A side falling below 30% of V_{CCA}</i>	10
• Changed goes below $0.7V_{CCB}$ to: <i>goes below 0.4V</i>	10
• Changed $0.3V_{CCA}$ to: <i>30% of V_{CCA} in the Low to High Transition Characteristics</i>	11
• Deleted <i>Since the A-side does not have a static offset low voltage, no pedestal is seen on the A-side as shown in Fig 6-1</i>	11
• Changed $0.7V_{CCA}$ to <i>30% of V_{CCA} in the High-to-Low Transition Characteristics</i>	12
• Changed <i>isolate a badly behaved to separate a misbehaving in the Device Functional Modes</i>	12
• Changed $0.7V_{CCA}$ to <i>30% of V_{CCA} in the Application Information</i>	13
• Changed falls below 0.45V to: falls below 0.4Vt.....	13
• Changed (0.45V) to: (0.4V) in the <i>Pullup Resistor Sizing</i>	14

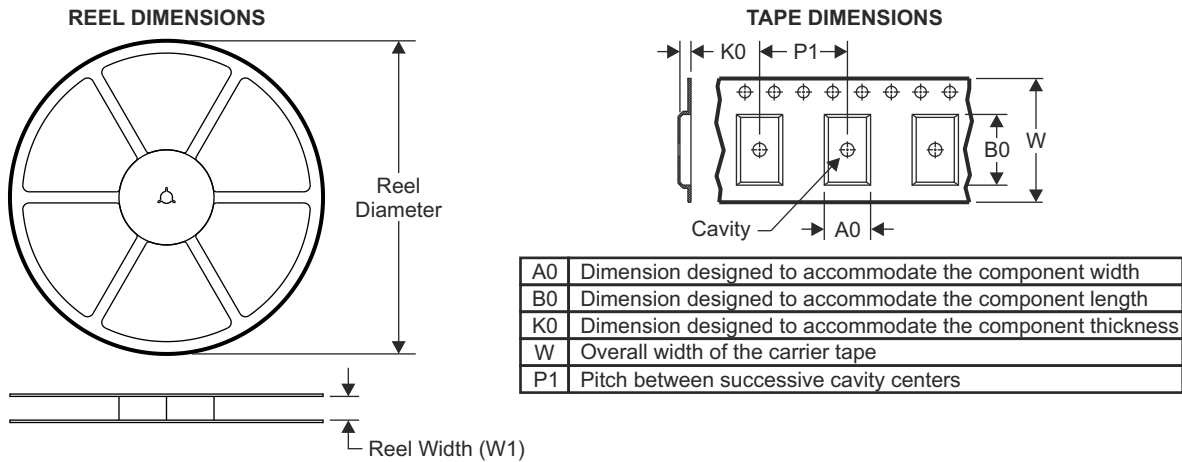
Changes from Revision A (December 2014) to Revision B (December 2018)	Page
• Changed the appearance of the DGK pin out image	3
• Changed $V_{CCA} < V_{CCB}$ To: $V_{CCA} \leq V_{CCB}$ in the Design Requirements list.....	14

Changes from Revision * (December 2014) to Revision A (December 2014)	Page
• 完全版の初回リリース.....	1

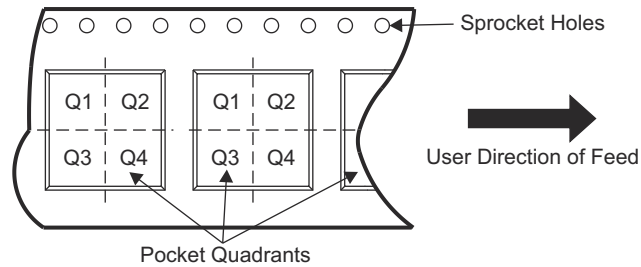
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

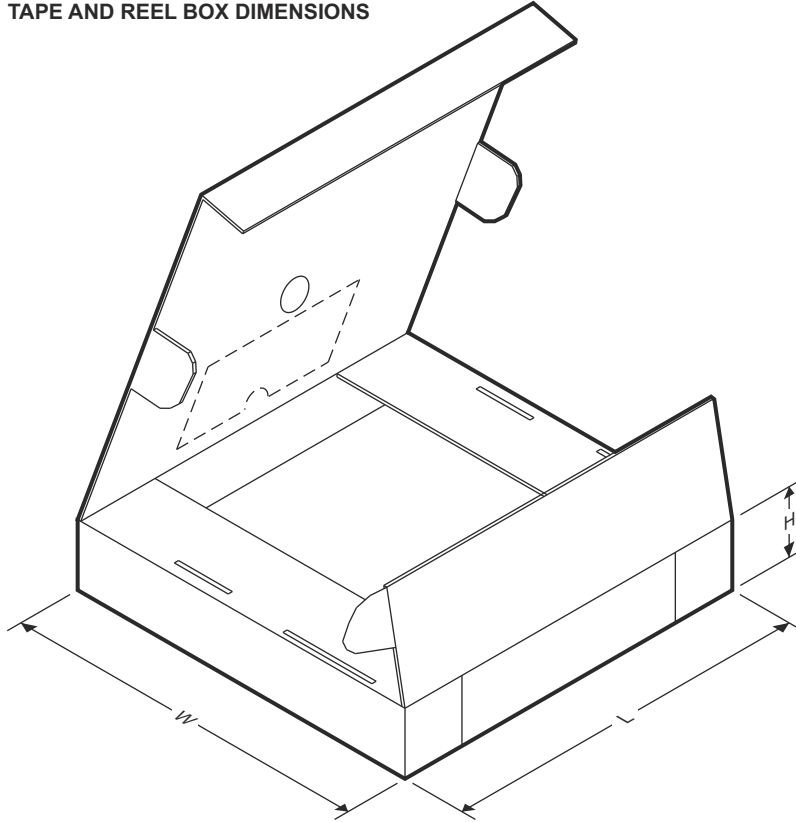


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9617BDGKR	VSSOP	DGK	8	2500	330	12.4	5.3	3.4	1.4	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9617BDGKR	VSSOP	DGK	8	2500	364	364	27

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9617BDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 85	ZBOK	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

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1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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