

TCAN104xAV-Q1 車載用、デュアル CAN FD トランシーバ、1.8V I/O 対応、スタンバイ・モード付き

1 特長

- AEC-Q100 (グレード 1): 車載アプリケーション認定済み
- 独立したモード制御を備えた 2 つの高速 CAN トランシーバ
- ISO 11898-2:2016 物理層規格の要件に適合
- 機能安全対応
 - 機能安全システム的设计に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5、8Mbps)
 - 短く対称的な伝搬遅延時間によりタイミング・マージンを強化
- I/O 電圧範囲: 1.7 V ~ 5.5 V
 - 1.8V、2.5V、3.3V、5V のアプリケーションをサポート
- 12V および 24V バッテリ・アプリケーションに対応
- レシーバ同相入力電圧: $\pm 12V$
- 保護機能:
 - バス・フォルト保護: $\pm 58V$
 - 低電圧保護
 - TXD ドミナント・タイムアウト (DTO)
 - 最小 9.2kbps のデータ・レート
 - サーマル・シャットダウン保護 (TSD)
- 動作モード:
 - 通常モード
 - リモート・ウェイクアップ要求をサポートする、低消費電力スタンバイ・モード
- 電源非接続時の最適化された挙動
 - バスおよびロジック・ピンは高インピーダンス (動作中のバス、アプリケーションに対して無負荷)
 - ホットプラグ対応: 電源オン/オフ時のバスおよび RXD 出力のグリッチ・フリー動作
- 接合部温度範囲: $-40^{\circ}C \sim 150^{\circ}C$
- SOIC (14) パッケージおよび自動光学検査 (AOI) 性能を向上させたリードレス VSON (14) パッケージ (4.5mm \times 3.0mm) で供給

2 アプリケーション

- 車両および輸送システム
 - 車体制御モジュール
 - 車載ゲートウェイ
 - 先進運転支援システム (ADAS)
 - インフォテインメント

3 概要

TCAN1046AV-Q1 および TCAN1048AV-Q1 (TCAN104xAV-Q1) は、ISO 11898-2:2016 高速 CAN (Controller Area Network) 仕様の物理層要件を満たすデュアル高速 CAN トランシーバです。

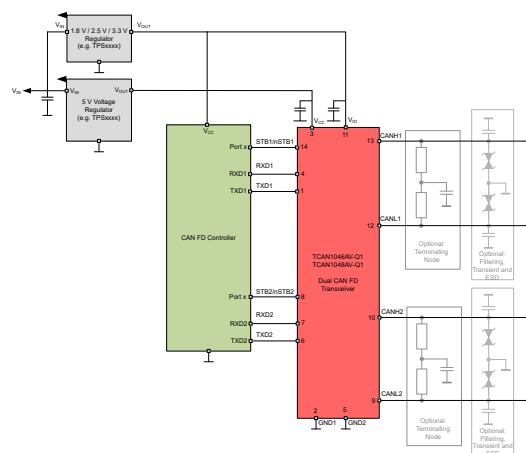
TCAN104xAV-Q1 トランシーバは Classical CAN ネットワークおよび最高 8 メガビット/秒 (Mbps) の CAN FD ネットワークの両方に対応しています。このデバイスは V_{IO} 端子による内部ロジック・レベル変換機能を内蔵しているため、トランシーバの I/O を 1.8V、2.5V、3.3V、5V のロジック I/O に直接接続できます。

2 つの CAN チャンネルは、スタンバイ・ピンによる独立したモード制御をサポートしています。したがって、他の CAN チャンネルの状態に影響を与えないで、各トランシーバを低消費電力状態であるスタンバイ・モードに移行できます。このデバイスは、スタンバイ・モードのとき、ISO 11898-2:2016 に定義されたウェイクアップ・パターン (WUP) によるリモート・ウェイクアップをサポートします。

製品情報

部品番号	パッケージ	本体サイズ (公称)
TCAN1046AV-Q1	VSON (14)	4.50mm \times 3.00mm
	SOIC (14)	8.95mm \times 3.91mm
	SOT-23 (14) ⁽¹⁾	4.20mm \times 1.90mm
TCAN1048AV-Q1	VSON (14)	4.50mm \times 3.00mm
	SOIC (14)	8.95mm \times 3.91mm

(1) 製品プレビュー



概略回路図



4 概要 (続き)

このトランシーバは、サーマル・シャットダウン (TSD)、TXD ドミナント・タイムアウト (DTO)、最高 $\pm 58V$ のバス・フォルト保護を含む多くの保護および診断機能も備えています。このデバイスは、電源低電圧またはフローティング・ピンのシナリオでフェイルセーフ動作を定義しています。

5 Device Comparison

表 5-1. Device Comparison Table

Part Number	Bus Fault Protection on both CAN Channels	Low Voltage I/O Logic Support	Standby (STB) Pin Mode
TCAN1046AV-Q1	$\pm 58 V$	Yes	Active-high
TCAN1048AV-Q1	$\pm 58 V$	Yes	Active-low

6 Pin Configuration and Functions

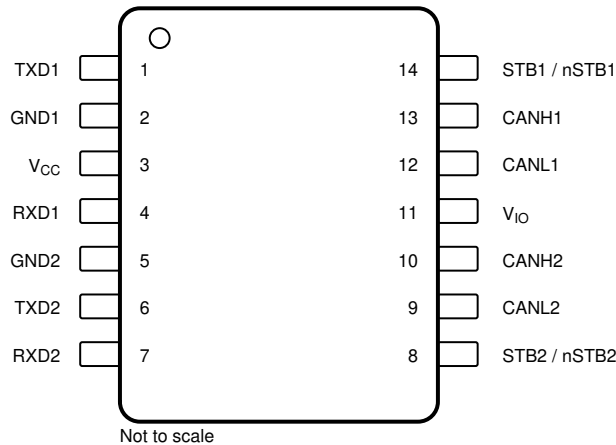


图 6-1. D Package , 14 Pin SOIC, Top View

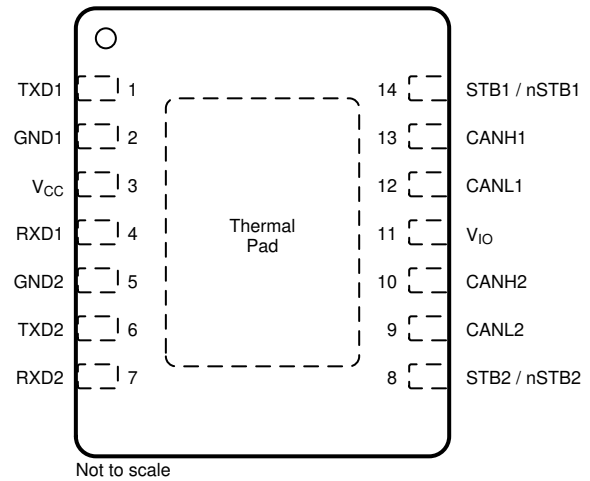


图 6-2. DMT Package, 14 Pin VSON, Top View

表 6-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input 1, integrated pull-up
GND1	2	GND	Ground connection
V _{CC}	3	Supply	5-V supply voltage
RXD1	4	Digital Output	CAN receive data output 1, tri-state when V _{IO} < UV _{VIO}
GND2	5	GND	Ground connection
TXD2	6	Digital Input	CAN transmit data input 2, integrated pull-up
RXD2	7	Digital Output	CAN receive data output 2, tri-state when V _{IO} < UV _{VIO}
STB2	8	Digital Input	Standby input 2 for mode control, integrated pull up (TCAN1046AV-Q1)
nSTB2			Standby input 2 for mode control, inverse logic with integrated pull down (TCAN1048V-Q1)
CANL2	9	Bus IO	Low-level CAN bus 2 input/output line
CANH2	10	Bus IO	High-level CAN bus 2 input/output line
V _{IO}	11	Supply	IO supply voltage
CANL1	12	Bus IO	Low-level CAN bus 1 input/output line
CANH1	13	Bus IO	High-level CAN bus 1 input/output line
STB1	14	Digital Input	Standby input 1 for mode control, integrated pull up (TCAN1046AV-Q1)
nSTB1			Standby input 1 for mode control, inverse logic with integrated pull down (TCAN1048AV-Q1)
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

7 Device and Documentation Support

7.1 Device Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system specification; however, reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources are helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

7.1.1 Device Nomenclature

CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016 High speed medium access unit (original High Speed CAN transceiver standard)
- ISO 11898-5 High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode).
- ISO 11898-6 High speed medium access unit with selective wake.
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- GMW3122: GM requirements for HS CAN
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps

EMC requirements:

- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for HS CAN

Conformance Test requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

7.2 Documentation Support

7.2.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 7-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TCAN1046AV-Q1	Click here	Click here	Click here	Click here	Click here
TCAN1048AV-Q1	Click here	Click here	Click here	Click here	Click here

7.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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7.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

7.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

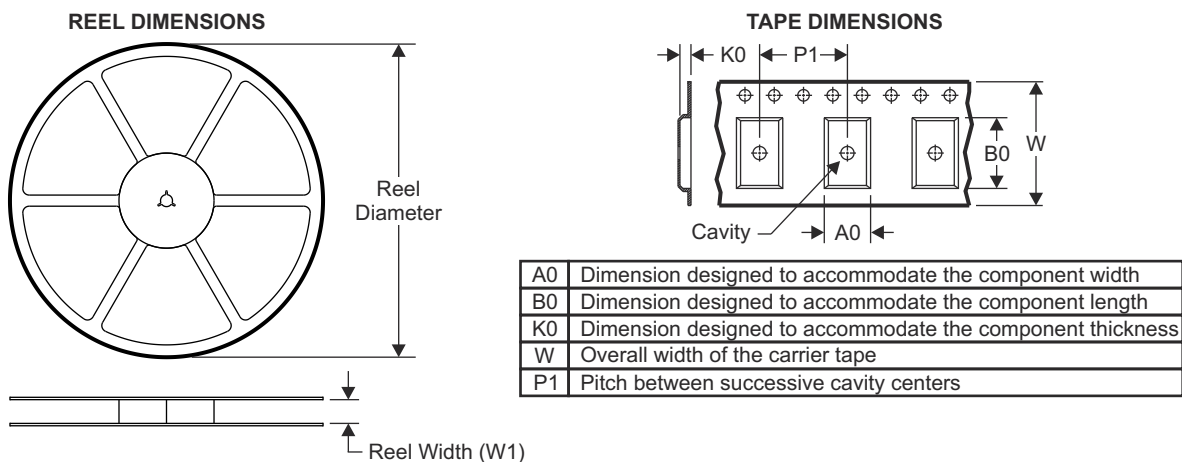
7.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

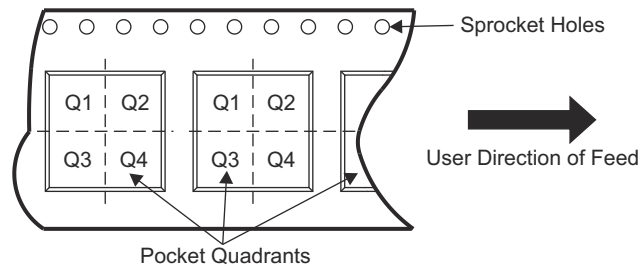
8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Tape and Reel Information

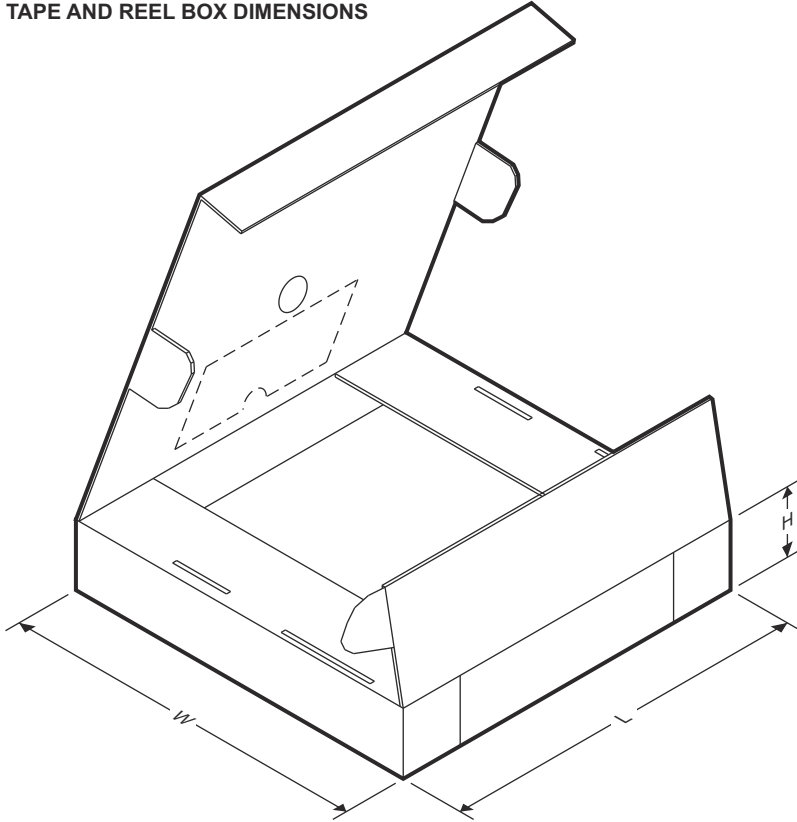


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1046AVDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1048AVDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1046AVDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1048AVDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1046AVDMTRQ1	VSON	DMT	14	3000	370.0	355.0	55.0
TCAN1048AVDMTRQ1	VSON	DMT	14	3000	370.0	355.0	55.0
TCAN1046AVDRQ1	SOIC	D	14	2500	853.0	449.0	35.0
TCAN1048AVDRQ1	SOIC	D	14	2500	853.0	449.0	35.0

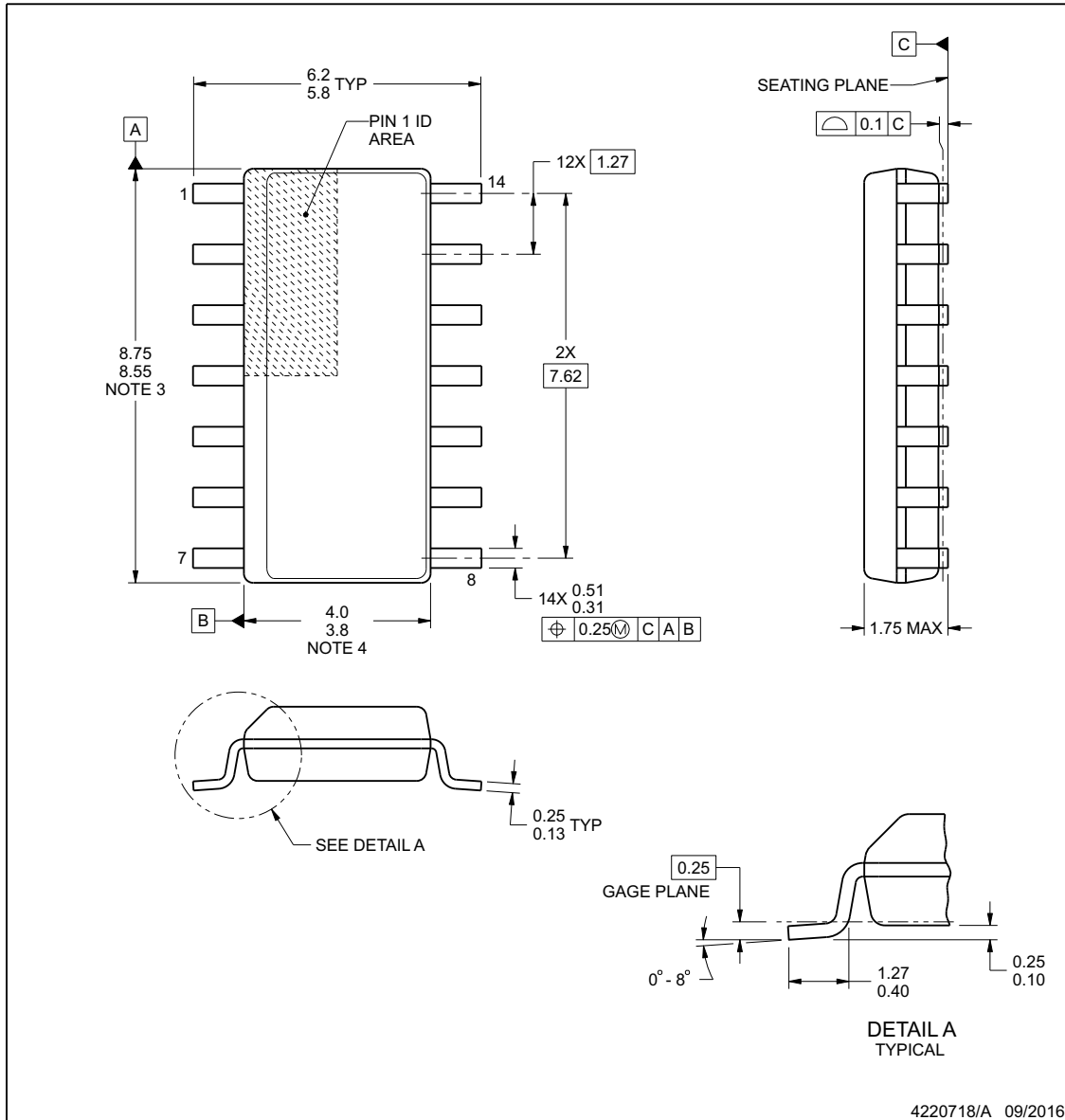


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

www.ti.com

ADVANCE INFORMATION

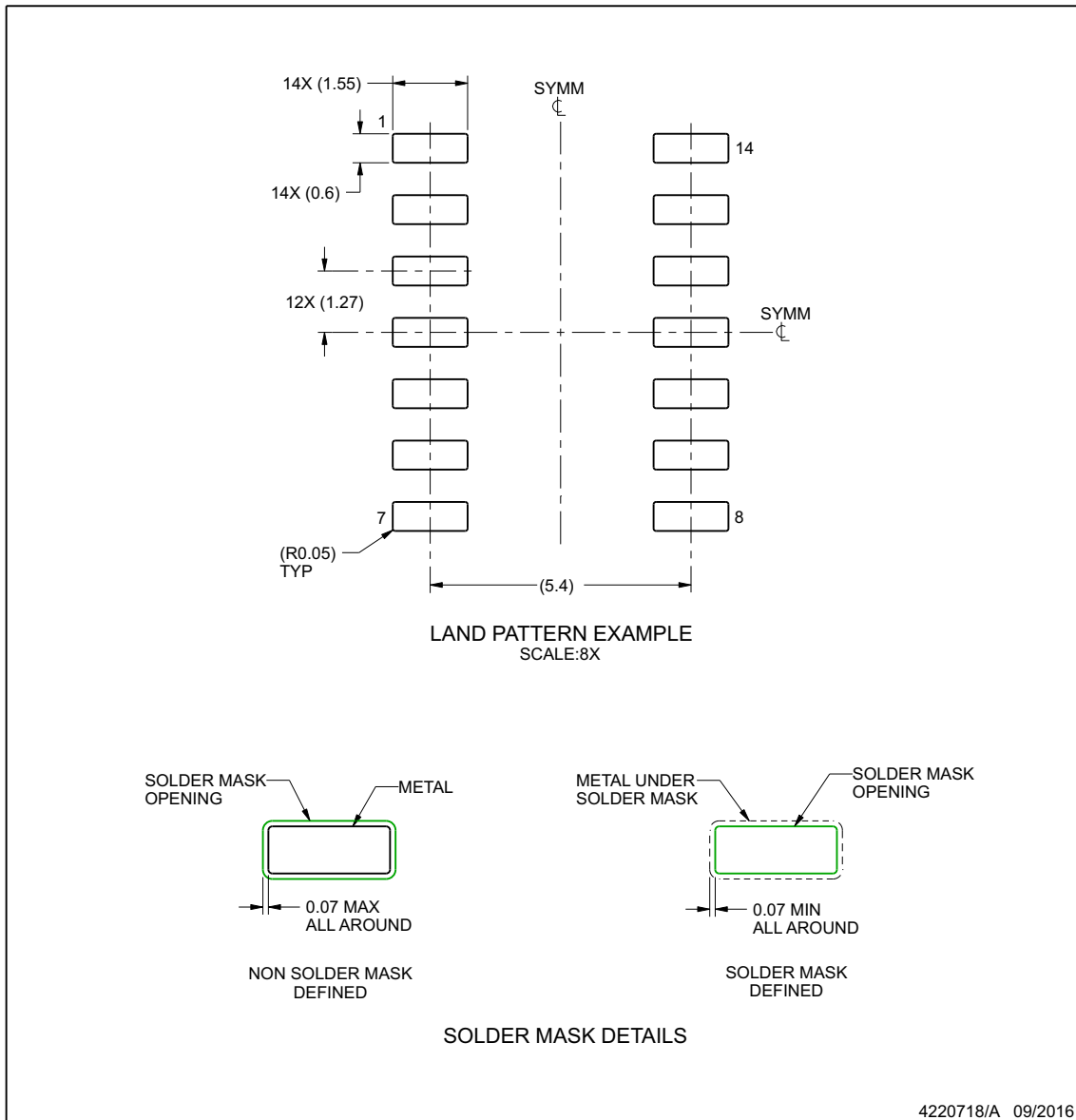
EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

ADVANCE INFORMATION



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

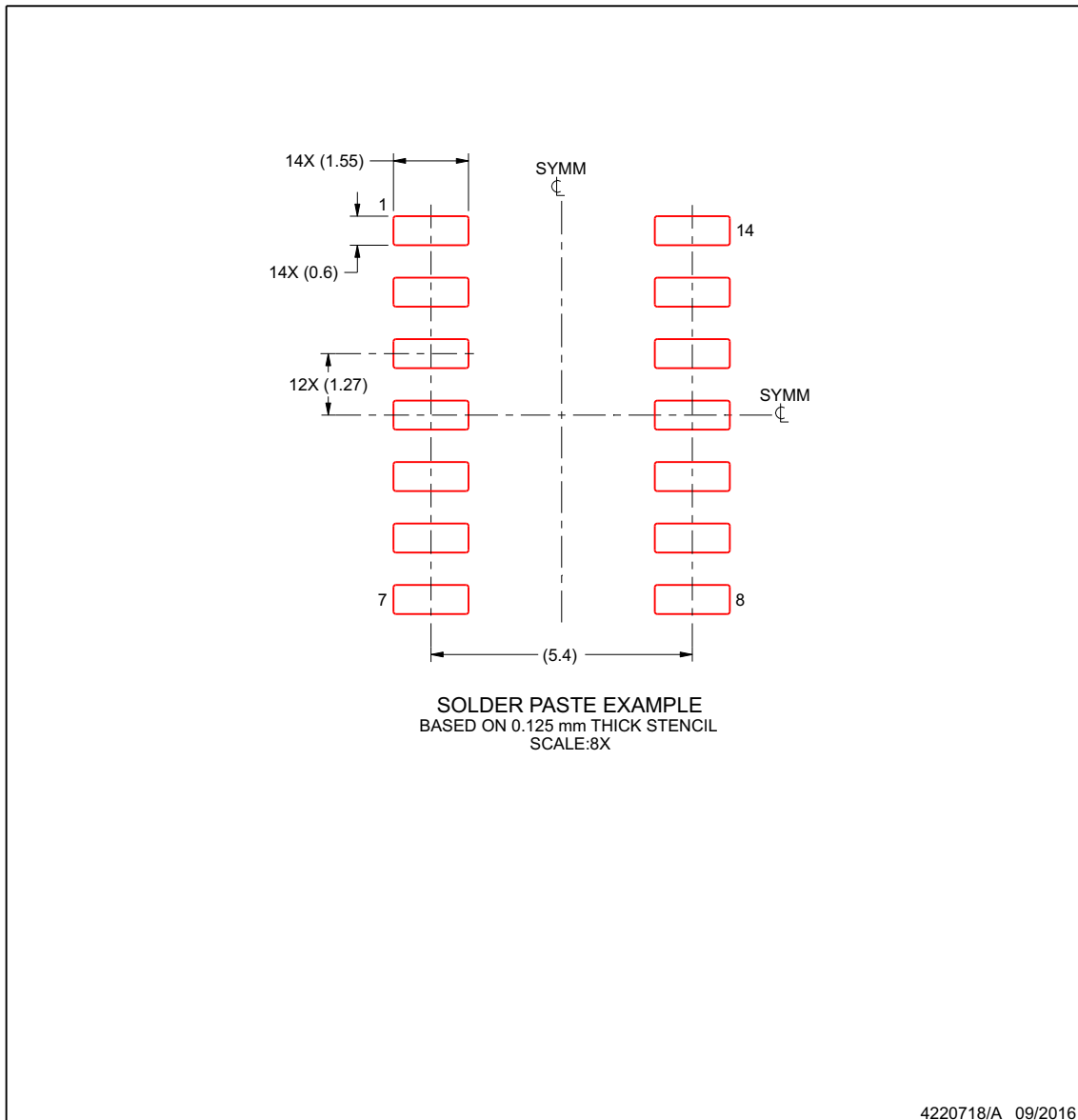
www.ti.com

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

www.ti.com

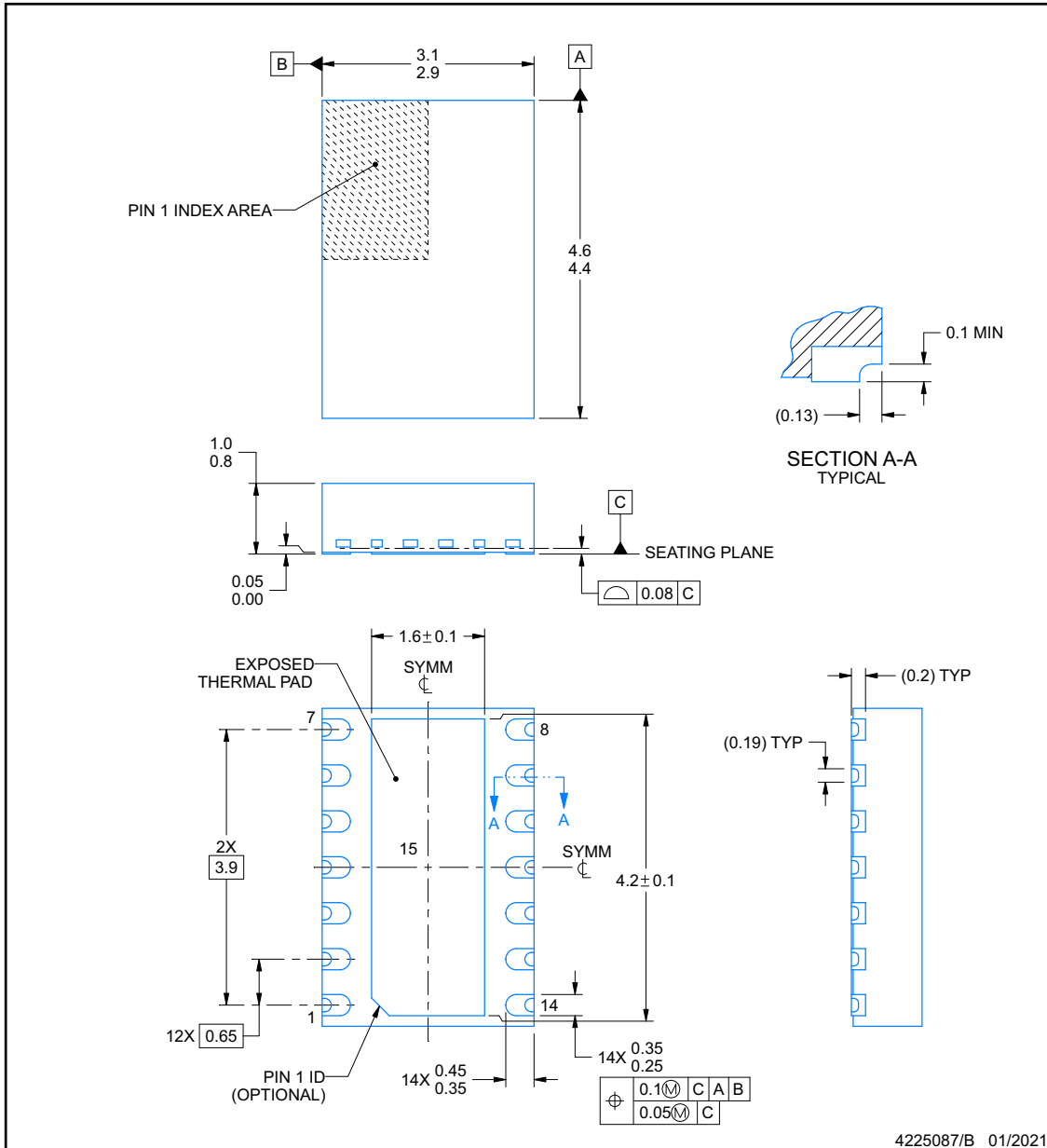
ADVANCE INFORMATION



DMT0014B

PACKAGE OUTLINE
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

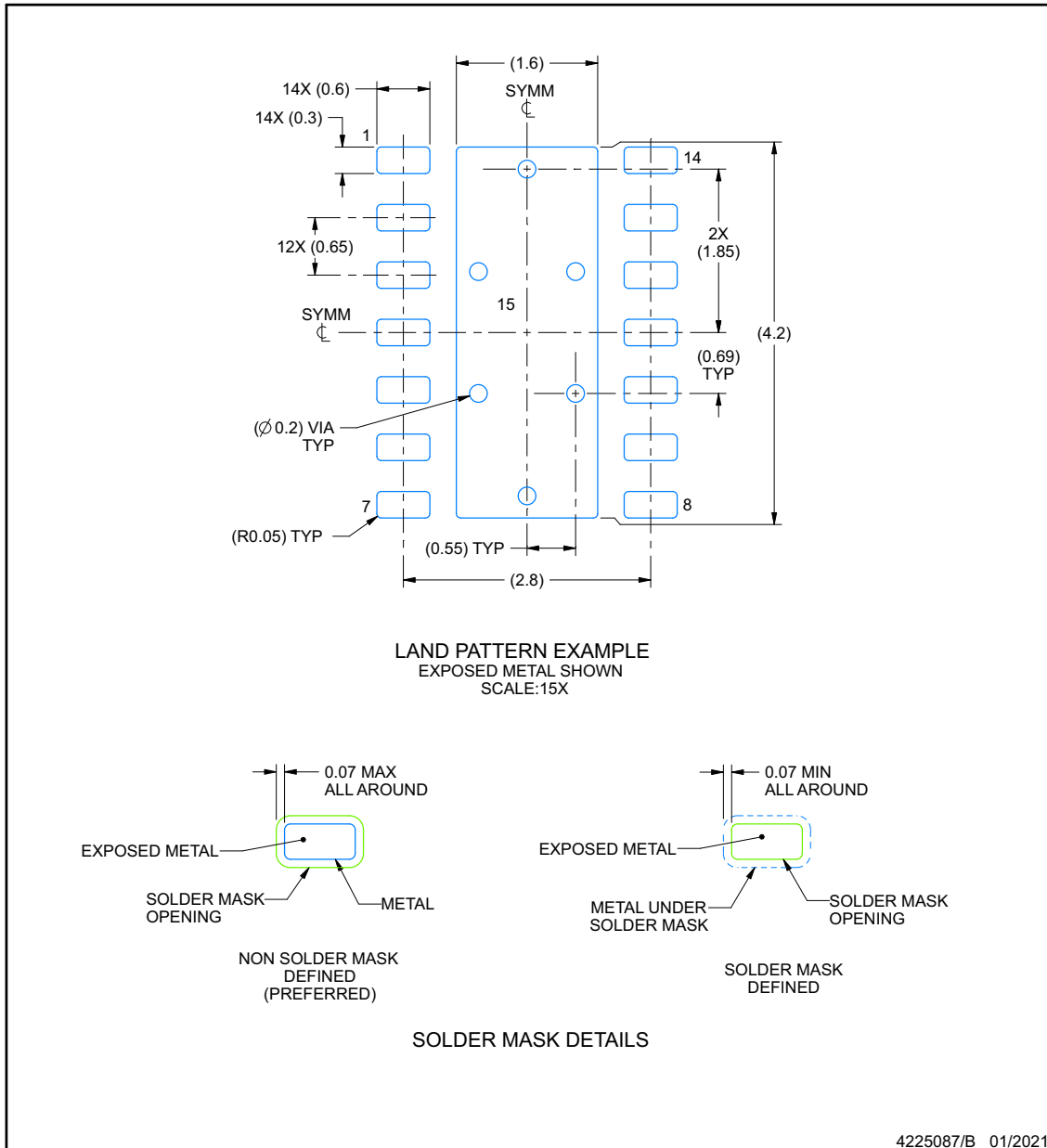
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

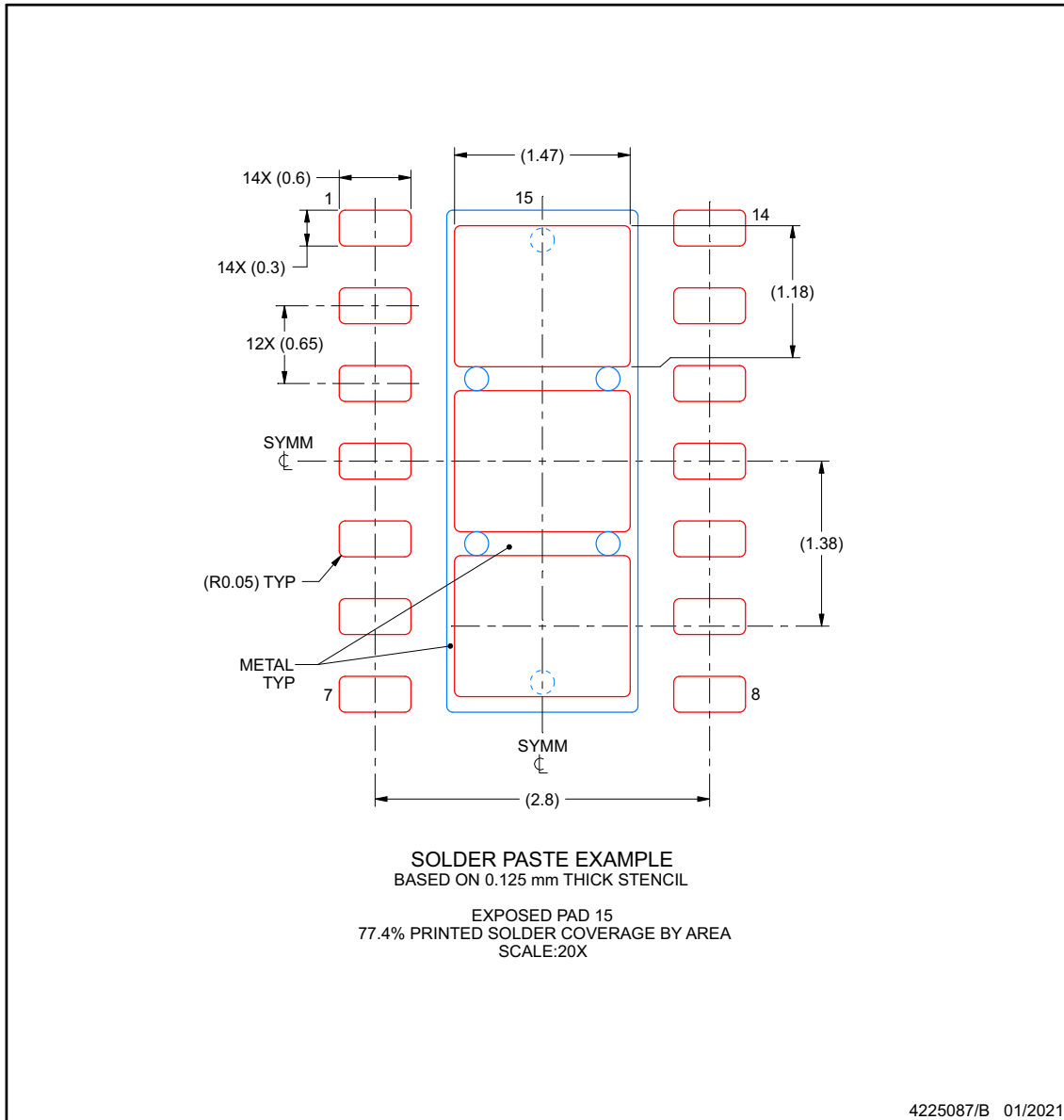
EXAMPLE STENCIL DESIGN

DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

ADVANCE INFORMATION



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1046AVDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	46AV	Samples
TCAN1046AVDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV	Samples
TCAN1046AVDYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV	Samples
TCAN1048AVDMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	48AV	Samples
TCAN1048AVDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1048AV	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

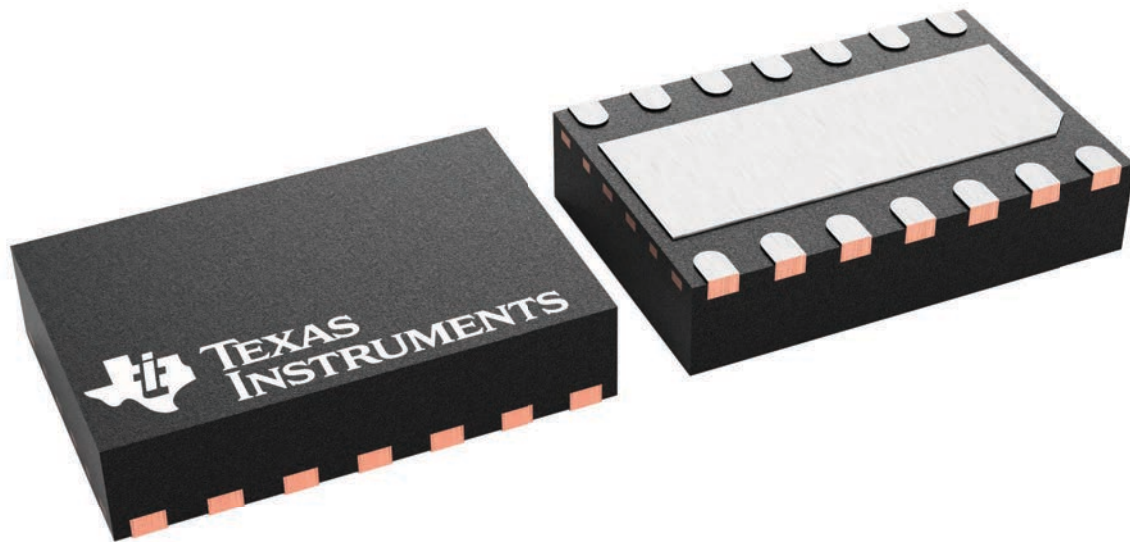
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225088/A

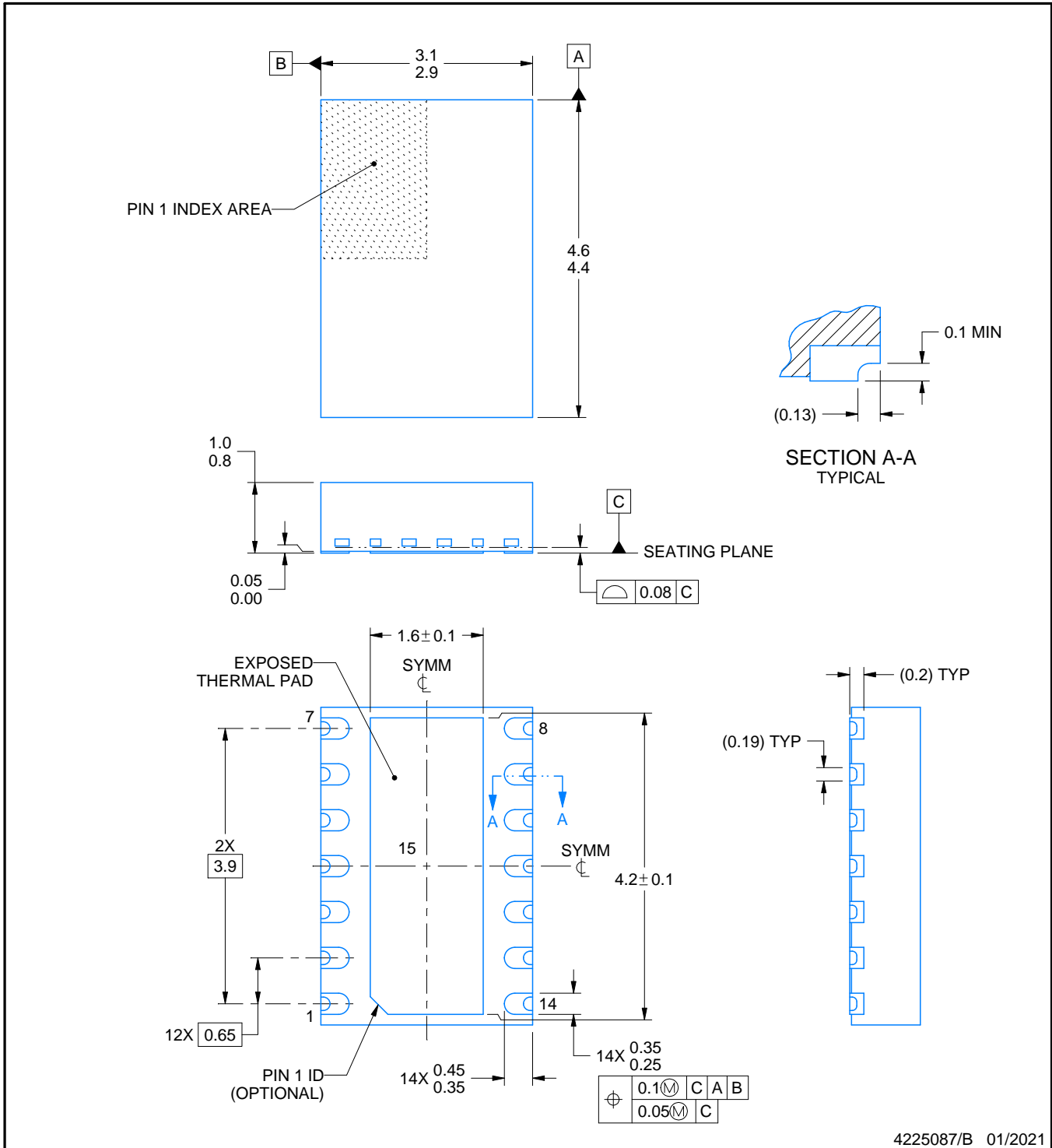
DMT0014B



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4225087/B 01/2021

NOTES:

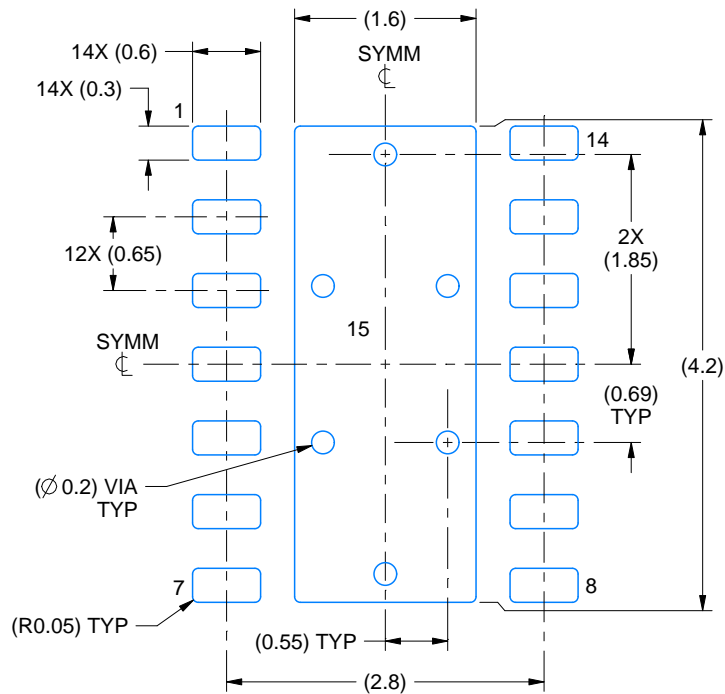
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

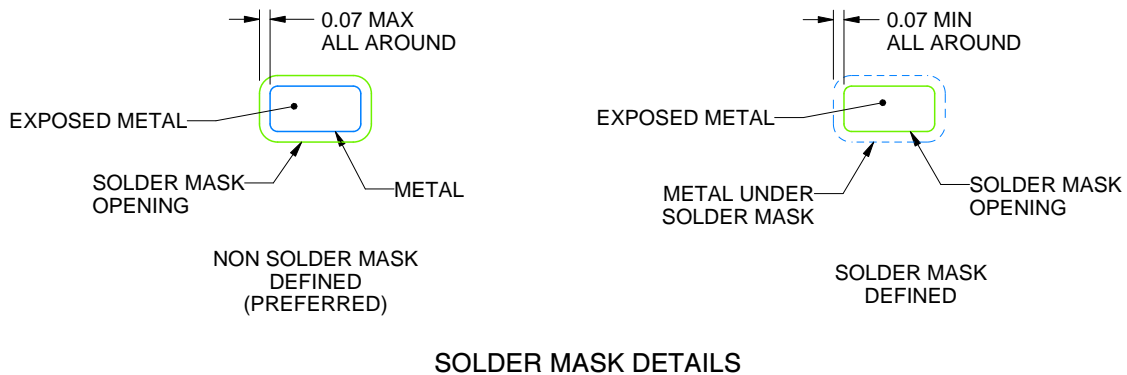
DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

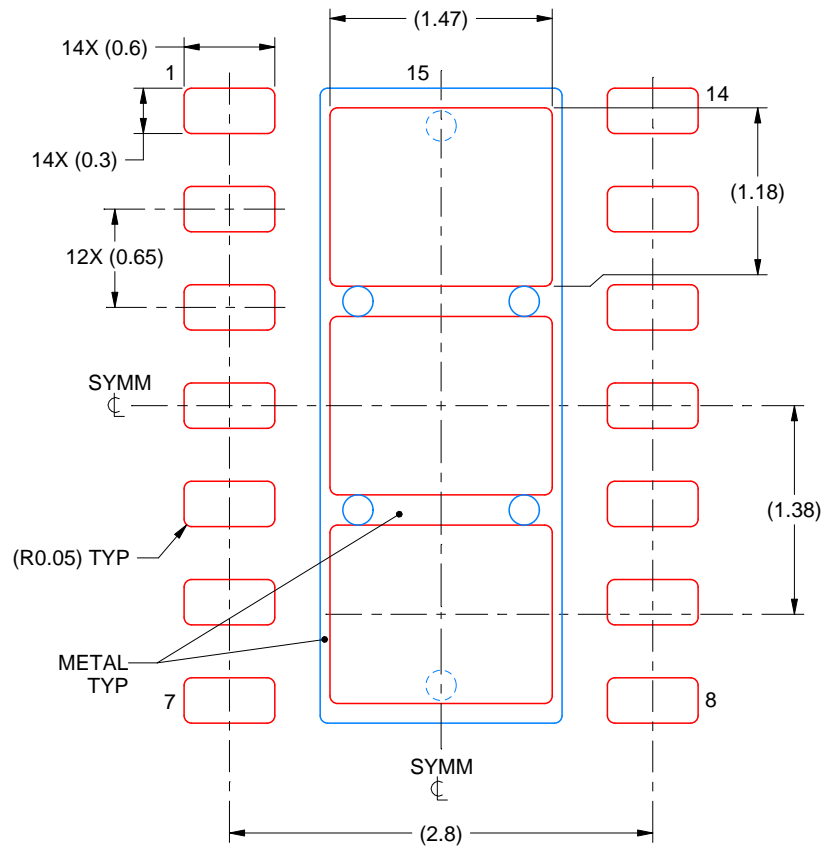
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

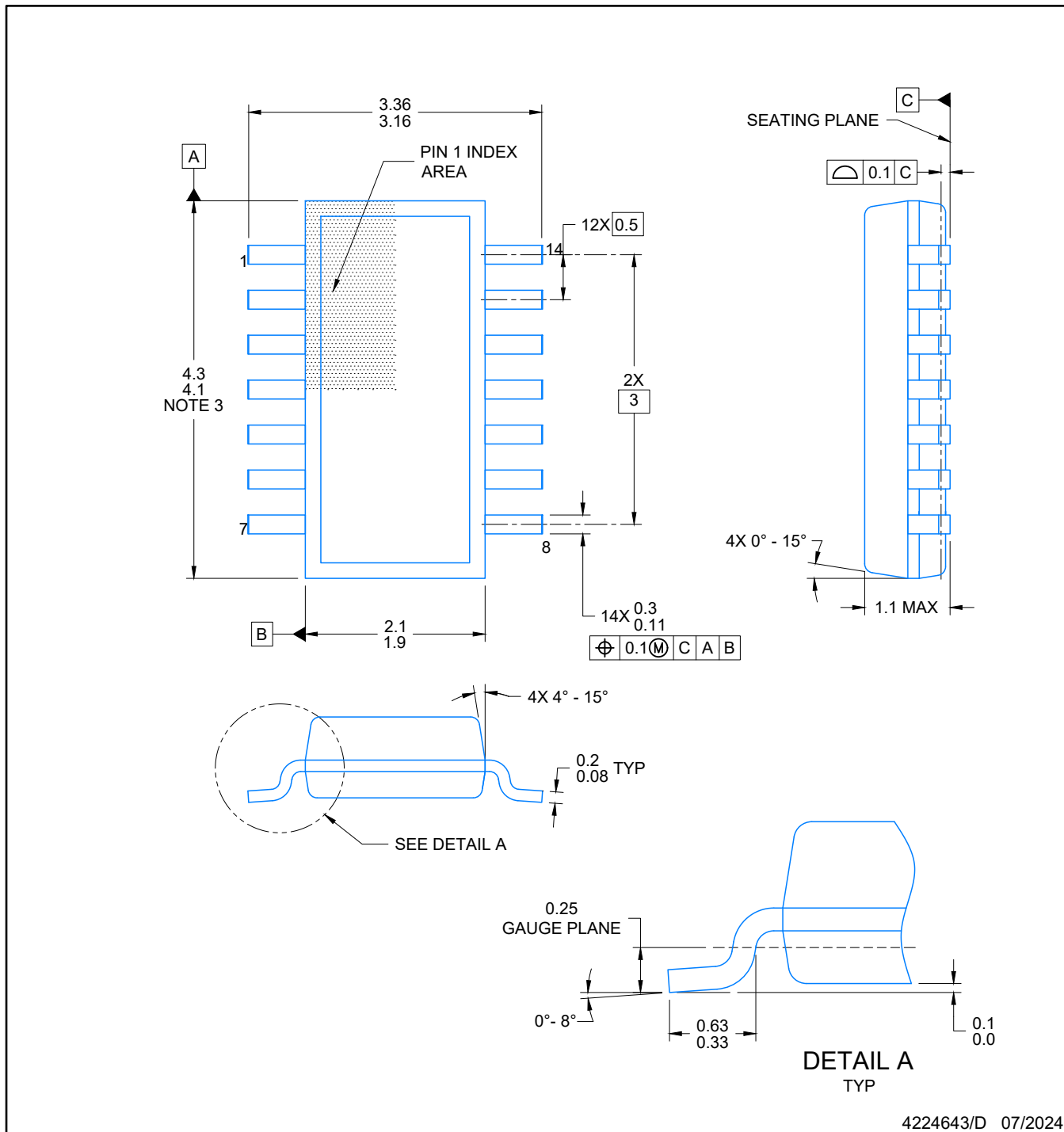


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

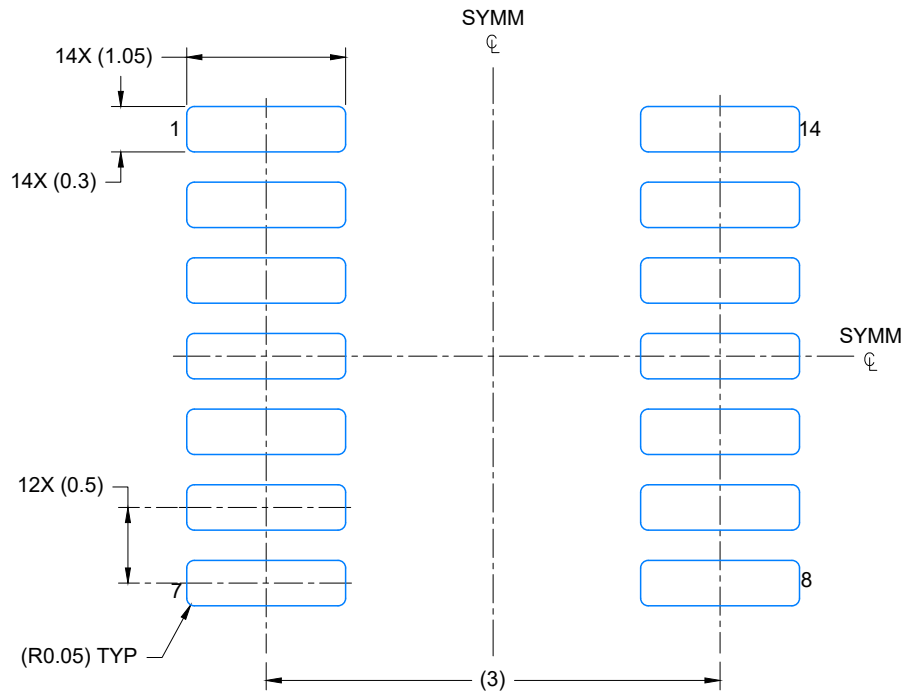
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



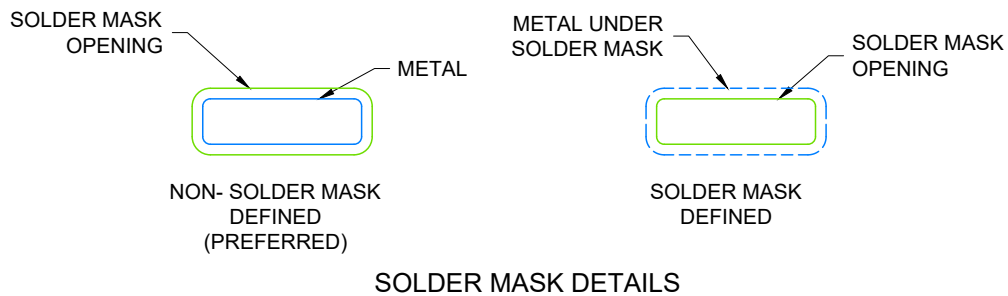
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



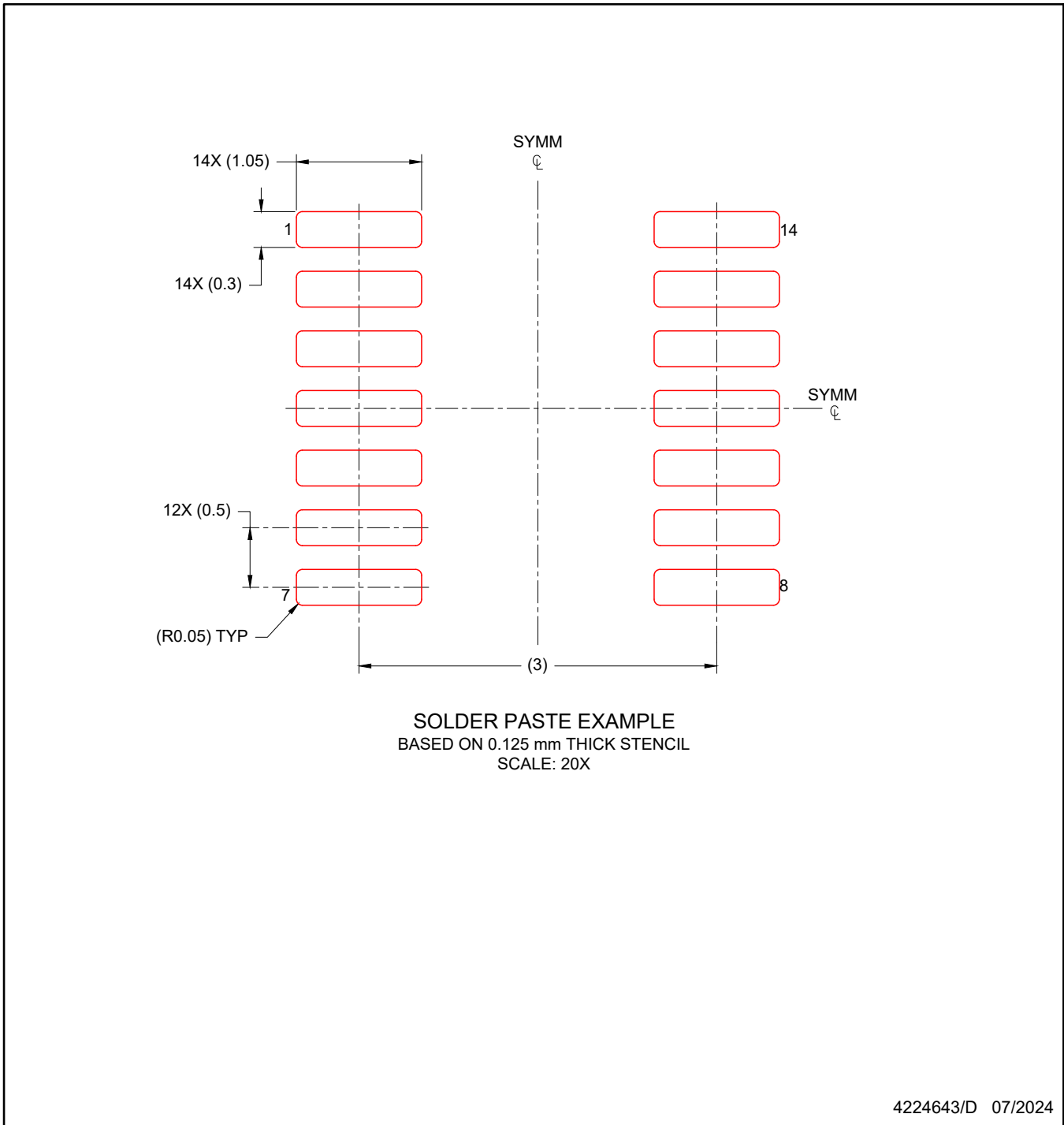
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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