TCAN1462-Q1 および TCAN14622-Q1 フォルト保護 CAN FD トランシーバ、信号改善機能 (SIC) およびスタンバイ・モード付き

1 特長

- AEC Q100 (グレード 1): 車載アプリケーション認定済み
- ISO 11898-2:2016 および CiA 601-4 規格の要件に適合
- Classical CAN および最大 8Mbps の CAN FD
  - 複雑なトポロジでリンギング効果を低減することにより、バス信号をアクティブに改良
  - Classic CAN ネットワークでの使用に対する下位互換性
- V_{IO} レベル・シフト対応：1.7V～5.5V
- 動作モード
  - 通常モード
  - リモート・ウェイクアップ要求をサポートする、低消費電力スタンバイ・モード
- 無電源時の理想的なパッシブ動作
  - バスおよびロジック端子は高インピーダンス (動作中のバスまたはアプリケーションに無負荷)
  - ホットプラグ対応：バスおよび RXD 出力での、電力オン / オフのグリッチ・フリー動作
  - フローティング論理ピンと低電圧電源条件におけるデバイスの動作を定義
- 保護機能
  - バス・ピンの IEC ESD 保護
  - CAN バスの障害耐性：±58V
  - V_{CC} および V_{IO} (V バージョンのみ) 電源端子の低電圧保護
  - TXD ドミナント状態タイムアウト (TXD DTO)
  - サーマル・シャットダウン保護 (TSD)
- SOIC (8)、小型フットプリント SOT23 (8)、自動光学検査 (AOI) 性能を向上させたウェッタブル・フランクのリードレス 3mm x 3mm VSON (8) パッケージで供給

2 アプリケーション

- 車載ゲートウェイ
- 先進運転支援システム (ADAS)
- ボディ・エレクトロニクス / 照明
- ハイブリッド、電気、パワートレイン・システム
- 車載インフォテインメントおよびクラスタ

3 概要

TCAN1462-Q1 および TCAN1462V-Q1 は、ISO 11898-2:2016 高速 CAN 仕様と CiA 601-4 信号改善 (SIC) 仕様の物理層の要件を満たす高速 CAN トランシーバです。このデバイスは、ドミナントとリセッシブのエッジで信号リンギングを低減し、複雑なネットワーク・トポロジで高いスループットを実現します。信号改善機能を活用すると、アプリケーションは 2Mbps、5Mbps、さらに複数の未終端のスタブを持つ大規模ネットワークで動作できるようになり、CAN FD (フレキシブル・データ・レート) の真の利点を抽出することができます。

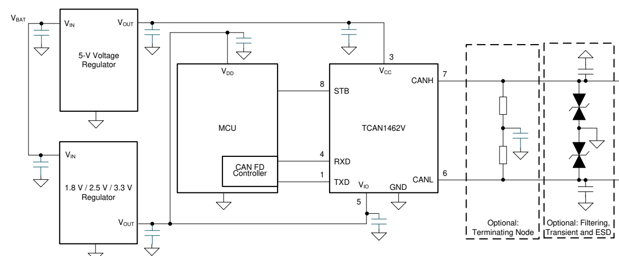
これらのデバイスは、CiA 601-4 が規定するタイミング仕様を満たしており、通常の CAN FD トランシーバと比較して、はるかに厳密なビット・タイミング対称性を備えています。この結果、より大きなタイミング・ウィンドウを使用して正しいビットをサンプリングし、リンギングとビット歪みを本質的に持つ大きく複雑なスター・ネットワークでエラー・フリーの通信を実現できます。

これらのデバイスは、TCAN1046A-Q1 や TCAN1042-Q1 など、8 ピンの CAN FD トランシーバとピン互換です。

デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
TCAN1462(V)-Q1	SOT-23 (DDF)	2.90mm × 1.60mm
	VSON (DRB)	3.00mm × 3.00mm
	SOIC (D)	4.90mm × 3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ブロック概略図

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4 Revision History

DATE	REVISION	NOTES
February 2022	*	Initial Revision

5 概要 (続き)

「V」接尾辞付きの TCAN1462-Q1 デバイスには、V_{IO} ロジック電源ピン経由の内部ロジック・レベル変換が搭載されており、1.8V、3.3V、5V のコントローラと直接接続できます。これらのトランシーバは低消費電力スタンバイ・モードをサポートしており、ISO 11898-2:2016 に定義されたウェイクアップ・パターン (WUP) に準拠した CAN バスによるリモート・ウェイクアップが可能です。このデバイス・ファミリは、低電圧検出、サーマル・シャットダウン (TSD)、ドライバ・ドミナント・タイムアウト (TXD DTO)、±58V のバス・フォルト保護などの多くの保護機能も備えています。

6 Device Comparison Table

Device Number	Bus Fault Protection	Low voltage I/O Logic Support on Pin 5	Pin 8 Mode Selection
TCAN1462-Q1	± 58 V	No	Low Power Standby Mode with Remote Wake
TCAN1462V-Q1	± 58 V	Yes	

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7 Pin Configurations and Functions

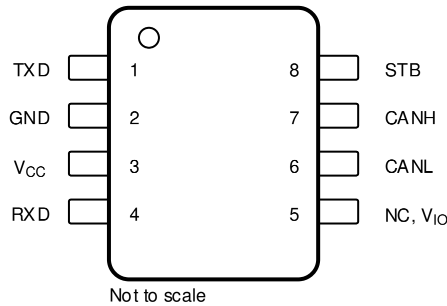

図 7-1. SOIC (D) and SOT-23 (DDF) Package, 8 Pin (Top View)

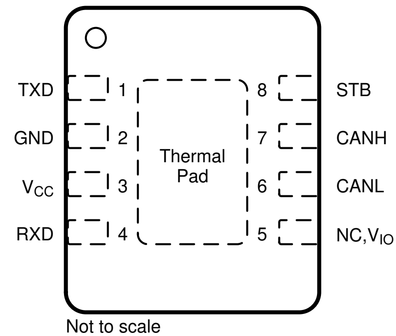

図 7-2. VSON (DRB) Package, 8 Pin (Top View)

表 7-1. Pin Functions

PINS		TYPE	DESCRITION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	Supply	5 V supply voltage
RXD	4	Digital Output	CAN receive data output, tristate when powered off
V_{IO}	5	Supply	Logic supply voltage
NC		--	No Connect (not internally connected); Devices without V_{IO}
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby mode control input, integrated pull-up
Thermal Pad (VSON only)	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 サポート・リソース

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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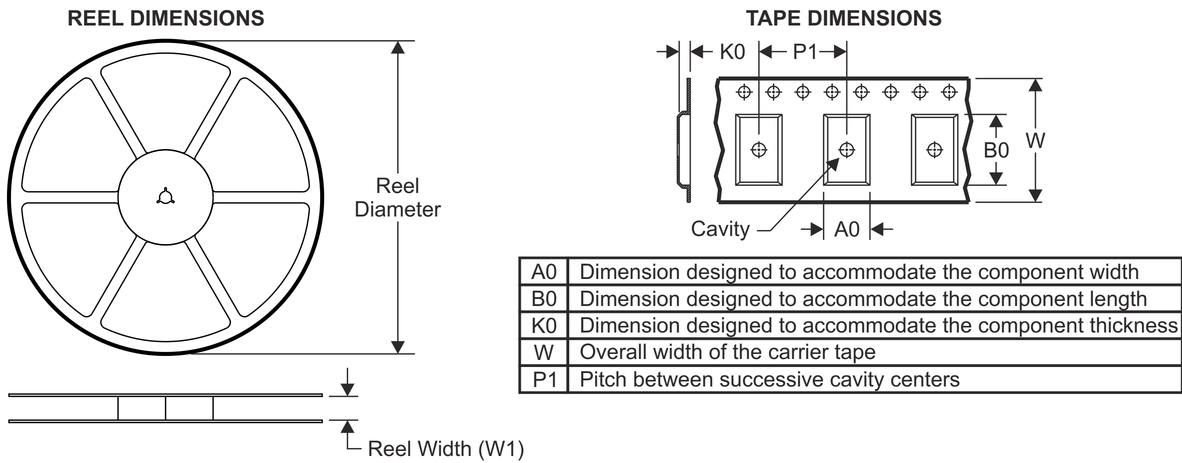
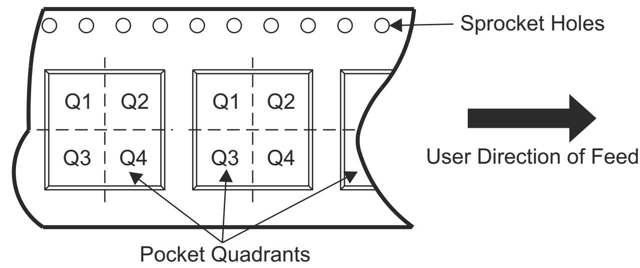
9.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1462DRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q2
TCAN1462VDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q2
TCAN1462DDFRQ1	SOT-23	DDF	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1462VDDFRQ1	SOT-23	DDF	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1462DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TCAN1462VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

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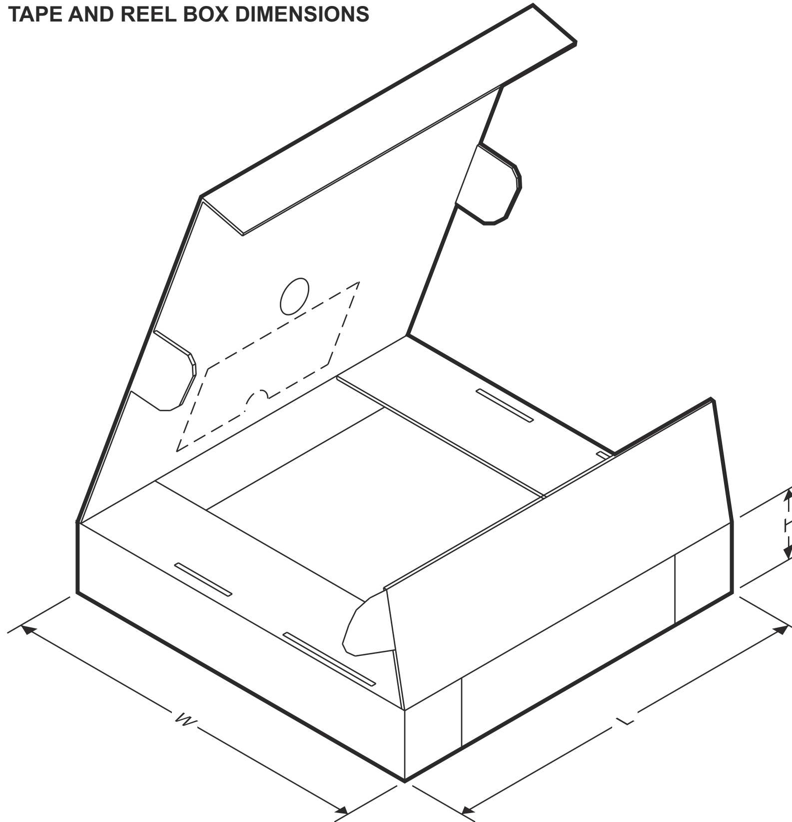
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1462DRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1462VDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TCAN1462DDFRQ1	SOT-23	DDF	8	3000	210.0	185.0	210.0
TCAN1462VDDFRQ1	SOT-23	DDF	8	3000	210.0	185.0	210.0
TCAN1462DRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0
TCAN1462VDRBRQ1	SON	DRB	8	3000	346.0	346.0	35.0

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PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

C
SEATING PLANE
.228-.244 TYP
[5.80-6.19]
.004 [0.1] C
A
PIN 1 ID AREA
6X .050
[1.27]
1
8
.189-.197
[4.81-5.00]
NOTE 3
2X
.150
[3.81]
4X (0° -15°)
4
5
8X .012-.020
[0.31-0.51]
.010 [0.25] Ⓜ C A B
B
.150-.157
[3.81-3.98]
NOTE 4
.069 MAX
[1.75]
.005-.010 TYP
[0.13-0.25]
4X (0° -15°)
SEE DETAIL A
.010
[0.25]
0° - 8°
.016-.050
[0.41-1.27]
.041
[1.04]
.004-.010
[0.11-0.25]
DETAIL A
TYPICAL

4221445/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

TEXAS INSTRUMENTS
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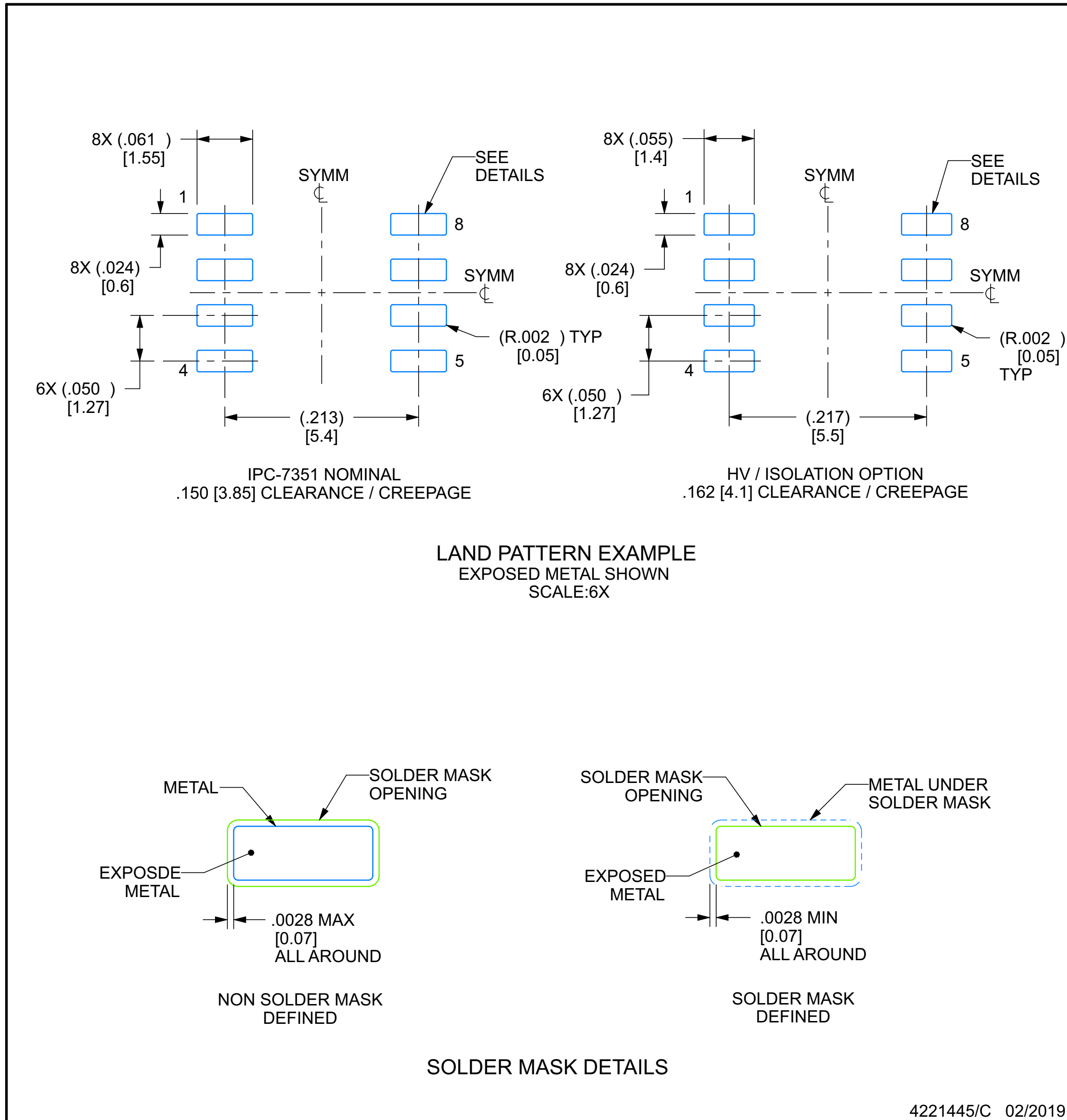

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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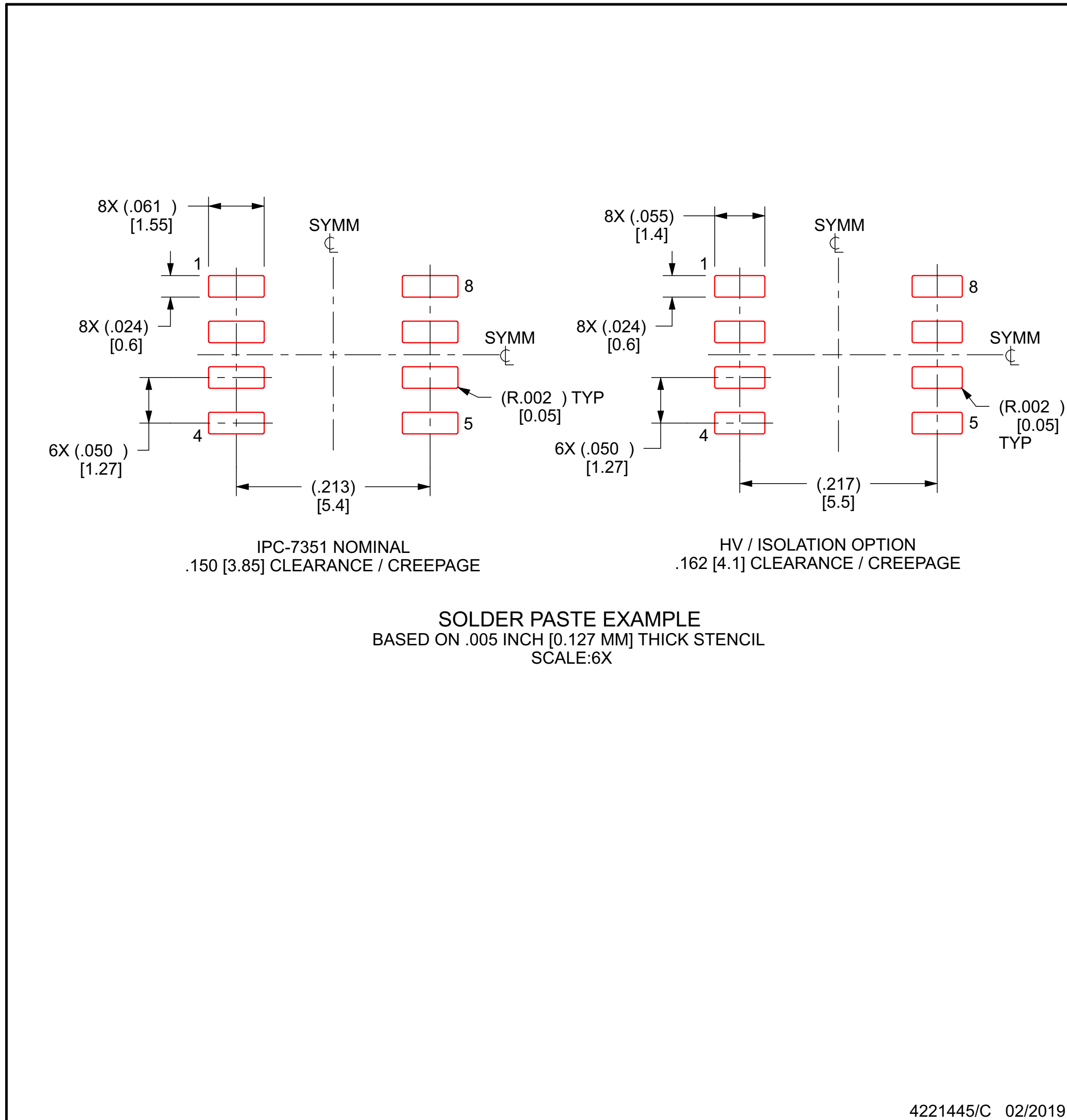
EXAMPLE STENCIL DESIGN

D0008B SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGE OUTLINE

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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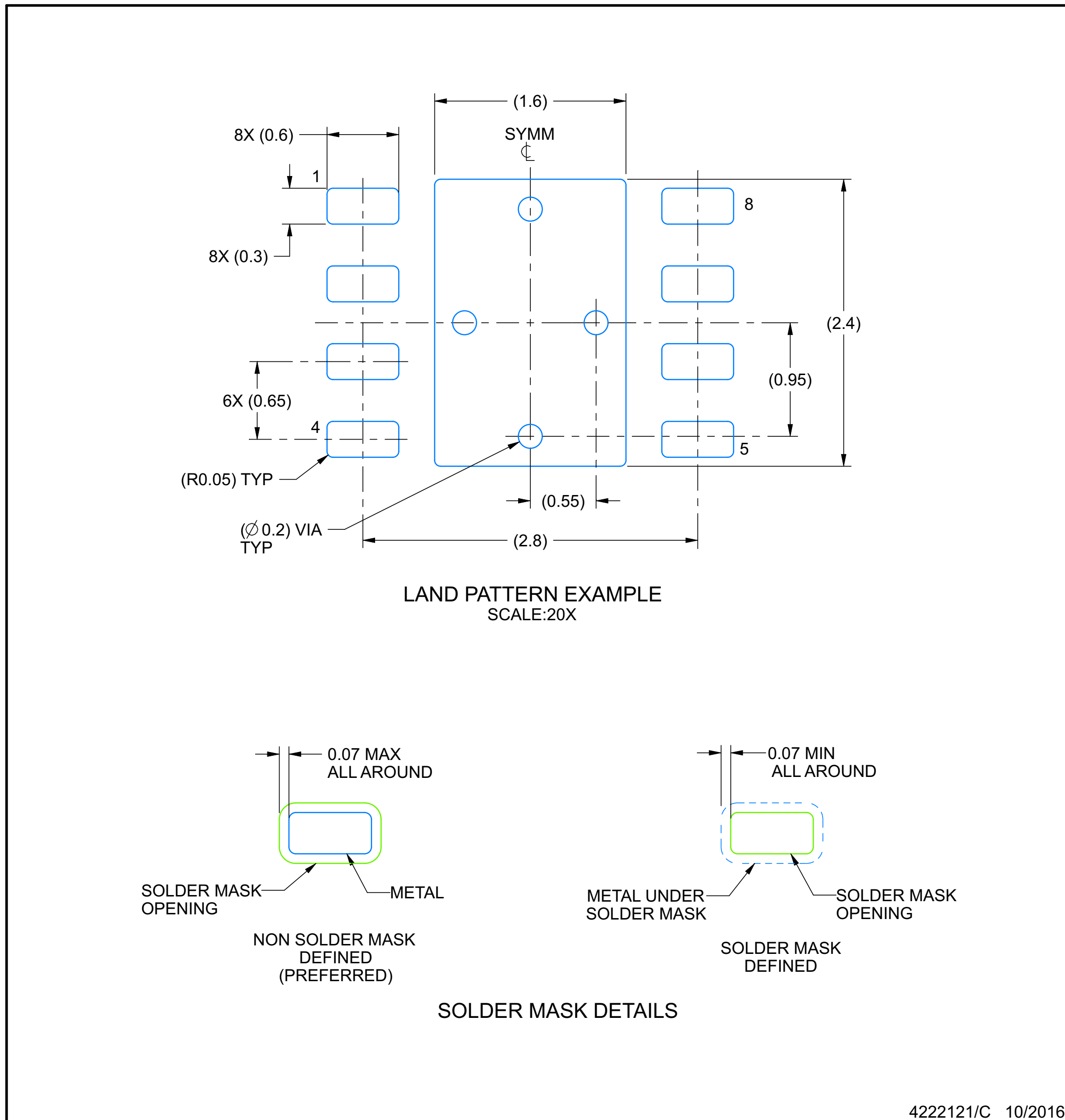
EXAMPLE BOARD LAYOUT

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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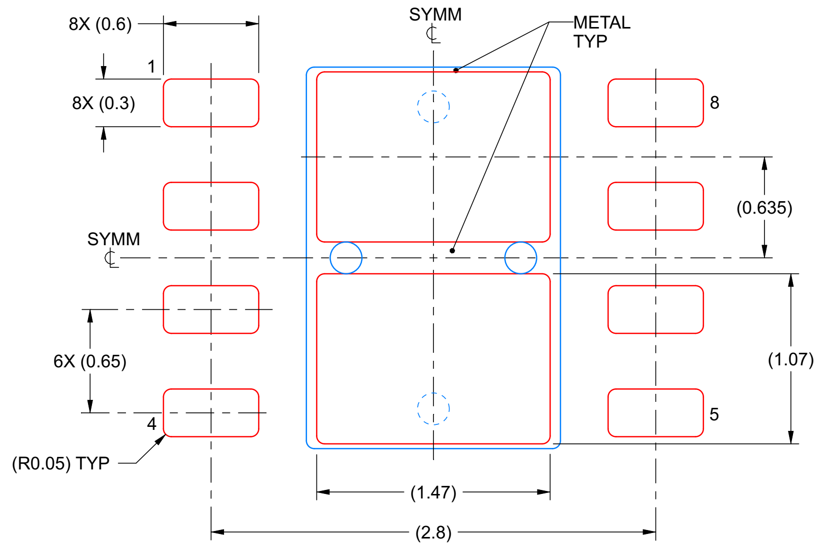
EXAMPLE STENCIL DESIGN

DRB0008F **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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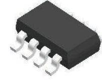

PACKAGE OUTLINE

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

2.95
2.65 TYP

PIN 1 ID
AREA

A

1

8

6X 0.65

2.95
2.85
NOTE 3

2X
1.95

4

5

8X 0.4
0.2

0.1 Ⓜ C A Ⓢ B Ⓢ

B

1.65
1.55

C

SEATING PLANE

0.1 C

1.1 MAX

0.20
0.08 TYP

SEE DETAIL A

0.25
GAGE PLANE

0° - 8°

0.6
0.3

0.1
0.0

DETAIL A
TYPICAL

4222047/B 11/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

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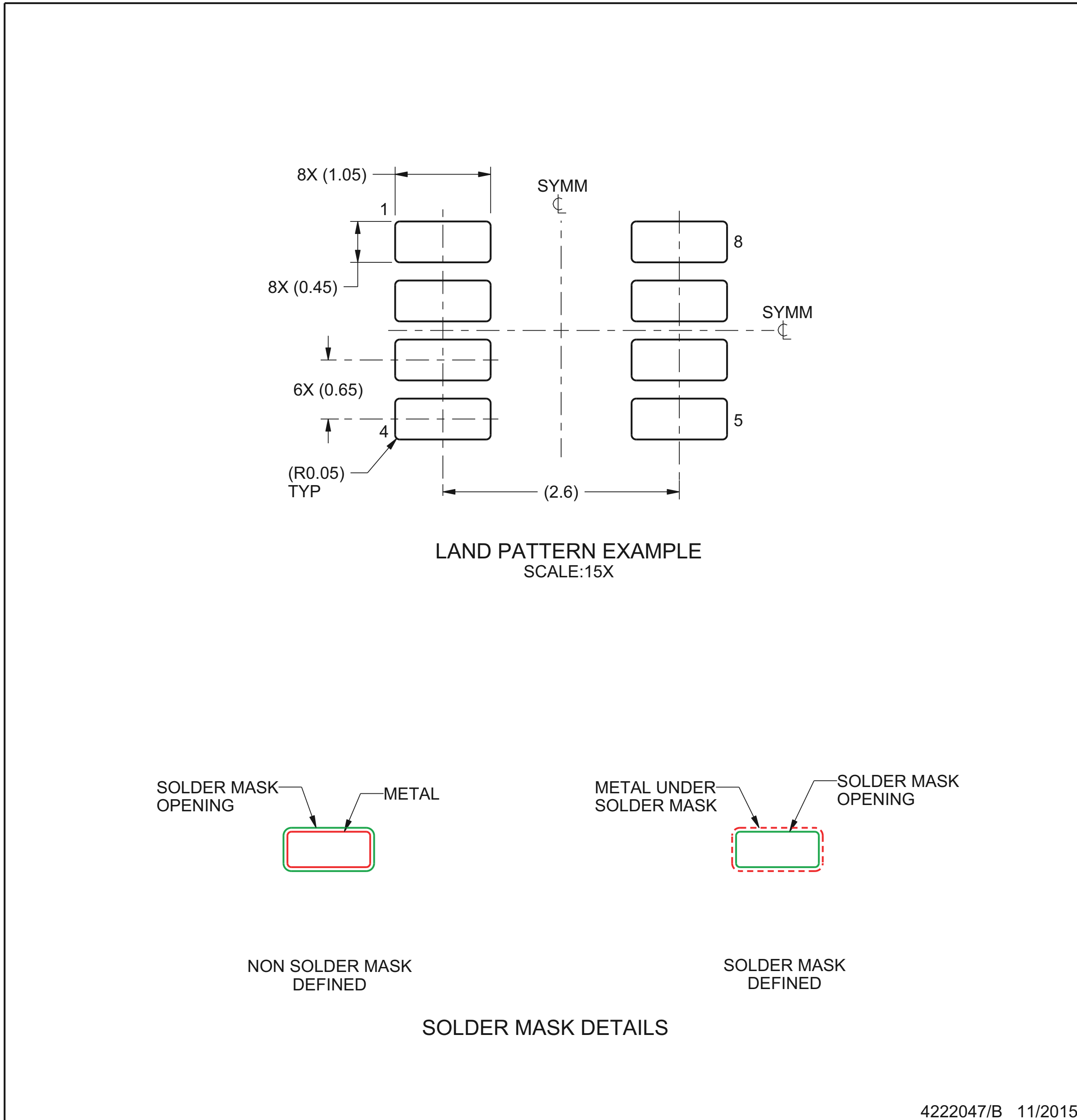

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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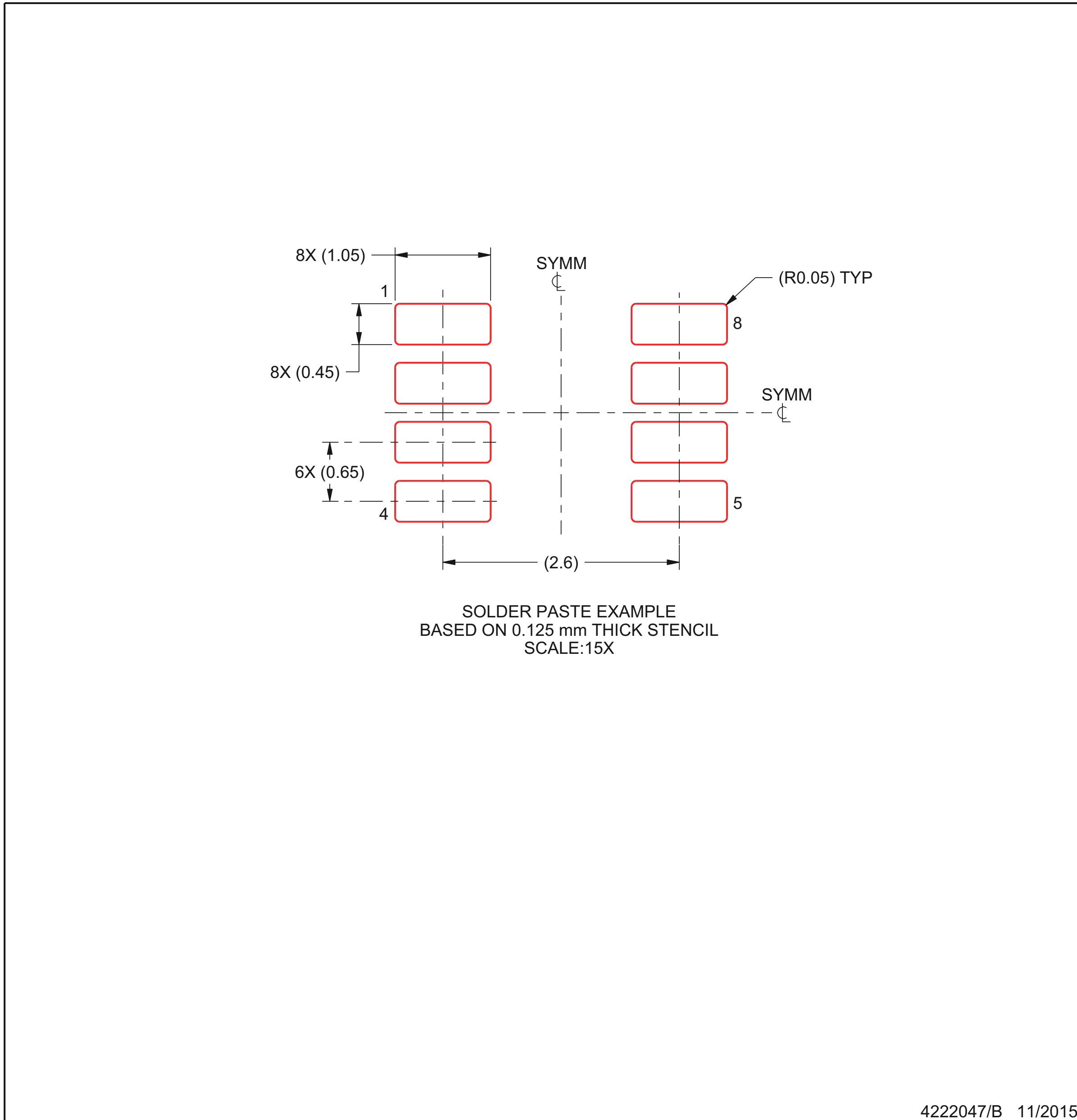
EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1462DRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1462	Samples
TCAN1462DRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1462	Samples
TCAN1462VDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1462V	Samples
TCAN1462VDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1462V	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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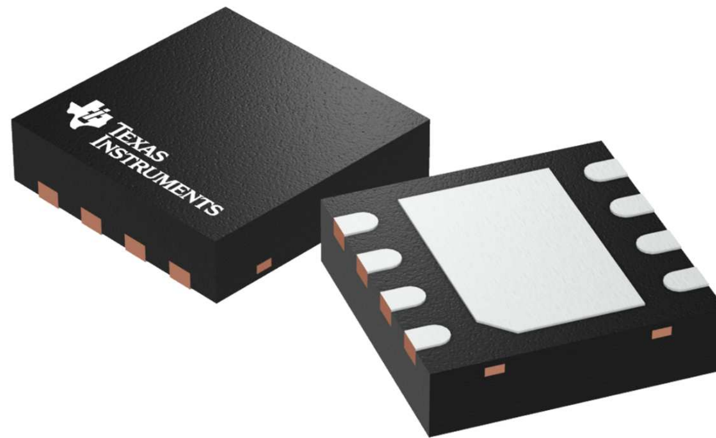
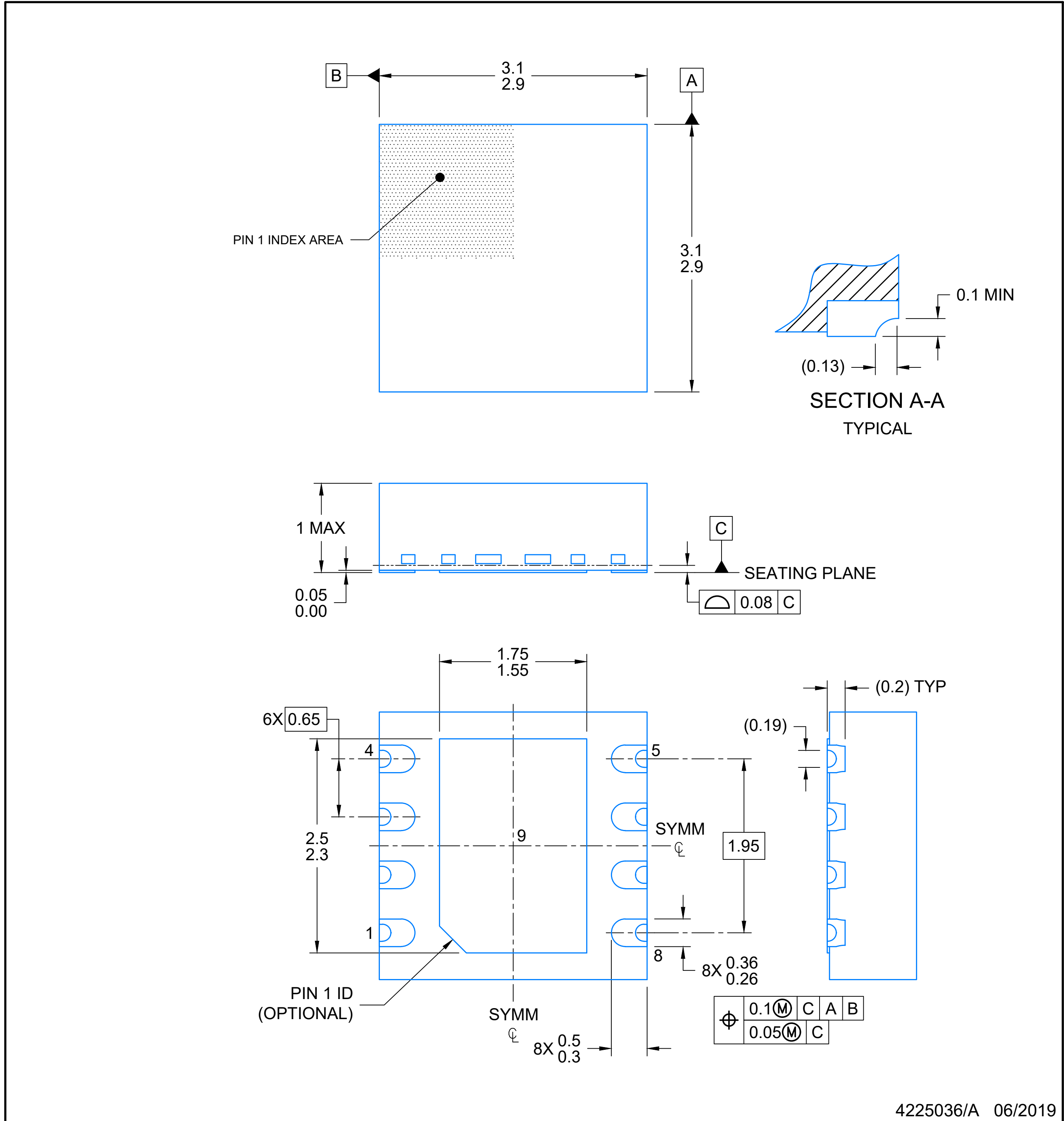
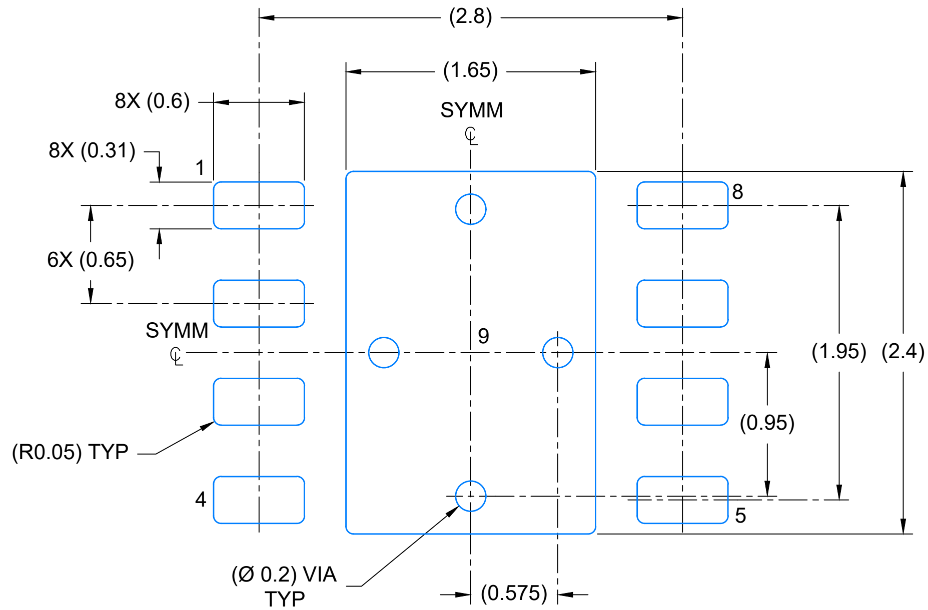


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

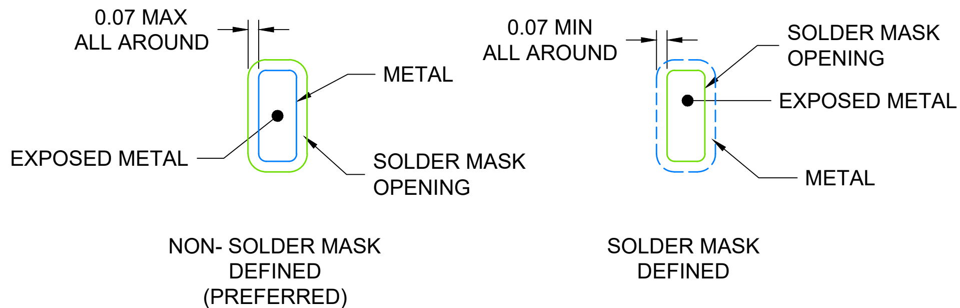


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

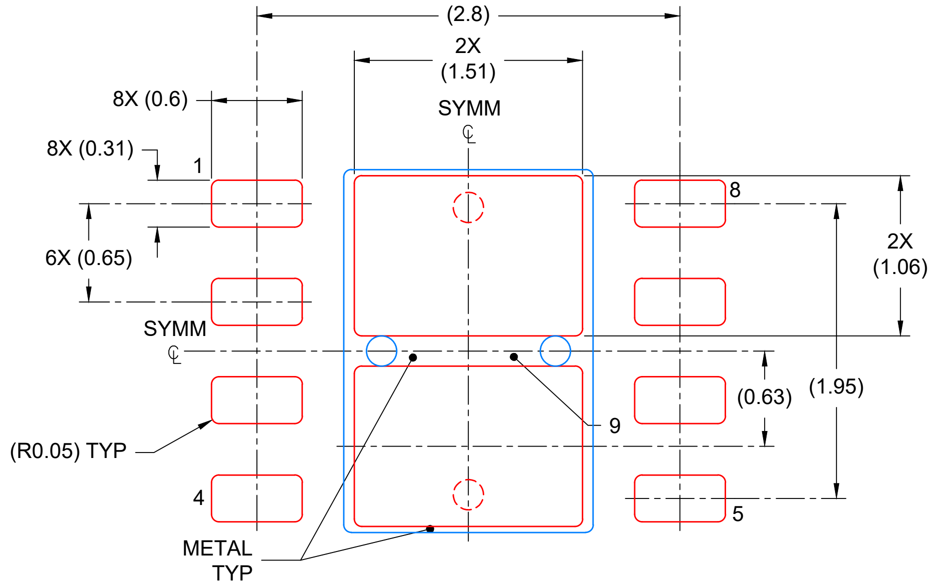
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



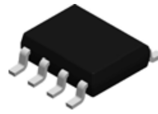
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

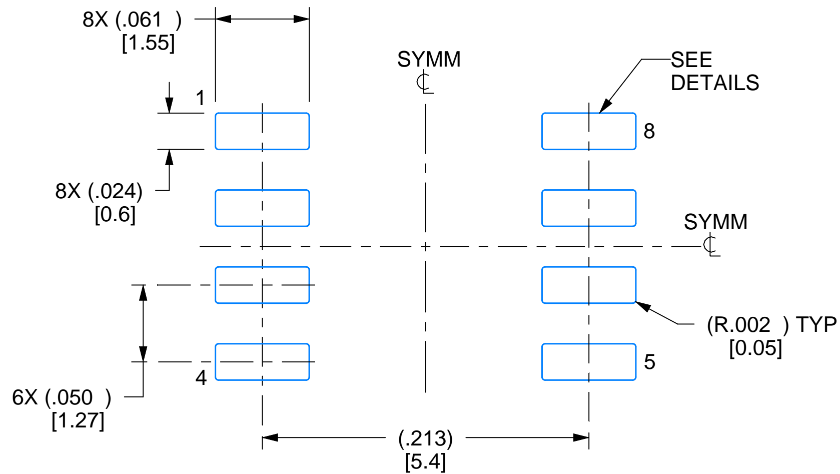
SMALL OUTLINE INTEGRATED CIRCUIT

C
SEATING PLANE
.228-.244 TYP
[5.80-6.19]
A
PIN 1 ID AREA
.004 [0.1] C
6X .050
[1.27]
1
8
.189-.197
[4.81-5.00]
NOTE 3
2X
.150
[3.81]
4X (0°-15°)
4
5
8X .012-.020
[0.31-0.51]
B
.150-.157
[3.81-3.98]
NOTE 4
.010 [0.25] Ⓜ C A B
.069 MAX
[1.75]
.005-.010 TYP
[0.13-0.25]
4X (0°-15°)
SEE DETAIL A
.010
[0.25]
0° - 8°
.004-.010
[0.11-0.25]
.016-.050
[0.41-1.27]
(.041)
[1.04]
DETAIL A
TYPICAL

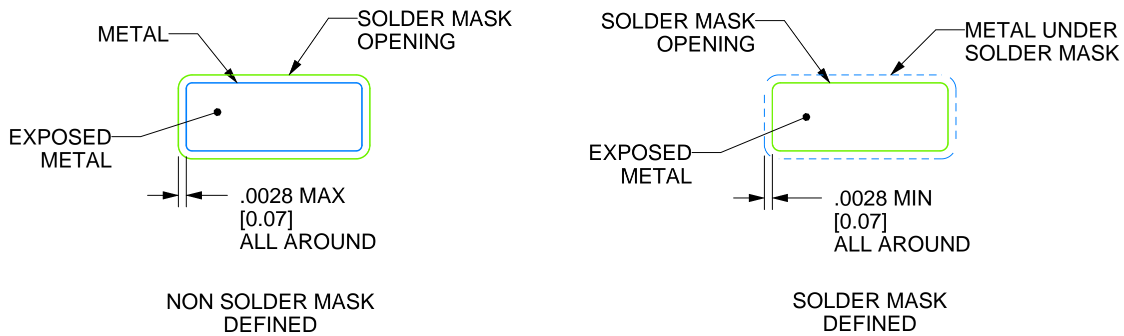
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

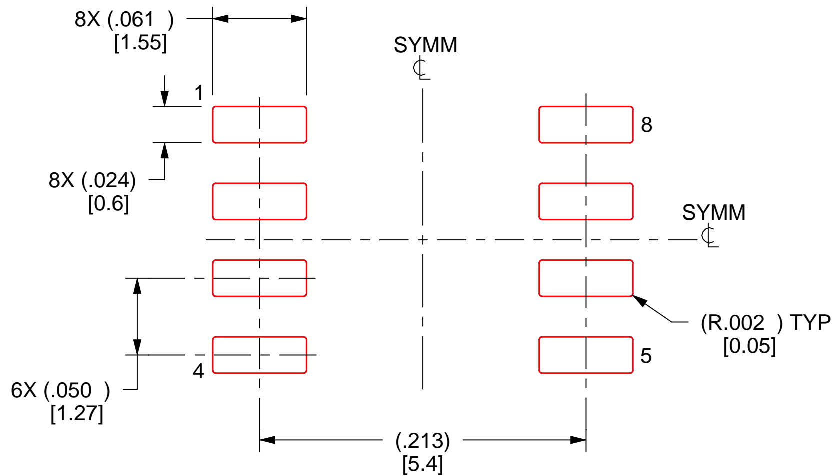
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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