TEXAS INSTRUMENTS
TCAN4551-Q1
JAJSHT0 – AUGUST 2019

TCAN4551-Q1 車載用コントローラ・エリア・ネットワーク・フレキシブル・データ・レート (CAN FD) コントローラ、トランシーバ内蔵

1 特長

- AEC Q100：車載アプリケーション用に認定済み
  - 温度グレード 1：-40°C～125°C、T_A
- CAN FD トランシーバとシリアル・ペリフェラル・インターフェイス (SPI) を内蔵した CAN FD コントローラ
- ISO 11898-1:2015 と Bosch M_CAN リビジョン 3.2.1.1 の両方をサポートする CAN FD コントローラ
- ISO 11898-2:2016 の要件に適合
- 最高 18MHz の SPI クロック速度で、最高 8Mbps の CAN FD データ・レートをサポート
- Classic CAN と後方互換
- 通常、スタンバイ、スリープ、フェイルセーフの各動作モードを使用可能
- マイクロプロセッサ用の 1.8V、3.3V～5V の入出力ロジックのサポート
- CAN バスでの広い動作範囲
  - ±58V のバス障害保護
  - ±12V 同相
- 電源非接続時の最適化された挙動
  - バスおよびロジック端子は高インピーダンス (動作中のバスまたはアプリケーションに無負荷)
  - 電源オンおよびオフ時のグリッチ・フリー動作

2 アプリケーション

- ボディ・エレクトロニクスとライティング
- インフォテインメント / クラスタ
- 産業用輸送
- 非軍事目的ドローン

3 概要

TCAN4551-Q1 は、最高 8Mbps のデータ・レートをサポートする CAN FD トランシーバを内蔵した CAN FD コントローラです。この CAN FD コントローラは、ISO11898-1:2015 高速コントローラ・エリア・ネットワーク (CAN) データ・リンク層の仕様と、ISO11898–2:2016 高速 CAN 仕様の物理層の要件を満たしています。TCAN4551-Q1 は、シリアル・ペリフェラル・インターフェイス (SPI) を経由して、CAN バスとシステム・プロセッサとの間のインターフェイスとして機能し、Classic CAN と CAN FD の両方をサポートします。これにより、CAN および CAN FD のポートの拡張や CAN FD をサポートしていないプロセッサでの CAN のサポートが可能になります。TCAN4551-Q1 は、CAN FD トランシーバの機能 (バスへの差動送信、バスからの差動受信) を提供します。このデバイスは、ローカル・ウェイクアップ (LWU) によるウェイクアップと、ISO11898-2:2016 ウェイクアップ・パターン (WUP) を実装した CAN バスを使用するウェイクアップをサポートしています。

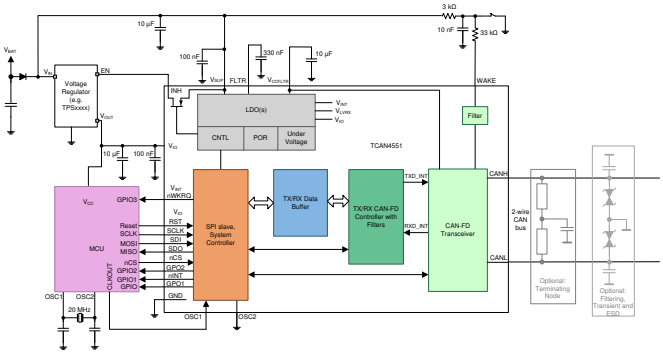
このデバイスには多くの保護機能が組み込まれているため、デバイスと CAN バスの堅牢性を確保できます。このような保護機能の例として、フェイルセーフ機能、内部ドミナント状態タイムアウト広いバス動作範囲などが挙げられます。

製品情報(1)

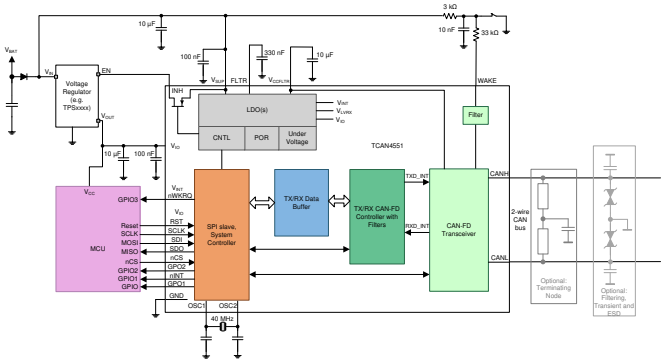
型番	パッケージ	本体サイズ (公称)
TCAN4551-Q1	VQFN (20)	4.50mm×3.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図、MUC から CLKIN



概略回路図、水晶振動子



目次

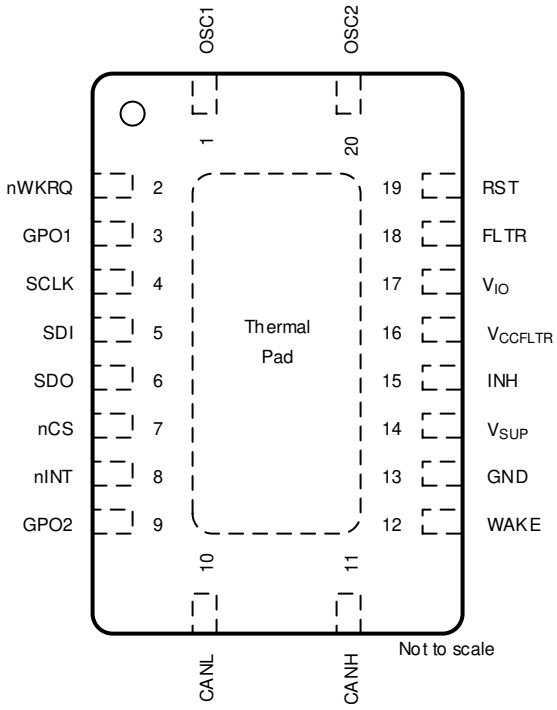
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2019 年 8 月	*	初版

5 Pin Configuration and Functions

RGY Package
20 Pin (VQFN)
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	OSC1	I	External crystal oscillator or clock input
2	nWKRQ	DO	Wake request (active low)
3	GPO1	DO	Configurableoutput function pin through SPI
4	SCLK	DI	SPI clock input
5	SDI	DI	SPI slave data input from master output
6	SDO	DO	SPI slave data output to master input
7	nCS	DI	SPI chip select
8	nINT	DO	Interrupt pin to MCU (active low)
9	GPO2	DO	Configurable output function pin through SPI
10	CANL	HV Bus I/O	Low level CAN bus line
11	CANH	HV Bus I/O	High level CAN bus line
12	WAKE	HVI	Wake input, high voltage input
13	GND	GND	Ground connection
14	V_{SUP}	HV Supply In	Supply from battery
15	INH	HVO	Inhibit to control system voltage regulators and supplies (open drain)
16	V_{CCFLTR}	Supply Filter	Internal 5 V regulator filter, requires external capacitor to ground
17	V_{IO}	Supply In	Digital I/O voltage supply
18	FLTR	—	Internal regulator filter, requires external capacitor to ground
19	RST	DI	Device reset
20	OSC2	O	External crystal oscillator output; when using single input clock to OSC1 this pin should be connected to ground

(1) Note: DI = Digital Input; DO = Digital Output; HV = High Voltage; Thermal PAD and GND Pins must be soldered to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage	–0.3	42	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN bus I/O voltage (CANH, CANL)	–58	58	V
V_{WAKE}	WAKE pin input voltage	–0.3	42	V
V_{INH}	Inhibit pin output voltage	–0.3	42	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{SO}	Digital output terminal voltage	–0.5	6	V
$I_{O(SO)}$	Digital output current		8	mA
$I_{O(INH)}$	Inhibit output current		4	mA
$I_{O(WAKE)}$	Wake current if due to ground shift $V_{(WAKE)} \leq V_{(GND)} – 0.3$ V		3	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level 3A per AEC Q100-002 All terminal except for CANH and CANL. (1) WAKE terminals which are with respect to ground only (2)		±4000	V
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level H2 for CANH and CANL (2)		±12000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM) classification level C5, per AEC Q100-011	All terminals	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Terminals stressed with respect to GND

6.3 ESD Ratings, IEC ESD and ISO Transient Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge according to IBEE CAN EMC (1)	Contact discharge	±8000	V
$V_{(ESD)}$	Electrostatic discharge according to SAEJ2962-2 (2)	Contact discharge	±8000	V
		Air discharge	±15 000	
ISO7637 Transients according to IBEE CAN EMC test spec CAN bus terminals (CANH and CANL), V_{SUP} and WAKE (3)		Pulse 1	-100	
		Pulse 2	75	
		Pulse 3a	-150	
		Pulse 3b	100	

(1) IEC 61000-4-2 is a system-level ESD test. Results given here are specific to the IBEE LIN EMC Test specification conditions per IEC TS 62228. Different system-level configurations may lead to different results
(2) SAEJ2962-2 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request.
(3) ISO7637 is a system-level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system-level configurations may lead to different results.

6.4 Recommended Operating Conditions

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{SUP}	Supply voltage	5.5		30	V

Recommended Operating Conditions (continued)

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IO}	Logic pin supply voltage	1.71		5.25	V
$I_{OH(DO)}$	Digital terminal high-level output current	–2			mA
$I_{OL(DO)}$	Digital terminal low-level output current			2	mA
$I_{O\ (INH)}$	INH output current			1	mA
$C_{(FLTR)}$	Filter pin capacitance See Power Supply Recommendations	300			nF
$C_{(VCCFLTR)}$	Internal 5 V regulator filter capacitance See Power Supply Recommendations	10			µF
C_{WAKE}	External WAKE pin capacitance	10			nF
T_{SDR}	Thermal shutdown rising	160			℃
T_{SDF}	Thermal shutdown falling			150	℃
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		℃

6.5 Thermal Information

THERMAL METRIC(1)		TCAN4551 PKG DES (RGY) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Supply Characteristics

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SUP}	Supply current, normal mode	Dominant	See 図 4 R_L = 60 Ω, C_L = open. typical bus load.			80	mA
			See 図 4 R_L = 50 Ω, C_L = open, high bus load.			90	mA
		Dominant with bus fault	See 図 4 CANH = - 25 V, R_L = open, C_L = open			180	mA
		Recessive	See 図 4 R_L = 60 Ω, C_L = open, R_{CM} = open,			15	mA
	Supply current, standby mode		See 図 4 R_L = 60 Ω, C_L = open, -40°C < T_A < 85°C, , CANH/L terminated to 2.5 V			3.5	mA
			See 図 4 RL = 60 Ω, C_L = open, -40°C < T_A < 85°C, CANH/L terminated to GND ± 100 mV			3.4	mA
I_{SUP}	Supply current, sleep mode		SPI bus, OSC/CLKIN disabled: -40°C < T_A < 85°C, V_{IO} = 0		25	42	µA
I_{VIO}	I/O supply current normal mode dominant	I/O supply current	CLKIN = 40 MHz, V_{IO} = 5 V			800	µA
			Crystal = 40 MHz, V_{IO} = 5 V			3	mA

Supply Characteristics (continued)

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VIO}	I/O supply current, sleep mode	I/O supply current	Sleep Mode V_{IO} = 5 V; OSC1 = CLKIN = 0 V and OSC2 = GND (1)			9	µA
UV_{SUP}	Under voltage detection on V_{SUP} rising ramp for protected mode		See Section Under Voltage Lockout (UVLO) and Unpowered Device		5.5	5.9	V
	Under voltage detection on V_{SUP} falling ramp for protected mode			4.5	4.7		V
t_{TSD}	Thermal shutdown timer (2)	Thermal shutdown timer (2)	See section Thermal Shutdown for description of thermal shut down.	200		500	ms

(1) When a crystal is used this current will be higher until the crystal's capacitors bleed off their energy. How much current and length of time to bleed of the energy is system dependent and will not be specified.
(2) Specified by design

6.7 Electrical Characteristics

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
CAN DRIVER ELECTRICAL CHARACTERISTICS						
$V_{O(D)}$	Bus output voltage (dominant) CANH	See 図 4 and 図 5, TXD_INT = 0 V, EN = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
	Bus output voltage (dominant) CANL		0.5		2.25	V
$V_{O(R)}$	Bus output voltage (recessive)	See 図 2 and 図 5, TXD_INT = V_{IO}, R_L = open (no load), R_{CM} = open	2	2.5	3	V
$V_{(DIFF)}$	Maximum differential voltage rating	See 図 2 and 図 5	–5.0		10	V
$V_{O(STB)}$	Bus output voltage (Standby Mode) CANH	See 図 2 and 図 5, TXD_INT = V_{IO}, R_L = open (no load), R_{CM} = open	–0.1		0.1	V
	Bus output voltage (Standby Mode) CANL		–0.1		0.1	V
	Bus output voltage (Standby Mode) CANH - CANL		–0.2		0.2	V
$V_{OD(D)}$	Differential output voltage (dominant)	See 図 2 and 図 5, TXD_INT = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	V
		See 図 2 and 図 5, TXD_INT = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, R_{CM} = open	1.4		3	V
		See 図 2 and 図 5, TXD_INT = 0 V, R_L = 2.24 kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{OD(R)}$	Differential output voltage (recessive)	See 図 2 and 図 5, TXD_INT = V_{IO}, R_L = 60 Ω, C_L = open, R_{CM} = open	–120		12	mV
		See 図 2 and 図 5, TXD_INT = V_{IO}, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	mV
V_{SYM}	Output symmetry (dominant or recessive) (VO(CANH) + VO(CANL)) / VCC	See 図 2 and 図 5, R_L = 60 Ω, C_L = open, R_{CM} = open, C1 = 4.7 nF, TXD_INT - 250 kHZ, 1 MHz	0.9		1.1	V/V
V_{SYM_DC}	Output symmetry (dominant or recessive) (VCC – VO(CANH) – VO(CANL)) with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s)	See 図 2 and 図 5, R_L = 60 Ω, C_L = open, R_{CM} = open, C1 = 4.7 nF	–300		300	mV
IOS_DOM	Short-circuit steady-state output current, dominant	See 図 2 and 図 9, -3.0 V ≤ V_{CANH} ≤ 18.0 V, CANL = open, TXD_INT = 0 V	–100			mA
		See 図 2 and 図 9, -3.0 V ≤ V_{CANL} ≤+18.0 V, CANH = open, TXD_INT = 0 V			100	mA

(1) All TXD_INT, RXD_INT and EN_INT references are for internal nodes that represent the same functions for a physical layer transceiver.

Electrical Characteristics (continued)

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
IOS_REC	Short-circuit steady-state output current, recessive	See 図 2 and 図 9, – 27 V ≤ V_{BUS} ≤ 32 V, V_{BUS} = CANH = CANL	–5		5	mA
CAN RECEIVER ELECTRICAL CHARACTERISTICS						
V_{ITdom}	Receiver dominant state differential input voltage range, bus biasing active	-12.0 V ≤ V_{CANL} ≤ +12.0 V -12.0 V ≤ V_{CANH} ≤ +12.0 V See 図 6, 表 2	0.9		8	V
V_{ITrec}	Receiver recessive state differential input voltage range bus biasing active		–3.0		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal modes	See 図 6, 表 2		120		mV
$V_{IT(ENdom)}$	Receiver dominant state differential input voltage range, bus biasing inactive (VDiff)	-12.0 V ≤ V_{CANL} ≤ +12.0 V -12.0 V ≤ V_{CANH} ≤ +12.0 V See 図 6, 表 2	1.15		8	V
$V_{IT(ENrec)}$	Receiver recessive state differential input voltage range, bus biasing inactive (VDiff)	-12.0 V ≤ V_{CANL} ≤ +12.0 V -12.0 V ≤ V_{CANH} ≤ +12.0 V See 図 6, 表 2	–3		0.4	V
V_{CM}	Common mode range: normal	See 図 6, 表 2	–12		12	V
$V_{CM(EN)}$	Common mode range: standby mode	See 図 6, 表 2	–12		12	V
$I_{IOFF(LKG)}$	Power-off (unpowered) bus input leakage current	V_{CANH} = V_{CANL} = 5 V, V_{sup} to GND via 0 Ω and 47 kΩ resistor			5	µA
C_I	Input capacitance to ground (CANH or CANL)				25	pF
C_{ID}	Differential input capacitance				14	pF
R_{ID}	Differential input resistance	TXD_INT = V_{CCINT}, normal mode: -2.0 V ≤ V_{CANH} ≤+7.0 V; -2.0 V ≤V_{CANL} ≤ + 7.0 V	60		100	kΩ
R_{IN}	Single ended Input resistance (CANH or CANL)	-2.0 V ≤ V_{CANH} ≤+7.0 V; -2.0 V ≤V_{CANL} ≤ + 7.0 V	30		50	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – ($R_{IN(CANH)}$) / ($R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5.0 V	–1		1	%
V_{CCFLTR} TERMINAL						
$V_{MEASURE}$	Voltage measured at VCCFLTR terminal		4.75	5	5.25	V
FLTR TERMINAL						
$V_{MEASURE}$	Voltage measured at FLTR pin			1.5		V
$C_{(FLTR)}$	Filter pin capacitor	External filter capacitor	300	330		nF
INH OUTPUT TERMINAL (HIGH VOLTAGE OUTPUT)						
ΔV_H	High-level voltage drop INH with respect to V_{SUP}	I_{INH} = - 0.5 mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current	INH = 0 V, Sleep Mode	–0.5		0.7	µA
WAKE INPUT TERMINAL (HIGH VOLTAGE INPUT)						
V_{IH}	High-level input voltage	Standby mode, WAKE pin enabled	V_{SUP}–2			V
V_{IL}	Low-level input voltage	Standby mode, WAKE pin enabled			V_{SUP}–3	V
I_{IH}	High-level input current	WAKE = V_{SUP}–1 V	–25	–15		µA
I_{IL}	Low-level input current	WAKE = 1 V		15	25	µA
t_{WAKE}	WAKE filter time	Wake up filter time from a wake edge on WAKE; standby, sleep mode	50			µs
SDI, SCK, GPO1 INPUT TERMINALS						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	Inputs = V_{IO} = 5.25 V	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{IO} = 5.25 V	–100		–5	µA
C_{IN}	Input capacitance	18 MHz		10	12	pF

Electrical Characteristics (continued)

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
$I_{LKG(OFF)}$	Unpowered leakage current (SDI and SCK only)	Inputs = 5.25 V, V_{IO} = V_{SUP} = 0 V	–1		1	µA
nCS INPUT TERMINAL						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	nCS = V_{IO} = 5.25 V	–1		1	µA
I_{IL}	Low-level input leakage current	nCS = V_{IO} = 5.25 V	–50		–5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	nCS = 5.25 V, V_{IO} = V_{SUP} = 0 V	–1		1	µA
RST INPUT TERMINAL						
V_{IH}	High-level input voltage		0.7			V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
I_{IH}	High-level input leakage current	RST = V_{IO} = 5.25 V	1		10	µA
I_{IL}	Low-level input leakage current	RST = 0 V	–1		1	µA
$I_{LKG(OFF)}$	Unpowered leakage current	RST = V_{IO}, V_{SUP} = 0 V	–7.5		7.5	µA
t_{PULSE_WIDTH}	Width of the input pulse		30			µs
SDO, GPO1, GPO2 OUTPUT TERMINAL; nINT (OPEN DRAIIN) and nWKRQ (WHEN PROGRAMMED TO WORK OFF OF VIO AND IS OPEN DRAIN)						
V_{OH}	High-level output voltage		0.8			V_{IO}
V_{OL}	Low-level output voltage				0.2	V_{IO}
nWKRQ OUTPUT TERMINAL (DEFAULT INTERNAL VOLTAGE RAIL)						
V_{OH}	High-level output voltage	Default value when based upon internal voltage rail	2.8		3.6	V
V_{OL}	Low-level output voltage	Default value when based upon internal voltage rail			0.7	V
OSC1 TERMINAL AND CRYSTAL SPECIFICATION						
V_{IH}	High-level input voltage		0.85		1.10	V_{IO}
V_{IL}	Low-level input voltage				0.3	V_{IO}
F_{OSC1}	Clock-In frequency tolerance , see section Crystal and Clock Input Requirements	20 MHz	–0.5		0.5	%
F_{OSC1}	Clock-In frequency tolerance, see section Crystal and Clock Input Requirements	40 MHz	–0.5		0.5	%
t_{DC}	Input duty cycle		45		55	%
ESR	Crystal ESR for load capacitance (2)				60	Ω

(2) Specified by design

6.8 Timing Requirements

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

		MIN	TYP	MAX	UNIT
MODE CHANGE TIMES (FULL DEVICE)					
$t_{MODE\_STBY\_NOM}$	Standby to normal mode change time based upon SPI write			70	µs
$t_{MODE\_NOM\_SLP}$	SPI write to go to Sleep from Normal: INH and nWKRQ turned off, See			200	µs
$t_{MODE\_SLP\_STBY}$	WUP or LWU event until INH and nWKRQ asserted, See			200	µs
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode, See			200	µs

6.9 Switching Characteristics

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS (CAN TRANSCEIVER ONLY)						
t_{pHR}	Propagation delay time, high TXD_INT to Driver Recessive (1)	See 図 5, RST = 0 V. Typical conditions: R_L = 60 Ω, C_L = 100 pF, R_{CM} = open	50	85	110	ns
t_{pLD}	Propagation delay time, low TXD_INT to driver dominant (1)		35	75	100	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHR} - t_{pLD}\|$)			30	40	ns
$t_{R/F}$	Differential output signal rise time:		8	55	75	ns
t_{pRH}	Propagation delay time, bus recessive input to high RXD_INT output	See 図 6, typical conditions: CANL = 1.5 V, CANH = 3.5 V.	35	55	90	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD_INT low output		35	55	90	ns
t_{pHR}	Propagation delay time, high TXD_INT to Driver Recessive (1)	See 図 5, RST = 0 V. Typical conditions: R_L = 60 Ω, C_L = 100 pF, R_{CM} = open V_{IO} = 1.8 V	50	85	120	ns
t_{pLD}	Propagation delay time, low TXD_INT to driver dominant (1)		35	75	110	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHR} - t_{pLD}\|$)			30	40	ns
$t_{R/F}$	Differential output signal rise time:		8	55	75	ns
t_{pRH}	Propagation delay time, bus recessive input to high RXD_INT output	See 図 6, typical conditions: CANL = 1.5 V, CANH = 3.5 V. V_{IO} = 1.8 V	35	55	105	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD_INT low output		35	55	105	ns
DEVICE SWITCHING CHARACTERISTICS						
t_{LOOP}	Loop delay(2)(CAN transceiver only)	See 図 7, RST = 0 V. typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF			235	ns
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake up request	See 図 23, standby mode.	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout: time that a WUP must take place within to be considered valid	See 図 23	0.5		2.9	ms
$t_{SILENCE}$	Timeout for bus inactivity (3)	Timer is reset and restarted when bus changes from dominant to recessive or vice versa.	0.6		1.2	s
$t_{INACTIVE}$	Time required for the processor to clear wake flag or put the device into normal mode upon power up, power on reset or after wake event otherwise the device will enter sleep mode (3)		2	4	6	min
t_{Bias}	Time from the start of a dominant-recessive-dominant sequence	Each phase 6 µs until V_{sym} ≥ 0.1. See 図 11			250	µs
t_{Power_Up}	Power up time on V_{SUP} (3)	See 図 14			250	µs
$t_{TXD\_INT\_DTO}$	Dominant time out(4) (CAN transceiver only)(1)	See 図 24, R_L = 60 Ω, C_L = open	1		5	ms
TRANSMITTER AND RECEIVER SWITCHING CHARACTERISTICS						

(1) All TXD_INT, RXD_INT, EN_INT and CAN transceiver only references are for internal nodes that represent the same functions for a stand-alone transceiver.
(2) Time span from signal edge on TXD_INT input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.
(3) Specified by design
(4) The TXD_INT dominant time out ($t_{TXD\_INT\_DTO}$) disables the driver of the transceiver once the TXD_INT has been dominant longer than $t_{TXD\_INT\_DTO}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD_INT has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD_INT) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{TXD\_INT\_DTO}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{TXD\_INT\_DTO}$ = 11 bits / 1.2 ms = 9.2 kbps.

Switching Characteristics (continued)

over operating free-air temperature range for – 40 ℃ ≤ T_A ≤ 125 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Bit(Bus)2M}$	Transmitted recessive bit width @ 2 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF	435		530	ns
$t_{Bit(Bus)5M}$	Transmitted recessive bit width @ 5 Mbps		155		210	ns
$t_{Bit(Bus)8M}$ (5)	Transmitted recessive bit width @ 8 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} ≥ 3.135 V	80		135	ns
$t_{Bit(Bus)8M}$ (5)	Transmitted recessive bit width @ 8 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} = 1.8 V	80		135	ns
$t_{Bit(RXD)2M}$	Received recessive bit width @ 2 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF,V_{IO} ≥ 3.135 V	400		550	ns
$t_{Bit(RXD)5M}$	Received recessive bit width @ 5 Mbps		120		220	ns
$t_{Bit(RXD)2M}$	Received recessive bit width @ 2 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} = 1.8 V	394		550	ns
$t_{Bit(RXD)5M}$	Received recessive bit width @ 5 Mbps		114		220	ns
$t_{Bit(RXD)8M}$ (5)	Received recessive bit width @ 8 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} ≥ 3.135 V	80		135	ns
$t_{Bit(RXD)8M}$ (5)	Received recessive bit width @ 8 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} = 1.8 V	72		135	ns
Δt_{Rec} (6)	Receiver Timing symmetry @ 2 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} ≥ 3.135 V	–65	30	40	ns
	Receiver Timing symmetry @ 5 Mbps		–45	5	15	ns
Δt_{Rec} (6)	Receiver Timing symmetry @ 2 Mbps	See 図 6, RST = 0 V typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF, V_{IO} 1.8 V	–71	30	40	ns
	Receiver Timing symmetry @ 5 Mbps		–51	5	15	ns
SPI SWITCHING CHARACTERISTICS						
f_{SCK}	SCK, SPI clock frequency (3)				18	MHz
t_{SCK}	SCK, SPI clock period (3)	See 図 13	56			ns
t_{RSCK}	SCK rise time (3)	See 図 12			10	ns
t_{FSCK}	SCK fall time (3)	See 図 12			10	ns
t_{SCKH}	SCK, SPI clock high (3)	See 図 13	18			ns
t_{SCKL}	SCK, SPI clock low (3)	See 図 13	18			ns
t_{CSS}	Chip select setup time (3)	See 図 12	28			ns
t_{CSH}	Chip select hold time (3)	See 図 12	28			ns
t_{CSD}	Chip select disable time (3)	See 図 12	125			ns
t_{SISU}	Data in setup time (3)	See 図 12	5			ns
t_{SIH}	Data in hold time (3)	See 図 12	10			ns
t_{SOV}	Data out valid (3)	See 図 13			20	ns
t_{RSO}	SO rise time (3)	See 図 13			10	ns
t_{FSO}	SO fall time (3)	See 図 13			10	ns

(5) Characterized but not 100% tested
(6) $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

6.10 Typical Characteristics

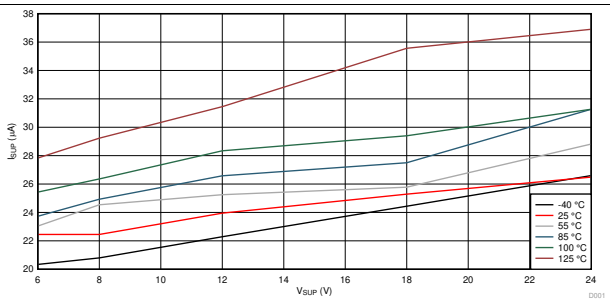


図 1. I_{SUP} vs V_{SUP} Sleep Mode

7 Parameter Measurement Information

注

All TXD_INT, RXD_INT and EN_INT references are for internal nodes that represent the same functions for a physical layer transceiver. In test mode these can be brought out to pins to test the transceiver or CAN FD controller.

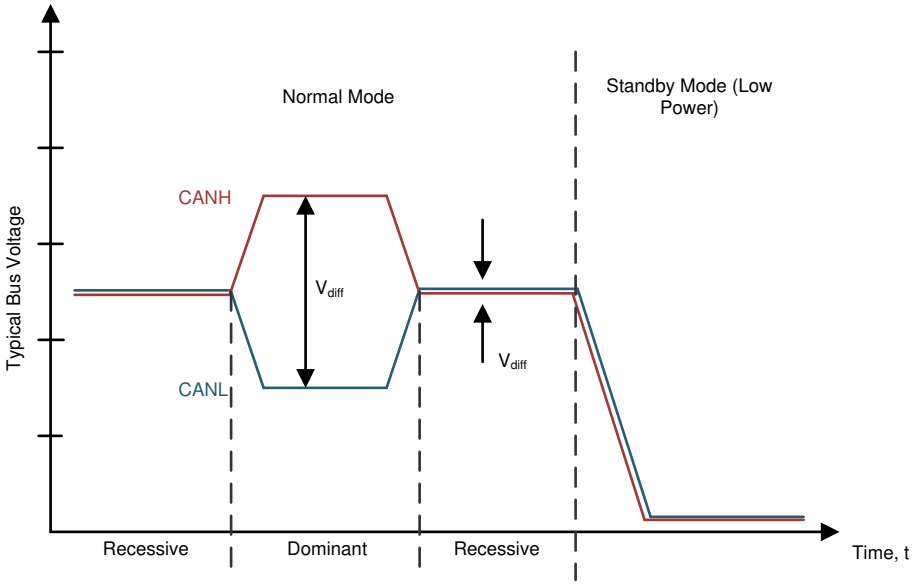


図 2. Bus States (Physical Bit Representation)

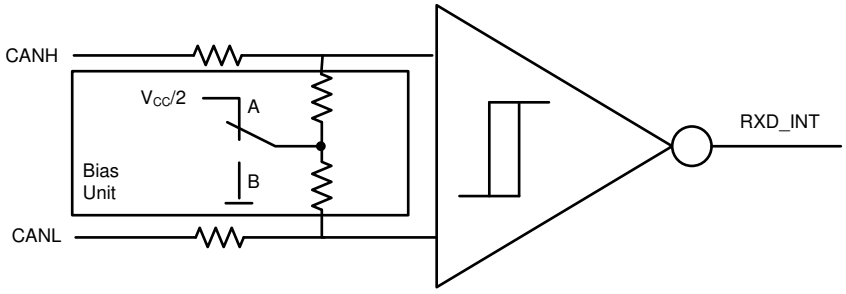


図 3. Simplified Recessive Common Mode Bias Unit and Receiver

Parameter Measurement Information (continued)

注

A: Classic CAN and CAN FD modes

B: Standby and Sleep Modes (Low Power)

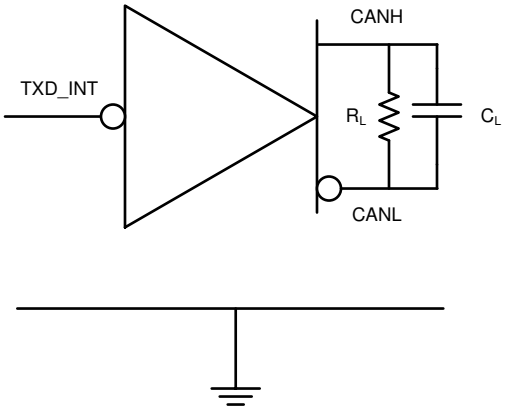


図 4. Supply Test Circuit

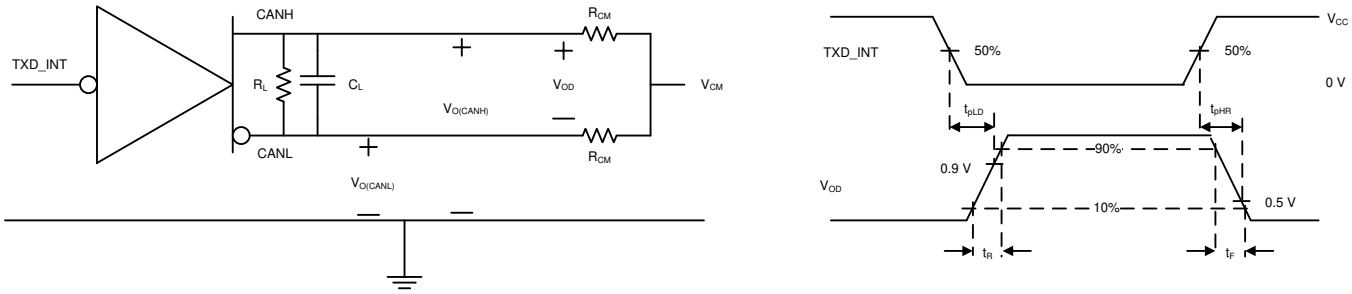


図 5. Driver Test Circuit and Measurement

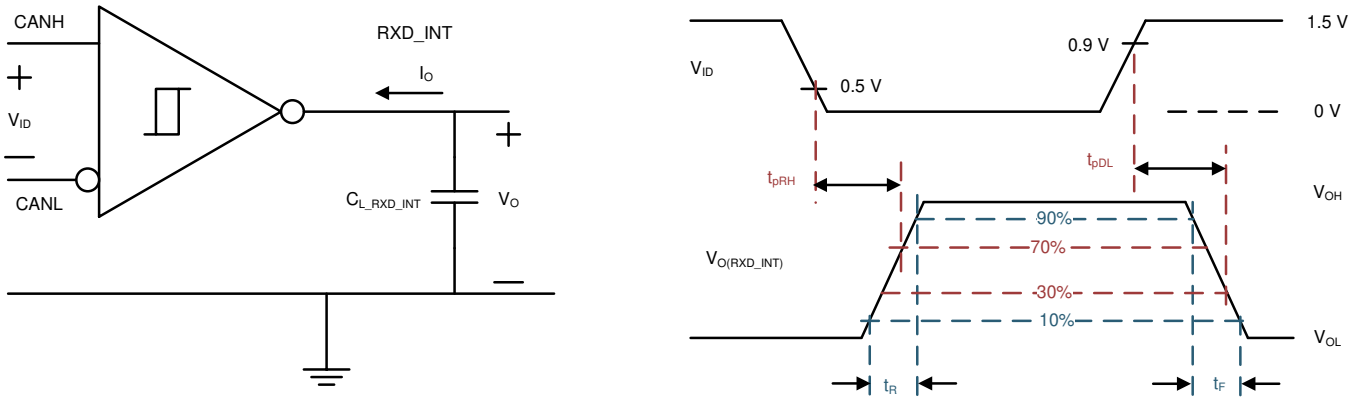


図 6. Receiver Test Circuit and Measurement

Parameter Measurement Information (continued)

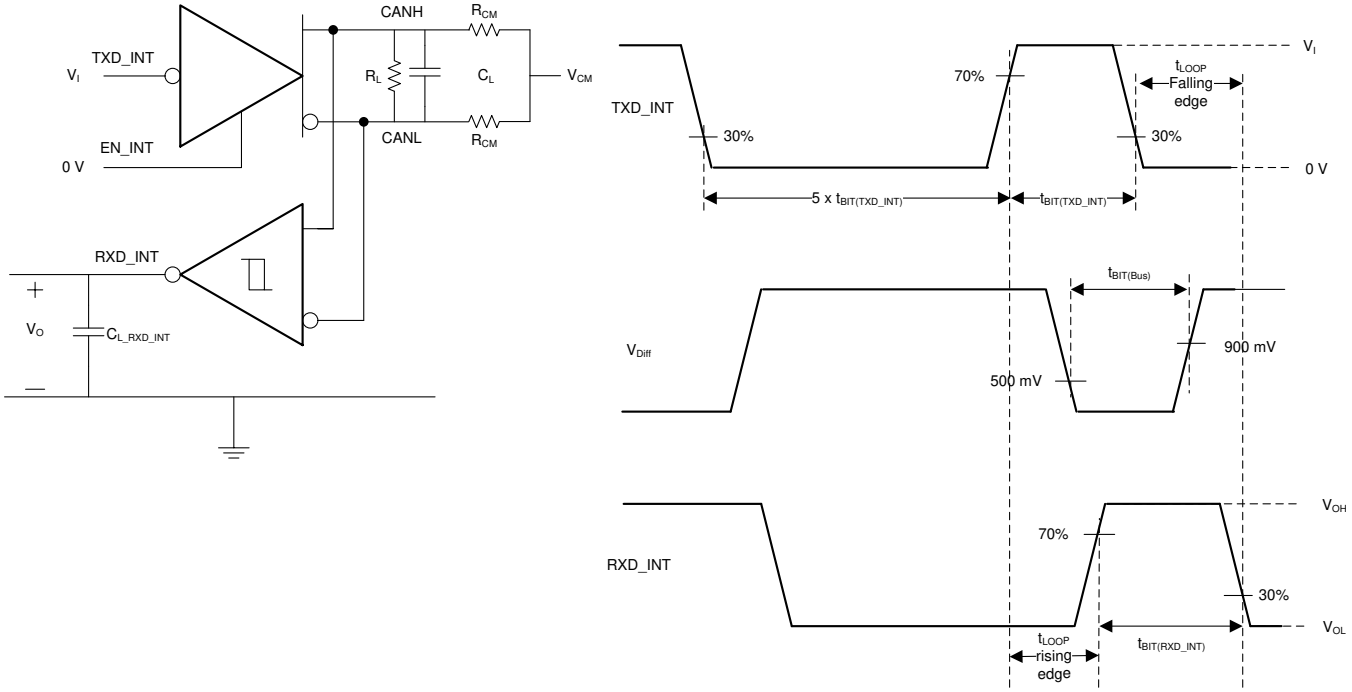


図 7. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

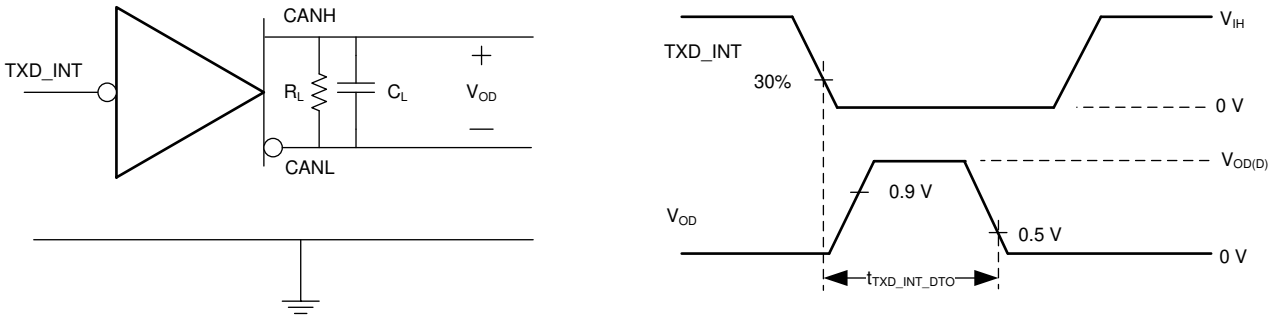


図 8. TXD_INT Dominant Timeout Test Circuit and Measurement

Parameter Measurement Information (continued)

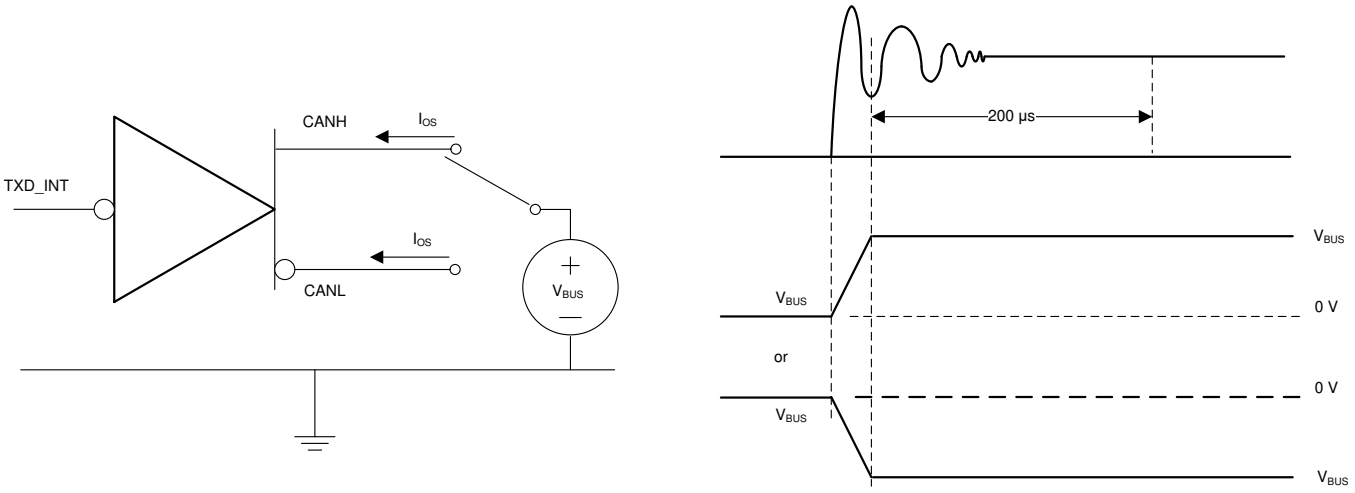


図 9. Driver Short-Circuit Current Test and Measurement

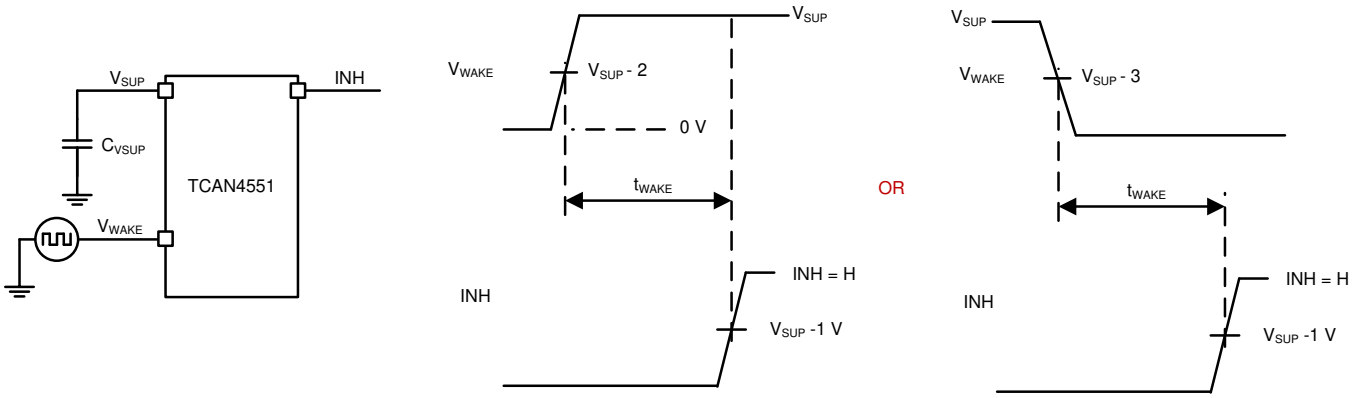


図 10. t_{WAKE} While Monitoring INH Output

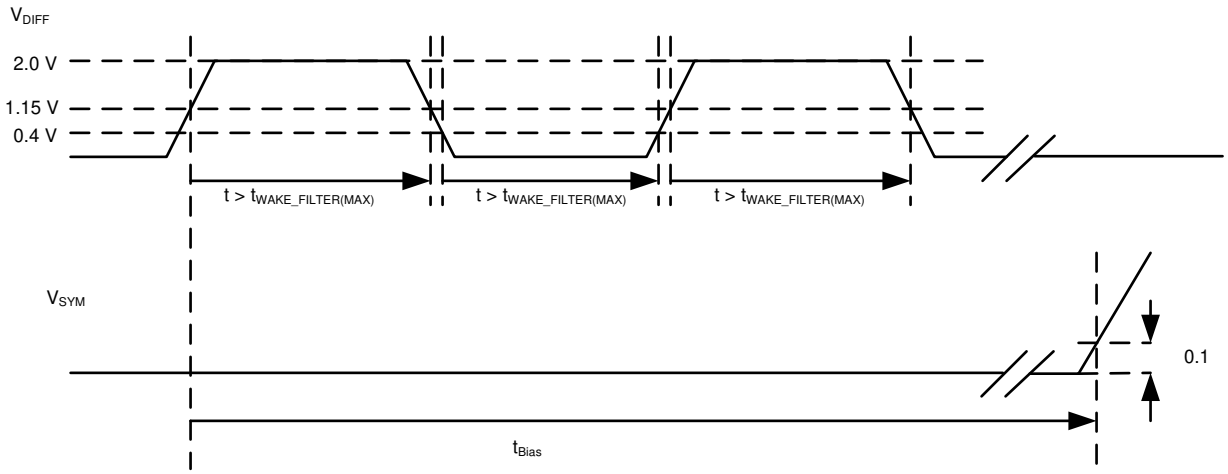


図 11. Test Signal Definition for Bias Reaction Time Measurement

Parameter Measurement Information (continued)

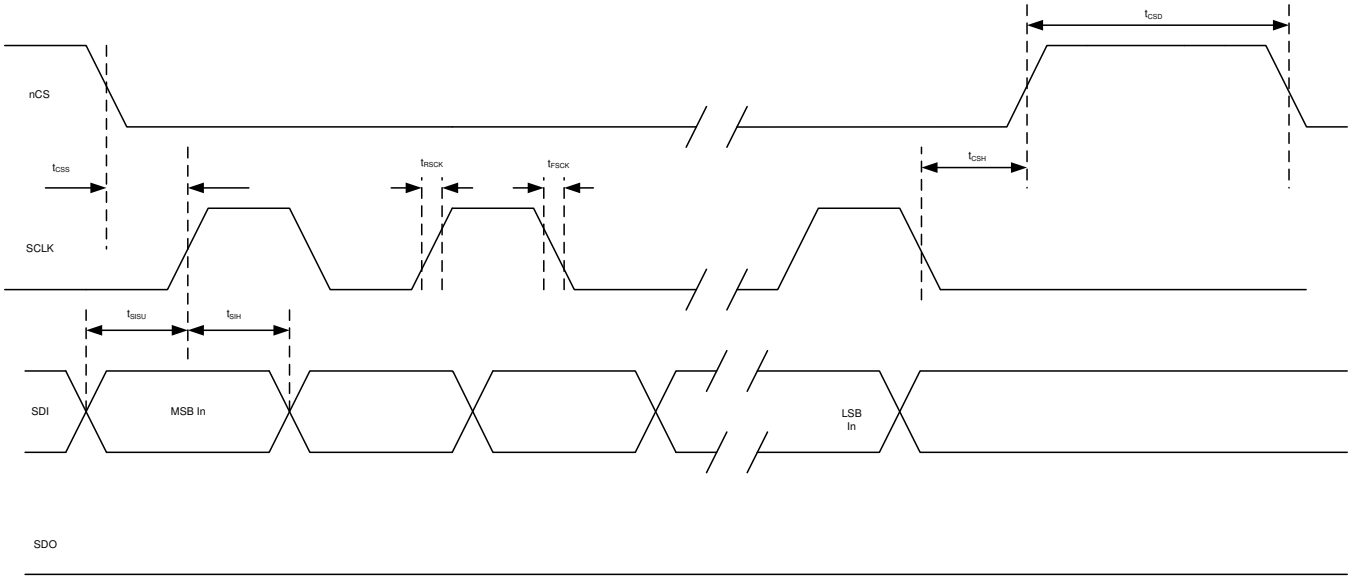


図 12. SPI AC Characteristic Write

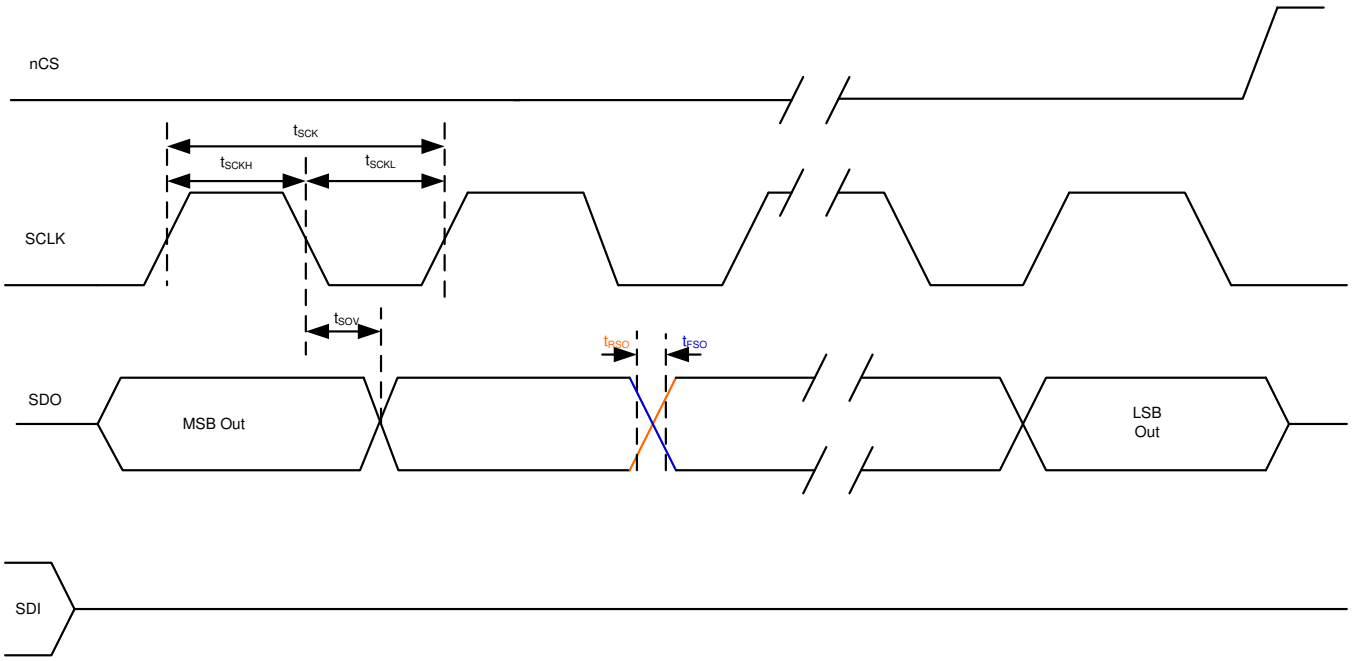


図 13. SPI AC Characteristic Read

Parameter Measurement Information (continued)

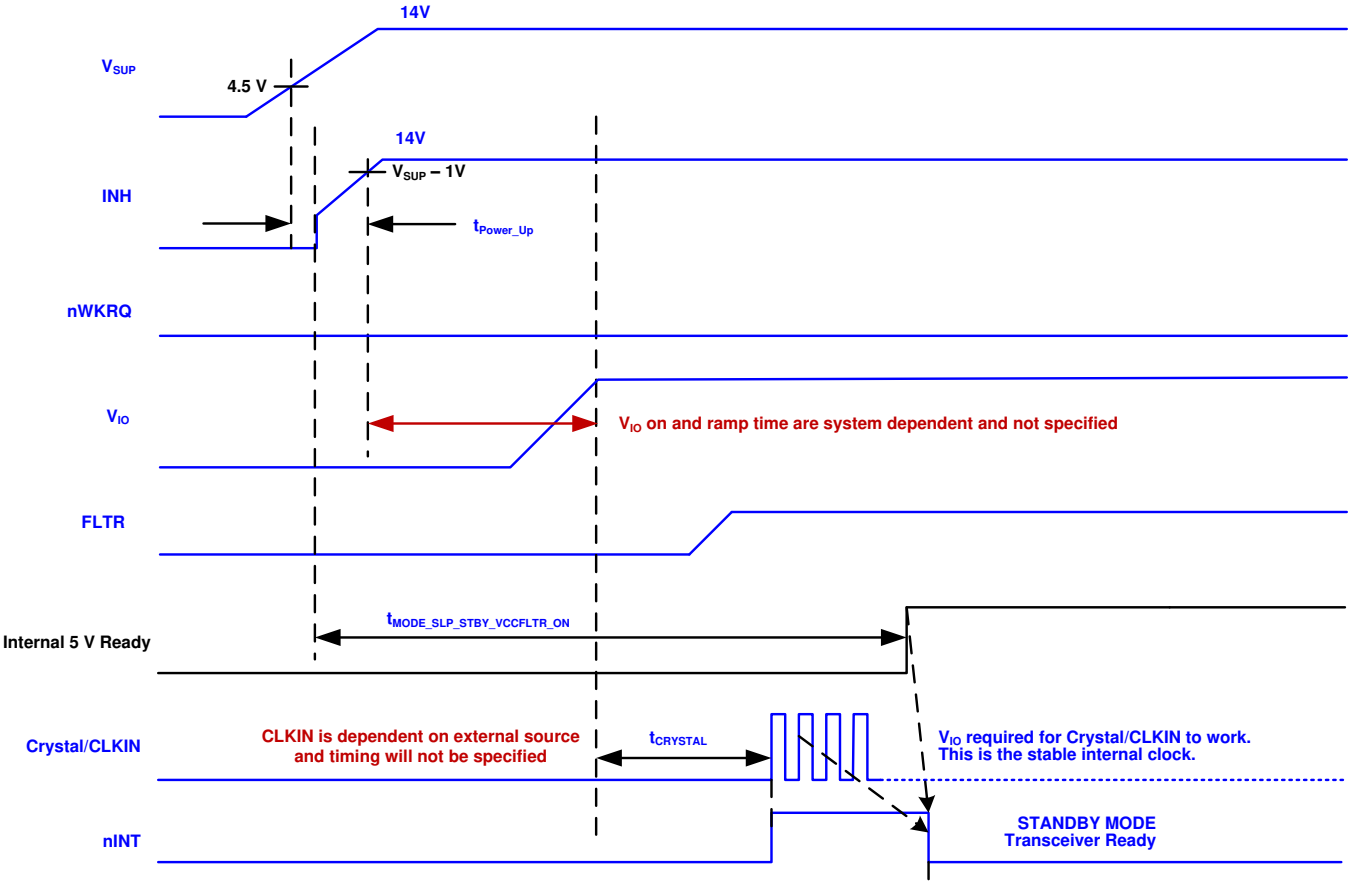


図 14. Power Up Timing

Parameter Measurement Information (continued)

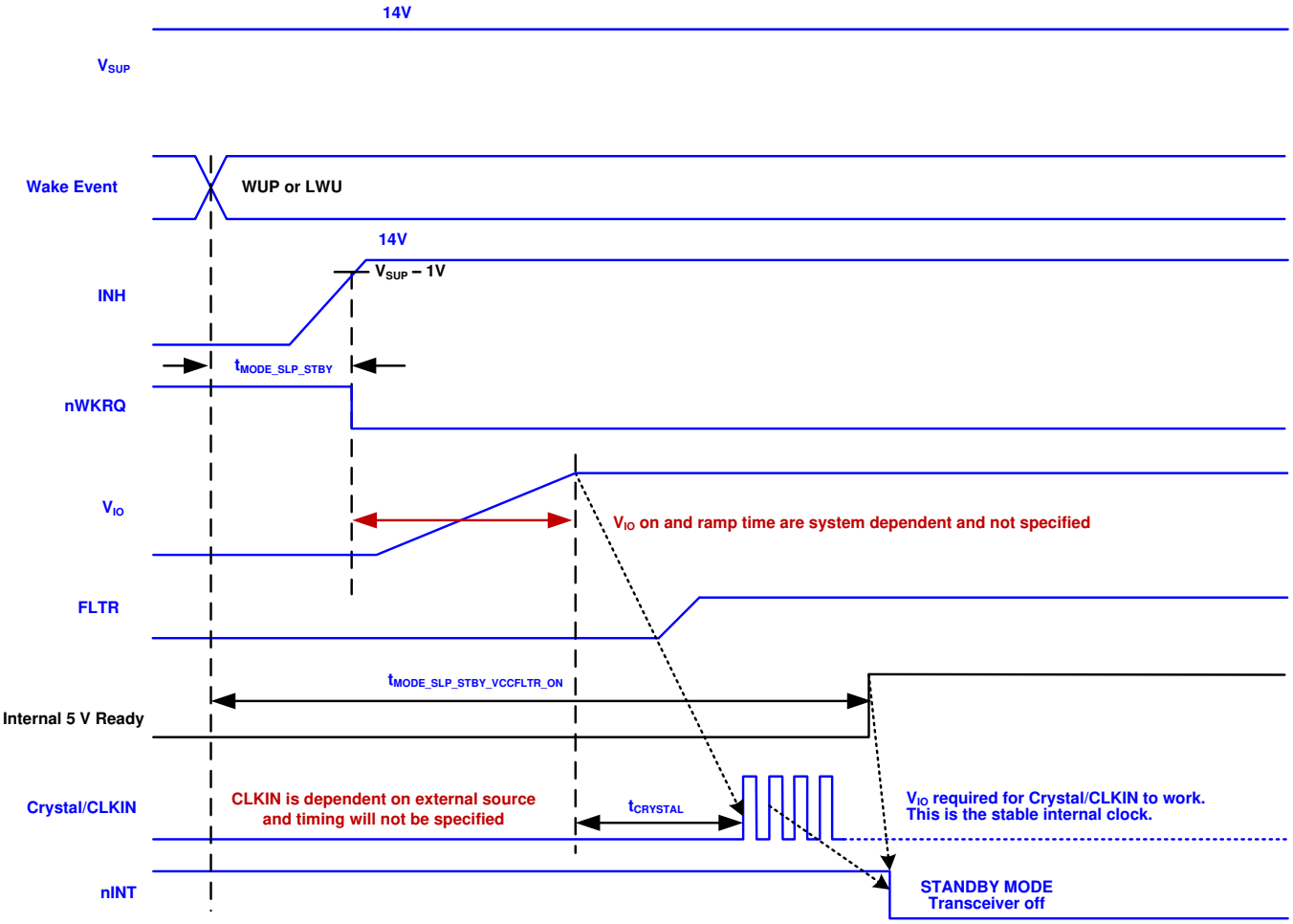


図 15. Sleep to Standby Timing

Parameter Measurement Information (continued)

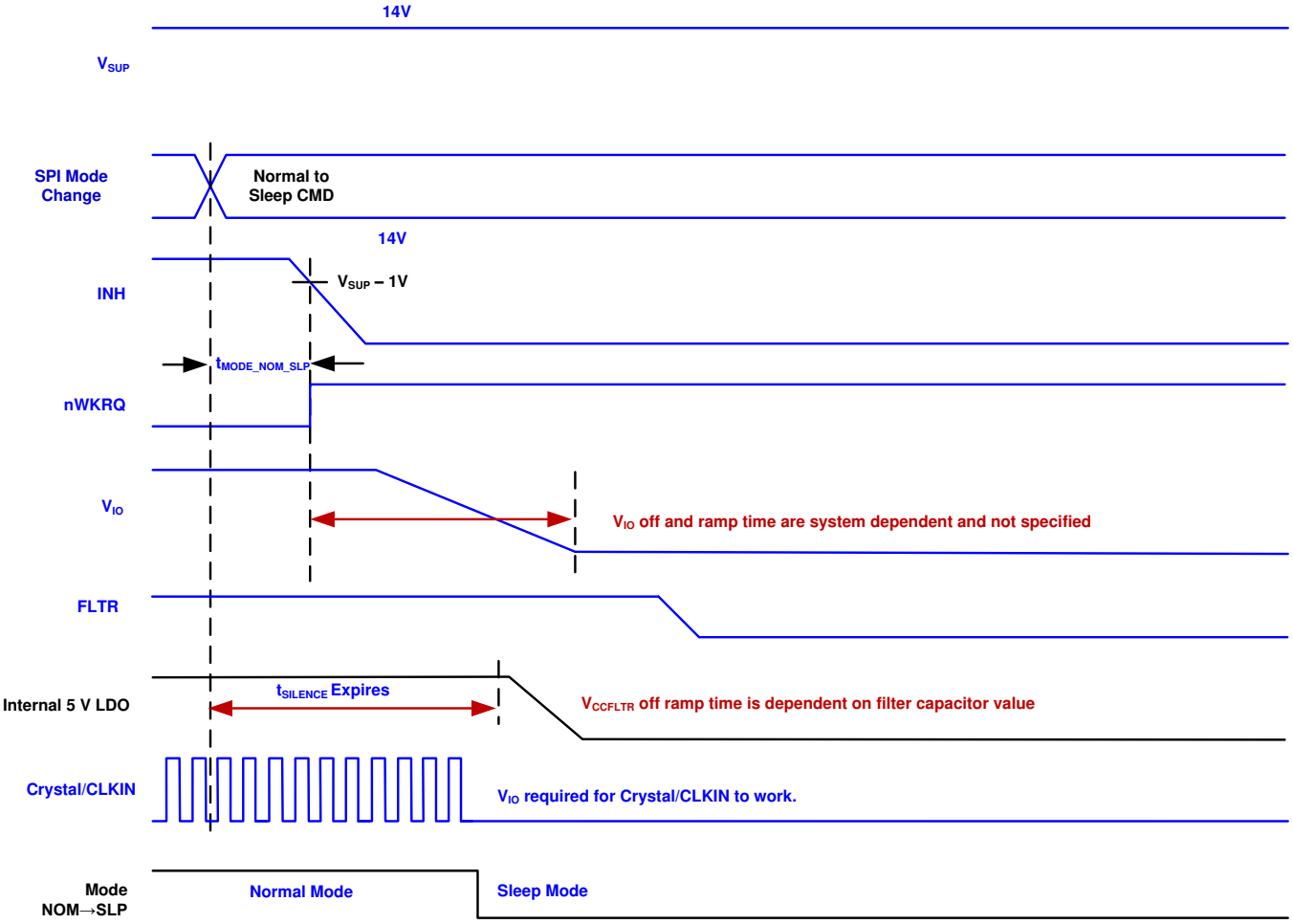


図 16. Normal to Sleep Timing

Parameter Measurement Information (continued)

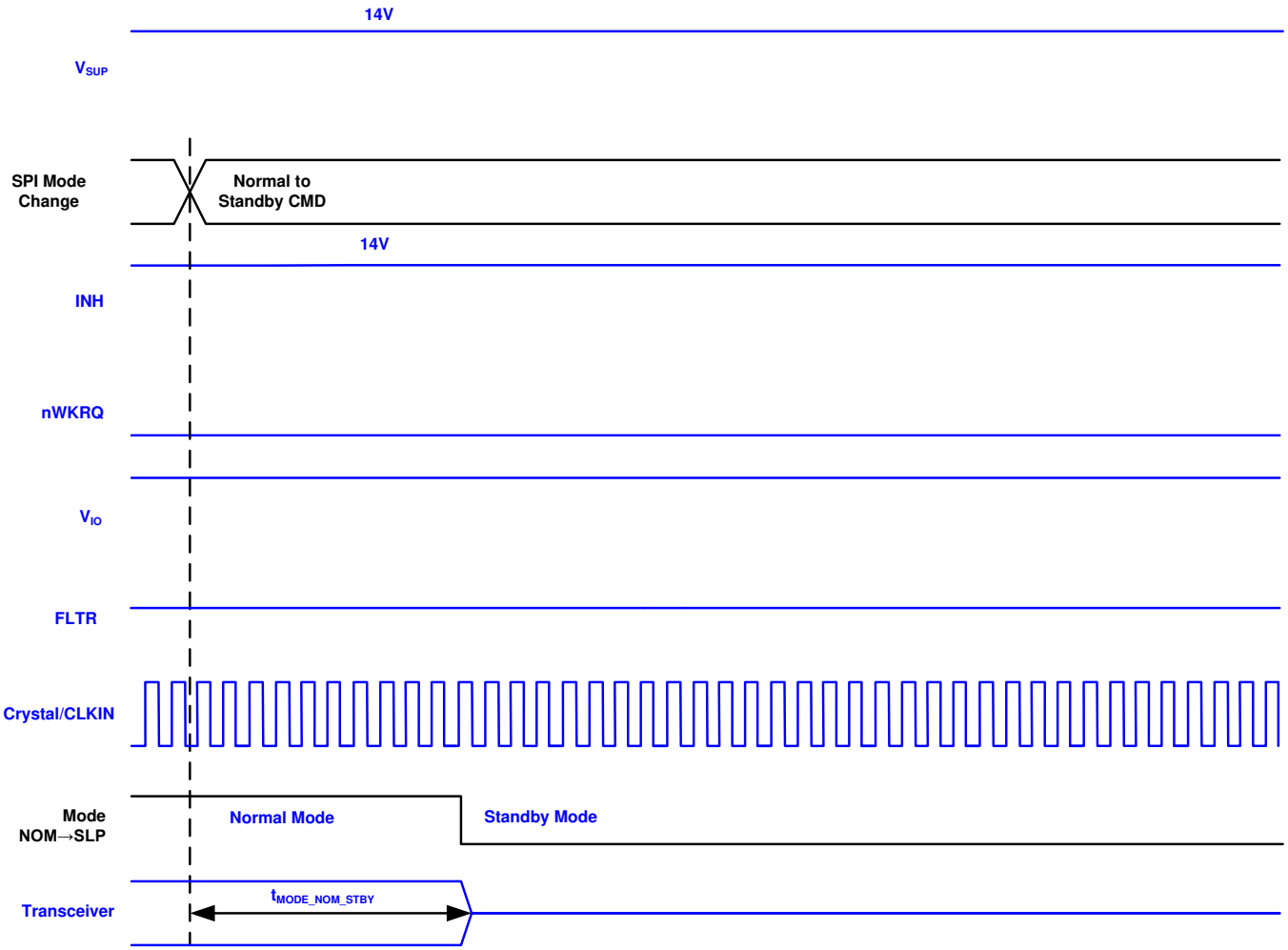


図 17. Normal to Standby Timing

8 Detailed Description

8.1 Overview

The TCAN4551-Q1 is a CAN FD controller with an integrated CAN FD transceiver supporting data rates up to 8 Mbps. The CAN FD controller meets the specifications of the ISO 11898-1:2015 high speed Controller Area Network (CAN) data link layer and meets the physical layer requirements of the ISO 11898-2:2016 High Speed Controller Area Network (CAN) specification providing an interface between the CAN bus and the CAN protocol controller supporting both classical CAN and CAN FD up to 5 megabits per second (Mbps). The TCAN4551-Q1 provides CAN FD transceiver functionality: differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features providing device and CAN bus robustness. The device can also wake up via remote wake up using CAN bus implementing the ISO 11898-2:2016 Wake Up Pattern (WUP). Input/Output support for 1.8 V, 3.3 V and 5 V microprocessors using V_{IO} pin for seamless interface. The TCAN4551-Q1 has a Serial Peripheral Interface (SPI) that connects to a local microprocessor for the device's configuration; transmission and reception of CAN frames. The SPI interface supports clock rates up to 18 MHz.

The CAN bus has two logical states during operation: recessive and dominant. See 図 2 and 図 3.

In the recessive bus state, the bus is biased to a common mode of 2.5 V via the high resistance internal input resistors of the receiver of each node. Recessive is equivalent to logic high. The recessive state is also the idle state.

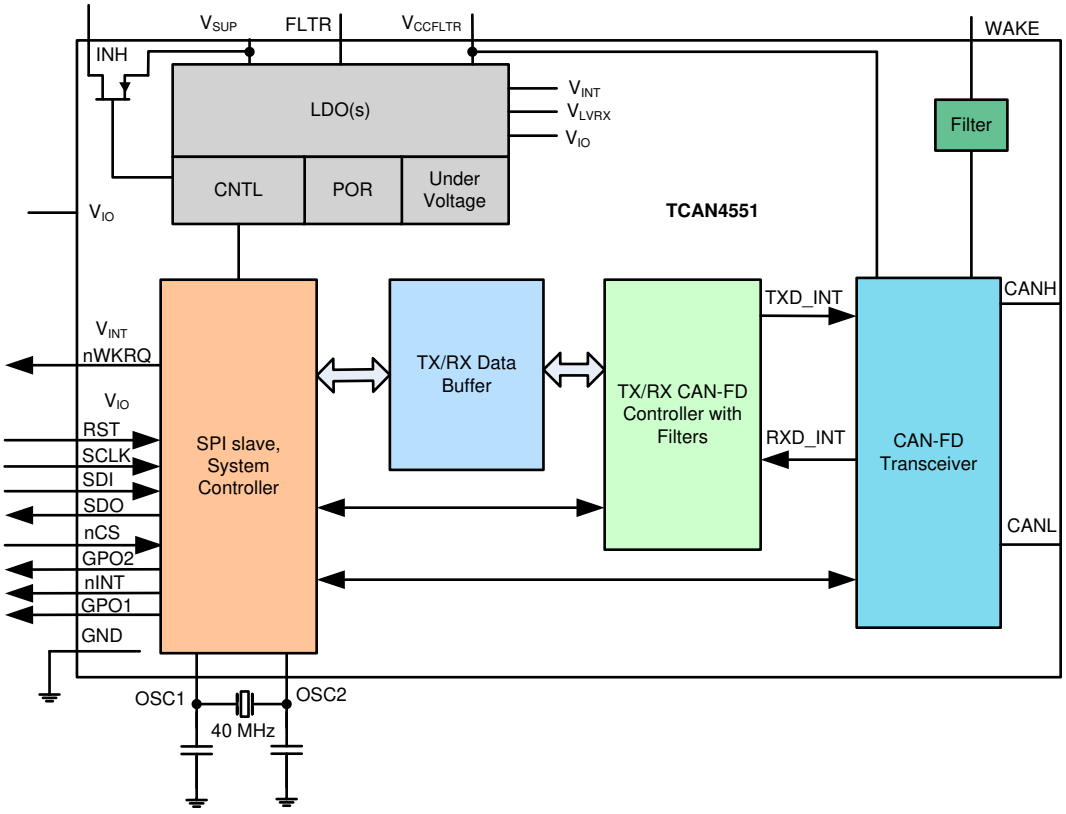
In the dominant bus state, the bus is driven differentially by one or more drivers. Current flows through the termination resistors and generates a differential voltage on the bus. Dominant is equivalent to logic low. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes may transmit a dominant bit at the same time. In this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

Transceivers with low power Standby Mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See 図 2 and 図 3. The TCAN4551-Q1 supports auto biasing, see CAN Bus Biasing

The TCAN4551-Q1 has the ability to configure many of the pins for multiple purposes and are described in more detail in Feature Description section. Much of the parametric data is based on internal links like the TXD/RXD_INT which represent the TXD and RXD of a standalone CAN transceiver. The TCAN4551-Q1 has a test mode that maps these signals to an external pin in order to perform compliance testing on the transceiver (TXD/RXD_INT_PHY) and CAN core (TXD/RXD_INT_CAN) independently.

8.2 Functional Block Diagram



注

- OSC1 pin is either a crystal or external clock input
- When OSC1 is used as an external clock input pin OSC2 must be connected directly to ground
- When using an external clock input on OSC1 the input voltage should be the same as the V_{IO} voltage rail
- The recommended crystal or clock rate to meet CAN FD 5 Mbps rates is 40 MHz

Functional Block Diagram (continued)

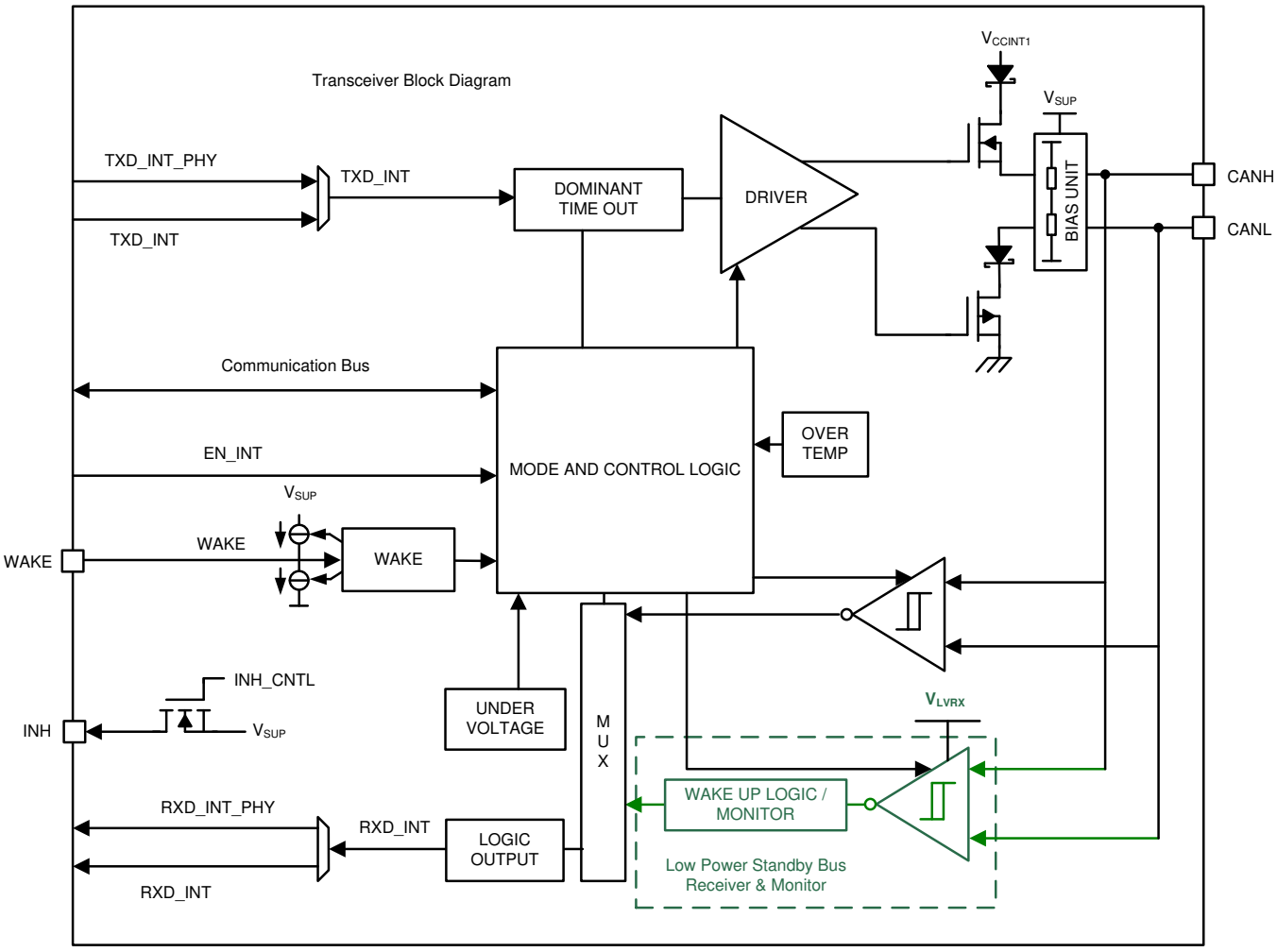


図 18. CAN Transceiver Block Diagram

Functional Block Diagram (continued)

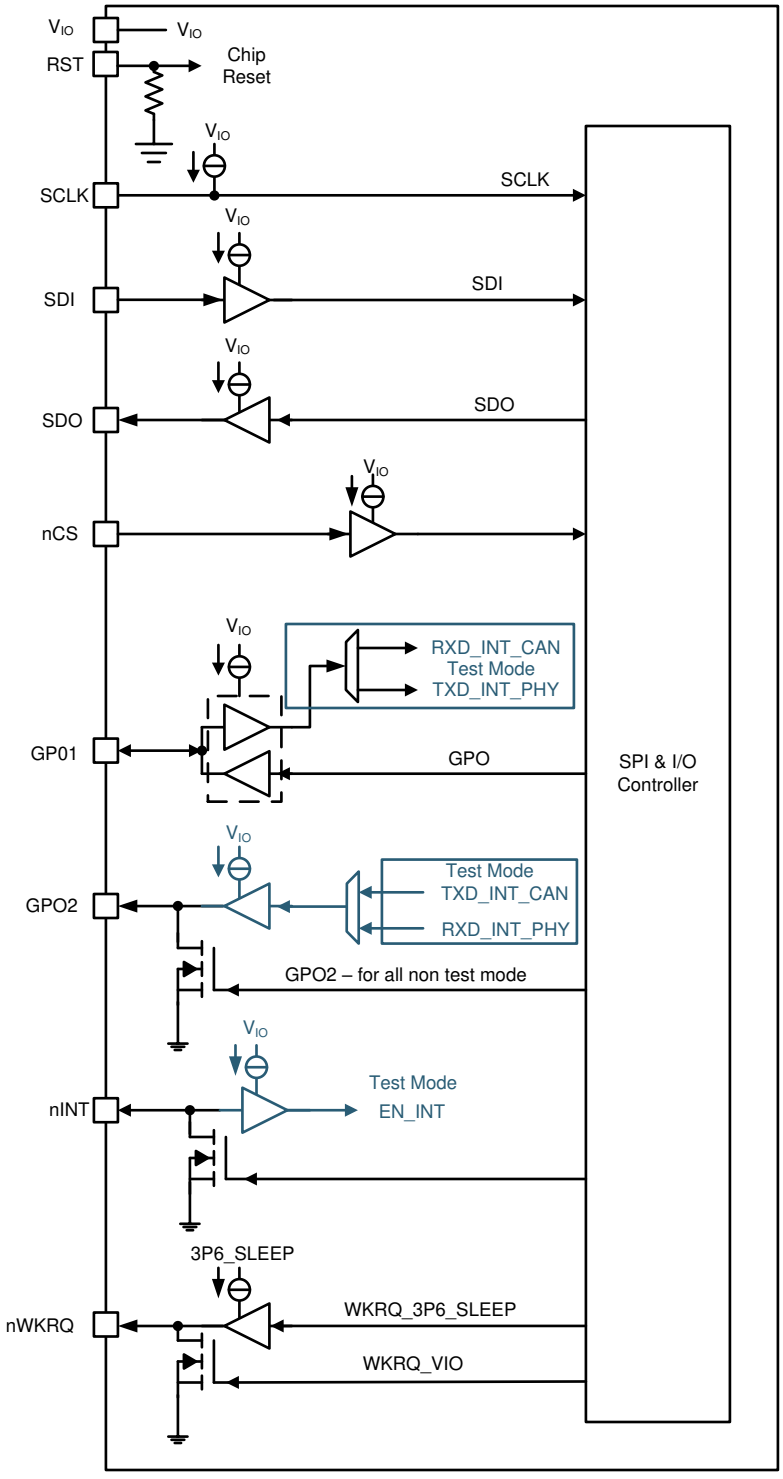


図 19. SPI and Digital IO Block Diagram

8.3 Feature Description

8.3.1 V_{SUP} Pin

This pin connects to the battery supply. It provides the supply to the internal regulators that support the digital core and CAN transceiver. This Pin requires a 100 nF capacitor at the pin. See Power Supply Recommendations for more information. Upon power up; V_{SUP} needs to rise above UV_{SUP} rising threshold.

8.3.2 V_{IO} Pin

The V_{IO} pin provides the digital IO voltage to match the microprocessor IO voltage thus avoiding the requirements for a level shifter. V_{IO} supports IO pins SPI IO, GPO1 and GPO2. It also provides power to the oscillator block supporting the crystal or CLKIN pins. It supports a range of 1.8 V to 5 V ±5 %, nominal value providing the widest range of controller support. This pin requires a 100 nF capacitor at the pin. See Power Supply Recommendations for more information.

8.3.3 GND

This pin is a ground pin as is the thermal pad. Both need to connect to a ground plane to support heat dissipation.

8.3.4 INH Pin

The INH pin is a high voltage output pin that provides voltage from the V_{SUP} minus a diode drop to enable an external high voltage regulator. These regulators are usually used to support the microprocessor and V_{IO} pin. The INH function is on in all modes but sleep mode. In sleep mode the INH pin is turned off, going into a high Z state. This allows the node to be placed into the lowest power state while in sleep mode. If this function is not required it can be disabled by setting register 16'h0800[9] = 1 using the SPI interface. If not required in the end application to initiate a system wake-up, INH can be left floating.

注

This terminal should be considered a "high voltage logic" terminal. It is not a power output thus should be used to drive the EN terminal of the system's power management device. It should be not used as a switch for power management supply itself. This terminal is not reverse battery protected and thus should not be connected outside of the system module.

8.3.5 WAKE Pin

The WAKE pin is used for a high voltage device local wake up (LWU). This function is explained further in Local Wake Up (LWU) via WAKE Input Terminal section. The pin is defaulted to bi-directional edge trigger, meaning it recognizes a LWU on either a rising or falling edge of WAKE pin transition. This default value can be changed via a SPI command that disables the function, make it a rising edge only or a falling edge only. This is done by using register 16'h0800[31:30]. Pin requires a 10 nF capacitor to ground for improved transient immunity in applications that route WAKE externally. If local wake-up functionality is not needed in the end application, WAKE can be tied directly to V_{SUP} or GND.

8.3.6 FLTR Pin

This pin is used to provide filtering for the internal digital core regulator. Pin requires 300 nF of capacitance to ground. See Power Supply Recommendations for more information.

8.3.7 V_{CCFLTR} Pin

This pin is used to provide filtering for the internal 5 V transceiver regulator. Pin requires 10 µF of capacitance to ground. See Power Supply Recommendations for more information.

Feature Description (continued)

8.3.8 RST Pin

The RST pin is a device reset pin. It has a weak internal pull down resistor for normal operation. If communication has stopped with the TCAN4551-Q1, the RST pin can be pulsed high and then back low for greater than t_{PULSE_WIDTH} to perform a power on reset to the device. This resets the device to the default settings and puts the device into standby mode. If the device was in normal or standby mode the INH and nWKRQ pins remain active (on) and do not toggle; see 図 20. If the device is in sleep mode and reset is toggled the device enters standby mode and at that time INH and nWKRQ turns on; see 図 21.

After a RST has taken place, a wait time of ≥ 700 µs should be used before reading or writing to the TCAN4551-Q1.

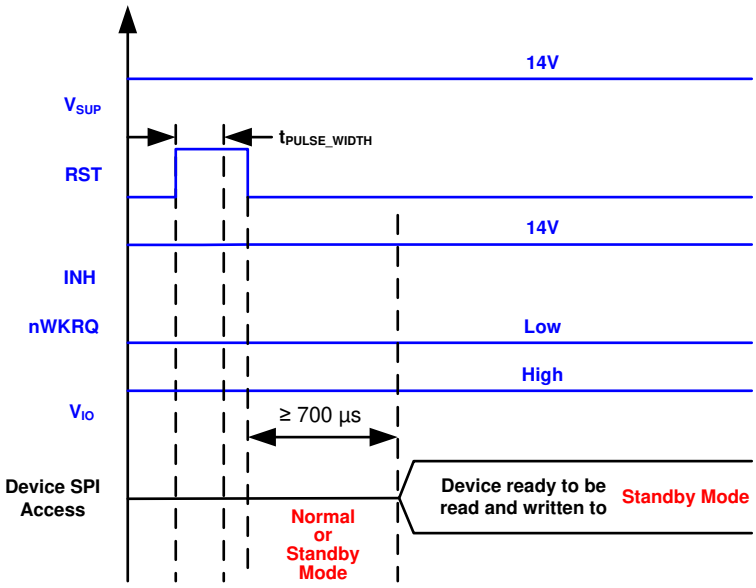


図 20. Timing for RST Pin in Normal and Standby Modes

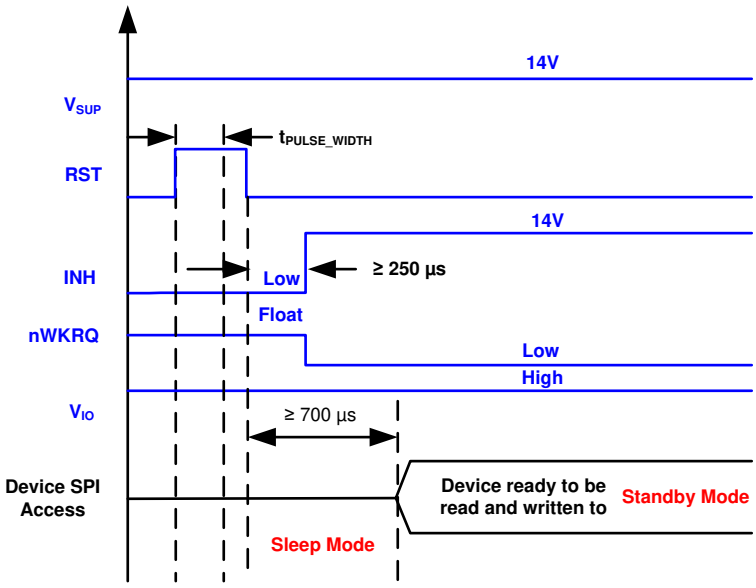


図 21. Timing for RST Pin in Sleep Mode

Feature Description (continued)

8.3.9 OSC1 and OSC2 Pins

These pins are used for a crystal oscillator. The OSC1 pin can also be used as a single-ended clock input from the microprocessor or some other clock source. See Application Design Consideration section for further information on the functions of these pins. It is recommended to provide a 40 MHz crystal or CLKIN to support CAN FD data rates. When V_{IO} = 1.8 V an external clock should be used instead of a crystal.

8.3.10 nWKRQ Pin

This pin is a dedicated wake up request pin from a bus wake (WUP) request, local wake (LWU) request and power on (PWRON). The nWKRQ pin is defaulted to a wake enable based upon a wake event. In this configuration the output is pulled low and latched to serve as an enable for a regulator that does not use the INH pin to control voltage level. The nWKRQ pin can be configured by setting 16'h0800[8] = 1 as an interrupt pin that pulls the output low, but once the wake interrupt flag is cleared it releases the output back to a high. This pin defaults to an internal 3.6 V rail that is active during sleep mode. In this configuration, if a wake event takes place, the nWKRQ pin switches from high to low. This output can be configured to be powered from the V_{IO} rail through SPI programming, 16'h0800[19]. When powered off of the V_{IO} pin, the device does not insert an interrupt until the V_{IO} rail is stable. When configured for V_{IO}, this pin is an open drain output and requires an external pull up resistor to V_{IO} rail. This configuration bit is saved for all modes of operation and does not reset in sleep mode. As some external regulators or power management chips may need a digital logic pin for a wake up request, this pin can be used.

注

- This pin is active low and is logical OR of CANINT, LWU and WKERR register 16'h0820 that are not masked
- If a pull-up resistor is placed on this pin it must be configured for power from the V_{IO} rail

8.3.11 nINT Interrupt Pin

The nINT is a dedicated open drain global interrupt output pin. This pin needs an external pull-up resistor to V_{IO} to function properly. All interrupt requests are reflected by this pin when pulled low.

In test mode, this pin is used as an EN pin input for testing the CAN transceiver and is shown as EN_INT throughout the document. When this pin is high, the device is in normal mode and when low it is in standby mode. This is accomplished by writing 0 to register 16'h0800[0].

注

This pin is an active low and is the logical OR of all faults in registers 16'h0820 and 16'h0824 that are not masked.

8.3.12 GPO1 Pin

This pin defaults out as the M_CAN_INT 1 (active low) interrupt. The functionality of the pin can be changed to a configurable output function pin by setting register 16'h0800[15:14] = 00. The GPO function is further configured by using register 16'h0800[11:10].

When in test mode the GPO1 pin is used to provide the input signal for the transceiver (TXD_INT_PHY) or the input to the M_CAN core (RXD_INT_CAN). This is accomplished by first putting the device into test mode using register 16'h0800[21] = 1 and then selecting which part of the device is to be tested by setting register 16'h0800[0]

8.3.13 GPO2 Pin

The GPO2 pin is an open drain configurable output function pin that provides selected interrupts. This pin needs an external pull-up resistor to V_{IO} to function properly. The output function can be changed by using register 16'h0800[23:22].

Feature Description (continued)

In test mode, this pin becomes the RXD_INT_PHY transceiver output or TXD_INT_CAN CAN Controller output pin.

8.3.14 CANH and CANL Bus Pins

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low voltage WUP CAN receiver. The functionality of these is explained throughout the document. See section CAN Bus Biasing for can bus biasing.

8.4 Device Functional Modes

The TCAN4551-Q1 has several operating modes: normal, standby, and sleep modes and two protected modes. The first three mode selections are made by the SPI register. The two protected modes are modified standby modes used to protect the device or bus. The TCAN4551-Q1 automatically goes from sleep to standby mode when receiving a WUP or LWU event. See 表 1 for the various modes and what parts of the device are active during the each mode.

The TCAN4551-Q1 state diagram figure, see 図 22, shows the biasing of the CAN bus in each of the modes of operation.

表 1. Mode Overview

Mode	RST Pin	nINT	nWKRQ	INH	GPO2	Low Power CAN RX	WAKE Pin	SPI	GPO1	OSC	CAN TX/ RX	Memory & Configuration
Normal	L	On	On	On	On	Off	Off	On	On	On	On	Saved
Standby	L	On	On	On	On	On	On	On	On	On	Off	Saved
TSD Protected	L	On	On	On	On	On	On	On	On	On	Off	Saved
Sleep	L	Off	On	Off	Off	On	On	Off	Off	Off	Off	Partial Saved

注

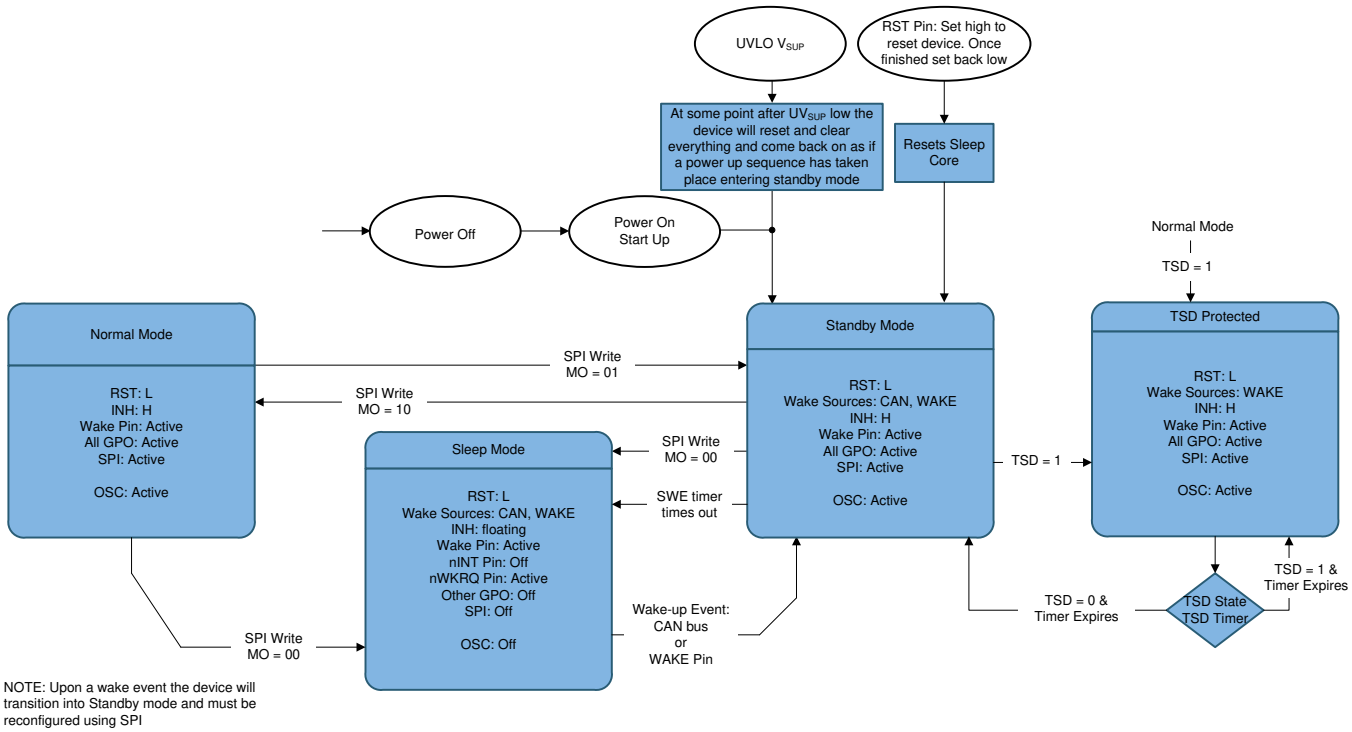


図 22. Device State Diagram

8.4.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translate a digital input on the internal TXD_INT signal from the CAN FD controller to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a digital output on the internal RXD_INT signal to the CAN FD controller. Normal mode is enabled or disabled via the SPI interface.

注

If an under voltage event has taken place and cleared, the interrupt flags have to be cleared before the device can enter normal mode.

8.4.2 Standby Mode

In standby mode, the bus transmitter does not send data nor will the normal mode receiver accept data. There are several blocks that are active in this mode. The low power CAN receiver is active, monitoring the bus for the wake up pattern (WUP). The wake pin monitor is active. The SPI interface is active so that the microprocessor can read and write registers in the memory for status and configuration. The INH pin is active in order to supply an enable to the V_{IO} controller if this function is used. The nWKRQ pin is low in this mode in the default configuration and can also be used as a digital enable pin to an external regulator or power management integrated circuit (PMIC). All other blocks are put into the lowest power state possible. This is the only mode that the TCAN4551-Q1 automatically switches to without a SPI transaction. The device goes from sleep mode to standby mode automatically upon a bus WUP event or a local wake up from the wake pin. Upon entry to Standby Mode, only one wake interrupt is given (either LWU, CANINT). New wake interrupts is not given in standby mode unless the device changes to normal or sleep mode and then back to standby. This prevents CAN traffic from spamming the processor with interrupts while in standby, and it gives the processor the first wake interrupt that was issued.

Upon power up, a power on reset or wake event from sleep mode the TCAN4551-Q1 enters standby mode. This starts a four minute timer, $t_{INACTIVE}$, that requires the processor to either reset the interrupt flags or configure the device to normal mode. This feature makes sure the node is in the lowest power mode if the processor does not come up properly. This automatic mode change also takes place when the device has been put into sleep mode and receives a wake event, WUP or LWU. To disable this feature for sleep events register 16'h0800[1] (SWE_DIS) must be set to one. This will not disable the feature when powering up or when a power on reset takes place.

8.4.3 Sleep Mode

Sleep mode is similar to the standby mode except the SPI interface and INH is disabled. As the low power CAN receiver is powered off of V_{SUP} the implementer can turn off V_{IO}. The nWKRQ pin is powered off the V_{SUP} supply internal logic level regulator. This allows the TCAN4551-Q1 to provide an interrupt to the MCU when a wake event takes place with out requiring V_{IO} to be up. When the device goes into sleep mode the power to the registers and memory is removed to conserve power. This requires the device to be re-configured prior to being put into normal mode. As the SPI interface is turned off the only ways to exit sleep mode is by a wake up event, RST pin toggle or power cycle. A sleep mode status flag is provided to determine if the device entered sleep mode through normal operation or if a fault caused the mode change. Register 16'h0820[23] provides the status. If a fault causes the device to enter sleep mode, this flag is set to a one.

注

Difference between sleep and standby mode

- Sleep mode reduces whole node power by shutting off INH/nWKRQ to MCU VREG and shuts off SPI.
- Standby mode reduces TCAN4551-Q1 power as INH and nWKRQ is enabled turning on node MCU VREG and SPI interface is active.

注

When entering sleep mode it is possible for the TCAN4551-Q1 to assert an interrupt due to UV_{CCFLTR} event as the LDO is powering down. This interrupt should be ignored or can be masked out by using 16'h830[22] before initiating the go to sleep command.

8.4.3.1 Bus Wake via RXD_INT Request (BWRR) in Sleep Mode

As the TCAN4551-Q1 supports low power sleep mode and uses a wake up from the CAN bus mechanism called bus wake via RXD_INT Request (BWRR). Once this pattern is received, the TCAN4551-Q1 automatically switches to standby mode and inserts an interrupt onto the nINT and nWKRQ pins to indicate to a host microprocessor that the bus is active, and it should wake up and service the TCAN4551-Q1. The low power receiver and bus monitor are enabled in sleep mode to allow for RXD_INT Wake Requests via the CAN bus. A wake up request is output to the internal RXD_INT (driven low) as shown in 図 24. The wake logic monitors RXD_INT for transitions (high to low) and reactivate the device to standby mode based on the RXD_INT Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, see 図 3.

These devices use the wake up pattern (WUP) from ISO 11898-2:2016 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the RXD_INT terminal (BWRR).

The wake up pattern (WUP) consists of

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the RXD_INT signal every time a filtered dominant time is received from the bus. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor recognizes the WUP and transition to BWRR output. Immediately upon verification receiving a WUP the device transitions the bus monitor into BWRR mode, and indicates all filtered dominant bus times on the RXD_INT internal signal by driving it low for the dominant bus time that is in excess of t_{WK_FILTER}, thus the RXD_INT output during BWRR matches the classical 8 pin CAN devices that used the single filtered dominant on the bus as the wake up request mechanism from ISO 11898-2:2016.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no BWRR is generated.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a BWRR may be generated.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP, and thus, a BWRR is always be generated.

See 図 23 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under voltage event occurs on V_{CCFLTR} the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time otherwise the device is in a state waiting for the next recessive and then a valid WUP pattern.

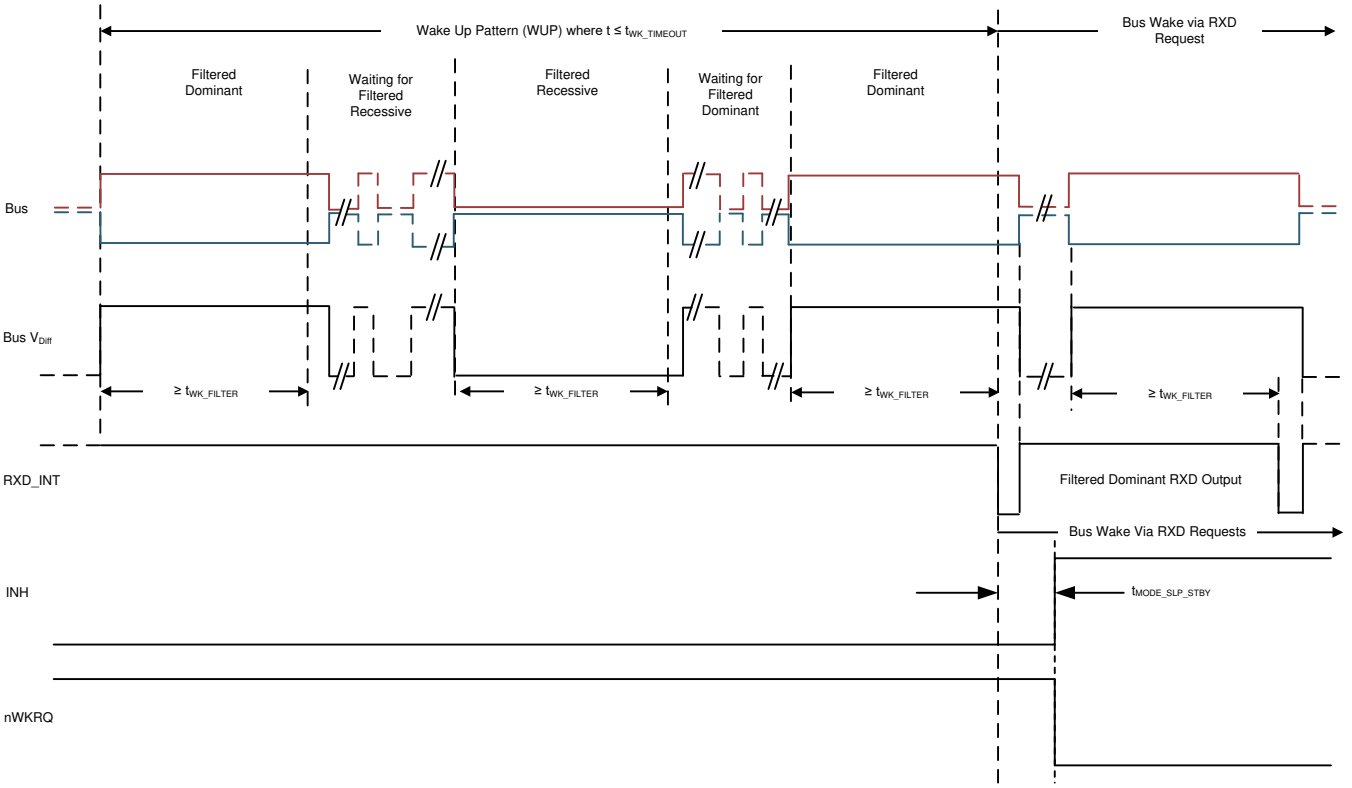


図 23. Wake Up Pattern (WUP) and Bus Wake via RXD_INT Request (BWRR)

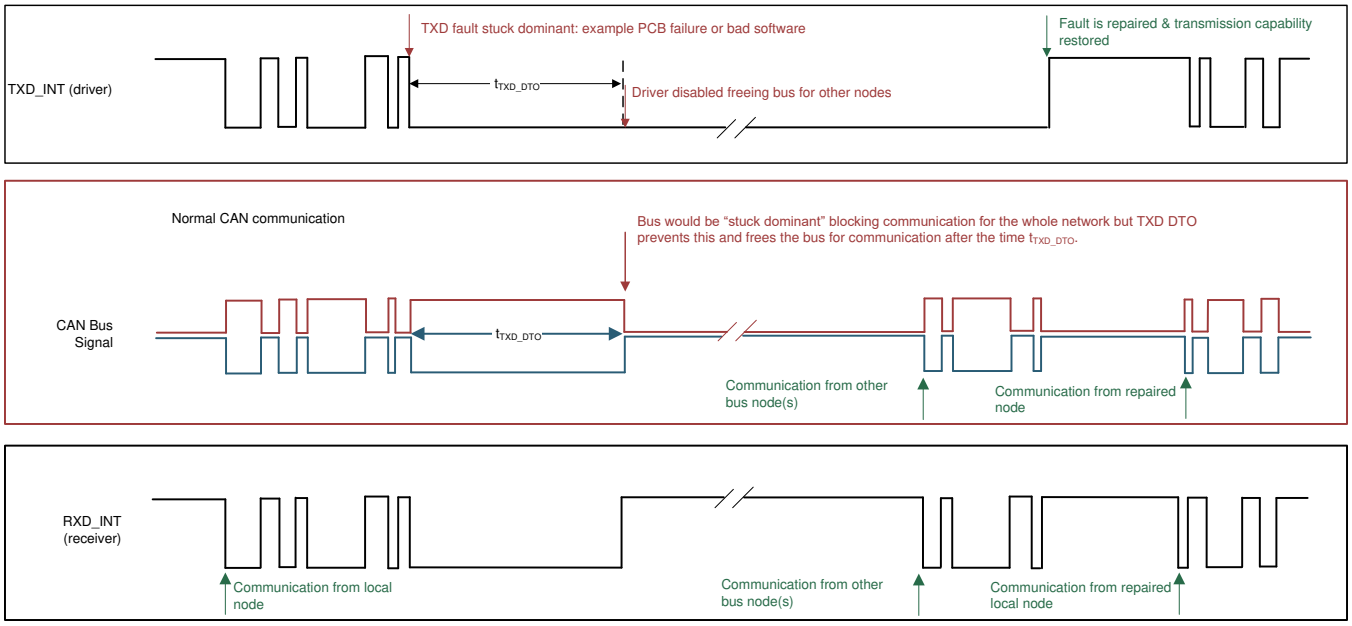


図 24. Example timing diagram with TXD_INT DTO

8.4.3.2 Local Wake Up (LWU) via WAKE Input Terminal

The WAKE terminal is a high voltage input terminal which can be used for local wake up (LWU) request via a voltage transition. The terminal triggers a LWU event on either a low to high or high to low transition as it has bi-directional input thresholds. This terminal may be used with a switch to V_{SUP} or ground. If the terminal is not used it should be pulled to ground or V_{SUP} to avoid unwanted wake up events.

The LWU circuitry is active in sleep mode and standby mode. If a valid LWU event occurs, the device transitions to standby mode. The LWU circuitry is not active in normal mode. To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal. The wake filter time for a valid wake to avoid glitches on wake pin is provided by filter value of $t_{WAKE(MIN)}$. A constant high level on WAKE has an internal pull up to V_{SUP} and a constant low level on WAKE has an internal pull down to GND. On power up, this may look like a LWU event and could be flagged as such.

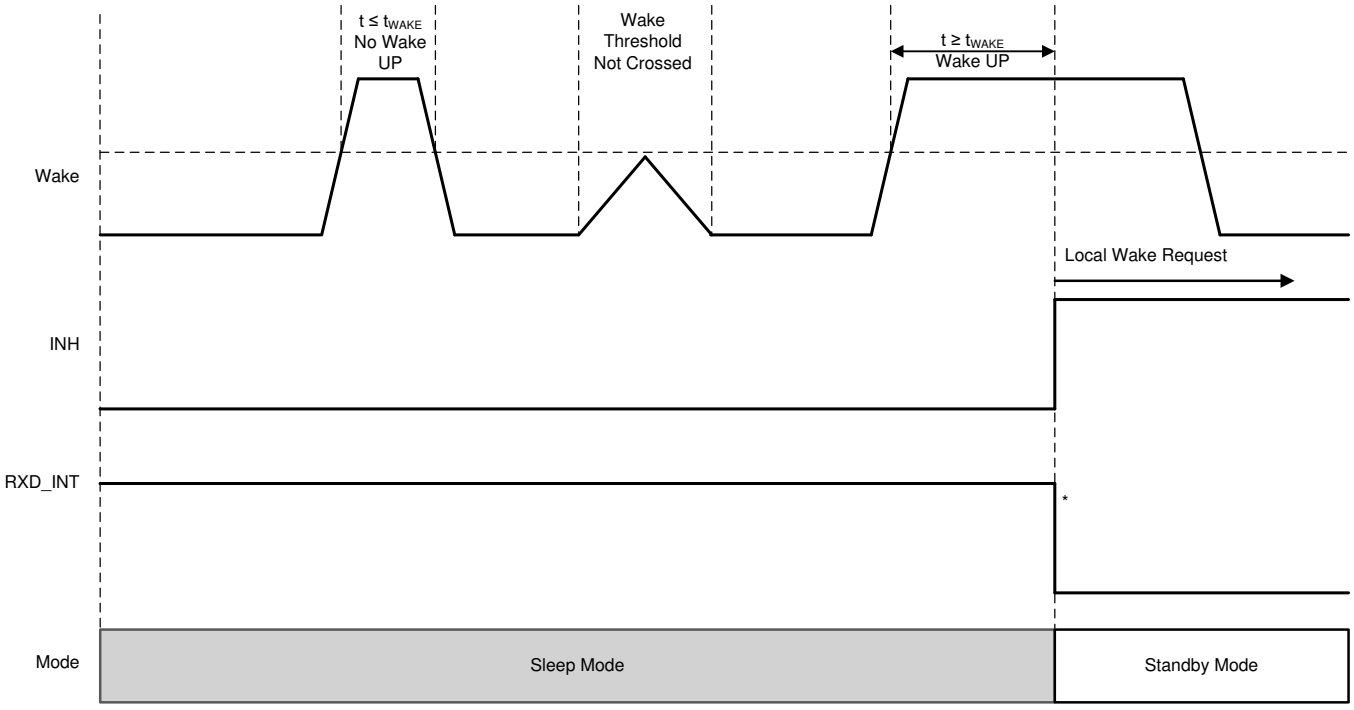


図 25. Local Wake Up – Rising Edge

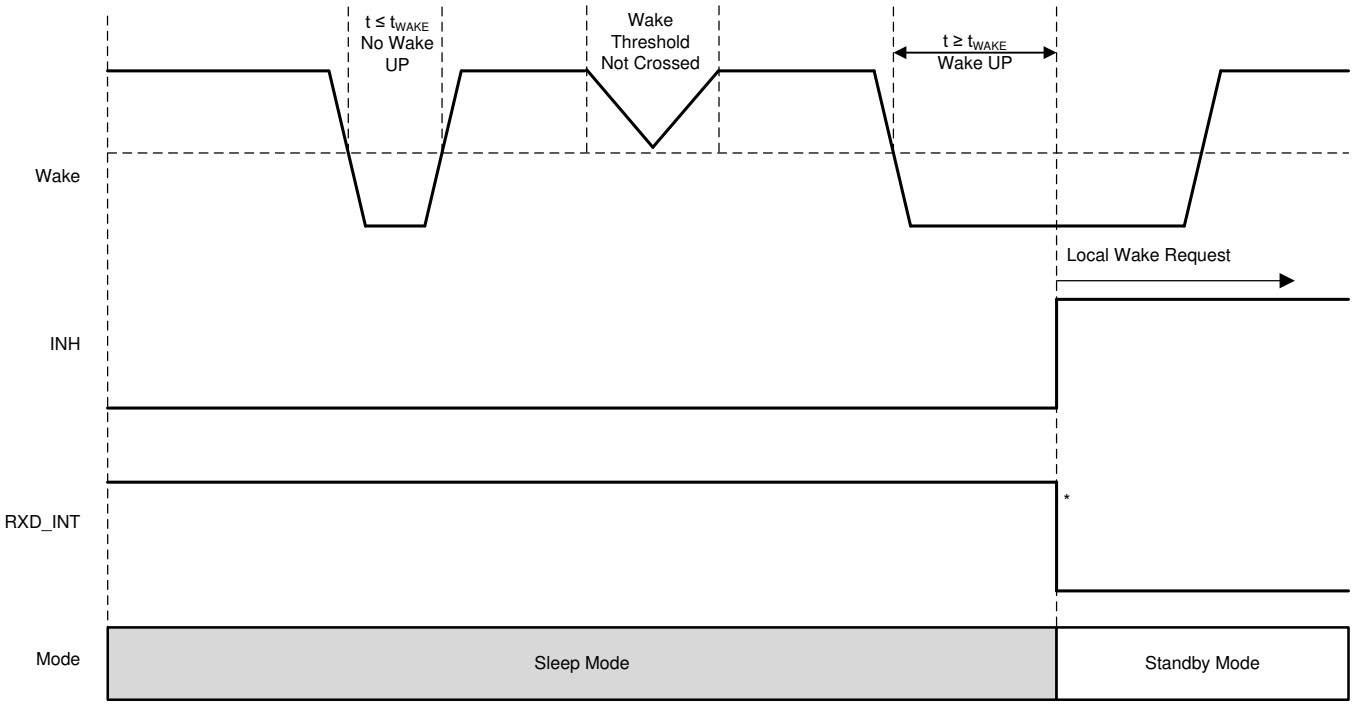


図 26. Local Wake Up – Falling Edge

注

RXD_INT is an internal signal and can be seen in Transceiver test mode when V_{IO} is present.

8.4.4 Test Mode

The TCAN4551-Q1 includes a test mode that has four configurations. Two are enabled by the SPI interface using the configuration register by setting register bit 16'h0800[21] = 1. In this mode the transceiver TXD_INT_PHY or CAN core RXD_INT_CAN can be mapped to the GPO1 pin and RXD_INT_PHY or TXD_INT_CAN can be mapped to the GPO2 pin. EN_INT pin is mapped to the nINT pin, see図 27 and 図 28. This is accomplished by setting register 16'h0800[0] to 0 for transceiver testing or 1 for M_CAN core testing. This mapping is only valid when in test mode. There are two M_CAN core specific test modes entered using SPI but written to the M_CAN core registers directly, see 図 29 and 図 30.

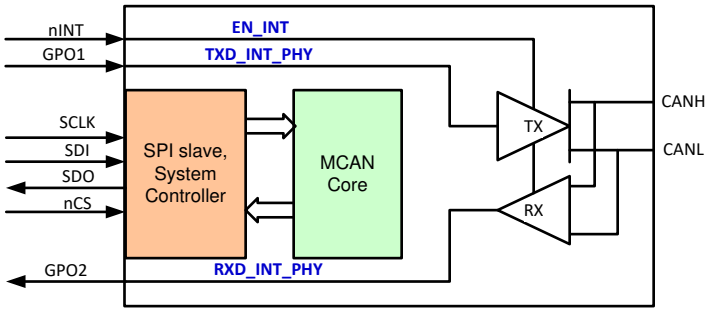


図 27. Transceiver Test Mode

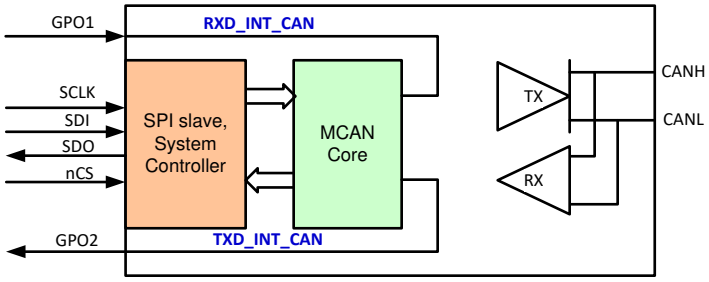


図 28. SPI and M_CAN Core Test Mode

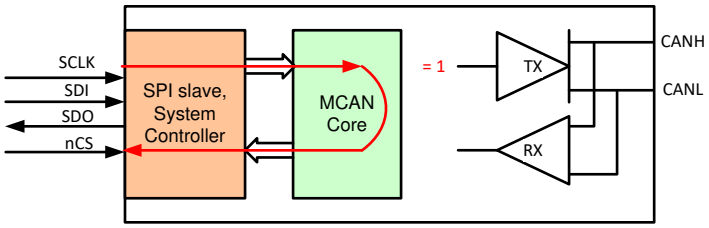


図 29. M_CAN Internal Loop Back Test Mode

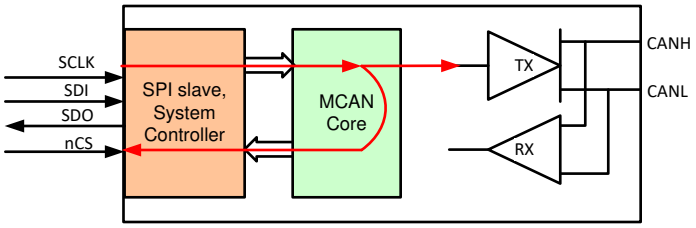


図 30. M_CAN External Loop Back Test Mode

8.4.5 Failsafe Feature

The TCAN4551-Q1 has three methods the failsafe feature is used in order to reduce node power consumption for a node system issue. Failsafe is the method the device uses to enter sleep mode from various other modes when specific issues arise. This feature uses the Sleep Wake Error (SWE) timer to determine if the node processor can communicate to the TCAN4551-Q1. The SWE timer is default enabled through the SWE_DIS; 16'h0800[1] = 0 but can be disabled by writing a one to this bit. Even when the timer is disabled, a power on reset re-enables the timer and thus be active. Failsafe Feature is default disabled but can be enabled by writing a one to 16'h0800[13], FAILSAFE_EN.

Upon power up the SWE timer starts, $t_{INACTIVE}$, the processor has typically four minutes to configure the TCAN4551-Q1, clear the PWRON flag or configure the device for normal mode; see 図 31. This feature cannot be disabled. If the device has not had the PWRON flag cleared or been placed into normal mode, it enters sleep mode. The device wakes up if the CAN bus provides a WUP or a local wake event takes place, thus entering standby mode. Once in standby mode $t_{SILENCE}$ and $t_{INACTIVE}$ timers starts. If $t_{INACTIVE}$ expires, the device re-enters sleep mode.

The second failure mechanism that causes the device to use the failsafe feature, if enabled, is when the device receives a CANINT, CAN bus wake (WUP) or WAKE pin (LWU), while in sleep mode such that the device leaves sleep mode and enters standby mode. The processor has four minutes to clear the flags and place the device into normal mode. If this does not happen the device enters sleep mode.

The third failure mechanism that causes the device to use the failsafe feature is when in standby or normal mode and the CANSLNT flag persists for $t_{INACTIVE}$, the device enters sleep mode. Examples of events that could create this are CLKIN or Crystal stops working, processor is no longer working and not able to exercise the SPI bus, a go-to-sleep command comes in and the processor is not able to receive it or is not able to respond. See state diagram 図 32.

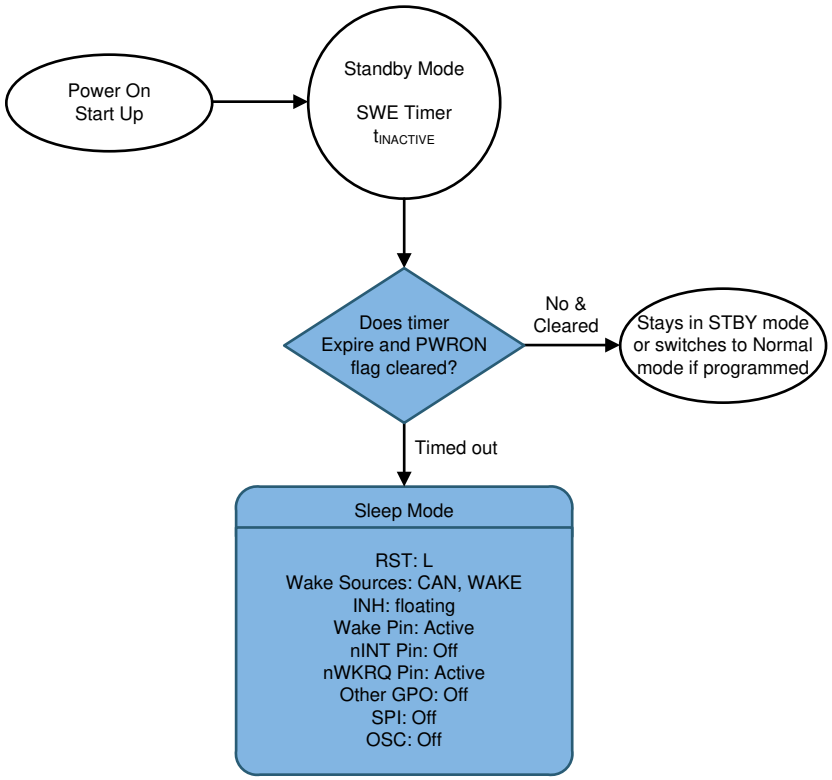


図 31. Power On Fail-safe Feature

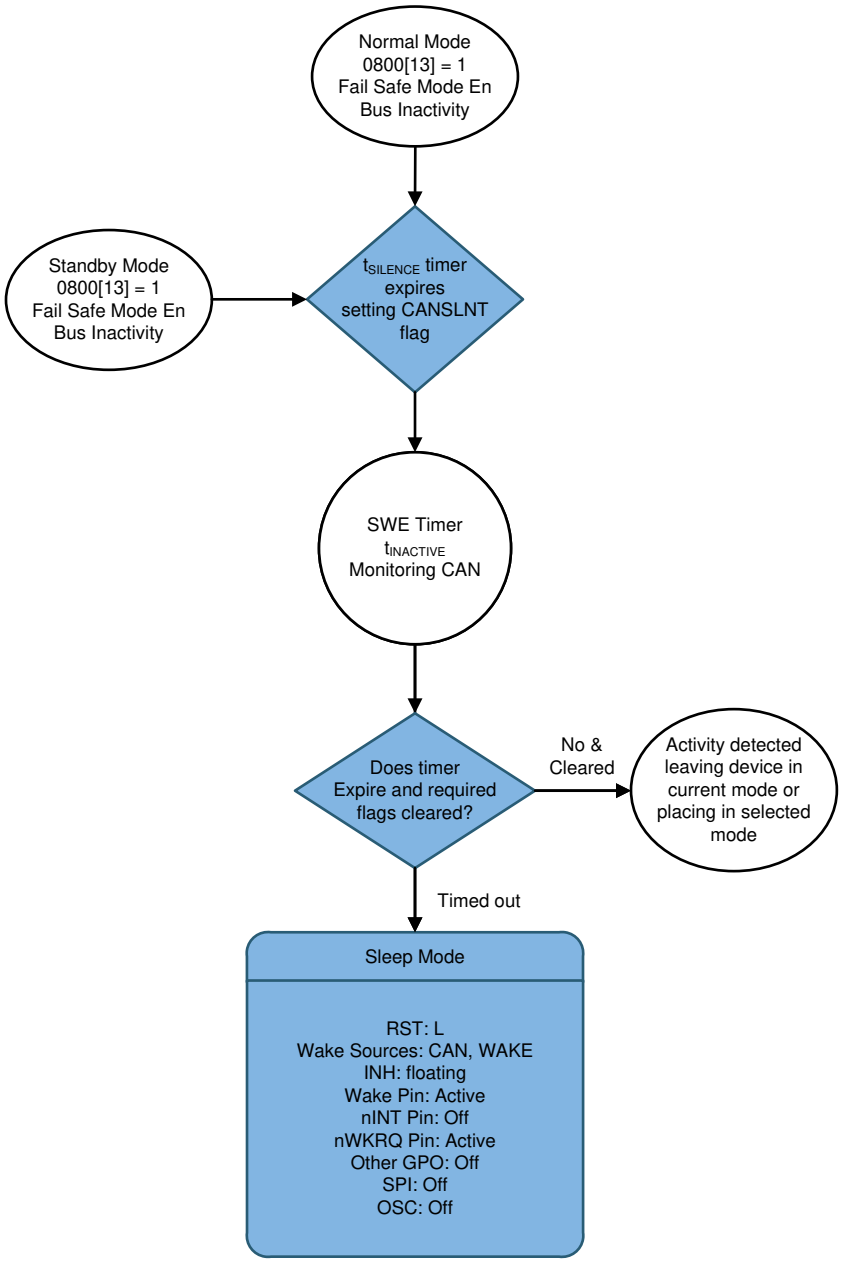


図 32. Normal and Standby Fail-safe Feature

8.4.6 Protection Features

The TCAN4551-Q1 has several protection features that are described as follows.

8.4.6.1 Driver and Receiver Function

The TXD_INT and RXD_INT are internal signal paths that behave like the TXD and RXD pins for a physical layer transceiver. During normal operation they are not accessible to external pins. The TCAN4551-Q1 provides a test mode that maps these signals to external pins see Test Mode. The digital logic input and output levels for these devices are CMOS levels with respect to V_{IO} for compatibility with protocol controllers having 3.3 V to 5 V logic or I/O. 表 2 and 表 1 provides the states of the CAN driver and CAN receiver in each mode.

表 2. Driver Function Table

DEVICE MODE	TXD_INT INPUT	BUS OUTPUTS		DRIVEN BUS STATE
		CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Standby	X	Z	Z	Weak Pull to GND
Sleep	X	Z	Z	Weak Pull to GND

表 3. Receiver Function Table Normal and Standby Modes

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD_INT TERMINAL
Normal	$V_{ID} \geq 0.9$ V	Dominant	L
	$0.5 \text{ V} < V_{ID} < 0.9$ V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	H
Standby/Sleep	$V_{ID} \geq 1.15$ V	Dominant	See 図 23
	$0.4 \text{ V} < V_{ID} < 1.15$ V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	H

8.4.6.2 Floating Terminals

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See 表 4 for details on terminal bias conditions.

表 4. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
SCLK	Pull up	Weakly biases input
SDI	Pull up	Weakly biases input
nCS	Pull up	Weakly biases input so the device is not selected
nWKRQ	Pull up	Weakly biases output when using internal voltage rail. When using open drain configuration an external pull up is be needed.
RST	Pull down	Weakly biases RST terminal towards normal operation mode

注

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a failsafe protection. Special care needs to be taken when the device is used with MCUs utilizing open drain outputs.

8.4.6.3 TXD_INT Dominant Timeout (DTO)

The TCAN4551-Q1 supports dominant state timeout. This is an internal function based upon the TXD_INT path. The transceiver can be tested for this by placing the device into test mode and putting a dominant on the GPO1 pin and monitor the GPO2 for RXD_INT_PHY. The TXD_INT DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD_INT is held dominant (low) longer than the timeout period $t_{TXD\_INT\_DTO}$. The TXD_INT DTO circuit is triggered by a falling edge on TXD_INT. If no rising edge is seen before the timeout constant of the circuit, $t_{TXD\_INT\_DTO}$, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal (high) is seen on TXD_INT terminal, thus clearing the dominant timeout. The receiver remains active and the RXD_INT terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD_INT DTO fault.

注

The minimum dominant TXD_INT time allowed by the TXD_INT DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD_INT) for the worst case, where five successive dominant bits are followed immediately by an error frame.

8.4.6.4 CAN Bus Short Circuit Current Limiting

This device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting. The device has TXD_INT dominant timeout which prevents permanently having the higher short circuit current of dominant state in case of a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD_INT dominant timeout and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

注

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using 式 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Receive \times IOS(SS)\_REC] \quad (1)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

注

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate V_{SUP}.

8.4.6.5 Thermal Shutdown

This is a device preservation event. If the junction temperature of the device exceeds the thermal shut down threshold, the device turns off the internal 5 V LDO for the CAN transceiver thus blocking the signal to bus transmission path. A thermal shut down interrupt flag is set and an interrupt is inserted so that the microprocessor is informed. If this event happens, other interrupt flags may be set as an example a bus fault where the CAN bus is shorted to V_{bat}. When this happens the digital core and SPI interface are still active. After a time of ≈ 300 ms the device checks the temperature of the junction. The thermal shutdown (TSD) timer starts when TSD fault event starts and exits to standby mode when a TSD fault is not present when the TSD timer is expired. While in thermal shut down protected mode a SPI write to change the device to either Normal or Standby mode is ignored while writes to change to sleep mode is accepted.

8.4.6.6 Under Voltage Lockout (UVLO) and Unpowered Device

The TCAN4551-Q1 monitors the V_{SUP} and V_{CCFLTR} pin for undervoltage events. These voltage rails have under voltage detection circuitry which places the device into a protected state if an under voltage fault occurs for UV_{SUP} . This protects the bus during an under voltage event on these terminals. If V_{SUP} is in under voltage, the device loses the source needed to keep the internal regulators active. This causes the device to go into a state where communication between the microprocessor and the TCAN4551-Q1 is disabled. The TCAN4551-Q1 is not able to receive information from the bus, and thus does not pass any signals from the bus, including any Bus Wake via BWRR signals to the microprocessor. See 表 5.

8.4.6.6.1 UV_{SUP} and UV_{CCFLTR}

When V_{SUP} drops to UV_{SUP} level, the V_{CC} CAN transceiver regulator loses the ability to maintain 5 V output. At this point, the UV_{CCFLTR} interrupt flag is set and the TCAN4551-Q1 turns off the regulator and place the CAN transceiver into a standby state. If V_{SUP} returns to minimum levels the device enters standby mode. If V_{SUP} continues to decrease to the power on reset level, the TCAN4551-Q1 shuts everything down. When V_{SUP} returns to acceptable levels the device will come up the same as initial power on. All registers are cleared and the device has to be reconfigured.

表 5. Under Voltage Lockout I and O Level Shifting Devices

V_{SUP}	Internal LDO	DEVICE STATE	BUS	RXD_INT
> UV_{SUP}	> UV_{CCFLTR}	Normal	Per TXD_INT	Mirrors Bus
< UV_{SUP}	NA	Protected	High Impedance	High (Recessive)
> UV_{SUP}	< UV_{CCFLTR}	Protected	High Impedance	High (Recessive)

注

Once an under voltage condition and interrupt flags are cleared and the V_{SUP} supply has returned to valid level, the device typicallys need t_{MODE_CHANGE} to transition to normal operation. The host processor should not attempt to send or receive messages until this transition time has expired. If EN is low and V_{SUP} has an under voltage event, the device goes into a protected mode which disables the wake up receiver and places the RXD_INT output into a high impedance state.

8.4.6.6.2 Fault and M_CAN Core Behavior:

During a UV_{CCFLTR} or TSD fault the TCAN4551-Q1 automatically does the following to keep the M_CAN core in a known state. A write of 1 to CCCR.INIT will be issued anytime there is a transition from Normal → Standby. Any currently pending TX or RX processing is halted. Once the device re-enters Normal mode, a write of 0 to CCCR.INIT is issued, and any pending messages (TXBRP active bits) is automatically transmitted.

8.4.7 CAN FD

The TCAN4551-Q1 performs CAN communication according to ISO 11898-1:2015 and Bosch CAN protocol specification 3.2.1.1.

8.5 Programming

The TCAN4551-Q1 uses 32 bit accesses. The TCAN4551-Q1 provides 2K bytes of MRAM that is fully configurable for TX/RX buffer/FIFO as needed based upon the system needs. To avoid ECC errors right after initialization, the MRAM should be zeroed out during the initialization, power up, power on reset and wake events, a process thus ensuring ECC is properly calculated.

Programming (continued)

注

At power up, MRAM values are unknown and thus ECC values is not valid. It is important that at least 2 words (8 bytes) of payload data be written into any TX buffer element, even if the DLC is less than 8. Failure to do this results in a M_CAN BEU error, which puts the TCAN4551-Q1 device into initialization mode, and require user intervention before CAN communication can continue. One way to avoid this, the MRAM should be zeroed out after power up, a power on reset or coming out of sleep mode.

8.5.1 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (Slave Data In), SDO (Slave Data Out) and SCLK (SPI Clock). Each SPI transaction is a 32 bit word containing a command byte followed by two address bytes and length bytes. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (byte). This register provides the high level status information about the device status. The two data bytes which are the 'response' to the command byte are shifted out next. Data bytes shifted out during a write command is content of the registers prior to the new data being written and updating the registers. Data bytes shifted out during a read command are the current content of the registers and the registers will not be updated.

The SPI input data on SDI is sampled on the low to high edge of the SCLK. The SPI output data on SDO is changed on the high to low edge of the SCLK.

8.5.1.1 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SDO pin of the device is high impedance allowing a SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

8.5.1.2 SPI Clock Input (SCLK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of SCLK and the SPI Data Output is changed on the falling edge of the SCLK.

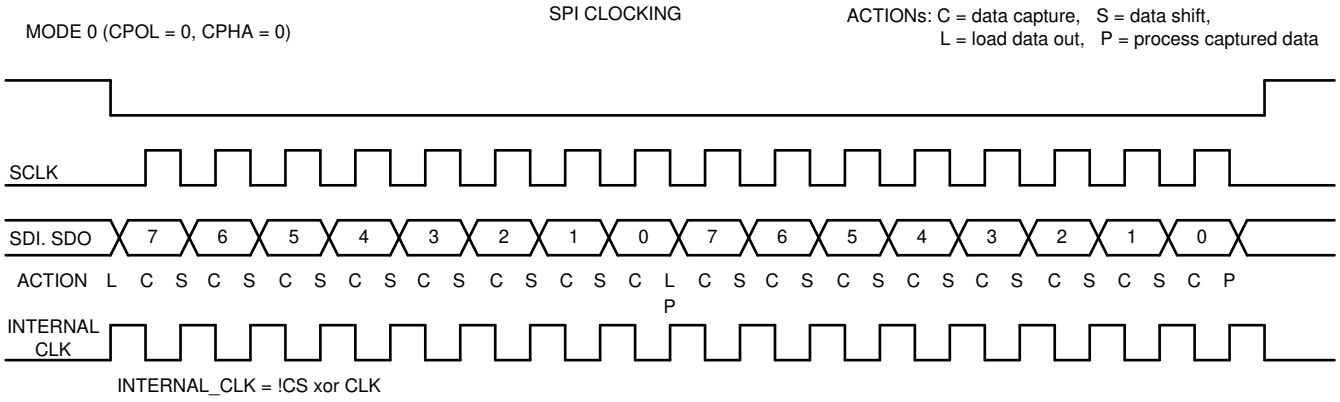


図 33. SPI Clocking

8.5.1.3 SPI Data Input (SDI):

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS the SDI samples the input shifted data on each rising edge of the SCLK. The data is shifted into a 32 bit shift register. If the command code was a write, the new data is written into the addressed register only after exactly 32 bits have been shifted in by SCLK and the nCS has a rising edge to deselect the device. If there are not exactly a multiple of 32 bits shifted in to the device, the during one SPI transaction (nCS low) the last word of the transfer is ignored, the SPIERR flag is set.

Programming (continued)

注

Due to needing multiples of 32 bits on each SPI transaction, the device should be wired for parallel operation of the SPI as a bus with control to the device via nCS and not as a daisy chain of shift registers.

8.5.1.4 SPI Data Output (SDO):

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 32) to be shifted out if the SPI is clocked. Once SCLK begins, on the first low to high edge of the clock the SDO retains the Global Fault Flag which is bit 31 of the shift. On the first falling edge of SCLK, the shifting out of the data continues with each falling edge on SCLK until all 32 bits have been shifted out the shift register.

8.5.2 Register Descriptions

The Addresses for each area of the device are as follows:

- Register 16'h0000 through 16'h000C are Device ID and SPI Registers
- Register 16'h0800 through 16'h083C are device configuration registers and Interrupt Flags
- Register 16'h1000 through 16'h10FC are for M_CAN
- Register 16'h8000 through 16'h87FF is for MRAM.

The start address must be word aligned (32-bit). Any time the registers are accessed, bits [1:0] of the address are ignored as the addresses are always word (32-bit/4-byte) aligned. As an example for accessing the M_CAN registers, for the register 0x1004, give the SPI address 1004, 1005, 1006 or 1007, and access register 1004. The registers are 32 bit and only 1004 is valid in this example.

When entering the MRAM start address, the 0x8000 prefix is not necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] is 0x0634.

表 6 provides programming op Codes.

表 6. Access Commands

NAME	OP CODE	DESCRIPTION	USAGE
WRITE_B_FL (burst: one SPI transfer Length: fixed)	8'h61	Write one or more addresses	< WRITE_B_FL > <2 address bytes> <1 length bytes> <length words of write data>
READ_B_FL (burst: one SPI transfer Length: fixed)	8'h41	Read one or more internal SPI addresses	< READ_B_FL > <2 address bytes> <1 length bytes> <length words of read data>

Notes:

- The two low order address bits is ignored
- A length of 8’h00 indicates 256 words to be transferred

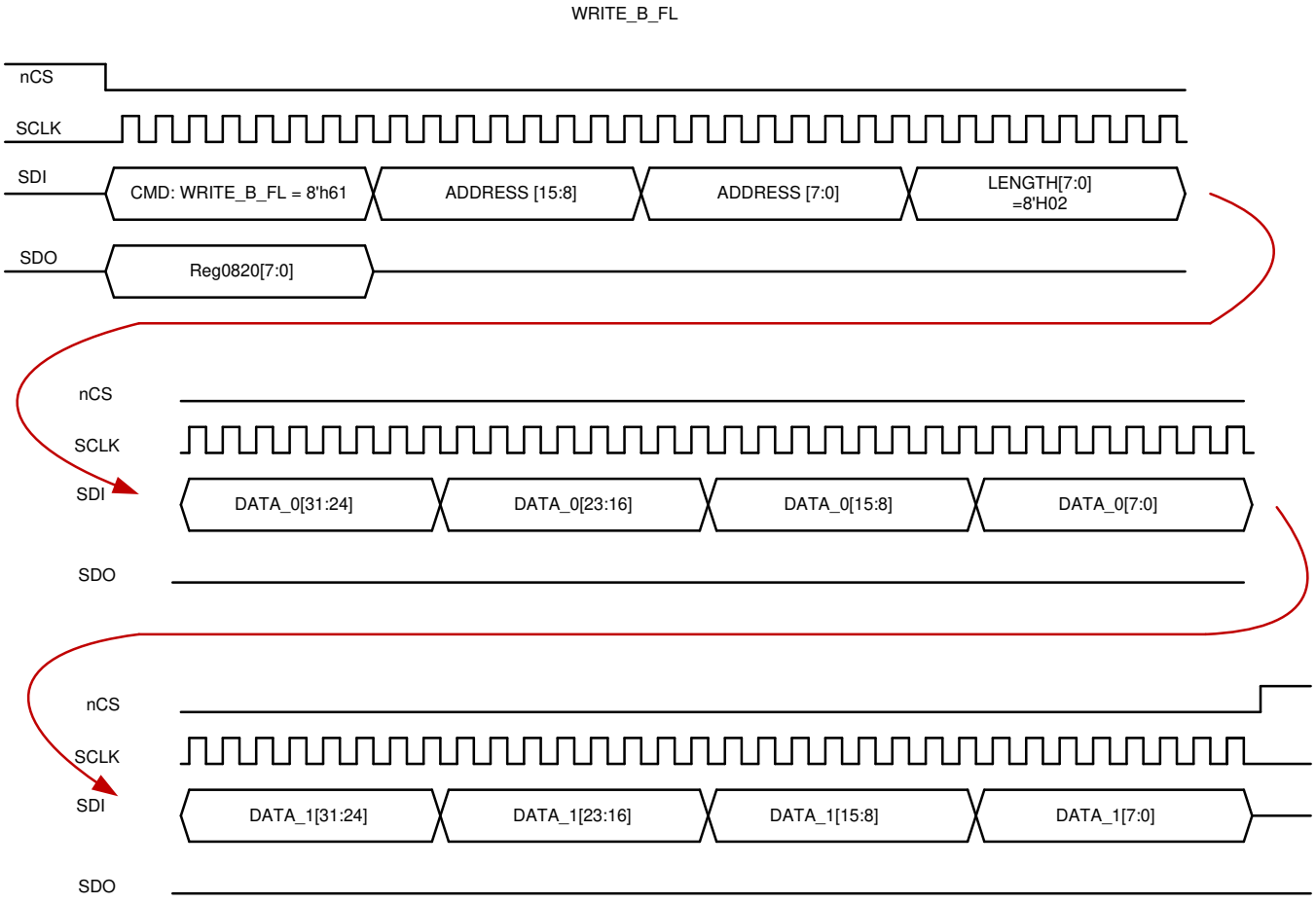


図 34. Write

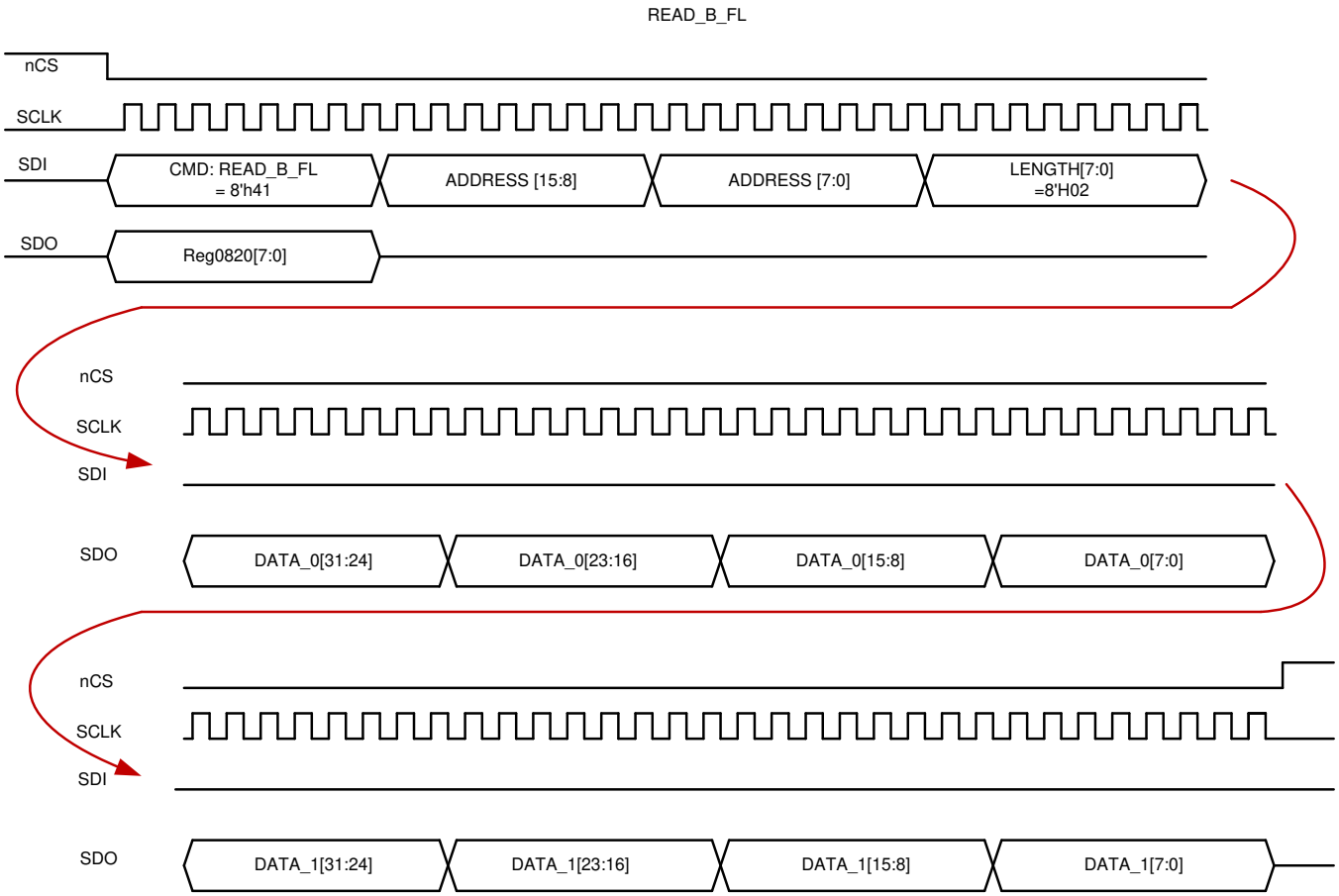


図 35. Read (Command OpCode 8h41)

8.6 Register Maps

The TCAN4551-Q1 has a comprehensive register set with 32 bit addressing. The register is broken down into several sections:

- Device ID and Interrupt/Diagnostic Flag Registers: 16'h0000 to 16'h002F.
- Device Configuration Registers: 16'h0800 to 16'h08FF .
- Interrupt/Diagnostic Flag and Enable Flag Registers: 16'h0820/0824 and 16'h0830.
- CAN FD Register Set: 16'h1000 to 16'h10FF.

注

All addresses are the lower order 16 address bit within the defined 32 bit address space.

Upper 16 address bits are ignored.

Register Maps (continued)

8.6.1 Device ID and Interrupt/Diagnostic Flag Registers: 16'h0000 to 16'h002F

This register block provided the device name and revision level. It provides all the interrupt flags as well.

Table 7. Device ID and Interrupt/Diagnostic Flag Registers

ADDRESS	REGISTER	TCAN4551 VALUE	ACCESS
‘h0000	DEVICE_ID[7:0] "T"	54	R
	DEVICE_ID[15:8] "C"	43	R
	DEVICE_ID[23:16] "A"	41	R
	DEVICE_ID[31:24] "N"	4E	R
‘h0004	DEVICE_ID[39:32] "4"	34	R
	DEVICE_ID[47:40] "5"	35	R
	DEVICE_ID[55:48] "5"	35	R
	DEVICE_ID[63:56] “1”	31	R
‘h0008	SPI_2_revision, 8’h00 (Reserved), REV_ID Major, REV_ID Minor REV_ID Major	00	R
‘h000C	Status	00	R

Table 8. Device Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WC	W	Write
Reset or Default Value		
-n		Value after reset or the default value
U	U	Undefined

8.6.1.1 DEVICE_ID1[31:0] (address = h0000) [reset = h4E414354]

Figure 36. Device ID1

31	30	29	28	27	26	25	24
DEVICE_ID1[31:24]							
RO							
23	22	21	20	19	18	17	16
DEVICE_ID1[23:16]							
RO							
15	14	13	12	11	10	9	8
DEVICE_ID1[15:8]							
RO							
7	6	5	4	3	2	1	0
DEVICE_ID1[7:0]							
RO							

Table 9. Device ID Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVICE_ID1[31:0]	RO	h4E414354	DEVICE_ID1[31:0]

8.6.1.2 DEVICE_ID2[31:0] (address = h0004) [reset = h31353534]

Figure 37. Device ID2

31	30	29	28	27	26	25	24
DEVICE_ID2[31:24]							
RO							
23	22	21	20	19	18	17	16
DEVICE_ID2[23:16]							
RO							
15	14	13	12	11	10	9	8
DEVICE_ID2[15:8]							
RO							
7	6	5	4	3	2	1	0
DEVICE_ID2[7:0]							
RO							

Table 10. Device ID Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DEVICE_ID2[31:0]	RO	h31353534	DEVICE_ID2[63:32]

8.6.1.3 Revision (address = h0008) [reset = h00110201]

Figure 38. Revision

31	30	29	28	27	26	25	24
SPI_2_REVISION							
RO							
23	22	21	20	19	18	17	16
RSVD							
RO							
15	14	13	12	11	10	9	8
REV_ID MAJOR							
RO							
7	6	5	4	3	2	1	0
REV_ID MINOR							
RO							

Table 11. Revision Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SPI_2_REVISION	RO	h00	Revision version of the SPI module
23:16	RSVD	RO	h11	Reserved
15:8	REV_ID MAJOR	RO	h02	Device REV_ID Major
7:0	REV_ID MINOR	RO	h01	Device REV_ID Minor

8.6.1.4 Status (address = h000C) [reset = h0000000U]

Figure 39. Status

31	30	29	28	27	26	25	24
RSVD		Internal_read_error	Internal_write_error	Internal_error_log_write	Read_fifo_underflow	Read_fifo_empty	Write_fifo_overflow
RO		W1C	W1C	W1C	W1C	W1C	W1C
23	22	21	20	19	18	17	16
RSVD		SPI_end_error	Invalid_command	Write_overflow	write_underflow	Read_overflow	read_underflow
RO		W1C	W1C	W1C	W1C	W1C	W1C
15	14	13	12	11	10	9	8
RSVD							
RO							
7	6	5	4	3	2	1	0
RSVD		Write_fifo_available	Read_fifo_available	Internal_access_active	Internal_error_interrupt	SPI_error_interrupt	Interrupt
RO		RO	RO	RO	RO	RO	RO

Table 12. Status Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	RO	1'b0	Reserved
29	Internal_read_error	W1C	1'b0	Internal read received an error response
28	Internal_write_error	W1C	1'b0	Internal write received an error response
27	Internal_error_log_write	W1C	1'b0	Entry written to the Internal error log
26	Read_fifo_underflow	W1C	1'b0	Read FIFO underflow after 1 or more read data words returned
25	Read_fifo_empty	W1C	1'b0	Read FIFO empty for first read data word to return
24	Write_fifo_overflow	W1C	1'b0	Write/command FIFO overflow
23:22	RSVD	RO	1'b0	Reserved
21	SPI_end_error	W1C	1'b0	SPI transfer did not end on a byte boundary
20	Invalid_command	W1C	1'b0	Invalid SPI command received
19	Write_overflow	W1C	1'b0	SPI write sequence had continue requests after the data transfer was completed
18	write_underflow	W1C	1'b0	SPI write sequence ended with less data transferred then requested
17	Read_overflow	W1C	1'b0	SPI read sequence had continue requests after the data transfer was completed
16	read_underflow	W1C	1'b0	SPI read sequence ended with less data transferred then requested
15:8	RSVD	RO	8'h00	Reserved
7:6	RSVD	RO	1'b0	Reserved
5	Write_fifo_available	RO	1'b0	write fifo empty entries is greater than or equal to the write_fifo_threshold
4	Read_fifo_available	RO	1'b0	Read fifo entries is greater than or equal to the read_fifo_threshold
3	Internal_access_active	RO	U	Internal Multiple transfer mode access in progress
2	Internal_error_interrupt	RO	1'b0	Unmasked Internal error set
1	SPI_error_interrupt	RO	1'b0	Unmasked SPI error set
0	Interrupt	RO	U	Value of interrupt input level (active high)

8.6.2 Device Configuration Registers: 16'h0800 to 16'h08FF

Registers not listed are reserved and return h'00.

Table 13. Device Configuration Registers

ADDRESS	REGISTER	VALUE	ACCESS
0800	Modes of Operation and Pin Configurations	h'C8000468	R/W/U
0804	Timestamp Prescalar	h'00000002	R/W
0808	Read and Write Test Registers	h'00000000	R/W
080C – 0810	ECC and TDR Registers	h'00000000	R/W/U
0814 -081C	Reserved	h'00000000	R
0820	Interrupt Flags	h'00000000	R
0824	MCAN Interrupt Flags	h'00000000	R
0829 – 082F	Reserved	h'00000000	R
0830	Interrupt Enable	h'FFFFFFFF	R/W
0834 – 083F	Reserved	h'00000000	R

NOTE

The following bits are being saved when entering sleep mode and will show up **bold** in register maps.

- 16'h0800 bits 0, 1, 8, 9, 10, 11, 13, 19, 21, 22, 23, 30 and 31.
- 16'h0820 bits 19 and 21
- 16'h0830 bits 14 and 15

8.6.2.1 Modes of Operation and Pin Configuration Registers (address = h0800) [reset = hC8000460]

Figure 40. Modes of Operation and Pin Configuration Registers

31	**30**	29	28	27	26	25	24
WAKE_CONFIG		RSVD		CLK_REF	RSVD	RSVD	RSVD
R/W		R		R/W	R	R	R
23	**22**	**21**	20	**19**	18	17	16
GPO2_CONFIG		**TEST_MODE_EN**	RSVD	**nWKRQ_VOLTAGE**	RSVD	RSVD	
R/W		R/W	R	R/W	R	R	
15	14	**13**	12	**11**	**10**	**9**	**8**
RSVD		**FAIL_SAFE_EN**	RSVD	**GPO1_GPO_CONFIG**		**INH_DIS**	**nWKRQ_CONFIG**
R		R/W	R	R/W		R/W	R/W
7	6	5	4	3	2	**1**	**0**
MODE_SEL		RSVD	RSVD	RSVD	DEVICE_RESET	**SWE_DIS**	**TEST_MODE_CONFIG**
R/W/U		R	R	R	R/W/U	R/W	R/W

Table 14. Modes of Operation and Pin Configuration Registers Field Descriptions

Bit	Field	Type	Reset	Description
31:30	**WAKE_CONFIG**	R/W	2'b11	WAKE_CONFIG: Wake pin configuration 00 = Disabled 01 = Rising edge 10 = Falling edge 11 = Bi-Directional – either edge
29:28	RSVD	R	2'b00	Reserved

Table 14. Modes of Operation and Pin Configuration Registers Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CLK_REF	R/W	1'b1	CLK_REF: CLKIN/Crystal Frequency Reference 0 = 20 MHz 1 = 40 MHz
26:24	RSVD	R	3'b000	Reserved
23:22	**GPO2_CONFIG**	R/W	2'b00	GPO2_CONFIG: GPO2 Pin GPO Configuration 00 = No Action 01 = MCAN_INT 0 interrupt (Active low) 10 = Reserved 11 = Mirrors nINT pin (Active low) See NOTE section
21	**TEST_MODE_EN**	R/W	1'b0	TEST_MODE_EN: Test mode enable. When set device is in test mode 0 = Disabled 1 = Enabled
20	RSVD	R	1'b0	Reserved
19	**nWKRQ_VOLTAGE**	R/W	1'b0	nWKRQ_VOLTAGE: nWKRQ Pin GPO buffer voltage rail configuration: See 0 = Internal voltage rail 1 = VIO voltage rail
18:16	RSVD	R	3'b000	Reserved
15:14	RSVD	R	2'b00	Reserved
13	**FAIL_SAFE_EN**	R/W	1'b0	FAIL_SAFE_EN: Fail safe mode enable: 0 = Disabled 1 = Enabled NOTE: Excludes power up fail safe.
12	RSVD	R	1'b0	Reserved
11:10	**GPO1_GPO_CONFIG**	R/W	2'b01	GPO1_GPO_CONFIG: GPO1 pin GPO1 function select 00 = SPI fault Interrupt (Active low) 01 = MCAN_INT 1 (Active low) 10 = Under voltage or thermal event interrupt (Active low) 11 = Reserved
9	**INH_DIS**	R/W	1'b0	INH_DIS: INH Pin Disable 0 = Pin enabled 1 = Pin disabled
8	**nWKRQ_CONFIG**	R/W	1'b0	nWKRQ_CONFIG: nWKRQ Pin Function 0 = Mirrors INH function 1 = Wake request interrupt
7:6	MODE_SEL	R/W	2'b01	MODE_SEL: Mode of operation select 00 = Sleep 01 = Standby 10 = Normal 11 = Reserved See NOTE section
5	RSVD	R	1'b1	When writing to this register, this bit must always be a 1
4	RSVD	R	1'b0	Reserved
3	RSVD	R	1'b0	Reserved
2	DEVICE_RESET	R/WC	1'b0	DEVICE_RESET: Device Reset 0 = Current configuration 1 = Device resets to default NOTE: Same function as RST pin
1	**SWE_DIS**	R/W	1'b0	SWE_DIS: Sleep Wake Error Disable: 0 = Enabled 1 = Disabled NOTE: This disables the device from starting the four minute timer when coming out of sleep mode on a wake event. If this is enabled a SPI read or write must take place within this four minute window or the device will go back to sleep. This does not disable the function for initial power on or in case of a power on reset.

Table 14. Modes of Operation and Pin Configuration Registers Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TEST_MODE_CONFIG	R/W	1'b0	Test Mode Configuration 0 = Phy Test with TXD/RXD_INT_PHY and EN_INT are mapped to external pins 1 = CAN Controller test with TXD/RXD_INT_CAN mapped to external pins

NOTE

- The Mode of Operation changes the mode but will read back the mode the device is currently in.
- When the device is changing the device to normal mode a write of 0 to CCCR.INIT is automatically issued and when changing from normal mode to standby or sleep modes a write of 1 to CCCR.INIT is automatically issued.
- When GPO1 is configured as a GPO for interrupts the interrupts list represent the following and are active low:
  - 00: SPI Fault Interrupt. Matches SPIERR if not masked
  - 01: MCAN_INT:1 m_can_int1.
  - 10: Under Voltage or Thermal Event Interrupt: Logical OR of $UV_{CCFLTR,}$ UV_{SUP}, TSD faults that are not masked.
- When GPO1 is configured as a GPO for interrupts the interrupts list represent the following and are active low:
  - 00: SPI Fault Interrupt. Matches SPIERR if not masked
  - 01: MCAN_INT:1 m_can_int1.
  - 10: Under Voltage or Thermal Event Interrupt: Logical OR of $UV_{CCFLTR,}$ UV_{SUP}, TSD faults that are not masked.
- nWKRQ pin defaults to a push-pull active low configuration based off an internal voltage rail. When configuring this to work off of V_{IO} the pin becomes and open drain output and a external pull up resistor to the V_{IO} rail is required.

8.6.2.2 Timestamp Prescalar (address = h0804) [reset = h00000002]

Figure 41. Timestamp Prescalar

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
Timestamp Prescalar							
R/W							

Table 15. EMC Enhancement and Timestamp Prescalar Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	8'h00	Reserved
23:16	RSVD	R	8'h00	Reserved
15:8	RSVD	R	8'h00	Reserved
7:0	Timestamp Prescalar	R/W	8'h02	Writing to this register resets the internal timestamp counter to 0 and will set the internal CAN clock divider used for MCAN Timestamp generation to (Timestamp Prescalar x 8)

8.6.2.3 Test Register and Scratch Pad (address = h0808) [reset = h00000000]

Saved in sleep mode

Figure 42. Test and Scratch Pad Register

31	30	29	28	27	26	25	24
Test Read and Write							
R/W							
23	22	21	20	19	18	17	16
Test Read and Write							
R/W							
15	14	13	12	11	10	9	8
Scratch Pad 1							
R/W							
7	6	5	4	3	2	1	0
Scratch Pad 2							
R/W							

Table 16. Test and Scratch Pad Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	Test Read and Write	RW	8'h00	Test Read and Write Register
23:16	Test Read and Write	R/W	8'h00	Test Read and Write Register
15:8	Scratch Pad 1	R/W	8'h00	Bits 15:8 are saved when device is configured for sleep mode
7:0	Scratch Pad 2	R/W	8'h00	Bits 7:0 are saved when device is configured for sleep mode

8.6.2.4 Test Register (address = h080C) [reset = h00000000]

Figure 43. Test Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD	RSVD	ECC_ERR_FORCE_BIT_SEL					
R	R	R/W					
15	14	13	12	11	10	9	8
RSVD		RSVD	ECC_ERR_FORCE	ECC_ERR_CHECK	RSVD	RSVD	RSVD
R		R	R/W	R/W	R	R	R
7	6	5	4	3	2	1	0
RSVD							
R							

Table 17. Test Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	8'h00	Reserved
23:22	RSVD	R	2'b00	Reserved
21:16	ECC_ERR_FORCE_BIT_SEL	R/W	6'b000000	ECC_ERR_FORCE_BIT_SEL 000000 = Bit 0 000001 = Bit 1 .... 100110 = Bit 38 All other bit combinations are Reserved
15:13	RSVD	R	3'b000	Reserved
12	ECC_ERR_FORCE	R/W	1'b0	ECC_ERR_FORCE 0 = No Force 1 = Force a single bit ECC error
11	ECC_ERR_CHECK	R/W	1'b0	ECC_ERR_CHECK 0 = No Single Bit ECC error detected 1 = Single Bit ECC error detected
10	RSVD	R	1b'0	Reserved
9:0	RSVD	R	10'b0000000000	Reserved

8.6.3 Interrupt/Diagnostic Flag and Enable Flag Registers: 16'h0820/0824 and 16'h0830

This register block provides all the interrupt flags for the device. As the M-CAN interrupt flags 16'h0824 are described in 16'h1050 MCAN register description section and will be shown here but need to go to 16'h1050 for description. 16h'0830 is Interrupt enable to trigger an interrupt for 16'h0820.

8.6.3.1 Interrupts (address = h0820) [reset = h00100000]

Figure 44. Interrupts

31	30	29	28	27	26	25	24
CANBUSNOM	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
RU	R	R	R	R	R	R	R
23	22	21	20	**19**	18	17	16
RSVD	UVSUP	RSVD	PWRON	**TSD**	RSVD	RSVD	ECCERR
R	R/WC	R	R/WC/U	R/WC	R	R	R/WC
15	14	13	12	11	10	9	8
CANINT	LWU	WKERR	RSVD	RSVD	CANSLNT	RSVD	CANDOM
R/WC	R/WC	R/WC	R	R	R/WC	R	R/WC
7	6	5	4	3	2	1	0
GLOBALERR	nWKRQ	CANERR	RSVD	SPIERR	RSVD	M_CAN_INT	VTWD
R	R	R	R	R	R	R	R

Table 18. Interrupts Field Descriptions

Bit	Field	Type	Reset	Description
31	CANBUSNOM	RU	1'b0	CAN Bus normal (Flag and Not Interrupt) Will change to 1 when in normal mode after first Dom to Rec transition
30:24	RSVD	R	7b'0000000	Reserved
23	SMS	R/WC	1'b0	Sleep Mode Status (Flag & Not an interrupt) Only sets when sleep mode is entered by a WKERR or TSD fault
22	UVSUP	R/WC	1'b0	Under Voltage V_{SUP} and UV_{CCFLTR}
21	RSVD	R	1'b0	Reserved
20	PWRON	R/WC/U	1'b1	Power ON
19	**TSD**	R/WC	1'b0	Thermal Shutdown
18	RSVD	R	1'b0	Reserved
17	RSVD	R	1'b0	Reserved
16	ECCERR	R/WC	1'b0	Uncorrectable ECC error detected
15	CANINT	R/WC	1'b0	Can Bus Wake Up Interrupt
14	LWU	R/WC	1'b0	Local Wake Up
13	WKERR	R/WC	1'b0	Wake Error
12	RSVD	R	1'b0	Reserved
11	RSVD	R	1'b0	Reserved
10	CANSLNT	R/WC	1'b0	CAN Silent
9	RSVD	R	1'b0	Reserved
8	CANDOM	R/WC	1'b0	CAN Stuck Dominant
7	GLOBALERR	R	1'b0	Global Error (Any Fault)
6	WKRQ	R	1'b0	Wake Request
5	CANERR	R	1'b0	CAN Error
4	RSVD	R	1'b0	RSVD
3	SPIERR	R	1'b0	SPI Error
2	RSVD	R	1'b0	Reserved
1	M_CAN_INT	R	1'b0	M_CAN global INT

Table 18. Interrupts Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VTWD	R	1'b0	Global Voltage, Temp or WDTO

GLOBALERR: Logical OR of all faults in registers 0x0820-0824.

WKRQ: Logical OR of CANINT, LWU and WKERR.

CANBUSNOM is not an interrupt but a flag. In normal mode after the first dominant-recessive transition it will set. It will reset to 0 when entering Standby or Sleep modes or when a bus fault condition takes place in normal mode.

CANERR: Logical OR of CANSLNT and CANDOM faults.

SPIERR: Will be set if any of the SPI status register 16'h000C[30:16] is set.

- In the event of a SPI underflow, the error is not detected/alerted until the start of the next SPI transaction.
- 16'h0010[30:16] are the mask for these errors

VTWD: Logical or of UV_{CCFLTR}, UVSUP, TSD and ECCERR.

CANINT: Indicates a WUP has occurred; Once a CANINT flag is set, LWU events will be ignored. Flag can be cleared by changing to Normal or Sleep modes.

LWU: Indicates a local wake event, from toggling the WAKE pin, has occurred. Once a LWU flag is set, CANINT events will be ignored. Flag can be cleared by changing to Normal or Sleep modes.

WKERR: If the device receives a wake up request and does not transition to Normal mode or clear the PWRON or Wake flag before $t_{INACTIVE}$, the device will transition to Sleep Mode. After the wake event, a Wake Error (WKERR) will be reported and the SMS flag will be set to 1.

CANTO: CAN Timeout: flag indicates a CAN bus timeout event while in Standby mode with frame detection enabled. If there is no activity on the CAN bus for more than $t_{SILENCE}$ while in Standby mode with frame detect enabled, this flag is set.

NOTE

PWRON Flag is cleared by either writing a 1 or by going to sleep mode or normal mode from standby mode.

8.6.3.2 MCAN Interrupts (address = h0824) [reset = h00000000]

Figure 45. MCAN Interrupts

31	30	29	28	27	26	25	24
RSVD		ARA	PED	PEA	WDI	BO	EW
R		R	R	R	R	R	R
23	22	21	20	19	18	17	16
EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R	R	R	R	R	R	R	R

Table 19. MCAN Interrupts Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	1'b0	Reserved
29	ARA	R	1'b0	ARA: Access to Reserved Address
28	PED	R	1'b0	PED: Protocol Error in Data Phase (Data Bit Time is used)
27	PEA	R	1'b0	PEA: Protocol Error in Arbitration Phase (Nominal Bit Time is used)
26	WDI	R	1'b0	WDI: Watchdog Interrupt
25	BO	R	1'b0	BO: Bus_Off Status
24	EW	R	1'b0	EW: Warning Status
23	EP	R	1'b0	EP: Error Passive
22	ELO	R	1'b0	ELO: Error Logging Overflow
21	BEU	R	1'b0	BEU: Bit Error Uncorrected
20	BEC	R	1'b0	BEC: Bit Error Corrected
19	DRX	R	1'b0	DRX: Message stored to Dedicated Rx Buffer
18	TOO	R	1'b0	TOO: Timeout Occurred
17	MRAF	R	1'b0	MRAF: Message RAM Access Failure
16	TSW	R	1'b0	TSW: Timestamp Wraparound
15	TEFL	R	1'b0	TEFL: Tx Event FIFO Element Lost
14	TEFF	R	1'b0	TEFF: Tx Event FIFO Full
13	TEFW	R	1'b0	TEFW: Tx Event FIFO Watermark Reached
12	TEFN	R	1'b0	TEFN: Tx Event FIFO New Entry
11	TFE	R	1'b0	TFE: Tx FIFO Empty
10	TCF	R	1'b0	TCF: Transmission Cancellation Finished
9	TC	R	1'b0	TC: Transmission Completed
8	HPM	R	1'b0	HPM: High Priority Message
7	RF1L	R	1'b0	RF1L: Rx FIFO 1 Message Lost
6	RF1F	R	1'b0	RF1F: Rx FIFO 1 Full
5	RF1W	R	1'b0	RF1W: Rx FIFO 1 Watermark Reached
4	RF1N	R	1'b0	RF1N: Rx FIFO 1 New Message
3	RF0L	R	1'b0	RF0L: Rx FIFO 0 Message Lost
2	RF0F	R	1'b0	RF0F: Rx FIFO 0 Full
1	RF0W	R	1'b0	RF0W: Rx FIFO 0 Watermark Reached
0	RF0N	R	1'b0	RF0N: Rx FIFO 0 New Message

8.6.3.3 Interrupt Enables (address = h0830) [reset = hFFFFFFFF]

Figure 46. 32-bit, 4 Rows

31	30	29	28	27	26	25	24
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
RSVD	UVSUP	RSVD	RSVD	TSD	RSVD	RSVD	ECCERR
R	R/W	R	R	R/W	R	R	R/W
15	**14**	13	12	11	10	9	8
CANINT	**LWU**	RSVD	RSVD	RSVD	CANSLNT	RSVD	CANDOM
R/W	R/W	R	R	R	R/W	R	R
7	6	5	4	3	2	1	0
RSVD							
R							

Table 20. Interrupt Enables Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	8'hFF	Reserved
23	RSVD	R	1'b1	Reserved
22	UVSUP	R/W	1'b1	Under Voltage V_{SUP} and UV_{CCFLTR}
21	RSVD	R	1'b1	Reserved
20	RSVD	R	1'b1	Reserved
19	TSD	R/W	1'b1	Thermal Shutdown
18	RSVD	R	1'b1	Reserved
17	RSVD	R	1'b1	Reserved
16	ECCERR	R/W	1'b1	Uncorrectable ECC error detected
15	**CANINT**	R/W	1'b1	Can Bus Wake Up Interrupt
14	**LWU**	R/W	1'b1	Local Wake Up
13	RSVD	R	1'b1	Reserved
12	RSVD	R	1'b1	Reserved
11	RSVD	R	1'b1	Reserved
10	CANSLNT	R/W	1'b1	CAN Silent
9	RSVD	R	1'b1	Reserved
8	CANDOM	R/W	1'b1	CAN Stuck Dominant
7:0	RSVD	R	8'hFF	Reserved

8.6.4 CAN FD Register Set: 16'h1000 to 16'h10FF

The following tables provide the CAN FD programming register sets starting at 16'h1000.

The MRAM and start address for the following registers has special consideration:

- SIDFC (0x1084)
- XIDFC (0x1088)
- RXF0C (0x10A0)
- RXF1C (0x10B0)
- TXBC (0x10C0)
- TXEFC (0x10F0)

The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.

When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Table 21. Legend

Code	Description
R	Read
C	Clear on Write
d	date
n	Value after Reset
p	Protected Set
P	Protected Write
r	Release
S	Set on Read
t	Test Value
U	Undefined
W	Write
X	Reset on Read

Table 22. CAN FD Register Set

ADDRESS	SYMBOL	NAME	RESET	ACC
1000	CREL	Core Release Register	rrrd dddd	R
1004	ENDN	Endian Register	8765 4321	R
1008	CUST	Customer Register	0000 0000	R
100C	DBTP	Data Bit Timing & Prescaler Register	0000 0A33	RP
1010	TEST	Test Register	0000 0000	RP
1014	RWD	RAM Watchdog	0000 0000	RP
1018	CCCR	CC Control Register	0000 0019	RWPp
101C	NBTP	Nominal Bit Timing & Prescaler Register	0600 0A03	RP
1020	TSCC	Timestamp Counter Configuration	0000 0000	RP
1024	TSCV	Timestamp Counter Value	0000 0000	RC
1028	TOCC	Timeout Counter Configuration	FFFF 0000	RP
102C	TOCV	Timeout Counter Value	0000 FFFF	RC
1030	RSVD	Reserved	0000 0000	R
1034	RSVD	Reserved	0000 0000	R
1038	RSVD	Reserved	0000 0000	R
103C	RSVD	Reserved	0000 0000	R
1040	ECR	Error Counter Register	0000 0000	RX
1044	PSR	Protocol Status Register	0000 0707	RXS

Table 22. CAN FD Register Set (continued)

ADDRESS	SYMBOL	NAME	RESET	ACC
1048	TDCR	Transmitter Delay Compensation Register	0000 0000	RP
104C	RSVD	Reserved	0000 0000	R
1050	IR	Interrupt Register	0000 0000	RW
1054	IE	Interrupt Enable	0000 0000	RW
1058	ILS	Interrupt Line Select	0000 0000	RW
105C	ILE	Interrupt Line Enable	0000 0000	RW
1060	RSVD	Reserved	0000 0000	R
1064	RSVD	Reserved	0000 0000	R
1068	RSVD	Reserved	0000 0000	R
106C	RSVD	Reserved	0000 0000	R
1070	RSVD	Reserved	0000 0000	R
1074	RSVD	Reserved	0000 0000	R
1078	RSVD	Reserved	0000 0000	R
107C	RSVD	Reserved	0000 0000	R
1080	GFC	Global Filter Configuration	0000 0000	RP
1084	SIDFC	Standard ID Filter Configuration	0000 0000	RP
1088	XIDFC	Extended ID Filter Configuration	0000 0000	RP
108C	RSVD	Reserved	0000 0000	R
1090	XIDAM	Extended ID and MASK	1FFF FFFF	RP
1094	HPMS	High Priority Message Status	0000 0000	R
1098	NDAT1	New Data 1	0000 0000	RW
109C	NDAT2	New Data 2	0000 0000	RW
10A0	RXF0C	Rx FIFO 0 Configuration	0000 0000	RP
10A4	RXF0S	Rx FIFO 0 Status	0000 0000	R
10A8	RXF0A	Rx FIFO 0 Acknowledge	0000 0000	RW
10AC	RXBC	Rx Buffer Configuration	0000 0000	RP
10B0	RXF1C	Rx FIFO 1 Configuration	0000 0000	RP
10B4	RXF1S	Rx FIFO 1 Status	0000 0000	R
10B8	RXF1A	Rx FIFO 1 Acknowledge	0000 0000	RW
10BC	RXESC	Rx Buffer/FIFO Element Size Configuration	0000 0000	RP
10C0	TXBC	Tx Buffer Configuration	0000 0000	RP
10C4	TXFQS	Tx FIFO/Queue Status	0000 0000	R
10C8	TXESC	Tx Buffer Element Size Configuration	0000 0000	RP
10CC	TXBRP	Tx Buffer Request Pending	0000 0000	R
10D0	TXBAR	Tx Buffer Add Request	0000 0000	RW
10D4	TXBCR	Tx Buffer Cancellation Request	0000 0000	RW
10D8	TXBTO	Tx Buffer Transmission Occurred	0000 0000	R
10DC	TXBCF	Tx Buffer Cancellation Finished	0000 0000	R
10E0	TXBTIE	Tx Buffer Transmission Interrupt Enable	0000 0000	RW
10E4	TXBCIE	Tx Buffer Cancellation Finished Interrupt Enable	0000 0000	RW
10E8	RSVD	Reserved	0000 0000	R
10EC	RSVD	Reserved	0000 0000	R
10F0	TXEFC	Tx Event FIFO Configuration	0000 0000	RP
10F4	TXEFS	Tx Event FIFO Status	0000 0000	R
10F8	TXEFA	Tx Event FIFO Acknowledge	0000 0000	RW
10FC	RSVD	Reserved	0000 0000	R

Table 23. CAN FD Register Set Description

Offset	Name	Bit Pos.	MSB							LSB	Access
1000	CREL	7:0	Day[7:0] (two digit, BCD-Coded)								R
		15:8	Month[15:8] (two digit, BCD-Coded)								R
		23:16	SUBSTEP[7:4] (One digit, BCD-Coded)				Year[3:0] (one digit, BCD-Coded)				R
		31:24	REL[7:4] (One digit, BCD-Coded)				STEP[3:0] (one digit, BCD-Coded)				R
1004	ENDN	7:0	ETV[7:0] (Endianness Test Value)								R
		15:8	ETV[15:8] (Endianness Test Value)								R
		23:16	ETV[23:16] (Endianness Test Value)								R
		31:24	ETV[31:24] (Endianness Test Value)								R
1008	CUST	7:0									
		15:8									
		23:16									
		31:24									
100C	DBTP	7:0	DTSEG2(Data Time Seg before Sample Point)				DSJW (Data (Re)Synchronization Jump Width)				RP
		15:8	Reserved				DTSEG1(Data Time Seg before Sample Point)				RP
		23:16	TDC	Reserved			DBRP (Data Bit Rate Prescaler)				RP
		31:24	Reserved								R
1010	TEST	7:0	RX	TX		LBCK	Reserved				RP-U
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
1014	RWD	7:0	WDC (Watchdog Configuration)								RP
		15:8	WDV (Watchdog Counter Value)								R
		23:16	Reserved								R
		31:24	Reserved								R
1018	CCCR	7:0	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT	RWp
		15:8	NISO	TXP	EFBI	PXHD	Reserved		BRSE	FDOE	RP
		23:16	Reserved								R
		31:24	Reserved								R
101C	NBTP	7:0	Reserved	NTSEG2 (Nominal time Segment After Sample Point)							RP
		15:8	NTSEG1 (Nominal Time Segment Before Sample Point)								RP
		23:16	NBRP[7:0] (Nominal Bit Rate Prescaler)								RP
		31:24	NSJW[6;0] (Nominal (RE)Synchronization Jump Width)							NBRP[8]	RP
1020	TSCC	7:0	Reserved						TSS[1:0] Timestamp Select		RP
		15:8	Reserved								R
		23:16	Reserved				TCP (Timestamp Counter Prescaler)				RP
		31:24	Reserved								R
1024	TSCV	7:0	TSC[15:0] (Timestamp Counter)								RC
		15:8									RC
		23:16	Reserved								R
		31:24	Reserved								R
1028	TOCC	7:0	Reserved					TOS (Timeout SEL)		ETOC	RP
		15:8	Reserved								R
		23:16	TOP[15:0] (Timeout Period)								RP
		31:24									RP
102C	TOCV	7:0	TOC[15:0] (Timeout Counter)								RC
		15:8									RC
		23:16	Reserved								R
		31:24	Reserved								R
1030 – 103C	RSVD	31:0	Reserved								R
1040	ECR	7:0	TEC (Transmit Error Counter)								R
		15:8	REC (Receive Error Counter)								R
		23:16	CEL (CAN Error Logging)								X
		31:24	Reserved								R

Table 23. CAN FD Register Set Description (continued)

Offset	Name	Bit Pos.	MSB							LSB	Access
1044	PSR	7:0	BO	EW	EP	ACT (Activity)		LEC (Last Error Code)			RS
		15:8	Reserved	PXE	RFDF	RBRS	RESI	DLEC (Data Phase Last Error Code)			RSX
		23:16	Reserved	TDCV[6:0] (Transmitter Delay Compensation Value)							R
		31:24	Reserved								R
1048	TDCE	7:0	Reserved	TDCF (Transmitter Delay Compensation Filter Window Length)							RP
		15:8	Reserved	TDCO (Transmitter Delay Compensation Offset)							RP
		23:16	Reserved								R
		31:24	Reserved								R
104C	RSVD	31:0	Reserved								R
1050	IR	7:0	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N	R/W
		15:8	TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	R/W
		23:16	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW	R/W
		31:24	Reserved		ARA	PED	PEA	WDI	BO	EW	R/W
1054	IE	7:0	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE	R/W
		15:8	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	R/W
		23:16	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE	R/W
		31:24	Reserved		ARAE	PEDE	PEAE	WDIE	BOE	EWE	R/W
1058	ILS	7:0	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL	R/W
		15:8	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	R/W
		23:16	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL	R/W
		31:24	Reserved		ARAL	PEDL	PEAL	WDIL	BOL	EWL	R/W
105C	ILE	7:0	Reserved						EINT1	EINT0	R/W
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
1060 – 107C	RSVD	31:0	Reserved								R
1080	GFC	7:0	Reserved		ANFS		ANFE		RRFS	RRFE	RP
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
1084	SIDFC	7:0	FLSS[7:2] (Filter List Standard Start Address)						Reserved		RP
		15:8	FLSS[15:8] (Filter List Standard Start Address)								RP
		23:16	LSS (List Size Standard)								RP
		31:24	Reserved								R
1088	XIDFC	7:0	FLESA[7:2] (Filter List Extended Start Address)						Reserved		RP
		15:8	FLESA[15:8] (Filter List Extended Start Address)								RP
		23:16	Reserved	LSE (List Size Extended)							RP
		31:24	Reserved								R
108C	RSVD	31:0	Reserved								R
1090	XIDAM	7:0	EIDM[7:0] (Extended ID AND MASK)								RP
		15:8	EIDM[15:8] (Extended ID AND MASK)								RP
		23:16	EIDM[23:16] (Extended ID AND MASK)								RP
		31:24	Reserved			EIDM[28:24] (Extended ID AND MASK)					RP
1094	HPMS	7:0	MSI (Message Storage Index)		BIDX (Buffer Index)						R
		15:8	FLST	FIDX (Filter Index)							R
		23:16	Reserved								R
		31:24	Reserved								R
1098	NDAT1	7:0	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0	R/W
		15:8	ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8	R/W
		23:16	ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16	R/W
		31:24	ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24	R/W
109C	NDAT2	7:0	ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32	R/W
		15:8	ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40	R/W
		23:16	ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48	R/W
		31:24	ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56	R/W

Table 23. CAN FD Register Set Description (continued)

Offset	Name	Bit Pos.	MSB							LSB	Access
10A0	RXF0C	7:0	F0SA[7:2] (RX FIFO 0 Start Address)						Reserved		RP
		15:8	F0SA[15:8] (RX FIFO 0 Start Address)								RP
		23:16	Reserved	F0S (RX FIFO 0 Size)							RP
		31:24	F0OM	F0WM (RX FIFO 0 Watermark)							RP
10A4	RXF0S	7:0	Reserved								R
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
10A8	RXF0A	7:0	Reserved	F0A (RX FIFO 0 Acknowledge Index)							R/W
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
10AC	RXBC	7:0	RBSA[7:2] (RX Buffer Configuration)						Reserved		RP
		15:8	RBSA[15:8] (RX Buffer Configuration)								RP
		23:16	Reserved								R
		31:24	Reserved								R
10B0	RXF1C	7:0	F1SA[7:2] (RX FIFO 1 Start Address)						Reserved		RP
		15:8	F1SA[15:8] (RX FIFO 1 Start Address)								RP
		23:16	Reserved	F1S (RX FIFO 1 Size)							RP
		31:24	F1OM	F1WM (RX FIFO 1 Watermark)							RP
10B4	RXF1S	7:0	Reserved	F1FL (RX FIFO 1 Fill Level)							R
		15:8	Reserved	F1GI (RX FIFO 1 Get Index)							R
		23:16	Reserved	F1PI (RX FIFO 1 Put Index)							R
		31:24	DMS (Data Message Status)	Reserved					RF1L	F1F	R
10B8	RXF1A	7:0	Reserved	F1AI (RX FIFO 1 Acknowledge Index)							R/W
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
10BC	RXESC	7:0	Reserved	F1DS (RX FIFO 1 Data Field Size)			Reserved	F0DS (RX FIFO 0 Data Field Size)			RP
		15:8	Reserved				RBDS (RX Buffer Data Field Size)				RP
		23:16	Reserved								R
		31:24	Reserved								R
10C0	TXBC	7:0	TBSA[7:2] (TX Buffer Start Address)						Reserved		RP
		15:8	TBSA[15:8] (TX Buffer Start Address)								RP
		23:16	Reserved	NDTB (Number of Dedicated Transmit Buffers)							RP
		31:24	Reserved	TFQM		TFQS (Transmit FIFO/Queue Size)					RP
10C4	TXQFS	7:0	Reserved	TFFL (TX FIFO Free Level)							R
		15:8	Reserved			TFGI (TX FIFO Get Index)					R
		23:16	Reserved		TFQF	TFQP (TX FIFO/Queue Put Index)					R
		31:24	Reserved								R
10C8	TXESC	7:0	Reserved				TBDS (TX Buffer Data Field Size)				RP
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
10CC	TXBRP	7:0	TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0	R
		15:8	TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8	R
		23:16	TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16	R
		31:24	TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24	R
10D0	TXBAR	7:0	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0	R/W
		15:8	AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	R/W
		23:16	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16	R/W
		31:24	AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24	R/W
10D4	TXBCR	7:0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	RW
		15:8	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8	RW
		23:16	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16	RW
		31:24	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24	RW

Table 23. CAN FD Register Set Description (continued)

Offset	Name	Bit Pos.	MSB							LSB	Access
10D8	TXBTO	7:0	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0	R
		15:8	TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8	R
		23:16	TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16	R
		31:24	TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24	R
10DC	TXBCF	7:0	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	R
		15:8	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8	R
		23:16	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16	R
		31:24	CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24	R
10E0	TXBTIE	7:0	TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0	RW
		15:8	TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8	RW
		23:16	TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16	RW
		31:24	TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24	RW
10E4	TXBCIE	7:0	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0	RW
		15:8	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8	RW
		23:16	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16	RW
		31:24	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24	RW
10E8 - 10EC	RSVD	31:0	Reserved								R
10F0	TXEFC	7:0	EFSA[7:2] (Event FIFO Start Address)						Reserved		RP
		15:8	EFSA[15:8] (Event FIFO Start Address)								RP
		23:16	Reserved		EFS (Event FIFO Size)						RP
		31:24	Reserved		EFWM (Event FIFO Watermark)						RP
10F4	TXEFS	7:0	Reserved		EFFL (Event FIFO Fill Level)						
		15:8	Reserved			EFGI (Event FIFO Get Index)					
		23:16	Reserved			EFPI (Event FIFO Put Index)					
		31:24	Reserved						TEFL	EFF	R
10F8	TXEFA	7:0	Reserved			EFA (Event FIFO Acknowledge Index)					RW
		15:8	Reserved								R
		23:16	Reserved								R
		31:24	Reserved								R
10FC	RSVD	31:0	Reserved								R

8.6.4.1 Core Release Register (address = h1000) [reset = hrrrddddd]

Figure 47. Core Release Register

31	30	29	28	27	26	25	24
REL[3:0]				STEP[3:0]			
R				R			
23	22	21	20	19	18	17	16
SUBSTEP[3:0]				YEAR[3:0]			
R				R			
15	14	13	12	11	10	9	8
MONTH[7:0]							
R							
7	6	5	4	3	2	1	0
DAY[7:0]							
R							

Table 24. Core Release Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REL[3:0]	R	r	one digit, BCD-coded
27:24	STEP[3:0]	R	r	one digit, BCD-coded
23:20	SUBSTEP[3:0]	R	r	one digit, BCD-coded
19:16	YEAR[3:0]	R	d	one digit, BCD-coded
15:8	MONTH[7:0]	R	d	two digit, BCD-coded
7:0	DAY[7:0]	R	d	two digit, BCD-coded

8.6.4.2 Endian Register (address = h1004) [reset = h87654321]

Figure 48. Endian Register

31	30	29	28	27	26	25	24
ETV[31:24]							
R							
23	22	21	20	19	18	17	16
ETV[23:16]							
R							
15	14	13	12	11	10	9	8
ETV[15:8]							
R							
7	6	5	4	3	2	1	0
ETV[7:0]							
R							

Table 25. Endian Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ETV[31:24]	R	0x87	Endianness Test Value
23:16	ETV[23:16]	R	0x65	Endianness Test Value
15:8	ETV[15:8]	R	0x43	Endianness Test Value
7:0	ETV[7:0]	R	0x21	Endianness Test Value

8.6.4.3 Customer Register (address = h1008) [reset = h00000000]

Figure 49. Customer Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 26. Customer Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	h00000000	Reserved

8.6.4.4 Data Bit Timing & Prescaler (address = h100C) [reset = h0000A33]

Figure 50. Data Bit Timing & Prescaler

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
TDC	RSVD		DBRP[4:0]				
n	R		RP				
15	14	13	12	11	10	9	8
RSVD			DTSEG1[4:0]				
R			RP				
7	6	5	4	3	2	1	0
DTSEG2[3:0]				DSJW[3:0]			
RP				RP			

Table 27. Data Bit Timing & Prescaler Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23	TDC	RP	0x0	Transmitter Delay Compensation 0 – TDC Disabled 1 – TDC Enabled
22:21	RSVD	R	0x0	Reserved
20:16	DBRP[4:0]	RP	0x0	Data Bit Rate Prescaler
15:13	RSVD	R	0x0	Reserved
12:8	DTSEG1[4:0]	RP	0xA	Data time Segment before sample point
7:4	DTSEG2[3:0]	RP	0x3	Data time Segment before sample point
2:0	DSJW[3:0]	RP	0x3	Data (Re)Synchronization Jump Width

8.6.4.5 Test Register (address = h1010) [reset = h00000000]

Figure 51. Test Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RX	TX[1:0]		LBCK	RSVD			
R	RP		RP	R			

Table 28. Test Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	RSVD	R	0x0	Reserved
7	RX	R	U	Receive Pin (m_can_rx) 0 – CAN Bus is Dominant 1 – CAN Bus is Recessive
6:5	TX[1:0]	RP	0x0	Control of Transmit Pin (m_can_tx) 00 – Reset Value, updated at the end of the CAN bit time 01 – Sample Point can be monitored at PIN m_can_tx 10 – Dominant (‘0’) level at pin 11 – Recessive (‘1’) level at pin
4	LBCK	RP	0	LBCK: Loop Back Mode 0 – Reset Value, Loop Back Mode is Disabled 1 – Loop Back Mode is Enabled
3:0	RSVD	R	0x0	Reserved

8.6.4.6 RAM Watchdog (address = h1014) [reset = h00000000]

Figure 52. RAM Watchdog

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
WDV[7:0]							
R							
7	6	5	4	3	2	1	0
WDC[7:0]							
RP							

Table 29. RAM Watchdog Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	WDV[7:0]	R	0x0	Watchdog Counter Value
7:0	WDC[7:0]	RP	0x0	Watchdog Configuration

8.6.4.7 Control Register (address = h1018) [reset = 0000 0019]

Figure 53. Control Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
NISO	TXP	EFBI	PXHD	RSVD		BRSE	FDOE
RP	RP	RP	RP	R		RP	RP
7	6	5	4	3	2	1	0
TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
Rp	RP	Rp	R/W	R	Rp	RP	R/W

Table 30. Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15	NISO	RP	0	Non ISO Operation 0 – CAN FD Frame format according to ISO 11898-1:2015 1 – CAN FD Frame format according to Bosch CAN FD Specification V1.0
14	TXP	RP	0	Transmitter Pause 0 – Transmitter Pause Disabled 1 – Transmitter Pause Enabled
13	EFBI	RP	0	Edge Filtering during Bus Integration 0 – Edge Filtering Disabled 1 – Two Consecutive Dominant tq required to detect an edge for hard synchronization
12	PXHD	RP	0	Protocol Exception Handling Disable 0 – Protocol Exception Handling Enabled 1 – Protocol Exception Handling Disabled
11:10	RSVD	R	0x0	Reserved
9	BRSE	RP	0	Bit Rate Switch Enable 0 – Bit Rate Switching for Transmission Disabled 1 – Bit Rate Switching for Transmission Enabled
8	FDOE	RP	0	FD Operation Enable 0 – FD Operation Disabled 1 – FD Operation Enabled
7	TEST	Rp	0	Test Mode Enable 0 – Normal Mode of Operation, Register TEST Holds Reset Value 1 – Test Mode, Write Access to Register TEST Enabled
6	DAR	RP	0	Disable Automatic Retransmission 0 – Automatic Retransmission of Messages not Transmitted Successfully Enabled 1 – Automatic Retransmission Disabled
5	MON	Rp	0	Bus Monitoring Mode is Disabled 0 – Bus Monitoring Mode is Disabled 1 – Bus Monitoring Mode is Enabled
4	CSR	R/W	1	Clock Stop Request 0 – No clock Stop is requested 1 – Clock Stop Requested. When requested first INIT and then CSA will be set after all pending transfer request have completed and the CAN bus reached idle See NOTE section

Table 30. Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CSA	R	1	Clock Stop Acknowledge 0 – No Clock Stop Requested 1 – m_can may be set in power down by stopping m_can-hclk and m_can_cclk
2	ASM	Rp	0	Restricted Operation Mode 0 – Normal CAN Operation 1 – Restricted Operation Mode Active
1	CCE	RP	0	Configuration Change Enable 0 – CPU has no write access to the protected configuration registers 1 – CPU has write access to the protected configuration registers (While CCCR.INIT =1)
0	INIT	R/W	1	Initialization 0 – Normal Operation 1 – Initialization has started

NOTE

The TCAN4551-Q1 handles stop request through hardware. The means that a 1 should not be written to CCCR.CSR (Clock Stop Request) as this will interfere with normal operation. If a Read-Modify-Write operation is performed in Standby mode a CSR = 1 will be read back but a 0 should be written to it.

8.6.4.8 Nominal Bit Timing & Prescaler Register (address = h101C) [reset = h06000A03]

Figure 54. Nominal Bit Timing & Prescaler Register

31	30	29	28	27	26	25	24
NSJW[6:0]							NBRP[8]
RP							RP
23	22	21	20	19	18	17	16
NBRP[7:0]							
RP							
15	14	13	12	11	10	9	8
NTSEG1[7:0]							
RP							
7	6	5	4	3	2	1	0
RSVD	NTSEG2[6:0]						
R	RP						

Table 31. Nominal Bit Timing & Prescaler Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NSJW[6:0]	RP	0x3	Nominal (RE)Synchronization Jump Width 0x00 - 0x7F – Valid values are 0 to 127 - The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
24:16	NBRP[8:0]	RP	0x0	Nominal Bit Rate Prescaler 0x000 - 0x1FF – Value by which the oscillator frequency is divided for generating the bit time quanta. Valid values are 0 to 511. - The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:8	NTSEG1[7:0]	RP	0xA	Nominal Time Segment Before Sample Point) 0x01-0xFF – Valid values are 1 to 255 - The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
7	RSVD	R	0	Reserved
6:0	NTSEG2[6:0]	RP	0x3	Nominal Time Segment After Sample Point 0x01-0x7F – Valid values are 1 to 127 - The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

8.6.4.9 Timestamp Counter Configuration (address = h1020) [reset = h00000000]

Figure 55. Timestamp Counter Configuration

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD				TCP[3:0]			
R				RP			
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD						TSS[1:0]	
R						RP	

Table 32. Timestamp Counter Configuration Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:20	RSVD	R	0x0	Reserved
19:16	TCP[3:0]	RP	0x0	Timestamp Counter Prescaler 0x0 - 0xF – Configures timestamp and timeout counters time unit in multiples of CAN bit times [1…16]
15:8	RSVD	R	0x0	Reserved
7:2	RSVD	R	0x0	Reserved
1:0	TSS[1:0]	RP	0x0	Timestamp Select 00 – Timestamp counter value always 0x0000 01 – Timestamp counter value incremented according to TCP 10 – External timestamp counter value used 11 – Same as "00"

8.6.4.10 Timestamp Counter Value (address = h1024) [reset = h00000000]

Figure 56. Timestamp Counter Value

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
TSC[15:8]							
RC							
7	6	5	4	3	2	1	0
TSC[7:0]							
RC							

Table 33. Timestamp Counter Value Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:20	RSVD	R	0x0	Reserved
15:8	TSC[7:0]	RC	0x0	Timestamp Counter The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = “01”, the Timestamp Counter is incremented in multiples of CAN bit times [1…16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = “10”, TSC reflects the external Timestamp Counter value. A write access has no impact.
7:0	TSC[7:0]	RC	0x0	Timestamp Counter The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = “01”, the Timestamp Counter is incremented in multiples of CAN bit times [1…16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = “10”, TSC reflects the external Timestamp Counter value. A write access has no impact.

8.6.4.11 Timeout Counter Configuration (address = h1028) [reset = hFFFF0000]

Figure 57. Timeout Counter Configuration

31	30	29	28	27	26	25	24
TOP[15:8]							
R							
23	22	21	20	19	18	17	16
TOP[7:0]							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD					TOS[1:0]		ETOC
R					RP		RP

Table 34. Timeout Counter Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TOP[15:8]	RP	0xFF	Timeout Period Start value of the timeout counter (down-counter). Configures the timeout period
23:16	TOP[7:0]	RP	0xFF	Timeout Period Start value of the timeout counter (down-counter). Configures the timeout period
15:8	RSVD	R	0x0	Reserved
7:3	RSVD	R	0x0	Reserved
2:1	TOS[1:0]	RP	0x0	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored 00 – Continuous Operation 01 – Timeout controlled by TX Event FIFO 10 – Timeout controlled by Rx FIFO 0 11 – Timeout controlled by Rx FIFO 1
0	ETOC	RP	0	Enable Timeout Counter 0 – Timeout counter disabled 1 – Timeout counter enabled

8.6.4.12 Timeout Counter Value (address = h102C) [reset = h0000FFFF]

Figure 58. Timeout Counter Value

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
TOC[15:8]							
RC							
7	6	5	4	3	2	1	0
TOC[7:0]							
RC							

Table 35. Timeout Counter Value Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	TOC[15:8]	RC	0xFF	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1…16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS
7:0	TOC[7:0]	RC	0xFF	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1…16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS

8.6.4.13 Reserved (address = h1030 - h103C) [reset = h00000000]

Figure 59. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 36. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

8.6.4.14 Error Counter Register (address = h1040) [reset = h00000000]

Figure 60. Error Counter Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
CEL[7:0]							
X							
15	14	13	12	11	10	9	8
RP	REC[6:0]						
R	R						
7	6	5	4	3	2	1	0
TEC[7:0]							
R							

Table 37. Error Counter Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	CEL[7:0]	X	0x0	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO
15	RP	R	0	0 – The Receive Error Counter is below the error passive level of 128 1 – The Receive Error Counter has reached the error passive level of 128
14:8	REC[6:0]	R	0x0	Actual state of the Receive Error Counter, values between 0 and 127
7:0	TEC[7:0]	R	0x0	Actual state of the Transmit Error Counter, values between 0 and 255

NOTE

When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.

8.6.4.15 Protocol Status Register (address = h1044) [reset = h00000707]

Figure 61. Protocol Status Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD	TDCV[6:0]						
R	R						
15	14	13	12	11	10	9	8
RSVD	PXE	RFDF	RBRS	RESI	DLEC[2:0]		
R	X	X	X	X	S		
7	6	5	4	3	2	1	0
BO	EW	EP	ACT[1:0]		LEC[2:0]		
R	R	R	R		S		

Table 38. Protocol Status Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23	RSVD	R	0x0	Reserved
22:16	TDCV[6:0]	R	0x0	Transmitter Delay Compensation Value 0x00-0x7F – Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.
15	RSVD	R	0	Reserved
14	PXE	X	0	Protocol Exception Event 0 – No protocol exception event occurred since last read access 1 – Protocol exception event occurred
13	RFDF	X	0	Received a CAN FD Message This bit is set independent of acceptance filtering 0 – Since this bit was reset by the CPU, no CAN FD message has been received 1 – Message in CAN FD format with FDF flag set has been received
12	RBRS	X	0	BRS flag of last received CAN FD Message This bit is set together with RFDF, independent of acceptance filtering. 0 – Last received CAN FD message did not have its BRS flag set 1 – Last received CAN FD message had its BRS flag set
11	RESI	X	0	ESI flag of last received CAN FD Message This bit is set together with RFDF, independent of acceptance filtering. 0 – Last received CAN FD message did not have its ESI flag set 1 – Last received CAN FD message had its ESI flag set
10:8	DLEC[2:0]	X	0x7	Data Phase Last Error Code Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	BO	R	0	Bus_Off Status 0 – The M_CAN is not Bus_Off 1 – The M_CAN is in Bus_Off state
6	EW	R	0	Warning Status 0 – Both error counters are below the Error_Warning limit of 96 1 – At least one of error counter has reached the Error_Warning limit of 96

Table 38. Protocol Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EP	R	0	Error Passive 0 – The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1 – The M_CAN is in the Error_Passive state
4:3	ACT[1:0]	R	0x0	Activity Monitors the module's CAN communication state. 00 – Synchronizing - node is synchronizing on CAN communication 01 – Idle - node is neither receiver nor transmitter 10 – Receiver - node is operating as receiver 11 – Transmitter - node is operating as transmitter
2:0	LEC[2:0]	S	0x7	Last Error Code The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0 – No Error: No error occurred since LEC has been reset by successful reception or transmission 1 – Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2 – Form Error: A fixed format part of a received frame has the wrong format. 3 – AckError: The message transmitted by the M_CAN was not acknowledged by another node. 4 – Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5 – Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value '0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6 – CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7 – NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register.

NOTE

When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in DLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error

NOTE

The Bus_Off recovery sequence (see ISO 11898-1:2015) cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily checkup whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

8.6.4.16 Transmitter Delay Compensation Register (address = h1048) [reset = h00000000]

Figure 62. Transmitter Delay Compensation Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD	TDCO[6:0]						
R	RP						
7	6	5	4	3	2	1	0
RSVD	TDCF[6:0]						
R	RP						

Table 39. Transmitter Delay Compensation Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15	RSVD	R	0	Reserved
14:8	TDCO[6:0]	RP	0x0	Transmitter Delay Compensation Offset 0x00-0x7F - Offset value defining the distance between the measured delay from m_can_tx to m_can_rx and the secondary sample point. Valid values are 0 to 127 mtq.
7	RSVD	R	0	Reserved
6:0	TDCF[6:0]	RP	0x0	Transmitter Delay Compensation Filter Window Length 0x00-0x7F - Defines the minimum value of the SSP position, dominant edges on m_can_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq.

8.6.4.17 Reserved (address = h104C) [reset = h00000000]

Figure 63. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 40. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

8.6.4.18 Interrupt Register (address = h1050) [reset = h00000000]

Figure 64. Interrupt Register

31	30	29	28	27	26	25	24
RSVD		ARA	PED	PEA	WDI	BO	EW
R		R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
EP	ELO	BEU	BEC	DRX	TOO	MRF	TSW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 41. Interrupt Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	0x0	Reserved
29	ARA	R/W	0	Access to Reserved Address 0 – No access to reserved address occurred 1 – Access to reserved address occurred
28	PED	R/W	0	Protocol Error in Data Phase (Data Bit Time is used) 0 – No protocol error in data phase 1 – Protocol error in data phase detected (PSR.DLEC ≠ 0,7)
27	PEA	R/W	0	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0 – No protocol error in arbitration phase 1 – Protocol error in arbitration phase detected (PSR.LEC ≠ 0,7)
26	WDI	R/W	0	Watchdog Interrupt 0 – No Message RAM Watchdog event occurred 1 – Message RAM Watchdog event due to missing READY
25	BO	R/W	0	Bus_Off Status 0 – Bus_Off status unchanged 1 – Bus_Off status changed
24	EW	R/W	0	Warning Status 0 – Error_Warning status unchanged 1 – Error_Warning status changed
23	EP	R/W	0	Error Passive 0 – Error_Passive status unchanged 1 – Error_Passive status changed
22	ELO	R/W	0	ELO: Error Logging Overflow 0 – CAN Error Logging Counter did not overflow 1 – Overflow of CAN Error Logging Counter occurred
21	BEU	R/W	0	Bit Error Uncorrected Message RAM bit error detected, uncorrected. Controlled by input signal m_can_aeim_berr[1] generated by an optional external parity / ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0 – No bit error detected when reading from Message RAM 1 – Bit error detected, uncorrected (e.g. parity logic)
20	BEC	R/W	0	Bit Error Corrected Message RAM bit error detected and corrected. Controlled by input signal m_can_aeim_berr[0] generated by an optional external parity / ECC logic attached to the Message RAM. 0 – No bit error detected when reading from Message RAM 1 – Bit error detected and corrected (e.g. ECC)

Table 41. Interrupt Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	DRX	R/W	0	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0 – No Rx Buffer updated 1 – At least one received message stored into an Rx Buffer
18	TOO	R/W	0	Timeout Occurred 0 – No timeout 1 – Timeout reached
17	MRF	R/W	0	Message RAM Access Failure The flag is set, when the Rx Handler • has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler start processing of the following message • was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_CAN is switched into Restricted Operation Mode. To leave restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0 – No Message RAM access failure occurred 1 – Message RAM access failure occurred
16	TSW	R/W	0	Timestamp Wraparound 0 – No timestamp counter wrap-around 1 – Timestamp counter wrapped aroundo
15	TEFL	R/W	0	Tx Event FIFO Element Lost 0 – No Tx Event FIFO element lost 1 – Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W	0	Tx Event FIFO Full 0 – Tx Event FIFO not full 1 – Tx Event FIFO full
13	TEFW	R/W	0	Tx Event FIFO Watermark Reached 0 – Tx Event FIFO fill level below watermark 1 – Tx Event FIFO fill level reached watermark
12	TEFN	R/W	0	Tx Event FIFO New Entry 0 – Tx Event FIFO unchanged 1 – Tx Handler wrote Tx Event FIFO element
11	TFE	R/W	0	Tx FIFO Empty 0 – Tx FIFO non-empty 1 – Tx FIFO empty
10	TCF	R/W	0	Transmission Cancellation Finished 0 – No transmission cancellation finished 1 – Transmis
9	TC	R/W	0	Transmission Completed 0 – No transmission completed 1 – Transmission completed
8	HPM	R/W	0	High Priority Message 0 – No high priority message received 1 – High priority message received
7	RF1L	R/W	0	Rx FIFO 1 Message Lost 0 – No Rx FIFO 1 message lost 1 – Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	RF1F	R/W	0	Rx FIFO 1 Full 0 – Rx FIFO 1 not full 1 – Rx FIFO 1 full

Table 41. Interrupt Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RF1W	R/W	0	Rx FIFO 1 Watermark Reached 0 – Rx FIFO 1 fill level below watermark 1 – Rx FIFO 1 fill level reached watermark
4	RF1N	R/W	0	Rx FIFO 1 New Message 0 – No new message written to Rx FIFO 1 – New message written to Rx FIFO 1
3	RF0L	R/W	0	Rx FIFO 0 Message Lost 0 – No Rx FIFO 0 message lost 1 – Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W	0	Rx FIFO 0 Full 0 – Rx FIFO 0 not full 1 – Rx FIFO 0 full
1	RF0W	R/W	0	Rx FIFO 0 Watermark Reached 0 – Rx FIFO 0 fill level below watermark 1 – Rx FIFO 0 fill level reached watermark
0	RF0N	R/W	0	Rx FIFO 0 New Message 0 – No new message written to Rx FIFO 0 1 – New message written to Rx FIFO 0

8.6.4.19 Interrupt Enable (address = h1054) [reset = h00000000]

The settings in the Interrupt Enable register determine which status changes in the Interrupt Register will be signaled on an interrupt line.

- 0 – Interrupt disabled
- 1 – Interrupt enabled

Figure 65. Interrupt Enable Register

31	30	29	28	27	26	25	24
RSVD		ARAE	PEDE	PEAE	WDIE	BOE	EWE
R		R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
TEFLE	TEFFE	TEFW	TEFNE	TFEE	TCFE	TCE	HPME
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 42. Interrupt Enable Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	0x0	Reserved
29	ARAE	R/W	0	Access to Reserved Address Enable
28	PEDE	R/W	0	Protocol Error in Data Phase Enable
27	PEAE	R/W	0	Protocol Error in Arbitration Phase Enable
26	WDIE	R/W	0	Watchdog Interrupt Enable
25	BOE	R/W	0	Bus_Off Status Interrupt Enable
24	EWE	R/W	0	Warning Status Interrupt Enable
23	EPE	R/W	0	Error Passive Interrupt Enable
22	ELOE	R/W	0	Error Logging Overflow Interrupt Enable
21	BEUE	R/W	0	Bit Error Uncorrected Interrupt Enable
20	BECE	R/W	0	Bit Error Corrected Interrupt Enable
19	DRXE	R/W	0	Message stored to Dedicated Rx Buffer Interrupt Enable
18	TOOE	R/W	0	Timeout Occurred Interrupt Enable
17	MRAFE	R/W	0	Message RAM Access Failure Interrupt Enable
16	TSWE	R/W	0	Timestamp Wraparound Interrupt Enable
15	TEFLE	R/W	0	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	R/W	0	Tx Event FIFO Full Interrupt Enable
13	TEFW	R/W	0	Tx Event FIFO Watermark Reached Interrupt Enable
12	TEFNE	R/W	0	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	R/W	0	Tx FIFO Empty Interrupt Enable
10	TCFE	R/W	0	Transmission Cancellation Finished Interrupt Enable
9	TCE	R/W	0	Transmission Completed Interrupt Enable
8	HPME	R/W	0	High Priority Message Interrupt Enable
7	RF1LE	R/W	0	Rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	R/W	0	Rx FIFO 1 Full Interrupt Enable
5	RF1WE	R/W	0	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	R/W	0	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	R/W	0	Rx FIFO 0 Message Lost Interrupt Enable

Table 42. Interrupt Enable Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RF0FE	R/W	0	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	R/W	0	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	R/W	0	Rx FIFO 0 New Message Interrupt Enable

8.6.4.20 Interrupt Line Select (address = h1058) [reset = h00000000]

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

- 0 – Interrupt assigned to interrupt line m_can_int0
- 1 – Interrupt assigned to interrupt line m_can_int1

Figure 66. Interrupt Line Select Register

31	30	29	28	27	26	25	24
RSVD		ARAL	PEDL	PEAL	WDIL	BOL	EWL
R		R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43. Interrupt Line Select Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	0x0	Reserved
29	ARAL	R/W	0	Access to Reserved Address Line
28	PEDL	R/W	0	Protocol Error in Data Phase Line
27	PEAL	R/W	0	Protocol Error in Arbitration Phase Line
26	WDIL	R/W	0	Watchdog Interrupt Line
25	BOL	R/W	0	Bus_Off Status Interrupt Line
24	EWL	R/W	0	Warning Status Interrupt Line
23	EPL	R/W	0	Error Passive Interrupt Line
22	ELOL	R/W	0	Error Logging Overflow Interrupt Line
21	BEUL	R/W	0	Bit Error Uncorrected Interrupt Line
20	BECL	R/W	0	Bit Error Corrected Interrupt Line
19	DRXL	R/W	0	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	R/W	0	Timeout Occurred Interrupt Line
17	MRAFL	R/W	0	Message RAM Access Failure Interrupt Line
16	TSWL	R/W	0	Timestamp Wraparound Interrupt Line
15	TEFLL	R/W	0	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	R/W	0	Tx Event FIFO Full Interrupt Line
13	TEFWL	R/W	0	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	R/W	0	Tx Event FIFO New Entry Interrupt Line
11	TFEL	R/W	0	Tx FIFO Empty Interrupt Line
10	TCFL	R/W	0	Transmission Cancellation Finished Interrupt Line
9	TCL	R/W	0	Transmission Completed Interrupt Line
8	HPML	R/W	0	High Priority Message Interrupt Line
7	RF1LL	R/W	0	Rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	R/W	0	Rx FIFO 1 Full Interrupt Line
5	RF1WL	R/W	0	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	R/W	0	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	R/W	0	Rx FIFO 0 Message Lost Interrupt Line

Table 43. Interrupt Line Select Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RF0FL	R/W	0	Rx FIFO 0 Full Interrupt Line
1	RF0WL	R/W	0	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	R/W	0	Rx FIFO 0 New Message Interrupt Line

8.6.4.21 Interrupt Line Enable (address = h105C) [reset = h00000000]

Figure 67. Interrupt Line Enable Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD						EINT1	EINT0
R						R/W	R/W

Table 44. Interrupt Line Enable Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	RSVD	R	0x0	Reserved
7:2	RSVD	R	0x0	Reserved
1	EINT1	R/W	0	Enable Interrupt Line 1 0 - Interrupt line m_can_int1 disabled 1 - Interrupt line m_can_int1 enabled
0	EINT0	R/w	0	Enable Interrupt Line 0 0 - Interrupt line m_can_int0 disabled 1 - Interrupt line m_can_int0 enabled

8.6.4.22 Reserved (address = h1060 - h107C) [reset = h00000000]

Figure 68. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 45. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

8.6.4.23 Global Filter Configuration (address = h1080) [reset = h00000000]

Figure 69. Global Filter Configuration Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD		ANFS[1:0]		ANFE[1:0]		RRFS	RRFE
R		RP		RP		RP	RP

Table 46. Global Filter Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	RSVD	R	0x0	Reserved
7:6	RSVD	R	0x0	Reserved
5:4	ANFS[1:0]	RP	0x0	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00 - Accept in Rx FIFO 0 01 - Accept in Rx FIFO 1 10 - Reject 11 - Reject
3:2	ANFE[1:0]	RP	0x0	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00 - Accept in Rx FIFO 0 01 - Accept in Rx FIFO 1 10 - Reject 11 - Reject
1	RRFS	RP	0	Reject Remote Frames Standard 0 - Filter remote frames with 11-bit standard IDs 1 - Reject all remote frames with 11-bit standard IDs
0	RRFE	RP	0	Reject Remote Frames Extended 0 - Filter remote frames with 29-bit extended IDs 1 - Reject all remote frames with 29-bit extended IDs

8.6.4.24 Standard ID Filter Configuration (address = h1084) [reset = h00000000]

The MRAM and start address for this register, FLSSA, has special consideration.

- The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.
- When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Figure 70. Standard ID Filter Configuration Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
LSS[7:0]							
RP							
15	14	13	12	11	10	9	8
FLSSA[15:8]							
RP							
7	6	5	4	3	2	1	0
FLSSA[7:0]							
RP							

Table 47. Standard ID Filter Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	LSS[7:0]	RP	0x0	List Size Standard 0 - No standard Message ID filter 1-128 - Number of standard Message ID filter elements >128 - Values greater than 128 are interpreted as 128
15:0	FLSSA[15:0]	RP	0x0	Filter List Standard Start Address Start address of standard Message ID filter list

8.6.4.25 Extended ID Filter Configuration (address = h1088) [reset = h00000000]

The MRAM and start address for this register, FLSEA, has special consideration.

- The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.
- When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Figure 71. Extended ID Filter Configuration Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD	LSE[6:0]						
R	RP						
15	14	13	12	11	10	9	8
FLSEA[15:8]							
RP							
7	6	5	4	3	2	1	0
FLSEA[7:0]							
RP							

Table 48. Extended ID Filter Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23	RSVD	R	0	Reserved
22:16	LSE[6:0]	RP	0x0	List Size Extended 0 - No extended Message ID filter 1-64 - Number of extended Message ID filter elements >64 - Values greater than 64 are interpreted as 64
15:0	FLSEA[15:0]	RP	0x0	Filter List Extended Start Address Start address of extended Message ID filter list

8.6.4.26 Reserved (address = h108C) [reset = h00000000]

Figure 72. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 49. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

8.6.4.27 Extended ID AND Mask (address = h1090) [reset = h1FFFFFFF]

Figure 73. Extended ID AND Mask Register

31	30	29	28	27	26	25	24
RSVD		EIDM[28:24]					
R		RP					
23	22	21	20	19	18	17	16
EIDM[23:16]							
RP							
15	14	13	12	11	10	9	8
EIDM[15:8]							
RP							
7	6	5	4	3	2	1	0
RP-0xFF							
RP							

Table 50. Extended ID AND Mask Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	2'b00	Reserved
29:24	EIDM[28:24]	RP	6'b011111	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.
23:0	EIDM[23:16] to EIDM[7:0]	RP	0xFFFFFF	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

8.6.4.28 High Priority Message Status (address = h1094) [reset = h00000000]

Figure 74. High Priority Message Status Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
FLST	FIDX[6:0]						
R	R						
7	6	5	4	3	2	1	0
MSI[1:0]		BIDX[5:0]					
R		R					

Table 51. High Priority Message Status Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15	FLST	R	0x0	Filter List Indicates the filter list of the matching filter element. 0 - Standard Filter List 1 - Extended Filter List
14:8	FIDX[6:0]	R	0x0	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7:6	MSI[1:0]	R	0x0	Message Storage Indicator 00 - No FIFO selected 01 - FIFO message lost 10 - Message stored in FIFO 0 11 - Message stored in FIFO 1
5:0	BIDX[5:0]	R	0x0	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = ‘1’

8.6.4.29 New Data 1 (address = h1098) [reset = h00000000]

Figure 75. New Data 1 Register

31	30	29	28	27	26	25	24
ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 52. New Data 1 Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ND31 to ND0	R/W	0	The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a ’1’ to the corresponding bit position. Writing a ’0’ has no effect. A hard reset will clear the register. 0 - Rx Buffer not updated 1 - Rx Buffer updated from new message

8.6.4.30 New Data 2 (address = h109C) [reset = h00000000]

Figure 76. New Data 2 Register

31	30	29	28	27	26	25	24
ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 53. New Data 2 Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ND63 to ND32	R/W	0	The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a ’1’ to the corresponding bit position. Writing a ’0’ has no effect. A hard reset will clear the register 0 - Rx Buffer not updated 1 - Rx Buffer updated from new message

8.6.4.31 Rx FIFO 0 Configuration (address = h10A0) [reset = h00000000]

The MRAM and start address for this register, F0SA, has special consideration.

- The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.
- When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Figure 77. Rx FIFO 0 Configuration Register

31	30	29	28	27	26	25	24
F0OM	F0WM[6:0]						
RP	RP						
23	22	21	20	19	18	17	16
RSVD	F0S[6:0]						
R	RP						
15	14	13	12	11	10	9	8
F0SA[15:8]							
RP							
7	6	5	4	3	2	1	0
F0SA[7:0]							
RP							

Table 54. Rx FIFO 0 Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	RP	0	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode 0 - FIFO 0 blocking mode 1 - FIFO 0 overwrite mode
32:24	F0WM[6:0]	RP	0x0	Rx FIFO 0 Watermark 0 - Watermark interrupt disabled 1-64 - Level for Rx FIFO 0 watermark interrupt (IR.RF0W) >64 - Watermark interrupt disabled
23	RSVD	R	0	Reserved
22:16	F0S[6:0]	RP	0x0	Rx FIFO 0 Size 0 - No Rx FIFO 0 1-64 - Number of Rx FIFO 0 elements >64 - Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1
15:0	F0SA[15:0]	RP	0x00	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM

8.6.4.32 Rx FIFO 0 Status (address = h10A4) [reset = h00000000]

Figure 78. Rx FIFO 0 Status Register

31	30	29	28	27	26	25	24
RSVD						RF0L	F0F
R						R	R
23	22	21	20	19	18	17	16
RSVD		F0PI[5:0]					
R		R					
15	14	13	12	11	10	9	8
RSVD		F0GI[5:0]					
R		R					
7	6	5	4	3	2	1	0
RSVD	F0FL[6:0]						
R	R						

Table 55. Rx FIFO 0 Status Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RSVD	R	0x0	Reserved
25	RF0L	R	0	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0 - No Rx FIFO 0 message lost 1 - Rx FIFO 0 message lost; also set after write attempt to Rx FIFO 0 of size zero Note: Overwriting the oldest message when RXF0C.F0OM = '1' will not set this flag
24	F0F	R	0	Rx FIFO 0 Full 0 - Rx FIFO 0 not full 1 - Rx FIFO 0 full
23:22	RSVD	R	0x0	Reserved
21:16	F0PI[5:0]	R	0x0	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63
15:14	RSVD	R	0x0	Reserved
13:8	F0GI[5:0]	R	0x0	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63
7	RSVD	R	0	Reserved
6:0	F0FL[6:0]	R	0x0	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64.

8.6.4.33 Rx FIFO 0 Acknowledge (address = h10A8) [reset = h00000000]

Figure 79. Rx FIFO 0 Acknowledge Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD		F0AI[5:0]					
R		R/W					

Table 56. Rx FIFO 0 Acknowledge Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	RSVD	R	0x0	Reserved
7:6	RSVD	R	0x0	Reserved
5:0	F0AI[5:0]	R/W	0x0	Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

8.6.4.34 Rx Buffer Configuration (address = h10AC) [reset = h00000000]

Figure 80. Rx Buffer Configuration Register

31	30	29	28	27	26	25	24
RSVD							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RBSA[15:8]							
RP							
7	6	5	4	3	2	1	0
RBSA[7:0]							
RP							

Table 57. Rx Buffer Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:0	RBSA[15:0]	RP	0x0	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM . Also used to reference debug messages A,B,C

8.6.4.35 Rx FIFO 1 Configuration (address = h10B0) [reset = h00000000]

The MRAM and start address for this register, F1SA, has special consideration.

- The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.
- When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Figure 81. Rx FIFO 1 Configuration Register

31	30	29	28	27	26	25	24
F10M	F1WM[6:0]						
RP	RP						
23	22	21	20	19	18	17	16
RSVD	F1S[6:0]						
R	RP						
15	14	13	12	11	10	9	8
F1SA[15:8]							
RP							
7	6	5	4	3	2	1	0
F1SA[7:0]							
RP							

Table 58. Rx FIFO 1 Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31	F10M	RP	0	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode 0 - FIFO 1 blocking mode 1- FIFO 1 overwrite mode
30:24	F1WM[6:0]	RP	0x0	Rx FIFO 1 Watermark 0 - Watermark interrupt disabled 1-64 - Level for Rx FIFO 1 watermark interrupt (IR.RF1W) >64 - Watermark interrupt disabled
23	RSVD	R	0	Reserved
20:16	F1S[6:0]	RP	0x0	Rx FIFO 1 Size 0 - No Rx FIFO 1 1-64 - Number of Rx FIFO 1 elements >64 - Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1
15:0	F1SA[15:0]	RP	0x0	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM

8.6.4.36 Rx FIFO 1 Status (address = h10B4) [reset = h00000000]

Figure 82. Rx FIFO 1 Status Register

31	30	29	28	27	26	25	24
DMS[1:0]		RSVD				RF1L	F1F
R		R				R	R
23	22	21	20	19	18	17	16
RSVD		F1PI[5:0]					
R		R					
15	14	13	12	11	10	9	8
RSVD		F1GI[5:0]					
R		R					
7	6	5	4	3	2	1	0
RSVD	F1FL[6:0]						
R	R						

Table 59. Rx FIFO 1 Status Field Descriptions

Bit	Field	Type	Reset	Description
31:30	DMS[1:0]	R	0x0	Debug Message Status 00 - Idle state, wait for reception of debug messages, DMA request is cleared 01 - Debug message A received 10 - Debug messages A, B received 11 - Debug messages A, B, C received, DMA request is set
29:26	RSVD	R	0x0	Reserved
25	RF1L	R	0	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset 0 - No Rx FIFO 1 message lost 1 - Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Note: Overwriting the oldest message when RXF1C.F1OM = '1' will not set this flag.
24	F1F	R	0	Rx FIFO 1 Full 0 - Rx FIFO 1 not full 1 - Rx FIFO 1 full
23:22	RSVD	R	0x0	Reserved
21:16	F1PI[5:0]	R	0x0	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63
15:14	RSVD	R	0x0	Reserved
13:8	F1GI[5:0]	R	0x0	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63.
7	RSVD	R	0	Reserved
6:0	F1FL[6:0]	R	0x0	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64.

8.6.4.37 Rx FIFO 1 Acknowledge (address = h10B8) [reset = h00000000]

Figure 83. Rx FIFO 1 Acknowledge Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD		F1AI[5:0]					
R		R/W					

Table 60. Rx FIFO 1 Acknowledge Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	RSVD	R	0x0	Reserved
7:6	RSVD	R	0x0	Reserved
5:0	F1AI[5:0]	R/W	0x0	Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

8.6.4.38 Rx Buffer/FIFO Element Size Configuration (address = h10BC) [reset = h00000000]

Figure 84. Rx Buffer/FIFO Element Size Configuration Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD					RBDS[2:0]		
R					RP		
7	6	5	4	3	2	1	0
RSVD	F1DS[2:0]			RSVD	F0DS[2:0]		
R	RP			R	RP		

Table 61. Rx Buffer/FIFO Element Size Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
31:24	RSVD	R	0x0	Reserved
31:24	RSVD	R	0x0	Reserved
10:8	RBDS[2:0]	RP	0x0	Rx Buffer Data Field Size 000 - 8 byte data field 001 - 12 byte data field 010 - 16 byte data field 011 - 20 byte data field 100 - 24 byte data field 101 - 32 byte data field 110 - 48 byte data field 111 - 64 byte data field
7	RSVD	R	0	Reserved
6:4	F1DS[2:0]	RP	0x0	Rx FIFO 1 Data Field Size 000 - 8 byte data field 001 - 12 byte data field 010 - 16 byte data field 011 - 20 byte data field 100 - 24 byte data field 101 - 32 byte data field 110 - 48 byte data field 111 - 64 byte data field
3	RSVD	R	0	Reserved
2:0	F0DS[2:0]	RP	0x0	Rx FIFO 0 Data Field Size 000 - 8 byte data field 001 - 12 byte data field 010 - 16 byte data field 011 - 20 byte data field 100 - 24 byte data field 101 - 32 byte data field 110 - 48 byte data field 111 - 64 byte data field

8.6.4.39 Tx Buffer Configuration (address = h10C0) [reset = h00000000]

The MRAM and start address for this register, TBSA, has special consideration.

- The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.
- When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Figure 85. Tx Buffer Configuration Register

31	30	29	28	27	26	25	24
RSVD	TFQM	TFQS[5:0]					
R	RP	RP					
23	22	21	20	19	18	17	16
RSVD		NDTB[5:0]					
R		RP					
15	14	13	12	11	10	9	8
TBSA[15:8]							
RP							
7	6	5	4	3	2	1	0
TBSA[7:0]							
RP							

Table 62. Tx Buffer Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31	RSVD	R	0	Reserved
30	TFQM	RP	0	Tx FIFO/Queue Mode 0 - Tx FIFO operation 1 - Tx Queue operation
29:24	TFQS[5:0]	RP	0x0	Transmit FIFO/Queue Size 0 - No Tx FIFO/Queue 1-32 - Number of Tx Buffers used for Tx FIFO/Queue >32 - Values greater than 32 are interpreted as 32
23:22	RSVD	R	0x0	Reserved
21:16	NDTB[5:0]	RP	0x0	Number of Dedicated Transmit Buffers 0 - No Dedicated Tx Buffers 1-32 - Number of Dedicated Tx Buffers >32 - Values greater than 32 are interpreted as 32
15:0	TBSA[15:0]	RP	0x0	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

8.6.4.40 Tx FIFO/Queue Status (address = h10C4) [reset = h00000000]

Figure 86. Tx FIFO/Queue Status Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD		TFQF	TFQPI[4:0]				
R		R	R				
15	14	13	12	11	10	9	8
RSVD			TFGI[4:0]				
R			R				
7	6	5	4	3	2	1	0
RSVD		TFFL[5:0]					
R		R					

Table 63. Tx FIFO/Queue Status Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:22	RSVD	R	0x0	Reserved
21	TFQF	R	0	Tx FIFO/Queue Full 0 - Tx FIFO/Queue not full 1 - Tx FIFO/Queue full
20:16	TFQPI[4:0]	R	0x0	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31.
15:13	RSVD	R	0x0	Reserved
12:8	TFGI[4:0]	R	0x0	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = ‘1’).
7:6	RSVD	R	0x0	Reserved
5:0	TFFL[5:0]	R	0x0	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = ‘1’) Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO

8.6.4.41 Tx Buffer Element Size Configuration (address = h10C8) [reset = h00000000]

Figure 87. Tx Buffer Element Size Configuration Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD					TBDS[2:0]		
R					RP		

Table 64. Tx Buffer Element Size Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:8	RSVD	R	0x0	Reserved
7:3	RSVD	R	0x0	Reserved
2:0	TBDS[2:0]	RP	0x0	Tx Buffer Data Field Size 000 - 8 byte data field 001 - 12 byte data field 010 - 16 byte data field 011 - 20 byte data field 100 - 24 byte data field 101 - 32 byte data field 110 - 48 byte data field 111 - 64 byte data field Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as “0xCC” (padding bytes).

8.6.4.42 Tx Buffer Request Pending (address = h10CC) [reset = h00000000]

Figure 88. Tx Buffer Request Pending Register

31	30	29	28	27	26	25	24
TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP22	TRP24
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
R	R	R	R	R	R	R	R

Table 65. Tx Buffer Request Pending Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRP31 to TRP0	R	0	Transmission Request Pending Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF • after successful transmission together with the corresponding TXBTO bit • when the transmission has not yet been started at the point of cancellation • when the transmission has been aborted due to lost arbitration • when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0 - No transmission request pending 1- Transmission request pending Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding TXBRP bit is reset.

8.6.4.43 Tx Buffer Add Request (address = h10D0) [reset = h00000000]

Figure 89. Tx Buffer Add Request Register

31	30	29	28	27	26	25	24
AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
AR14	AR14	AR13	AR12	AR11	AR10	AR9	AR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 66. Tx Buffer Add Request Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AR31 to AR0	R/W	0	Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0 - No transmission request added 1 - Transmission requested added Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored.

8.6.4.43.1 Tx Buffer Cancellation Request (address = h10D4 [reset = h00000000]

Figure 90. Tx Buffer Cancellation Request Register

31	30	29	28	27	26	25	24
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 67. Tx Buffer Cancellation Request Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CR31 to CR0	R/W	0	Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0 - No cancellation pending 1 - Cancellation pending

8.6.4.43.2 Tx Buffer Add Request Transmission Occurred (address = h10D8) [reset = h00000000]

Figure 91. Tx Buffer Add Request Transmission Occurred Register

31	30	29	28	27	26	25	24
TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
R	R	R	R	R	R	R	R

Table 68. Tx Buffer Add Request Transmission Occurred Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO31 to TO0	R	0	Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a ‘1’ to the corresponding bit of register TXBAR. 0 - No transmission occurred 1 - Transmission occurred

8.6.4.43.3 Tx Buffer Cancellation Finished (address = h10DC) [reset = h00000000]

Figure 92. Tx Buffer Cancellation Finished Register

31	30	29	28	27	26	25	24
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
R	R	R	R	R	R	R	R
23	22	21	20	19	18	17	16
CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
R	R	R	R	R	R	R	R

Table 69. Tx Buffer Cancellation Finished Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CF31 to CF0	R	0	Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a ‘1’ to the corresponding bit of register TXBAR. 0 - No transmit buffer cancellation 1 - Transmit buffer cancellation finished

8.6.4.43.4 Tx Buffer Transmission Interrupt Enable (address = h10E0) [reset = h00000000]

Figure 93. Tx Buffer Transmission Interrupt Enable Register

31	30	29	28	27	26	25	24
TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 70. Tx Buffer Transmission Interrupt Enable Field Descriptions

Bit	Field	Type	Reset	Description
	TIE31 to TIE0	R/W	0	Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 - Transmission interrupt disabled 1 - Transmission interrupt enable

8.6.4.43.5 Tx Buffer Cancellation Finished Interrupt Enable (address = h10E4) [reset = h00000000]

Figure 94. Tx Buffer Cancellation Finished Interrupt Enable Register

31	30	29	28	27	26	25	24
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 71. Tx Buffer Cancellation Finished Interrupt Enable Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CFIE31 to CFIE0	RW	0	Bit 31:0 CFIE[31:0]: Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 - Cancellation finished interrupt disabled 1 - Cancellation finished interrupt enabled

8.6.4.43.6 Reserved (address = h10E8) [reset = h00000000]

Figure 95. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 72. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

8.6.4.43.7 Reserved (address = h10EC) [reset = h00000000]

Figure 96. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 73. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

8.6.4.43.8 Tx Event FIFO Configuration (address = h10F0) [reset = h00000000]

The MRAM and start address for this register, EFSA, has special consideration.

- The start address must be word aligned (32-bit) in the MRAM. The 2 least significant bits are ignored on a write to ensure this behavior.
- When entering the MRAM start address, the 0x8000 prefix is NOT necessary. For example, if the desired start address is 0x8634, then bits SA[15:0] will be 0x0634.

Figure 97. Tx Event FIFO Configuration Register

31	30	29	28	27	26	25	24
RSVD		EFWM[5:0]					
R		RP					
23	22	21	20	19	18	17	16
RSVD		EFS[5:0]					
R		RP					
15	14	13	12	11	10	9	8
EFSA[15:8]							
RP							
7	6	5	4	3	2	1	0
EFSA[7:0]							
RP							

Table 74. Tx Event FIFO Configuration Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RSVD	R	0x0	Reserved
29:24	EFWM[5:0]	RP	0x0	Event FIFO Watermark 0 - Watermark interrupt disabled 1-32 - Level for Tx Event FIFO watermark interrupt (IR.TEFW) >32 - Watermark interrupt disabled
23:22	RSVD	R	0x0	Reserved
21:16	EFS[5:0]	RP	0x0	Event FIFO Size 0 - Tx Event FIFO disabled 1-32 - Number of Tx Event FIFO elements >32 - Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS - 1
15:0	EFSA[15:0]	RP	0x0	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM

8.6.4.43.9 Tx Event FIFO Status (address = h10F4) [reset = h00000000]

Figure 98. Tx Event FIFO Status Register

31	30	29	28	27	26	25	24
RSVD						TEFL	EFF
R						R	R
23	22	21	20	19	18	17	16
RSVD			EFPI[4:0]				
R			R				
15	14	13	12	11	10	9	8
RSVD			REFGI[4:0]				
R			R				
7	6	5	4	3	2	1	0
RSVD		EFFL[5:0]					
R		R					

Table 75. Tx Event FIFO Status Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RSVD	R	0x0	Reserved
25	TEFL	R	0	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0 - No Tx Event FIFO element lost 1 - Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	EFF	R	0	Event FIFO Full 0 - Tx Event FIFO not full 1 - Tx Event FIFO full
23:21	RSVD	R	0x0	Reserved
20:16	EFPI[4:0]	R	0x0	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31.
15:13	RSVD	R	0x0	Reserved
12:8	REFGI[4:0]	R	0x0	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31.
7:6	RSVD	R	0x0	Reserved
5:0	EFFL[5:0]	R	0x0	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32

8.6.4.43.10 Tx Event FIFO Acknowledge (address = h10F8) [reset = h00000000]

Figure 99. Tx Event FIFO Acknowledge Register

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD			EFAI[4:0]				
R			R/W				

Table 76. Tx Event FIFO Acknowledge Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RSVD	R	0x0	Reserved
23:16	RSVD	R	0x0	Reserved
15:18	RSVD	R	0x0	Reserved
7:5	RSVD	R	0x0	Reserved
4:0	EFAI[4:0]	E/W	0x0	Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL.

8.6.4.43.11 Reserved (address = h10FC) [reset = h00000000]

Figure 100. Reserved

31	30	29	28	27	26	25	24
RSVD							
R							
23	22	21	20	19	18	17	16
RSVD							
R							
15	14	13	12	11	10	9	8
RSVD							
R							
7	6	5	4	3	2	1	0
RSVD							
R							

Table 77. Reserved Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RSVD	R	0	Reserved

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Design Consideration

9.1.1 Crystal and Clock Input Requirements

Selecting the crystal or clock input depends upon system implementation. To support 2 and 5 Mbps CAN FD the clock in or crystal needs to have 0.5% frequency accuracy. The minimum value of 20 MHz is needed to support CAN FD with a rate of 2 Mbps. The recommended value for CLKIN or crystal is 40 MHz to meet CAN FD rates up to 5 Mbps data rates in order to support higher data throughout. If a crystal is used see the manufacturer's documentation on proper biasing. When using a V_{IO} of 1.8 V an external clock of the same voltage should be used and not a crystal.

注

The TCAN4551-Q1 was evaluated with the NX2016SA 20MHz and 40MHz crystals

9.1.2 Bus Loading, Length and Number of Nodes

A typical CAN application can have a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as this transceiver family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2016 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA200.

A CAN system design is a series of tradeoffs. In ISO 11898-2:2016 the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN4551-Q1 is specified to meet the 1.5 V requirement with a across this load range and is specified to meet 1.4 V differential output at 45 Ω bus load. The differential input resistance of this family of transceiver is a minimum of 30kΩ. If 167 of these transceivers are in parallel on a bus, this is equivalent to an 180 Ω differential load in parallel with the 60 Ω from termination gives a total bus load of 45 Ω. Therefore, this family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2 V minimum differential input voltage requirement at each receiving node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond the original ISO 11898-2:2016 standard of 40 m by careful system design and data rate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

9.1.3 CAN Termination

The standard CAN bus interconnection to be a single twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (ZO).

Application Design Consideration (continued)

9.1.3.1 Termination

Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

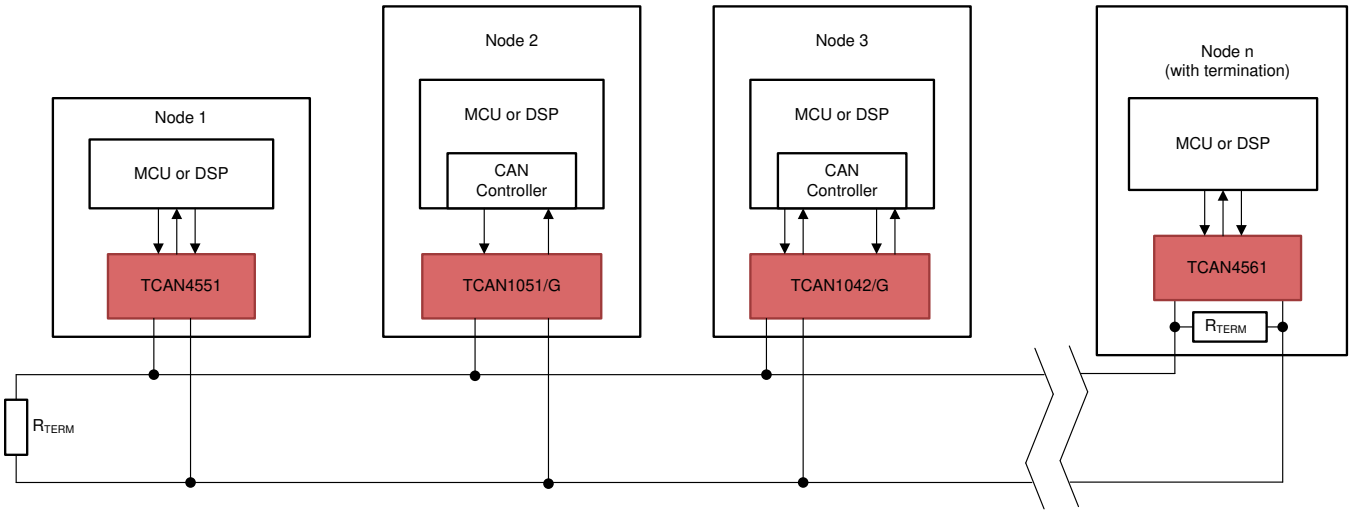


図 101. Typical CAN Bus

Termination may be a single 120 Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” may be used, see 図 102. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

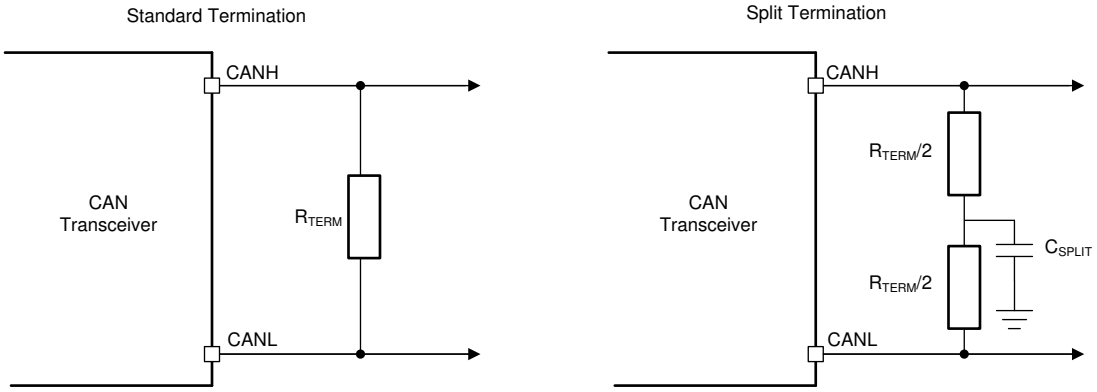


図 102. CAN Bus Termination Concepts

9.1.3.2 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 図 103 for the state diagram on how the TCAN4551-Q1 performs automatic biasing. Figure 図 104 provides the bus biasing based upon the mode of operation.

Application Design Consideration (continued)

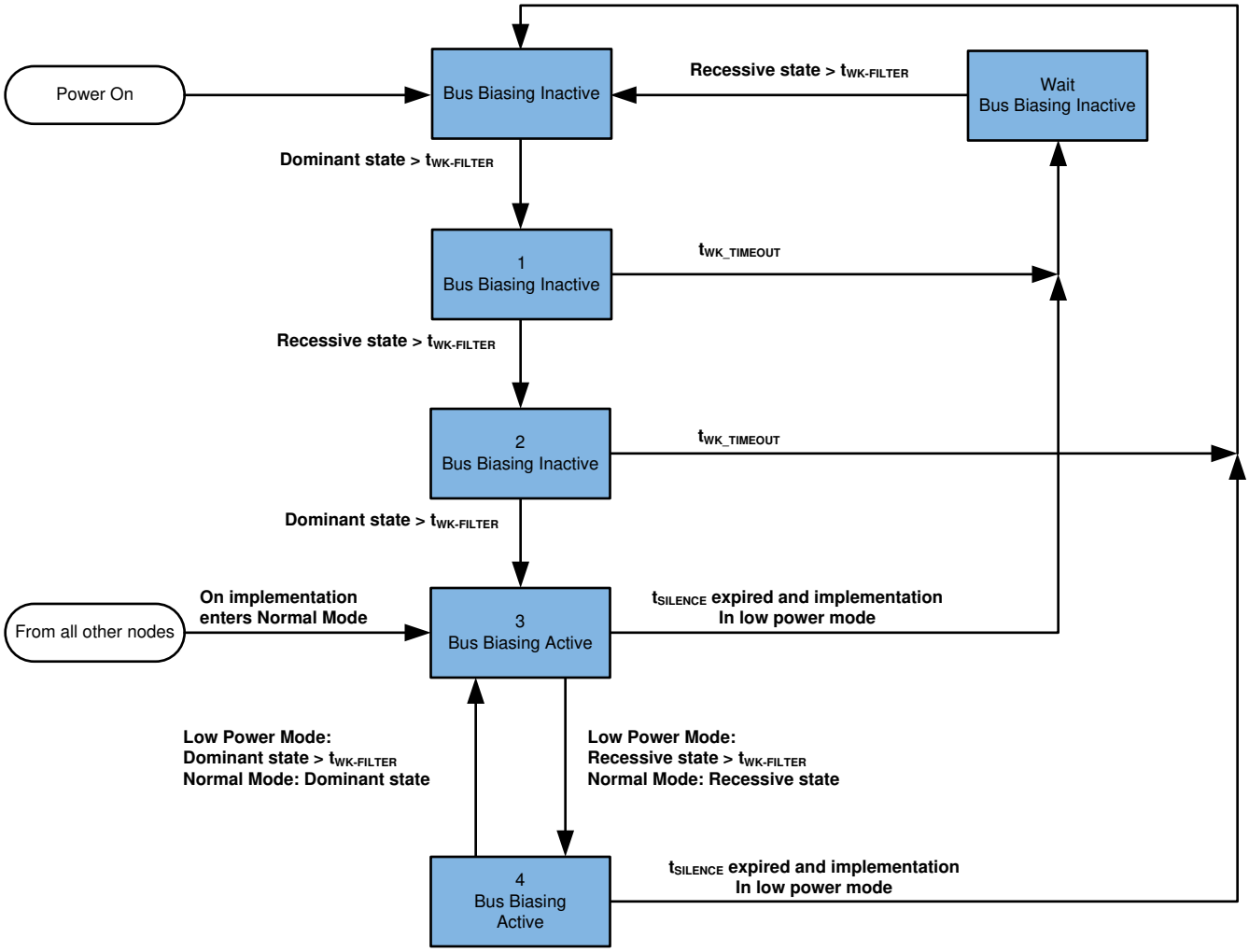


図 103. Automatic bus biasing state diagram

Application Design Consideration (continued)

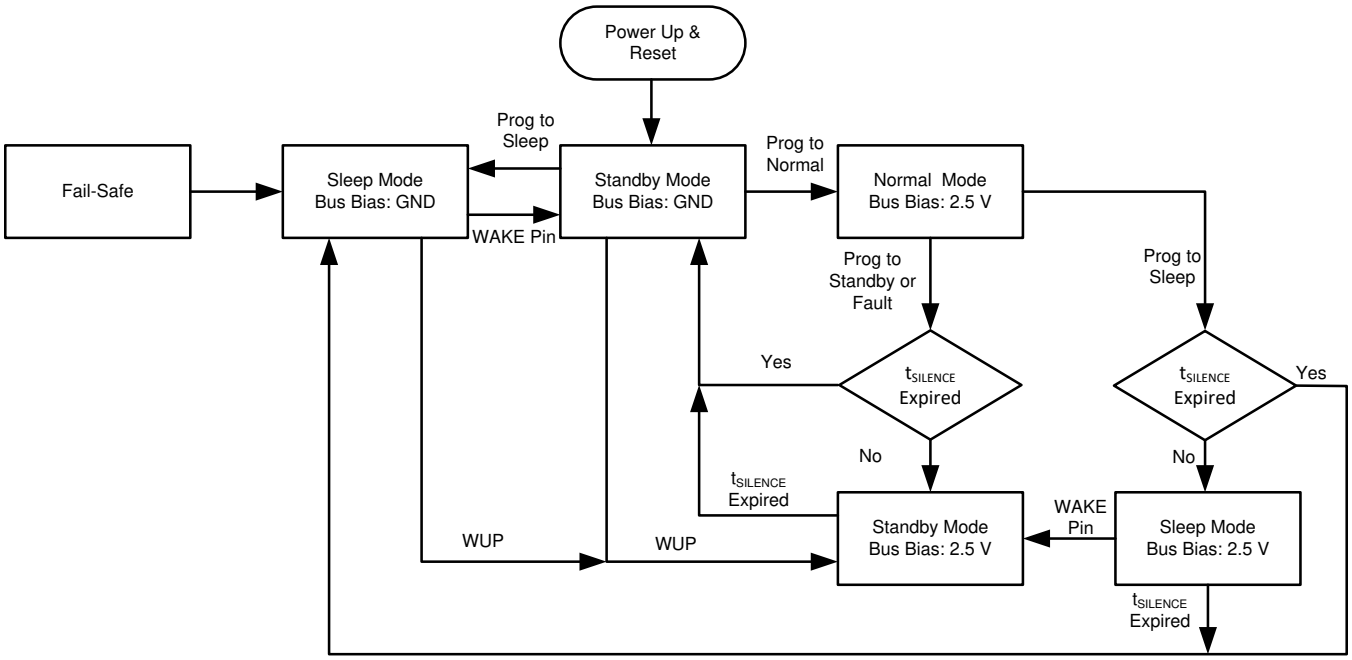


図 104. Bus Biasing Based on Modes of Operation

9.2 Typical Application

The TCAN4551-Q1 is typically used in applications with a host microprocessor or FPGA that does not include the link layer portion of the CAN protocol. Below is a typical application configuration for 3.3 V microprocessor applications.

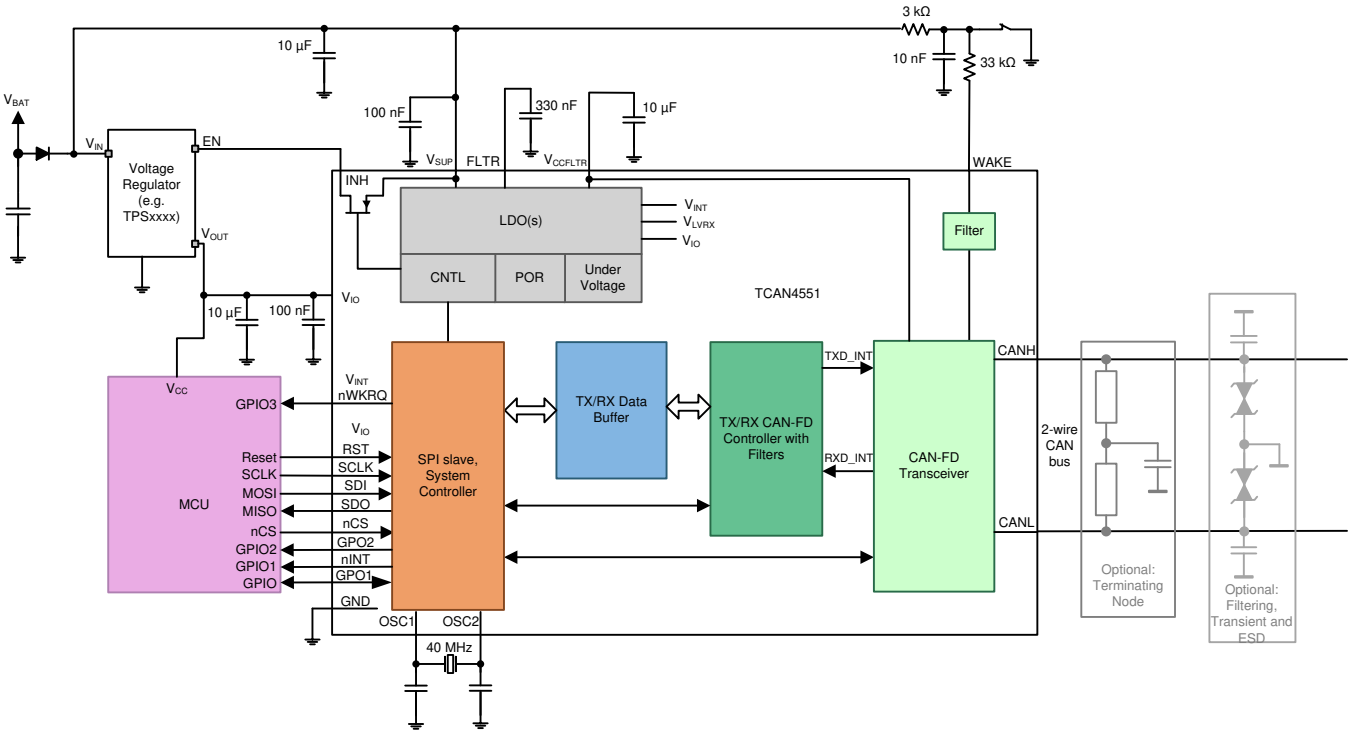


図 105. Typical CAN Applications for TCAN4551-Q1 for 3.3 V µC and Crystal

Note: Add decoupling capacitors as needed.

Typical Application (continued)

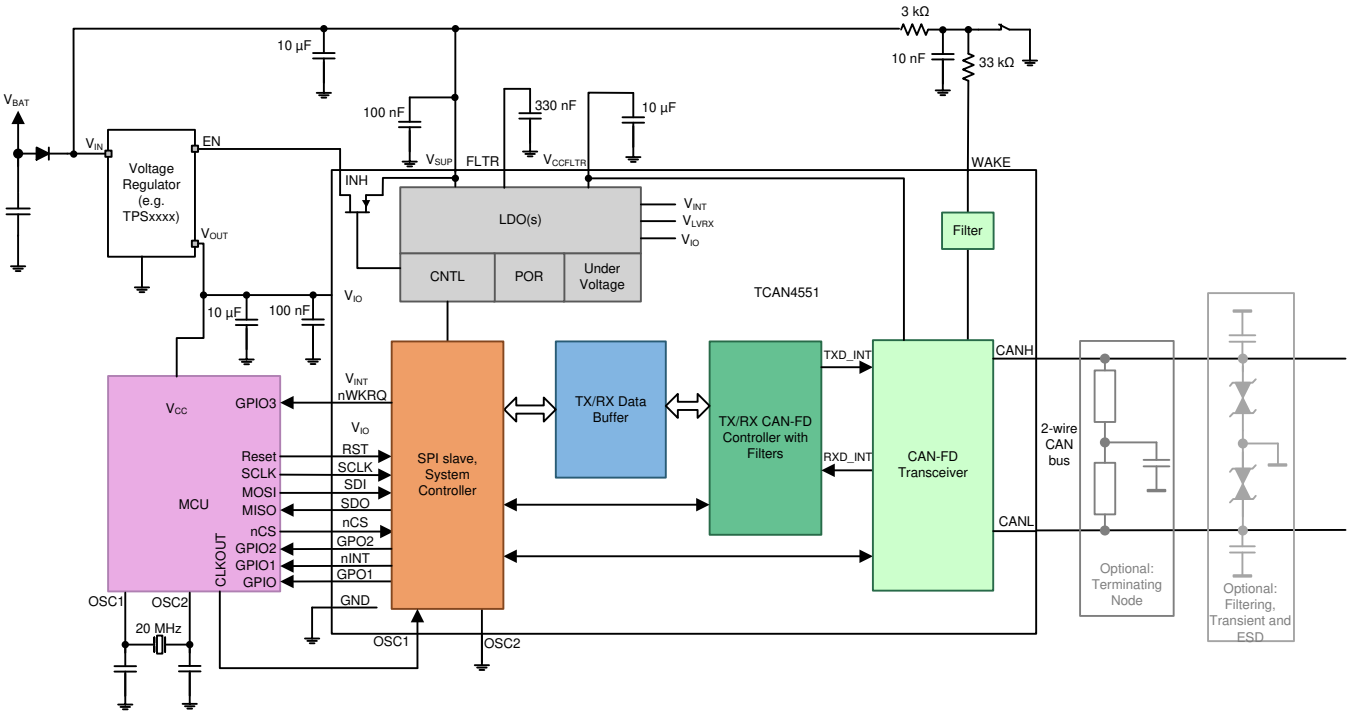


図 106. Typical CAN Applications for TCAN4551-Q1 for 3.3 V µC; Clock from MCU

9.2.1 Detailed Requirements

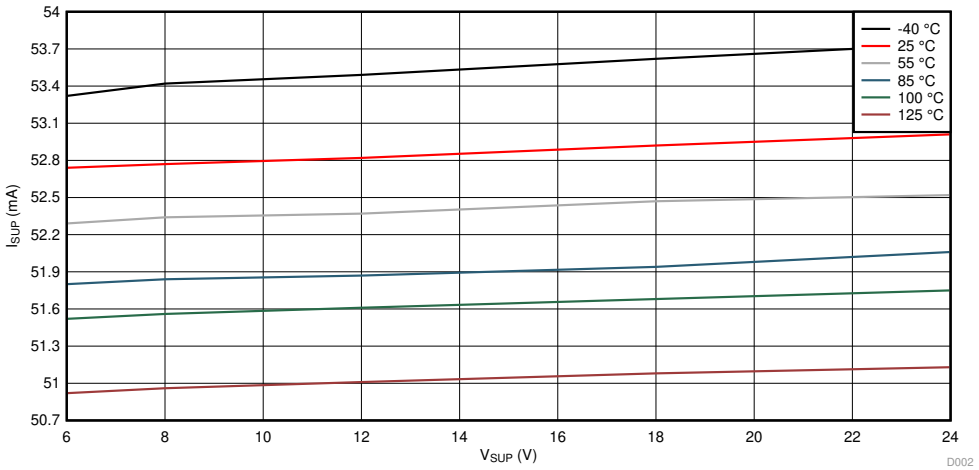
The TCAN4551-Q1 works with 1.8 V, 3.3 V and 5 V microprocessors when using the V_{IO} pin from the microprocessor voltage regulator. The bus termination is shown for illustrative purposes.

9.2.2 Detailed Design Procedures

The TCAN4551-Q1 is designed to work in application using the ISO 11898 standard supporting bus loads from 50 Ω to 65 Ω. As the TCAN4551-Q1 supports CAN FD data rates up to 8 Mbps the recommendation is to use a 40 MHz crystal and to keep trace lengths matched and as short as feasible between the processor and device. As stub length is defined in the standard it is recommended to design the system according to these.

Typical Application (continued)

9.2.3 Application Curves



CAN Bus State = Dominant

CAN Bus Load = 60 Ω

図 107. I_{SUP} Across V_{SUP} and Temperature

10 Power Supply Recommendations

The TCAN4551-Q1 is designed to operate off of the battery V_{bat}. It has internal regulators to reduce the voltage to acceptable low power levels supporting the CAN FD controller, CAN transceiver and low voltage CAN receiver. In order to support a wide range of microprocessors the SPI and GPO are powered off of the V_{IO} pin which supports levels from 1.8 V to 5.5 V. Bulk capacitance, should be placed on the V_{SUP} and the V_{IO} voltage rails where system requirements are met. It is recommended that a capacitance of a 100 nF is placed near the TCAN4551-Q1 V_{SUP} and the V_{IO} supply terminals. The FLTR terminal requires a minimum of 300 nF capacitance to ground to regulate the internal digital power rail. V_{CCFLTR} needs a minimum capacitance to ground of 10 µF at the terminal.

注

- The capacitance values selected should take into consideration the degradation over time such that the values do not fall below the minimum values shown
- Above is a minimum amount of capacitance but due to system considerations more may be needed

11 Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

11.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device itself. Transient voltage suppression (TVS) device can be added for extra protection, shown as D1. The production solution can be either a bi-directional TVS diode or a varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C10 and C11. A series common mode choke (CMC) is placed on the CANH and CANL lines between TCAN4551-Q1 and connector J1.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

注

High-frequency currents follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C3, C4 and C5 on the FLTR, V_{IO},V_{CCFLTR}, pins and C6 and C7 on the V_{SUP} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C9. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination.
- As terminal 8 (nINT) and 9 (GPO2) are open drain an external resistor to V_{IO} is required. These can have a value between 2 kΩ and 10 kΩ.
- Terminal 12 (WAKE) is a bi-directional triggered wake up input that is usually connected to an external switch. It should be configured as shown with a 10 nF (C8) to GND where R2 is 33 kΩ and R3 is 3 kΩ.
- Terminal 15 (INH) can be left floating if not used but a 100 kΩ pull-down resistor can be used to discharge the INH to a sufficient level when the INH output is high-Z.

11.2 Layout Example

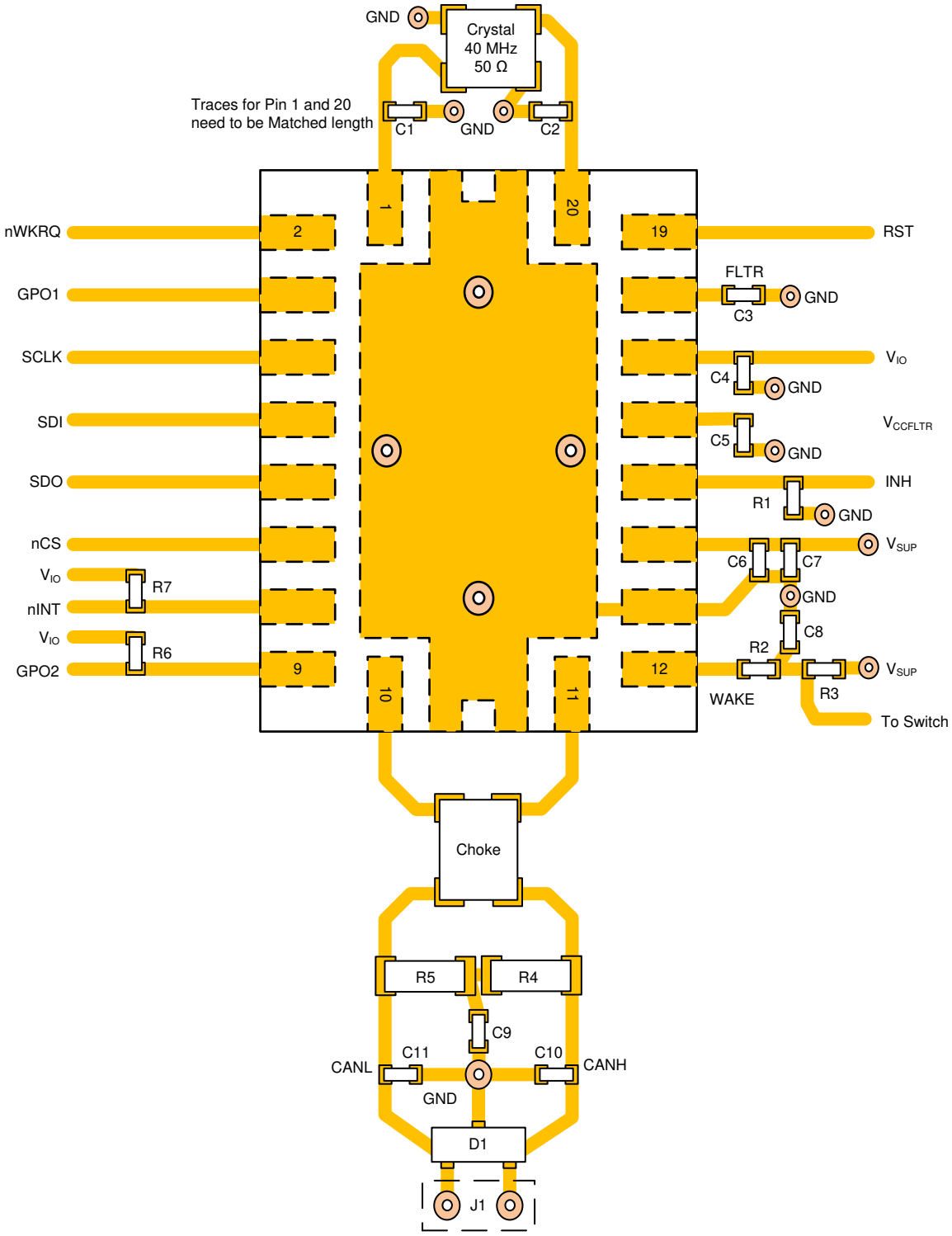


図 108. Example Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

12.1.1.1 CAN トランシーバの物理層の標準

- ISO 11898-2:2016：低消費電力モードを持つ高速媒体アクセス・ユニット
- ISO 8802-3: CSMA/CD - ISO11898-2から衝突検出用に参照
- CAN FD 1.0の仕様と資料
- Bosch、『CANのビット・タイミングの構成』、第6回国際CAN会議(ICC)、1999年からの資料。この資料の多くは、このシステム仕様にコピーされている、DCAN IP CANコントローラ仕様に繰り返されています。
- SAE J2284-2: 250kbpsの車載用アプリケーション向けの高速CAN (HSC)
- SAE J2284-3: 500kbpsの車載用アプリケーション向けの高速CAN (HSC)
- Bosch M_CAN コントローラ・エリア・ネットワーク・リビジョン 3.2.1.1 (2016/3/24)

12.1.1.2 EMC要件

- SAE J2962-2：CAN トランシーバの US3 要件
- CAN、LIN、FR V1.3 の HW 要件

12.1.1.3 準拠テストの要件

- HS_TRX_Test_Spec_V_1_0: 高速物理レイヤ用のGIFT/ICT CANテストの要件

12.1.1.4 コミュニティ・リソース

- 『A Comprehensible Guide to Controller Area Network』(英語)、Wilfried Voss、Copperhill Media Corporation
- 『CAN System Engineering: From Theory to Practical Applications』(英語)、第 2 版、2013 年、Dr. Wolfhard Lawrenz、Springer

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

E2E is a trademark of Texas Instruments.
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12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN4551RGYRQ1	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TCAN 4551Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

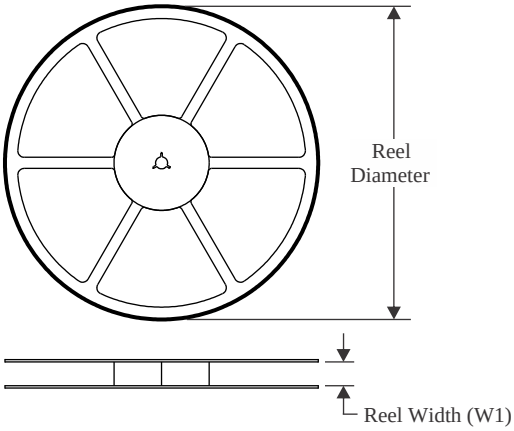
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

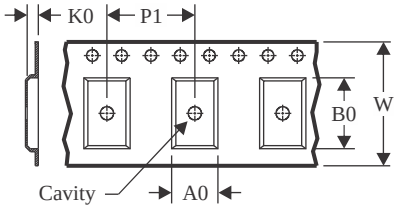
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

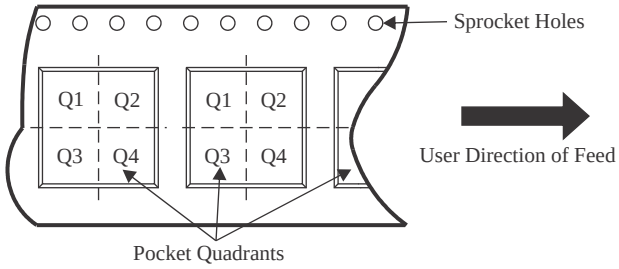


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

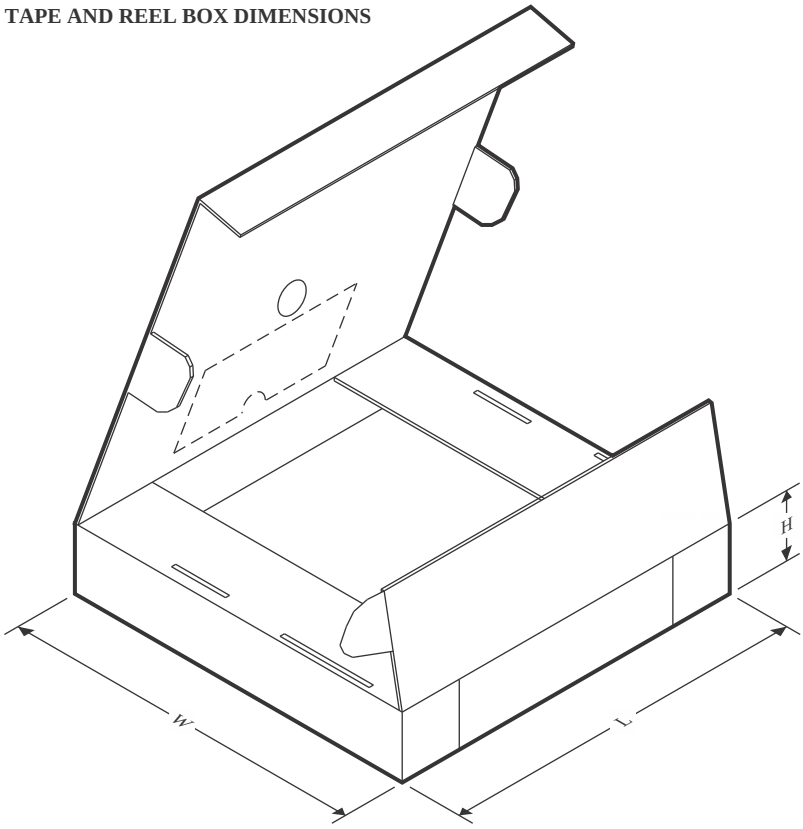
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN4551RGYRQ1	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN4551RGYRQ1	VQFN	RGY	20	3000	367.0	367.0	35.0

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