

# THS6301 G.Fast DSLライン・ドライバ・アンプ、帯域幅および電力スケーリング機能搭載

## 1 特長

- G.Fast 106MHz、212MHz DSLアプリケーションを実現
- レガシーVDSLおよびADSL2+アプリケーションのサポート
- G.Fastおよびレガシー・アプリケーションで高いMTPR (ライン電力 = 8dBm)
  - ADSL2+ = 69dB
  - VDSL-17a = 73dB
  - VDSL-30a = 69dB
  - G.Fast 106MHz = 62dB
  - G.Fast 212MHz = 55dB
- 各種のプロファイルに向けた複数の電力モード
- 外付けの抵抗によりバイアス電流を設定可能
- 低消費電力のライン終端モード: 10.2mA
- パワーダウン・モード
- 12Vテクノロジーにより大電力の出力をサポート

## 2 アプリケーション

- G.FastおよびレガシーDSLのライン・ドライバ
- 汎用の広帯域ライン・ドライバ
- PLCドライバ
- DAC出力アンプ

## 3 概要

THS6301はシングル・チャンネル、電流帰還アーキテクチャの差動ライン・ドライバで、G.Fastおよび各種のデジタル信号サブスクライバ・ライン(DSL)のホーム・ゲートウェイ・システムを実現します。

このデバイスは、ネイティブの離散マルチトーン変調(DMT)信号を使用する、106MHzおよび212MHzのG.Fastデジタル・サブスクライバ・ラインのプロファイルを実現します。THS6301は高い直線性で動作し、8dBmのライン電力で最高212MHzに対応します。

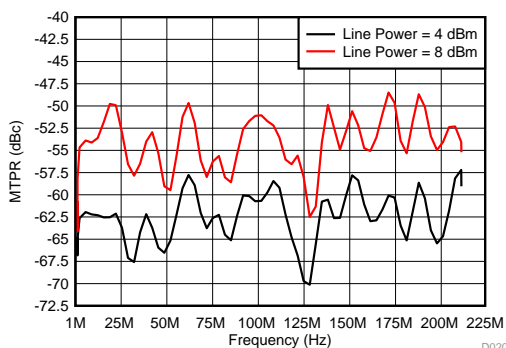
このデバイスは独自のアーキテクチャにより、静止電流を最小限に抑え、同時に非常に高い線形性を実現しています。アンプのバイアス設定は内部で固定されており、ライン駆動モードでアンプの最大能力が必要ない場合に電力を削減できます。柔軟性や省電力をさらに強化するため、デバイスのピンの1つに接続した単一の外付けバイアス抵抗により、全体の静止電流を変更可能です。また、このデバイスには2つのライン終端モードがあり、非常に低い消費電力でインピーダンスのマッチングを維持します。

### 製品情報<sup>(1)</sup>

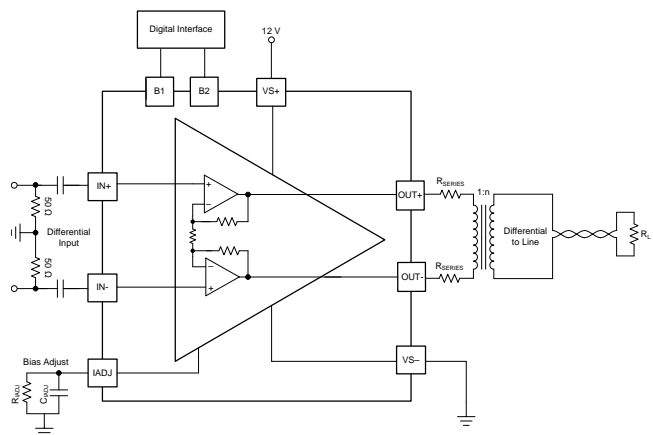
型番	パッケージ	本体サイズ(公称)
THS6301	VQFN (16)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

MTPR G.Fast 212MHz  
(Bias 10、PAR = 15dB、64中1の欠損トーン)



マルチトーン電力比(MTPR)プロファイル  
(G.Fast、212MHz、8dBm)



## 目次

<b>1</b>	特長 .....	1	8.4	Device Functional Modes .....	20
<b>2</b>	アプリケーション .....	1	8.5	Programming .....	20
<b>3</b>	概要 .....	1	<b>9</b>	<b>Application and Implementation</b> .....	21
<b>4</b>	改訂履歴 .....	2	9.1	Application Information .....	21
<b>5</b>	概要 (続き) .....	3	9.2	Typical Application .....	21
<b>6</b>	<b>Pin Configuration and Functions</b> .....	4	<b>10</b>	<b>Power Supply Recommendations</b> .....	24
<b>7</b>	<b>Specifications</b> .....	5	<b>11</b>	<b>Layout</b> .....	24
7.1	Absolute Maximum Ratings .....	5	11.1	Layout Guidelines .....	24
7.2	ESD Ratings .....	5	11.2	Layout Example .....	26
7.3	Recommended Operating Conditions .....	5	<b>12</b>	デバイスおよびドキュメントのサポート .....	27
7.4	Thermal Information .....	5	12.1	ドキュメントのサポート .....	27
7.5	Electrical Characteristics .....	6	12.2	ドキュメントの更新通知を受け取る方法 .....	27
7.6	Switching Characteristics .....	10	12.3	コミュニティ・リソース .....	27
7.7	Typical Characteristics .....	11	12.4	商標 .....	27
<b>8</b>	<b>Detailed Description</b> .....	18	12.5	静電気放電に関する注意事項 .....	27
8.1	Overview .....	18	12.6	Glossary .....	27
8.2	Functional Block Diagram .....	18	<b>13</b>	メカニカル、パッケージ、および注文情報 .....	27
8.3	Feature Description .....	19			

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### 2018年4月発行のものから更新

**Page**

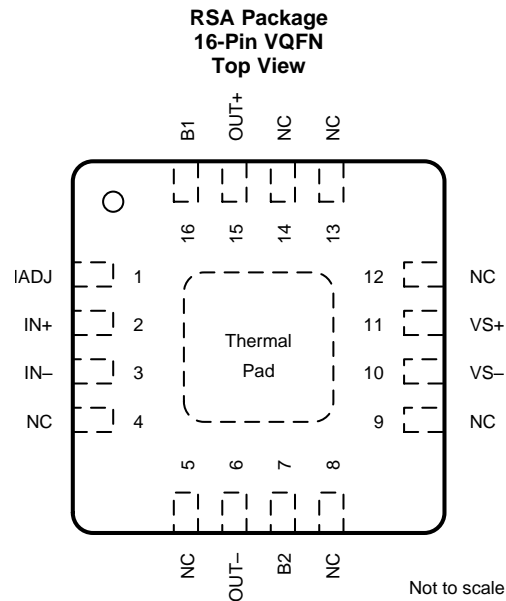
•	量産にリリース .....	1
---	---------------	---

## 5 概要 (続き)

さらに、このデバイスは固定ゲインの差動アンプとしても使用でき、差動アプリケーションの要求に応じて帯域幅および電力をスケールリングできます。

このデバイスは、4mm×4mm、16ピンのVQFNパッケージで供給されます。

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
B1	16	I	Most significant bit (MSB), logic level referenced to VS–
B2	7	I	Least significant bit (LSB), logic level referenced to VS–
IADJ	1	—	Bias current reference pin
IN–	3	I	Negative input
IN+	2	I	Positive input
NC	4	—	No internal connection to device (VS– recommended)
NC	5, 8, 9, 12, 13, 14	—	Not connected
OUT–	6	O	Negative output
OUT+	15	O	Positive output
VS–	10	—	Negative supply voltage connection
VS+	11	—	Positive supply voltage connection
Thermal pad		—	The thermal pad is connected to pin 4 via a downbond connection. The pad must be at the same potential as pin 4.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage <sup>(2)</sup>	VS pin to GND (all modes)		13.2	V
Digital inputs to GND	B1, B2	-0.3	5.5	V
Analog inputs to GND	VIN+, VIN-	2	10	V
Differential analog inputs	(VIN+ – VIN-)	-6	6	V
Continuous power dissipation		See <a href="#">Thermal Information</a>		
T <sub>stg</sub>	Storage temperature	-65	150	°C
T <sub>J</sub>	Junction temperature		150	°C

- Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Supply bypass capacitor type, value and location relative to the device are critical to prevent damage to the device when the device is turned on. See [Power Supply Recommendations](#).

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins <sup>(1)</sup>	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VS	Supply voltage	11.4	12	12.6	V
		±5.7	±6	±6.3	
T <sub>A</sub>	Ambient temperature	-40		85	°C
T <sub>J</sub>	Junction temperature	-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		THS6301	UNIT
		RSA (VQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	39	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	38.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	18	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.7	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $100\text{-}\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , drive mode 5 (B1B2 = 01, G.Fast mid power)<sup>(1)</sup> and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(2)</sup>
<b>AC PERFORMANCE</b>							
SSBW	Small-signal bandwidth	$V_{\text{OUT}} = 1\ V_{\text{PP}}$ , drive mode 1 (0Z, ADSL2+)		500		MHz	C
		$V_{\text{OUT}} = 1\ V_{\text{PP}}$ , drive mode 2 (Z1, VDSL low power)		565			C
		$V_{\text{OUT}} = 1\ V_{\text{PP}}$ , drive mode 3 (11, G.Fast low power and VDSL mid power)		635			C
		$V_{\text{OUT}} = 1\ V_{\text{PP}}$ , drive mode 4 (1Z, VDSL high power)		540			C
		$V_{\text{OUT}} = 1\ V_{\text{PP}}$ , drive mode 5 (01, G.Fast mid power)		670			C
		$V_{\text{OUT}} = 1\ V_{\text{PP}}$ , drive mode 6 (10, G.Fast high power)		618			C
LSBW	Large-signal bandwidth	$V_{\text{OUT}} = 15\ V_{\text{PP}}$ , drive mode 1 (0Z, ADSL2+)		160		MHz	C
		$V_{\text{OUT}} = 15\ V_{\text{PP}}$ , drive mode 2 (Z1, VDSL low power)		200			C
		$V_{\text{OUT}} = 15\ V_{\text{PP}}$ , drive mode 3 (11, G.Fast low power and VDSL mid power)		260			C
		$V_{\text{OUT}} = 15\ V_{\text{PP}}$ , drive mode 4 (1Z, VDSL high power)		270			C
		$V_{\text{OUT}} = 15\ V_{\text{PP}}$ , drive mode 5 (01, G.Fast mid power)		275			C
		$V_{\text{OUT}} = 15\ V_{\text{PP}}$ , drive mode 6 (10, G.Fast high power)		300			C
SR	Slew rate down	Drive mode 1 (0Z), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		3200		V/ $\mu\text{s}$	C
		Drive mode 2 (Z1), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		4000			C
		Drive mode 3 (11), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		6400			C
		Drive mode 4 (1Z), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		7100			C
		Drive mode 5 (01), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		8200			C
		Drive mode 6 (10), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		10500			C
	Slew rate up	Drive mode 1 (0Z), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		2500		V/ $\mu\text{s}$	C
		Drive mode 2 (Z1), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		3200			C
		Drive mode 3 (11), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		4400			C
		Drive mode 4 (1Z), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		5400			C
		Drive mode 5 (01), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		6500			C
		Drive mode 6 (10), 10%-90% $15\text{-}V_{\text{PP}}$ pulse		8000			C
$e_n$	Input-referred voltage noise	$f > 1\ \text{MHz}$ , drive mode 1 (0Z)		4.3		nV/ $\sqrt{\text{Hz}}$	C
		$f > 1\ \text{MHz}$ , drive mode 2 (Z1)		3.9			C
		$f > 1\ \text{MHz}$ , drive mode 3 (11)		3.9			C
		$f > 1\ \text{MHz}$ , drive mode 4 (1Z)		3.9			C
		$f > 1\ \text{MHz}$ , drive mode 5 (01)		3.7			C
		$f > 1\ \text{MHz}$ , drive mode 6 (10)		3.5			C
Noise floor, line termination mode		Line-termination modes, referred to $R_{\text{SERIES}}$		-154		dBm/Hz	C
		Power-down mode, referred to $R_{\text{SERIES}}$		-166			C
		Line-termination mode 00, output referred ( $f > 1\ \text{MHz}$ )		5.6		nV/ $\sqrt{\text{Hz}}$	C
		Line-termination mode Z0, output referred ( $f > 1\ \text{MHz}$ )		6			C
		Power-down mode, output referred ( $f > 1\ \text{MHz}$ )		1.6			C

(1) See Table 1 for the different Bias Modes of the device

(2) Test levels (all values set by characterization and simulation): (A) 100% tested at  $T_A \approx 25^\circ\text{C}$ . (B) Not tested in production; limits set by characterization and simulation. (C) Typical value only for information. (D) Simulated value only for information

**Electrical Characteristics (continued)**

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $100\text{-}\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , drive mode 5 (B1B2 = 01, G.Fast mid power)<sup>(1)</sup> and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(2)</sup>
ADSL2+ MTPR <sup>(3)</sup>		Line power = 8 dBm, $f \leq 552\ \text{kHz}$ , PAR = 15 dB		67		dB	C
		Line power = 8 dBm, $f \leq 1.104\ \text{MHz}$ , PAR = 15 dB		69			C
		Line power = 8 dBm, $f \leq 2.208\ \text{MHz}$ , PAR = 15 dB		67			C
VDSL2-17a MTPR <sup>(3)</sup>		Line power = 8 dBm, $f \leq 14\ \text{MHz}$ , PAR = 15 dB, bias = 11		73		dB	C
		Line power = 8 dBm, $f \leq 17.6\ \text{MHz}$ , PAR = 15 dB, bias = 11		71.5			C
VDSL2-30a MTPR <sup>(3)</sup>		Line power = 8 dBm, $f \leq 30\ \text{MHz}$ , PAR = 15 dB, bias = 11		69		dB	C
VDSL2-35b MTPR <sup>(3)</sup>		Line power = 8 dBm, $f \leq 35\ \text{MHz}$ , PAR = 15 dB, bias = 11		66		dB	C
G.Fast 106-MHz MTPR <sup>(3)</sup>		Line power = 4 dBm, $f \leq 106\ \text{MHz}$ , PAR = 15 dB, bias 01		68		dB	C
		Line power = 8 dBm, $f \leq 106\ \text{MHz}$ , PAR = 15 dB, bias 10		62			C
		Line-termination mode, line power = 8 dBm, PAR = 15 dB		60		dB	D
G.Fast 212-MHz MTPR <sup>(3)</sup>		Line power = 4 dBm, $f \leq 212\ \text{MHz}$ , PAR = 15 dB, bias 10		63		dB	C
		Line power = 8 dBm, $f \leq 212\ \text{MHz}$ , PAR = 15 dB, bias 10		55			C
		Line-termination mode, line power = 4 dBm, PAR = 15 dB		50			dB
Differential output impedance		Drive mode 6 (10, G.Fast high power), $f = 100\ \text{kHz}$		1.2		$\Omega$	D
		Drive mode 6 (10, G.Fast high power), $f = 50\ \text{MHz}$		1.7			D
		Drive mode 6 (10, G.Fast high power), $f = 106\ \text{MHz}$		2.8			D
		Drive mode 6 (10, G.Fast high power), $f = 212\ \text{MHz}$		5.3			D
		Power-down bias mode		2400			D
		Line-termination modes		1.3			D
<b>DC PERFORMANCE</b>							
$A_V$	Differential gain	At dc, no load, all modes	8.3	8.6	8.9	V/V	A
	Differential output offset		-100		100	mV	A
	Output swing	Differential, at dc, $200\text{-}\Omega$ load at amplifier output	18			$V_{PP}$	A
$R_{\text{IN-DIFF}}$	Differential input resistance		8	10	12	k $\Omega$	A
$R_{\text{IN-SE}}$	Single-ended input resistance		4	5	6	k $\Omega$	A

(3) ADSL2+, VDSL2-17a and VDSL2-30a profiles are specified with 1-in-4 missing tones; VDSL2-35b and G.Fast profiles are specified with 1-in-64 missing tones

**Electrical Characteristics (continued)**

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $100\text{-}\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , drive mode 5 (B1B2 = 01, G.Fast mid power)<sup>(1)</sup> and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(2)</sup>
	Linear output current	Drive mode 1 (0Z), sourcing, output offset < 20-mV deviation	40	75		mA	A
		Drive mode 1 (0Z), sinking, output offset < 20-mV deviation	40	70			A
		Drive mode 6 (10), sourcing, output offset < 20-mV deviation	80	160			A
		Drive mode 6 (10), sinking, output offset < 20-mV deviation	80	160			A
		High power termination mode (00), sourcing, output offset < 20-mV deviation	50	95			A
		High power termination mode (00), sinking, output offset < 20-mV deviation	50	90			A
		Low power termination mode (Z0), sourcing, output offset < 20-mV deviation	40	77			A
		Low power termination mode (Z0), sinking, output offset < 20-mV deviation	40	74			A
<b>COMMON MODE</b>							
	Input CM bias voltage		5.9	6	6.1	V	A
	Output CM bias voltage		5.9	6	6.1	V	A
<b>POWER SUPPLY</b>							
	Maximum supply voltage range	All modes			12.6	V	A
PSRR	Power-supply rejection ratio	f = dc	61			dB	A
$I_Q$	Quiescent current	Drive mode 1 (0Z, ADSL2+)	13	15.9	18.9	mA	A
		Drive mode 2 (Z1, VDSL low power)	16.7	20.1	24.3		A
		Drive mode 3 (11, G.Fast low power and VDSL mid power)	22.5	27.2	33.1		A
		Drive mode 4 (1Z, VDSL high power)	24	29.8	36.5		A
		Drive mode 5 (01, G.Fast mid power)	32.1	38.9	47.8		A
		Drive mode 6 (10, G.Fast high power)	36.7	45.3	56		A
		High power line termination mode (00)	13.6	16	18.9		A
		Low power line termination mode (Z0)	8.3	10.2	11.6		A
		Power-down mode		1.9	2.4		A



**Electrical Characteristics (continued)**

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $100\text{-}\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , drive mode 5 (B1B2 = 01, G.Fast mid power)<sup>(1)</sup> and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL <sup>(2)</sup>
Dynamic power consumption		Drive mode 1 (0Z, ADSL2+), line power = 8 dBm		220		mW	D
		Drive mode 2 (Z1, VDSL low power), line power = 8 dBm		280			D
		Drive mode 3 (11, G.Fast low power and VDSL mid power), line power = 8 dBm		310			D
		Drive mode 4 (1Z, VDSL high power), line power = 8 dBm		340			D
		Drive mode 5 (01, G.Fast mid power), line power = 4 dBm		480			D
		Drive mode 6 (10, G.Fast high power), line power = 8 dBm		590			D
		High power line termination mode (00), line power = 4 dBm		220			D
		Low power line termination mode (Z0), line power = 4 dBm		120			D
		Power-down mode		23			D

## 7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	Minimum logic high level	All digital pins, high	2.3			V
$V_{IL}$	Maximum logic low level	All digital pins, low			0.6	V
$V_{MID}$	Logic mid range	All digital pins, driven externally	1.2		1.6	V
$V_{Float}$	Logic self-bias voltage	All digital pins, floating	1.3	1.4	1.5	V
$I_{IH}$	Logic high-level leakage current	All digital pins, logic level = 3.6 V		110	135	$\mu$ A
$I_{IL}$	Logic low-level leakage current	All digital pins, logic level = ground	–85	–75		$\mu$ A
	Turn-on switching time	High power line termination mode (00) to drive mode 6 (10, G.Fast high power)		64		ns
		Low power line termination mode (Z0) to drive mode 6 (10, G.Fast high power)		50		
		Power down mode (ZZ) to Drive mode 6 (10, G.Fast high power)		60		
	Turn-off switching time	Drive mode 6 (10, G.Fast high power) to high power line termination mode (00)		76		ns
		Drive mode 6 (10, G.Fast high power) to low power line termination mode (Z0)		400		
		Drive mode 6 (10, G.Fast high power) to power-down mode (ZZ)		380		

### 7.7 Typical Characteristics

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_v$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

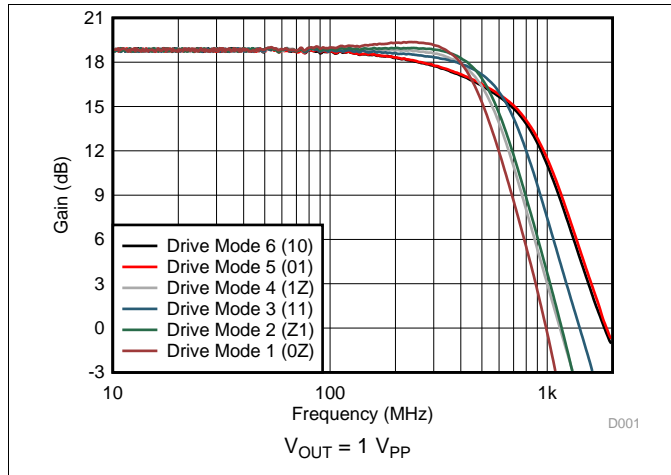


Figure 1. Small-Signal Bandwidth

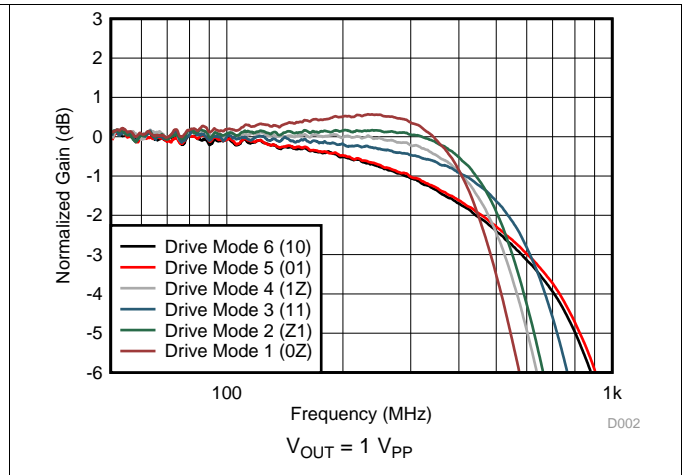


Figure 2. 3-dB Normalized Gain Small-Signal Bandwidth

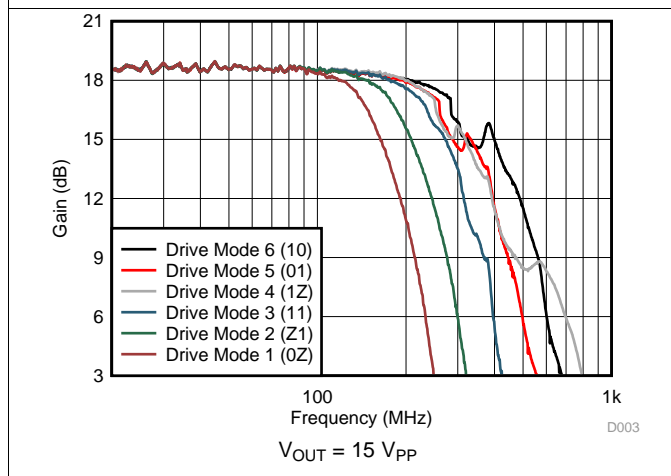


Figure 3. Large-Signal Bandwidth

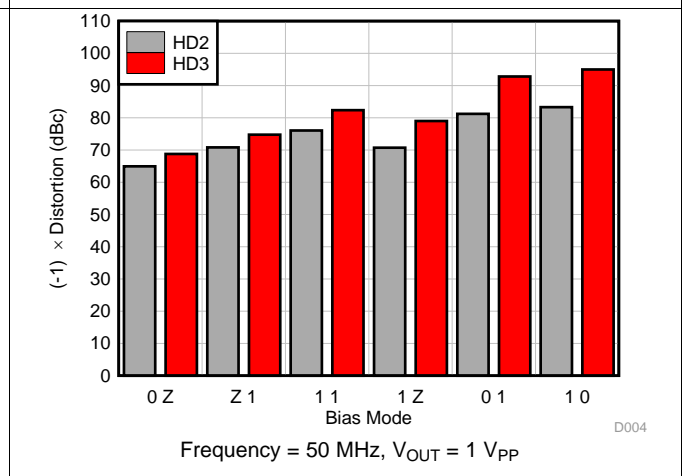


Figure 4. Bias Modes vs Distortion

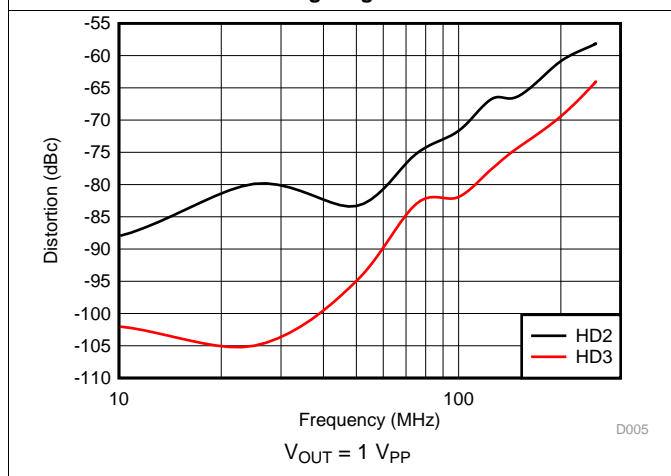


Figure 5. Distortion vs Frequency Drive Mode 6 (Bias 10)

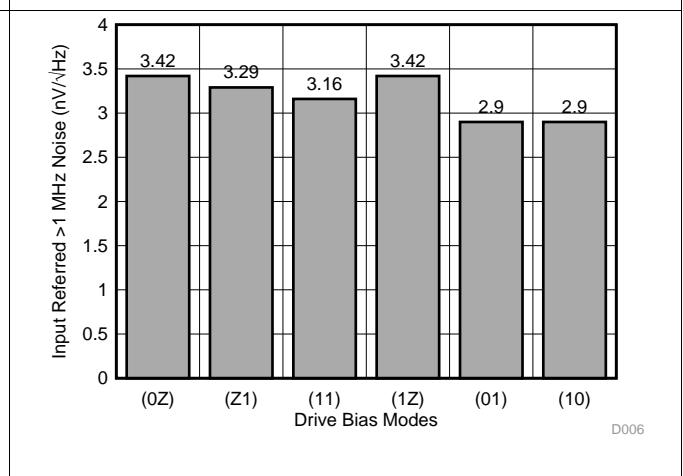
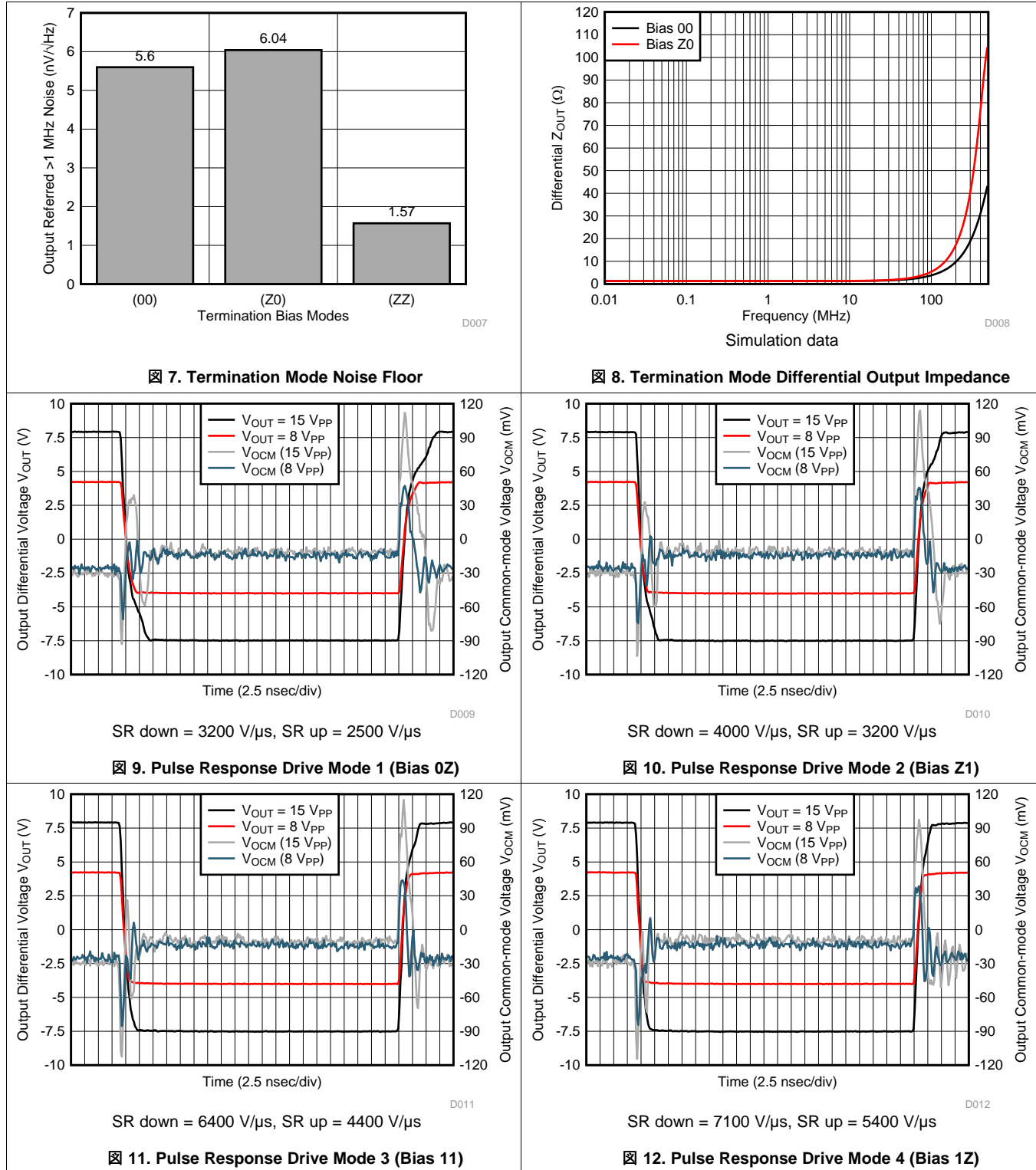


Figure 6. Input Voltage Noise

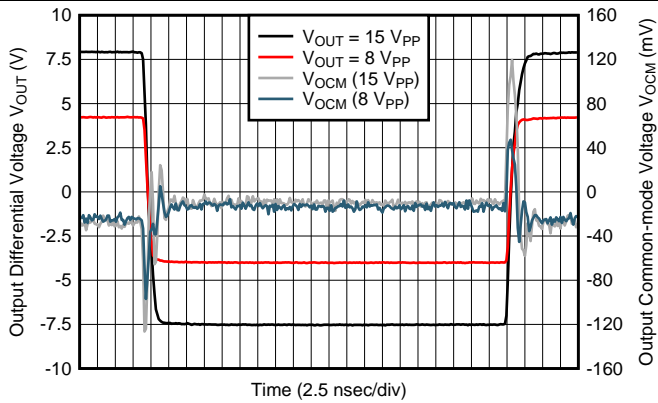
### Typical Characteristics (continued)

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_V$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



Typical Characteristics (continued)

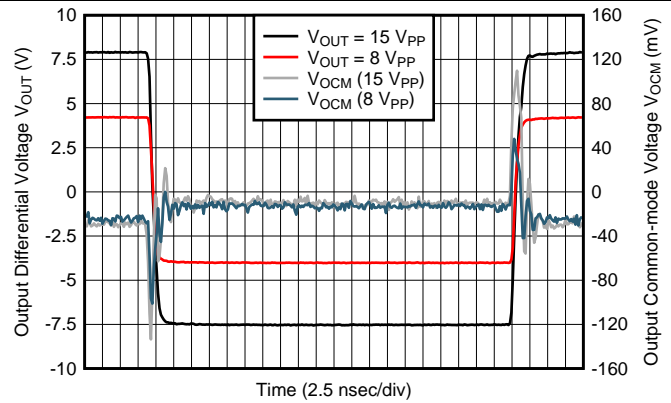
at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_V$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



SR down = 8200 V/ $\mu\text{s}$ , SR up = 6500 V/ $\mu\text{s}$

D013

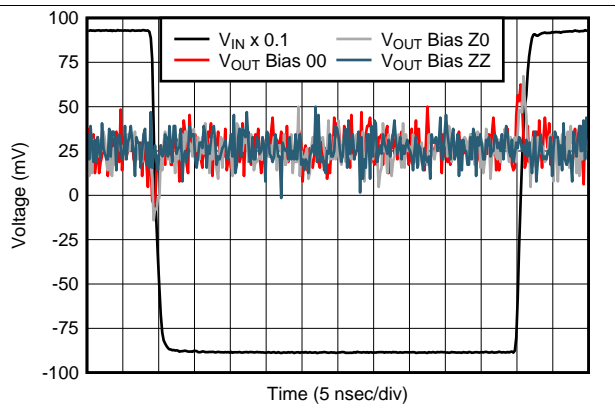
13. Pulse Response Drive Mode 5 (Bias 01)



SR down = 10500 V/ $\mu\text{s}$ , SR up = 8000 V/ $\mu\text{s}$

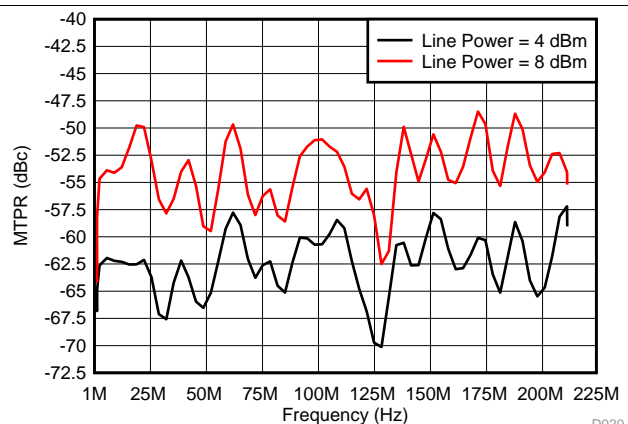
D014

14. Pulse Response Drive Mode 6 (Bias 10)



D015

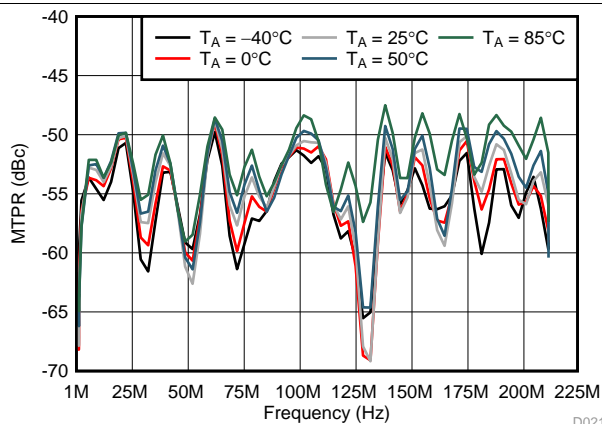
15. Pulse Response Termination and Power-Down Modes



D020

PAR = 15 dB, 1-in-64 missing tones

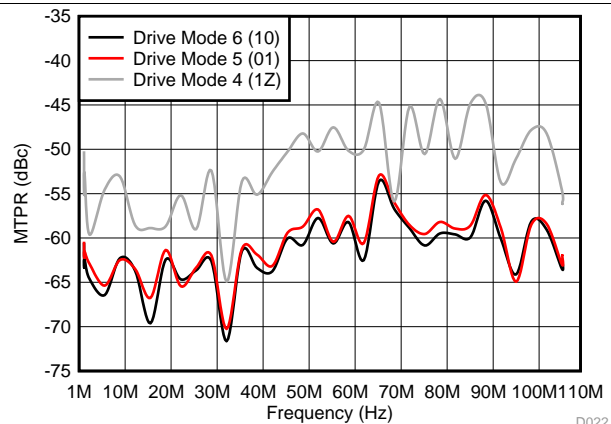
16. MTPR G.Fast 212-MHz Profile (Bias 10)



D021

PAR = 15 dB, 1-in-64 missing tones, Line power = 8 dBm

17. MTPR Over Temperature G.Fast 212-MHz Profile (Bias 10)



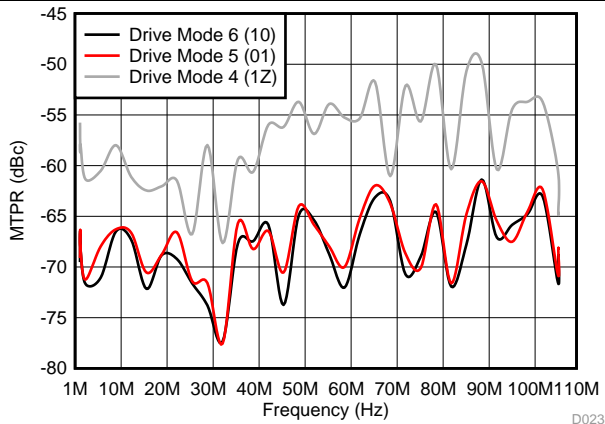
D022

PAR = 15 dB, 1-in-64 missing tones, line power = 8 dBm

18. MTPR G.Fast 106-MHz Profile

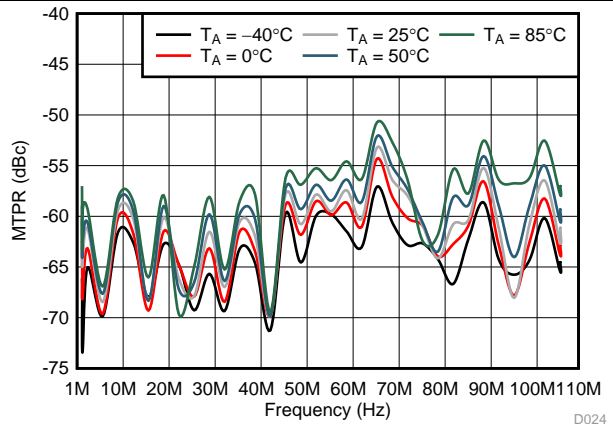
Typical Characteristics (continued)

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_V$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



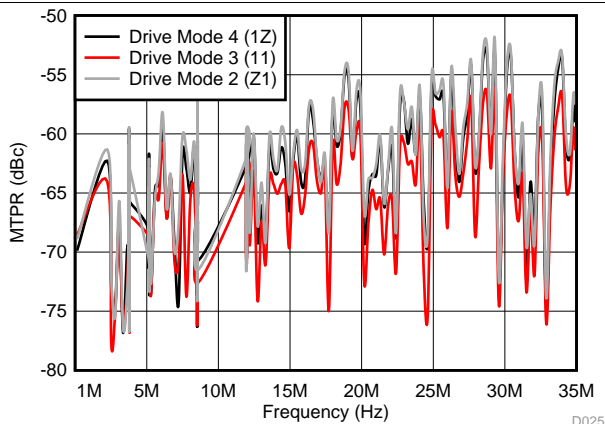
PAR = 15 dB, 1-in-64 missing tones, line power = 4 dBm

Figure 19. MTPR G.Fast 106-MHz Profile



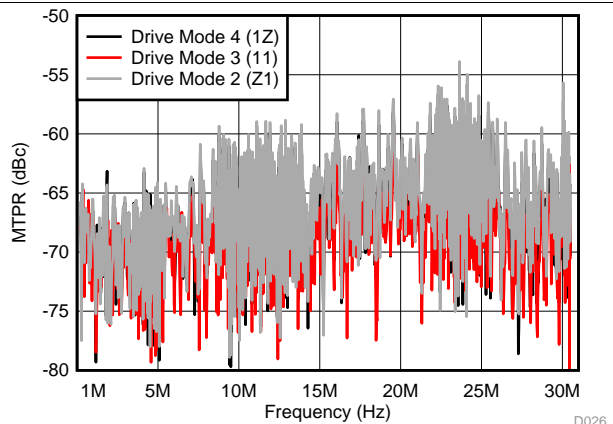
Line power = 8 dBm, PAR = 15 dB, 1-in-64 missing tones

Figure 20. MTPR Over Temperature G.Fast 106-MHz Profile (Bias 01)



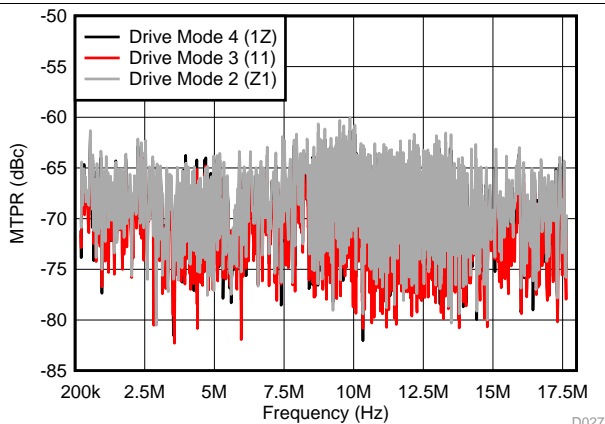
PAR = 15 dB, 1-in-64 missing tones, line power = 8 dBm

Figure 21. MTPR VDSL2-35b Profile



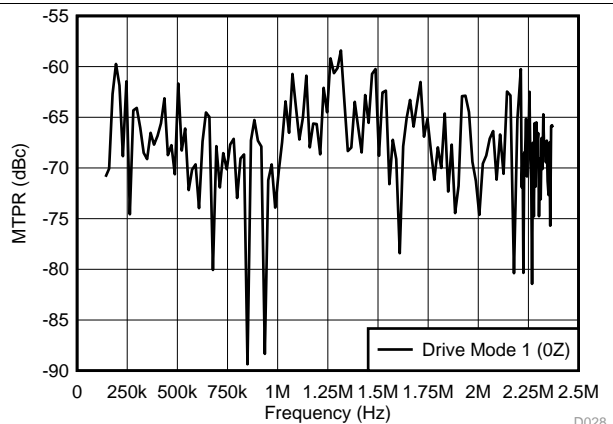
PAR = 15 dB, 1-in-4 missing tones, line power = 8 dBm

Figure 22. MTPR VDSL2-30a Profile



PAR = 15 dB, 1-in-4 missing tones, line power = 8 dBm

Figure 23. MTPR VDSL2-17a Profile

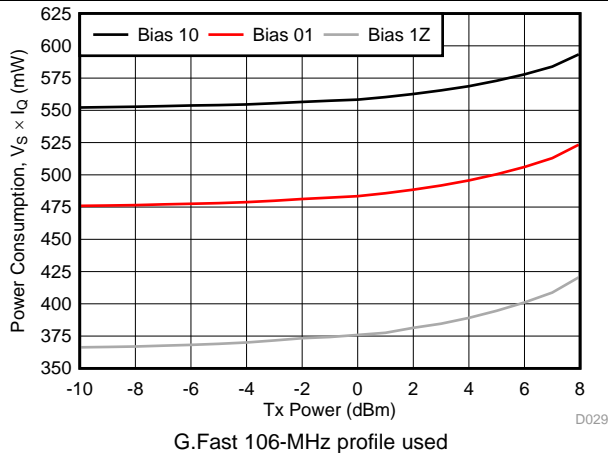


PAR = 15 dB, 1-in-4 missing tones, line power = 8 dBm

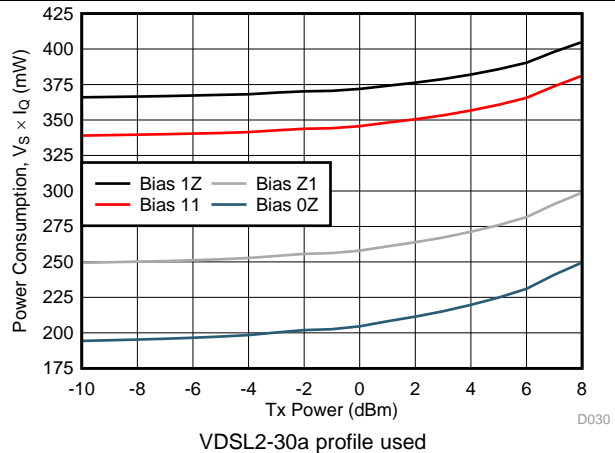
Figure 24. MTPR ADSL2+ Profile

**Typical Characteristics (continued)**

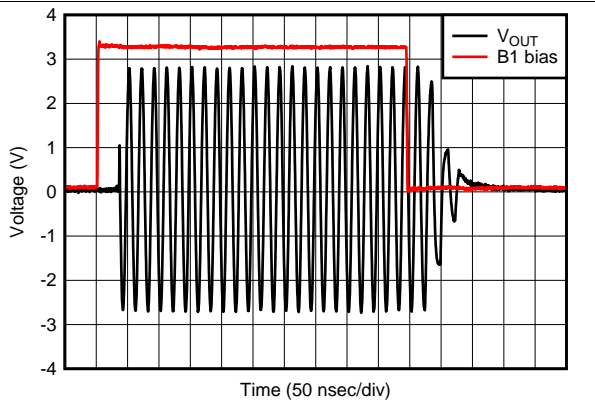
at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_V$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



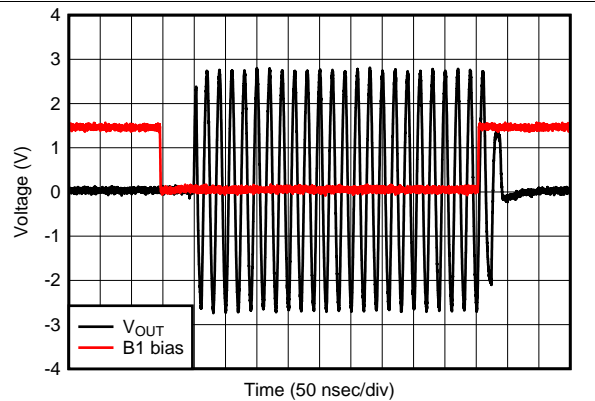
**25. G.Fast Modes Power Consumption**



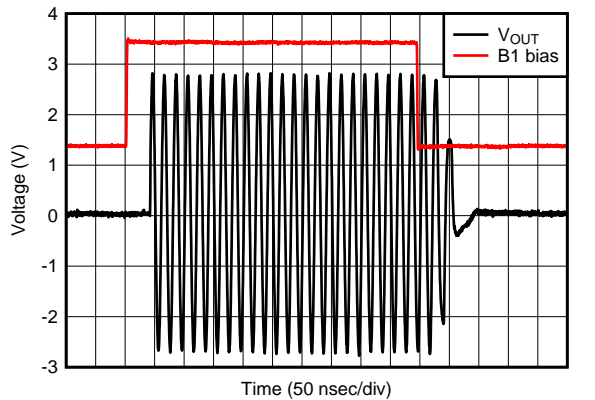
**26. xDSL Modes Power Consumption**



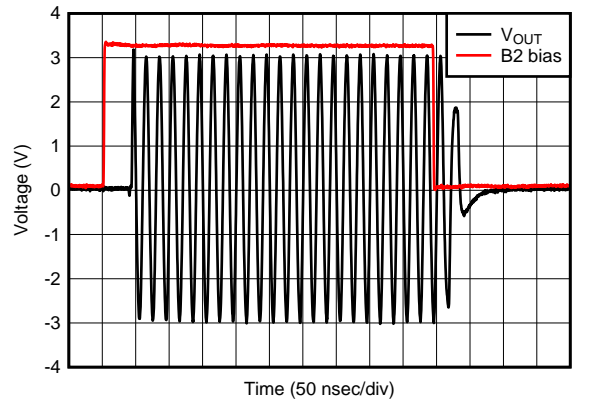
**27. Mode Switch Time 00 to 10**



**28. Mode Switch Time ZZ to 0Z**



**29. Mode Switch Time ZZ to 1Z**



**30. Mode Switch Time Z0 to Z1**

**Typical Characteristics (continued)**

at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_V$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)

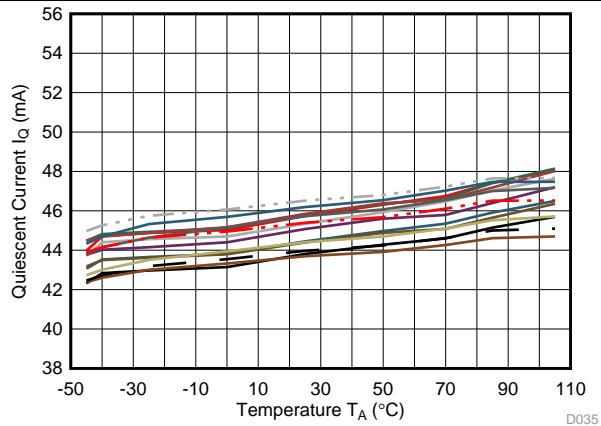


图 31.  $I_Q$  vs Temperature Drive Mode 6 (Bias 10)

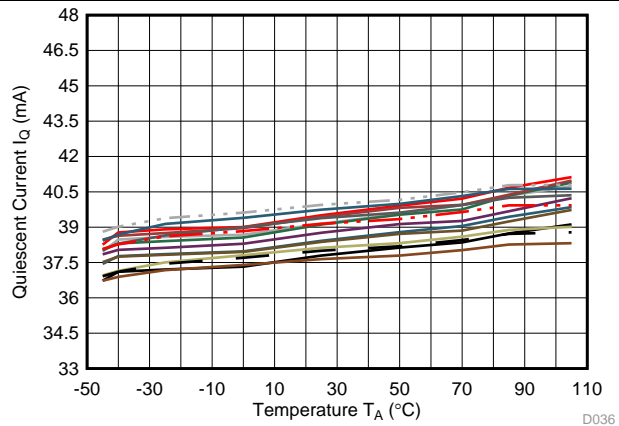


图 32.  $I_Q$  vs Temperature Drive Mode 5 (Bias 01)

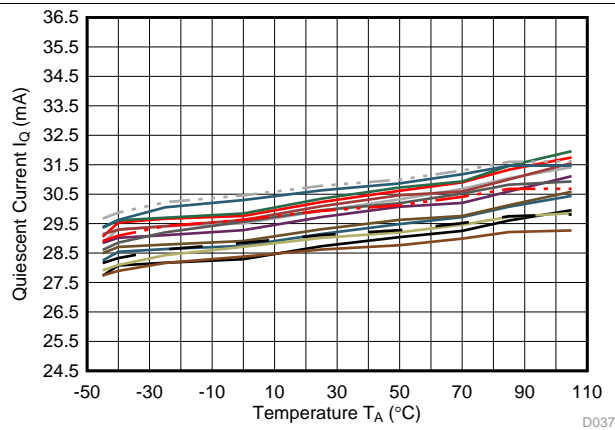


图 33.  $I_Q$  vs Temperature Drive Mode 4 (Bias 1Z)

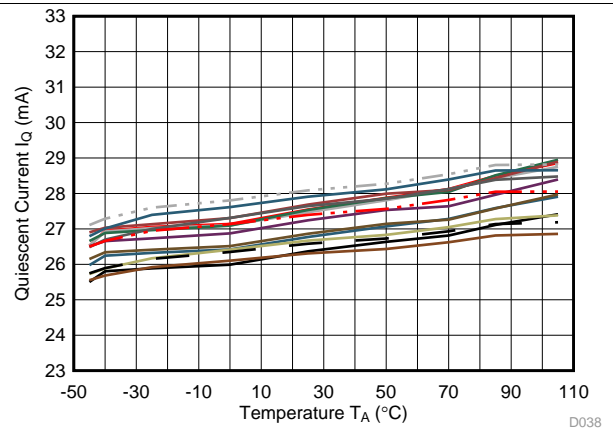


图 34.  $I_Q$  vs Temperature Drive Mode 3 (Bias 11)

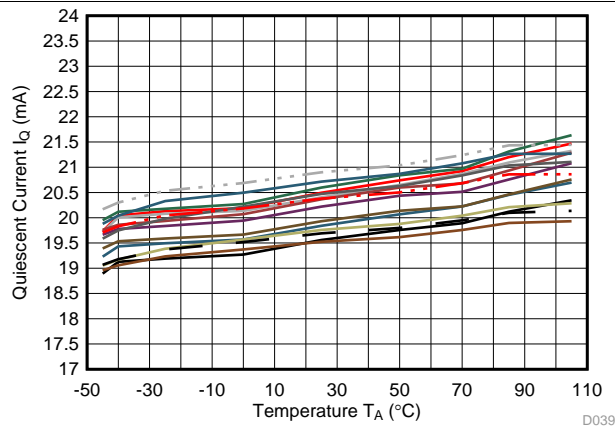


图 35.  $I_Q$  vs Temperature Drive Mode 2 (Bias Z1)

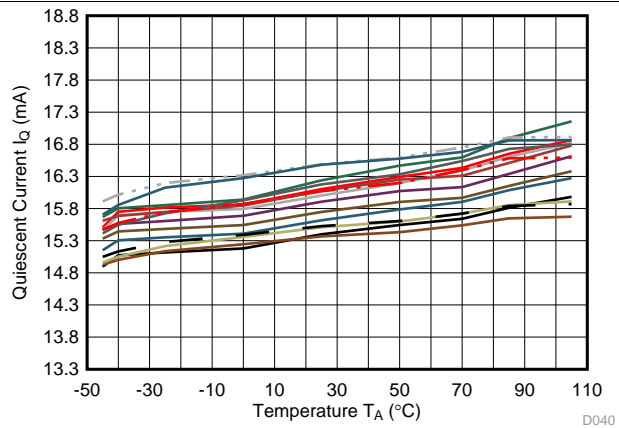
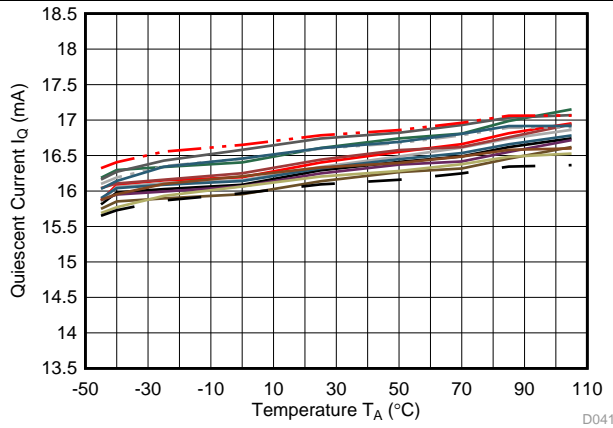


图 36.  $I_Q$  vs Temperature Drive Mode 1 (Bias 0Z)

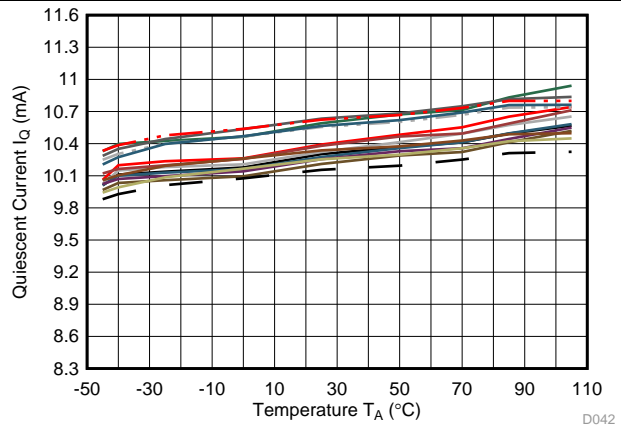


**Typical Characteristics (continued)**

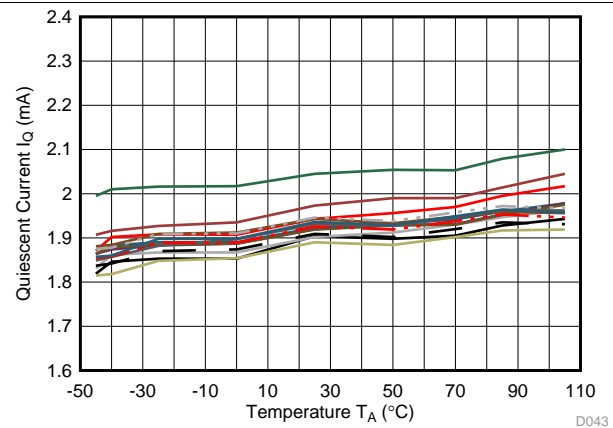
at  $T_A \approx 25^\circ\text{C}$ ,  $V_{S+} = 12\text{ V}$ ,  $V_{S-} = 0\text{ V}$ , voltage gain ( $A_V$ ) = 8.5 V/V, 100- $\Omega$  load,  $R_{\text{SERIES}} = 47.5\ \Omega$ ,  $R_{\text{IADJ}} = 75\ \text{k}\Omega$ ,  $C_{\text{IADJ}} = 100\ \text{pF}$ , and drive mode 5 (B1B2 = 01, G.Fast mid power mode) and output power measured at input of transformer (1:1) with no assumed transformer insertion losses (unless otherwise noted)



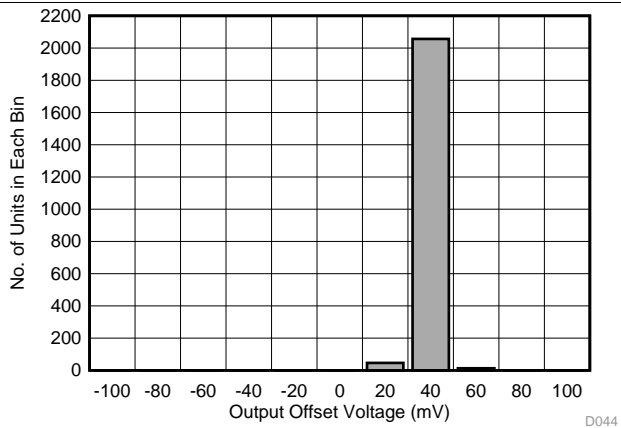
**37.  $I_Q$  vs Temperature High-Power Termination Mode (Bias 00)**



**38.  $I_Q$  vs Temperature Low-Power Termination Mode (Bias Z0)**



**39.  $I_Q$  vs Temperature Power-Down Mode (Bias ZZ)**



**40. Output Offset Voltage Histogram**

## 8 Detailed Description

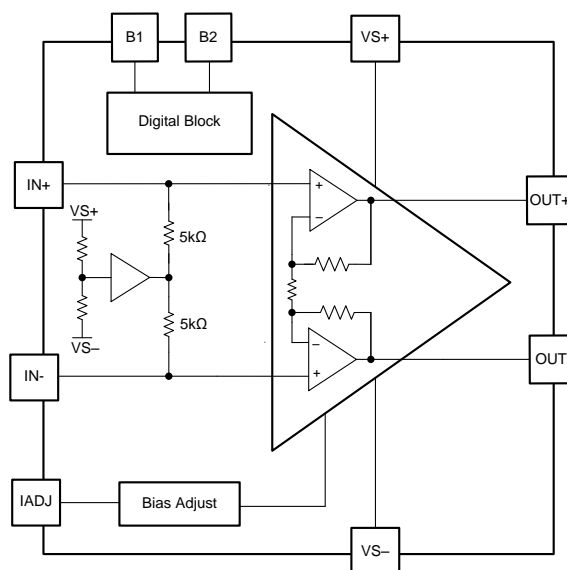
### 8.1 Overview

The THS6301 is a current-feedback architecture, differential line driver designed for G.Fast and xDSL systems. The device is targeted for use in G.Fast digital subscriber line (DSL) systems that enable native discrete multitone modulation (DMT) signals and supports an 8-dBm line power up to 212 MHz with good linearity.

The device consists of a unique architecture consisting of an amplifier in a noninverting configuration with an internally-fixed gain of 8.5 V/V. The THS6301 is designed to drive the high-performance G.Fast 212-MHz DSL profile, but is also backwards-compatible to drive lower frequency profiles. The device features selectable bias modes for the G.Fast 106-MHz profile, VDSL profiles, and ADSL profiles. These modes reduce the quiescent current of the device based on the frequency requirements of the various DSL profiles to maximize power efficiency. Along with adjustable bias modes, the device features two line-termination modes that maintain an output impedance match with low power consumption. The line-termination modes allow for the device to be in a low-power state without causing distortion on a shared signal line.

For further flexibility, the THS6301 features an IADJ pin that is used to further adjust the quiescent current of the device. A resistor connected to this pin can be changed to increase or decrease the device current to meet performance requirements and uses the lowest amount of power possible.

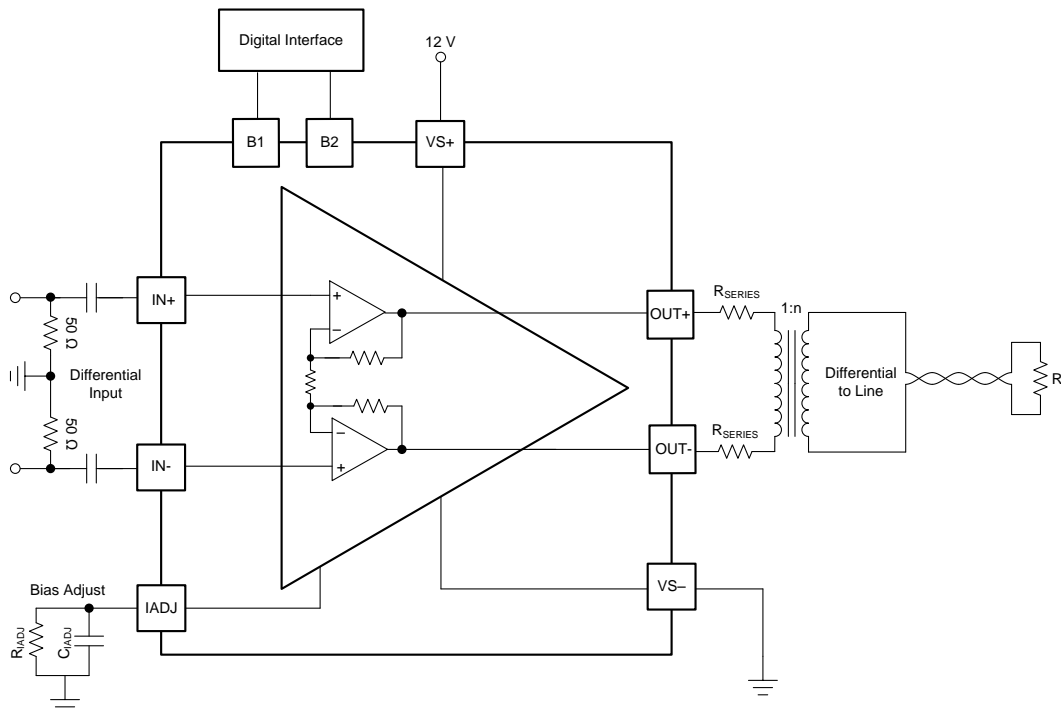
### 8.2 Functional Block Diagram



### 8.3 Feature Description

The THS6301 is a line driver that has a high current drive and a differential input and output. [Figure 41](#) shows an example circuit of the THS6301 configured to drive the G.Fast 212-MHz DSL profile. The bias control pins B1 and B2 are set to 3.3 V and ground, respectively, to put the device in the G.Fast 212-MHz bias mode. This bias mode optimizes the internal power consumption of the device to meet performance specifications of the G.Fast 212-MHz profile and can be changed to meet several different DSL profiles and other modes listed in [Table 1](#). The IADJ pin is biased with a 75-k $\Omega$  ( $R_{IADJ}$ ) resistor that adjusts the device quiescent current to a nominal state.  $R_{IADJ}$  can be increased to lower the quiescent current or decreased to raise the quiescent current of the device for fine-tuning.  $C_{IADJ}$  provides decoupling for the IADJ pin and is typically 100 pF.

The THS6301 has a 10-k $\Omega$ , internally-set differential input impedance and low output impedance. In [Figure 41](#) the input impedance is matched to 100  $\Omega$  by using a 100- $\Omega$  resistor connected differentially across the inputs. This value can easily be changed by using a different resistor to create the desired impedance at the input. Remember that the impedance in the device is actually the parallel combination of 10 k $\Omega$  and the external input resistor. For low impedances, this effect is minimal, but must be considered if the matched input impedance is increased. The output impedance of the THS6301 in [Figure 41](#) is set by the two  $R_{SERIES}$  resistors to match 100  $\Omega$ . The internal output resistance is very low ( $< 2 \Omega$  per output), so the output impedance is primarily set by the  $R_{SERIES}$  resistors. These resistors can be adjusted to match various output impedance values.



**Figure 41. G.Fast, 212-MHz Driving Mode Example Circuit**

## 8.4 Device Functional Modes

The THS6301 features nine different device operational modes, as listed in 表 1, to accommodate the G.Fast, xDSL, line termination, and power-down scenarios. The device is controlled by a 2-pin parallel interface that uses three-level logic to control the device state. The G.Fast and xDSL modes change the quiescent current of the device to meet signal performance requirements and maintain the lowest power possible, which allows for legacy DSL compatibility with maximum power efficiency. The two line-termination modes maintain a low impedance at the output and place the device in a low-power state. The line-termination modes allow for the muxing of multiple devices to one output line by putting the non-driving devices in a state that does not add distortion to the line. A power-down mode is also included to digitally shut down the device for the highest level of power savings. 表 1 lists the device power modes and the typical quiescent currents for each mode.

表 1. Bias Modes Truth Table

MODE DESCRIPTION	BIAS CONTROL PINS		RECOMMENDED DSL PROFILE	TYPICAL QUIESCENT CURRENT ( $R_{IADJ} = 75 \text{ K}\Omega$ )	SSBW ( $V_{OUT} = 1.7 \text{ V}_{PP}$ )
	B1	B2			
Power down	Z	Z	Power down	1.9 mA	N/A
Low-power termination	Z	0	Line termination (low power)	10.2 mA	N/A
High-power termination	0	0	Line termination (high power)	16 mA	N/A
Drive mode 1	0	Z	ADSL2+	15.9 mA	564 MHz
Drive mode 2	Z	1	VDSL (low power)	20.1 mA	659 MHz
Drive mode 3	1	1	G.Fast (low power) and VDSL (mid power)	27.2 mA	755 MHz
Drive mode 4	1	Z	VDSL (high power)	29.8 mA	605 MHz
Drive mode 5	0	1	G.Fast (mid power)	38.9 mA	864 MHz
Drive mode 6	1	0	G.Fast (high power)	45.3 mA	814 MHz

## 8.5 Programming

The THS6301 programming is controlled by two parallel pins, B1 and B2. These pins use three-level logic to create nine different combinations for each pair of pins. The pins have a high state (1) when the pin voltage is greater than 2.3 V, a low state (0) when the pin voltage is less than 0.6 V, and an open state (Z) where the pin floats at approximately 1.4 V or can be driven between 1.2 V and 1.6 V. 表 1 lists the logic combinations for the two pins and the corresponding power modes.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The device is a single-port, very-high-bit-rate linear xDSL, G.Fast differential line driver where the device drives a twisted pair cable. The signal is generated by a high-speed, digital-to-analog converter (DAC) at low signal swings that is amplified by the G.Fast line driver.

The G.Fast system is ac-coupled when transmitting information above the audio band. On the input of the line driver, this ac-coupling translates into the series capacitors to isolate the dc voltage coming from the DAC output common-mode voltage. On the output, a transformer is used to help isolate the 48 V present between the tip and ring of the telephone line.

The transformer can be set to any useful ratio. In practice, the transformer-turn ratio is set between 1:1 and 1:1.4 for the device. The output transformer usually has the active impedance synthesis factor set to 5. This synthesis factor means that the termination resistor ( $R_T$ ) is 1/5th of the load impedance reflected to the transformer secondary. Thus, the correct termination can be selected based on the transformer-turn ratio.

Note that the resulting load detected by the amplifier may affect the amplifier linearity or output voltage swing capabilities.

### 9.2 Typical Application

Figure 42 shows a typical application circuit for this device.

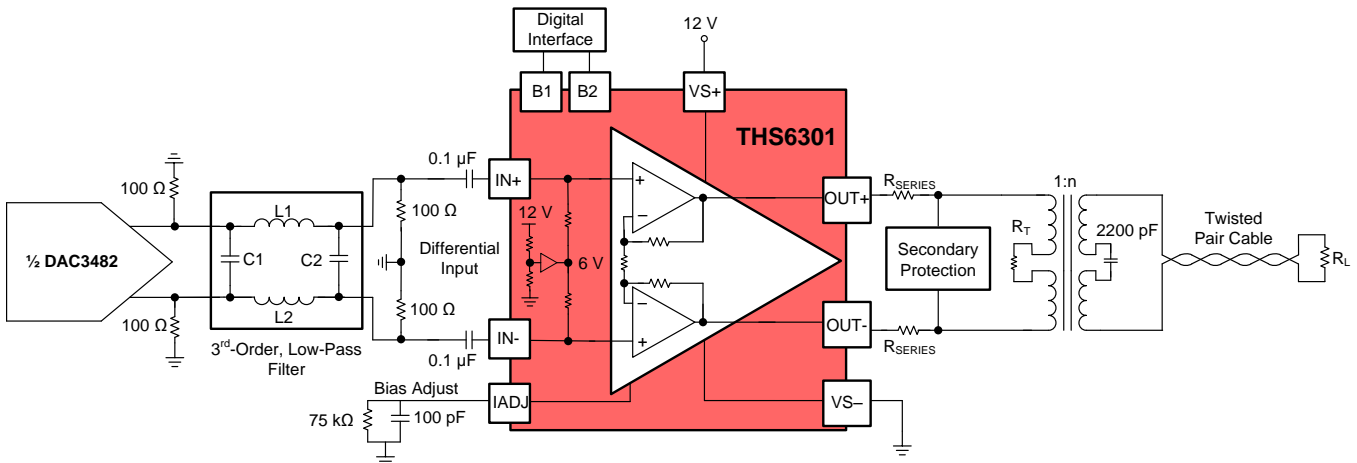


Figure 42. Typical G.FAST Line Driver Configuration

## Typical Application (continued)

### 9.2.1 Design Requirements

表 2 provides the design requirements for a G.Fast line driver, which is met by the THS6301 device.

**表 2. Design Requirements**

DESIGN REQUIREMENT	CONDITION
G.Fast, 106-MHz, 212-MHz transmit profile	Yes, using the bias control pins for line power = 8 dBm and PAR = 15 dBm
Legacy DSL profile support	Yes
Supply voltage	12 V
Output current drive	±80 mA, each output
Power-down functionality	High isolation from input to output
Input interface	AC coupled
Output transformer ratio	1:1.5
Surge protection	External needed

### 9.2.2 Detailed Design Procedure

The G.Fast signal input to the THS6301 comes from a high-speed DAC whose interleaving spurs are filtered out using either a 3rd- or 5th-order filter. Digital pre-emphasis can be employed in the DAC output such that the differential line driver compensates for the transmission line cable losses at long distance and high frequency. The THS6301 is operated on a 12-V single supply. Resulting from the single-supply operation, the device input is AC-coupled using a capacitor that blocks any DC current flowing out of the inputs to the adjacent circuitry. The AC-coupling capacitor forms a high-pass filter with the device input impedance. This pole must be set at a frequency low enough to not interfere with the desired xDSL or G.Fast signal.

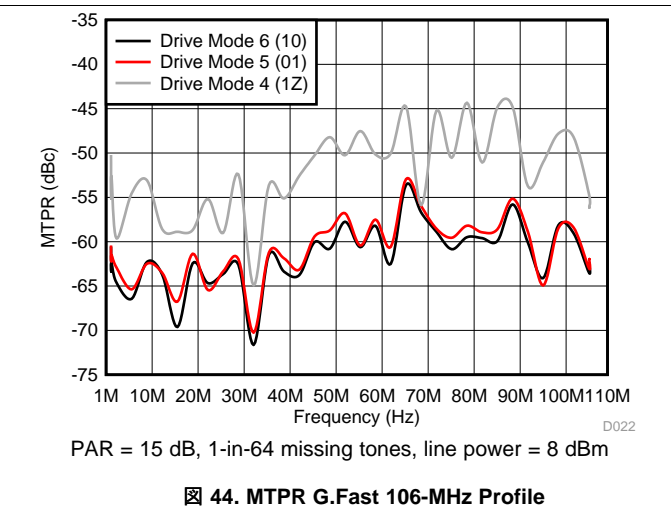
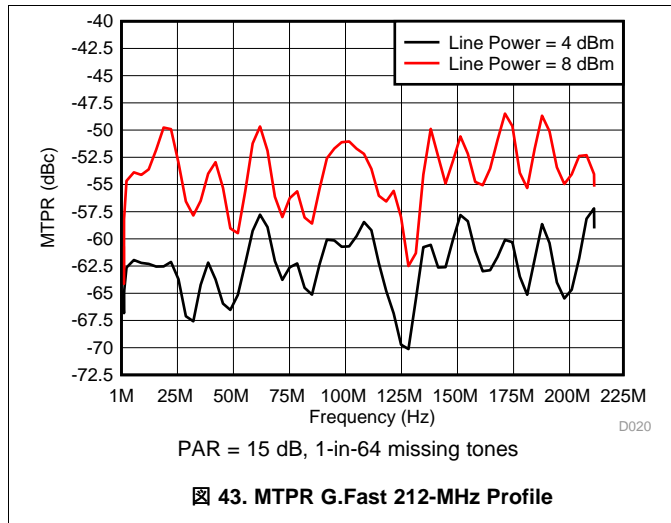
The THS6301 differential outputs usually drive a 1:n output transformer with a transformer turns ratio that can be changed depending upon the application. The output transformer selected must have low insertion loss in the desired frequency band in order to maintain good multi-tone power rejection (MTPR) for a given line power. The load is expected to be a transmission line with 100-Ω characteristic impedance on the primary side of the transformer. Referred to the transformer secondary, the load detected by the amplifier is  $1 / n^2$  with 1:n being the transformer turn ratio. Practical limitations force the transformer-turn ratio to be between 1:1 and 1:1.6. At the lighter load detected by the amplifier (1:1), the voltage swing is limited by the class AB output stage and the maximum achievable swing of the amplifier. At the heaviest load (1:1.6), the voltage swing is limited by the current drive capability of the amplifier. To satisfy the synthesis impedance factor and the loading, the termination resistance ( $R_T$ ) can be set to  $R_T = R_L / 5 = 100 \Omega / (5 \times n^2)$ .

For surge protection, consider adding a gas discharge tube (GDT) on the primary side of the output transformer. The gas discharge tube is required to shunt the large current that could flow through the cables during lightning surge, and protect the device outputs. The secondary protection is also normally added after the series resistance on the secondary transformer side. The secondary protection could be in the form of back to back switching diodes, which also help limit the residual surge current flowing into the device outputs.

For the power-supply bypass, consider using X7R or X5R because of the better stability of these materials over temperature.

### 9.2.3 Application Curves

☒ 43 and ☒ 44 show the MTPR results for 212-MHz and 160-MHz G.Fast profiles, respectively.



## 10 Power Supply Recommendations

The THS6301 is recommended to operate using a total supply voltage of 12 V. If a lower or higher supply voltage is required, select one that is between 11.4 V and 12.6 V for optimal performance. Use supply-decoupling capacitors on the power-supply pins to minimize distortion caused by parasitic signals on the power supply. This usage is especially important in applications where many devices share a single power-supply bus.

The device can be operated on split supplies (such as  $\pm 6$  V). However, the bias adjust resistor must be tied to the negative supply for proper device operation. When operating the device on split supply, pins 4 and 10 act as the negative supply voltage pin. The thermal pad must be tied to either GND or the negative supply voltage in split-supply operation. The device bias mode pins are now referenced to the negative supply voltage for the different logic levels.

As with all high-speed amplifiers, supply bypass capacitors are required for operation of the THS6301. Multiple capacitors are required to cover the entire frequency range of the device. For low frequency bypassing use a 10  $\mu$ F or larger tantalum capacitor (see the description of C1 in the *THS6301EVM User's Guide*). Place this capacitor within two or three centimeters of the amplifier. Use 0.1- $\mu$ F and 1-nF high-frequency bypass capacitors (these capacitors are labeled C2 and C3 on the EVM). Place these capacitors within two to three millimeters of the amplifier and must be directly connected to the power-supply planes with low-impedance vias. Texas Instruments recommends using the capacitors shown in the bill of materials (BOM) that accompanies the *THS6301EVM User's Guide*. The capacitor part numbers are listed in the THS6301EVM user's guide.

## 11 Layout

### 11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6301 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- a. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Excessive parasitic capacitance on the input pin can cause instability. In the line driver application, the parasitic capacitance forms a pole with the load detected by the amplifier and can reduce the effective bandwidth of the application circuit, thus leading to degraded performance. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.
- b. Minimize the distance ( $< 0.25$ " ) from the power-supply pins to high-frequency, 0.1- $\mu$ F decoupling capacitors. At the device pins, make sure that the ground and power-plane layout are not in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and decoupling capacitors. Always decouple the power-supply connections with these capacitors.
- c. Make sure the bias adjust resistor connected to the IADJ pin is not routed close to the device inputs in-order to avoid any high-frequency noise coupling into the IADJ pin and result in unexpected device behavior.
- d. Careful selection and placement of external components preserves the high-frequency performance of the device. Use very-low reactance-type resistors. Surface-mount resistors function best and allow a tighter overall layout. Metal-film or carbon composition, axially-leaded resistors also provide good high-frequency performance. Again, keep the leads and printed circuit board (PCB) traces as short as possible. Never use wire-wound type resistors in a high-frequency application.
- e. Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them.
- f. Do not socket a high-speed part such as the THS6301. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the device onto the board.
- g. TI recommends soldering the thermal pad to the PCB in order to conduct heat out of the device package. Vias underneath the part help regulate the flow of free air and also help conduct heat out of the package.



## Layout Guidelines (continued)

### 11.1.1 Power Dissipation and Thermal Considerations

For maximum performance and reliability, the designer must ensure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PCB. 式 1 calculates maximum power dissipation for a given package:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$

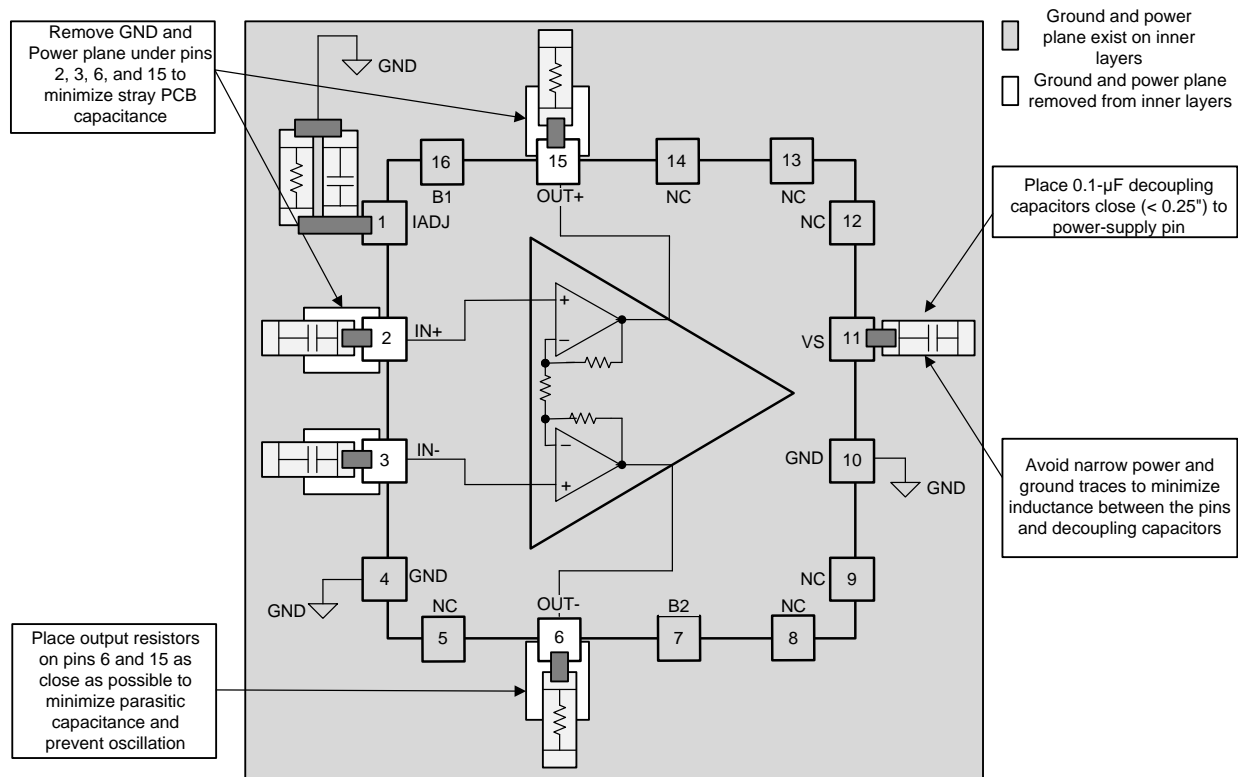
where

- $P_{D(MAX)}$  is the maximum power dissipation in the amplifier (W)
- $T_{J(MAX)}$  is the absolute maximum junction temperature (°C)
- $T_A$  is the ambient temperature (°C)
- $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
- $R_{\theta JC}$  is the thermal coefficient from silicon transistors to the case (°C/W)
- $R_{\theta CA}$  is the thermal coefficient from case to ambient temperature (°C/W) (1)

For systems where heat dissipation is more critical, the THS6301 is offered in an 16-pin VQFN package with thermal pad. Because of the thermal pad, the thermal coefficient for the VQFN package is substantially improved over the traditional SOIC. The data for the VQFN packages with thermal pad assume a board layout that follows the thermal pad layout guidelines referenced in this section and detailed in the [Quad Flatpack No-Lead Logic Packages](#) application note. If the thermal pad is not soldered to the PCB, the thermal impedance increases substantially, which may cause serious heat and performance issues. Be sure to always solder the thermal pad to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, this dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

## 11.2 Layout Example



☒ 45. Example Layout

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントのサポート

#### 12.1.1 関連資料

関連資料については、以下を参照してください。

- 『クワッド・フラットパックのリードなしロジック・パッケージ』アプリケーション・ノート
- 『ADSLライン・ドライバのアクティブ出力インピーダンス』アプリケーション・ノート
- 『THS6301EVMユーザー・ガイド』

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.4 商標

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 12.6 Glossary



**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6301IRSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS 6301	
THS6301IRSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS 6301	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

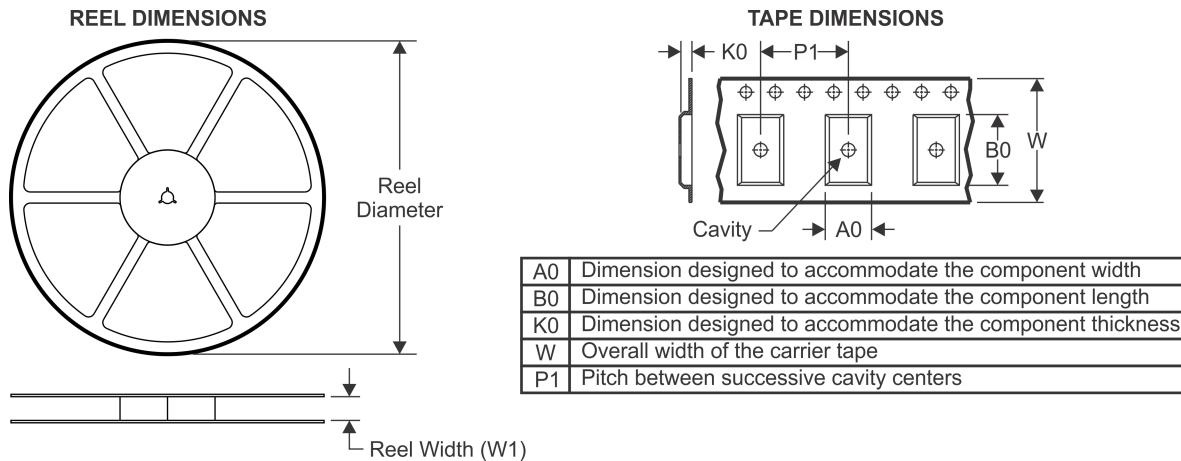
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6301IRSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
THS6301IRSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6301IRSAR	QFN	RSA	16	3000	367.0	367.0	35.0
THS6301IRSAT	QFN	RSA	16	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

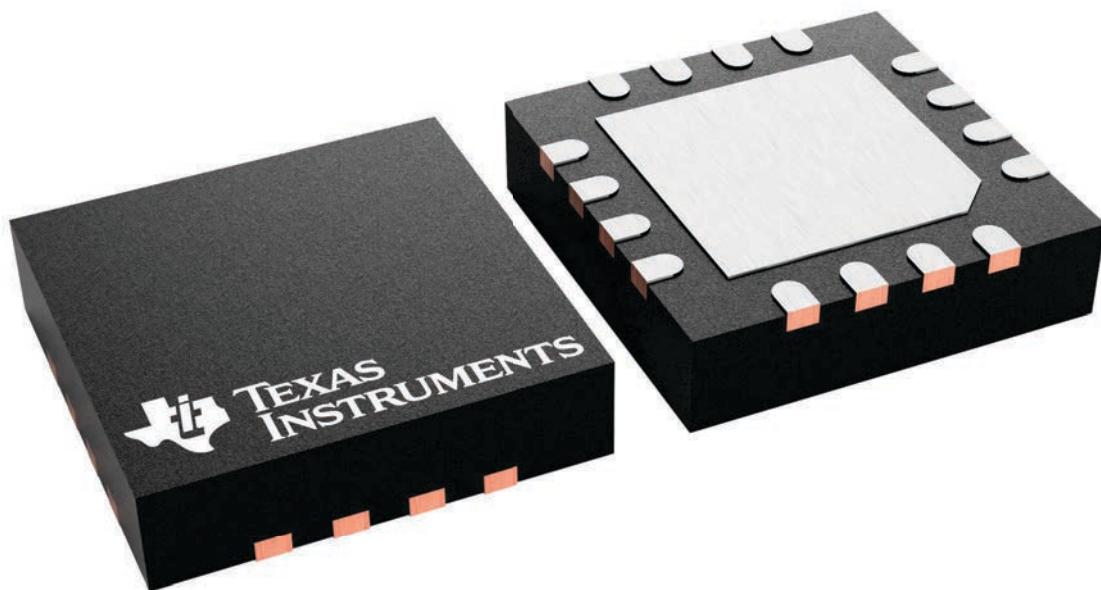
**RSA 16**

**VQFN - 1 mm max height**

4 x 4, 0.65 mm pitch

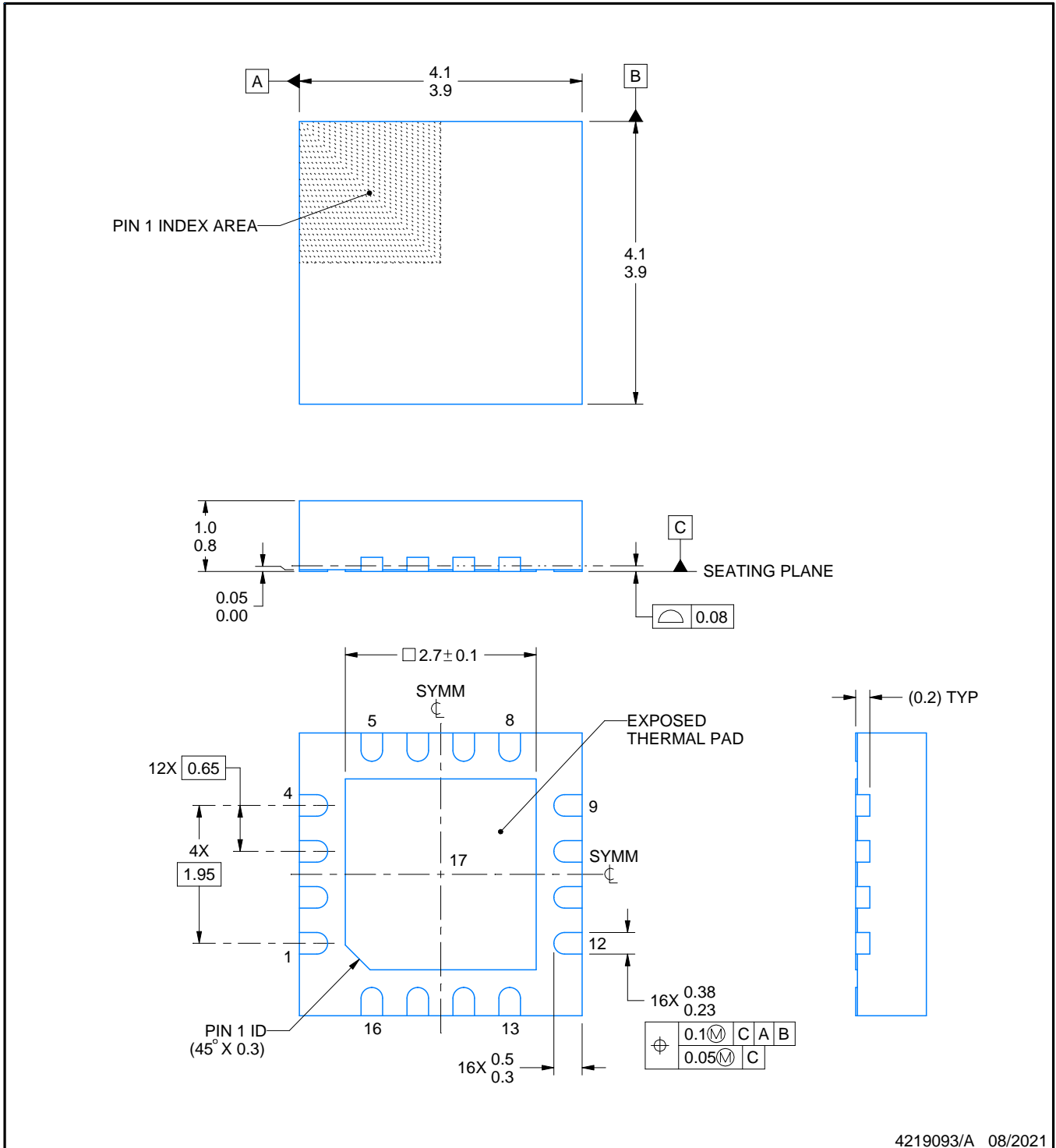
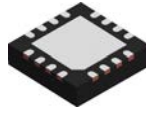
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4230969/A





4219093/A 08/2021

NOTES:

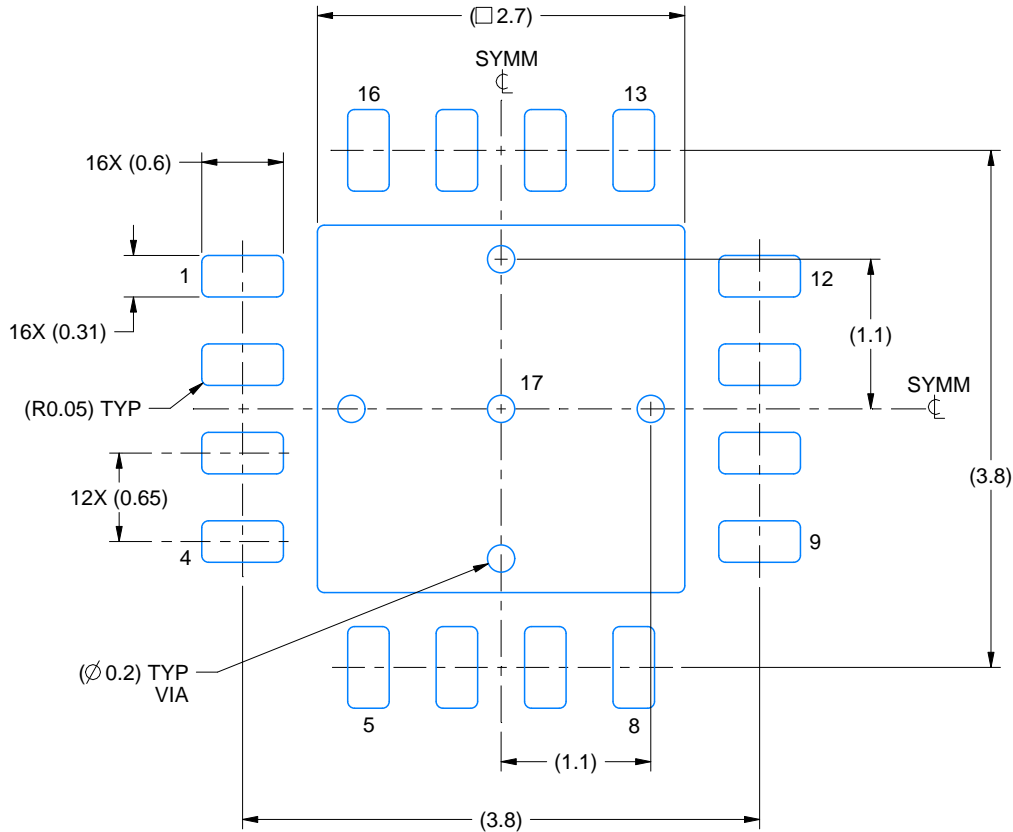
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

# EXAMPLE BOARD LAYOUT

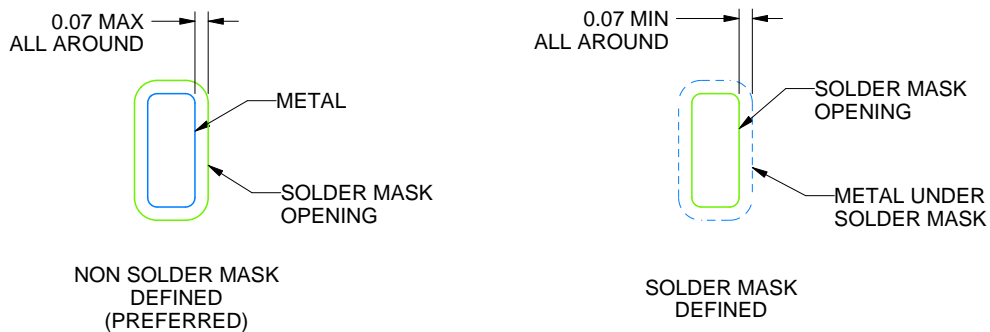
RSA0016B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

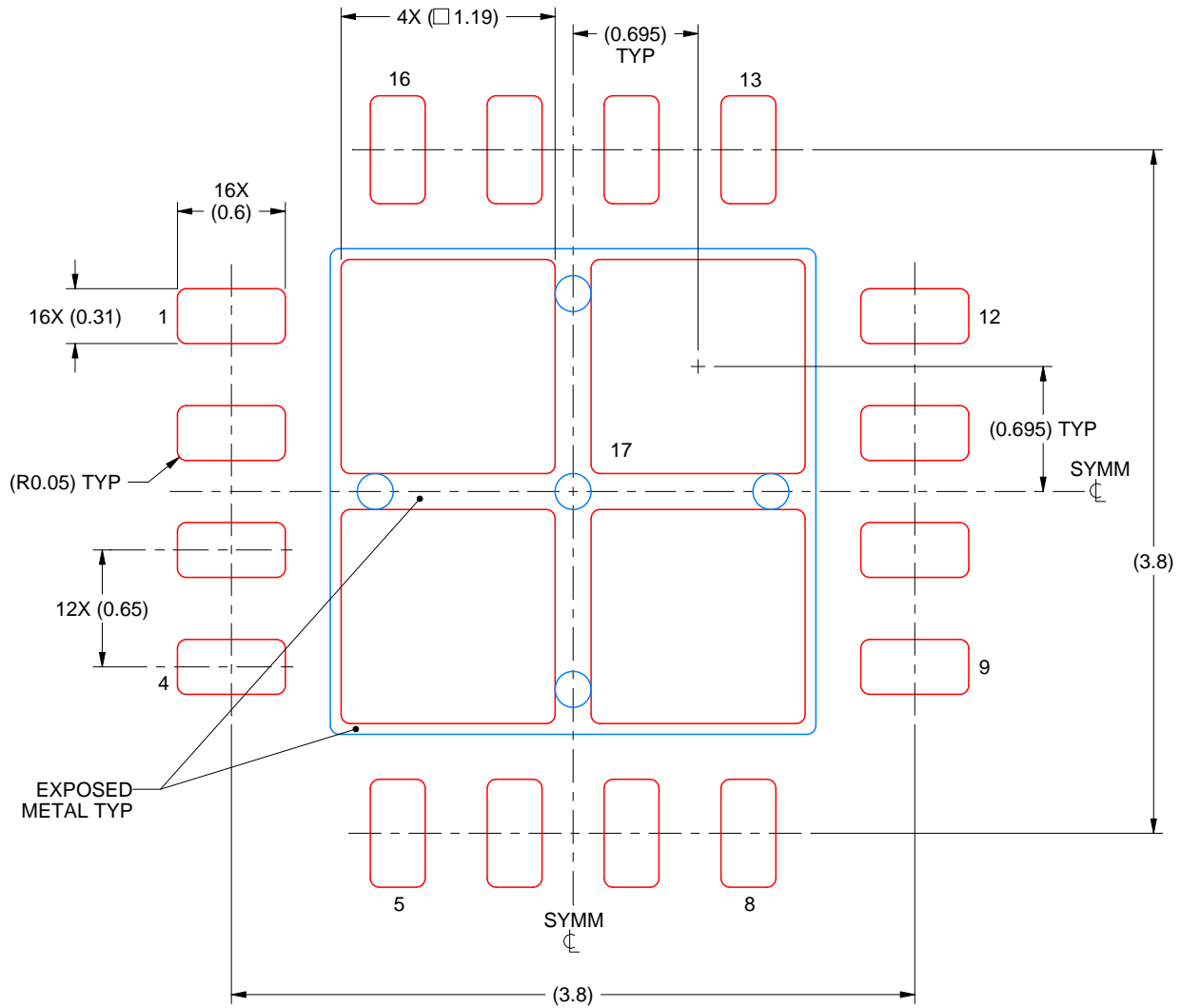
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSA0016B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 77% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:25X

4219093/A 08/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated