

## THVD14x9 3.3V~5V、サージ保護機能付き RS-485 トランシーバ

### 1 特長

- TIA/EIA-485A規格の要件を満たすか、それを上回る性能
- 電源電圧: 3V~5.5V
- バスI/O保護
  - $\pm 16\text{kV}$  HBM ESD
  - $\pm 8\text{kV}$  IEC 61000-4-2接触放電
  - $\pm 30\text{kV}$  IEC 61000-4-2空中放電
  - $\pm 4\text{kV}$  IEC 61000-4-4電気的高速過渡
  - $\pm 2.5\text{kV}$  IEC 61000-4-5 1.2/50 $\mu\text{s}$ サージ
- 2つの速度グレードで供給
  - THVD1419: 250kbps
  - THVD1429: 20Mbps
- 拡張周囲温度範囲:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
- 拡張動作同相範囲:  $\pm 12\text{V}$
- ノイズ除去用のレシーバのヒステリシス: 30mV
- 低消費電力
  - スタンバイ時消費電流: 2 $\mu\text{A}$ 未満
  - 動作時電流: 3mA未満
- グリッチなしの電源オン/オフによるホット・プラグイン能力
- 開放、短絡、アイドル・バスのフェイルセーフ
- 1/8の単位負荷(最大256のバス・ノード)
- 業界標準の8ピンSOICによるドロップイン互換

### 2 アプリケーション

- ワイヤレス・インフラ
- ビルディング・オートメーション
- HVACシステム
- ファクトリ・オートメーション/制御
- 電力網インフラストラクチャ
- スマート・メータ
- プロセス分析
- ビデオ監視

### 3 概要

THVD1419およびTHVD1429は、半二重RS-485トランシーバで、サージ保護機能が内蔵されています。標準の8ピンSOIC (D)パッケージに過渡電圧抑制(TVS)ダイオードを内蔵することで、サージ保護機能を実現しています。この特長により、信頼性が大きく向上し、データ・ケーブルに結合されたノイズ過渡に対する耐性が強化され、外付けの保護部品は不要になります。

これらの各デバイスは、単一の3.5Vまたは5V電源で動作します。このファミリのデバイスは同相電圧範囲が広いいため、長いケーブルを使用するマルチポイント・アプリケーションに最適です。

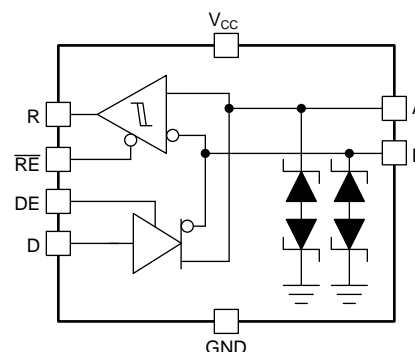
THVD1419およびTHVD1429デバイスは、業界標準のSOICパッケージで供給され、PCBの変更なしに簡単にドロップインできます。このデバイスは、 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$ の周囲自由通気温度範囲で仕様が規定されています。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
THVD1419	SOIC (8)	4.90mm×3.91mm
THVD1429		

(1) 利用可能なすべてのデバイスについては、このデータシートの末尾にある注文情報を参照してください。

#### THVD1419とTHVD1429のブロック図



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			<b>14</b>	<b>メカニカル、パッケージ、および注文情報</b>	<b>22</b>

## 4 改訂履歴

Revision B (December 2018) から Revision C に変更		Page
•	THVD1419 を「製品プレビュー」から「量産データ」に変更	1
•	Changed power dissipation numbers of THVD1419	6
•	Changed THVD1419 driver switching characteristics	8
•	Changed THVD1419 receiver switching characteristics	8
•	Added 図 7 to 図 9	9

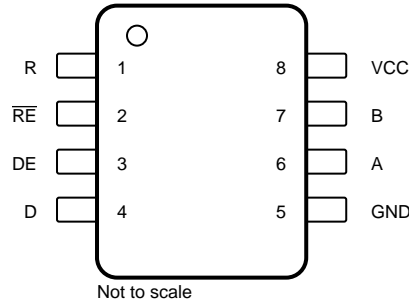
Revision A (December 2018) から Revision B に変更		Page
•	THVD1429を「事前情報」から「量産データ」に変更	1

## 5 Device Comparison Table

PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1419	Half	DE, $\overline{RE}$	up to 250 kbps	256
THVD1429			up to 20 Mbps	

## 6 Pin Configuration and Functions

THVD1419, THVD1429 Devices  
8-Pin D Package (SOIC)  
Top View



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	5	Ground	Device ground
R	1	Digital output	Receive data output
V <sub>CC</sub>	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	$V_{CC}$	-0.5	7	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-15	15	V
Input voltage	Range at any logic pin (D, DE, or /RE)	-0.3	5.7	V
Receiver output current	$I_O$	-24	24	mA
Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, 2010	±16	kV
			±8	kV
		Charged device model (CDM), per JEDEC JESD22-C101E	±1.5	kV

### 7.3 ESD Ratings [IEC]

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact Discharge, per IEC 61000-4-2	±8	kV
		Air-Gap Discharge, per IEC 61000-4-2	±30	kV
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	±4	kV
$V_{(surge)}$	Surge	Per IEC 61000-4-5, 1.2/50 $\mu$ s	±2.5	kV

## 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		5.5	V
V <sub>I</sub>	Input voltage at any bus terminal (separately or common mode) <sup>(1)</sup>	-12		12	V
V <sub>IH</sub>	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V <sub>ID</sub>	Differential input voltage	-12		12	V
I <sub>O</sub>	Output current, driver	-60		60	mA
I <sub>OR</sub>	Output current, receiver	-8		8	mA
R <sub>L</sub>	Differential load resistance	54			Ω
1/t <sub>UI</sub>	Signaling rate: THVD1419			250	kbps
1/t <sub>UI</sub>	Signaling rate: THVD1429			20	Mbps
T <sub>A</sub>	Operating ambient temperature	-40		125	°C
T <sub>J</sub>	Junction temperature	-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 7.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		THVD14x9	UNIT
		D (SOIC)	
		8-PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	120.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	62.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 7.6 Power Dissipation

PARAMETER	Description	TEST CONDITIONS	VALUE	UNIT
P <sub>D</sub>	Driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 125 °C, 50% duty cycle square wave at maximum signaling rate, THVD1419	Unterminated: R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	230	mW
		RS-422 load: R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF	350	mW
		RS-485 load: R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF	470	mW
	Driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 125 °C, 50% duty cycle square wave at maximum signaling rate, THVD1429	Unterminated: R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	350	mW
		RS-422 load: R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF	290	mW
		RS-485 load: R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF	300	mW

## 7.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Driver</b>						
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60 \Omega$ , $-12 \text{ V} \leq V_{\text{test}} \leq 12 \text{ V}$ , see <a href="#">10</a>	1.5	3.5		V
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60 \Omega$ , $-12 \text{ V} \leq V_{\text{test}} \leq 12 \text{ V}$ , $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$ , see <a href="#">10</a>	2.1			V
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 100 \Omega$ , see <a href="#">11</a>	2	4		V
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 54 \Omega$ , see <a href="#">11</a>	1.5	3.5		V
$\Delta V_{OD} $	Change in differential output voltage		-200		200	mV
$V_{OC}$	Common-mode output voltage	$R_L = 54 \Omega$ , see <a href="#">11</a>	1	$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		-200		200	mV
$I_{OS}$	Short-circuit output current	$DE = V_{CC}$ , $-7 \text{ V} \leq V_O \leq 12 \text{ V}$	-250		250	mA
<b>Receiver</b>						
$I_i$	Bus input current	$DE = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or $5.5 \text{ V}$	$V_i = 12 \text{ V}$	50	125	$\mu\text{A}$
			$V_i = -7 \text{ V}$	-100	-65	$\mu\text{A}$
			$V_i = -12 \text{ V}$	-150	-100	$\mu\text{A}$
$V_{TH+}$	Positive-going input threshold voltage	Over common-mode range of $\pm 12 \text{ V}$	See <sup>(1)</sup>	-100	-20	mV
$V_{TH-}$	Negative-going input threshold voltage		-200	-130	See <sup>(1)</sup>	mV
$V_{HYS}$	Input hysteresis		30		mV	
$C_{A,B}$	Input differential capacitance	Measured between A and B, $f = 1 \text{ MHz}$		220		pF
$V_{OH}$	Output high voltage	$I_{OH} = -8 \text{ mA}$	$V_{CC} - 0.4$	$V_{CC} - 0.3$		V
$V_{OL}$	Output low voltage	$I_{OL} = 8 \text{ mA}$		0.2	0.4	V
$I_{OZR}$	Output high-impedance current	$V_O = 0 \text{ V}$ or $V_{CC}$ , $\overline{RE} = V_{CC}$	-1		1	$\mu\text{A}$
<b>Logic</b>						
$I_{IN}$	Input current (D, DE, $\overline{RE}$ )	$4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$	-6.2		6.2	$\mu\text{A}$
<b>Device</b>						
$I_{CC}$	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE} = 0 \text{ V}$ , $DE = V_{CC}$ , No load	2.4	3	mA
		Driver enabled, receiver disabled	$\overline{RE} = V_{CC}$ , $DE = V_{CC}$ , No load	2	2.6	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0 \text{ V}$ , $DE = 0 \text{ V}$ , No load	700	960	$\mu\text{A}$
		Driver and receiver disabled	$\overline{RE} = V_{CC}$ , $DE = 0 \text{ V}$ , D = open, No load	0.1	2	$\mu\text{A}$
$T_{SD}$	Thermal shutdown temperature			170		$^{\circ}\text{C}$

(1) Under any specific conditions,  $V_{TH+}$  is assured to be at least  $V_{HYS}$  higher than  $V_{TH-}$ .

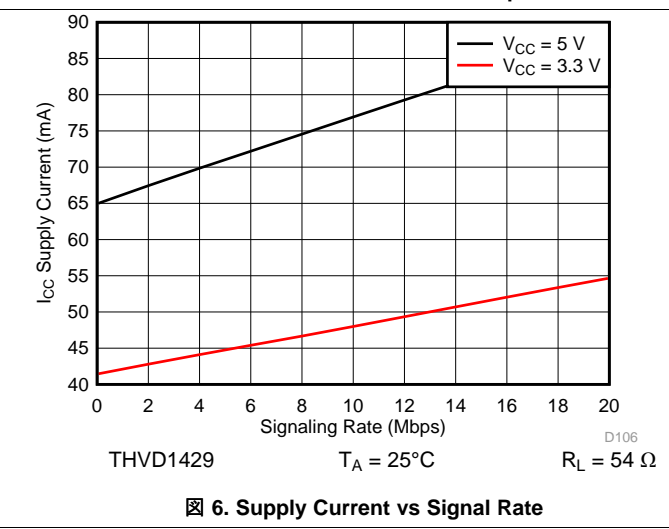
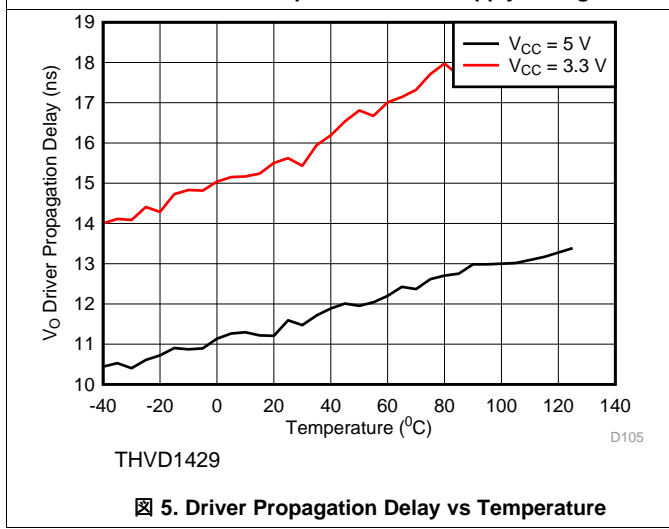
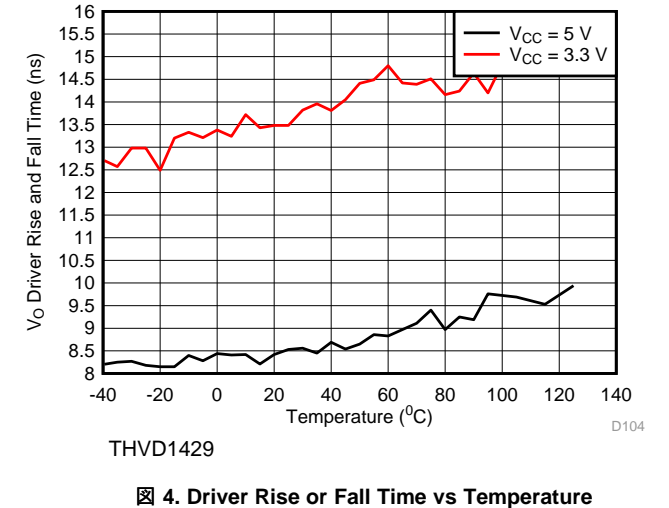
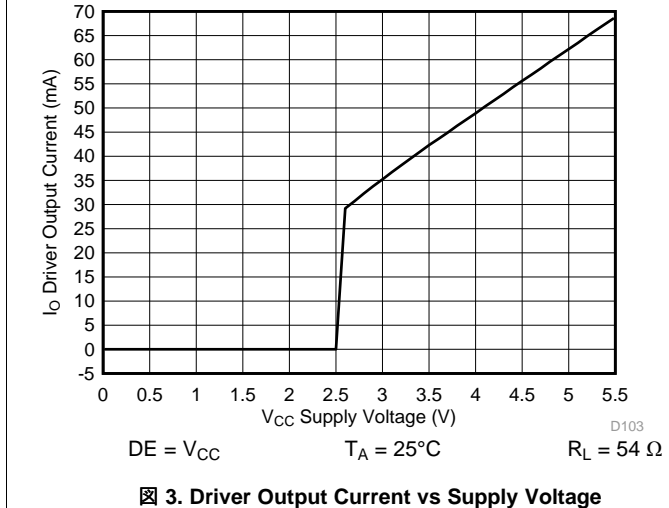
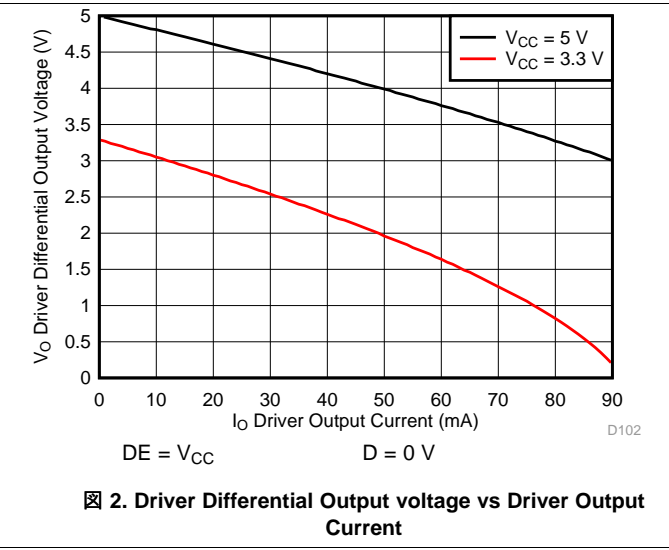
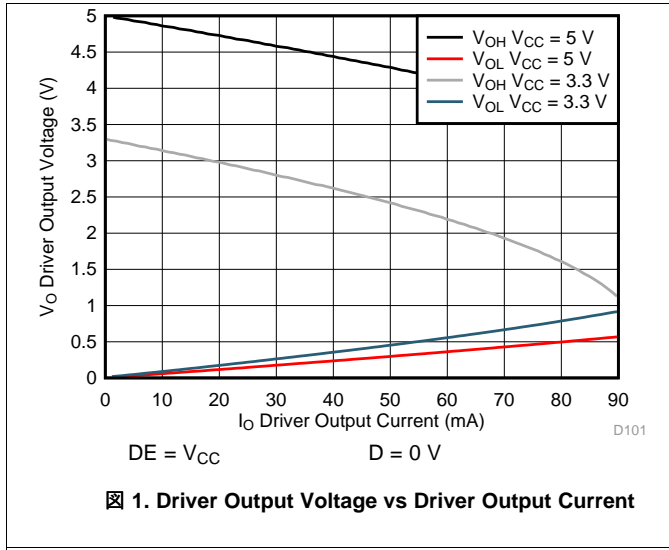
## 7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

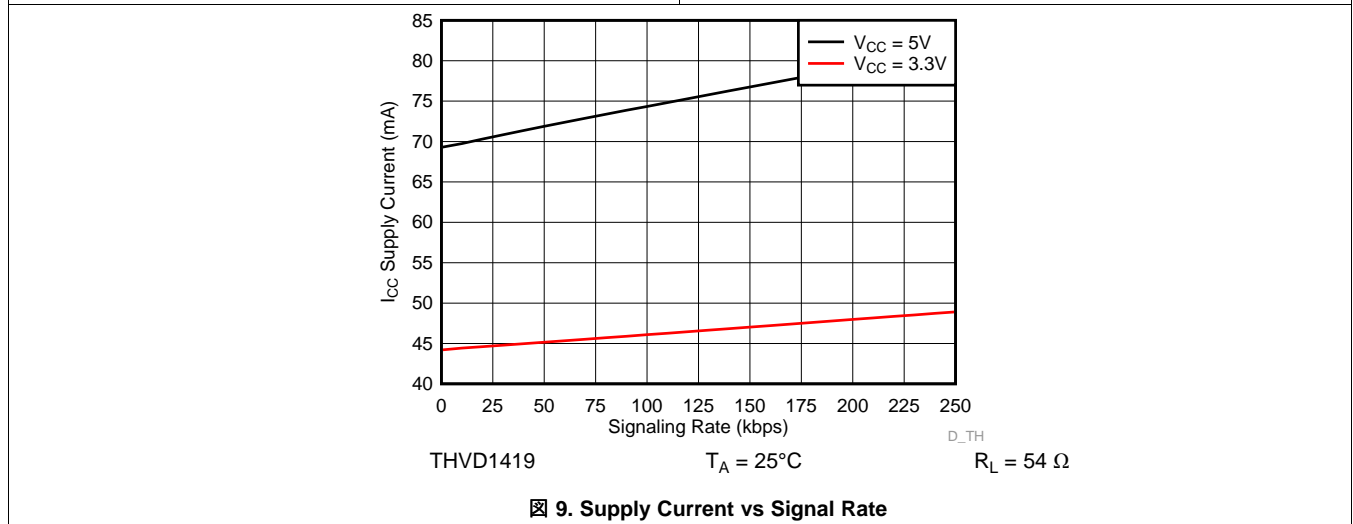
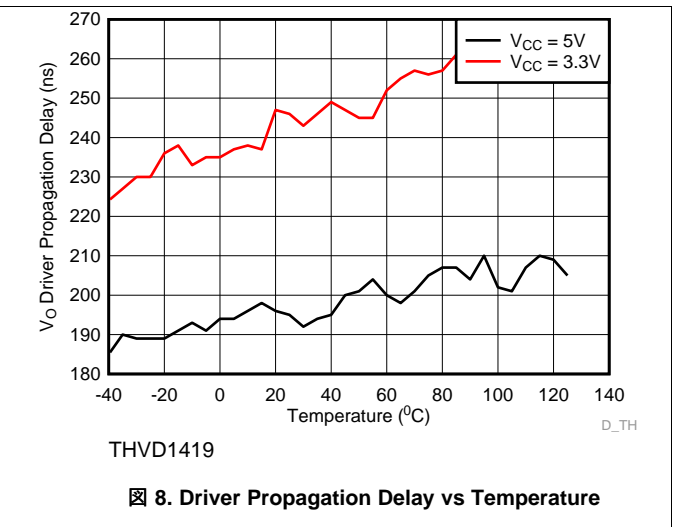
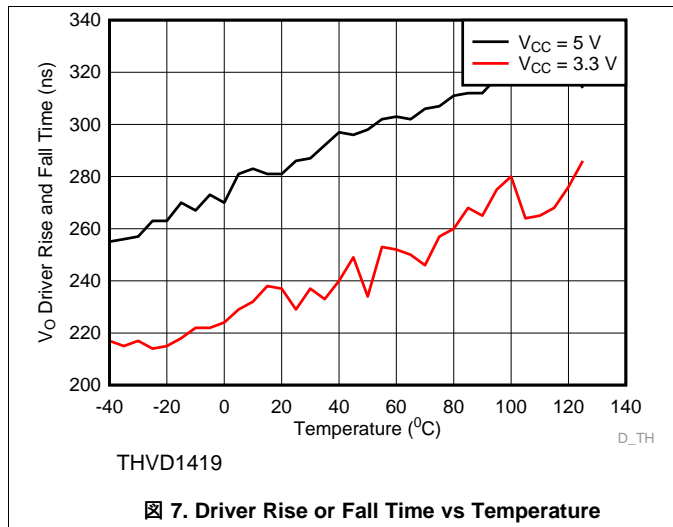
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Driver: THVD1419</b>						
$t_r, t_f$	Differential output rise / fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">12</a>		300	500	ns
$t_{PHL}, t_{PLH}$	Propagation delay			200	450	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				40	ns
$t_{PHZ}, t_{PLZ}$	Disable time			20	50	ns
$t_{PZH}, t_{PZL}$	Enable time	$\overline{RE} = 0 \text{ V}$ , see <a href="#">13</a> and <a href="#">14</a>		60	250	ns
		$\overline{RE} = V_{CC}$ , see <a href="#">13</a> and <a href="#">14</a>		3	11	$\mu\text{s}$
<b>Receiver: THVD1419</b>						
$t_r, t_f$	Output rise / fall time	$C_L = 15 \text{ pF}$ , see <a href="#">15</a>		14	20	ns
$t_{PHL}, t_{PLH}$	Propagation delay			30	50	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				7	ns
$t_{PHZ}, t_{PLZ}$	Disable time			35	45	ns
$t_{PZH(1)}, t_{PZL(1)}, t_{PZH(2)}, t_{PZL(2)}$	Enable time	$DE = V_{CC}$ , see <a href="#">16</a>		80	120	ns
		$DE = 0 \text{ V}$ , see <a href="#">17</a>		5	14	$\mu\text{s}$
<b>Driver: THVD1429</b>						
$t_r, t_f$	Differential output rise / fall time	$R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">12</a>		9	16	ns
$t_{PHL}, t_{PLH}$	Propagation delay			12	25	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				6	ns
$t_{PHZ}, t_{PLZ}$	Disable time			18	40	ns
$t_{PZH}, t_{PZL}$	Enable time	$\overline{RE} = 0 \text{ V}$ , see <a href="#">13</a> and <a href="#">14</a>		16	40	ns
		$\overline{RE} = V_{CC}$ , see <a href="#">13</a> and <a href="#">14</a>		2.8	11	$\mu\text{s}$
<b>Receiver: THVD1429</b>						
$t_r, t_f$	Output rise / fall time	$C_L = 15 \text{ pF}$ , see <a href="#">15</a>		2	6	ns
$t_{PHL}, t_{PLH}$	Propagation delay			12	45	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				6	ns
$t_{PHZ}, t_{PLZ}$	Disable time			14	28	ns
$t_{PZH(1)}, t_{PZL(1)}, t_{PZH(2)}, t_{PZL(2)}$	Enable time	$DE = V_{CC}$ , see <a href="#">16</a>		75	110	ns
		$DE = 0 \text{ V}$ , see <a href="#">17</a>		4.8	14	$\mu\text{s}$



### 7.9 Typical Characteristics



Typical Characteristics (continued)



## 8 Parameter Measurement Information

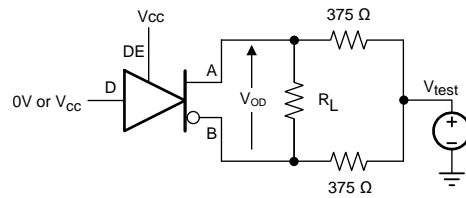


Figure 10. Measurement of Driver Differential Output Voltage With Common-Mode Load

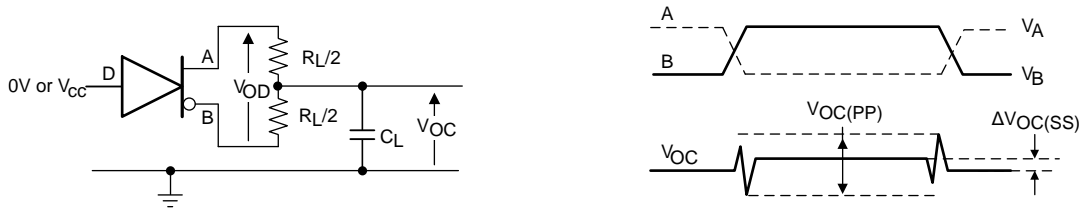


Figure 11. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

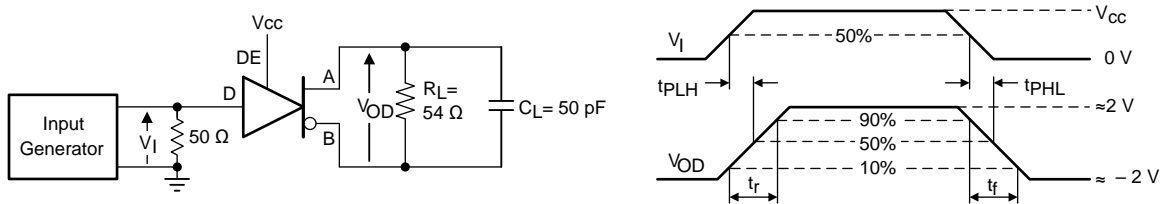


Figure 12. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

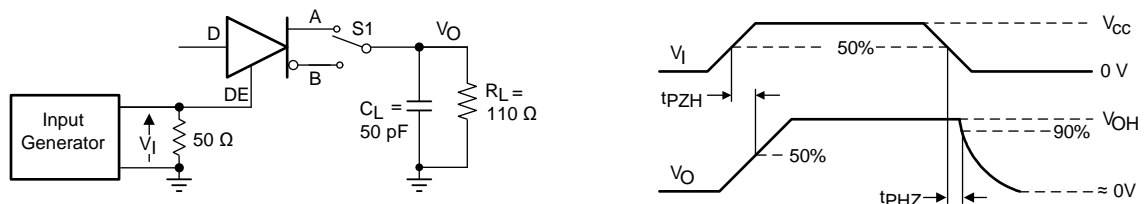


Figure 13. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

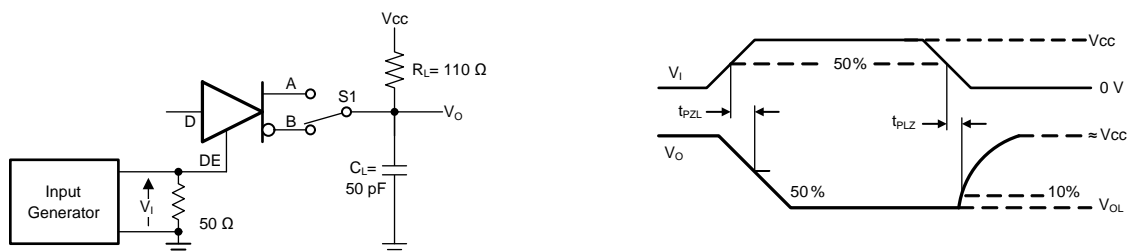
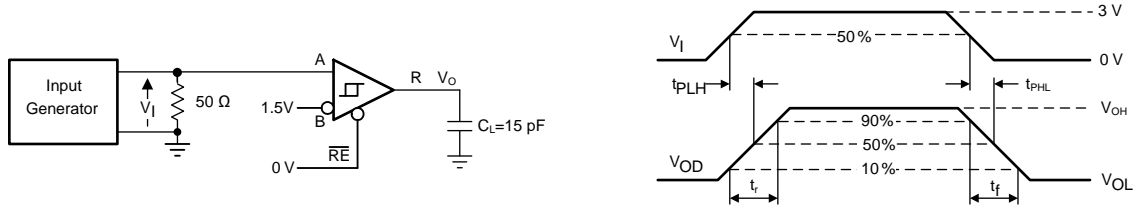
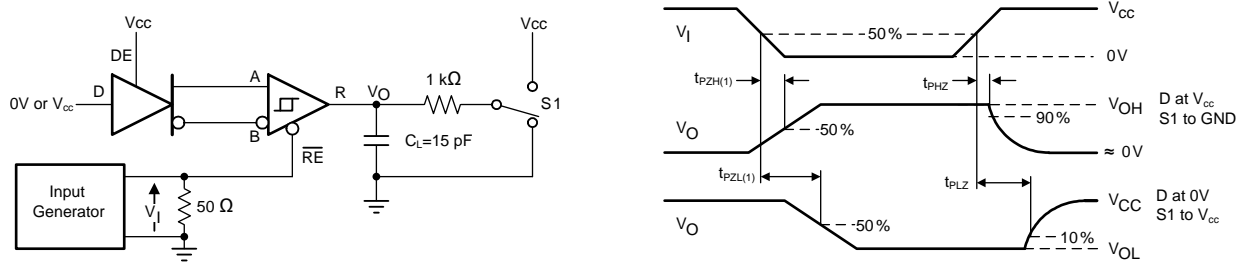


Figure 14. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

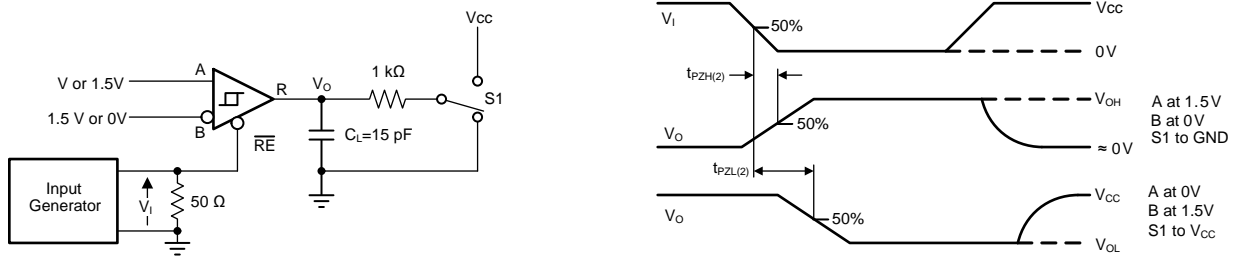
Parameter Measurement Information (continued)



15. Measurement of Receiver Output Rise and Fall Times and Propagation Delays



16. Measurement of Receiver Enable/Disable Times With Driver Enabled



17. Measurement of Receiver Enable Times With Driver Disabled

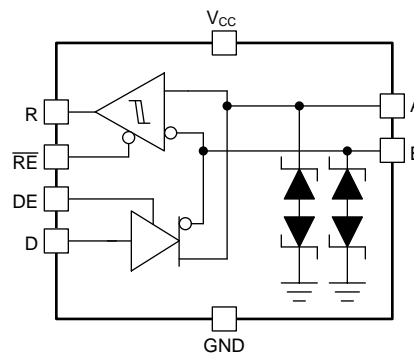
## 9 Detailed Description

### 9.1 Overview

THVD1419 and THVD1429 are surge-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 250 kbps and 20 Mbps respectively. Surge protection is achieved by integrating transient voltage suppresser (TVS) diodes in the standard 8-pin SOIC (D) package.

These devices have active-high driver enables and active-low receiver enables. A standby current of less than 2  $\mu$ A can be achieved by disabling both driver and receiver.

### 9.2 Functional Block Diagrams

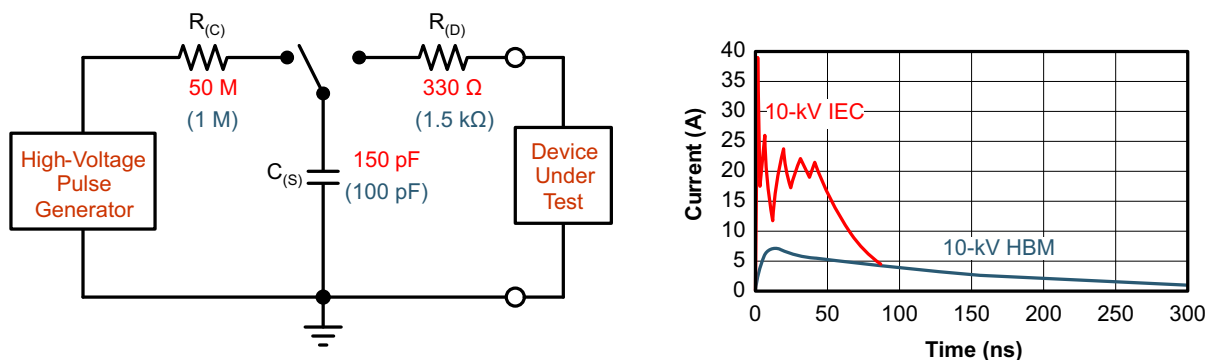


✎ 18. THVD1419 and THVD1429 Block Diagram

### 9.3 Feature Description

#### 9.3.1 Electrostatic Discharge (ESD) Protection

The bus pins of the THVD14x9 transceiver family include on-chip ESD protection against  $\pm 16$ -kV HBM and  $\pm 8$ -kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance,  $C_{(S)}$ , and 78% lower discharge resistance,  $R_{(D)}$ , of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.



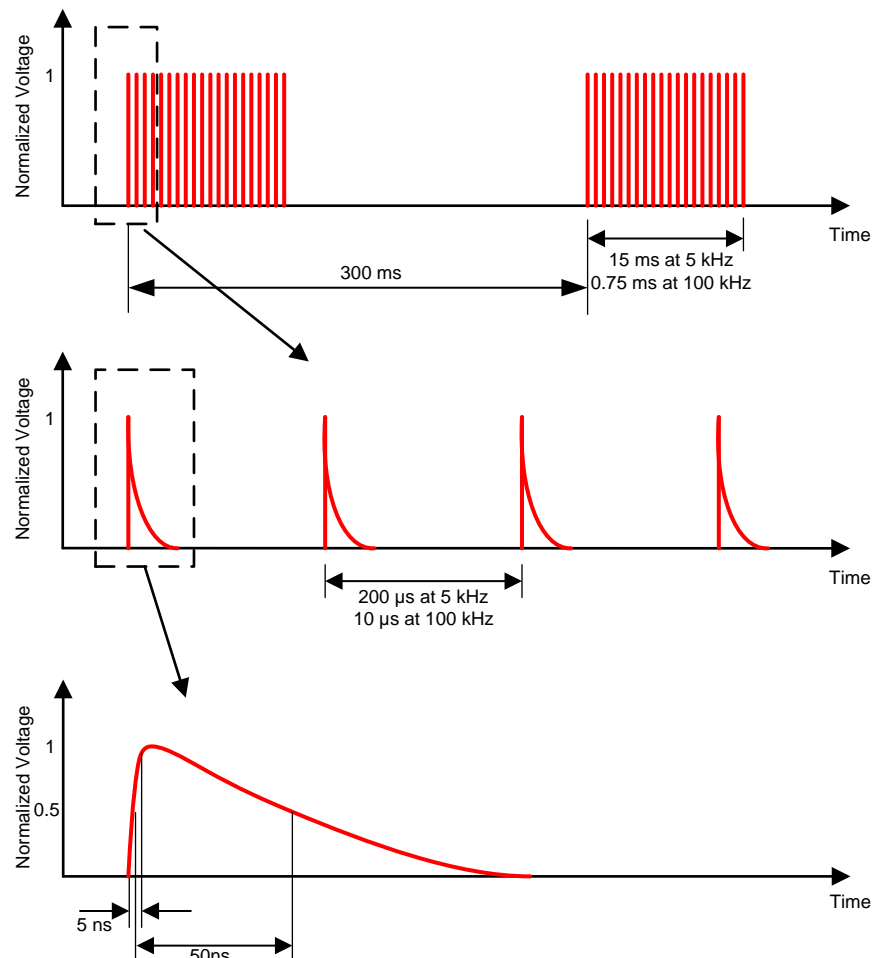
✎ 19. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables.

## Feature Description (continued)

### 9.3.2 Electrical Fast Transient (EFT) Protection

Inductive loads such as relays, switch contactors, or heavy-duty motors can create high-frequency bursts during transition. The IEC 61000-4-4 test is intended to simulate the transients created by such switching of inductive loads on AC power lines. [Figure 20](#) shows the voltage waveforms in to 50- $\Omega$  termination as defined by the IEC standard.



**Figure 20. EFT Voltage Waveforms**

Internal ESD protection circuits of the THVD14x9 protect the transceivers against EFT  $\pm 4$  kV.

### 9.3.3 Surge Protection

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

[Figure 21](#) compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

## Feature Description (continued)

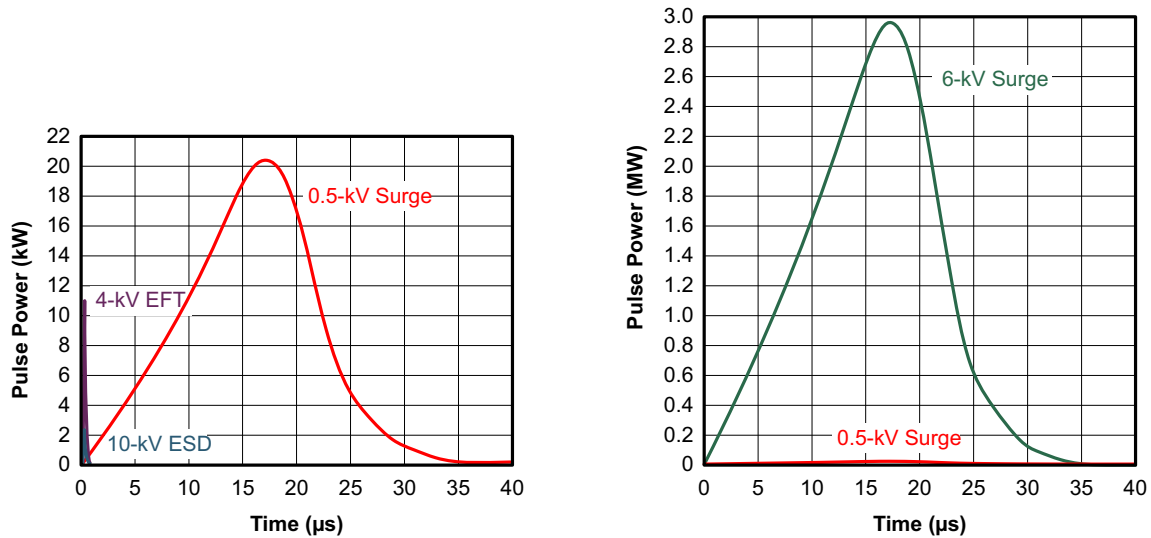


Figure 21. Power Comparison of ESD, EFT, and Surge Transients

Figure 22 shows the test setup used to validate THVD14x9 surge performance according to the IEC 61000-4-5 1.2/50-μs surge pulse.

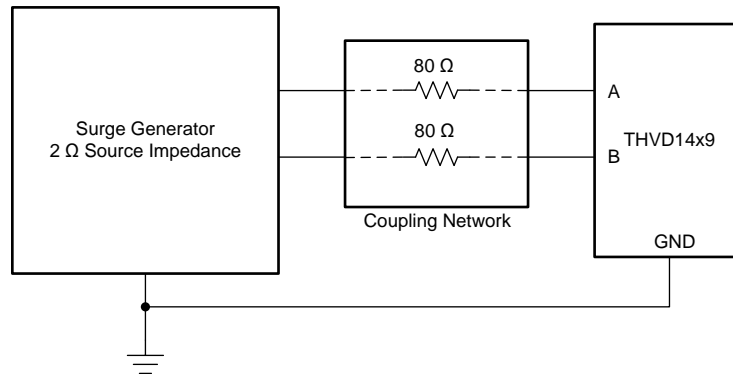


Figure 22. THVD14x9 Surge Test Setup

THVD14x9 product family is robust to  $\pm 2.5$ -kV surge transients without the need for any external components.

### 9.3.4 Failsafe Receiver

The differential receivers of the THVD14x9 family are failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

## 9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as  $V_{OD} = V_A - V_B$  is positive. When D is low, the output states reverse: B turns high, A becomes low, and  $V_{OD}$  is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output A turns high and B turns low.

表 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin,  $\overline{RE}$ , is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_A - V_B$  is higher than the positive input threshold,  $V_{TH+}$ , the receiver output, R, turns high. When  $V_{ID}$  is lower than the negative input threshold,  $V_{TH-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{TH+}$  and  $V_{TH-}$ , the output is indeterminate.

When  $\overline{RE}$  is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output



## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

THVD14x9 are half-duplex RS-485 transceivers with integrated system-level surge protection. Standard 8-pin SOIC (D) package allows drop-in replacement into existing systems and eliminate system-level protection components.

### 10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

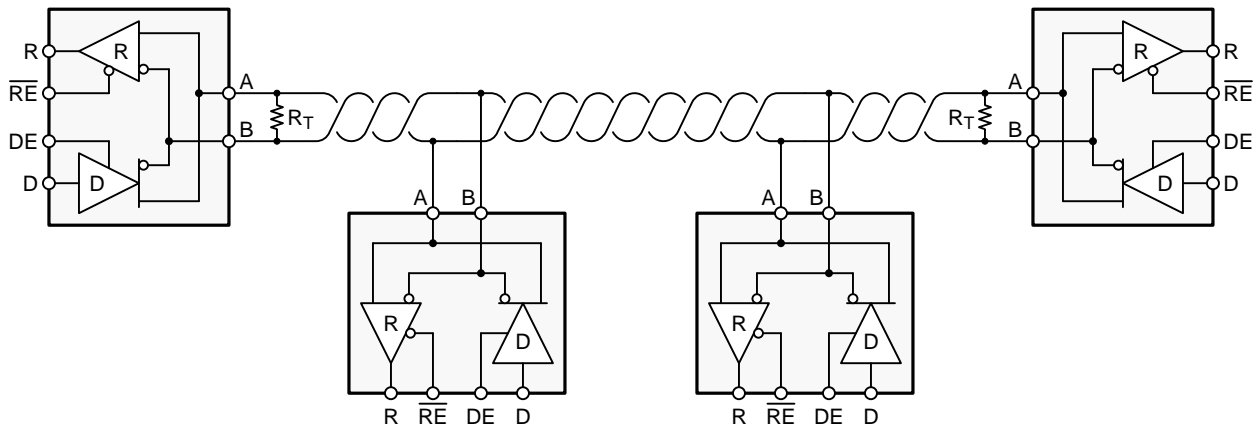


图 23. Typical RS-485 Network With Half-Duplex Transceivers

#### 10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

##### 10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

## Typical Application (continued)

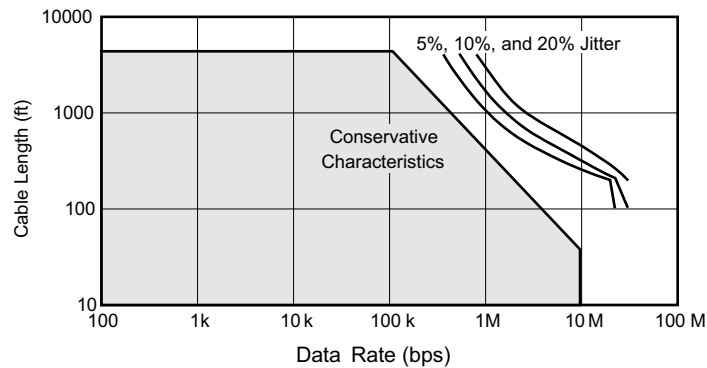


图 24. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 20 Mbps for the THVD1429) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

### 10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{(\text{STUB})} \leq 0.1 \times t_r \times v \times c$$

where

- $t_r$  is the 10/90 rise time of the driver
- $c$  is the speed of light ( $3 \times 10^8$  m/s)
- $v$  is the signal velocity of the cable or trace as a factor of  $c$

(1)

### 10.2.1.3 Bus Loading

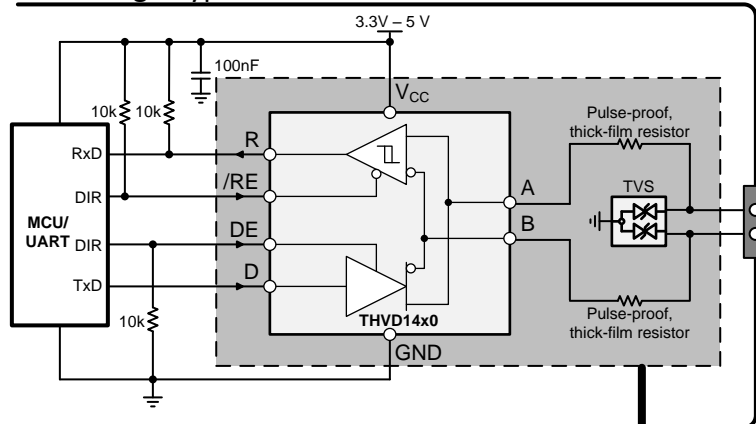
The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 k $\Omega$ . Because the THVD14x9 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

RS-485 transceivers operate in noisy industrial environments typically require surge protection at the bus pins. [Figure 25](#) compares 1-kV surge protection implementation with a regular RS-485 transceiver (such as THVD14x0) against with the THVD14x9. The internal TVS protection of the THVD14x9 achieves  $\pm 2.5$  kV IEC 61000-4-5 surge protection without any additional external components, reducing system level bill of materials.

System level surge protection implementation using a typical RS-485 transceiver



System level surge protection implementation using THVD14x9 transceiver

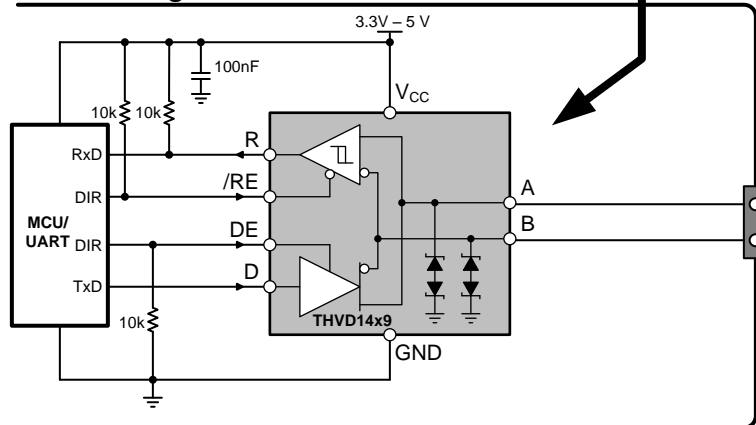
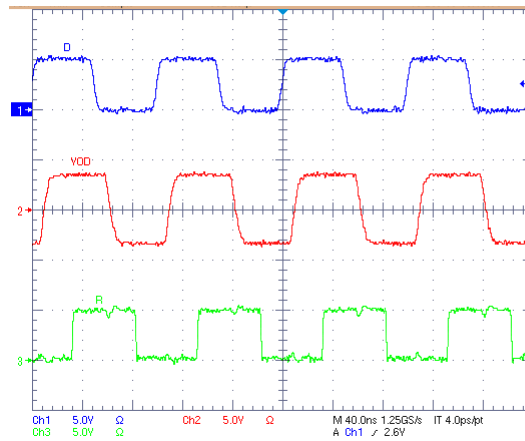


Figure 25. Implementation of System-Level Surge Protection Using THVD14x9

## Typical Application (continued)

### 10.2.3 Application Curves



$V_{CC} = 5\text{ V}$     54- $\Omega$  Termination     $T_A = 25^\circ\text{C}$

图 26. THVD1429 Waveforms at 20 Mbps

## 11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

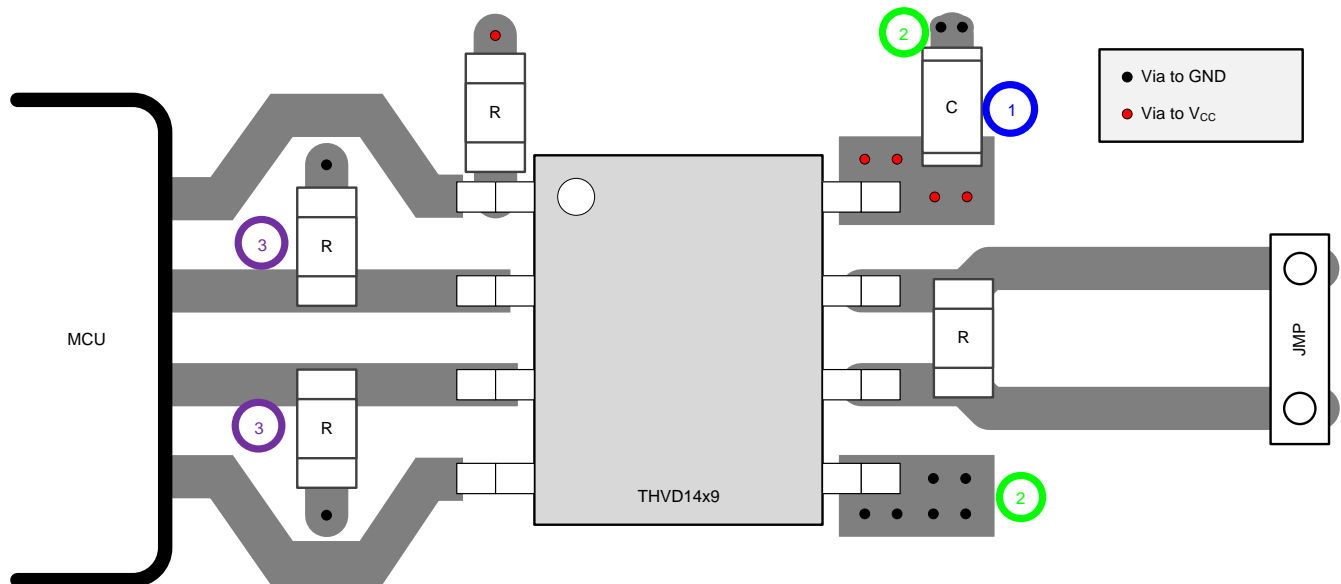
## 12 Layout

### 12.1 Layout Guidelines

Additional external protection components generally are not needed when using THVD14x9 transceivers.

1. Use  $V_{CC}$  and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the  $V_{CC}$  pins of transceiver, UART and/or controller ICs on the board.
2. Use at least two vias for  $V_{CC}$  and ground connections of decoupling capacitors to minimize effective via-inductance.
3. Use 1-k $\Omega$  to 10-k $\Omega$  pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.

### 12.2 Layout Example



27. Half-Duplex Layout Example

## 13 デバイスおよびドキュメントのサポート

### 13.1 デバイス・サポート

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表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
THVD1419	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
THVD1429	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

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### 13.5 コミュニティ・リソース

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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### 13.8 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1419DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1419	<a href="#">Samples</a>
THVD1419DT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1419	<a href="#">Samples</a>
THVD1429DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1429	<a href="#">Samples</a>
THVD1429DT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1429	<a href="#">Samples</a>

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1419DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1419DT	SOIC	D	8	250	177.8	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1429DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1429DT	SOIC	D	8	250	177.8	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1419DR	SOIC	D	8	2500	346.0	346.0	29.0
THVD1419DT	SOIC	D	8	250	213.0	191.0	35.0
THVD1429DR	SOIC	D	8	2500	346.0	346.0	29.0
THVD1429DT	SOIC	D	8	250	213.0	191.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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