

# THVD14xx ±18kV IEC ESD 保護機能搭載、3.3V~5V、RS-485 トランシーバ

## 1 特長

- TIA/EIA-485A 標準の要件に合致、または上回る仕様
- 電源電圧: 3V~5.5V
- 5V電源で差動出力が2.1Vを超えるためPROFIBUSと互換
- バスI/O ESD保護
  - ±30kV HBM
  - ±18kV IEC 61000-4-2接触放電
  - ±25kV IEC 61000-4-2エアギャップ放電
  - ±4kV IEC 61000-4-4高速過渡バースト
- 拡張動作同相範囲 ±15V
- 低EMIで500kbpsおよび50Mbpsのデータレート
- レシーバの大きなヒステリシスによるノイズ除去
- 低消費電力
  - スタンバイ時消費電流: 1µA未満
  - 動作時電流: 3mA未満
- 拡張周囲温度範囲: -40°C~+125°C
- グリッチなしの電源オン/オフによるホット・プラグイン能力
- 開放、短絡、アイドル・バスのフェイルセーフ
- 1/8の単位負荷(最大256のバス・ノード)
- 小型のVSONおよびVSSOPパッケージによる基板面積の削減、またはSOICによりドロップイン互換を実現

## 2 アプリケーション

- モータ駆動
- ファクトリ・オートメーション/制御
- 電力網インフラストラクチャ
- ビルディング・オートメーション
- HVACシステム
- ビデオ監視
- プロセス分析
- ワイヤレス・インフラ

## 3 概要

THVD14xxは、過酷な産業環境で動作するように設計された、ノイズ耐性の高いRS-485/RS-422トランシーバファミリです。これらのデバイスのバス・ピンは、高レベルのIEC電気的高速過渡(EFT)およびIEC静電放電(ESD)事象に対する耐性があるため、システム・レベルの保護部品を追加する必要がありません。

これらの各デバイスは3V~5.5Vの単一電源で動作します。このファミリのデバイスは拡張同相電圧範囲に対応し、長い距離のケーブルを通したマルチポイントのアプリケーションに適しています。

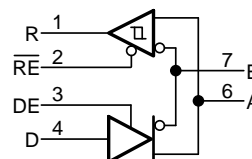
THVD14xxファミリのデバイスは小型のVSONおよびVSSOPパッケージで供給され、スペースに制約のあるアプリケーションで使用できます。このデバイスは、-40°C~125°Cの周囲自由通気温度範囲で仕様が規定されています。

### 製品情報<sup>(1)</sup>

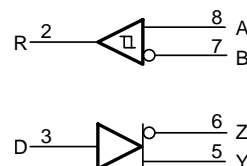
型番	パッケージ	本体サイズ(公称)
THVD1410	VSSOP (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
THVD1450	VSON (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
THVD1451	VSON (8)	3.00mm×3.00mm
	SOIC (8)	4.90mm×3.91mm
THVD1452	VSSOP (10)	3.00mm×3.00mm
	SOIC (14)	8.65mm×3.91mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

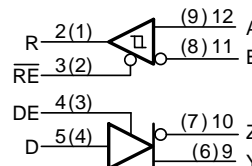
### THVD1410およびTHVD1450の概略回路図



### THVD1451の概略回路図



### THVD1452の概略回路図



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## 4 改訂履歴

### Revision D (March 2019) から Revision E に変更 Page

•	THVD1451 を「製品プレビュー」から「量産データ」に変更	1
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### Revision C (February 2019) から Revision D に変更 Page

•	THVD1410 を「製品プレビュー」から「量産データ」に変更	1
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### Revision B (December 2018) から Revision C に変更 Page

•	THVD1452 を「製品プレビュー」から「量産データ」に変更	1
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### Revision A (May 2018) から Revision B に変更 Page

•	「特長」に「5V電源で差動出力が2.1Vを超え...」を追加	1
•	「特長」の「±18kV IEC 61000-4-2エアギャップ放電」を「±25kV IEC 61000-4-2エアギャップ放電」に変更	1
•	THVD1451にSOIC (8)パッケージを追加	1
•	Added Thermal Pad to the THVD1450 DRB package	5
•	Added Thermal Pad to the THVD1451 DRB package	6
•	Changed all pins HBM ESD rating from 4 kV to 8 kV	8
•	Changed IEC ESD air-gap discharge rating from 18 kV to 25 kV	8
•	Changed THVD1410 power dissipation numbers	9
•	Changed THVD1410 driver $t_r$ , $t_f$ TYP from 400 ns to 460 ns and MAX from 600 ns to 680 ns	11
•	Changed THVD1410 receiver $t_r$ , $t_f$ TYP from 13 ns to 10 ns	11
•	Changed THVD1410 receiver $t_{PHL}$ , $t_{PLH}$ TYP from 60 ns to 35 ns	11
•	Added Typical Characteristics, THD1450D	14

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• Added condition to <a href="#">Figure 8</a> to <a href="#">Figure 3</a> .....	14
• Added Typical Characteristics, THD1410.....	15
• Changed A to A/Y and B to B/Z in <a href="#">Figure 20</a> to <a href="#">Figure 24</a> .....	16
• Added 3rd paragraph to the <i>Overview</i> section .....	18

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2017年11月発行のものから更新

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• ドキュメントのステータスを「事前情報」から「量産混在」データに変更.....	1
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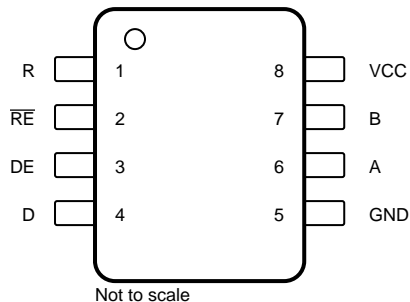
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## 5 Device Comparison Table

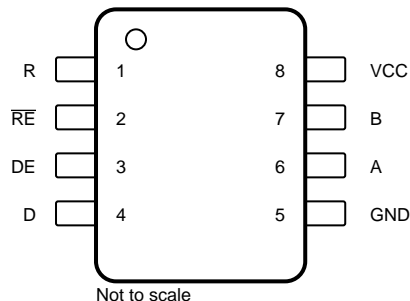
PART NUMBER	DUPLEX	ENABLES	SIGNALING RATE	NODES
THVD1410	Half	DE, $\overline{RE}$	up to 500 kbps	256
THVD1450	Half	DE, $\overline{RE}$	up to 50 Mbps	
THVD1451	Full	None		
THVD1452	Full	DE, $\overline{RE}$		

## 6 Pin Configuration and Functions

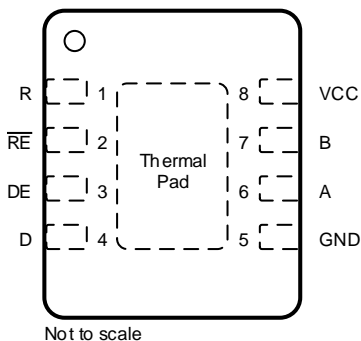
THVD1410, THVD1450 Devices  
8-Pin D Package (SOIC)  
Top View



THVD1410, THVD1450 Devices  
8-Pin DGK Package (VSSOP)  
Top View

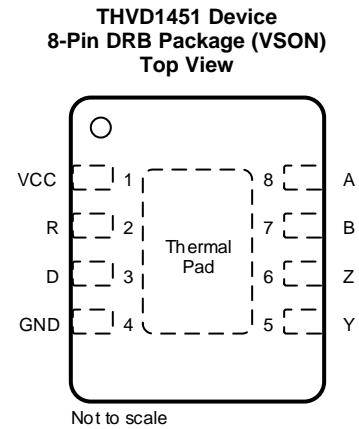
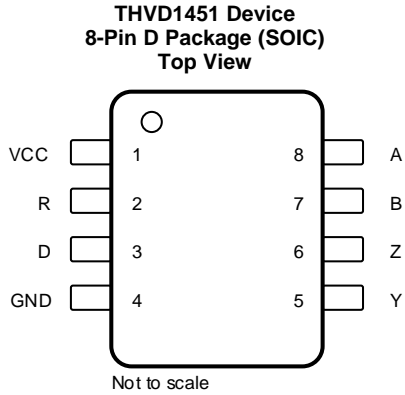


THVD1450 Device  
8-Pin DRB Package (VSON)  
Top View



### Pin Functions

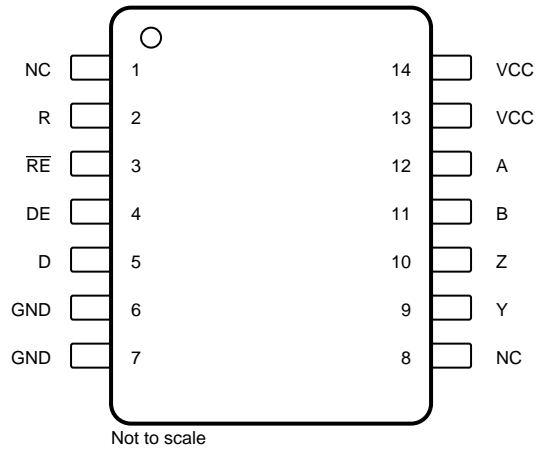
NAME	PIN			I/O	DESCRIPTION
	D	DGK	DRB		
A	6	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	4	4	Digital input	Driver data input
DE	3	3	3	Digital input	Driver enable, active high (2-M $\Omega$ internal pull-down)
GND	5	5	5	Ground	Device ground
R	1	1	1	Digital output	Receive data output
V <sub>CC</sub>	8	8	8	Power	3.3-V to 5-V supply
RE	2	2	2	Digital input	Receiver enable, active low (2-M $\Omega$ internal pull-up)
Thermal Pad	—	—		I/O	No electrical connection. Should be connected to GND for optimal thermal performance.



### Pin Functions

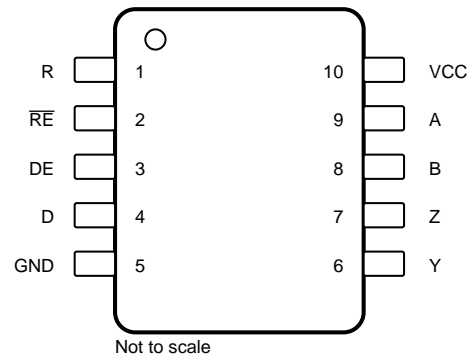
NAME	PIN		I/O	Description
	D	DRB		
A	8	8	Bus input	Bus input, A (complementary to B)
B	7	7	Bus input	Bus input, B (complementary to A)
D	3	3	Digital input	Driver data input
GND	4	4	Ground	Device ground
R	2	2	Digital output	Receive data output
V <sub>CC</sub>	1	1	Power	3.3-V to 5-V supply
Y	5	5	Bus output	Digital bus output, Y (Complementary to Z)
Z	6	6	Bus output	Digital bus output, Z (Complementary to Y)
Thermal Pad	—		I/O	No electrical connection. Should be connected to GND for optimal thermal performance.

THVD1452 Device  
14-Pin D Package (SOIC)  
Top View



NC – No internal connection

THVD1452 Device  
10-Pin DGS Package (VSSOP)  
Top View



Not to scale

### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D	DGS		
A	12	9	Bus input	Bus input, A (complementary to B)
B	11	8	Bus input	Bus input, B (complementary to A)
D	5	4	Digital input	Driver data input
DE	4	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	6, 7 <sup>(1)</sup>	5	Ground	Device ground
NC	1, 8	—	—	Internally not connected
R	2	1	Digital output	Receive data output
V <sub>CC</sub>	13, 14 <sup>(1)</sup>	10	Power	3.3-V to 5-V supply
Y	9	6	Bus output	Digital bus output, Y (Complementary to Z)
Z	10	7	Bus output	Digital bus output, Z (Complementary to Y)
RE	3	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)

(1) These pins are internally connected

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	$V_{CC}$	-0.5	7	V
Bus voltage	Range at any bus pin (A, B, Y, or Z) as differential or common-mode with respect to GND	-18	18	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$ )	-0.3	5.7	V
Receiver output current	$I_O$	-24	24	mA
Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Bus pins and GND	±30	kV
			All other pins	±8	kV
		Charged device model (CDM), per JEDEC JESD22-C101 <sup>(2)</sup>	All pins	±1.5	kV
		Machine model (MM), per JEDEC JESD22-A115-A	All pins	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 ESD Ratings [IEC]

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus pins and GND	±18	kV
		Air-gap discharge, per IEC 61000-4-2	Bus pins and GND	±25	kV
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus pins and GND	±4	kV



## 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		5.5	V
V <sub>I</sub>	Input voltage at any bus terminal <sup>(1)</sup>	-15		15	V
V <sub>IH</sub>	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V <sub>ID</sub>	Differential input voltage	-15		15	V
I <sub>O</sub>	Output current, driver	-60		60	mA
I <sub>OR</sub>	Output current, receiver	-8		8	mA
R <sub>L</sub>	Differential load resistance	54			Ω
1/t <sub>UI</sub>	Signaling rate: THVD1410			500	kbps
1/t <sub>UI</sub>	Signaling rate: THVD1450, THVD1451, THVD1452			50	Mbps
T <sub>A</sub>	Operating ambient temperature	-40		125	°C
T <sub>J</sub>	Junction temperature	-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 7.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		THVD1410 THVD1450 THVD1451	THVD1452	THVD1410 THVD1450	THVD1452	THVD1450 THVD1451	UNIT
		D (SOIC)	D (SOIC)	DGK (VSSOP)	DGS (VSSOP)	DRB (VSON)	
		8 PINS	14 PINS	8 PINS	10 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	114.3	86.4	155.2	155.6	48.6	°C/W
R <sub>θJC(to p)</sub>	Junction-to-case (top) thermal resistance	56.7	43.7	47.2	49.3	49.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	57.7	42.5	76.1	77.1	21.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	12.8	10.2	3.9	4.5	0.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	57	42.2	74.8	75.7	21.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Power Dissipation

PARAMETER	Description	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 125°C, 50% duty cycle square wave at 500kbps signaling rate, THVD1410	Unterminated: R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF		360		mW
		RS-422 load: R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF		370		mW
		RS-485 load: R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF		410		mW
	Driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 125°C, 50% duty cycle square wave at 50Mbps signaling rate, THVD145x devices	Unterminated: R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF		360		mW
		RS-422 load: R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF		320		mW
		RS-485 load: R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF		330		mW

## 7.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of  $V_{CC} = 5\text{ V}$ .

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>Driver</b>							
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60\ \Omega$ , $-15\text{ V} \leq V_{\text{test}} \leq 15\text{ V}$ (See <a href="#">20</a> ) <sup>(1)</sup>		1.5	3.5		V
		$R_L = 60\ \Omega$ , $-15\text{ V} \leq V_{\text{test}} \leq 15\text{ V}$ , $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ , (See <a href="#">20</a> )		2.1			V
		$R_L = 100\ \Omega$ (See <a href="#">21</a> )		2	4		V
		$R_L = 54\ \Omega$ (See <a href="#">21</a> )		1.5	3.5		V
$\Delta V_{OD} $	Change in differential output voltage			-200		200	mV
$V_{OC}$	Common-mode output voltage	$R_L = 54\ \Omega$ (See <a href="#">21</a> )		1	$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
$I_{OS}$	Short-circuit output current	$DE = V_{CC}$ , $-7\text{ V} \leq V_O \leq 12\text{ V}$		-250		250	mA
<b>Receiver</b>							
$I_i$	Bus input current	$DE = 0\text{ V}$ , $V_{CC} = 0\text{ V}$ or $5.5\text{ V}$	$V_i = 12\text{ V}$		50	125	$\mu\text{A}$
			$V_i = -7\text{ V}$	-100	-65		$\mu\text{A}$
		$DE = 0\text{ V}$ , $V_{CC} = 0\text{ V}$ or $5.5\text{ V}$	$V_i = 15\text{ V}$		60	125	$\mu\text{A}$
			$V_i = -15\text{ V}$	-200	-130		$\mu\text{A}$
$V_{TH+}$	Positive-going input threshold voltage			See <sup>(2)</sup>	-100	-20	mV
$V_{TH-}$	Negative-going input threshold voltage	Over common-mode range of $\pm 15\text{ V}$		-200	-130	See <sup>(2)</sup>	mV
$V_{HYS}$	Input hysteresis				30		mV
$V_{OH}$	Output high voltage	$I_{OH} = -8\text{ mA}$		$V_{CC} - 0.4$	$V_{CC} - 0.2$		V
$V_{OL}$	Output low voltage	$I_{OL} = 8\text{ mA}$			0.2	0.4	V
$I_{OZR}$	Output high-impedance current	$V_O = 0\text{ V}$ or $V_{CC}$ , $\overline{RE} = V_{CC}$		-1		1	$\mu\text{A}$
<b>Logic</b>							
$I_{IN}$	Input current (D, DE, $\overline{RE}$ )	$3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ , $0\text{ V} \leq V_{IN} \leq V_{CC}$		-6.2		6.2	$\mu\text{A}$
<b>Device</b>							
$I_{CC}$	Supply current (quiescent)	Driver and receiver enabled	$\overline{RE} = 0\text{ V}$ , $DE = V_{CC}$ , No load		2.4	3	mA
		Driver enabled, receiver disabled	$\overline{RE} = V_{CC}$ , $DE = V_{CC}$ , No load		2	2.5	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0\text{ V}$ , $DE = 0\text{ V}$ , No load		700	960	$\mu\text{A}$
		Driver and receiver disabled	$\overline{RE} = V_{CC}$ , $DE = 0\text{ V}$ , D = open, No load		0.1	1	$\mu\text{A}$
$T_{SD}$	Thermal shutdown temperature				170		°C

(1)  $|V_{OD}| \geq 1.4\text{ V}$  when  $T_A > 85\text{ }^\circ\text{C}$ ,  $V_{\text{test}} < -7\text{ V}$  and  $V_{CC} < 3.135\text{ V}$ .

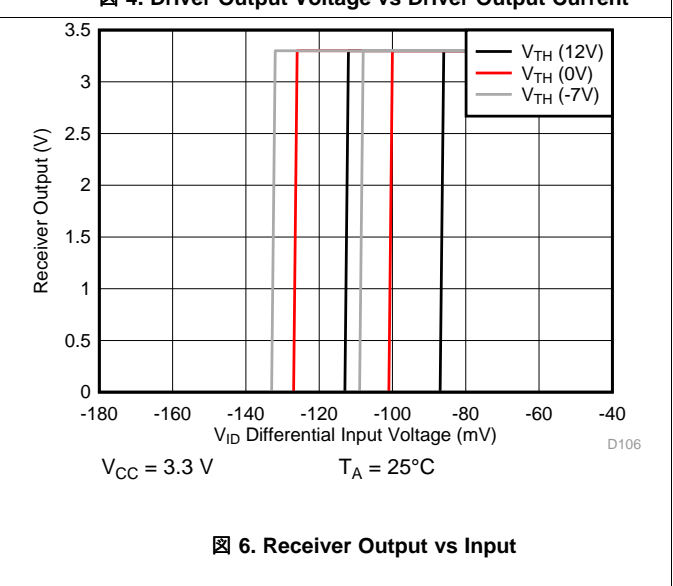
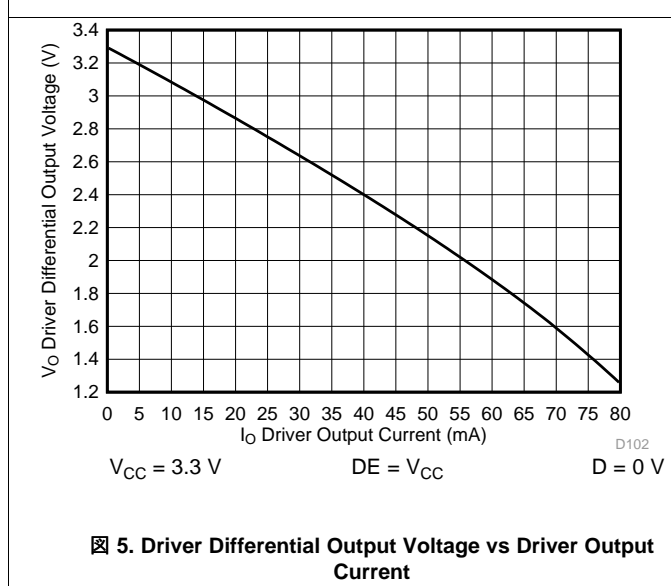
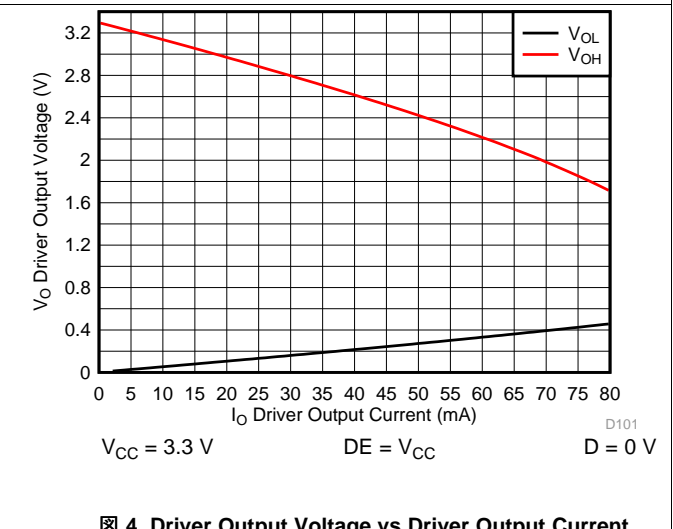
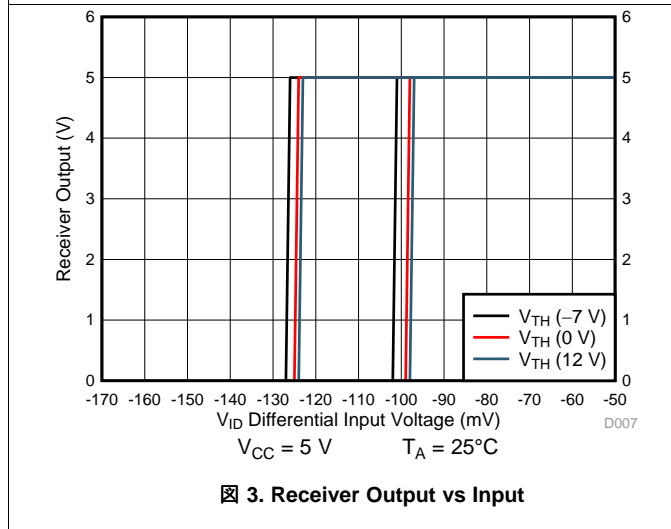
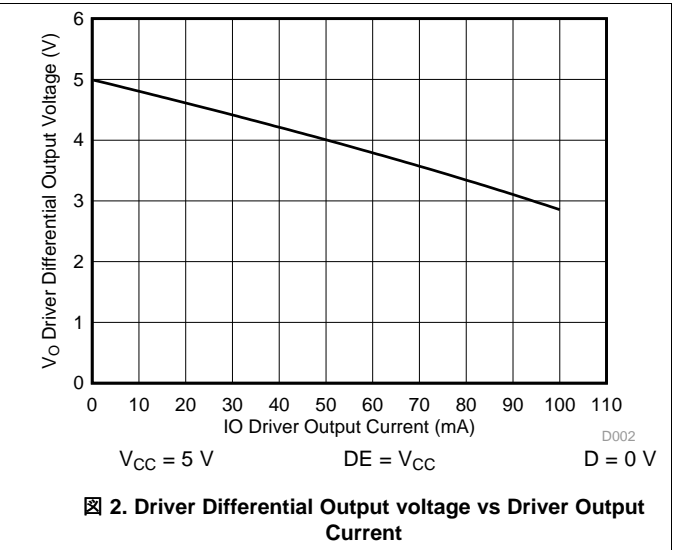
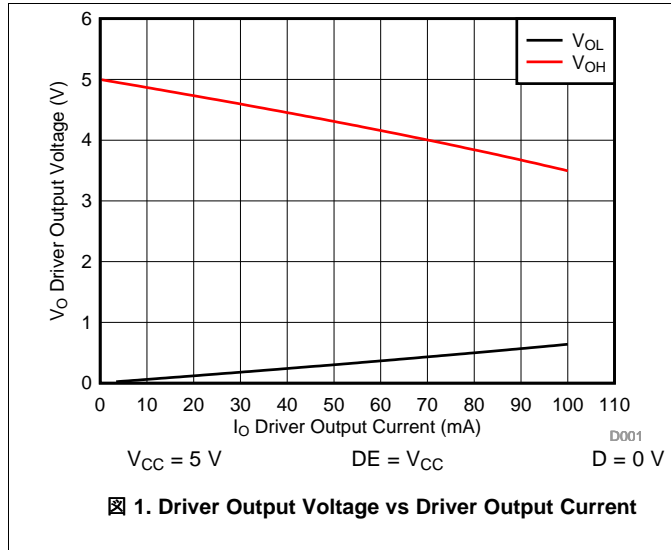
(2) Under any specific conditions,  $V_{TH+}$  is assured to be at least  $V_{HYS}$  higher than  $V_{TH-}$ .

## 7.8 Switching Characteristics

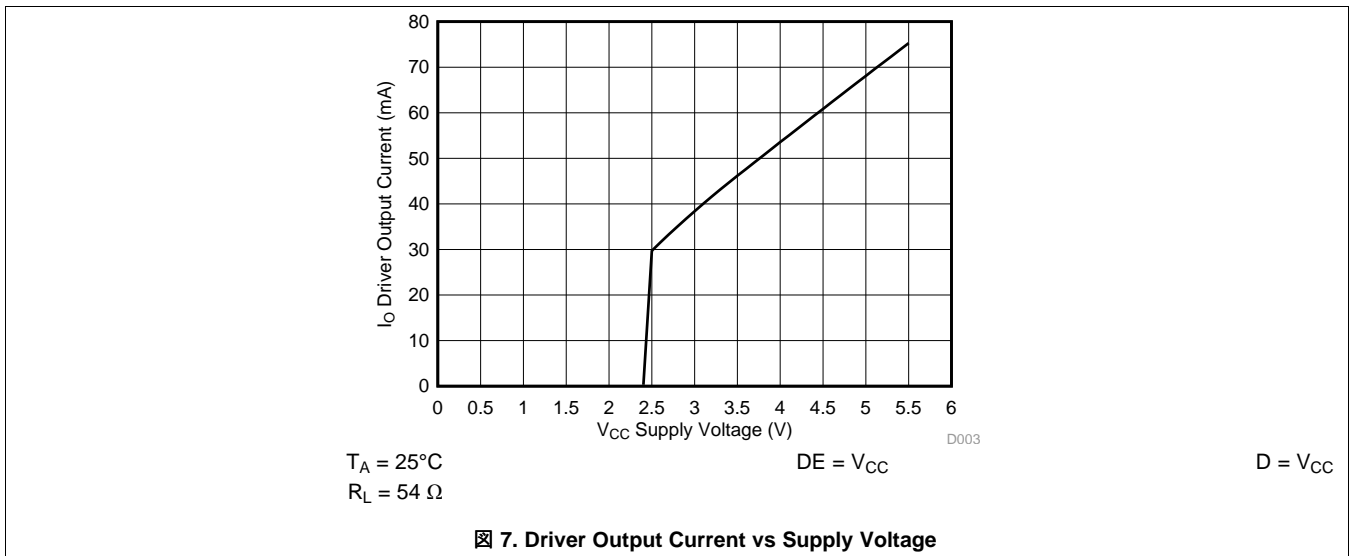
over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of  $V_{CC} = 5\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>Driver: THVD1410</b>							
$t_r, t_f$	Differential output rise/fall time	$R_L = 54\ \Omega, C_L = 50\ \text{pF}$ , See <a href="#">22</a>	250	460	680	ns	
$t_{PHL}, t_{PLH}$	Propagation delay			250	500	ns	
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				10	ns	
$t_{PHZ}, t_{PLZ}$	Disable time			80	200	ns	
$t_{PZH}, t_{PZL}$	Enable time	$\overline{RE} = 0\text{ V}$ , See <a href="#">23</a> and <a href="#">24</a>		100	600	ns	
		$\overline{RE} = V_{CC}$ , See <a href="#">23</a> and <a href="#">24</a>		4	11	$\mu\text{s}$	
<b>Receiver: THVD1410</b>							
$t_r, t_f$	Output rise/fall time	$C_L = 15\ \text{pF}$ , See <a href="#">25</a>		10	20	ns	
$t_{PHL}, t_{PLH}$	Propagation delay			35	110	ns	
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				7	ns	
$t_{PHZ}, t_{PLZ}$	Disable time			30	60	ns	
$t_{PZH(1)}, t_{PZL(1)}, t_{PZH(2)}, t_{PZL(2)}$	Enable time	$DE = V_{CC}$ , See <a href="#">26</a>		60	140	ns	
		$DE = 0\text{ V}$ , See <a href="#">27</a>		6	14	$\mu\text{s}$	
<b>Driver: THVD1450, THVD1451, THVD1452</b>							
$t_r, t_f$	Differential output rise/fall time	$R_L = 54\ \Omega, C_L = 50\ \text{pF}$ , See <a href="#">22</a>	1	3	6	ns	
$t_{PHL}, t_{PLH}$	Propagation delay			3	10	20	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				3.5	ns	
$t_{PHZ}, t_{PLZ}$	Disable time			15	25	ns	
$t_{PZH}, t_{PZL}$	Enable time	$\overline{RE} = 0\text{ V}$ , See <a href="#">23</a> and <a href="#">24</a>		20	50	ns	
		$\overline{RE} = V_{CC}$ , See <a href="#">23</a> and <a href="#">24</a>		2.5	10	$\mu\text{s}$	
<b>Receiver: THVD1450, THVD1451, THVD1452</b>							
$t_r, t_f$	Output rise/fall time	$C_L = 15\ \text{pF}$ , See <a href="#">25</a>		2	6	ns	
$t_{PHL}, t_{PLH}$	Propagation delay			25	40	ns	
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				3.5	ns	
$t_{PHZ}, t_{PLZ}$	Disable time			14	28	ns	
$t_{PZH(1)}, t_{PZL(1)}, t_{PZH(2)}, t_{PZL(2)}$	Enable time	$DE = V_{CC}$ , See <a href="#">26</a>		50	110	ns	
		$DE = 0\text{ V}$ , See <a href="#">27</a>		4	14	$\mu\text{s}$	

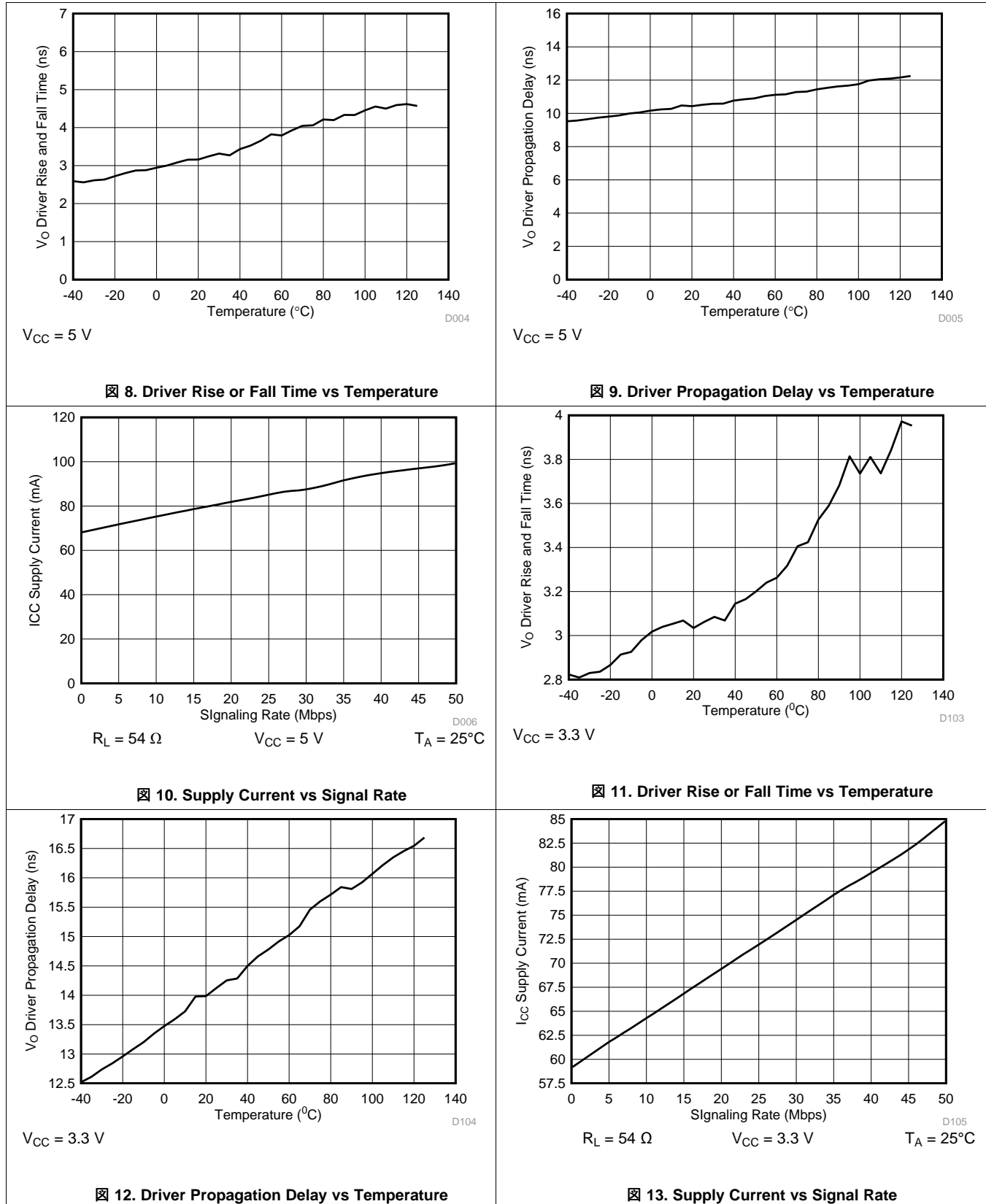
## 7.9 Typical Characteristics: All Devices



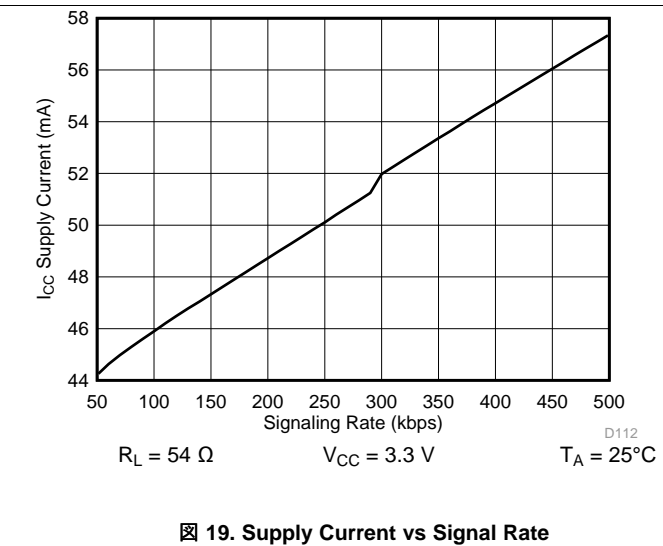
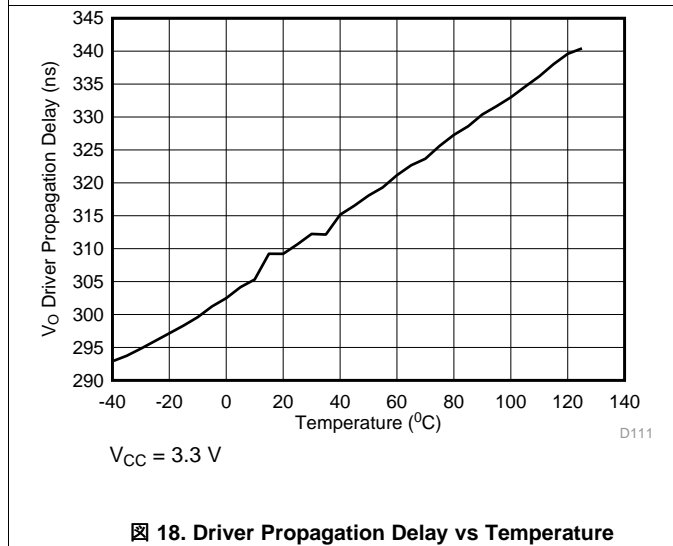
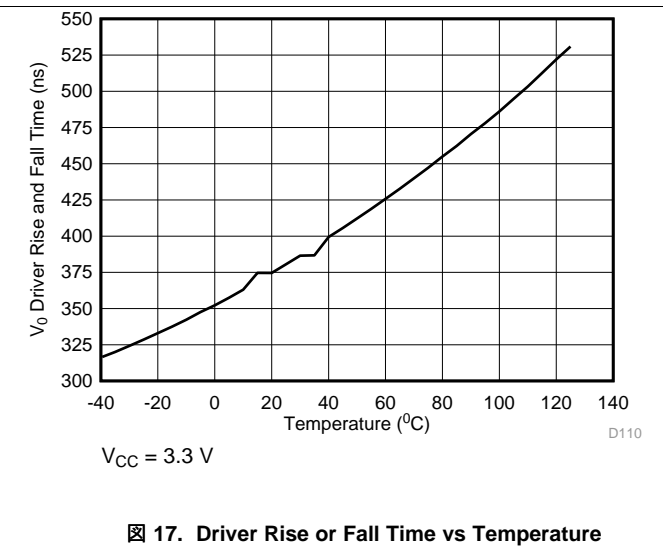
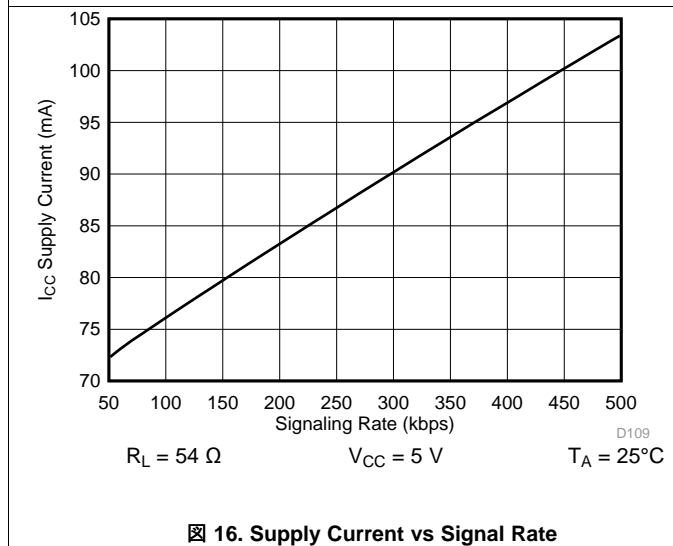
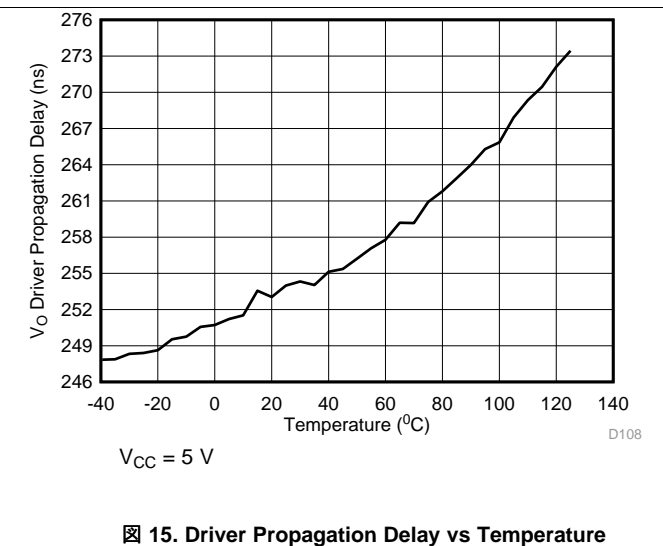
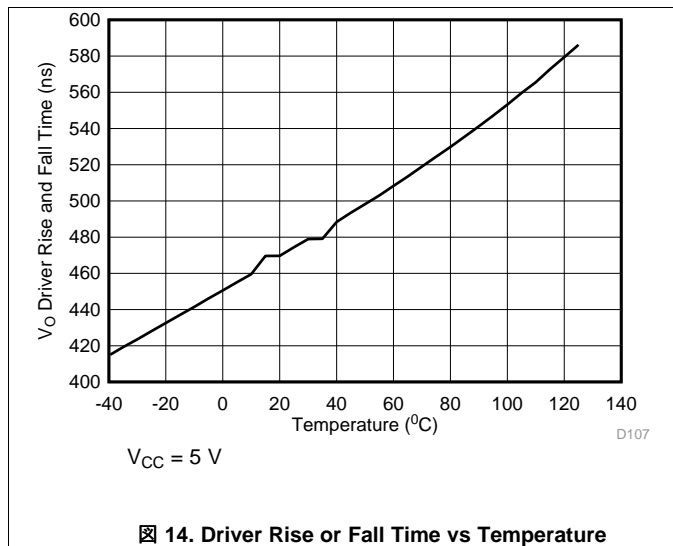
**Typical Characteristics: All Devices (continued)**



### 7.10 Typical Characteristics: THD1450, THVD1451 and THVD1452



### 7.11 Typical Characteristics: THVD1410



## 8 Parameter Measurement Information

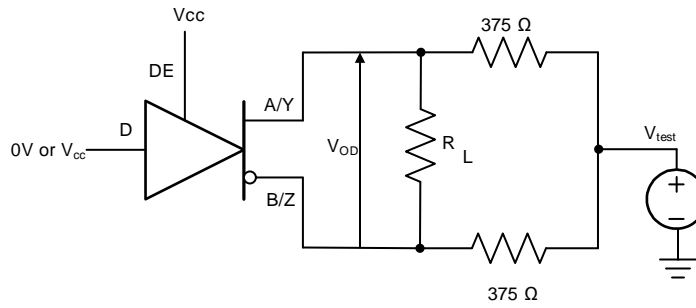


Figure 20. Measurement of Driver Differential Output Voltage With Common-Mode Load

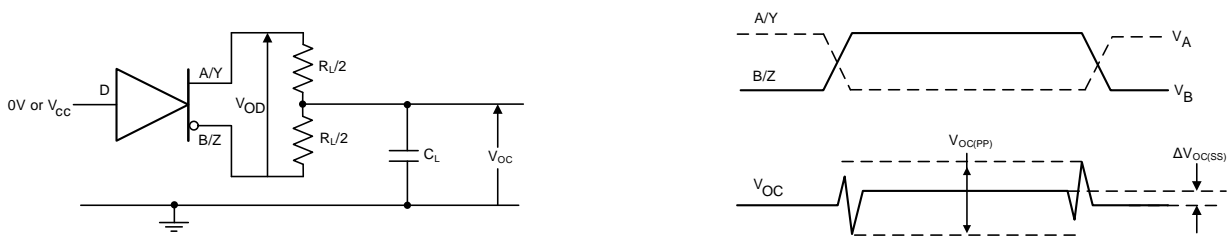


Figure 21. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

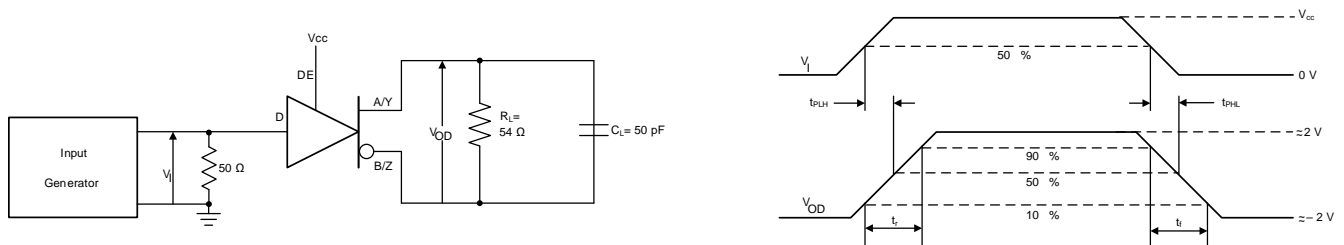


Figure 22. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

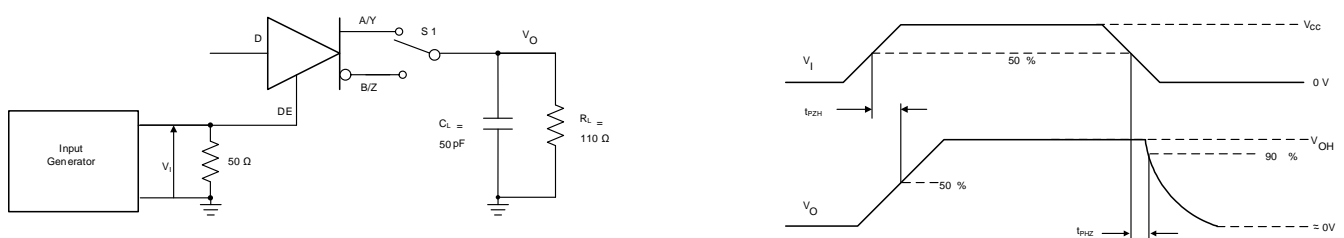


Figure 23. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load



Parameter Measurement Information (continued)

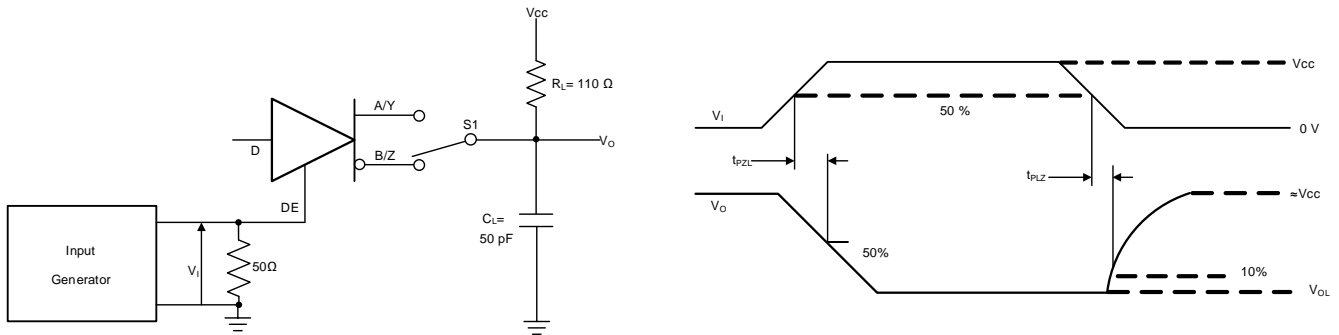


Figure 24. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

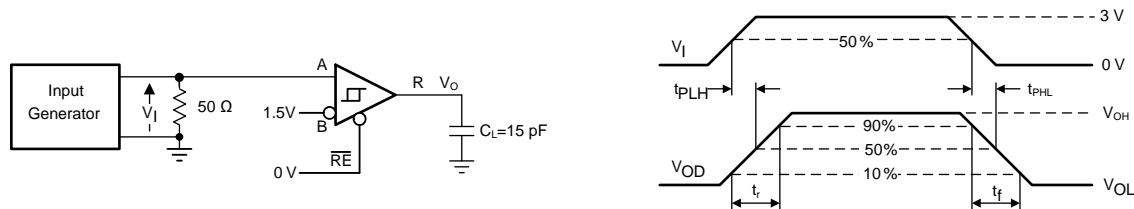


Figure 25. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

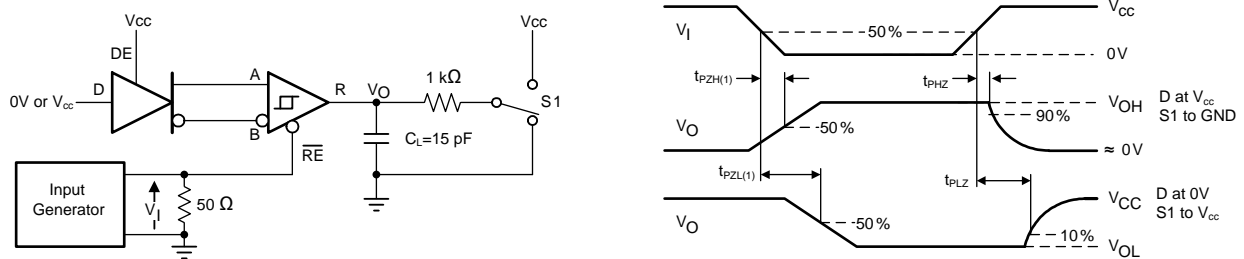


Figure 26. Measurement of Receiver Enable/Disable Times With Driver Enabled

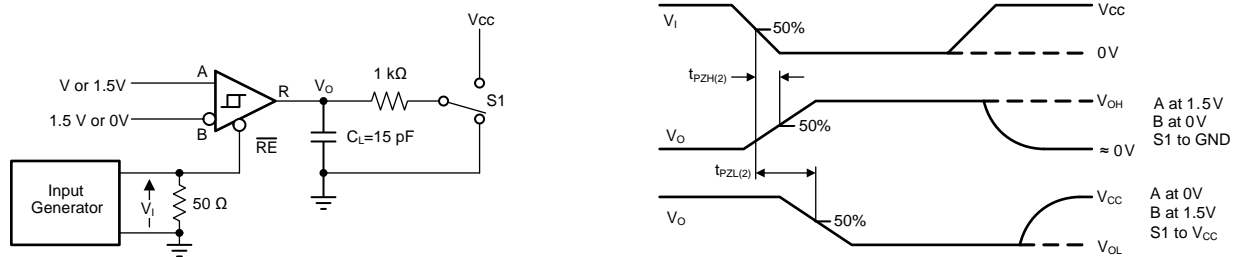


Figure 27. Measurement of Receiver Enable Times With Driver Disabled

## 9 Detailed Description

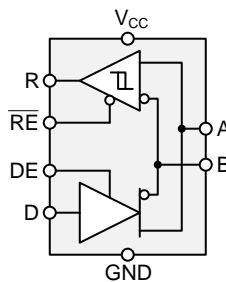
### 9.1 Overview

THVD1410 and THVD1450 are low-power, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 500 kbps and 50 Mbps respectively.

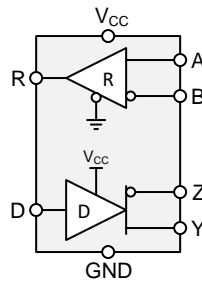
THVD1451 is fully enabled with no external enabling pins. THVD1452 has active-high driver enable and active-low receiver enable. A standby current of less than 1  $\mu\text{A}$  can be achieved by disabling both driver and receiver.

THVD14xx family of devices have a higher typical differential output voltage ( $V_{OD}$ ) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1 V is specified with  $V_{CC}$  voltage of 5 V  $\pm 10\%$  to meet the requirements of PROFIBUS applications.

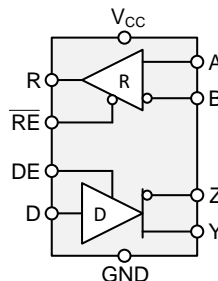
### 9.2 Functional Block Diagrams



☒ 28. THVD1410 and THVD1450



☒ 29. THVD1451



☒ 30. THVD1452

### 9.3 Feature Description

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to  $\pm 18$  kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to  $\pm 4$  kV. With careful system design, one could achieve  $\pm 4$  kV EFT Criterion A (no data loss when transient noise is present).

The THVD14xx device family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. The receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide ambient temperature range from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 9.4 Device Functional Modes

#### 9.4.1 Device Functional Modes for THVD1410 and THVD1450

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as  $V_{OD} = V_A - V_B$  is positive. When D is low, the output states reverse: B turns high, A becomes low, and  $V_{OD}$  is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output A turns high and B turns low.

**表 1. Driver Function Table for THVD1410 and THVD1450**

INPUT	ENABLE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin,  $\overline{\text{RE}}$ , is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_A - V_B$  is higher than the positive input threshold,  $V_{TH+}$ , the receiver output, R, turns high. When  $V_{ID}$  is lower than the negative input threshold,  $V_{TH-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{TH+}$  and  $V_{TH-}$ , the output is indeterminate.

When  $\overline{\text{RE}}$  is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

**表 2. Receiver Function Table for THVD1410 and THVD1450**

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{\text{RE}}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

### 9.4.2 Device Functional Modes for THVD1451

For this device, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input D at all times. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as  $V_{OD} = V_Y - V_Z$  is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and VOD is negative. The D pin has an internal pull-up resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output Y turns high and Z turns low.

表 3. Driver Function Table for THVD1451

INPUT	OUTPUTS		FUNCTIONS
	Y	Z	
H	H	L	Actively drive bus high
L	L	H	Actively drive bus low
OPEN	H	L	Actively drive bus High by default

When the differential input voltage defined as  $V_{ID} = V_A - V_B$  is higher than the positive input threshold,  $V_{TH+}$ , the receiver output, R, turns high. When  $V_{ID}$  is less than the negative input threshold,  $V_{TH-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{TH+}$  and  $V_{TH-}$  the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 4. Receiver Function Table for THVD1451

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	R	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

### 9.4.3 Device Functional Modes for THVD1452

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as  $V_{OD} = V_Y - V_Z$  is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and  $V_{OD}$  is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to  $V_{CC}$ , thus, when left open while the driver is enabled, output Y turns high and Z turns low.

**表 5. Driver Function Table for THVD1452**

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin,  $\overline{RE}$ , is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_A - V_B$  is higher than the positive input threshold,  $V_{TH+}$ , the receiver output, R, turns high. When  $V_{ID}$  is lower than the negative input threshold,  $V_{TH-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{TH+}$  and  $V_{TH-}$ , the output is indeterminate.

When  $\overline{RE}$  is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

**表 6. Receiver Function Table for THVD1452**

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The THVD14xx family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

### 10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

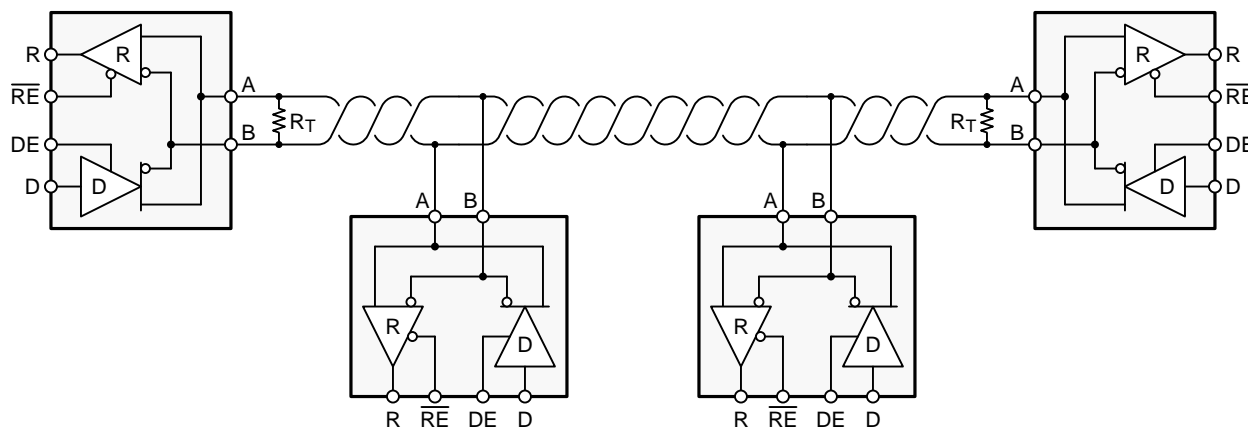


图 31. Typical RS-485 Network With Half-Duplex Transceivers

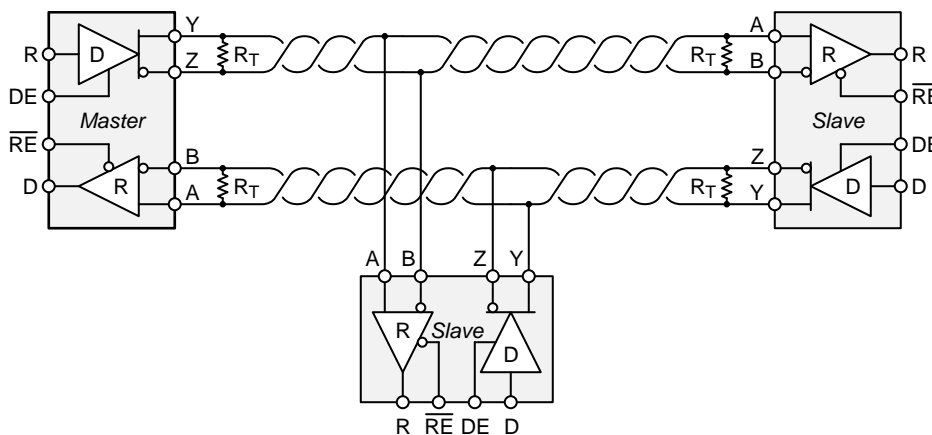


图 32. Typical RS-485 Network With Full-Duplex Transceivers

## Typical Application (continued)

### 10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

#### 10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

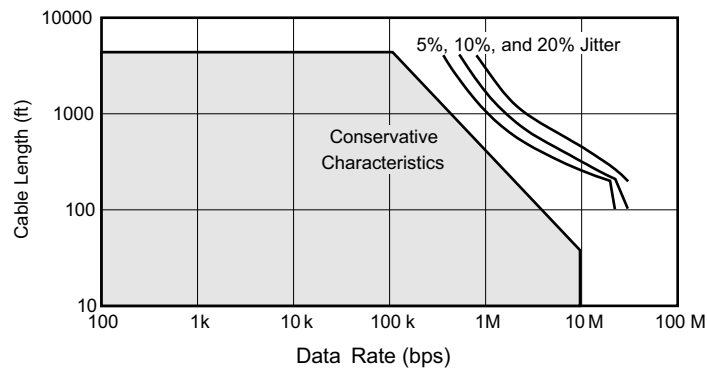


Figure 33. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD1450, THVD1451 and THVD1452) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

#### 10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c$$

where

- $t_r$  is the 10/90 rise time of the driver
- $c$  is the speed of light ( $3 \times 10^8$  m/s)
- $v$  is the signal velocity of the cable or trace as a factor of  $c$

(1)

#### 10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD14xx family consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

## Typical Application (continued)

### 10.2.1.4 Receiver Failsafe

The differential receivers of the THVD14xx family are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input  $V_{ID}$  is more positive than 200 mV, and must output a Low when  $V_{ID}$  is more negative than  $-200$  mV. The receiver parameters which determine the failsafe performance are  $V_{TH+}$ ,  $V_{TH-}$ , and  $V_{HYS}$  (the separation between  $V_{TH+}$  and  $V_{TH-}$ ). As shown in the table, differential signals more negative than  $-200$  mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the  $V_{TH+}$  threshold, and the receiver output will be High. Only when the differential input is more than  $V_{HYS}$  below  $V_{TH+}$  will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value,  $V_{HYS}$ , as well as the value of  $V_{TH+}$ .



## Typical Application (continued)

### 10.2.1.5 Transient Protection

The bus pins of the THVD14xx transceiver family include on-chip ESD protection against  $\pm 30$ -kV HBM and  $\pm 18$ -kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance,  $C_{(S)}$ , and 78% lower discharge resistance,  $R_{(D)}$ , of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

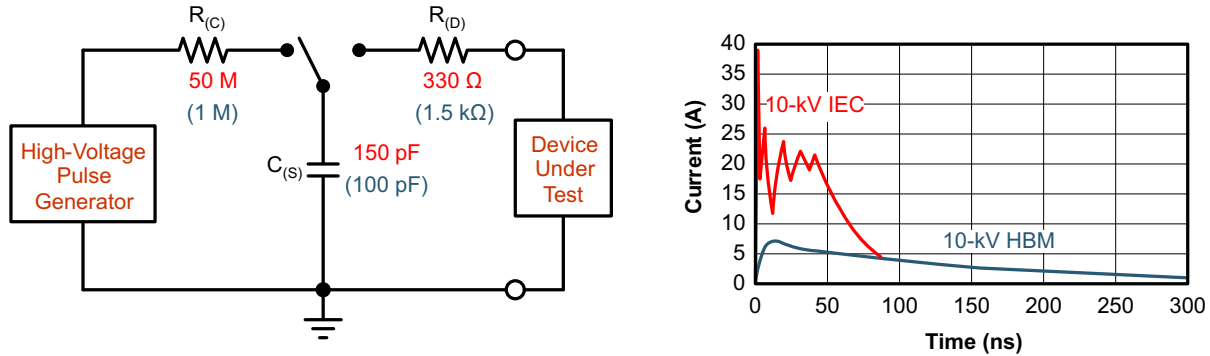


Figure 34. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 35 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

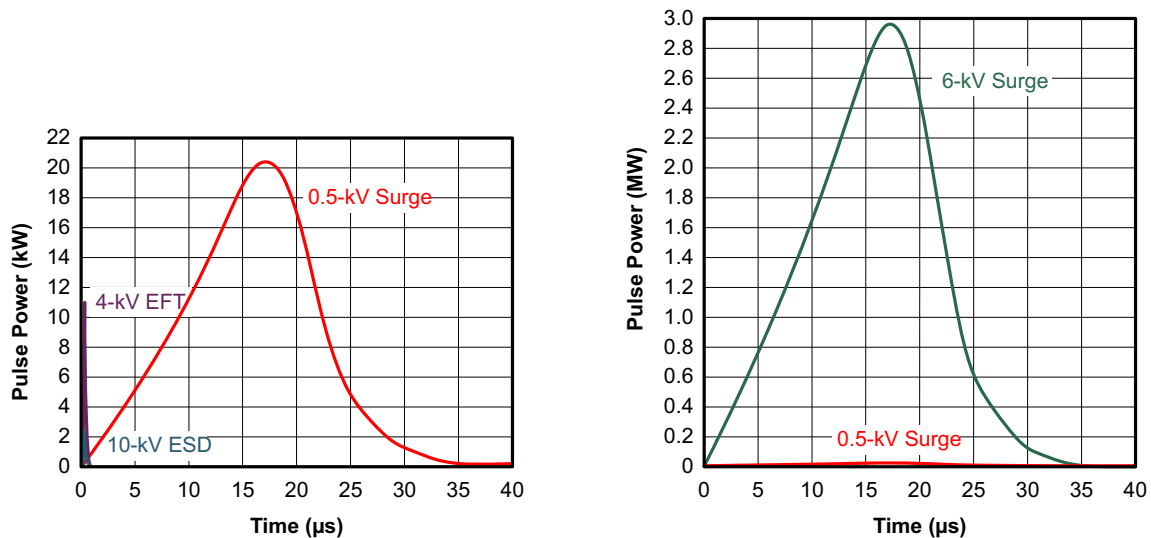
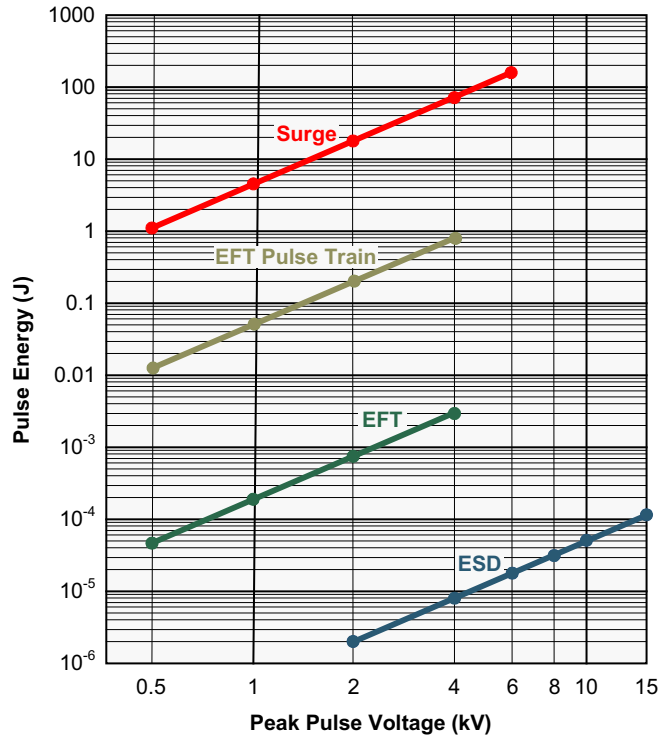


Figure 35. Power Comparison of ESD, EFT, and Surge Transients

### Typical Application (continued)

If the surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. [36](#) shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.



**36. Comparison of Transient Energies**

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

Figure 37 and Figure 38 suggest a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 7 shows the associated bill of materials.

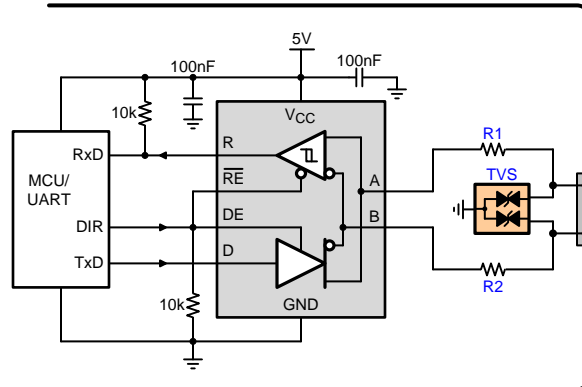


Figure 37. Transient Protection Against Surge Transients for Half-Duplex Devices

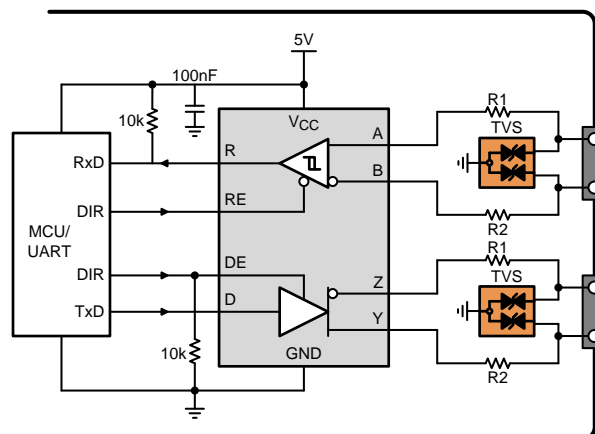
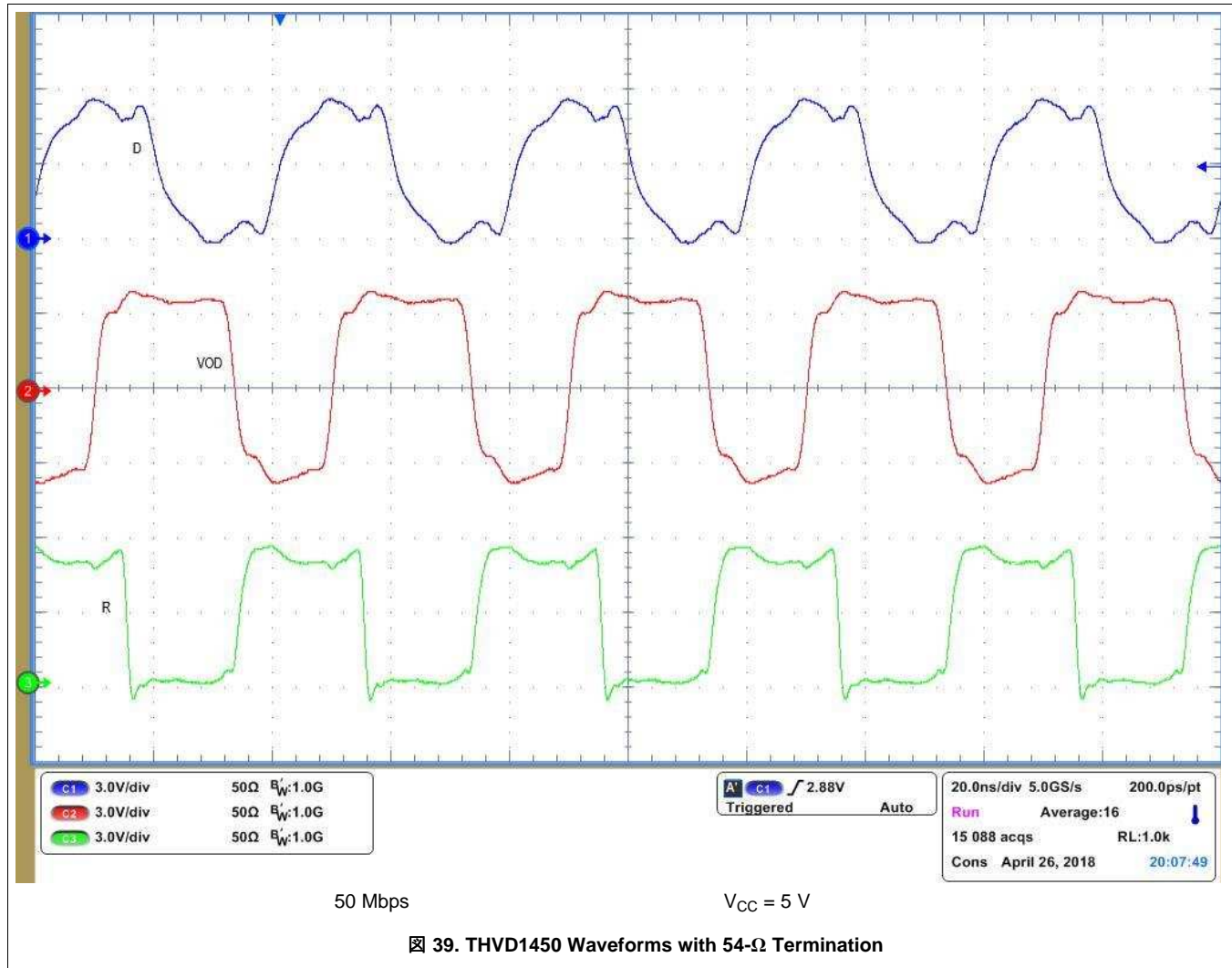


Figure 38. Transient Protection Against Surge Transients for Full-Duplex Devices

Table 7. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD14xx	TI
R1	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
R2			
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

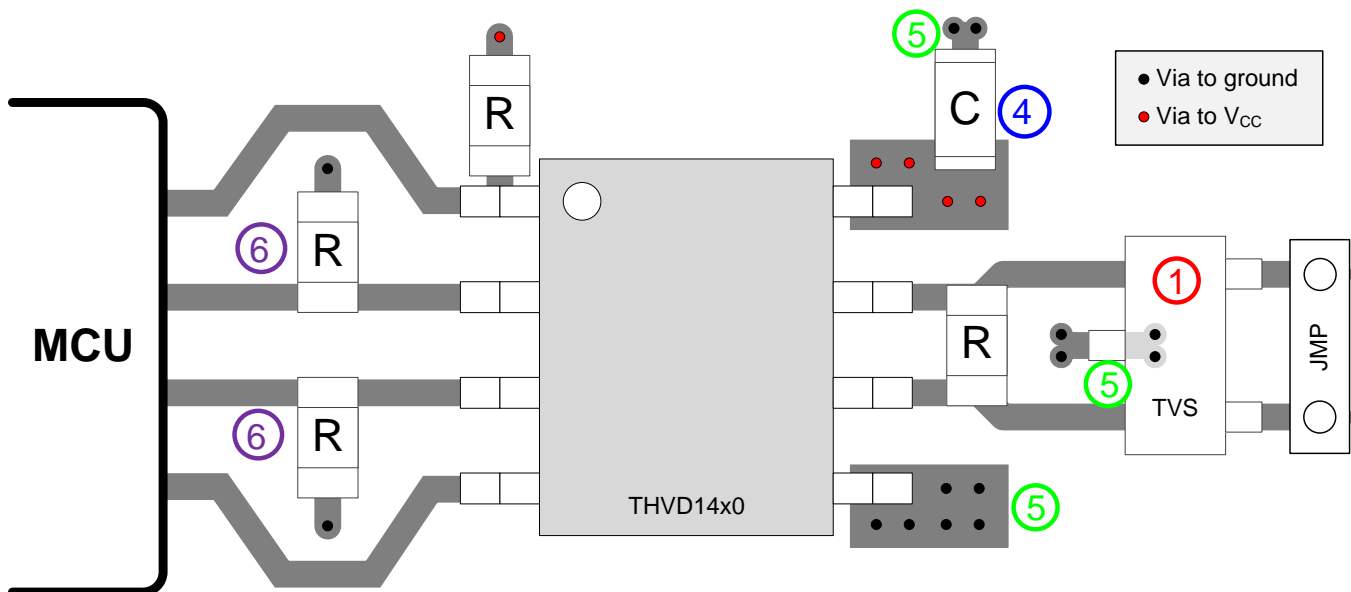
## 12 Layout

### 12.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
2. Use  $V_{CC}$  and ground planes to provide low-inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the  $V_{CC}$  pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for  $V_{CC}$  and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-k $\Omega$  to 10-k $\Omega$  pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

### 12.2 Layout Example



⊠ 40. Half-Duplex Layout Example

## 13 デバイスおよびドキュメントのサポート

### 13.1 デバイス・サポート

### 13.2 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

### 13.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 8. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
THVD1410	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
THVD1450	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
THVD1451	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
THVD1452	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

### 13.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 13.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.6 商標

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All other trademarks are the property of their respective owners.

### 13.7 静電気放電に関する注意事項



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### 13.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1410D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1410	<a href="#">Samples</a>
THVD1410DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1410	<a href="#">Samples</a>
THVD1410DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   SN   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1410	<a href="#">Samples</a>
THVD1410DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1410	<a href="#">Samples</a>
THVD1450D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450	<a href="#">Samples</a>
THVD1450DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1450	<a href="#">Samples</a>
THVD1450DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-1-260C-UNLIM	-40 to 125	1450	<a href="#">Samples</a>
THVD1450DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1450	<a href="#">Samples</a>
THVD1450DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1450	<a href="#">Samples</a>
THVD1450DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1450	<a href="#">Samples</a>
THVD1451D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451	<a href="#">Samples</a>
THVD1451DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1451	<a href="#">Samples</a>
THVD1451DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1451	<a href="#">Samples</a>
THVD1451DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1451	<a href="#">Samples</a>
THVD1452D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452	<a href="#">Samples</a>
THVD1452DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1452	<a href="#">Samples</a>
THVD1452DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1452	<a href="#">Samples</a>
THVD1452DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1452	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THVD1410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1410DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1450DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1450DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1450DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1450DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1451DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1451DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1451DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
THVD1452DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD1452DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1410DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THVD1410DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
THVD1410DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1450DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
THVD1450DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1450DRBR	SON	DRB	8	3000	346.0	346.0	35.0
THVD1450DRBT	SON	DRB	8	250	200.0	183.0	25.0
THVD1451DR	SOIC	D	8	2500	353.0	353.0	32.0
THVD1451DRBR	SON	DRB	8	3000	346.0	346.0	35.0
THVD1451DRBT	SON	DRB	8	250	200.0	183.0	25.0
THVD1452DGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
THVD1452DR	SOIC	D	14	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
THVD1410D	D	SOIC	8	75	507	8	3940	4.32
THVD1410DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1450D	D	SOIC	8	75	507	8	3940	4.32
THVD1450DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THVD1451D	D	SOIC	8	75	507	8	3940	4.32
THVD1452D	D	SOIC	14	50	507	8	3940	4.32
THVD1452DGS	DGS	VSSOP	10	80	330	6.55	500	2.88

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

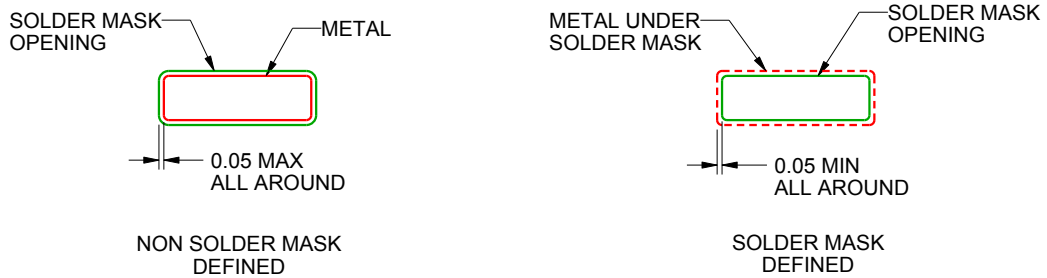
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

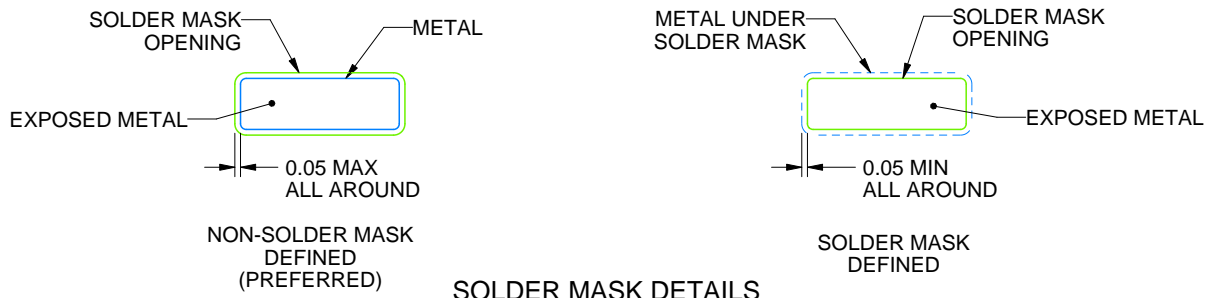
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**DRB 8**

**GENERIC PACKAGE VIEW**

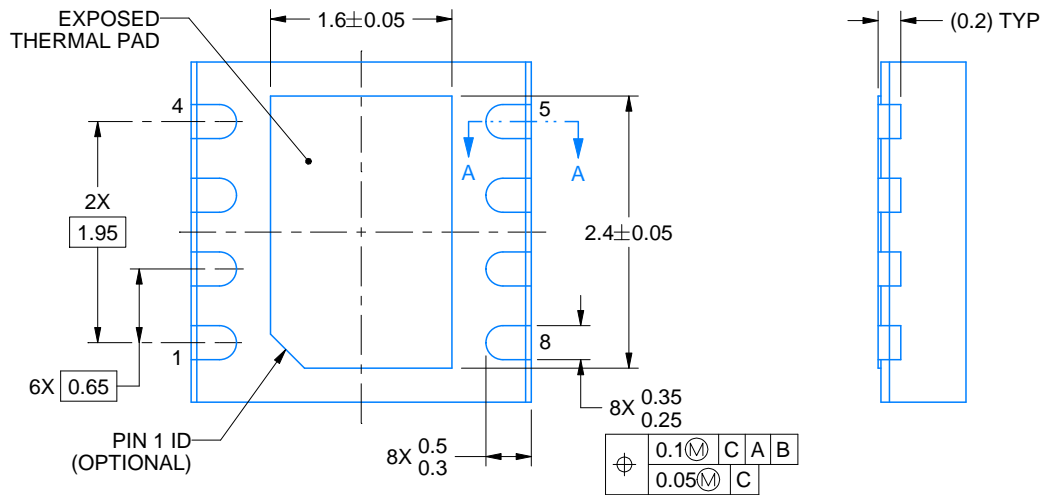
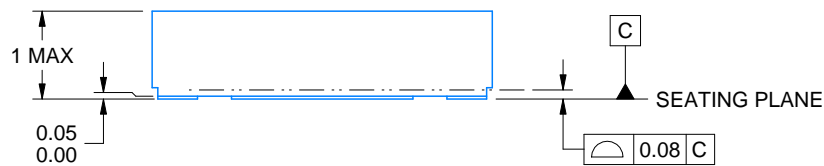
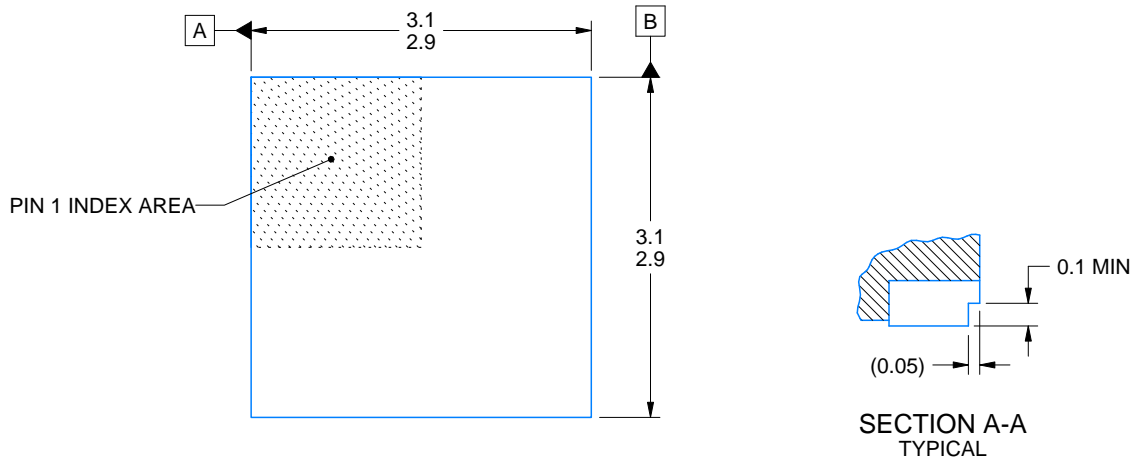
**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L



4222121/C 10/2016

NOTES:

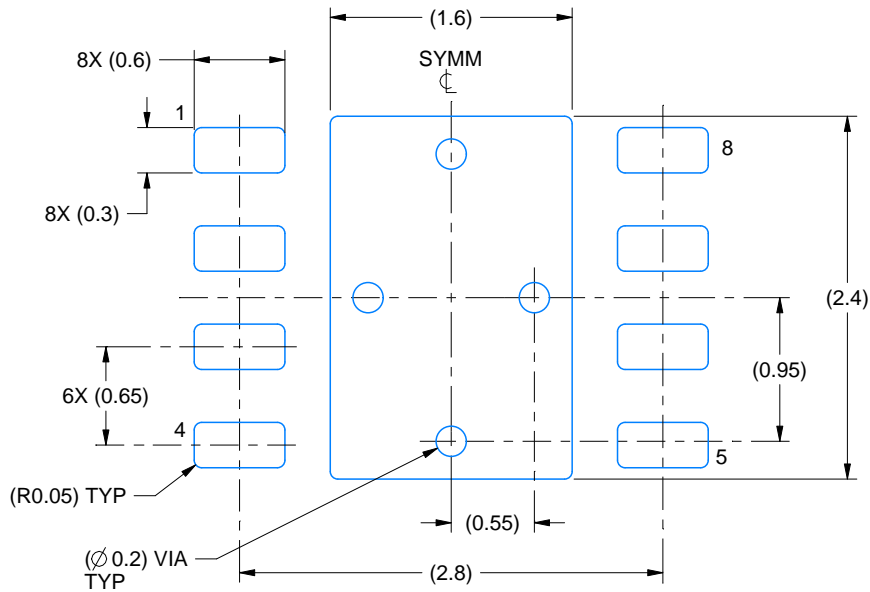
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

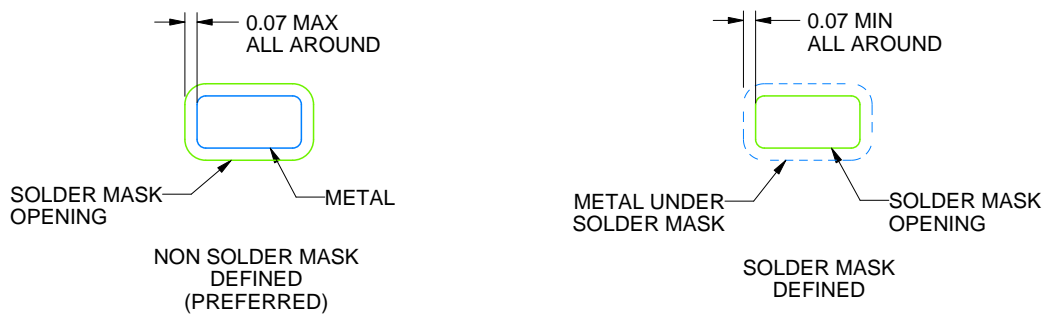
DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222121/C 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

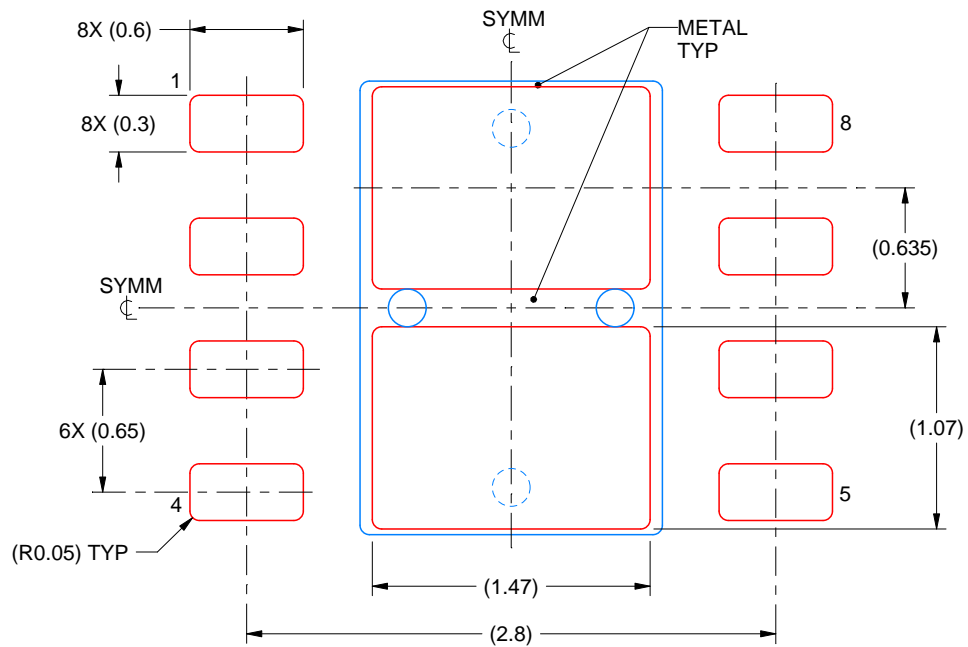


# EXAMPLE STENCIL DESIGN

DRB0008F

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
82% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4222121/C 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

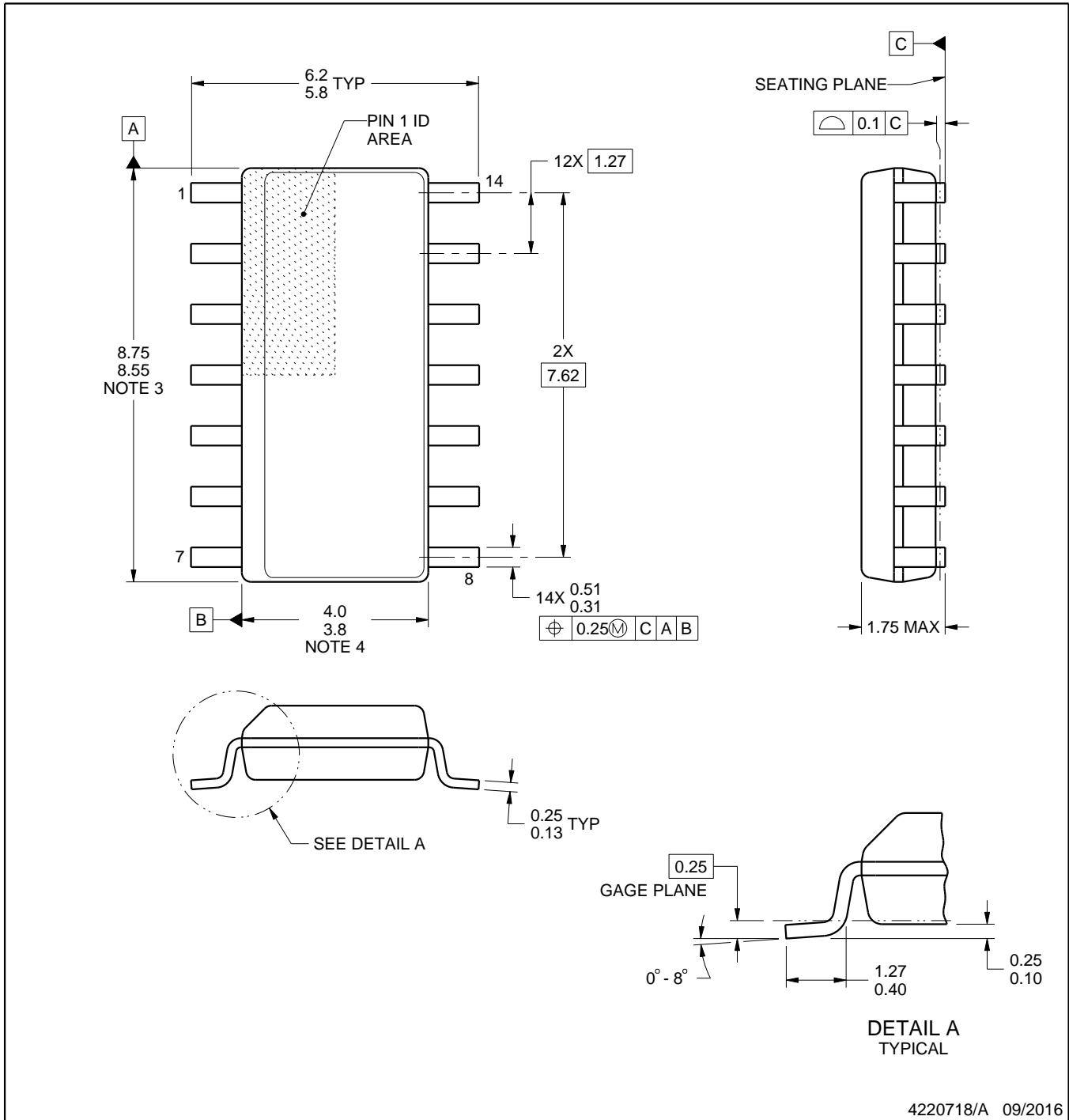
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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