参考資料

TL16C550C 自動フロー制御機能搭載非同期通信素子

1 特長

- Auto-$\overline{\text{RTS}}$ および Auto-$\overline{\text{CTS}}$ をプログラム可能
- Auto-$\overline{\text{CTS}}$ モードでは、$\overline{\text{CTS}}$ はトランスミッタを制御します
- Auto-$\overline{\text{RTS}}$ モードでは、RCV FIFO の内容とスレッショルドは $\overline{\text{RTS}}$ を制御します
- シリアルおよびモデム制御出力は、機器が同じ電力降下にあるときに RJ11 ケーブルを直接駆動します
- 既存の TL16C450 ソフトウェアすべてで動作可能
- リセット後、すべてのレジスタは TL16C450 レジスタ・セットと同じになります
- 最大 1Mbaud の動作に対応する、最大 16MHz のクロック・レート
- TL16C450 モードでは、ホールド・レジスタとシフト・レジスタにより、CPU とシリアル・データの間で正確な同期が不要になります
- プログラム可能なボーレート・ジェネレータにより、任意の入力基準クロックを 1～(2^{16} -1) 分割し、内部 16× クロックを生成できます
- シリアル・データ・ストリームに追加またはそこから削除された標準の非同期通信ビット (スタート、ストップ、パリティ)
- 5V および 3.3V で動作
- 独立したレシーバ・クロック入力
- 送信、受信、ライン・ステータス、およびデータ・セット割り込みを個別に制御できます
- シリアル・インターフェイスの特性を完全にプログラム可能：
  - 5、6、7、8 ビット文字
  - 偶数、奇数、パリティなしのビット生成と検出
  - 1、1 1/2、または 2 ストップ・ビットの生成
  - ボー生成 (最大速度 1Mbit/s)
- 不正スタート・ビットの検出
- 完全なステータス報告機能
- 双方向データ・バスと制御バス向けの 3 ステート出力 TTL ドライブ機能
- ライン・ブレイク生成および検出
- 内部診断機能：
  - 通信リンク・フォルト分離のループバック制御
  - ブレーク、パリティ、オーバーラン、フレーム化エラーのシミュレーション
- 完全に優先順位付けされた割り込みシステム制御
- モデム制御機能 ($\overline{\text{CTS}}$、$\overline{\text{RTS}}$、$\overline{\text{DSR}}$、$\overline{\text{DTR}}$、$\overline{\text{RI}}$、および $\overline{\text{DCD}}$)

2 概要

TL16C550C および TL16C550CI は、TL16C550B 非同期通信素子 (ACE) の機能アップグレードであり、TL16C450 の機能アップグレードです。電源投入時の TL16C450 (文字モードまたは TL16C450 モード) と機能的に同等である TL16C550C と TL16C550B などの TL16C550CI は、代替 FIFO モードに設定できます。これにより、受信および送信された文字をバッファリングすることで、CPU に過剰なソフトウェア・オーバーヘッドが発生しなくなります。レシーバとトランスミッタの FIFO には、レシーバ FIFO の 1 バイトあたり 3 ビットのエラー・ステータスを含む、最大 16 バイトが保存されます。FIFO モードでは、選択可能な自動フロー制御機能があり、ソフトウェアの過負荷を大幅に低減し、$\overline{\text{RTS}}$ 出力信号と $\overline{\text{CTS}}$ 入力信号を使用してシリアル・データ・フローを自動的に制御することで、システム効率を上げることができます。

TL16C550C および TL16C550CI は、ペリフェラル・デバイスまたはモデムから受信したデータのシリアルからパラレルへの変換と、CPU から受信したデータのパラレルからシリアルへの変換を実行します。CPU は、いつでも ACE ステータスを読み取ることができます。ACE には、包括的なモデム制御機能と、通信リンクのソフトウェア管理を最小限に抑えるようにカスタマイズできるプロセッサ割り込みシステムが含まれています。

TL16C550C と TL16C550CI のどちらの ACE にも、プログラマブル・ボーレート・ジェネレータが搭載されており、基準クロックを 1～65535 のディバイダで除算し、内部トランスミッタ・ロジック用に 16× 基準クロックを生成できます。レシーバ・ロジックでこの 16× クロックを使用するための規定が含まれています。ACE は 1Mbaud のシリアル・レート (16MHz 入力クロック) に対応しているため、ビット時間は 1μs、標準的な文字時間は 10μs (スタート・ビット、8 データ・ビット、ストップ・ビット) です。

TL16C550C と TL16C550CI の TL16C450 端子機能のうち 2 つが $\overline{\text{TXRDY}}$ および $\overline{\text{RXRDY}}$ に変更され、DMA コントローラに信号を供給します。

English Data Sheet: SLLS177

Table of Contents

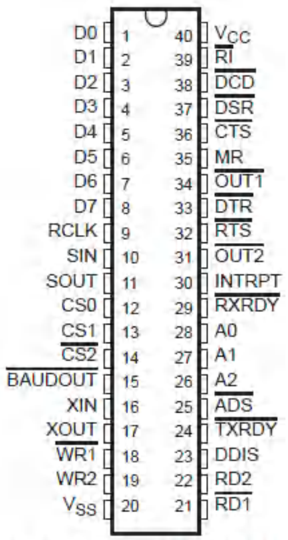
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (January 2006) to Revision I (March 2021) **Page**

- データシート・フォーマットを変更.......... 1
- Added the *Pin Configuration and Functions* section.......... 3
- Added the *Thermal Information* table. 7

4 Pin Configuration and Functions



NOTE: 40-pin DIP (N package) will be obsoleted as of 7/30/2006. Please contact your local distributor or TI Sales Office for more information.

図 4-1. N Package (Top View)

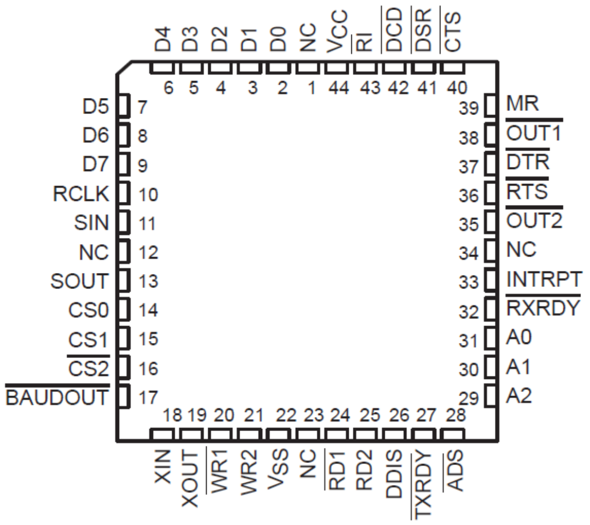


図 4-2. FN Package (Top View)

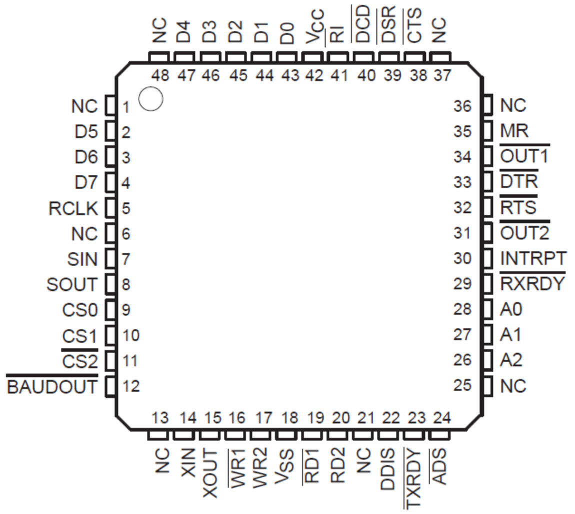


図 4-3. PT/PFB Package (Top View)

NC - No internal connection

表 4-1. Pin Functions

TERMINAL				I/O	DESCRIPTION
NAME	NO.N(1)	NO.FN	NO.PT		
A0	28	31	28	I	Register select. A0 −A2 are used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses and refer to $\overline{\text{ADS}}$ description.
A1	27	30	27		
A2	26	29	26		

表 4-1. Pin Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	**NO.N(1)**	**NO.FN**	**NO.PT**		
$\overline{\text{ADS}}$	25	28	24	I	Address strobe. When $\overline{\text{ADS}}$ is active (low), A0, A1, and A2 and CS0, CS1, and $\overline{\text{CS2}}$ drive the internal select logic directly; when $\overline{\text{ADS}}$ is high, the register select and chip select signals are held at the logic levels they were in when the low-to-high transition of $\overline{\text{ADS}}$ occurred
$\overline{\text{BAUDOUT}}$	15	17	12	O	Baud out. $\overline{\text{BAUDOUT}}$ is a 16 x clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{\text{BAUDOUT}}$ may also be used for the receiver section by tying this output to RCLK.
CS0	12	14	9	I	Chip select. When CS0 and CS1 are high and $\overline{\text{CS2}}$ is low, these three inputs select the ACE. When any of these inputs are inactive, the ACE remains inactive (refer to $\overline{\text{ADS}}$ description).
CS1	13	15	10		
$\overline{\text{CS2}}$	14	16	11		
$\overline{\text{CTS}}$	36	40	38	I	Clear to send. $\overline{\text{CTS}}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates that $\overline{\text{CTS}}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{\text{CTS}}$ changes levels and the auto-$\overline{\text{CTS}}$ mode is not enabled, an interrupt is generated. $\overline{\text{CTS}}$ is also used in the auto-$\overline{\text{CTS}}$ mode to control the transmitter
D0	1	2	43	I/O	Data bus. Eight data lines with 3-state outputs provide a bidirectional path for data, control, and status information between the ACE and the CPU.
D1	2	3	44		
D2	3	4	45		
D3	4	5	46		
D4	5	6	47		
D5	6	7	2		
D6	7	8	3		
D7	8	9	4		
$\overline{\text{DCD}}$	38	42	40	I	Data carrier detect. $\overline{\text{DCD}}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (ΔDCD) of the modem status register indicates that $\overline{\text{DCD}}$ has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{\text{DCD}}$ changes levels, an interrupt is generated
DDIS	23	26	22	O	Driver disable. DDIS is active (high) when the CPU is not reading data. When active, DDIS can disable an external transceiver.
$\overline{\text{DSR}}$	37	41	39	I	Data set ready. $\overline{\text{DSR}}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (ΔDSR) of the modem status register indicates $\overline{\text{DSR}}$ has changed levels since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{\text{DSR}}$ changes levels, an interrupt is generated.
$\overline{\text{DTR}}$	33	37	33	O	Data terminal ready. When active (low), $\overline{\text{DTR}}$ informs a modem or data set that the ACE is ready to establish comunication. $\overline{\text{DTR}}$ is placed in the active level by setting the DTR bit of the modem control register. $\overline{\text{DTR}}$ is placed in the inactive level either as a result of a master reset, during loop mode operation, or clearing the DTR bit.
INTRPT	30	33	30	O	Interrupt.When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register, or an enabled modem status interrupt. INTRPT is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	39	35	I	Master reset. When active (high), MR clears most ACE registers and sets the levels of various output signals (refer to Table 2).
$\overline{\text{OUT1}}$	34	38	34	O	Outputs 1 and 2. These are user-designated output terminals that are set to the active (low) level by setting respective modem control register (MCR) bits (OUT1 and OUT2). $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$ are set to inactive the (high) level as a result of master reset, during loop mode operations, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR.
$\overline{\text{OUT2}}$	31	35	31		

表 4-1. Pin Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.N(1)	NO.FN	NO.PT		
RCLK	9	10	5	I	Receiver clock. RCLK is the 16 x baud rate clock for the receiver section of the ACE.
$\overline{\text{RD1}}$ RD2	21 22	24 25	19 20	I	Read inputs. When either $\overline{\text{RD1}}$ or RD2 is active (low or high respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied to its inactive level (i.e., RD2 tied low or $\overline{\text{RD1}}$ tied high
$\overline{\text{RI}}$	39	43	41	I	Ring indicator. $\overline{\text{RI}}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that $\overline{\text{RI}}$ has transitioned from a low to a high level since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated
$\overline{\text{RTS}}$	32	36	32	O	Request to send. When active, $\overline{\text{RTS}}$ informs the modem or data set that the ACE is ready to receive data. $\overline{\text{RTS}}$ is set to the active level by setting the RTS modem control register bit and is set to the inactive (high) level either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) ofthe MCR. In the auto-$\overline{\text{RTS}}$ mode, $\overline{\text{RTS}}$ is set to the inactive level by the receiver threshold control logic
$\overline{\text{RXRDY}}$	29	32	29	O	Receiver ready. Receiver direct memory access (DMA) signalling is available with $\overline{\text{RXRDY}}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected using the FIFO control register bit 3 (FCR3). When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA mode 0 (FCR0 = 0 or FCR0 =1, FCR3 = 0), when there is at least one character in the receiver FIFO or receiver holding register, $\overline{\text{RXRDY}}$ is active (low). When $\overline{\text{RXRDY}}$ has been active but there are no characters in the FIFO or holding register, $\overline{\text{RXRDY}}$ goes inactive (high).In DMA mode 1 (FCR0 = 1, FCR3 = 1), when the trigger level or the time-out has been reached, $\overline{\text{RXRDY}}$ goes active (low); when it has been active but there are no more characters in the FIFO or holding register, it goes inactive (high).
SIN	10	11	7	I	Serial data input. SIN is serial data input from a connected communications device.
SOUT	11	13	8	O	Serial data output. SOUT is composite serial data output to a connected communication device. SOUT is set to the marking (high) level as a result of master reset.
$\overline{\text{TXRDY}}$	24	27	23	O	Transmitter ready. Transmitter DMA signalling is available with $\overline{\text{TXRDY}}$. When operating in the FIFO mode, one of two types of DMA signalling can be selected using FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled.
V_{CC}	40	44	42		5-V supply voltage
V_{SS}	20	22	18		Supply common
$\overline{\text{WR1}}$ WR2	18 19	20 21	16 17	I	Write inputs. When either $\overline{\text{WR1}}$ or WR2 is active (low or high respectively) and while the ACE is selected,the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied to its inactive level (i.e., WR2 tied low or $\overline{\text{WR1}}$ tied high).
XIN XOUT	16 17	18 19	14 15	I/O	External clock. XIN and XOUT connect the ACE to the main timing reference (clock or crystal).

(1) The N package is **Not Recommended for New Designs**.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(3)		–0.5	7	V
V_I	Input voltage range at any input		–0.5	7	V
V_O	Output voltage range		–0.5	7	V
T_A	Operating free-air temperature range	TL16C550C	0	70	°C
		TL16C550CI	–40	85	°C
T_{stg}	Storage temperature		–65	150	°C
T_C	Case temperature for 10 seconds	FN package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N(1) (2) or PT package		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The N package is Not Recommended for New Designs.
(3) All voltage values are with respect to V_{SS}.

5.2 Recommended Operating Conditions (Low Voltage - 3.3 nominal)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Input voltage, V_I	0		V_{CC}	V
High-level input voltage, V_{IH} (1)	0.7 V_{CC}			V
Low-level input voltage, V_{IL} (1)			0.3 V_{CC}	V
Output voltage, V_O (2)	0		V_{CC}	V
High-level output current, I_{OH} (all outputs)			1.8	mA
Low-level output current, I_{OL} (all outputs)			3.2	mA
Input capacitance			1	pF
Operating free-air temperature, T_A	0	25	70	°C
Junction temperature range, T_J (3)	0	25	115	°C
Oscillator/clock speed			14.9	MHz

(1) Meets TTL levels, V_{IHmin} = 2 V and V_{ILmax} = 0.8 V on nonhysteresis inputs.
(2) Applies for external output buffers.
(3) These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

5.3 Recommended Operating Conditions (Standard Voltage - 5 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage, V_{IH}	Except XIN	2			V
	XIN	0.7 V_{CC}			
Low-level input voltage, V_{IL}	Except XIN			0.8	V
	XIN			0.3 V_{CC}	
Output voltage, V_O (1)		0		V_{CC}	V
High-level output current, I_{OH} (all outputs)				4	mA
Low-level output current, I_{OL} (all outputs)				4	mA
Input capacitance				1	pF
Operating free-air temperature, T_A		0	25	70	°C
Junction temperature range, T_J (2)		0	25	115	°C
Oscillator/clock speed				16	MHz

(1) Applies for external output buffers.
(2) These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

5.4 Thermal Information

THERMAL METRIC(1)		TL16C550C	TL16C550C	TL16C550C	UNIT
		PT	PFB	FN	
		48 PINS	48 PINS	44 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.5	73.6	62.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.0	26.3	37.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.2	37.2	39.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	1.9	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.0	37.0	38.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics (Low Voltage - 3.3 V nominal)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH} (2)	High-level output voltage	I_{OH} = − 1 mA		2.4			V
V_{OL} (2)	Low-level output voltage	I_{OL} = 1.6 mA				0.5	V
I_I	Input current	V_{CC} = 3.6 V, V_I = 0 to 3.6 V,	V_{SS} = 0, All other terminals floating			10	μA
I_{OZ}	High-impedance-state output current	V_{CC} = 3.6 V, V_O = 0 to 3.6 V Chip selected in write mode or chip deselect	V_{SS} = 0,			± 20	μA
I_{CC}	Supply current	V_{CC} = 3.6 V, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2V, All other inputs at 0.8 V, No load on outputs,	T_A = 25°C XTAL1 at 4 MHz, Baud rate = 50 kbit/s			8	mA
$C_{i(CLK)}$	Clock input capacitance	V_{CC}= 0, f =1 MHz, **All other terminals grounded**	V_{SS} = 0, T_A = 25°C		15	20	pF
$C_{o(CLK)}$	Clock output capacitance				20	30	pF
C_i	Input capacitance				6	10	pF
C_o	Output capacitance				10	20	pF

(1) All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
(2) These parameters apply for all outputs except XOUT.

5.6 Electrical Characteristics (Standard Voltage - 5 V nominal)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH} (2)	High-level output voltage	I_{OH} = − 1 mA		2.4			V
V_{OL} (2)	Low-level output voltage	I_{OL} = 1.6 mA		0.4			V
I_I	Input current	V_{CC} = 5.25 V, V_I = 0 to 5.25 V,	V_{SS} = 0, All other terminals floating	10			μA
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V, V_O = 0 to 5.25 V, Chip selected in write mode or chip deselect	V_{SS} = 0,	± 20			μA
I_{CC}	Supply current	V_{CC} = 5.25 V, $\overline{SIN}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2V, All other inputs at0.8 V, No load on outputs,	T_A = 25°C XTAL1 at 4 MHz, Baud rate = 50 kbit/s	10			mA
$C_{i(CLK)}$	Clock input capacitance	V_{CC}= 0, f =1 MHz, **All other terminals grounded**	V_{SS} = 0, T_A = 25°C,		15	20	pF
$C_{o(CLK)}$	Clock output capacitance				20	30	pF
C_i	Input capacitance				6	10	pF
C_o	Output capacitance				10	20	pF

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) These parameters apply for all outputs except XOUT.

5.7 System Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature

		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{cR}	Cycle time, read (tw7 + td8 + td9)	RC			87		ns
t_{cW}	Cycle time, write (tw6 + td5 + td6)	WC			87		ns
t_{w1}	Pulse duration, clock high	t_{XH}	5	f = 16 MHz Max, V_{CC} = 5 V	25		ns
t_{w2}	Pulse duration, clock low	t_{XL}					
t_{w5}	Pulse duration, $\overline{\text{ADS}}$ low	t_{ADS}	6.7		9		ns
t_{w6}	Pulse duration, $\overline{\text{WR}}$	t_{WR}	6		40		ns
t_{w7}	Pulse duration, $\overline{\text{RD}}$	t_{RD}	7		40		ns
t_{w8}	Pulse duration, MR	t_{MR}			1		ns
t_{su1}	Setup time, address valid before $\overline{\text{ADS}}$ ↑	t_{AS}	6.7		8		ns
t_{su2}	Setup time, CS valid before $\overline{\text{ADS}}$ ↑	t_{CS}					
t_{su3}	Setup time, data valid before $\overline{\text{WR1}}$ ↑ or WR2 ↓	t_{DS}	6		15		ns
t_{su4}	Setup time, $\overline{\text{CTS}}$ ↑ before midpoint of stop bit		17		10		ns
t_{h1}	Hold time, address low after $\overline{\text{ADS}}$ ↑	t_{AH}	6.7		0		ns
t_{h2}	Hold time, CS valid after $\overline{\text{ADS}}$ ↑	t_{CH}					
t_{h3}	Hold time, CS valid after $\overline{\text{WR1}}$ ↑ or WR2 ↓	t_{WCS}	6		10		ns
t_{h4}	Hold time, address valid after $\overline{\text{WR1}}$ ↑ or WR2 ↓	t_{WA}					
t_{h5}	Hold time, data valid after $\overline{\text{WR1}}$ ↑ or WR2 ↓	t_{DH}	6		5		ns
t_{h6}	Hold time, chip select valid after $\overline{\text{RD1}}$ ↑ or RD2 ↓	t_{RCS}	7		10		ns
t_{h7}	Hold time, address valid after $\overline{\text{RD1}}$ ↑ or RD2 ↓	t_{RA}	7		20		ns
t_{d4} (1)	Delay time, CS valid before $\overline{\text{WR1}}$ ↓ or WR2 ↑	t_{CSW}	6		7		ns
t_{d5} (1)	Delay time, address valid before $\overline{\text{WR1}}$ ↓ or WR2 ↑	t_{AW}					
t_{d6} (1)	Delay time, write cycle, $\overline{\text{WR1}}$ ↑ or WR2 ↓ to $\overline{\text{ADS}}$ ↓	t_{WC}	6		40		ns
t_{d7} (1)	Delay time, CS valid to $\overline{\text{RD1}}$ ↓ or RD2 ↑	t_{CSR}	7		7		ns
t_{d8} (1)	Delay time, address valid to $\overline{\text{RD1}}$ ↓ or RD2 ↑	t_{AR}					
t_{d9}	Delay time, read cycle, $\overline{\text{RD1}}$ ↑ or RD2 ↓ to $\overline{\text{ADS}}$ ↓	t_{RC}	7		40		ns
t_{d10}	Delay time, $\overline{\text{RD1}}$ ↓ or RD2 ↑ to data valid	t_{RVD}	7	C_L = 75 pF		45	ns
t_{d11}	Delay time, $\overline{\text{RD1}}$ ↑ or RD2 ↓ to floating data	t_{HZ}	7	C_L = 75 pF		20	ns

(1) Only applies when $\overline{\text{ADS}}$ is low.

5.8 System Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature(1)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(R)}$	Disable time, $\overline{RD1}$ ↓ ↑ or RD2 ↑ ↓ to DDIS ↑ ↓	t_{RDD}	7	C_L = 75 pF	20		ns

(1) Charge and discharge times are determined by V_{OL}, V_{OH}, and external loading.

5.9 Baud Generator Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	t_{LW}	5	f = 16 MHz, CLK ÷ 2, V_{CC} = 5 V	50		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	t_{HW}	5				
t_{d1}	Delay time, XIN ↑ to $\overline{BAUDOUT}$ ↑	t_{BLD}	5			45	ns
t_{d2}	Delay time, XIN ↑ ↓ to $\overline{BAUDOUT}$ ↓	t_{BHD}	5			45	ns

5.10 Receiver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature(1)

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample	t_{SCD}	8			10	ns
t_{d13}	Delay time, stop to set INTRPT or read RBR to LSI interrupt or stop to $\overline{RXRDY}$ ↓	t_{SINT}	8, 9, 10, 11, 12			1	RCLK cycle
t_{d14}	Delay time, read RBR/LSR to reset INTRPT	t_{RINT}	8, 9, 10, 11, 12	C_L = 75 pF		70	ns

(1) In the FIFO mode, the read cycle (RC) = 425 ns (min) between reads of the receive FIFO and the status registers (interrupt identification register or line status register).

5.11 Transmitter Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		ALT. SYMBOL	FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, initial write to transmit start	t_{IRS}	13		8	24	baudout cycles
t_{d16}	Delay time, start to INTRPT	t_{STI}	13		8	10	baudout cycles
t_{d17}	Delay time, $\overline{\text{WR}}$ (WR THR) to reset INTRPT	t_{HR}	13	C_L = 75 pF		50	ns
t_{d18}	Delay time, initial write to INTRPT (THRE[1])	t_{SI}	13		16	34	baudout cycles
t_{d19}	Delay time, read IIR[1] to reset INTRPT (THRE[1])	t_{IR}	13	C_L = 75 pF		35	ns
t_{d20}	Delay time, write to $\overline{\text{TXRDY}}$ inactive	t_{WXI}	14, 15	C_L = 75 pF		35	ns
t_{21}	Delay time, start to $\overline{\text{TXRDY}}$ active	t_{SXA}	14, 15	C_L = 75 pF		9	baudout cycles

(1) THRE = transmitter holding register empty; IIR = interrupt identification register.

5.12 Modem Control Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 75 pF

PARAMETER		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
t_{d22}	Delay time, WR MCR to output	t_{MDO}	16		50	ns
t_{d23}	Delay time, modem interrupt to set INTRPT	t_{SIM}	16		35	ns
t_{d24}	Delay time, RD MSR to reset INTRPT	t_{RIM}	16		40	ns
t_{d25}	Delay time, $\overline{\text{CTS}}$ low to SOUT ↓		17		24	baudout cycles
t_{d26}	Delay time, RCV threshold byte to $\overline{\text{RTS}}$ ↑		18		2	baudout cycles
t_{d27}	Delay time, read of last byte in receive FIFO to $\overline{\text{RTS}}$ ↓		18		2	baudout cycles
t_{d28}	Delay time, first data bit of 16th character to $\overline{\text{RTS}}$ ↑		19		2	baudout cycles
t_{d29}	Delay time, $\overline{\text{RBRRD}}$ low to $\overline{\text{RTS}}$ ↓		19		2	baudout cycles

6 Parameter Measurement Information

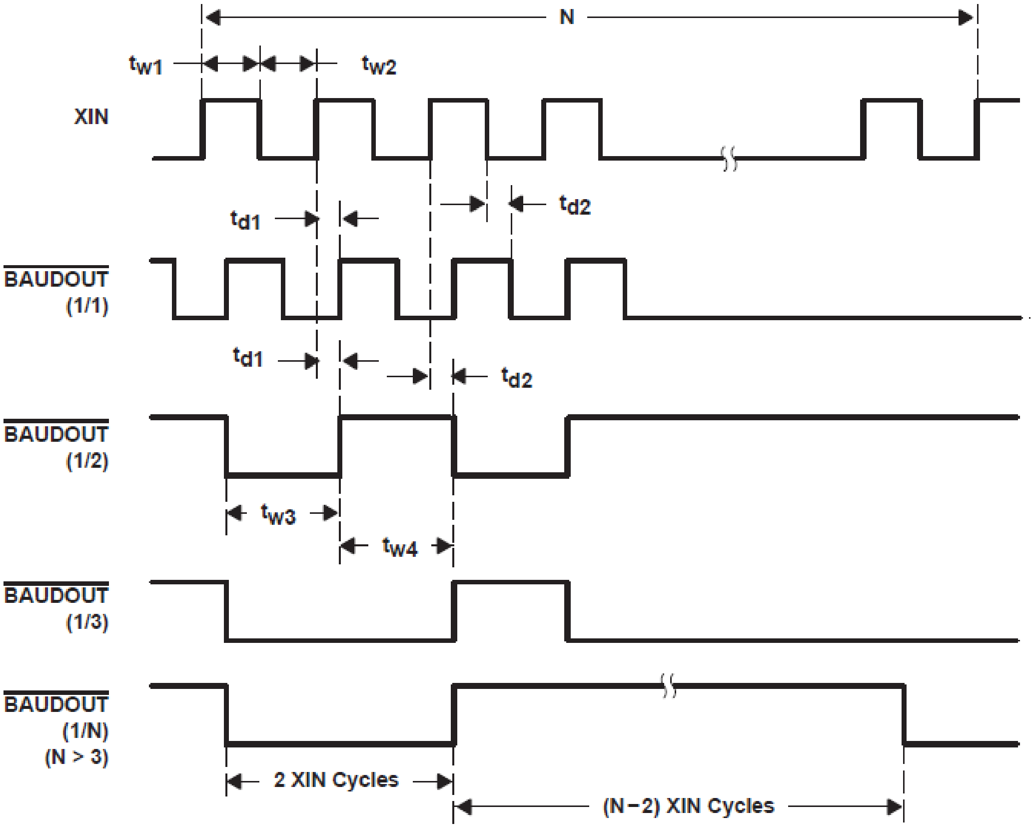


図 6-1. Baud Generator Timing Waveforms

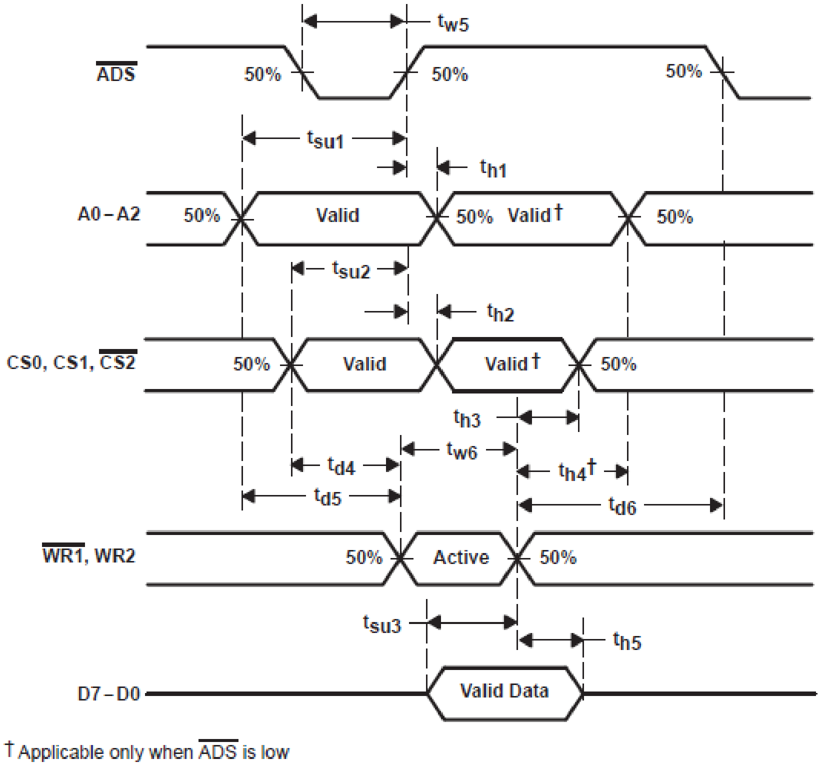
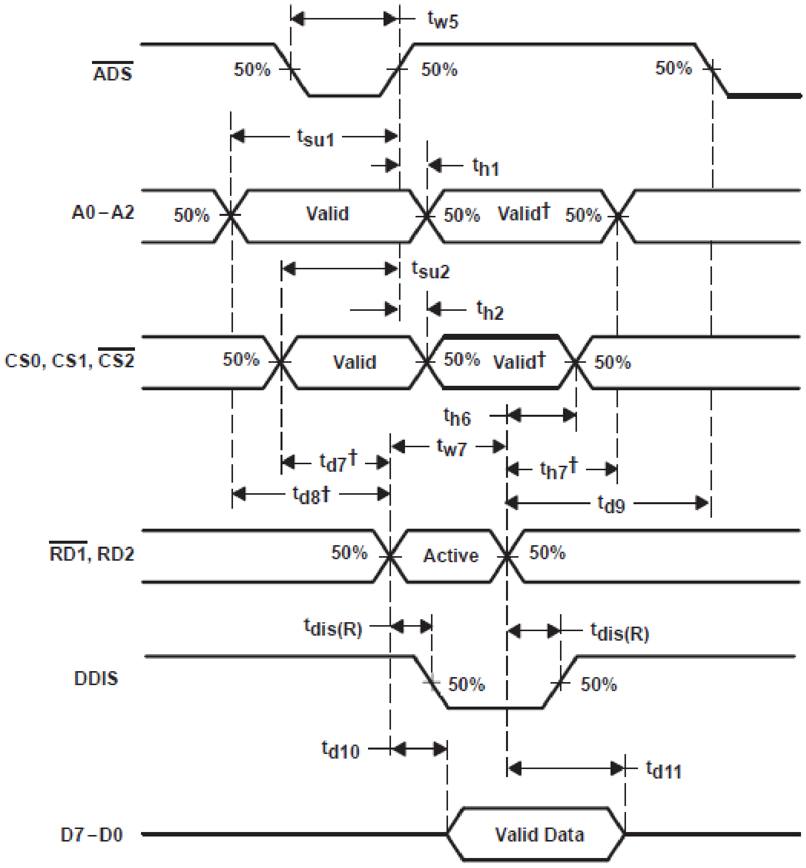


図 6-2. Write Cycle Timing Waveforms



† Applicable only when $\overline{ADS}$ is low

図 6-3. Read Cycle Timing Waveforms

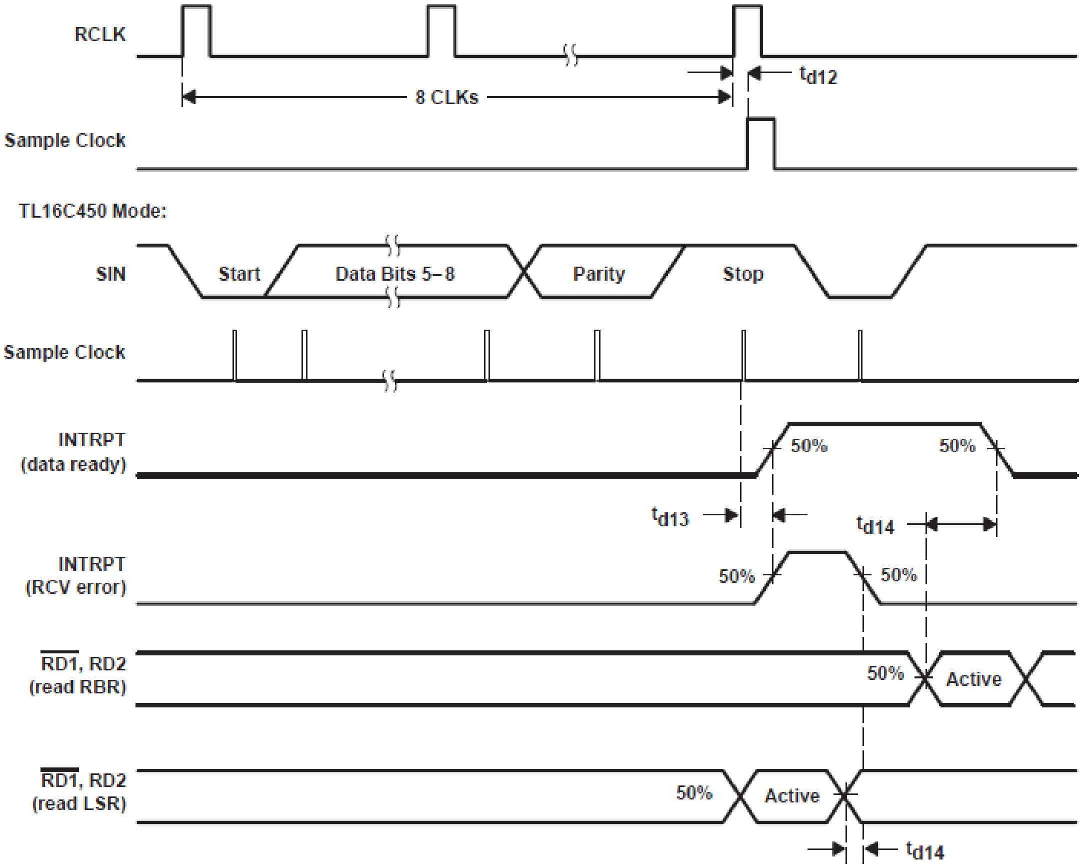
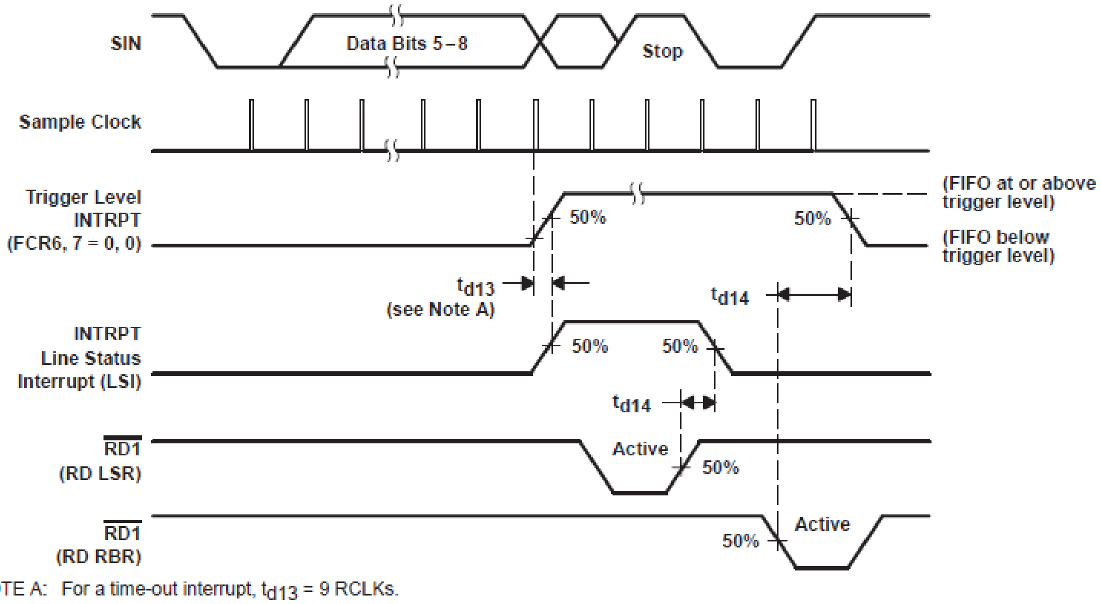


図 6-4. Receiver Timing Waveforms



NOTE A: For a time-out interrupt, t_{d13} = 9 RCLKs.

図 6-5. Receive FIFO First Byte (Sets DR Bit) Waveforms

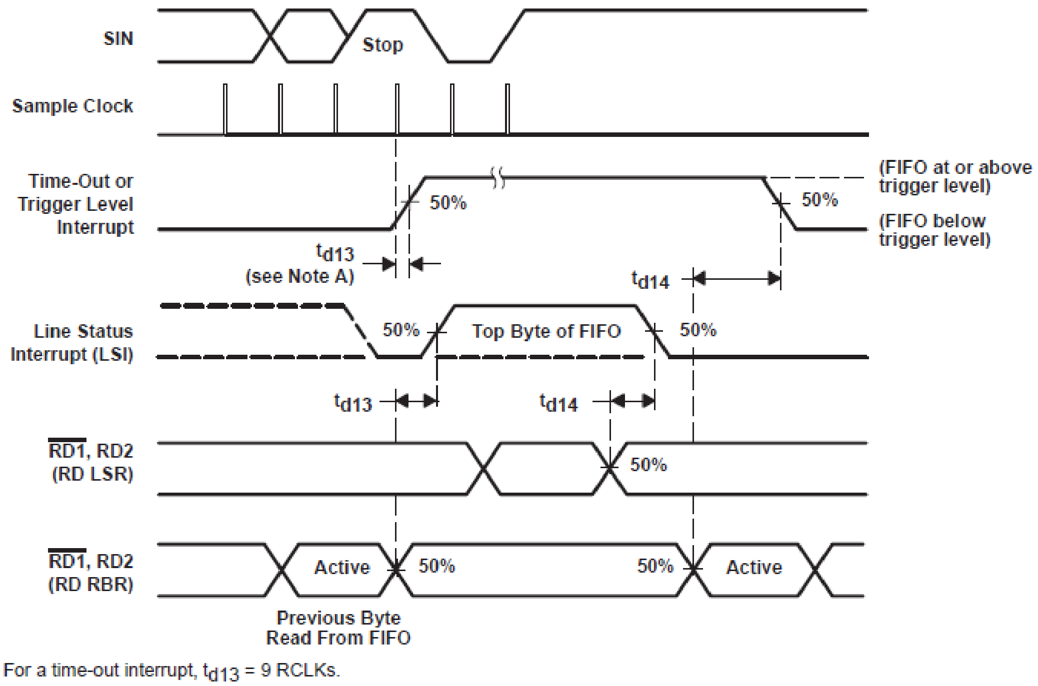


図 6-6. Receive FIFO Bytes Other Than the First Byte (DR Internal Bit Already Set) Waveforms

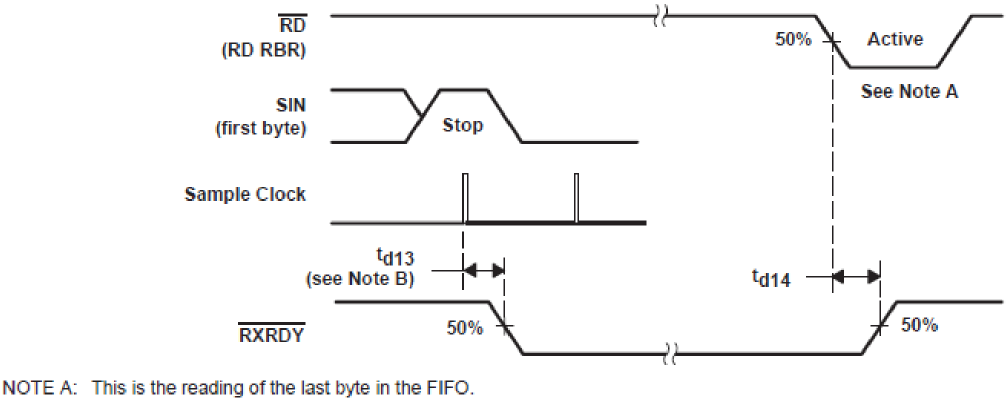
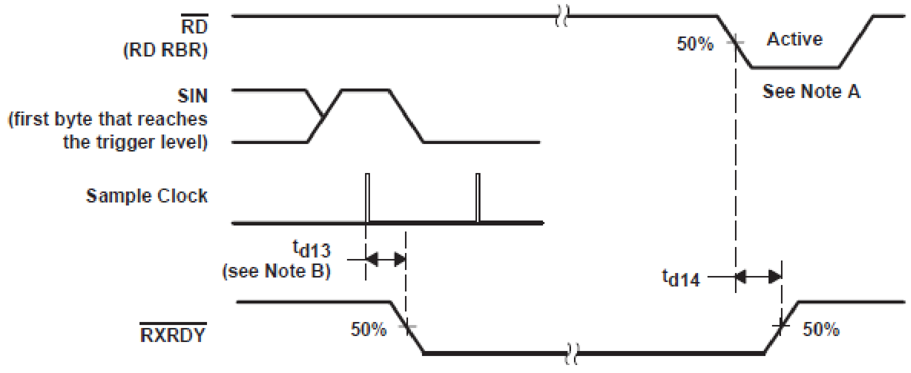


図 6-7. Receiver Ready ($\overline{\text{RXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



NOTES: A. This is the reading of the last byte in the FIFO.
B. For a time-out interrupt, t_{d13} = 9 RCLKs.

図 6-8. Receiver Ready (RXRDY) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

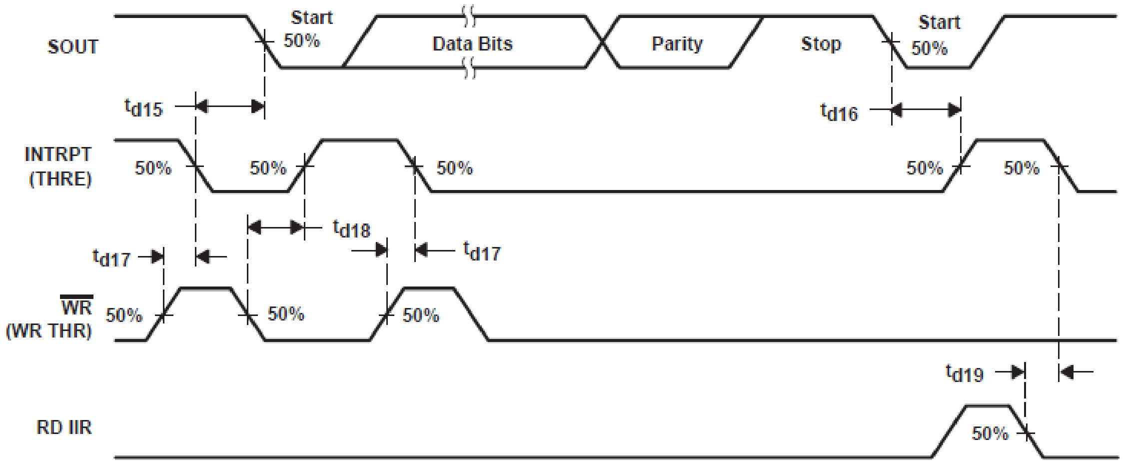


図 6-9. Transmitter Timing Waveforms

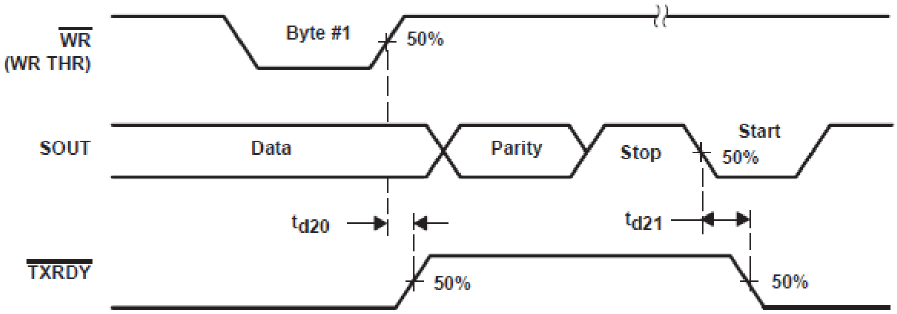


図 6-10. Transmitter Ready ($\overline{\text{TXRDY}}$) Waveforms, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

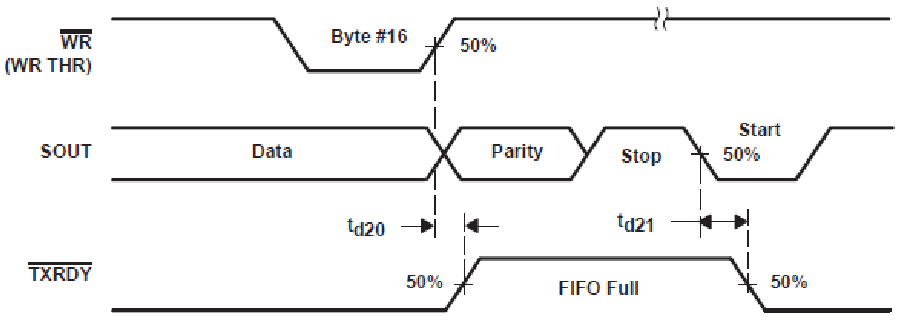


図 6-11. Transmitter Ready ($\overline{TXRDY}$) Waveforms, FCR0 = 1 and FCR3 = 1 (Mode 1)

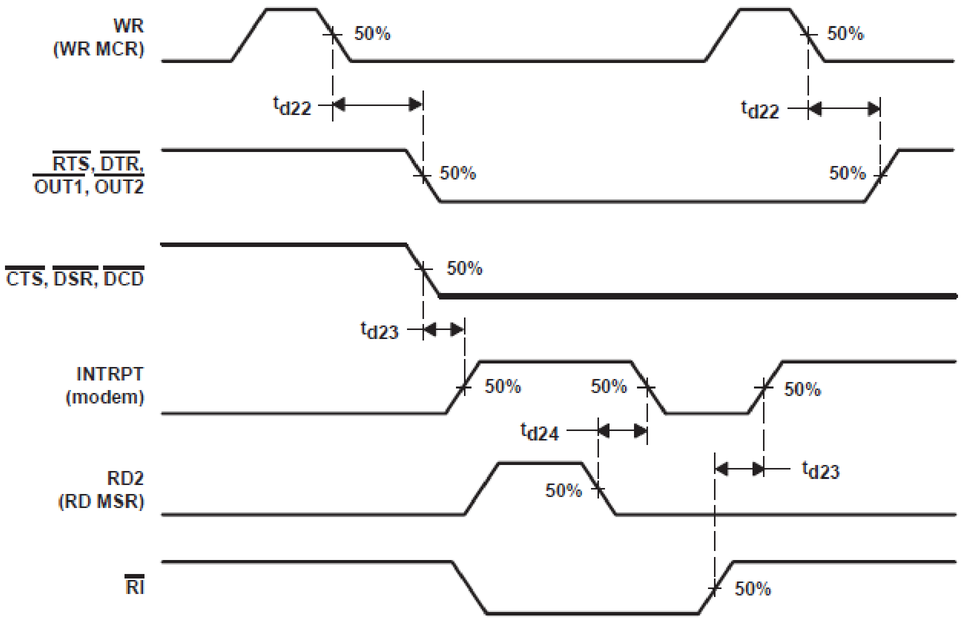


図 6-12. Modem Control Timing Waveforms

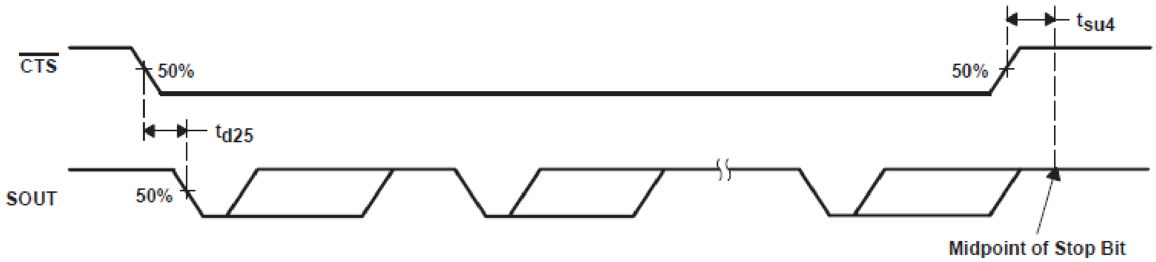


図 6-13. $\overline{CTS}$ and SOUT Autoflow Control Timing (Start and Stop) Waveforms

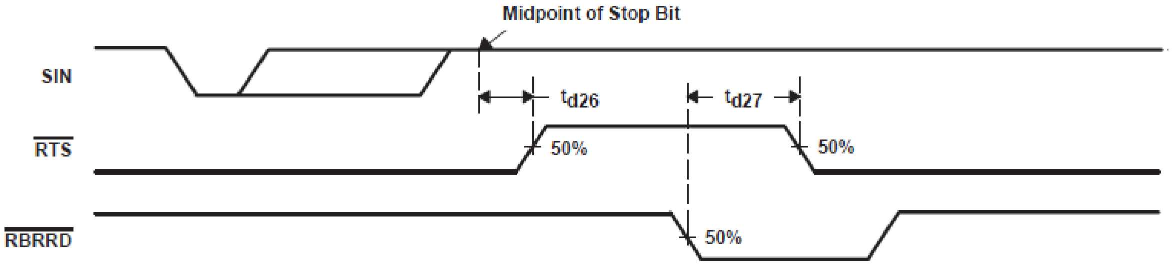


図 6-14. Auto-$\overline{RTS}$ Timing for RCV Threshold of 1, 4, or 8 Waveforms

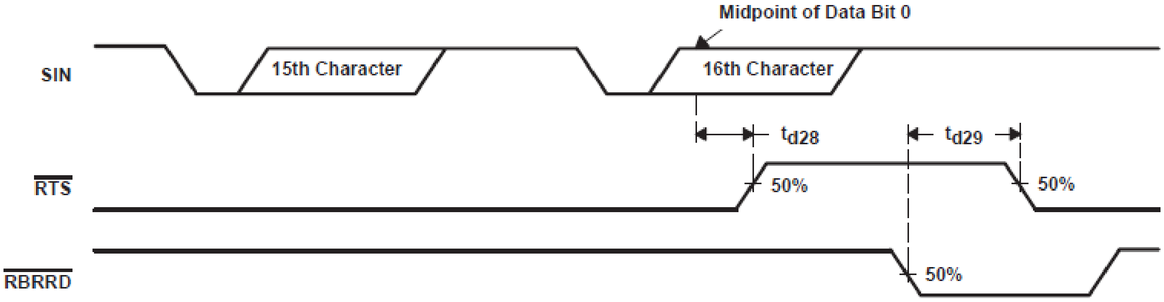


図 6-15. Auto-$\overline{RTS}$ Timing for RCV Threshold of 14 Waveforms

7 Detailed Description

7.1 Autoflow Control (see 図 7-1)

Autoflow control is comprised of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. With auto-$\overline{CTS}$, the $\overline{CTS}$ input must be active before the transmitter FIFO can emit data. With auto-$\overline{RTS}$, $\overline{RTS}$ becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using ACE1 and ACE2 from a TLC16C550C with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

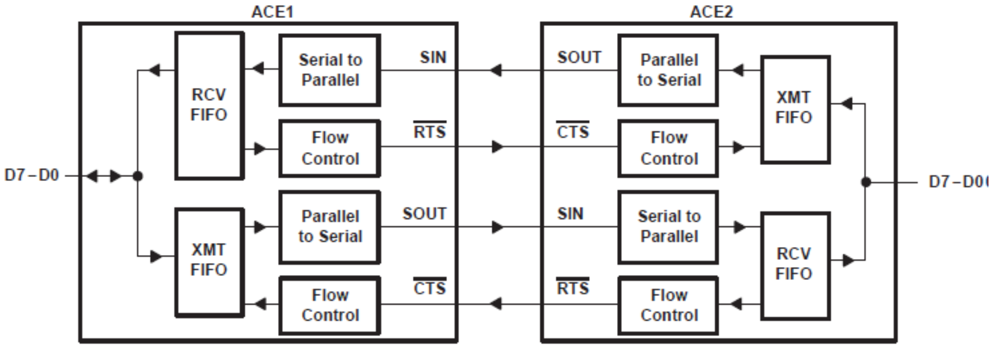


図 7-1. Autoflow Control (Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$) Example

7.2 Auto-$\overline{RTS}$ (see 図 7-1)

Auto-$\overline{RTS}$ data flow control originates in the receiver timing and control block (see セクション 7.6) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see 図 7-3), $\overline{RTS}$ is deasserted. With trigger levels of 1, 4, and 8, the sending ACE may send an additional byte after the trigger level is reached (assuming the sending ACE has another byte to send) because it may not recognize the deassertion of $\overline{RTS}$ until after it has begun sending the additional byte. $\overline{RTS}$ is automatically reasserted once the RCV FIFO is emptied by reading the receiver buffer register.

When the trigger level is 14 (see Figure 4), $\overline{RTS}$ is deasserted after the first data bit of the 16th character is present on the SIN line. $\overline{RTS}$ is reasserted when the RCV FIFO has at least one available byte space.

7.3 Auto-$\overline{CTS}$ (see 図 7-1)

The transmitter circuitry checks $\overline{CTS}$ before sending the next data byte. When $\overline{CTS}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{CTS}$ must be released before the middle of the last stop bit that is currently being sent (see 図 7-2). The auto-$\overline{CTS}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{CTS}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{CTS}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result

7.4 Enabling Autoflow Control and Auto-$\overline{CTS}$

Autoflowcontrol is enabled by setting modem control register bits 5 (autoflow enable or AFE) and 1 (RTS) to a 1. Autoflow incorporates both auto-$\overline{RTS}$ and auto-$\overline{CTS}$. When only auto-$\overline{CTS}$ is desired, bit 1 in the modem control register should be cleared (this assumes that a control signal is driving $\overline{CTS}$).

7.5 Auto-$\overline{\text{CTS}}$ and Auto-$\overline{\text{RTS}}$ Functional Timing

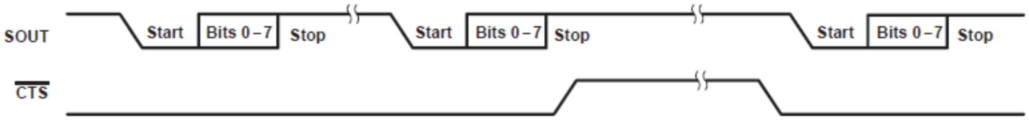


図 7-2. $\overline{\text{CTS}}$ Functional Timing Waveforms

NOTES:

1. When $\overline{\text{CTS}}$ is low, the transmitter keeps sending serial data out.
2. If $\overline{\text{CTS}}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte but it does not send the next byte.
3. When $\overline{\text{CTS}}$ goes from high to low, the transmitter begins sending data again.

The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes. These are described in 図 7-3 and 図 7-4.

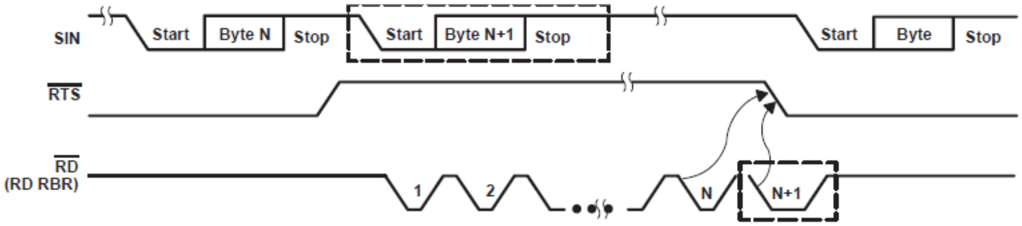


図 7-3. $\overline{\text{RTS}}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 1, 4, or 8 Bytes

NOTES:

1. N = RCV FIFO trigger level (1, 4, or 8 bytes)
2. The two blocks in dashed lines cover the case where an additional byte is sent as described in the preceding auto-$\overline{\text{RTS}}$ section.

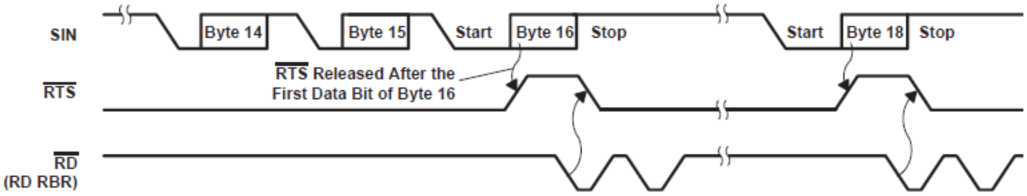
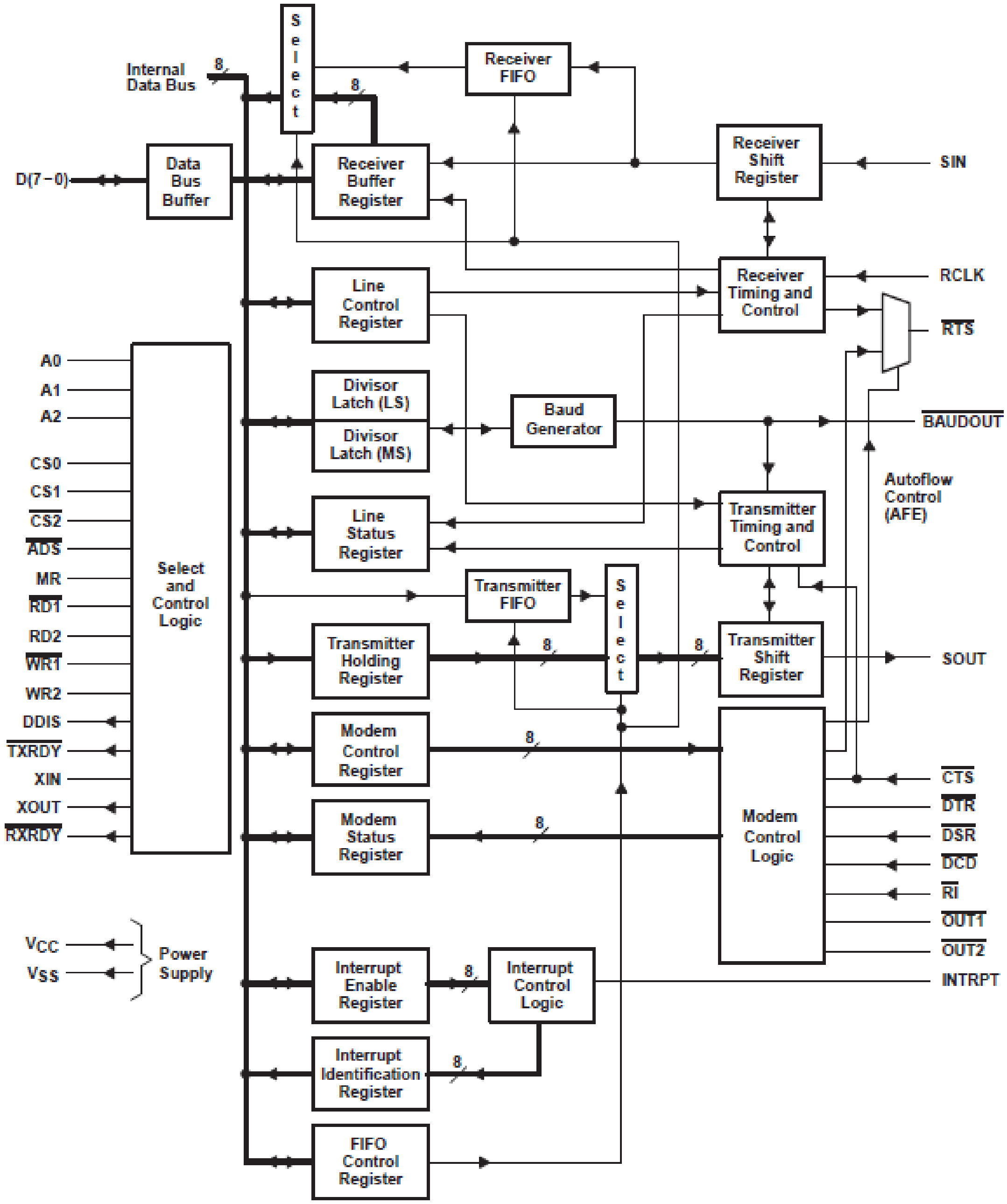


図 7-4. $\overline{\text{RTS}}$ Functional Timing Waveforms, RCV FIFO Trigger Level = 14 Bytes

NOTES:

1. $\overline{\text{RTS}}$ is deasserted when the receiver receives the first data bit of the sixteenth byte. The receive FIFO is full after finishing the sixteenth byte.
2. $\overline{\text{RTS}}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing or there is more than one byte of space available.
3. When the receive FIFO is full, the first receive buffer register read reasserts $\overline{\text{RTS}}$.

7.6 Functional Block Diagram



7.7 Principles of Operation

表 7-1. Register Selection

DLAB(1)	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable register
X	L	H	L	Interrupt identification register (read only)
X	L	H	L	FIFO control register (write)
X	L	H	H	Line control register
X	H	L	L	Modem control register
X	H	L	H	Line status register

表 7-1. Register Selection (continued)

DLAB[1]	A2	A1	A0	REGISTER
X	H	H	L	Modem status register
X	H	H	H	Scratch register
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

(1) The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 4).

表 7-2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Master reset	All bits cleared (0 − 3 forced and 4 − 7 permanent)
Interrupt identification register	Master reset	Bit 0 is set, bits 1, 2, 3, 6, and 7 are cleared, and bits 4 − 5 are permanently cleared
FIFO control register	Master reset	All bits cleared
Line control register	Master reset	All bits cleared
Modem control register	Master reset	All bits cleared (6 − 7 permanent)
Line status register	Master reset	Bits 5 and 6 are set; all other bits are cleared
Modem status register	Master reset	Bits 0 − 3 are cleared; bits 4 − 7 are input signals
SOUT	Master reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IR/write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master reset	High
$\overline{\text{RTS}}$	Master reset	High
$\overline{\text{DTR}}$	Master reset	High
$\overline{\text{OUT1}}$	Master reset	High
Scratch register	Master reset	No effect
Divisor latch (LSB and MSB) registers	Master reset	No effect
Receiver buffer register	Master reset	No effect
Transmitter holding register	Master reset	No effect
RCVR FIFO	MR/FCR1 −FCR0/ΔFCR0	All bits cleared
XMIT FIFO	MR/FCR2 −FCR0/ΔFCR0	All bits cleared

7.7.1 Accessible Registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in 表 7-2. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow 表 7-3.

表 7-3. Summary of Accessible Registers

BIT NO.	REGISTER ADDRESS											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0(1)	Data Bit 0	Enable Received Data Available Interrupt (ERBI)	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (ΔCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (ΔDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits (STB)	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 3(2)	DMA Mode Select	Parity Enable (PEN)	OUT2	Framing Error (FE)	Delta Data Carrier Detect (ΔDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Autoflow Control Enable (AFE)	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (2)	Receiver Trigger (LSB)	Break Control	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (2)	Receiver Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO(2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

(1) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
(2) These bits are always 0 in the TL16C450 mode.

7.7.2 FIFO Control Register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables and clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signalling.

- Bit 0: This bit, when set, enables the transmitter and receiver FIFOs. Bit 0 must be set when other FCR bits are written to or they are not programmed. Changing this bit clears the FIFOs.
- Bit 1: This bit, when set, clears all bytes in the receiver FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2: This bit, when set, clears all bytes in the transmit FIFO and clears its counter. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 3: When FCR0 is set, setting FCR3 causes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ to change from level 0 to level 1.
- Bits 4 and 5: These two bits are reserved for future use.
- Bits 6 and 7: These two bits set the trigger level for the receiver FIFO interrupt (see 表 7-4).

表 7-4. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

7.7.3 FIFO Interrupt Mode Operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1, IER2 = 1), a receiver interrupt occurs as follows:

1. The received data available interrupt is issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR = 06) has higher priority than the received data available (IIR = 04) interrupt.
4. The data ready bit (LSR0) is set when a character is transferred from the shift register to the receiver FIFO. It is cleared when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled:

1. - At least one character is in the FIFO.
   - The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).
   - The most recent microprocessor read of the FIFO has occurred more than four continuous character times before. This causes a maximum character received command to interrupt an issued delay of 160 ms at a 300 baud rate with a 12-bit character.
2. Character times are calculated by using the RCLK input for a clock signal (makes the delay proportional to the baud rate).
3. When a time-out interrupt has occurred, it is cleared and the timer is cleared when the microprocessor reads one character from the receiver FIFO.
4. When a time-out interrupt has not occurred, the time-out timer is cleared after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register empty interrupt [IIR (3 −0) = 2] occurs when the transmit FIFO is empty. It is cleared [IIR (3 −0) = 1] when the THR is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.

2. The transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time that the FIFO was empty. The first transmitter interrupt after changing FCR0 is immediate if it is enabled.

7.7.4 FIFO Polled Mode Operation

With FCR0 = 1 (transmitter and receiver FIFOs enabled), clearing IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program checks receiver and transmitter status using the LSR. As stated previously:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 − LSR 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode; the IIR is not affected since IER2 = 0.
- LSR5 indicates when the THR is empty.
- LSR6 indicates that both the THR and TSR are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO polled mode. However, the receiver and transmitter FIFOs are still fully capable of holding characters.

7.7.5 Interrupt Enable Register (IER)

The IER enables each of the five types of interrupts (refer to 表 7-5) and enables INTRPT in response to an interrupt generation. The IER can also disable the interrupt system by clearing bits 0 through 3. The contents of this register are summarized in 表 7-3 and are described in the following bullets.

- Bit 0: When set, this bit enables the received data available interrupt.
- Bit 1: When set, this bit enables the THRE interrupt.
- Bit 2: When set, this bit enables the receiver line status interrupt.
- Bit 3: When set, this bit enables the modem status interrupt.
- Bits 4 through 7: These bits are not used (always cleared).

7.7.6 Interrupt Identification Register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 − Receiver line status (highest priority).
- Priority 2 − Receiver data ready or receiver character time-out.
- Priority 3 − Transmitter holding register empty.
- Priority 4 − Modem status (lowest priority).

When an interrupt is generated, the IIR indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in 表 7-3 and described in 表 7-5. Detail on each bit is as follows:

- Bit 0: This bit is used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending If bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 3.
- Bit 3: This bit is always cleared in TL16C450 mode. In FIFO mode, bit 3 is set with bit 2 to indicate that a time-out interrupt is pending.
- Bits 4 and 5: These two bits are not used (always cleared).
- Bits 6 and 7: These bits are always cleared in TL16C450 mode. They are set when bit 0 of the FIFO control register is set.

表 7-5. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER				PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 3	BIT 2	BIT 1	BIT 0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Read the line status register
0	1	0	0	2	Received data available	Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode	Read the receiver buffer register
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times, and there is at least one character in it during this time	Read the receiver buffer register
0	0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Read the interrupt identification register(if source of interrupt) or writing into the transmitter holding register
0	0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Read the modem status register

7.7.7 Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in 表 7-3 and described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in 表 7-6.

表 7-6. Serial Character Word Length

BIT 1	BIT 0	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit 2 are shown in 表 7-7.

表 7-7. Number of Stop Bits Generated

BIT 2	WORD LENGTH SELECTED BY BITS 1 AND 2	NUMBER OF STOP BITS GENERATED
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set even parity (an even number of logic 1s in the data and parity bits) is selected. When parity is enabled and bit 4 is cleared, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This bit is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set. If bit 5 is cleared, stick parity is disabled.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition; i.e., a condition where SOUT is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled and has no affect on the transmitter logic; it only effects SOUT.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

7.7.8 Line Status Register (LSR)

[1]The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in 表 7-3 and described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. DR is set whenever a complete incoming character has been received and transferred into the RBR or the FIFO. DR is cleared by reading all of the data in the RBR or the FIFO.
- Bit 1[2]:This bit is the overrun error (OE) indicator. When OE is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. OE is cleared every time the CPU reads the contents of the LSR. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
- Bit 2 **(see Footnote 2)**: This bit is the parity error (PE) indicator. When PE is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). PE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.
- Bit 3 **(see Footnote 2)**: This bit is the framing error (FE) indicator. When FE is set, it indicates that the received character didnot have a valid (set) stop bit. FE is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE tries to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE samples this start bit twice and then accepts the input data.
- Bit 4 **(see Footnote 2)**: This bit is the break interrupt (BI) indicator. When BI is set, it indicates that the received data input was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is cleared every time the CPU reads the contents of the LSR. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state for at least two RCLK samples and then receives the next valid start bit.
- Bit 5: This bit is the THRE indicator. THRE is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when THRE is set, an interrupt is generated. THRE is set when the contents of the THR are transferred to the TSR. THRE is cleared concurrent with the loading of the THR by the CPU. In the FIFO mode, THRE is set when the transmit FIFO is empty; it is cleared when at least one byte is written to the transmit FIFO.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. TEMT bit is set when the THR and the TSR are bothempty. When either the THR or the TSR contains a data character, TEMT is cleared. In the FIFO mode, TEMT is set when the transmitter FIFO and shift register are both empty.
- Bit 7: In the TL16C550C mode, this bit is always cleared. In the TL16C450 mode, this bit is always cleared. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

---

[1] The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.

[2] Bits 1 through 4 are the error conditions that produce a receiver line status interrupt.

7.7.9 Modem Control Register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in 表 7-3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the $\overline{\text{DTR}}$ output
- Bit 1: This bit (RTS) controls the $\overline{\text{RTS}}$ output
- Bit 2: This bit (OUT1) controls $\overline{\text{OUT1}}$, a user-designated output signal.
- Bit 3: This bit (OUT2) controls $\overline{\text{OUT2}}$, a user-designated output signal.

When any of bits 0 through 3 are set, the associated output is forced low. When any of these bits are cleared, the associated output is forced high.

- Bit 4: This bit (LOOP) provides a local loop back feature for diagnostic testing of the ACE. When LOOP is set, the following occurs:
-
  - The transmitter SOUT is set high.
  - The receiver SIN is disconnected.
  - The output of the TSR is looped back into the receiver shift register input.
  - The four modem control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$) are disconnected.
  - The four modem control outputs ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$, and $\overline{\text{OUT2}}$) are internally connected to the four modem control inputs.
  - The four modem control outputs are forced to the inactive (high) levels.
- Bit 5: This bit (AFE) is the autoflow control enable. When set, the autoflow control as described in the detailed description is enabled.

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt's sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

The ACE flow can be configured by programming bits 1 and 5 of the MCR as shown in 表 7-8.

表 7-8. ACE Flow Configuration

MCR BIT 5 (AFE)	MCR BIT 1 (RTS)	ACE FLOW CONFIGURATION
1	1	Auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$ enabled (autoflow control enabled)
1	0	Auto-$\overline{\text{CTS}}$ only enabled
0	X	Auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$ disabled

7.7.10 Modem Status Register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information; when a control input from the modem changes state, the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in 表 7-3 and are described in the following bulleted list.

- Bit 0: This bit is the change in clear-to-send (ΔCTS) indicator. ΔCTS indicates that the $\overline{\text{CTS}}$ input has changed state since the last time it was read by the CPU. When ΔCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled (ΔCTS is cleared), no interrupt is generated.
- Bit 1: This bit is the change in data set ready (ΔDSR) indicator. ΔDSR indicates that the $\overline{\text{DSR}}$ input has changed state since the last time it was read by the CPU. When ΔDSR isset and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. TERI indicates that the $\overline{\text{RI}}$ input to the chip has changed from a low to a high level. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the change in data carrier detect (ΔDCD) indicator. ΔDCD indicates that the $\overline{\text{DCD}}$ input to the chip has changed state since the last time it was read by the CPU. When ΔDCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear-to-send ($\overline{\text{CTS}}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{\text{DSR}}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of the ring indicator ($\overline{\text{RI}}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{\text{DCD}}$) input. When the ACE is in the diagnostic test mode (LOOP [MCR4] = 1), this bit is equal to the MCR bit 3 (OUT2).

7.7.11 Programming Baud Generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 16 MHz and divides it by a divisor in the range between 1 and (2^{16}−1).The output frequency of the baud generator is sixteen times (16 x) the baud rate. The formula for the divisor is:

$$\text{divisor} = \text{XIN frequency input} \div (\text{desired baud rate} \times 16) \quad (1)$$

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

表 7-9 and 表 7-10 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38.4 kbits/s and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency (refer to 図 7-5 for examples of typical clock circuits).

表 7-9. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

表 7-10. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628

表 7-10. Baud Rates Using a 3.072-MHz Crystal (continued)

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

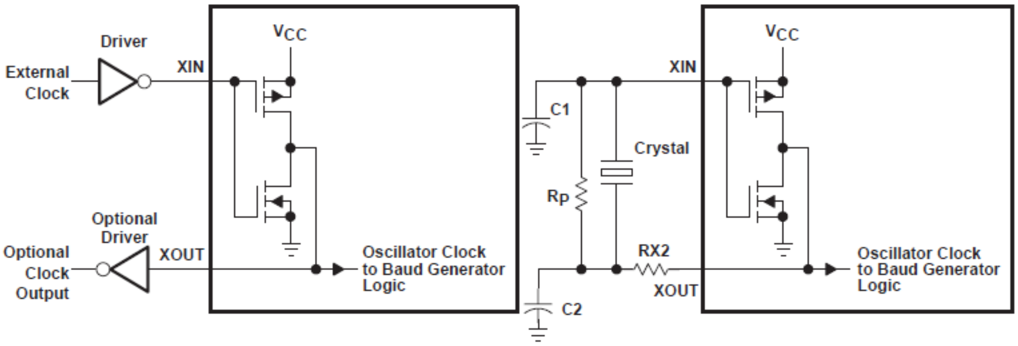


図 7-5. Typical Clock Circuits

表 7-11. TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
3.072 MHz	1 MW	1.5 kW	10 − 30 pF	40 − 60 pF
1.8432 MHz	1 MW	1.5 kW	10 − 30 pF	40 − 60 pF

7.7.12 Receiver Buffet Register (RBR)

The ACE receiver section consists of a receiver shift register (RSR) and a RBR. The RBR is actually a 16-byte FIFO. Timing is supplied by the 16 x receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE RSR receives serial data from SIN. The RSR then concatenates the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the RBR and the received data available interrupt is enabled (IER0 = 1), an interrupt is generated. This interrupt is cleared when the data is read out of the RBR. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

7.7.13 Scratch Register

The scratch register is an 8-bit register that is intended for the programmer's use as a scratchpad in the sense that it temporarily holds the programmer's data without affecting any other ACE operation.

7.7.14 Transmitter Holding Register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by $\overline{\text{BAUDOUT}}$. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at SOUT. In the TL16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER1 = 1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

8 Application Information

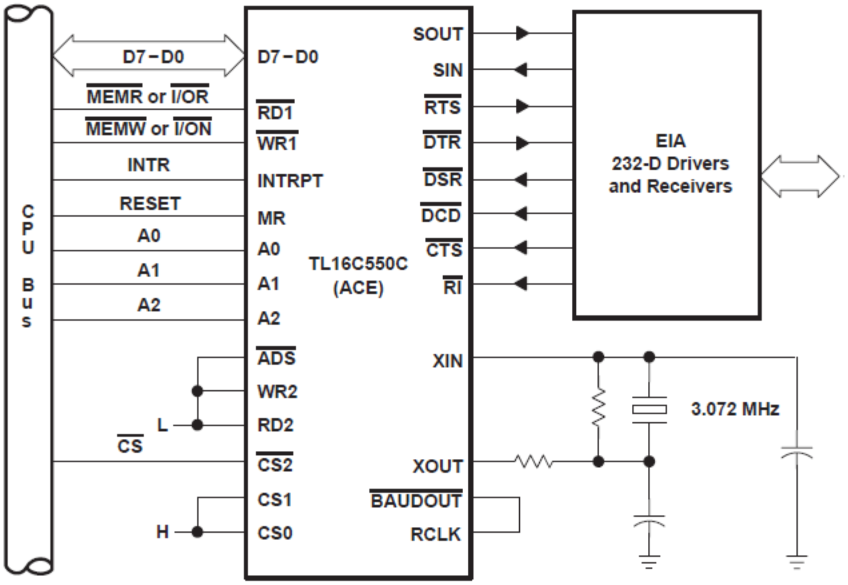


図 8-1. Basic TL16C550C Configuration

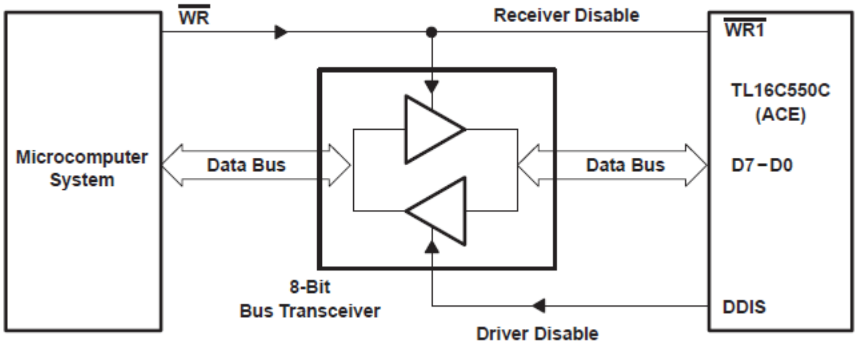


図 8-2. Typical Interface for a High Capacity Data Bus

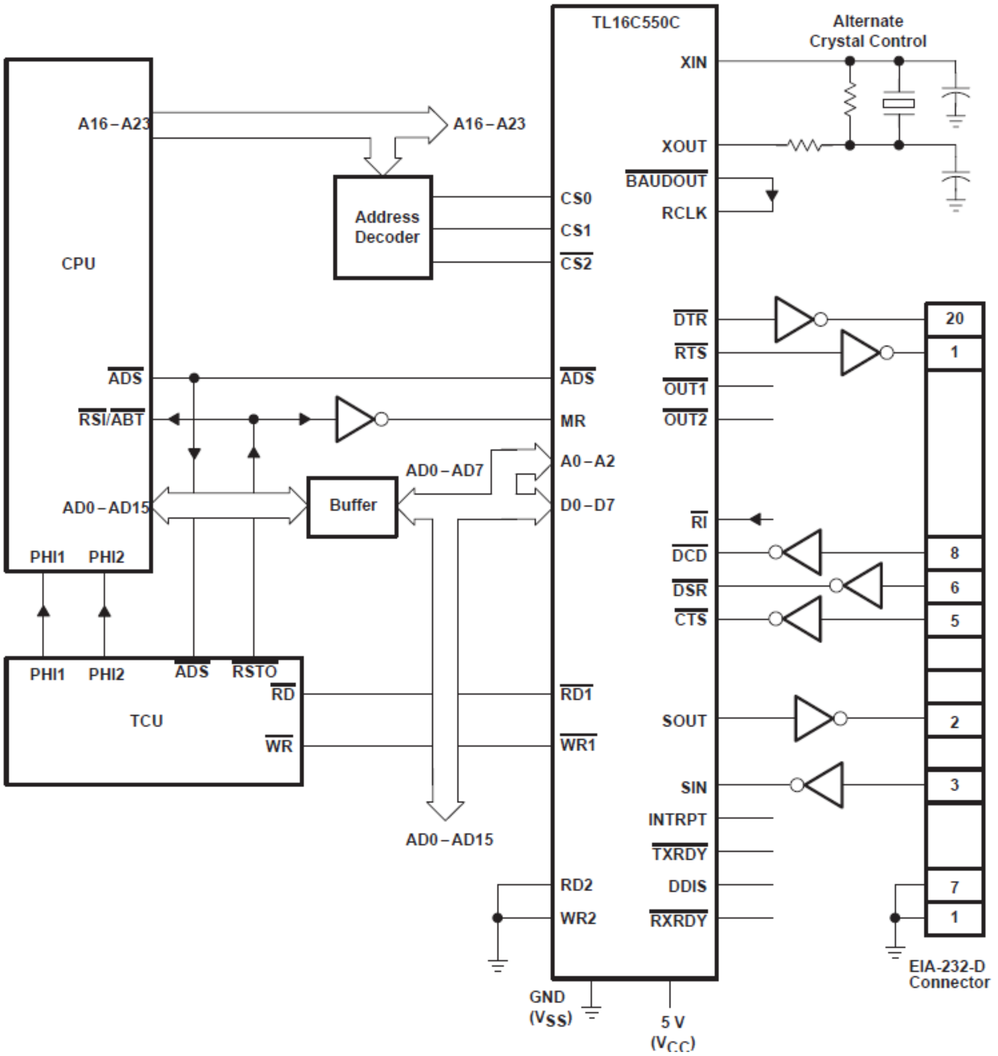


図 8-3. Typical TL16C550C Connection to a CPU

(2)

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

TI 用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL16C550CFNR	ACTIVE	PLCC	FN	44	500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TL16C550CFN	Samples
TL16C550CFNRG4	ACTIVE	PLCC	FN	44	500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TL16C550CFN	Samples
TL16C550CIFNR	ACTIVE	PLCC	FN	44	500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C550CIFN	Samples
TL16C550CIFNRG4	ACTIVE	PLCC	FN	44	500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TL16C550CIFN	Samples
TL16C550CIPTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TA550CI	Samples
TL16C550CIPTRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TA550CI	Samples
TL16C550CPFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TA550CPFB	Samples
TL16C550CPTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TA550C	Samples
TL16C550CPTRG4	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TA550C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

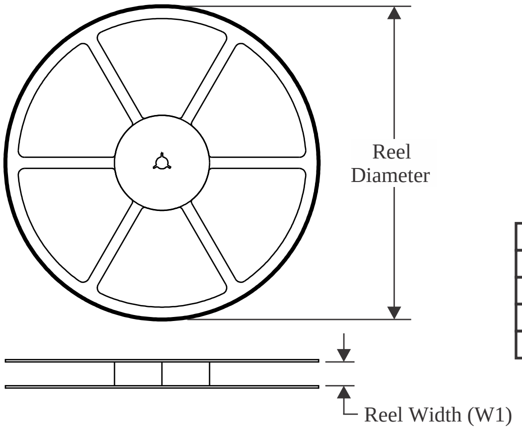
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

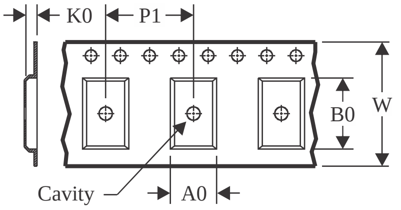
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

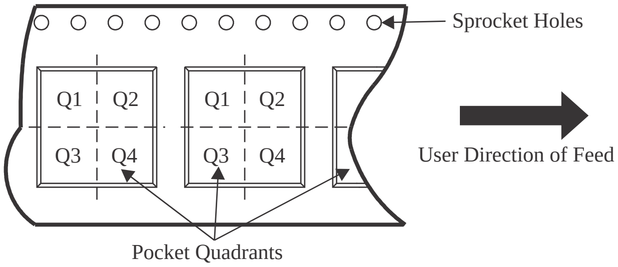


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

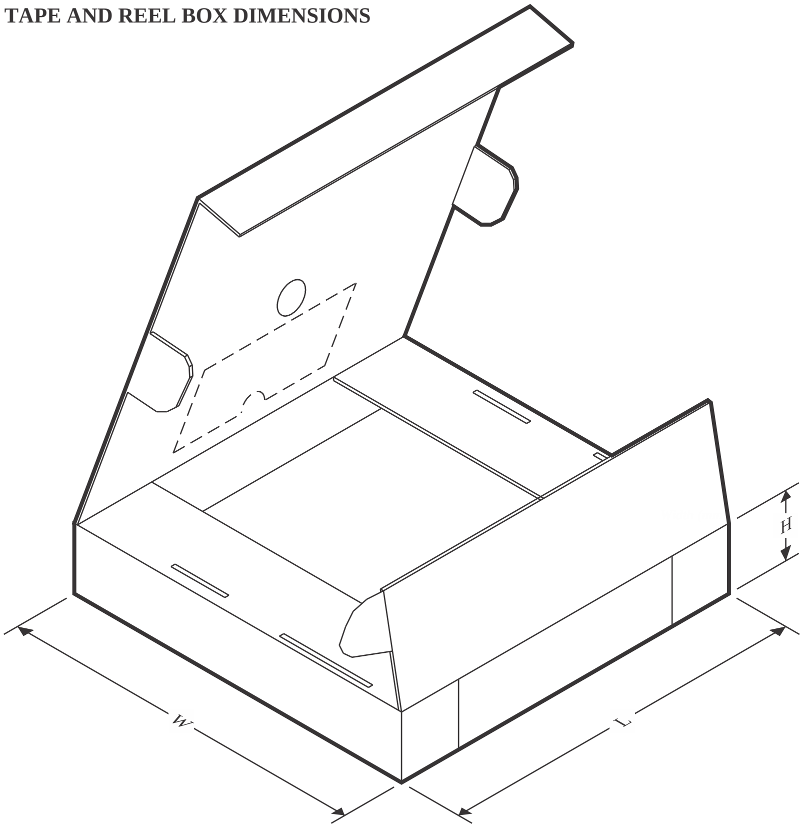
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL16C550CIPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
TL16C550CIPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
TL16C550CPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TL16C550CPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TL16C550CPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
TL16C550CPTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



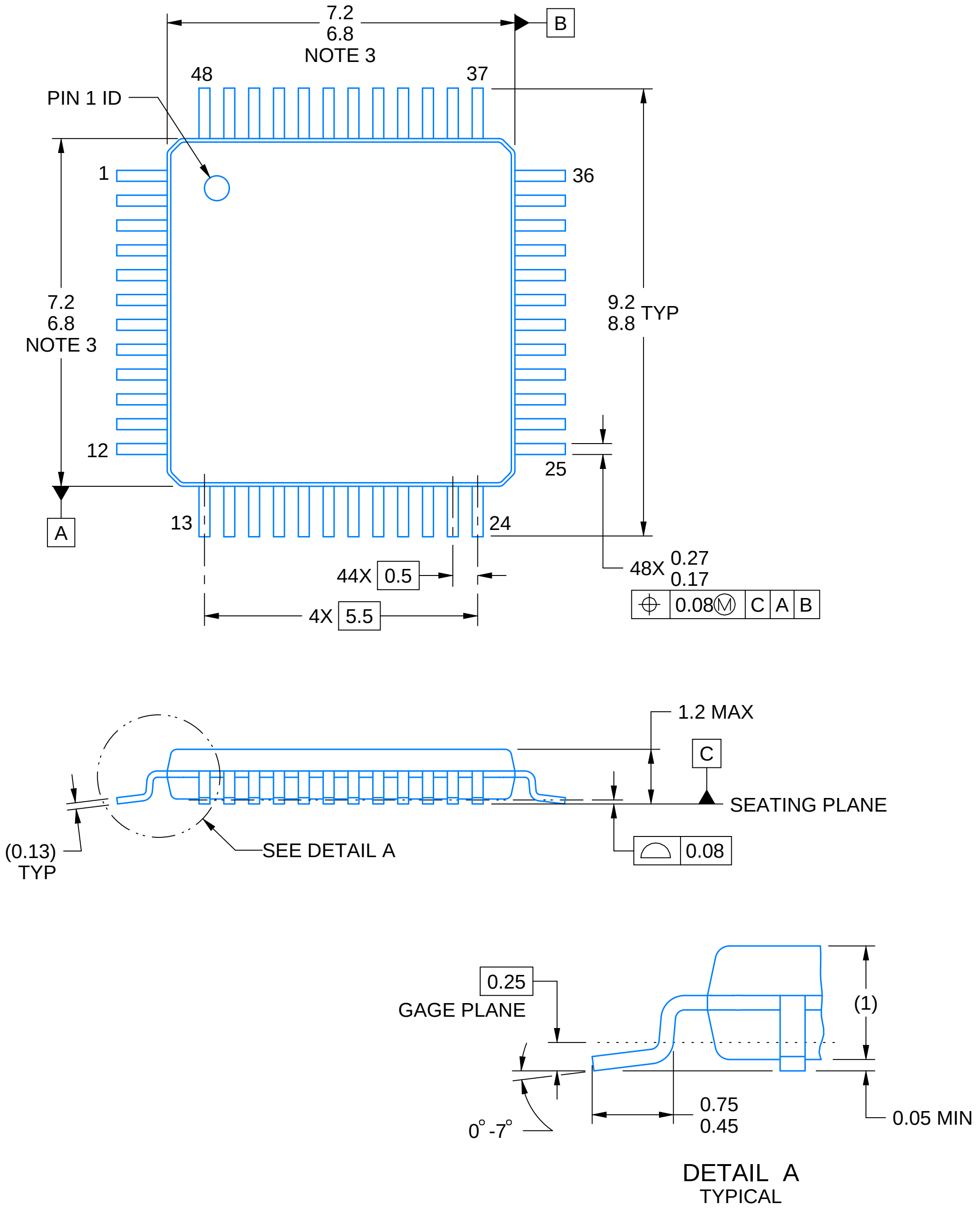
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL16C550CIPTR	LQFP	PT	48	1000	350.0	350.0	43.0
TL16C550CIPTR	LQFP	PT	48	1000	350.0	350.0	43.0
TL16C550CPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TL16C550CPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TL16C550CPTR	LQFP	PT	48	1000	350.0	350.0	43.0
TL16C550CPTR	LQFP	PT	48	1000	350.0	350.0	43.0

PACKAGE OUTLINE

TQFP - 1.2 mm max height

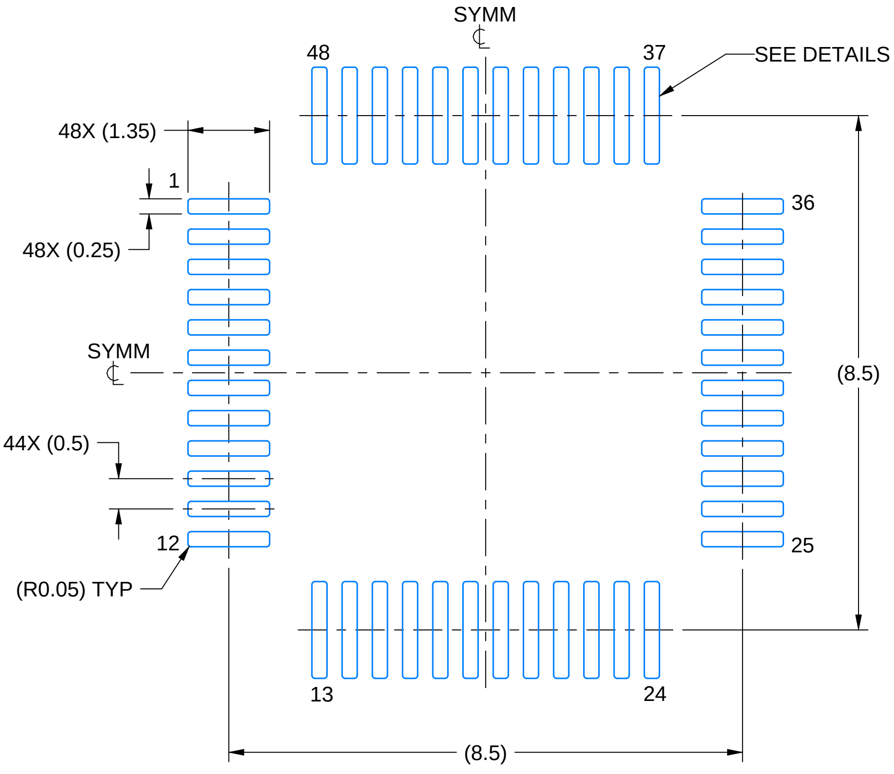
PLASTIC QUAD FLATPACK



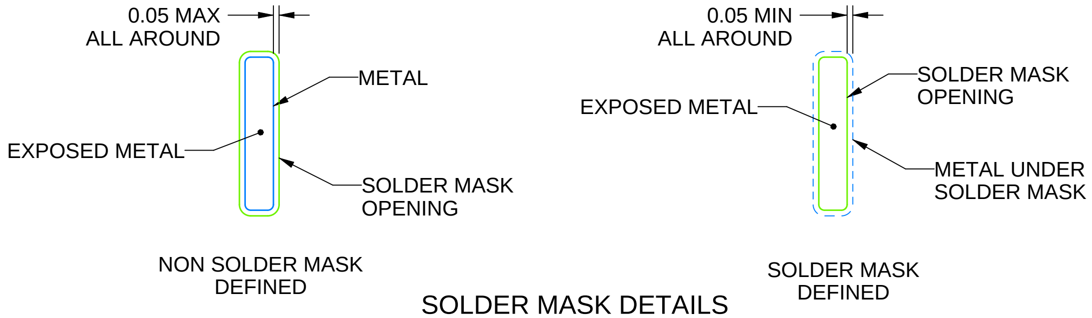
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

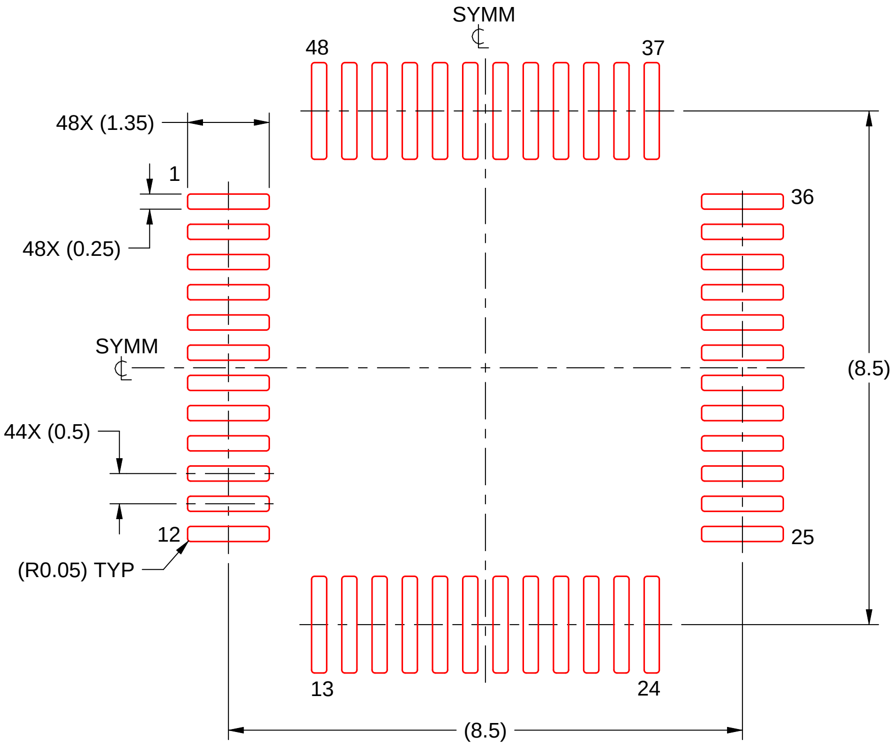


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

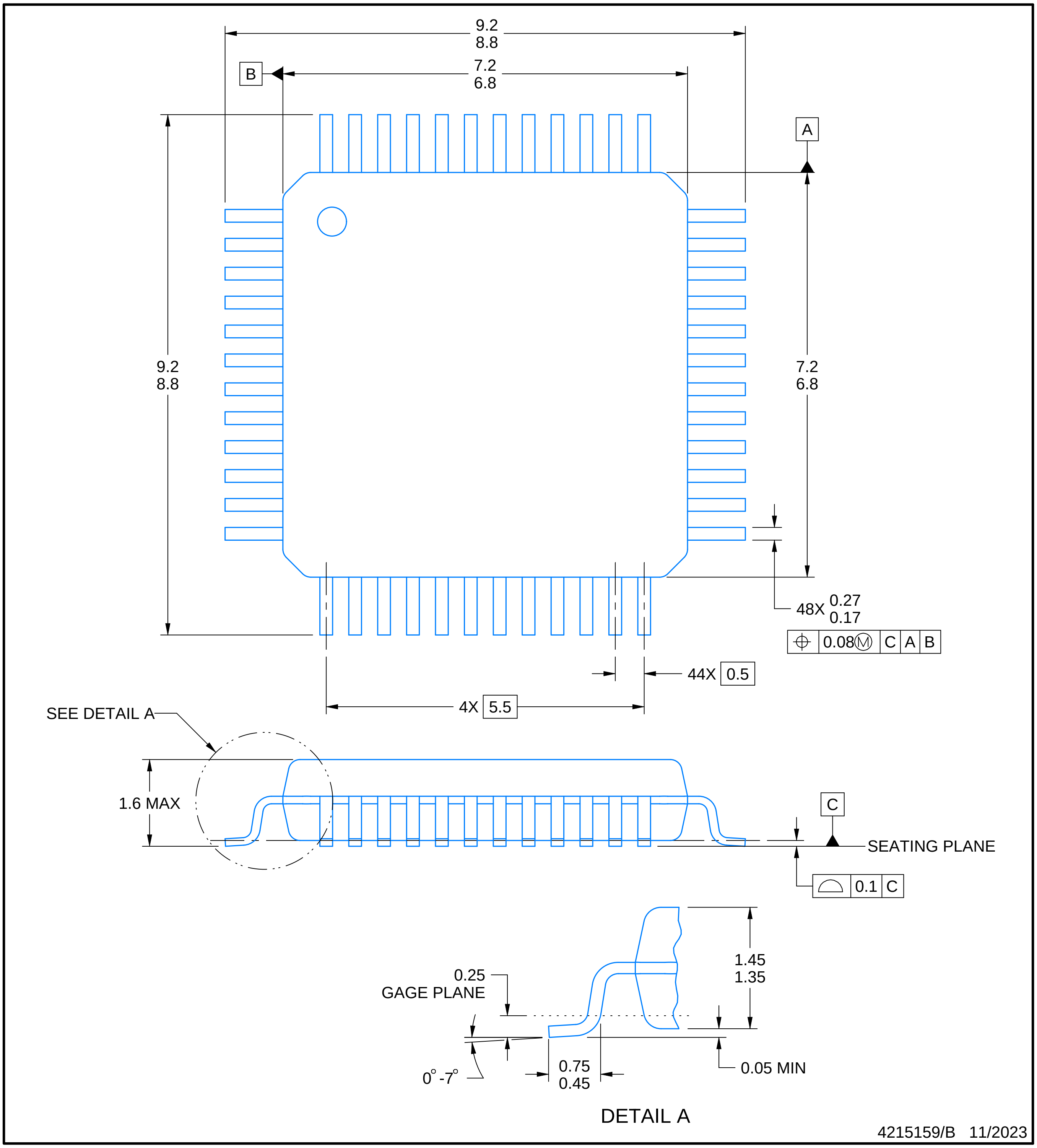


SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

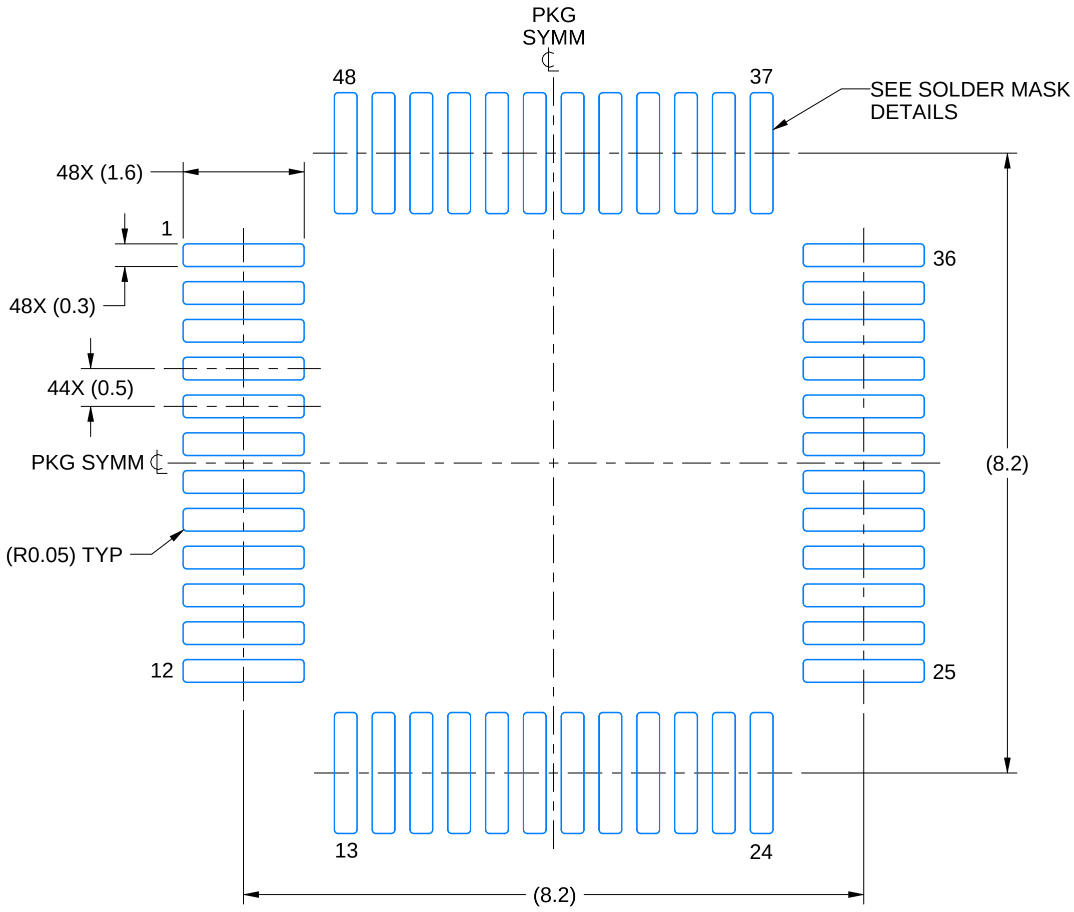
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



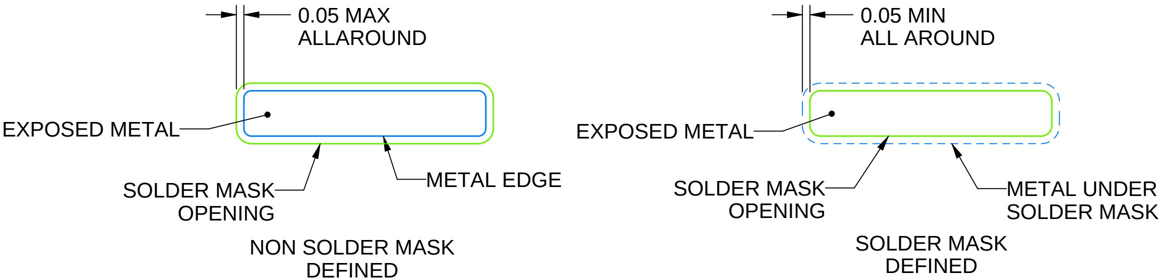
4215159/B 11/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

4215159/B 11/2023

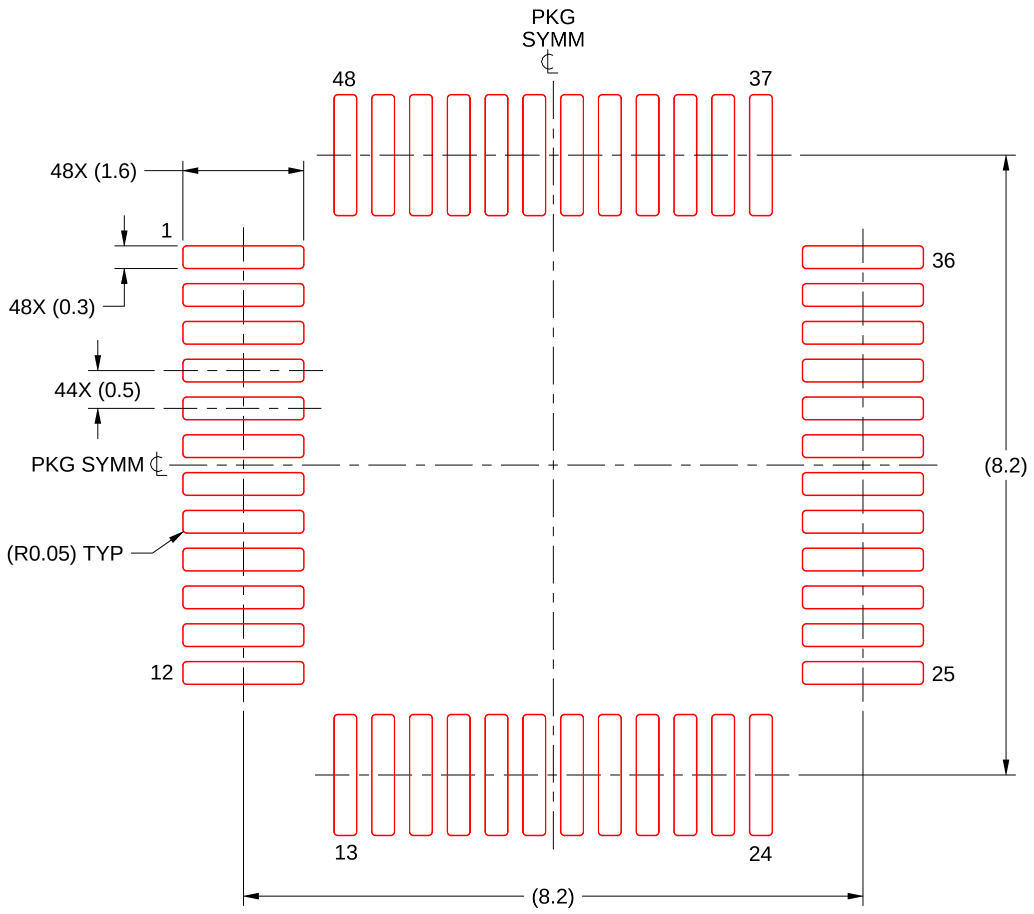
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

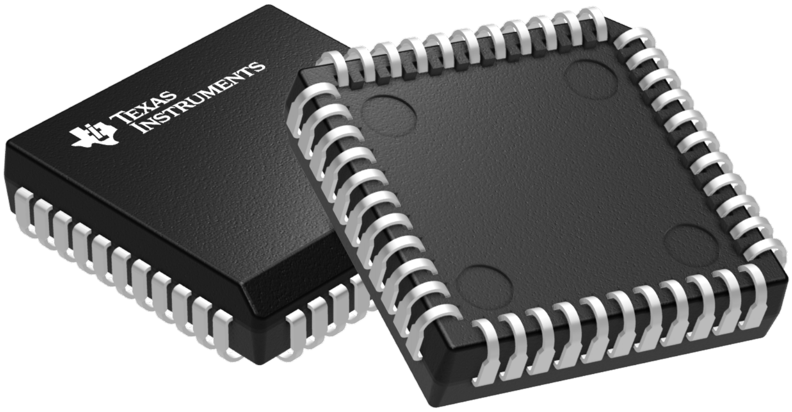
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FN 44

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

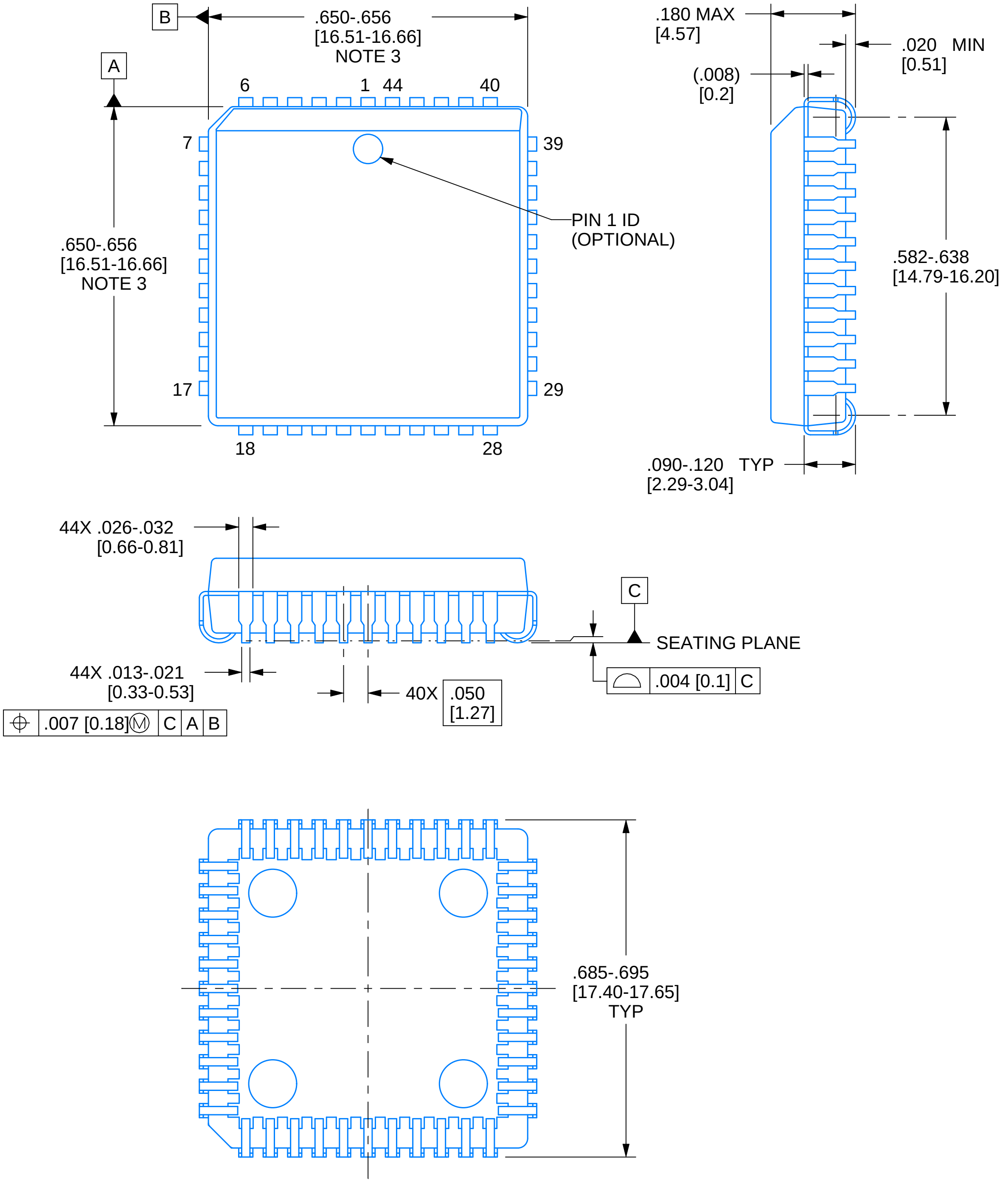
4040005-4/C

PACKAGE OUTLINE

FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



4215154/A 04/2017

NOTES:

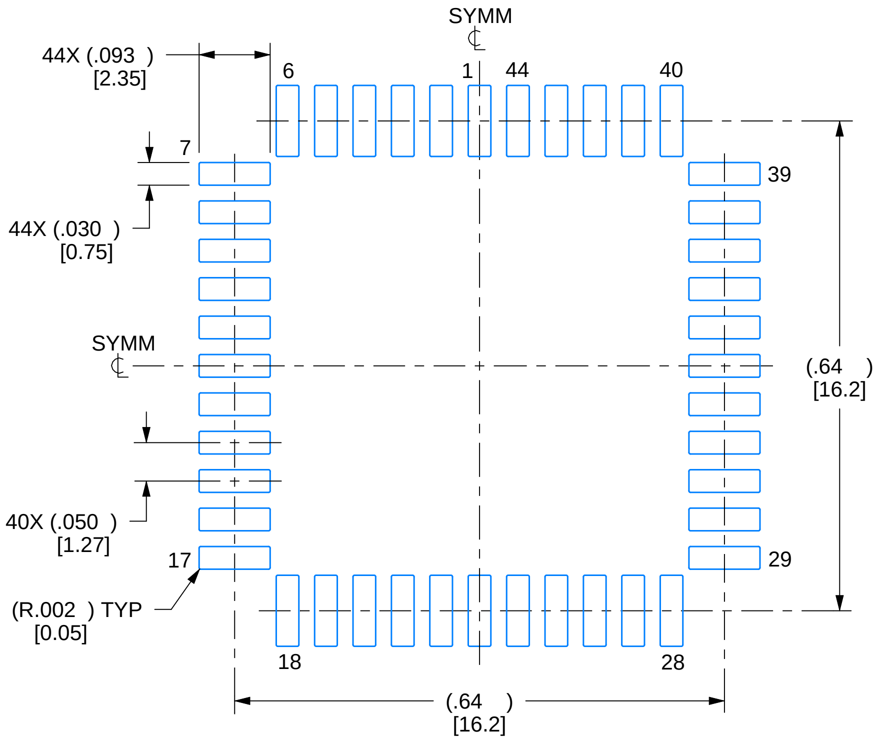
1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.

EXAMPLE BOARD LAYOUT

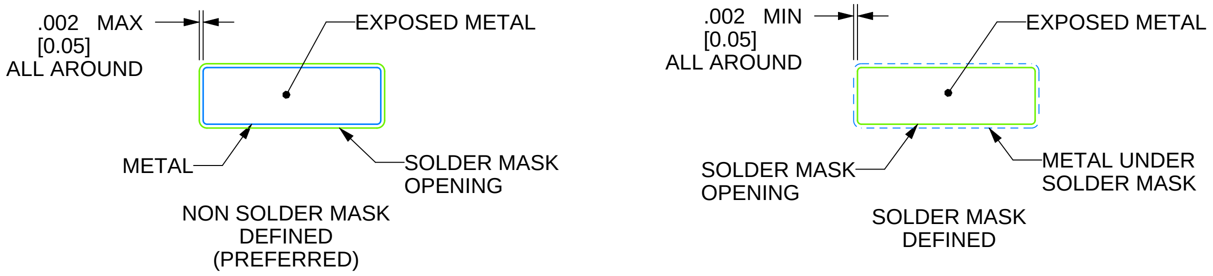
FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



NON SOLDER MASK
DEFINED
(PREFERRED)

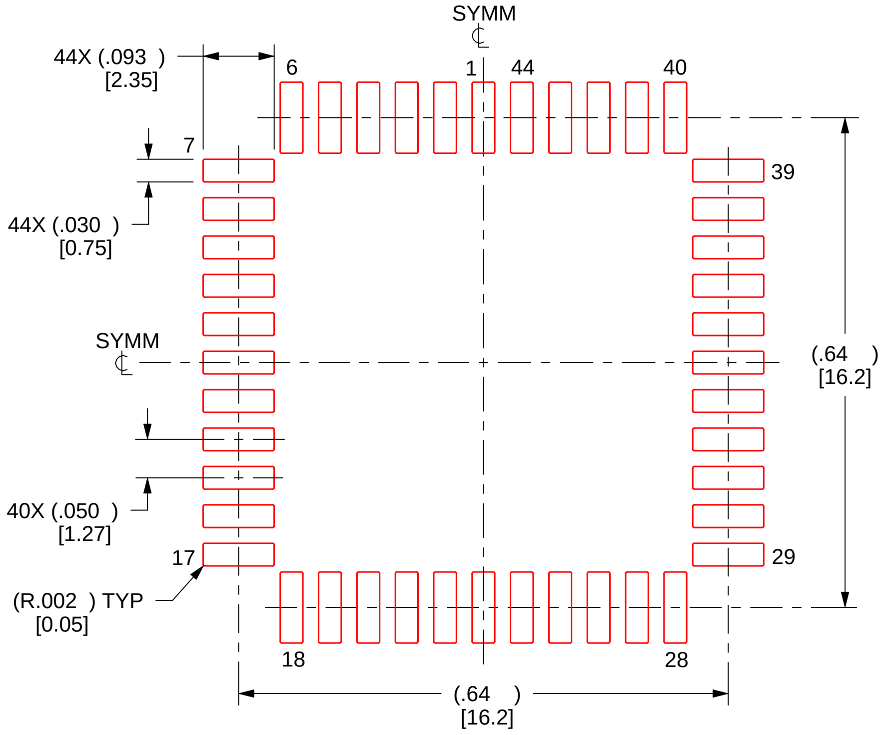
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4215154/A 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215154/A 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265