TL431-Q1/TL432-Q1 可変、高精度シャント・レギュレータ

1 特長

- 車載アプリケーションに対応
- AEC-Q100 テスト・ガイダンス
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃
- 25℃ での基準電圧の許容公差
  - 1% (A グレード)
  - 0.5% (B グレード)
- 温度ドリフト (標準値)
  - 14mV (Q 温度)
- 低い出力ノイズ
- 出力インピーダンス：0.2Ω (標準値)
- シンク電流能力：1mA～100mA
- 可変出力電圧：V_{REF}～36V

2 アプリケーション

- 可変の基準電圧および電流
- フライバック SMPS の 2 次側レギュレーション
- ツェナーの代替品
- 電圧監視
- 基準電圧内蔵のコンパレータ

3 概要

TL431LI-Q1/TL432LI-Q1 は、TL431-Q1/TL432-Q1 のピン互換の代替品です。TL43xLI-Q1 は安定性が高く、温度ドリフト (VI(dev)) が小さく、リファレンス電流 (Iref) も小さいため、システム精度が向上します。

TL431-Q1 は、該当する車載用温度範囲全体にわたって熱的に安定であることが規定された 3 ピン可変シャント・レギュレータです。出力電圧は、2 つの外付け抵抗を使用して、V_{REF} (約 2.5V) から 36V までの範囲で任意の値に設定できます (図 28 を参照)。このデバイスの出力インピーダンスは 0.2Ω (標準値) です。これらのデバイスは、アクティブ出力回路による非常に鋭い起動特性を備えているため、オンボード・レギュレーション、可変電源、スイッチング電源などの多くの用途でツェナー・ダイオードの優れた代替品となります。

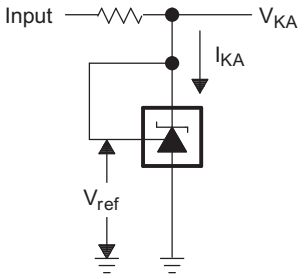
TL432-Q1 デバイスの機能と電気的仕様は TL431-Q1 デバイスと完全に同じです。しかし、DBZ パッケージのピン配置が異なります。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TL431A-Q1	SOT-23 (5)	2.90mm×1.60mm
TL43x-Q1	SOT-23 (3)	2.92mm×1.30mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (November 2016) から Revision F に変更 **Page**

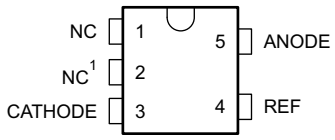
- TL431LI-Q1/TL432LI-Q1 は、TL431-Q1/TL432-Q1 のピン互換の代替品です。TL43xLI-Q1 は安定性が高く、温度ドリフト (VI(dev)) が小さく、リファレンス電流 (Iref) も小さいため、システム精度が向上します。 ... 1
- TL431-Q1 を TL432-Q1 のデータシートと結合 ... 1

Revision D (March 2013) から Revision E に変更 **Page**

- 「*アプリケーション*」セクション、「*製品情報*」表、「*ピン構成および機能*」セクション、「*仕様*」セクション、「*ESD 定格*」表、「*詳細説明*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」追加 ... 1
- データシートの末尾にあるパッケージ・オプションの*追記*を参照し、「*注文情報*」表を 削除 ... 1
- Added *Thermal Information* table ... 4
- Changed $R_{\theta JA}$ values for 5-pin DBV (SOT-23) From: 206 To: 215 and for 3-pin DBZ (SOT-23) From: 206 To: 334.7 ... 4

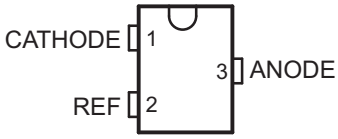
5 Pin Configuration and Functions

TL431A-Q1 DBV Package
5-Pin SOT-23
Top View

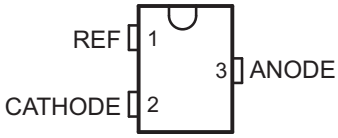


(1) Pin 2 is connected internally to ANODE (die substrate) and must be left floating or connected to ANODE.

TL431-Q1 DBZ Package
3-Pin SOT-23
Top View



TL432-Q1 DBZ Package
3-Pin SOT-23
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TL431A-Q1	TL431-Q1	TL432-Q1		
	DBV	DBZ	DBZ		
ANODE	5	3	3	O	Common pin, normally connected to ground.
CATHODE	3	1	2	I/O	Shunt current or voltage input
NC	1, 2	—	—	—	No connection(1)
REF	4	2	1	I	Threshold relative to common anode

(1) Pin 2 of the 5-pin DBV (SOT-23) package is connected internally to ANODE (die substrate) and must be left floating or connected to ANODE.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Cathode voltage(2)			37	V
Continuous cathode current		–100	150	mA
Reference input current	Low	–50		µA
	High		10	mA
Operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the ANODE pin, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM)	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{KA}	Cathode voltage	V_{REF}	36	V
I_{KA}	Cathode current	1	100	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TL43x-Q1		UNIT
		DBV (SOT-23)	DBZ (SOT-23)	
		5 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	215	334.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	135.2	113.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43	67.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.6	6.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.1	65.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: TL43x-Q1

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_{KA} = 10 mA, see Figure 20		2440	2495	2550	mV
$V_{I(DEV)}$	Deviation of reference voltage over full temperature(1)	$V_{KA} = V_{REF}$, I_{KA} = 10 mA, T_A = –40°C to 125°C, see Figure 20			14	34	mV
$\Delta V_{REF}/\Delta V_{KA}$	Ratio of change in reference voltage to the change in cathode voltage	I_{KA} = 10 mA, see Figure 21	ΔV_{KA} = 10 V – V_{REF}		–1.4	–2.7	mV/V
			ΔV_{KA} = 36 V – 10 V		–1	–2	

(1) The deviation parameters ($V_{I(DEV)}$ and $I_{I(DEV)}$) are defined as the differences between the maximum and minimum values obtained over the recommended temperature range.

Electrical Characteristics: TL43x-Q1 (continued)

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{REF}	Reference current	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, see Figure 21		2	4	µA
$I_{I(DEV)}$	Deviation of reference current over full temperature(1)	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = –40°C to 125°C, see Figure 21		0.8	2.5	µA
I_{MIN}	Minimum cathode current for regulation	V_{KA} = V_{REF}, see Figure 20		0.4	1	mA
I_{OFF}	OFF-state cathode current	V_{KA} = 36 V, V_{REF} = 0, see Figure 22		0.1	1	µA
$\|Z_{KA}\|$	Dynamic impedance(1)	I_{KA} = 1 mA to 100 mA, V_{KA} = V_{REF}, f ≤ 1 kHz, see Figure 20		0.2	0.5	Ω

6.6 Electrical Characteristics: TL43xA-Q1

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	V_{KA} = V_{REF}, I_{KA} = 10 mA, see Figure 20		2470	2495	2520	mV
$V_{I(DEV)}$	Deviation of reference voltage over full temperature(1)	V_{KA} = V_{REF}, I_{KA} = 10 mA, T_A = –40°C to 125°C, see Figure 20			14	34	mV
$\Delta V_{REF}/\Delta V_{KA}$	Ratio of change in reference voltage to the change in cathode voltage	I_{KA} = 10 mA, see Figure 21	ΔV_{KA} = 10 V – V_{REF}		–1.4	–2.7	mV/V
			ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{REF}	Reference current	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, see Figure 21			2	4	µA
$I_{I(DEV)}$	Deviation of reference current over full temperature(1)	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = –40°C to 125°C, see Figure 21			0.8	2.5	µA
I_{MIN}	Minimum cathode current for regulation	V_{KA} = V_{REF}, see Figure 20			0.4	0.7	mA
I_{OFF}	OFF-state cathode current	V_{KA} = 36 V, V_{REF} = 0, see Figure 22			0.1	0.5	µA
$\|Z_{KA}\|$	Dynamic impedance(1)	I_{KA} = 1 mA to 100 mA, V_{KA} = V_{REF}, f ≤ 1 kHz, see Figure 20			0.2	0.5	Ω

(1) The deviation parameters ($V_{I(DEV)}$ and $I_{I(DEV)}$) are defined as the differences between the maximum and minimum values obtained over the recommended temperature range.

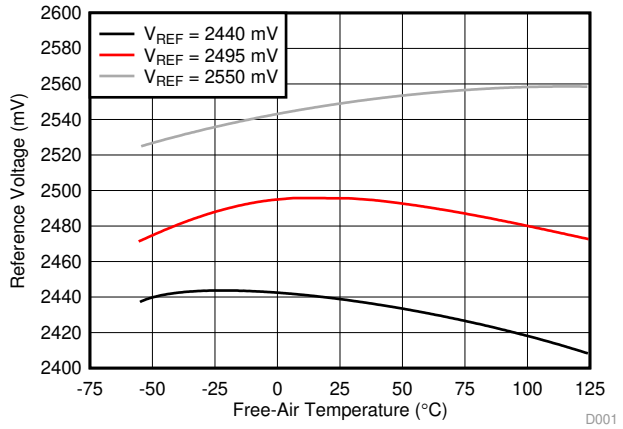
6.7 Electrical Characteristics: TL43xB-Q1

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	V_{KA} = V_{REF}, I_{KA} = 10 mA, see Figure 20		2483	2495	2507	mV
$V_{I(DEV)}$	Deviation of reference voltage over full temperature(1)	V_{KA} = V_{REF}, I_{KA} = 10 mA, T_A = –40°C to 125°C, see Figure 20			14	34	mV
$\Delta V_{REF}/\Delta V_{KA}$	Ratio of change in reference voltage to the change in cathode voltage	I_{KA} = 10 mA, see Figure 21	ΔV_{KA} = 10 V – V_{REF}		–1.4	–2.7	mV/V
			ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{REF}	Reference current	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, see Figure 21			2	4	µA
$I_{I(DEV)}$	Deviation of reference current over full temperature(1)	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = –40°C to 125°C, see Figure 21			0.8	2.5	µA
I_{MIN}	Minimum cathode current for regulation	V_{KA} = V_{REF}, see Figure 20			0.4	0.7	mA
I_{OFF}	OFF-state cathode current	V_{KA} = 36 V, V_{REF} = 0, see Figure 22			0.1	0.5	µA
$\|Z_{KA}\|$	Dynamic impedance(1)	I_{KA} = 1 mA to 100 mA, V_{KA} = V_{REF}, f ≤ 1 kHz, see Figure 20			0.2	0.5	Ω

(1) The deviation parameters ($V_{I(DEV)}$ and $I_{I(DEV)}$) are defined as the differences between the maximum and minimum values obtained over the recommended temperature range.

6.8 Typical Characteristics



Data is for devices having the indicated value of V_{REF} at I_{KA} = 10 mA, T_A = 25°C.

Figure 1. Reference Voltage vs Free-air Temperature

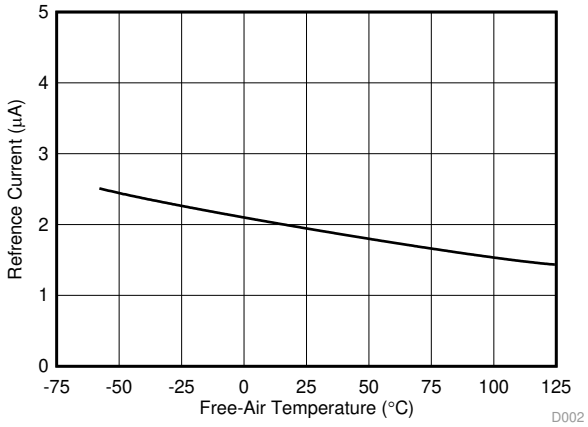


Figure 2. Reference Current vs Free-air Temperature

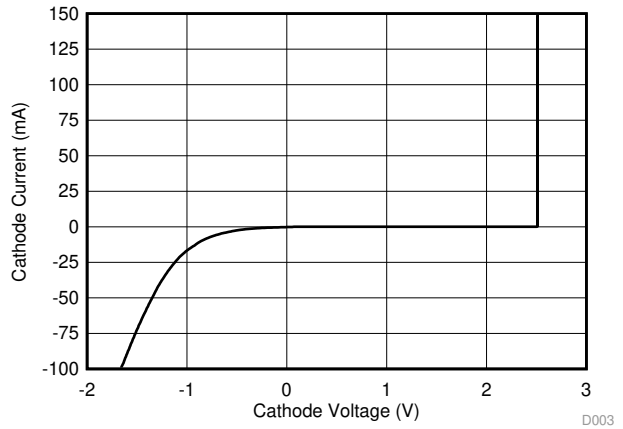


Figure 3. Cathode Current vs Cathode Voltage

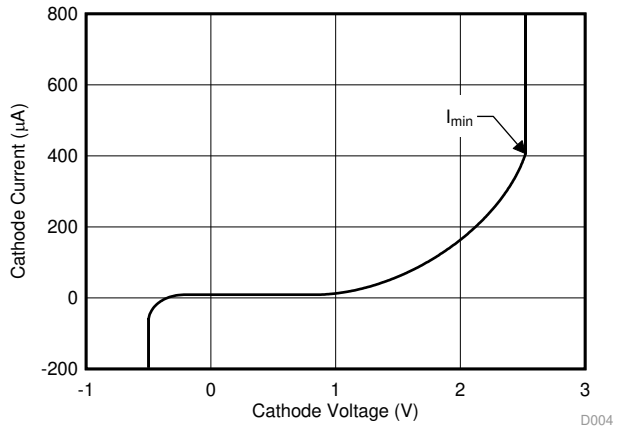


Figure 4. Cathode Current vs Cathode Voltage

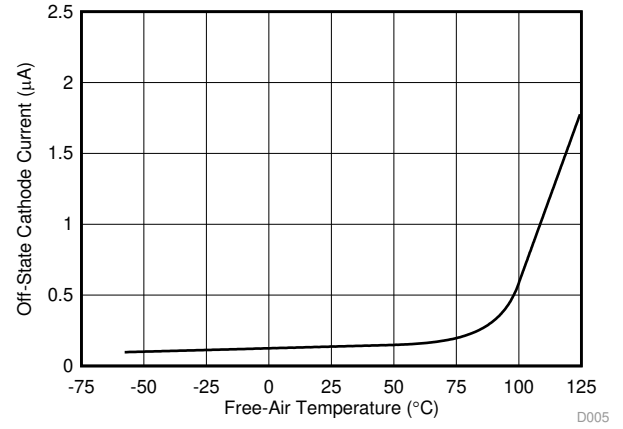


Figure 5. OFF-State Cathode Current vs Free-air Temperature

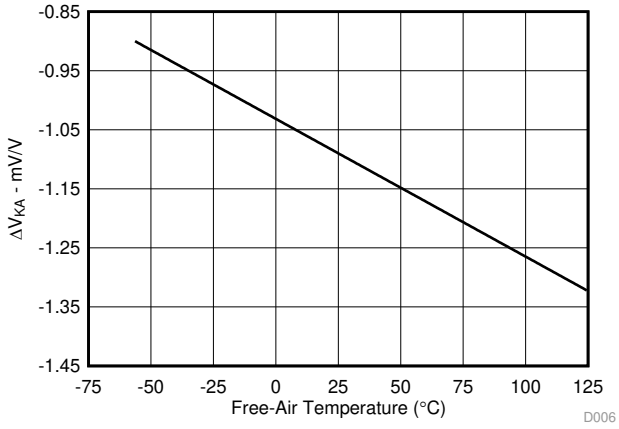


Figure 6. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Free-air Temperature

Typical Characteristics (continued)

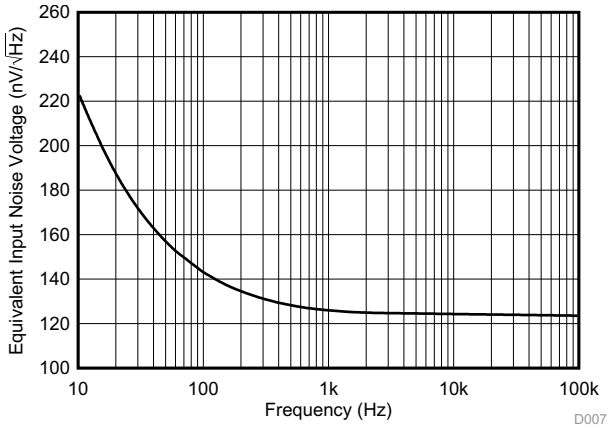


Figure 7. Equivalent Input Noise Voltage vs Frequency

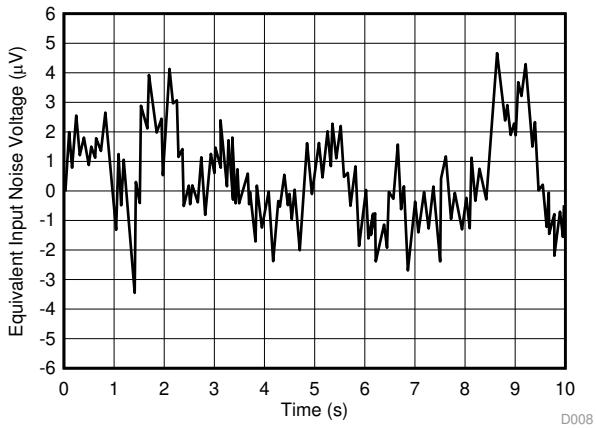


Figure 8. Equivalent Input Noise Voltage Over a 10-s Period

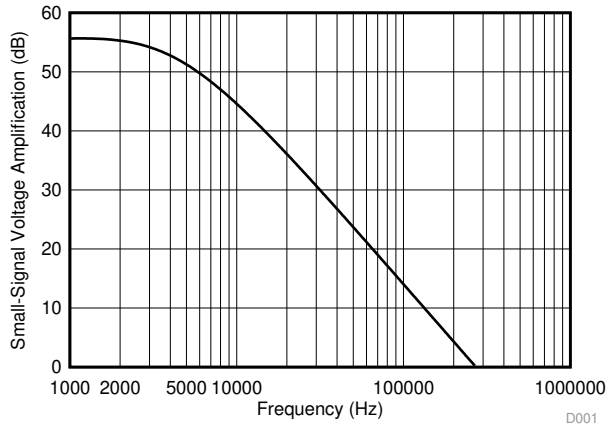


Figure 9. Small-Signal Voltage Amplification vs Frequency

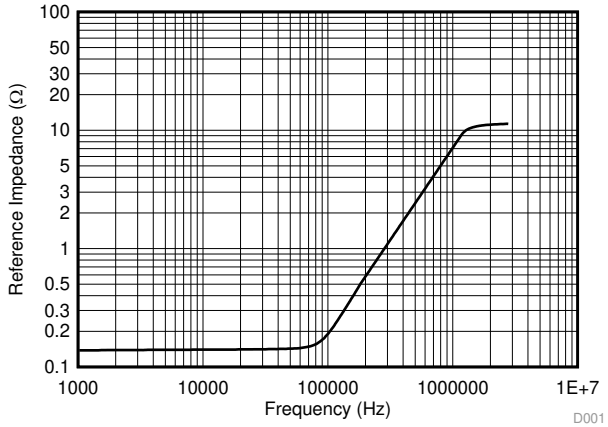


Figure 10. Reference Impedance vs Frequency

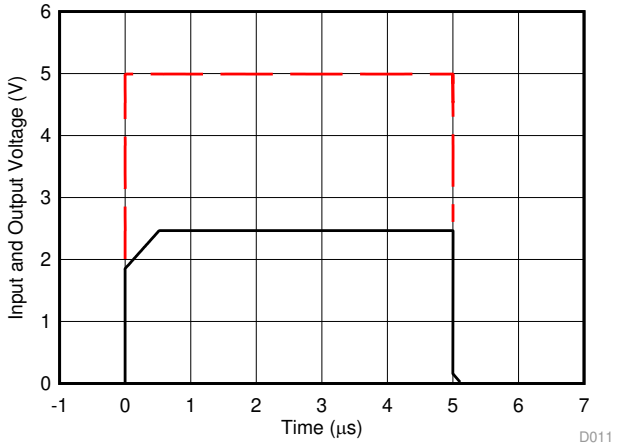
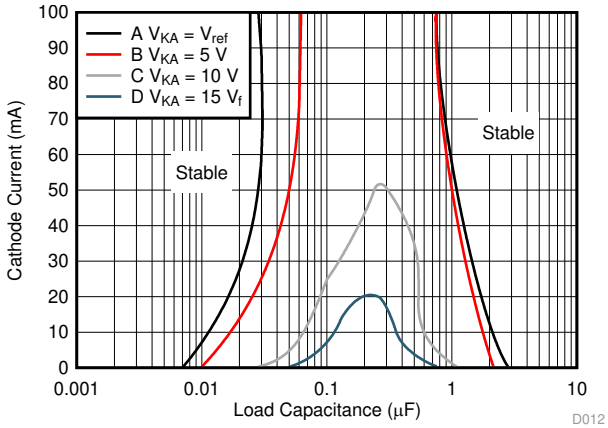


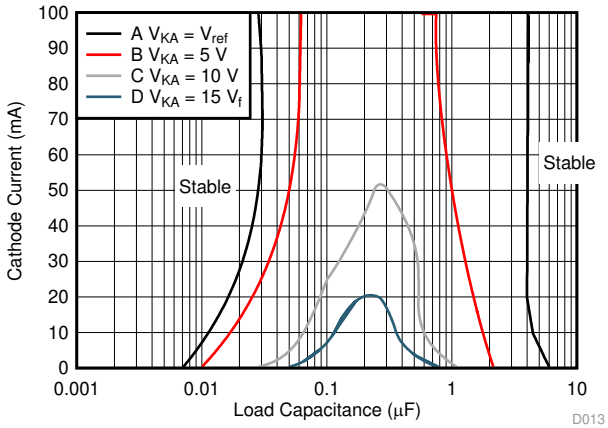
Figure 11. Pulse Response



The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V_{REF} were adjusted to establish the initial V_{KA} and I_{KA} conditions with C_L = 0. V_{BATT} and C_L then were adjusted to determine the ranges of stability (see Figure 18 and Figure 19 for test circuits).

Figure 12. Stability Boundary Conditions for All TL43x Devices (Except for SOT23-3, SC-70, and Q-TEMP Devices)

Typical Characteristics (continued)



The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V_{REF} were adjusted to establish the initial V_{KA} and I_{KA} conditions with C_L = 0. V_{BATT} and C_L then were adjusted to determine the ranges of stability (see Figure 18 and Figure 19 for test circuits).

Figure 13. Stability Boundary Conditions for All TL43x, SOT-23, SC-70, and Q-TEMP Devices

7 Parameter Measurement Information

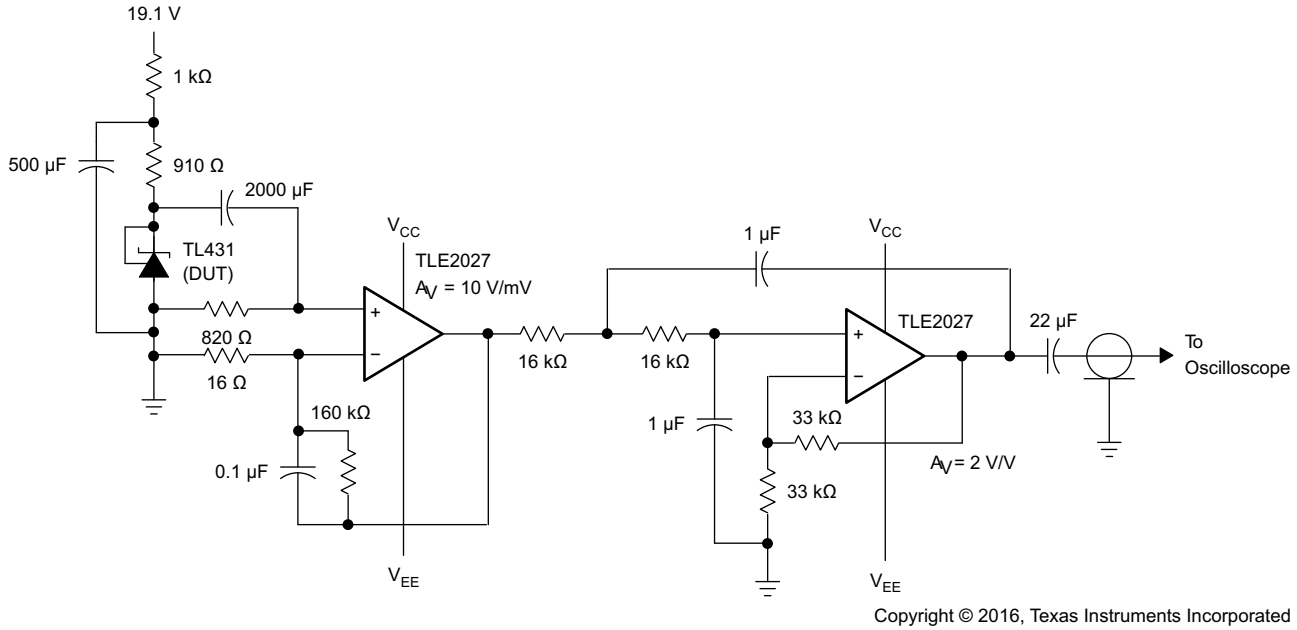


Figure 14. Test Circuit for Equivalent Input Noise Voltage

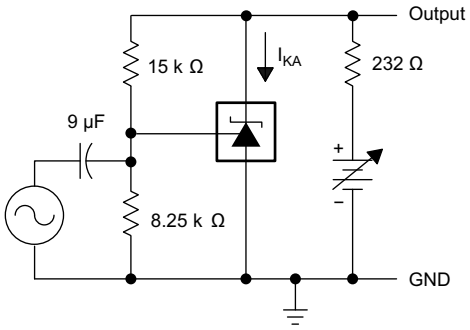


Figure 15. Test Circuit for Voltage Amplification

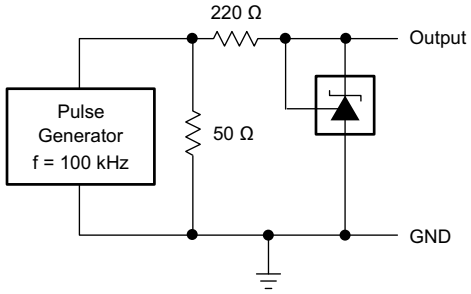


Figure 17. Test Circuit for Pulse Response

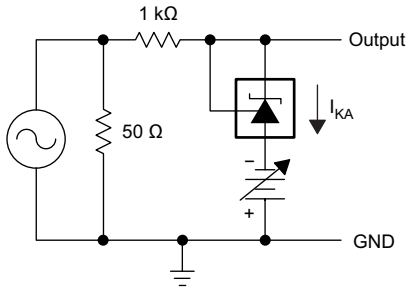


Figure 16. Test Circuit for Reference Impedance

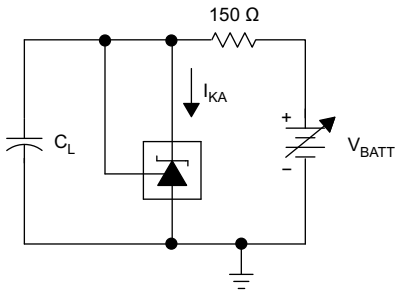


Figure 18. Test Circuit for Curve A

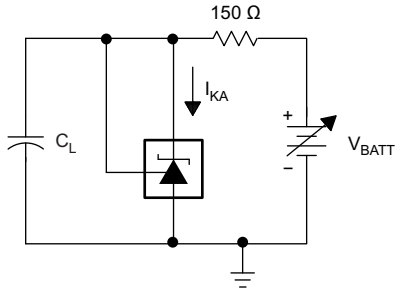


Figure 19. Test Circuit for Curves B, C, and D

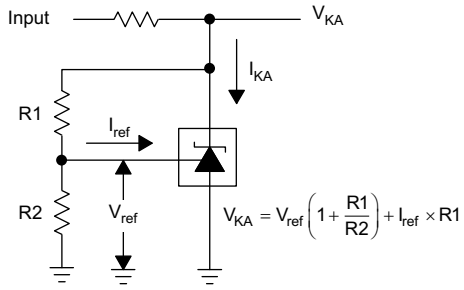


Figure 21. Test Circuit for $V_{KA} > V_{REF}$

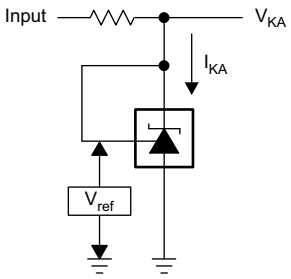


Figure 20. Test Circuit for $V_{KA} = V_{REF}$

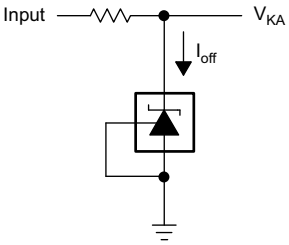


Figure 22. Test Circuit for I_{OFF}

8 Detailed Description

8.1 Overview

This device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This is due to its key components containing an accurate voltage reference and op amp, which are fundamental analog building blocks. The TL43x-Q1 can be used as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference.

The TL43x-Q1 can be operated and adjusted to cathode voltages from 2.5 V to 36 V, making this part optimum for a wide range of end equipments in industrial, auto, telecommunications, and computing. For this device to behave as a shunt regulator or error amplifier, at least 1 mA ($I_{MIN(MAX)}$) must be supplied to the cathode pin. Under this condition, feedback can be applied from the CATHODE and REF pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5% and 1%. These reference options are denoted by B (0.5%) or A (1%) in the part number (TL431x-Q1).

8.2 Functional Block Diagram

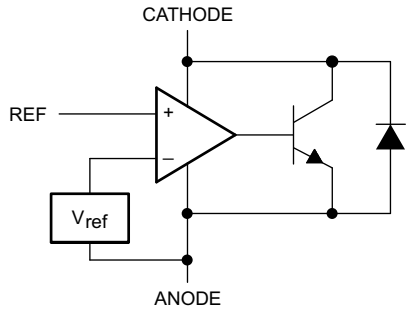
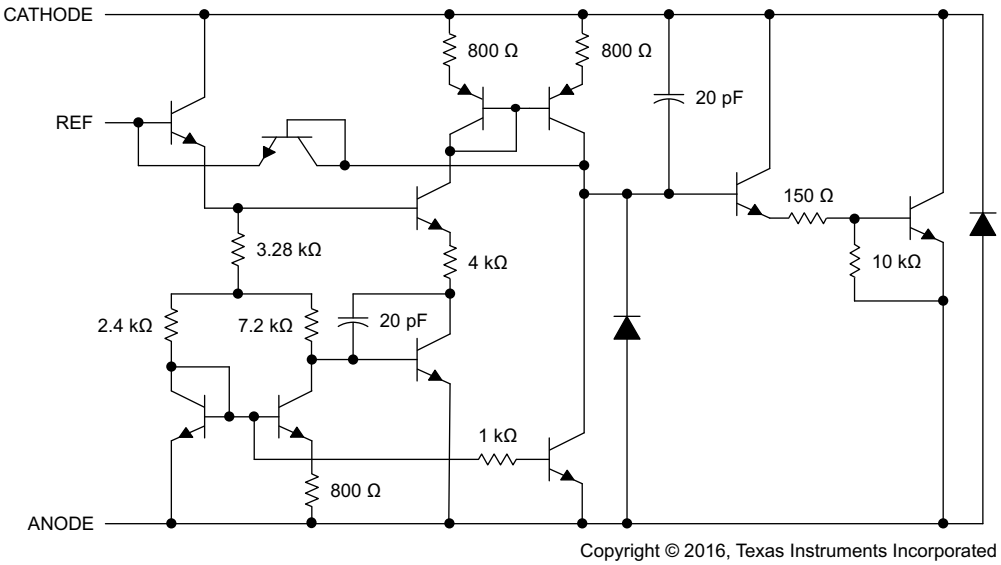


Figure 23. Equivalent Schematic



All component values are nominal.

Figure 24. Detailed Schematic

8.3 Feature Description

The TL43x-Q1 consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, shown in Figure 24. A Darlington pair is used to allow this device to sink a maximum current of 100 mA.

When operated with enough voltage headroom (at least 2.5 V) and cathode current (I_{KA}), the TL43x-Q1 forces the reference pin to 2.5 V. However, the reference pin can not be left floating, as I_{REF} must be at least 4 µA (see *Specifications*). This is because the reference pin is driven into an NPN, which requires base current to operate properly.

When feedback is applied from the CATHODE and REF pins, the TL43x-Q1 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current required in the above feedback situation must be applied to this device in open loop, servo, or error amplifying implementations for it to be in the proper linear region giving the device enough gain.

Unlike many linear regulators, the TL43x-Q1 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor Figure 24 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

8.4 Device Functional Modes

8.4.1 Open Loop (Comparator)

When the cathode or output voltage or current of the TL43x-Q1 is not being fed back to the reference or input pin in any form, the device operates in open loop. With proper cathode current (I_{KA}) applied to this device, the TL43x-Q1 has the characteristics shown in Figure 24. With such high gain in this configuration, the device is typically used as a comparator. The integrated reference makes TL43x the prefered choice when trying to monitor a certain level of a single signal.

8.4.2 Closed Loop

When the cathode or output voltage or current of the TL43x-Q1 is being fed back to the reference or input pin in any form, the device operates in closed loop. The majority of applications involving the TL43x-Q1 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

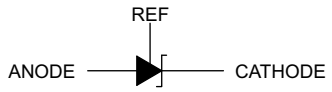


Figure 25. Logic Symbol

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

As this device has many applications and setups, there are many situations that this data sheet can not characterize in detail. The linked application notes help the make the best choices when using this part.

Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet provides a deeper understanding of this devices stability characteristics and aid the user in making the right choices when choosing a load capacitor. *Setting the Shunt Voltage on an Adjustable Shunt Regulator* assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

9.2 Typical Applications

9.2.1 Comparator Application

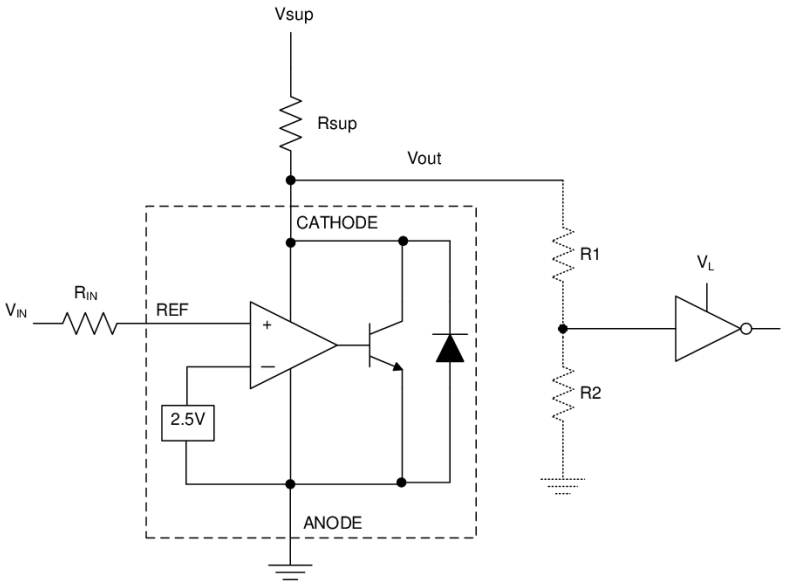


Figure 26. Comparator Application Schematic

Typical Applications (continued)

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage	0 V to 5 V
Input resistance	10 kΩ
Supply voltage	24 V
Cathode current, I_K	5 mA
Output voltage level	Approximately 2 V to V_{SUP}
Logic input thresholds, V_{IH} / V_{IL}	V_L

9.2.1.2 Detailed Design Procedure

When using the TL43x-Q1 as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

9.2.1.2.1 Basic Operation

In the configuration shown in Figure 26 the TL43x-Q1 behaves as a comparator, comparing the REF pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_{KA}), the TL43x-Q1 has enough open loop gain to provide a quick response. This is shown in Figure 27, where the R_{SUP} = 10 kΩ (I_{KA} = 500 µA) situation responds much slower than R_{SUP} = 1 kΩ (I_{KA} = 5 mA). With the TL43x-Q1's maximum operating current (I_{MIN}) being 1 mA, operation below that could result in low gain, leading to a slow response.

9.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage is within the range of 2.5 V ± (0.5%, 1%, or 1.5%) depending on which version is being used. The more overdrive voltage provided, the faster the TL43x-Q1 responds.

For applications where the TL43x-Q1 is being used as a comparator, it is best to set the trip point to greater than the positive expected error (for example: +1% for the A version). For fast response, setting the trip point to at least 10% of the internal V_{REF} should suffice.

For minimal drop or difference from V_{INREF} to the REF pin, TI recommends using an input resistor <10 kΩ to provide I_{REF}

9.2.1.2.3 Output Voltage and Logic Input Level

For the TL43x-Q1 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL}.

As seen in Figure 26, the TL43x-Q1's output low level voltage in open-loop or comparator mode is approximately 2 V, which is typically sufficient for 5-V supplied logic. However, would not work for 3.3-V and 1.8-V supplied logic. To accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

The TL43x-Q1's output high voltage is equal to V_{SUP} due to the TL43x-Q1 being open-collector. If V_{SUP} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, ensure the sum of the resistive divider (R1 and R2 in Figure 24) is much greater than R_{SUP} to not interfere with the TL43x-Q1's ability to pull close to V_{SUP} when turning off.

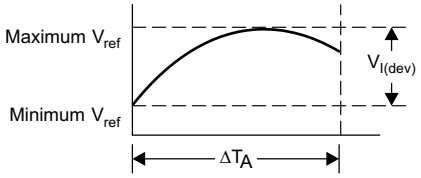
9.2.1.2.4 Input Resistance

In this application, the TL43x-Q1 requires an input resistance in addition to the reference current (I_{REF}) to ensure the device is in the proper operating regions while turning on. The actual voltage seen at the REF pin is $V_{REF} = V_{IN} – I_{REF} \times R_{IN}$. Because I_{REF} can be as high as 4 µA, TI recommends using a resistance small enough to mitigate the error that I_{REF} creates from V_{IN}.

9.2.1.2.5 Deviation Parameters and Calculating Dynamic Impedance

The deviation parameters, $V_{I(DEV)}$ and $I_{I(DEV)}$, are defined as the differences between the maximum and minimum values obtained over the recommended temperature range. The average full-range temperature coefficient of the reference voltage (α_{Vref}) is defined in Equation 1.

$$\left|\alpha_{V_{ref}}\right| \frac{ppm}{^{\circ}C} = \frac{\left(\frac{V_{I(dev)}}{V_{ref}\,\text{at } 25^{\circ}C}\right) \times 10^6}{\Delta T_A}$$



where

- ΔT_A is the recommended operating free-air temperature range of the device (1)

α_{Vref} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

Example:

Maximum V_{REF} = 2496 mV at 30°C, minimum V_{REF} = 2492 mV at 0°C, V_{REF} = 2495 mV at 25°C, ΔT_A = 70°C for TL43x.

$$\left|\alpha_{V_{ref}}\right| = \frac{\left(\frac{4\text{ mV}}{2495\text{ mV}}\right) \times 10^6}{70^{\circ}C} \approx \frac{23\text{ ppm}}{^{\circ}C} \quad (2)$$

Because minimum V_{REF} occurs at the lower temperature, the coefficient is positive.

The dynamic impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_{KA}$.

When the device is operating with two external resistors, see Figure 21, the total dynamic impedance of the circuit is given by Equation 3.

$$\left|z'\right| = \frac{\Delta V}{\Delta I} \approx \left|Z_{KA}\right| \left(1 + \frac{R1}{R2}\right) \quad (3)$$

9.2.1.3 Application Curve

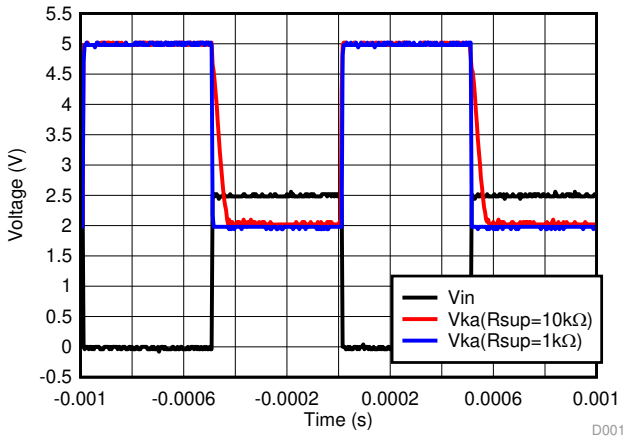
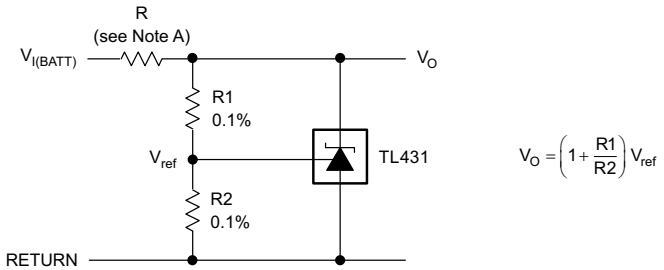


Figure 27. Output Response With Various Cathode Currents

9.2.2 Other Application Circuits

Figure 28 to Figure 40 show application circuit examples using the TL431-Q1 device. Customers must fully validate and test any circuit before implementing a design based on an example in this section. Unless otherwise noted, the design procedures in *Comparator Application* are applicable.



A. R must provide cathode current ≥1 mA to the TL431-Q1 at minimum $V_{I(BATT)}$.

Figure 28. Shunt Regulator

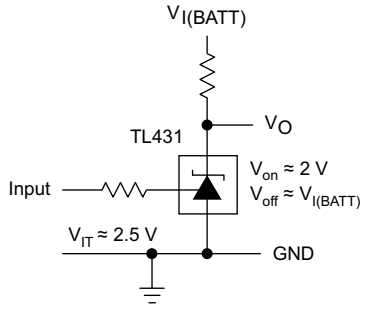
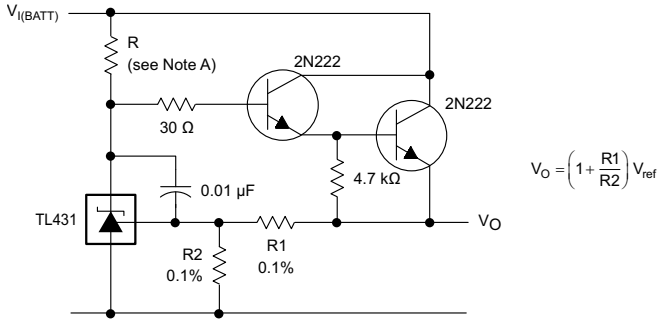


Figure 29. Single-Supply Comparator with Temperature-Compensated Threshold



A. R must provide cathode current ≥1 mA to the TL431-Q1 at minimum $V_{I(BATT)}$.

Figure 30. Precision High-Current Series Regulator

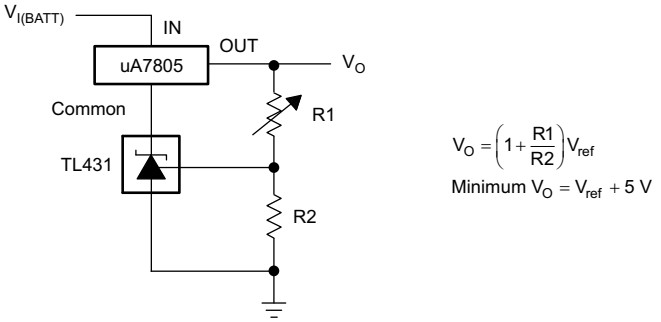


Figure 31. Output Control of a Three-Terminal Fixed Regulator

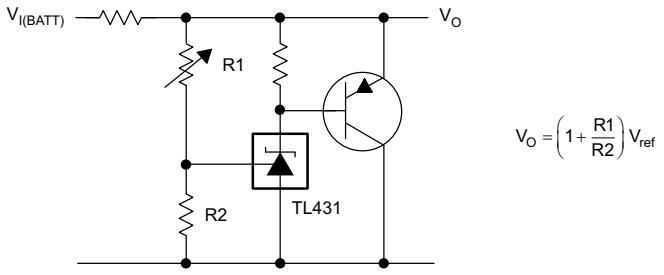
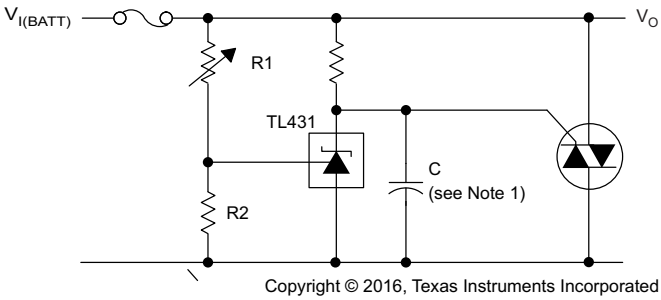


Figure 32. High-Current Shunt Regulator



(1) See Figure 12 and Figure 13 to determine allowable values for C.

Figure 33. Crowbar Circuit

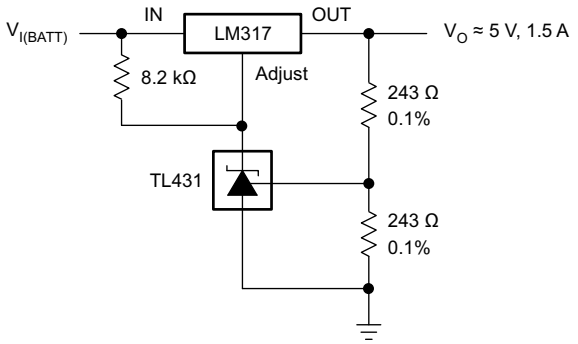
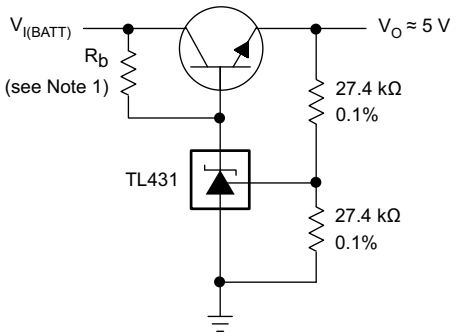


Figure 34. Precision 5-V, 1.5-A Regulator



(1) R_b must provide cathode current ≥1 mA to the TL431-Q1.

Figure 35. Efficient 5-V Precision Regulator

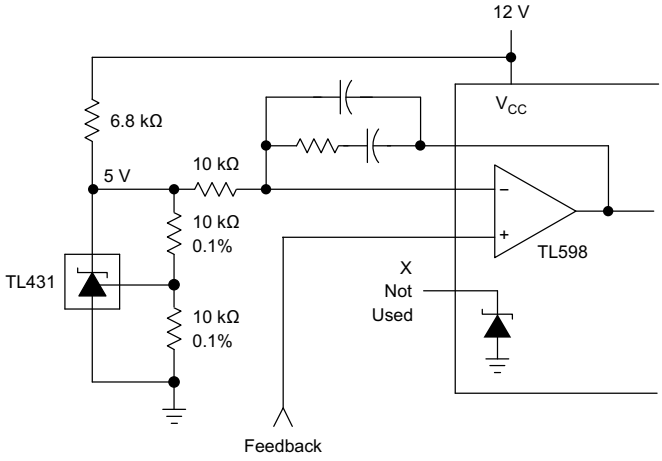
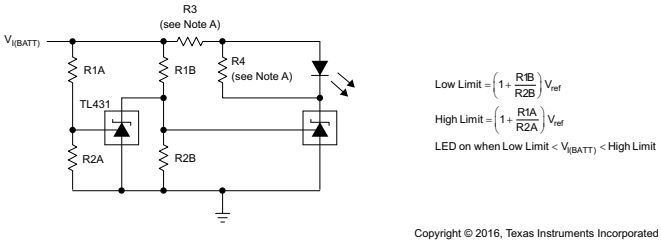


Figure 36. PWM Converter with Reference



A. R3 and R4 are selected to provide the desired LED intensity and cathode current ≥1 mA to the TL431-Q1 at the available $V_{I(BATT)}$.

Figure 37. Voltage Monitor

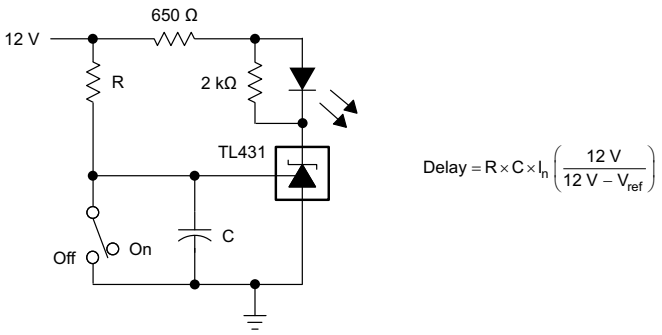


Figure 38. Delay Timer

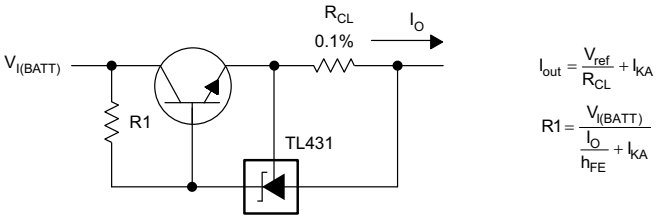


Figure 39. Precision Current Limiter

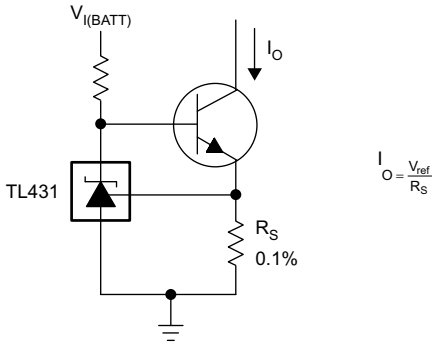


Figure 40. Precision Constant-Current Sink

10 Power Supply Recommendations

When using the TL43x-Q1 as a linear regulator to supply a load, designers typically use a bypass capacitor on the output or cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 12 and Figure 13.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the REF pin, as not to exceed its absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

11 Layout

11.1 Layout Guidelines

Bypass capacitors must be placed as close to the device as possible. Current-carrying traces must have widths appropriate for the amount of current they are carrying; in the case of the TL43x-Q1, these currents are low.

11.2 Layout Example

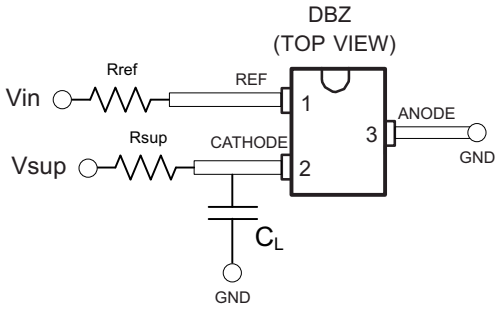


Figure 41. DBZ Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『Automotive LED Lighting With Adjustable Shunt References』(英語)*
- *『Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet』(英語)*
- *『Setting the Shunt Voltage on an Adjustable Shunt Regulator』(英語)*

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TL431-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TL432-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TL431LI-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TL432LI-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TACQ	Samples
TL431AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TAQU	Samples
TL431BQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T3FU	Samples
TL432AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TOIQ	Samples
TL432BQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TOHQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL431-Q1, TL432-Q1 :

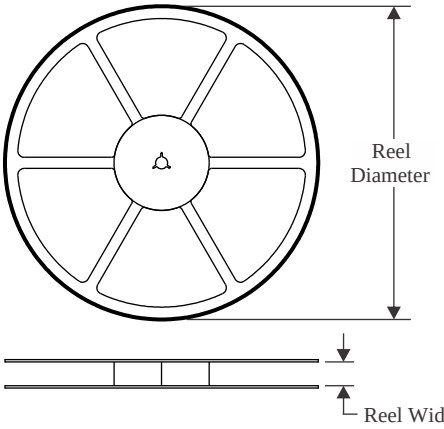
- Catalog : TL431, TL432

NOTE: Qualified Version Definitions:

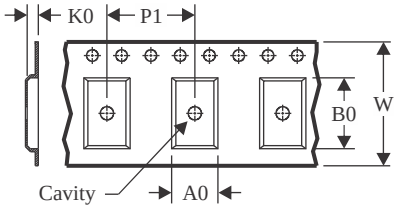
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

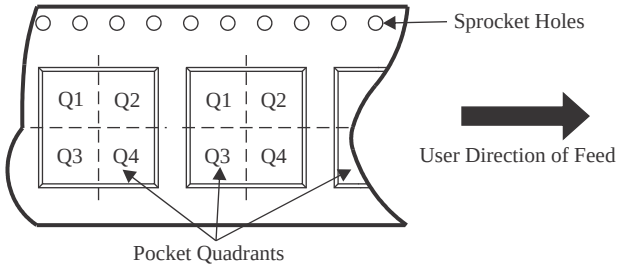


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

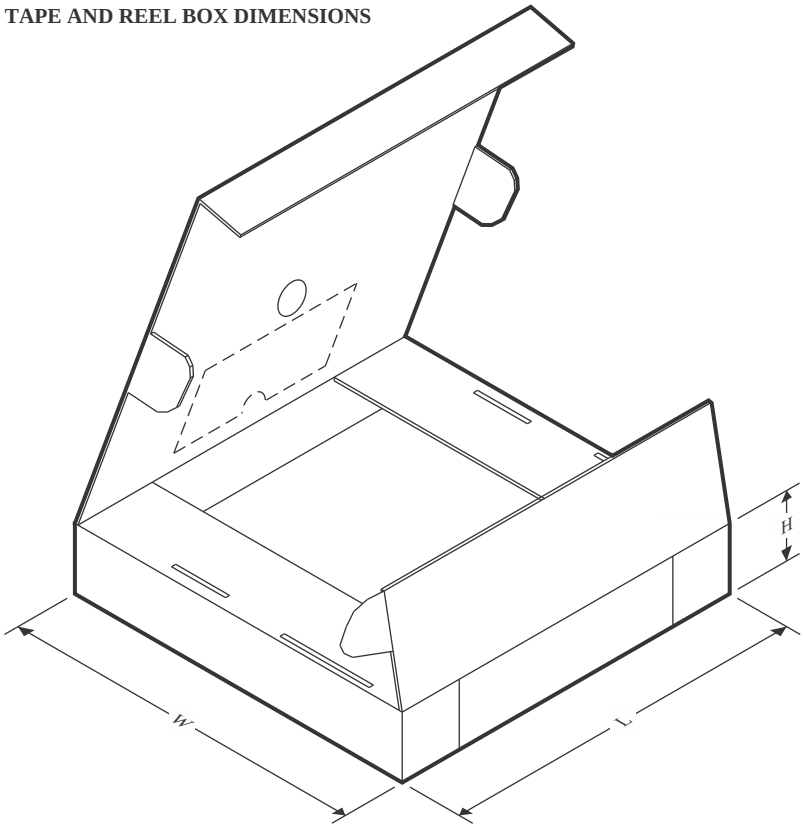
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL431AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL431AQDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL431AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TL431BQDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL432AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL432AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
TL432BQDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

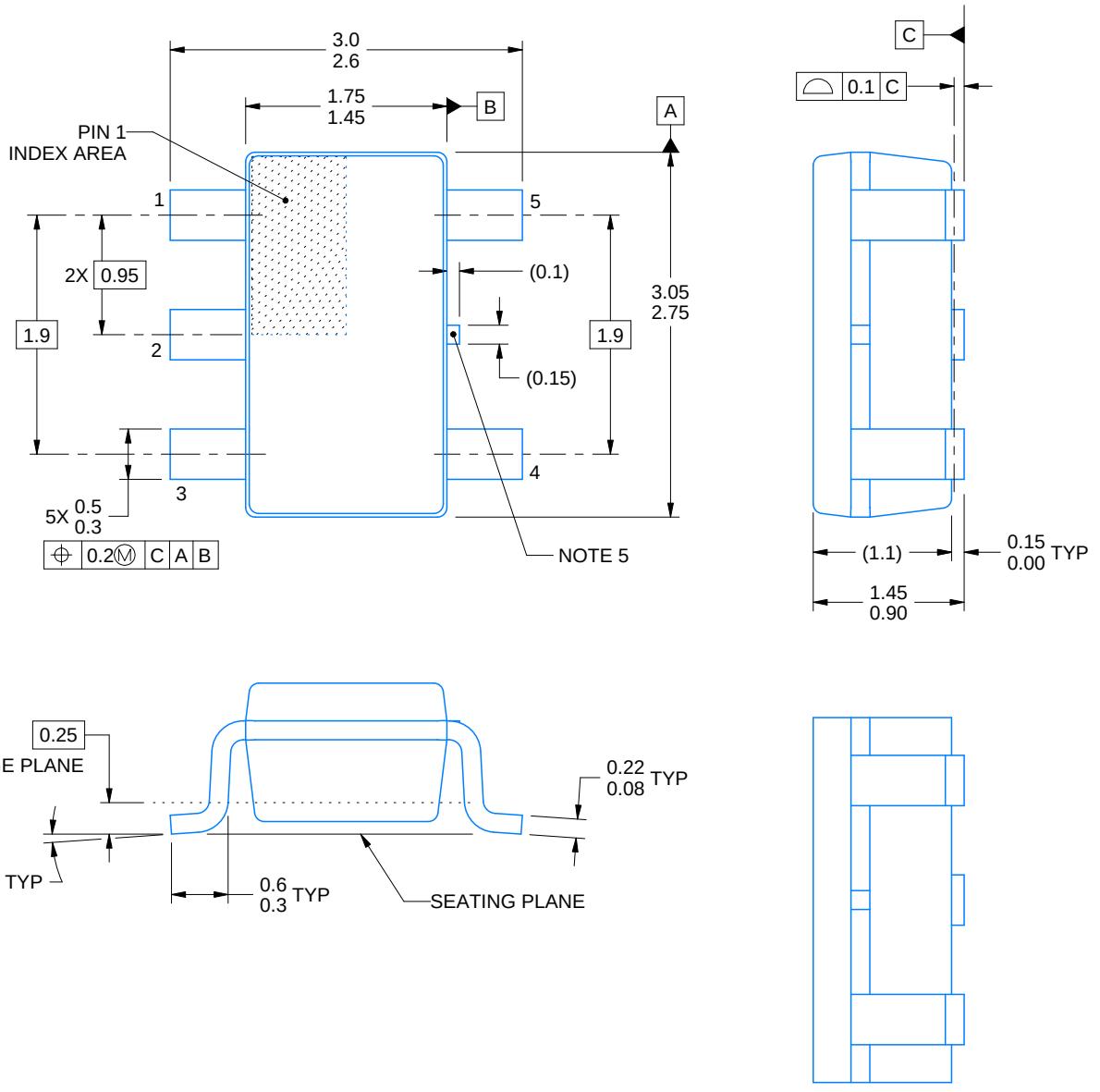
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL431AQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TL431AQDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL431AQDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TL431BQDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL432AQDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL432AQDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TL432BQDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

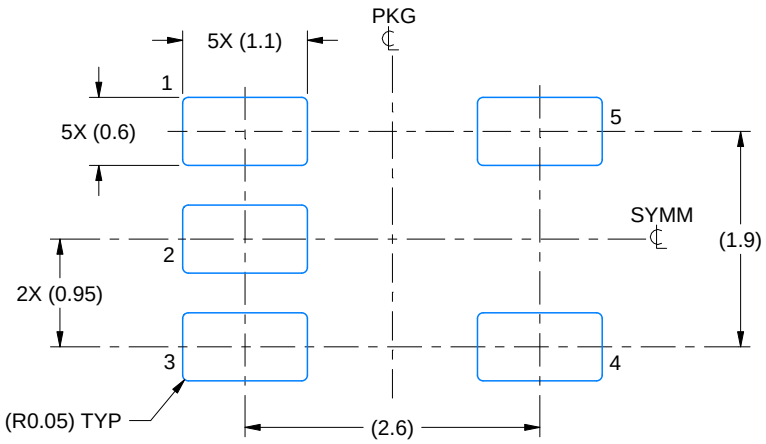


ALTERNATIVE PACKAGE SINGULATION VIEW

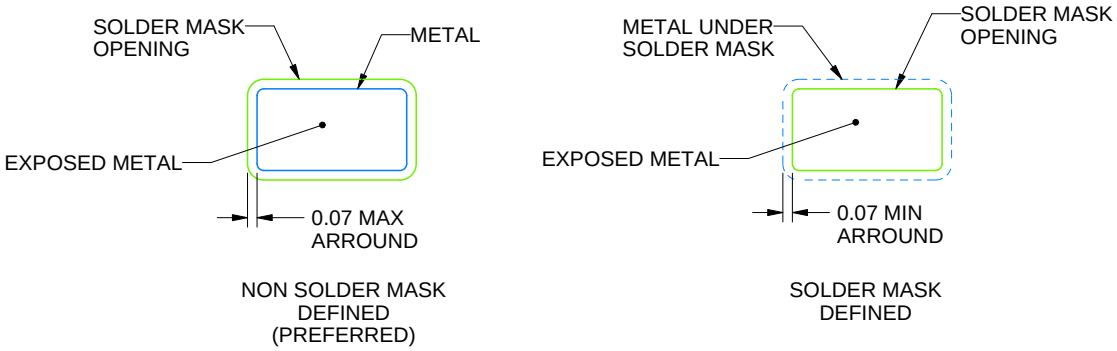
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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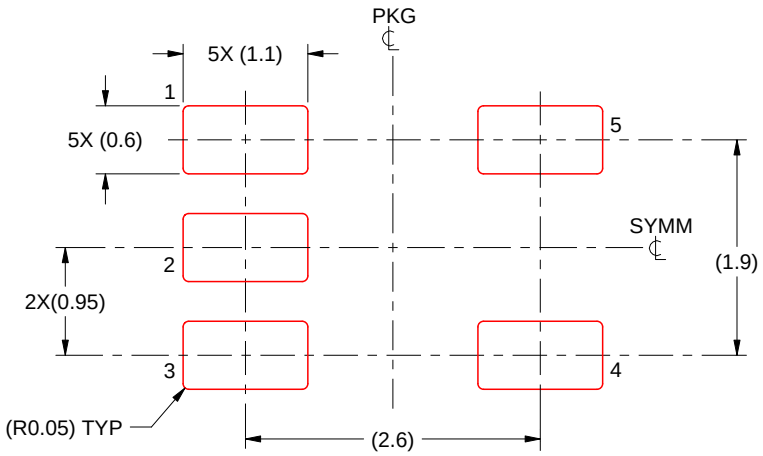
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

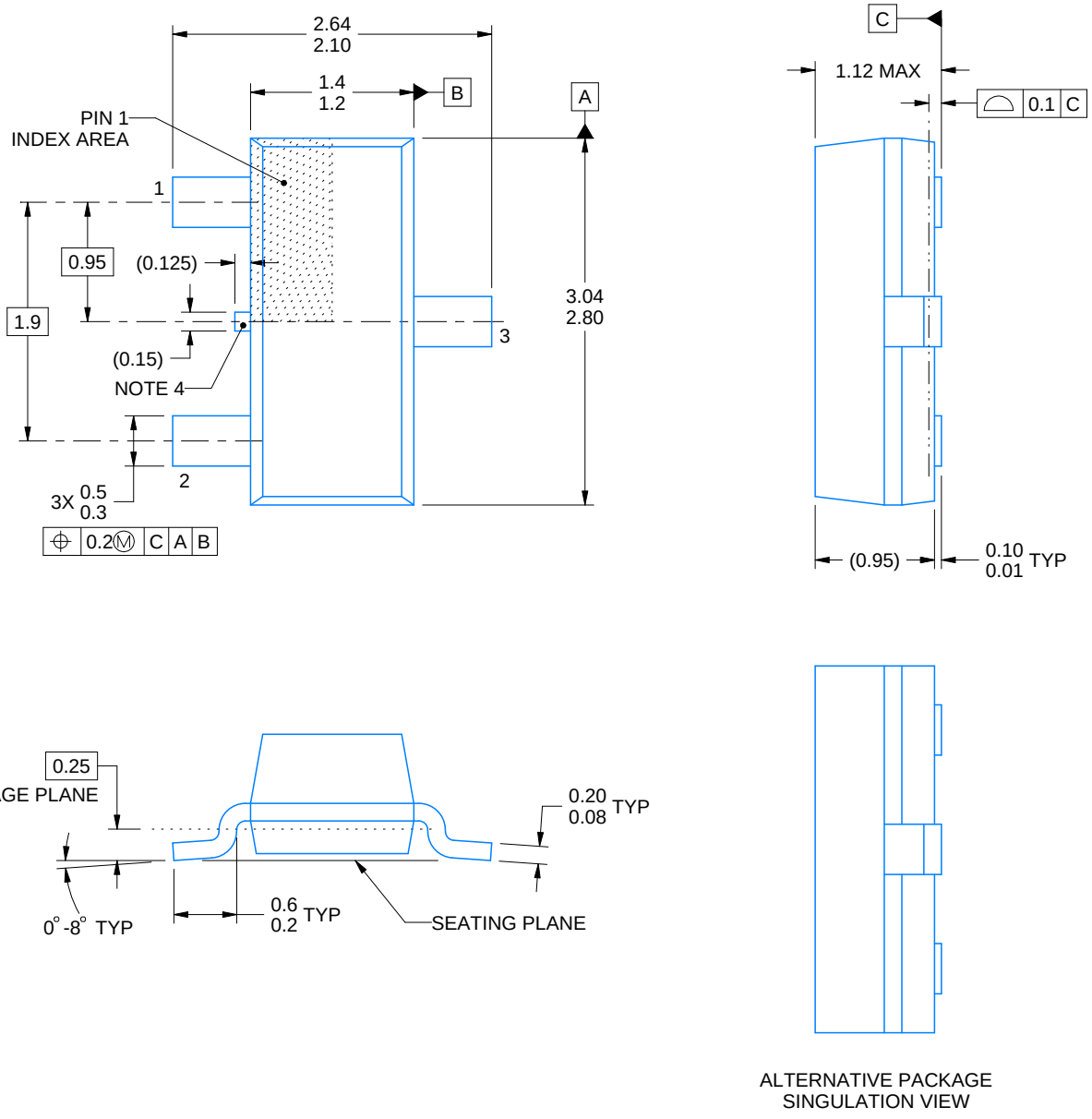
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

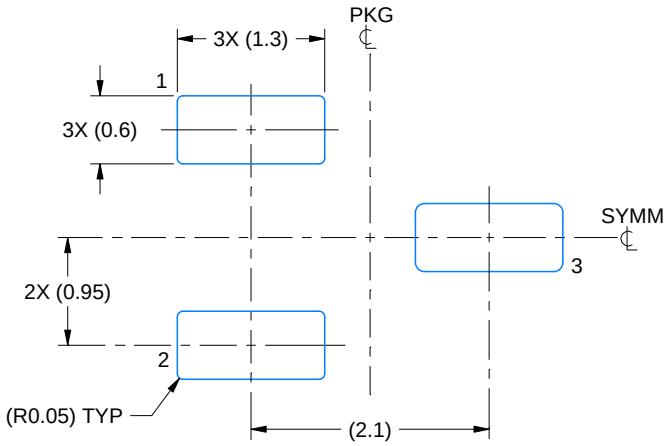
SMALL OUTLINE TRANSISTOR



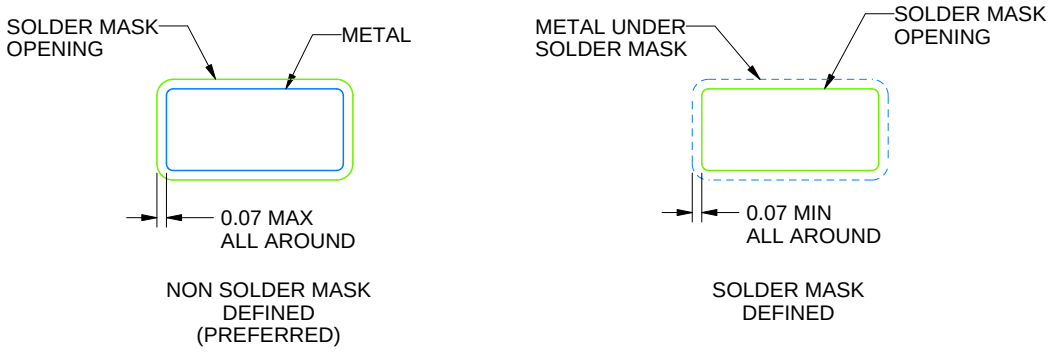
4214838/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

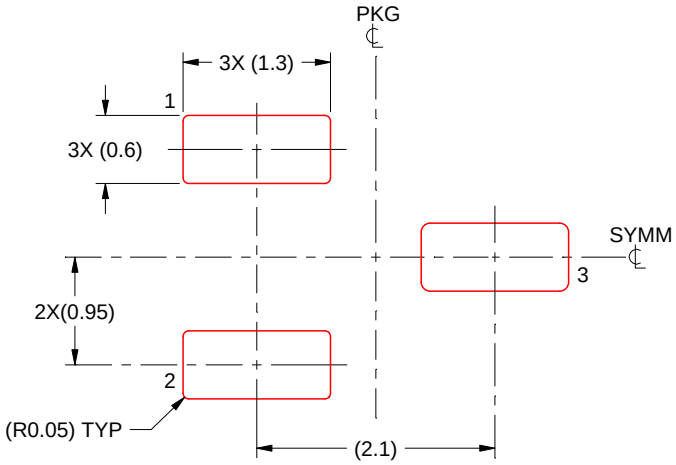


SOLDER MASK DETAILS

4214838/E 06/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/E 06/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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