

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS084F – APRIL 1994 – REVISED JANUARY 2002

- Complete PWM Power Control
- 3.6-V to 40-V Operation
- Internal Undervoltage-Lockout Circuit
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 20 kHz to 500 kHz
- Variable Dead Time Provides Control Over Total Range
- $\pm 3\%$  Tolerance on Reference Voltage (TL5001A)
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

## description

The TL5001 and TL5001A incorporate on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001/A contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor. The TL5001A has a typical reference voltage tolerance of  $\pm 3\%$  compared to  $\pm 5\%$  for the TL5001.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low  $V_{CC}$  conditions, the UVLO circuit turns the output off until  $V_{CC}$  recovers to its normal operating range.

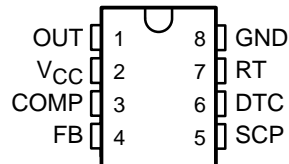
The TL5001C and TL5001AC are characterized for operation from  $-20^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The TL5001I and TL5001AI are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The TL5001Q and TL5001AQ are characterized for operation from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The TL5001M and TL5001AM are characterized for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### AVAILABLE OPTIONS

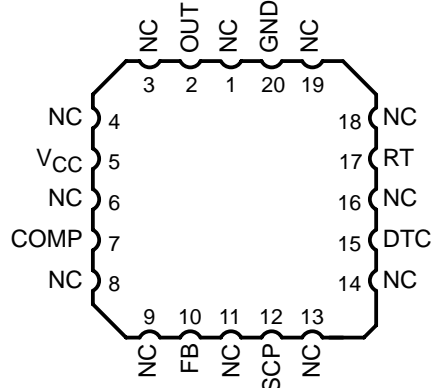
T <sub>A</sub>	PACKAGED DEVICES			
	SMALL OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)
-20°C to 85°C	TL5001CD	TL5001CP	—	—
	TL5001ACD	TL5001ACP	—	—
-40°C to 85°C	TL5001ID	TL5001IP	—	—
	TL5001AID	TL5001AIP	—	—
-40°C to 125°C	TL5001QD	—	—	—
	TL5001AQD	—	—	—
-55°C to 125°C	—	—	TL5001MJG	TL5001MFK
	—	—	TL5001AMJG	TL5001AMFK

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR).

D, JG OR P PACKAGE  
(TOP VIEW)



FK PACKAGE  
(TOP VIEW)



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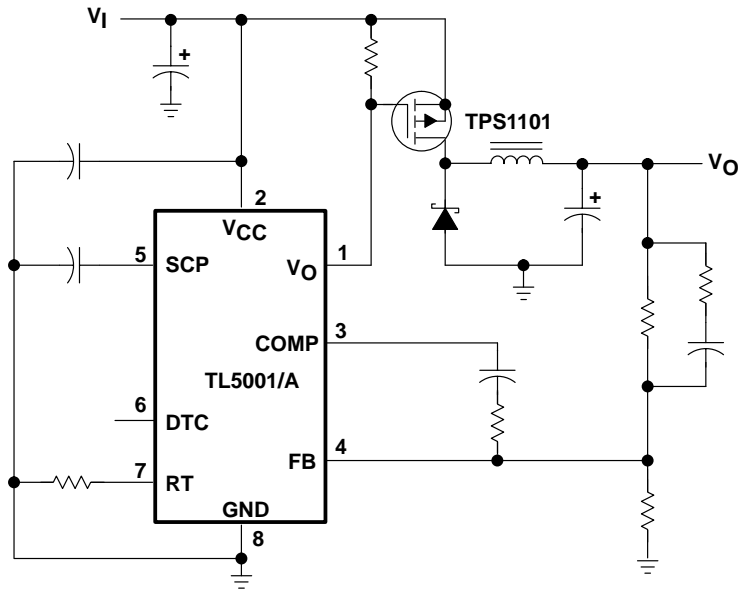
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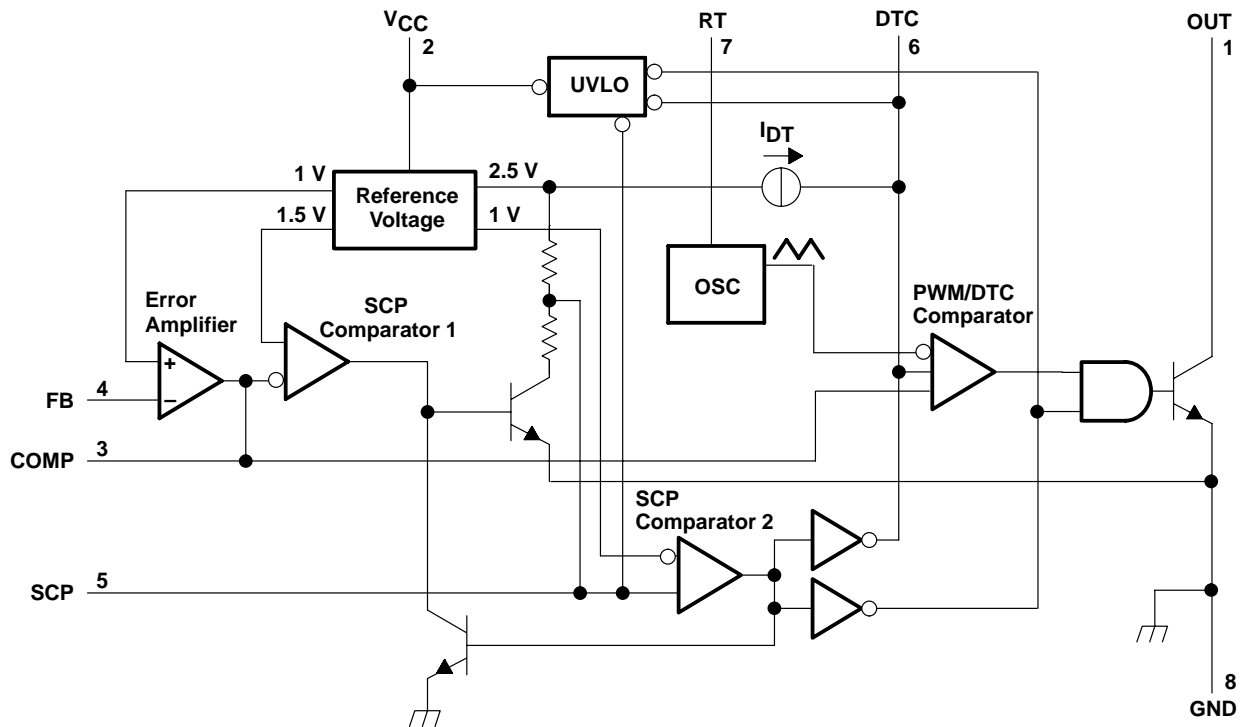
# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## schematic for typical application



## functional block diagram



## detailed description

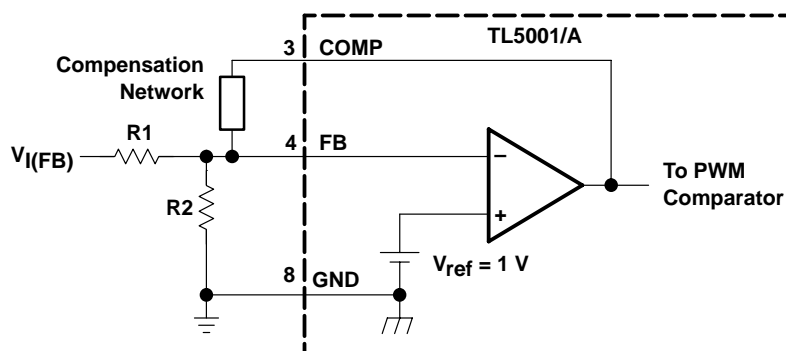
### voltage reference

A 2.5-V regulator operating from  $V_{CC}$  is used to power the internal circuitry of the TL5001 and TL5001A and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input which typically is within 2% of nominal over the operating temperature range.

### error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2) (1 \text{ V})$$



**Figure 1. Error-Amplifier Gain Setting**

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45  $\mu$ A, the total dc load resistance should be 100 k $\Omega$  or more.

### oscillator/PWM

The oscillator frequency ( $f_{osc}$ ) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 k $\Omega$  to 250 k $\Omega$ . The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

### dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current ( $I_{DT}$ ) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage ( $V_{DT}$ ), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when  $V_{DT}$  is 0.7 V or less and 100% when  $V_{DT}$  is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250  $\Omega$ ), choosing  $R_{DT}$  for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 ( $V_{osc,max}$  and  $V_{osc,min}$  are the maximum and minimum oscillator levels):

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### dead-time control (DTC) (continued)

$$R_{DT} = (R_t + 1250) [D(V_{oscmax} - V_{oscmin}) + V_{oscmin}]$$

Where

$R_{DT}$  and  $R_t$  are in ohms,  $D$  in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor ( $C_{DT}$ ) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT} R_{DT} \left( 1 - e^{-t/R_{DT} C_{DT}} \right)$$

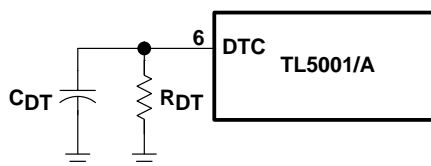


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant,  $R_{DT}C_{DT}$ , should be  $t_0/3$  to  $t_0/5$ . The TL5001/A remains off until  $V_{DT} \approx 0.7$  V, the minimum ramp value.  $C_{DT}$  is discharged every time UVLO or SCP becomes active.

### undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

### short-circuit protection (SCP)

The TL5001/A includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001/A output transistor.

short-circuit protection (SCP) (continued)

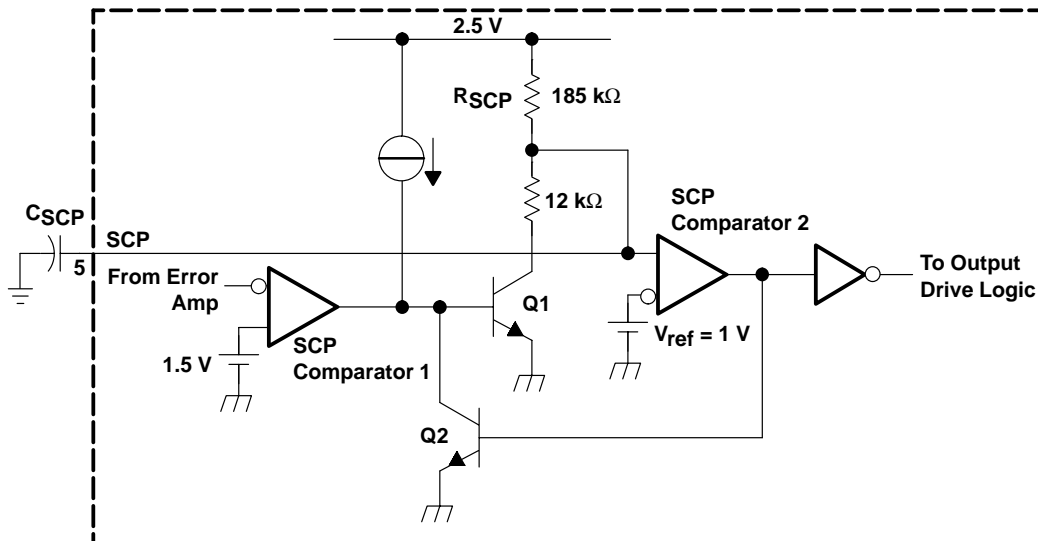


Figure 3. SCP Circuit

The timer operates by charging an external capacitor ( $C_{SCP}$ ), connected between the SCP terminal and ground, towards 2.5 V through a 185-k $\Omega$  resistor ( $R_{SCP}$ ). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 - 0.185)\left(1 - e^{-t/\tau}\right) + 0.185$$

Where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period,  $t_{SCP}$ , occurs when  $V_{SCP} = 1$  V. Solving for  $C_{SCP}$  yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

Where

t is in seconds, C in  $\mu$ F.

$t_{SCP}$  must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001/A is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	41 V
Amplifier input voltage, $V_{I(FB)}$	20 V
Output voltage, $V_{O, OUT}$	51 V
Output current, $I_{O, OUT}$	21 mA
Output peak current, $I_{O(peak), OUT}$	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating ambient temperature range, $T_A$ :	
TL5001C, TL5001AC	–20°C to 85°C
TL5001I, TL5001AI	–40°C to 85°C
TL5001Q, TL5001AQ	–40°C to 125°C
TL5001M, TL5001AM	–55°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

## recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{CC}$	3.6	40	V
Amplifier input voltage, $V_{I(FB)}$	0	1.5	V
Output voltage, $V_{O, OUT}$		50	V
Output current, $I_{O, OUT}$		20	mA
COMP source current		45	$\mu\text{A}$
COMP dc load resistance	100		$\text{k}\Omega$
Oscillator timing resistor, $R_t$	15	250	$\text{k}\Omega$
Oscillator frequency, $f_{osc}$	20	500	kHz
Operating ambient temperature, $T_A$	TL5001C, TL5001AC	–20	85
	TL5001I, TL5001AI	–40	85
	TL5001Q, TL5001AQ	–40	125
	TL5001M, TL5001AM	–55	125

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 100\text{ kHz}$  (unless otherwise noted)

## reference

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	COMP connected to FB	0.95	1	1.05	0.97	1	1.03	V
Input regulation	$V_{CC} = 3.6\text{ V to }40\text{ V}$		2	12.5		2	12.5	mV
Output voltage change with temperature	$T_A = -20^\circ\text{C to }25^\circ\text{C}$ (C suffix)	-10	-1	10	-10	-1	10	mV/V
	$T_A = -40^\circ\text{C to }25^\circ\text{C}$ (I suffix)	-10	-1	10	-10	-1	10	
	$T_A = 25^\circ\text{C to }85^\circ\text{C}$	-10	-2	10	-10	-2	10	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

## undervoltage lockout

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Upper threshold voltage	$T_A = 25^\circ\text{C}$		3			3		V
Lower threshold voltage	$T_A = 25^\circ\text{C}$		2.8			2.8		V
Hysteresis	$T_A = 25^\circ\text{C}$	100	200		100	200		mV
Reset threshold voltage	$T_A = 25^\circ\text{C}$	2.1	2.55		2.1	2.55		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

## short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
SCP threshold voltage	$T_A = 25^\circ\text{C}$	0.95	1.00	1.05	0.97	1.00	1.03	V
SCP voltage, latched	No pullup	140	185	230	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120		60	120	mV
Input source current	$T_A = 25^\circ\text{C}$	-10	-15	-20	-10	-15	-20	$\mu\text{A}$
SCP comparator 1 threshold voltage			1.5			1.5		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

## oscillator

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	$R_t = 100\text{ k}\Omega$		100			100		kHz
Standard deviation of frequency			15			15		kHz
Frequency change with voltage	$V_{CC} = 3.6\text{ V to }40\text{ V}$		1			1		kHz
Frequency change with temperature	$T_A = -40^\circ\text{C to }25^\circ\text{C}$	-4	-0.4	4	-4	-0.4	4	kHz
	$T_A = -20^\circ\text{C to }25^\circ\text{C}$	-4	-0.4	4	-4	-0.4	4	kHz
	$T_A = 25^\circ\text{C to }85^\circ\text{C}$	-4	-0.2	4	-4	-0.2	4	kHz
Voltage at RT			1			1		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .



# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 100\text{ kHz}$  (unless otherwise noted) (continued)

## dead-time control

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Output (source) current	TL5001C	$V_{(DT)} = 1.5\text{ V}$	$0.9 \times I_{RT}^{\ddagger}$		$1.1 \times I_{RT}$	$0.9 \times I_{RT}^{\ddagger}$		$1.1 \times I_{RT}$	$\mu\text{A}$
	TL5001I	$V_{(DT)} = 1.5\text{ V}$	$0.9 \times I_{RT}^{\ddagger}$		$1.2 \times I_{RT}$	$0.9 \times I_{RT}^{\ddagger}$		$1.2 \times I_{RT}$	
Input threshold voltage		Duty cycle = 0%	0.5	0.7		0.5	0.7		V
		Duty cycle = 100%		1.3	1.5		1.3	1.5	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Output source current at RT

## error amplifier

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Input voltage		$V_{CC} = 3.6\text{ V to }40\text{ V}$	0		1.5	0		1.5	V
Input bias current				-160	-500		-160	-500	nA
Output voltage swing	Positive		1.5	2.3		1.5	2.3		V
	Negative			0.3	0.4		0.3	0.4	V
Open-loop voltage amplification				80			80		dB
Unity-gain bandwidth				1.5			1.5		MHz
Output (sink) current		$V_{I(FB)} = 1.2\text{ V}$ , COMP = 1 V	100	600		100	600		$\mu\text{A}$
Output (source) current		$V_{I(FB)} = 0.8\text{ V}$ , COMP = 1 V	-45	-70		-45	-70		$\mu\text{A}$

† All typical values are at  $T_A = 25^\circ\text{C}$ .

## output

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Output saturation voltage		$I_O = 10\text{ mA}$		1.5	2		1.5	2	V
Off-state current		$V_O = 50\text{ V}$ , $V_{CC} = 0$			10			10	$\mu\text{A}$
		$V_O = 50\text{ V}$			10			10	
Short-circuit output current		$V_O = 6\text{ V}$		40			40		mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .

## total device

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			TL5001AC, TL5001AI			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Standby supply current	Off state			1	1.5		1	1.5	mA
Average supply current		$R_t = 100\text{ k}\Omega$		1.4	2.1		1.4	2.1	mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .





# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 100\text{ kHz}$  (unless otherwise noted)

## reference

PARAMETER	TEST CONDITIONS		TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	$T_A = 25^\circ\text{C}$	COMP connected to FB	0.95	1.00	1.05	0.97	1.00	1.03	V
	$T_A = \text{MIN to MAX}$		0.93	0.98	1.07	0.94	0.98	1.06	
Input regulation	$T_A = \text{MIN to MAX}$	$V_{CC} = 3.6\text{ V to }40\text{ V}$	2		12.5	2		12.5	mV
Output voltage change with temperature	$T_A = \text{MIN to MAX}$		*-6	2	*6	*-6	2	*6	%

† All typical values are at  $T_A = 25^\circ\text{C}$ .

\*Not production tested.

## undervoltage lockout

PARAMETER	TEST CONDITIONS	TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Upper threshold voltage	$T_A = \text{MIN}, 25^\circ\text{C}$	3.00			3.00			V
	$T_A = \text{MAX}$	2.55			2.55			
Lower threshold voltage	$T_A = \text{MIN}, 25^\circ\text{C}$	2.8			2.8			V
	$T_A = \text{MAX}$	2.0			2.0			
Hysteresis	$T_A = \text{MIN to MAX}$		100	200	100	200	mV	
Reset threshold voltage	$T_A = \text{MIN}, 25^\circ\text{C}$	2.10	2.55	2.10	2.55	V		
	$T_A = \text{MAX}$	0.35	0.63	0.35	0.63			

† All typical values are at  $T_A = 25^\circ\text{C}$ .

## short-circuit protection

PARAMETER	TEST CONDITIONS		TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
SCP threshold voltage	$T_A = \text{MIN}, 25^\circ\text{C}$		0.95	1.00	1.05	0.97	1.00	1.03	V
	$T_A = \text{MAX}$		0.93	0.98	1.07	0.94	0.98	1.06	
SCP voltage, latched	$T_A = \text{MIN to MAX}$	No pullup	140	185	230	140	185	230	mV
SCP voltage, UVLO standby	$T_A = \text{MIN to MAX}$	No pullup	60		120	60		120	mV
Equivalent timing resistance	$T_A = \text{MIN to MAX}$		185			185			k $\Omega$
SCP comparator 1 threshold voltage	$T_A = \text{MIN to MAX}$		1.5			1.5			V

† All typical values are at  $T_A = 25^\circ\text{C}$ .



# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 100\text{ kHz}$  (unless otherwise noted) (continued)

## oscillator

PARAMETER	TEST CONDITIONS		TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Frequency	$T_A = \text{MIN to MAX}$	$R_t = 100\text{ k}\Omega$	100			100			kHz
Standard deviation of frequency	$T_A = \text{MIN to MAX}$		2			2			kHz
Frequency change with voltage	$T_A = \text{MIN to MAX}$	$V_{CC} = 3.6\text{ V to }40\text{ V}$	1			1			kHz
Frequency change with temperature	$T_A = \text{MIN to MAX}$	Q suffix	*-6	3	*6	*-6	3	*6	kHz
		M suffix	*-9	5	*9	*-9	5	*9	
Voltage at RT	$T_A = \text{MIN to MAX}$		1			1			V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

\*Not production tested.

## dead-time control

PARAMETER	TEST CONDITIONS		TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Output (source) current	$T_A = \text{MIN to MAX}$	$V_{(DT)} = 1.5\text{ V}$	$0.9 \times I_{RT}^\ddagger$		$1.1 \times I_{RT}$	$0.9 \times I_{RT}^\ddagger$		$1.1 \times I_{RT}$	$\mu\text{A}$
Input threshold voltage	$T_A = 25^\circ\text{C}$	Duty cycle = 0%	0.5	0.7		0.5	0.7		V
		Duty cycle = 100%		1.3	1.5		1.3	1.5	
	$T_A = \text{MIN to MAX}$	Duty cycle = 0%	0.4	0.7		0.4	0.7		
		Duty cycle = 100%		1.3	1.7		1.3	1.7	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Output source current at RT

## error amplifier

PARAMETER	TEST CONDITIONS		TL5001Q, TL5001M			TL5001AQ, TL5001AM			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
Input bias current	$T_A = \text{MIN to MAX}$		-160	-500		-160	-500		nA
Output voltage swing	Positive	$T_A = \text{MIN to MAX}$	1.5	2.3		1.5	2.3		V
			0.3	0.4		0.3	0.4		V
Open-loop voltage amplification	$T_A = \text{MIN to MAX}$		80			80			dB
			80			80			
Unity-gain bandwidth	$T_A = \text{MIN to MAX}$		1.5			1.5			MHz
Output (sink) current	$T_A = \text{MIN to MAX}$	$V_{I(\text{FB})} = 1.2\text{ V}, \text{ COMP} = 1\text{ V}$	100	600		100	600		$\mu\text{A}$
Output (source) current	$T_A = \text{MIN}, 25^\circ\text{C}$	$V_{I(\text{FB})} = 0.8\text{ V}, \text{ COMP} = 1\text{ V}$	-45	-70		-45	-70		$\mu\text{A}$
	$T_A = \text{MAX}$		-30	-45		-30	-45		

† All typical values are at  $T_A = 25^\circ\text{C}$ .



# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 100\text{ kHz}$  (unless otherwise noted) (continued)

### output

PARAMETER	TEST CONDITIONS		TL5001Q, TL5001M		TL5001AQ, TL5001AM		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
Output saturation voltage	$T_A = \text{MIN to MAX}$	$I_O = 10\text{ mA}$	1.5		2	1.5	2	V
Off-state current	$T_A = \text{MIN to MAX}$	$V_O = 50\text{ V}, V_{CC} = 0$			10		10	$\mu\text{A}$
		$V_O = 50\text{ V}$			10		10	
Short-circuit output current	$T_A = \text{MIN to MAX}$	$V_O = 6\text{ V}$	40			40		mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .

### total device

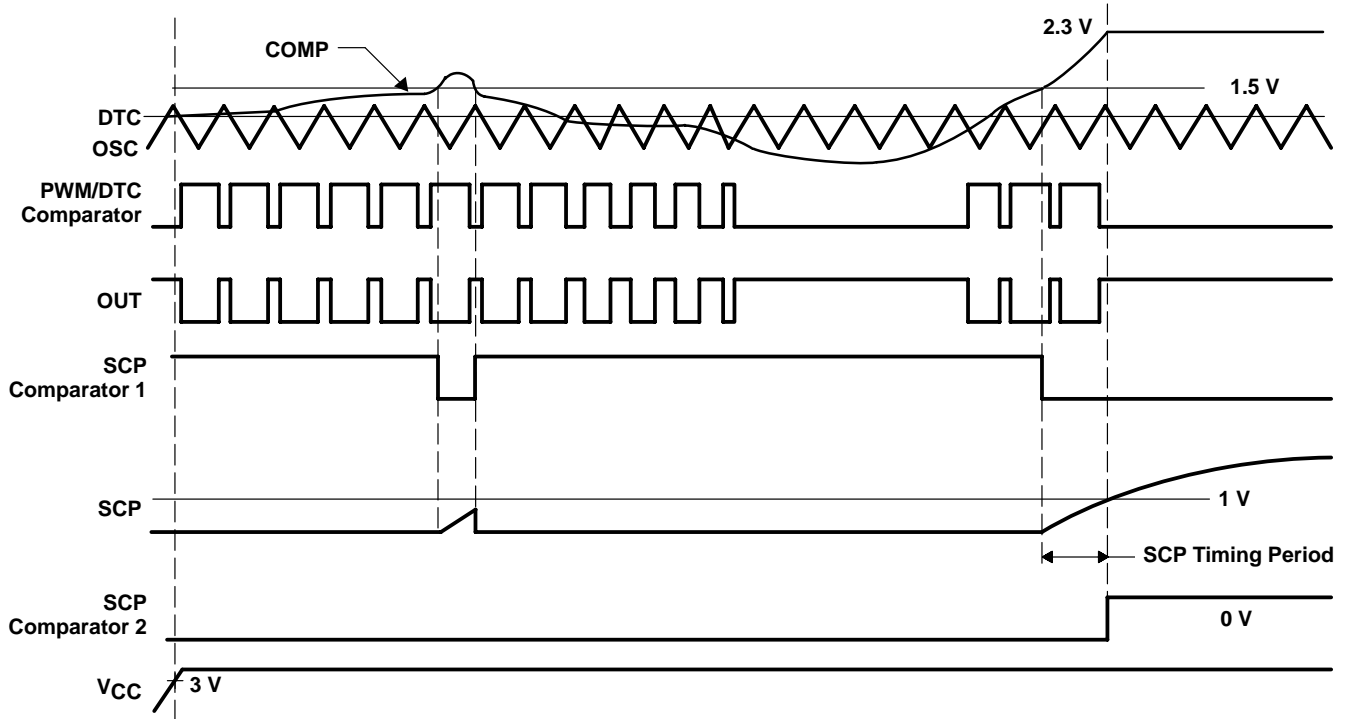
PARAMETER		TEST CONDITIONS		TL5001Q, TL5001M		TL5001AQ, TL5001AM		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
Standby supply current	Off state	$T_A = \text{MIN to MAX}$		1		1.5	1	1.5	mA
Average supply current		$T_A = \text{MIN to MAX}$	$R_t = 100\text{ k}\Omega$	1.4		2.1	1.4	2.1	mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## PARAMETER MEASUREMENT INFORMATION



NOTE A: The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

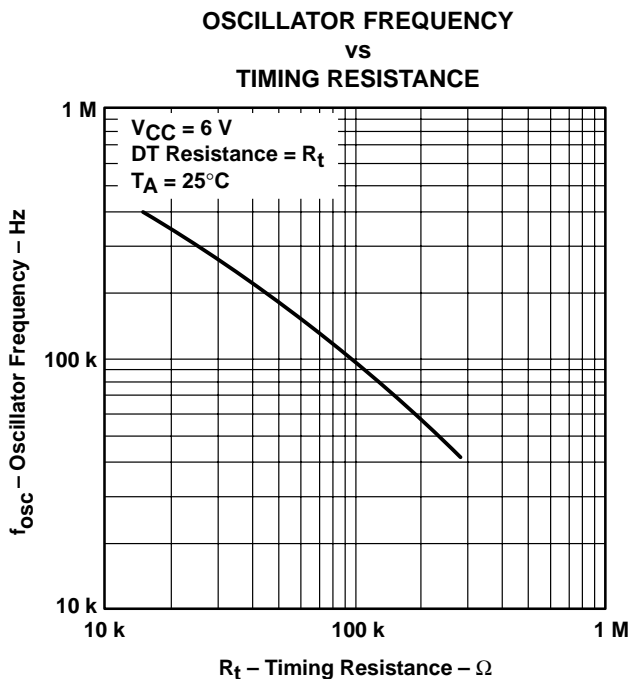


Figure 5

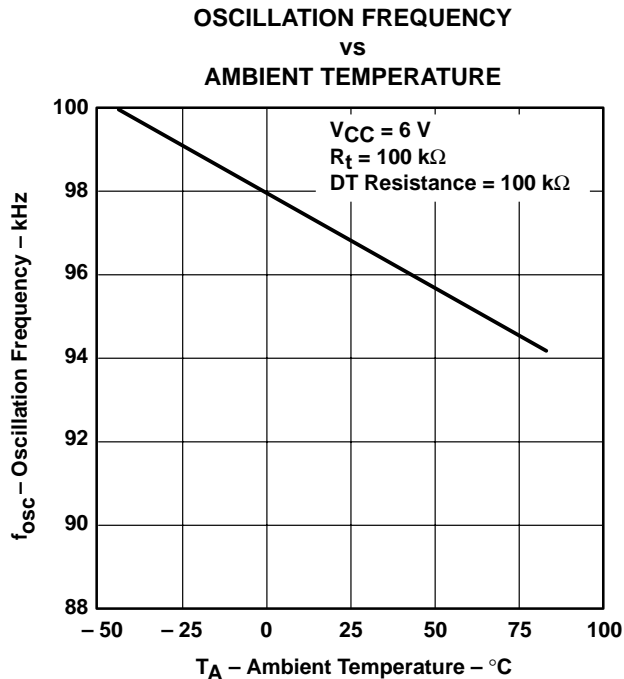


Figure 6

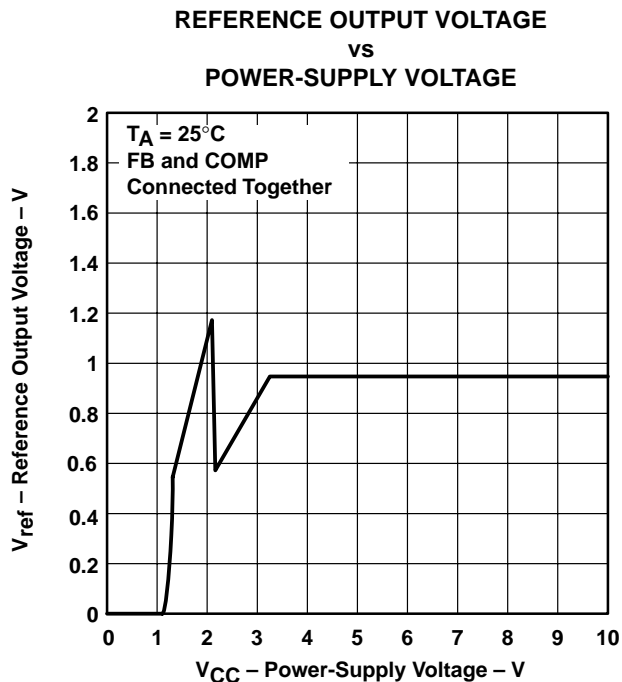


Figure 7

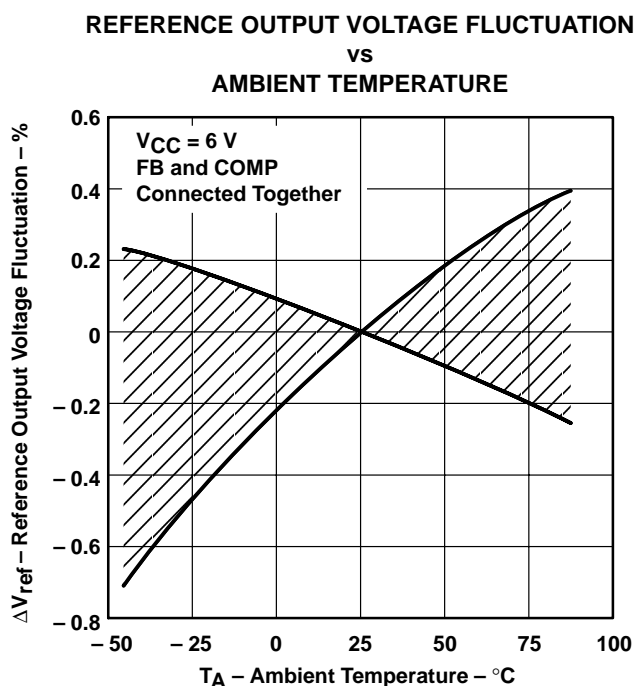
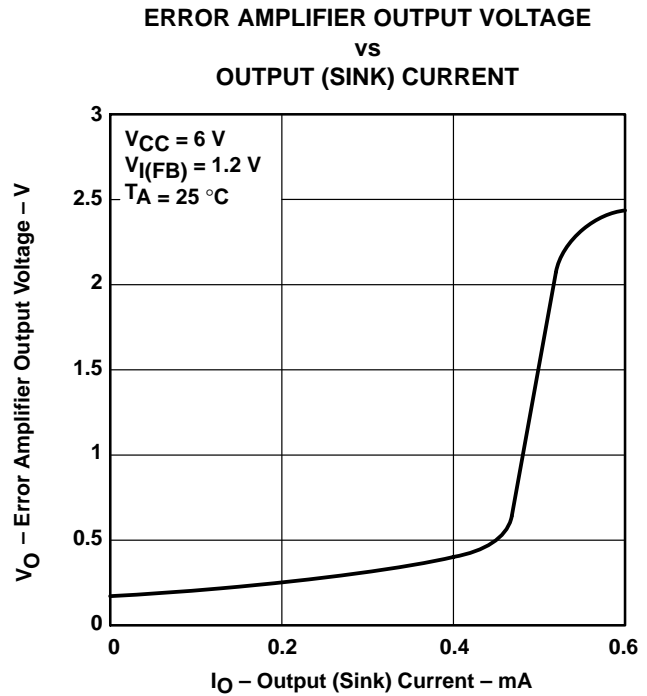
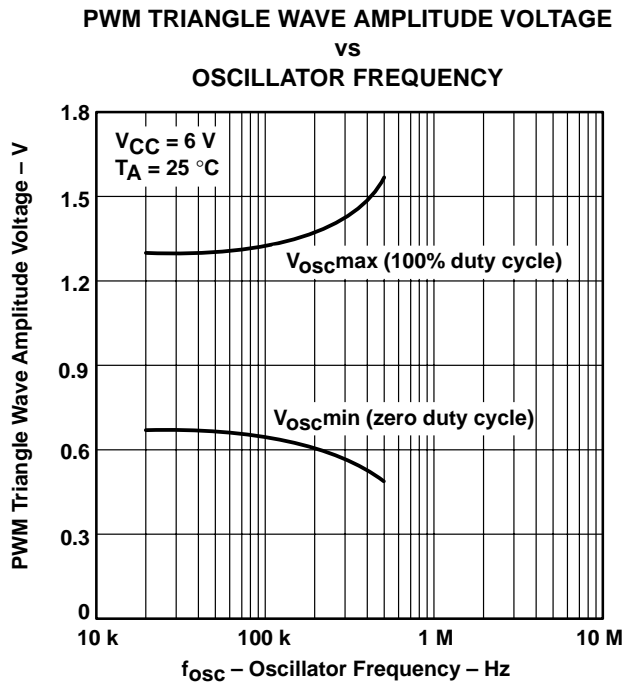
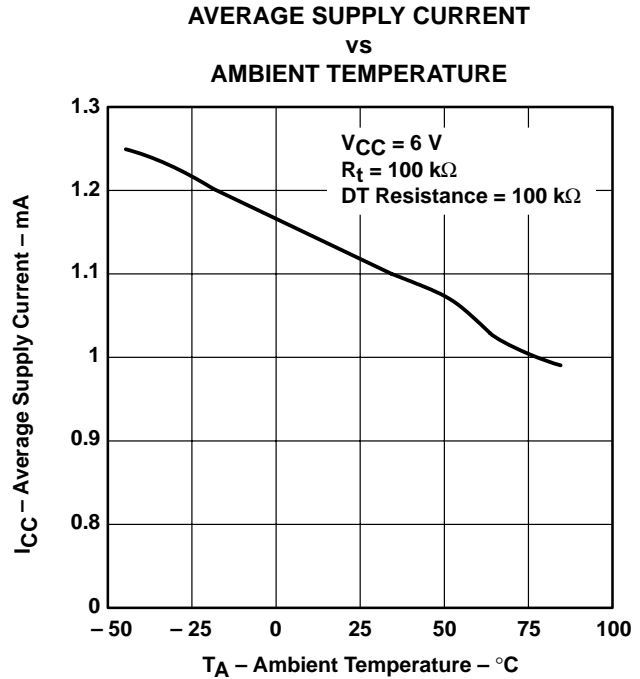
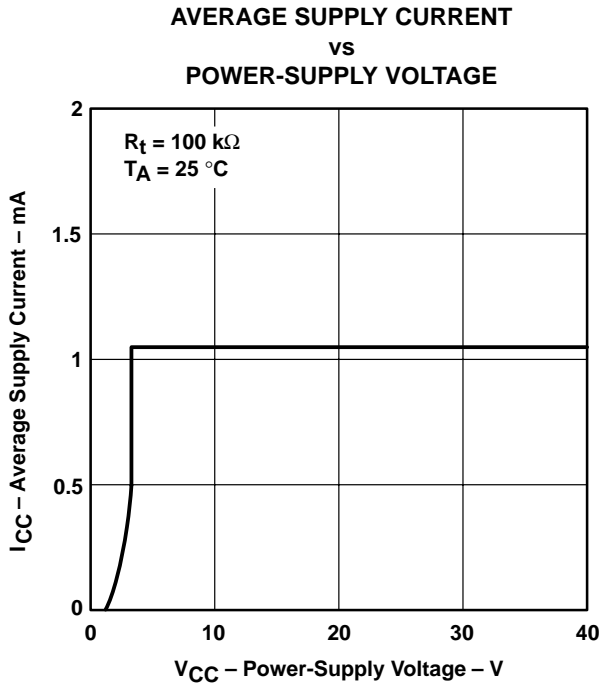


Figure 8

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

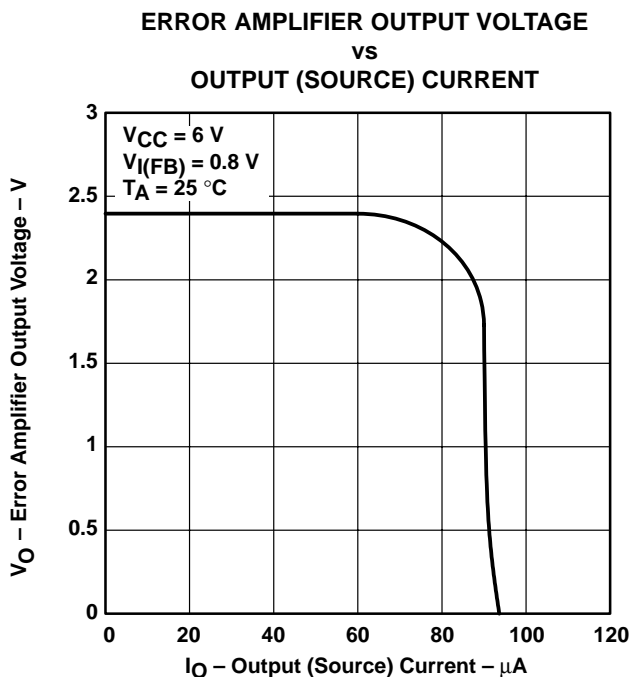


Figure 13

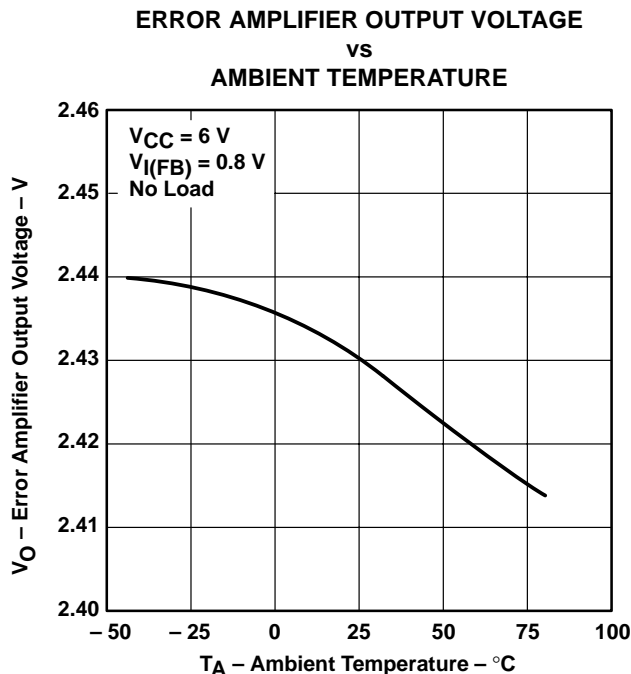


Figure 14

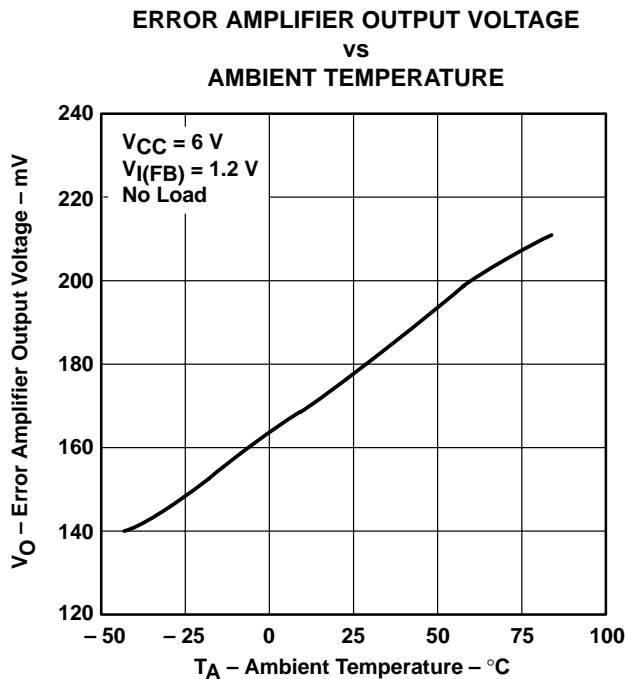


Figure 15

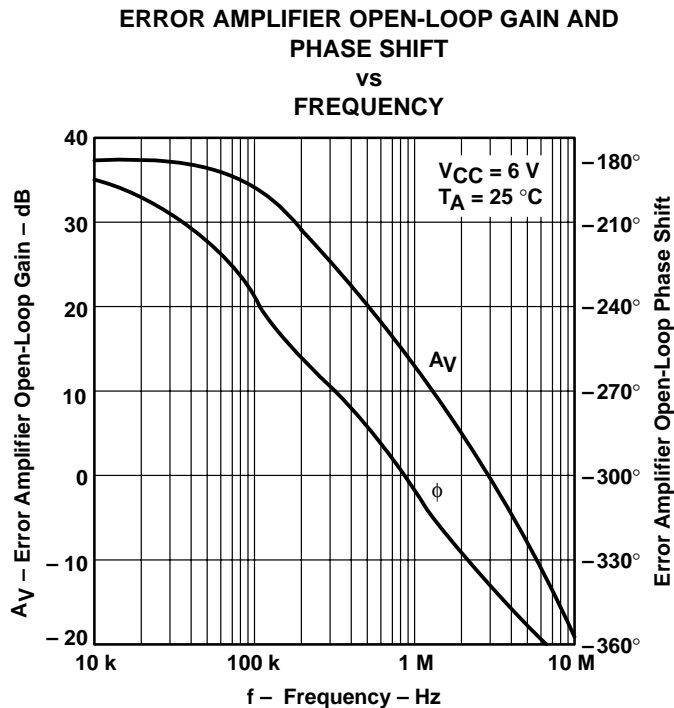


Figure 16

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## TYPICAL CHARACTERISTICS

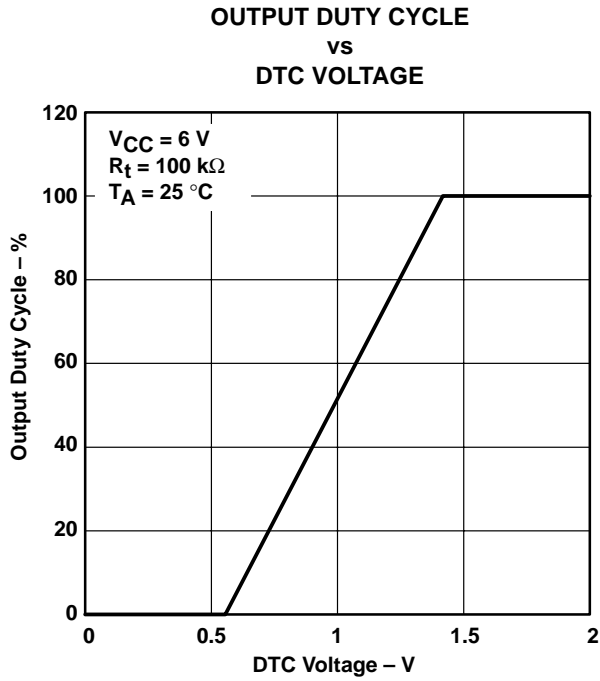


Figure 17

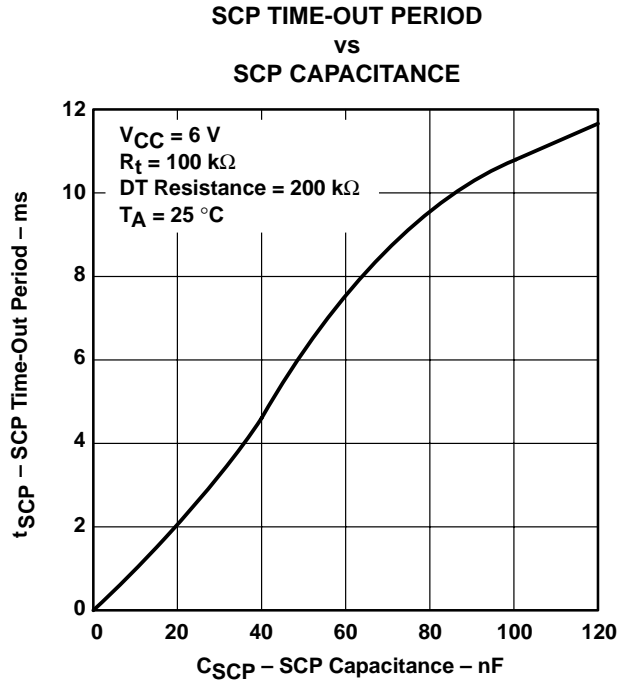


Figure 18

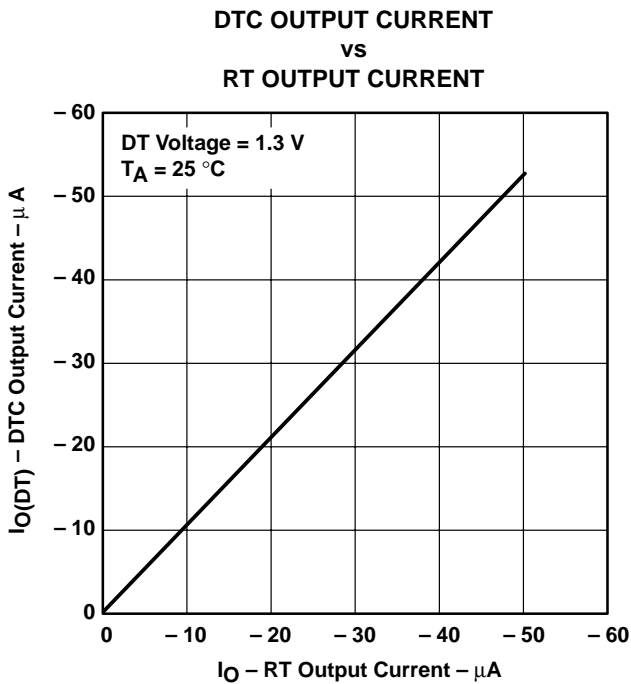


Figure 19

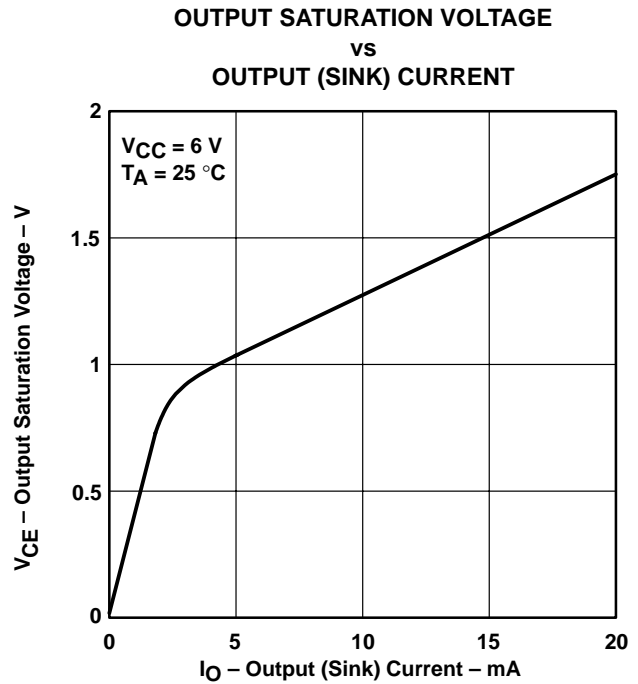
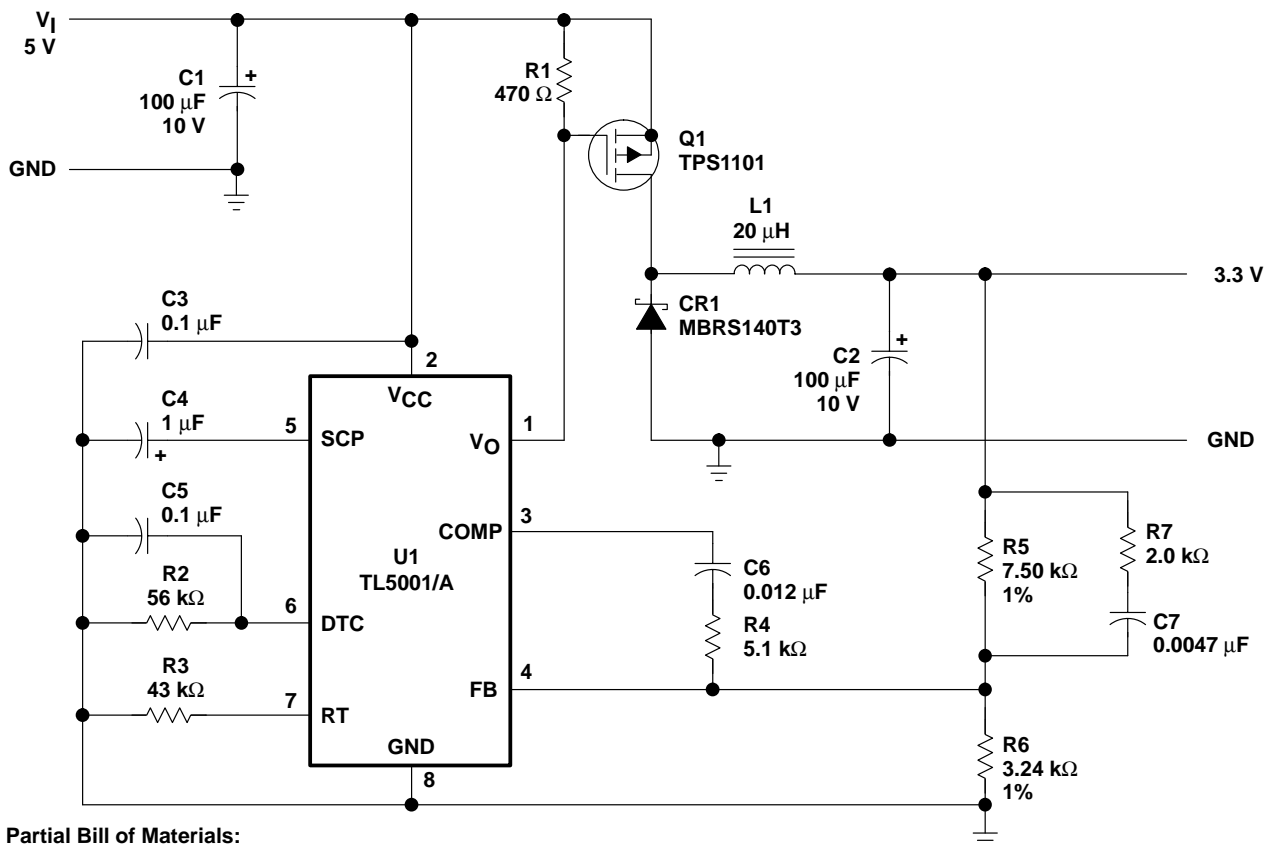


Figure 20





APPLICATION INFORMATION



Partial Bill of Materials:

U1	TL5001/A	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T50-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

- NOTES: A. Frequency = 200 kHz  
 B. Duty cycle = 90% max  
 C. Soft-start time constant (TC) = 5.6 ms  
 D. SCP TC = 70 msA

Figure 21. Step-Down Converter

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

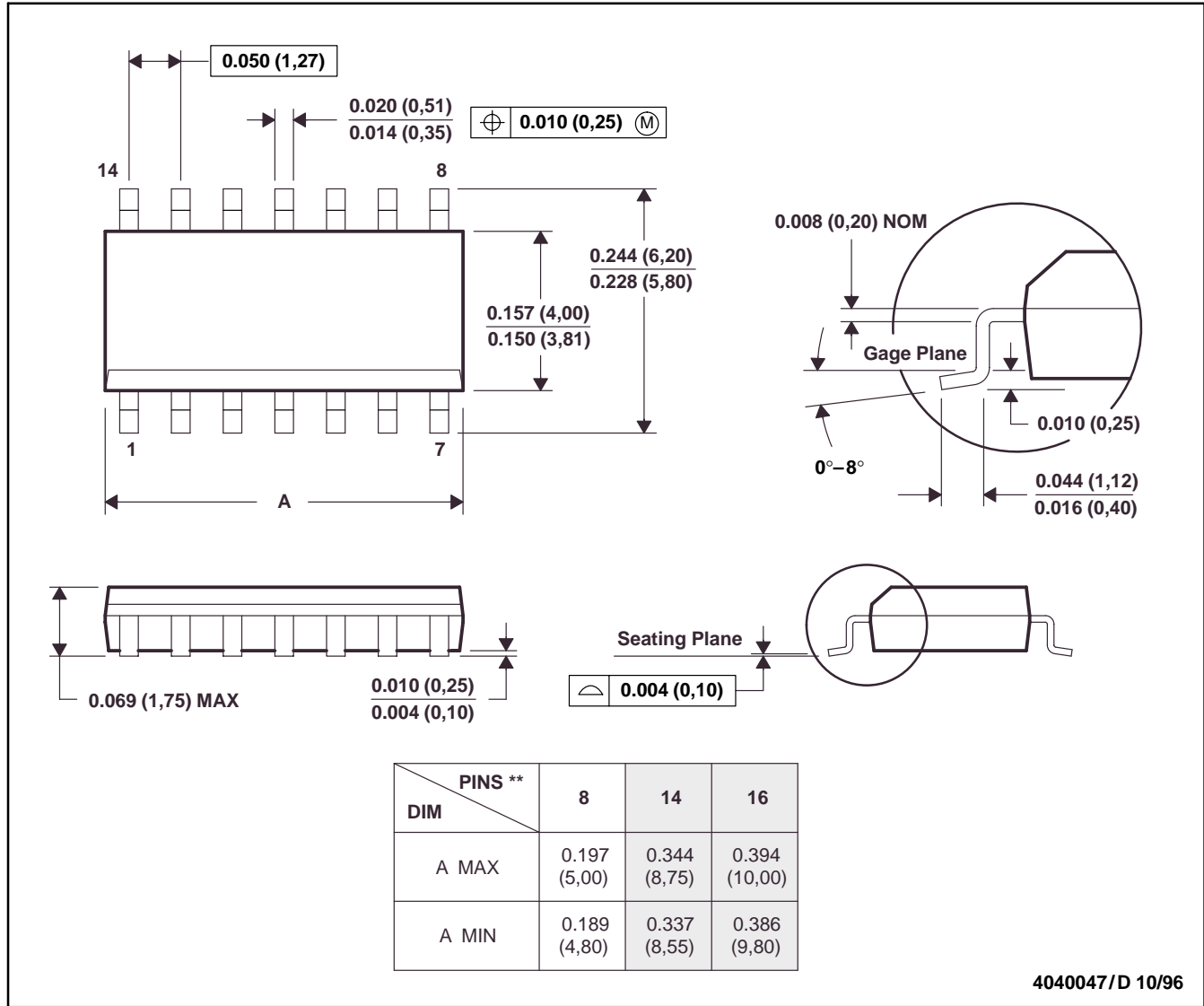
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## MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: B. All linear dimensions are in inches (millimeters).  
 C. This drawing is subject to change without notice.  
 D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 E. Falls within JEDEC MS-012

# TL5001, TL5001A PULSE-WIDTH-MODULATION CONTROL CIRCUITS

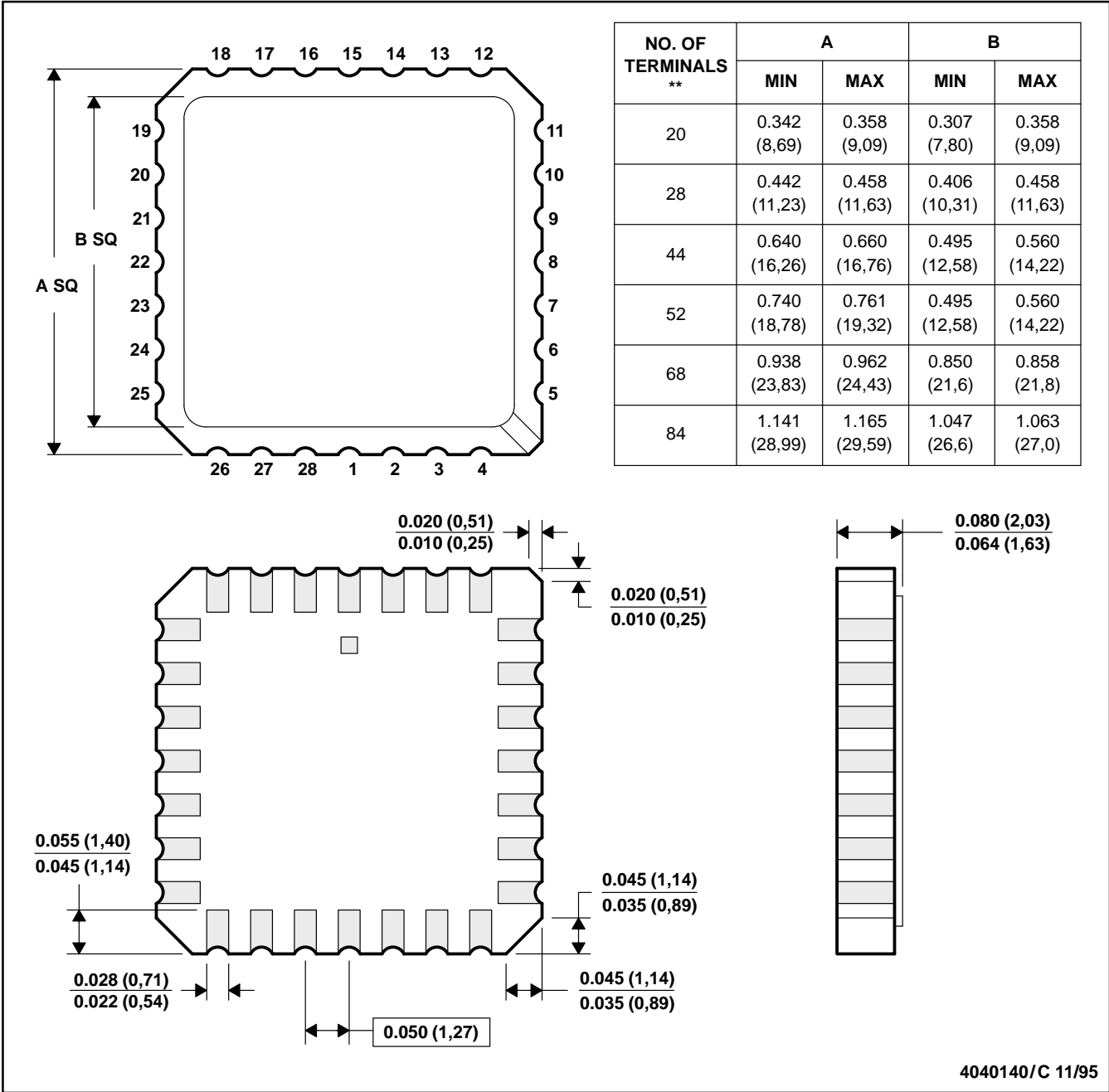
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## MECHANICAL DATA

**FK (S-CQCC-N\*\*)**

**LEADLESS CERAMIC CHIP CARRIER**

28 TERMINALS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold-plated.
  - E. Falls within JEDEC MS-004

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9958301QPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9958301QPA TL5001M	<a href="#">Samples</a>
5962-9958302Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9958302Q2A TL5001 AMFKB	<a href="#">Samples</a>
5962-9958302QPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9958302QPA TL5001AM	<a href="#">Samples</a>
TL5001ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	<a href="#">Samples</a>
TL5001ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	5001AC	<a href="#">Samples</a>
TL5001AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001AI	<a href="#">Samples</a>
TL5001AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL5001AIP	<a href="#">Samples</a>
TL5001AMFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9958302Q2A TL5001 AMFKB	<a href="#">Samples</a>
TL5001AMJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9958302QPA TL5001AM	<a href="#">Samples</a>
TL5001AQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001AQ	<a href="#">Samples</a>
TL5001AQDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		5001AQ	<a href="#">Samples</a>
TL5001AQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001AQ	<a href="#">Samples</a>
TL5001AQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		5001AQ	<a href="#">Samples</a>
TL5001CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL5001CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	5001C	<a href="#">Samples</a>
TL5001CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	TL5001CP	<a href="#">Samples</a>
TL5001CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		T5001	<a href="#">Samples</a>
TL5001CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	T5001	<a href="#">Samples</a>
TL5001ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001I	<a href="#">Samples</a>
TL5001IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5001I	<a href="#">Samples</a>
TL5001IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL5001IP	<a href="#">Samples</a>
TL5001IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL5001IP	<a href="#">Samples</a>
TL5001IPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		Z5001	<a href="#">Samples</a>
TL5001MJG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL5001MJG	<a href="#">Samples</a>
TL5001MJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9958301QPA TL5001M	<a href="#">Samples</a>
TL5001QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001Q	<a href="#">Samples</a>
TL5001QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		5001Q	<a href="#">Samples</a>
TL5001QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5001Q	<a href="#">Samples</a>
TL5001QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		5001Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL5001, TL5001A, TL5001AM, TL5001M :**

- Catalog : [TL5001A](#), [TL5001](#)
  
- Automotive : [TL5001A-Q1](#), [TL5001A-Q1](#)
  
- Military : [TL5001M](#), [TL5001AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5001ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001AQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TL5001IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001IPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TL5001QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5001QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5001ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5001AQDR	SOIC	D	8	2500	350.0	350.0	43.0
TL5001AQDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TL5001CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL5001CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL5001IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL5001IPSR	SO	PS	8	2000	356.0	356.0	35.0
TL5001QDR	SOIC	D	8	2500	350.0	350.0	43.0
TL5001QDRG4	SOIC	D	8	2500	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9958302Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL5001ACD	D	SOIC	8	75	507	8	3940	4.32
TL5001AID	D	SOIC	8	75	507	8	3940	4.32
TL5001AIDG4	D	SOIC	8	75	507	8	3940	4.32
TL5001AIP	P	PDIP	8	50	506	13.97	11230	4.32
TL5001AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL5001AQD	D	SOIC	8	75	505.46	6.76	3810	4
TL5001AQDG4	D	SOIC	8	75	505.46	6.76	3810	4
TL5001CD	D	SOIC	8	75	507	8	3940	4.32
TL5001CDG4	D	SOIC	8	75	507	8	3940	4.32
TL5001CP	P	PDIP	8	50	506	13.97	11230	4.32
TL5001CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL5001ID	D	SOIC	8	75	507	8	3940	4.32
TL5001IP	P	PDIP	8	50	506	13.97	11230	4.32
TL5001IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL5001QD	D	SOIC	8	75	505.46	6.76	3810	4
TL5001QDG4	D	SOIC	8	75	505.46	6.76	3810	4

## GENERIC PACKAGE VIEW

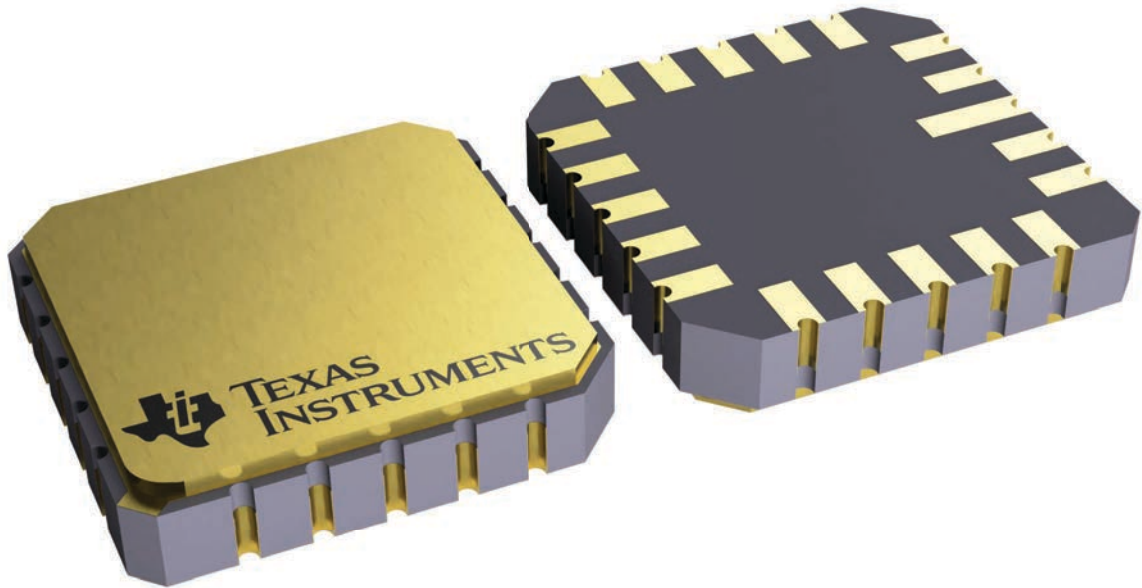
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

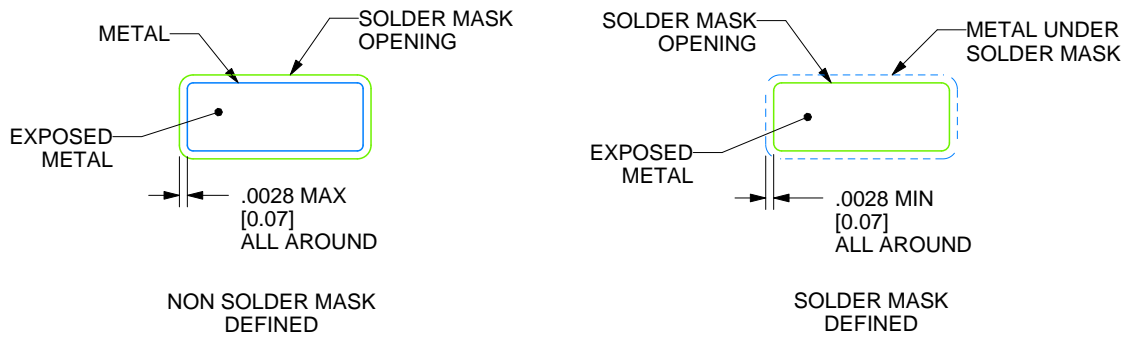
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

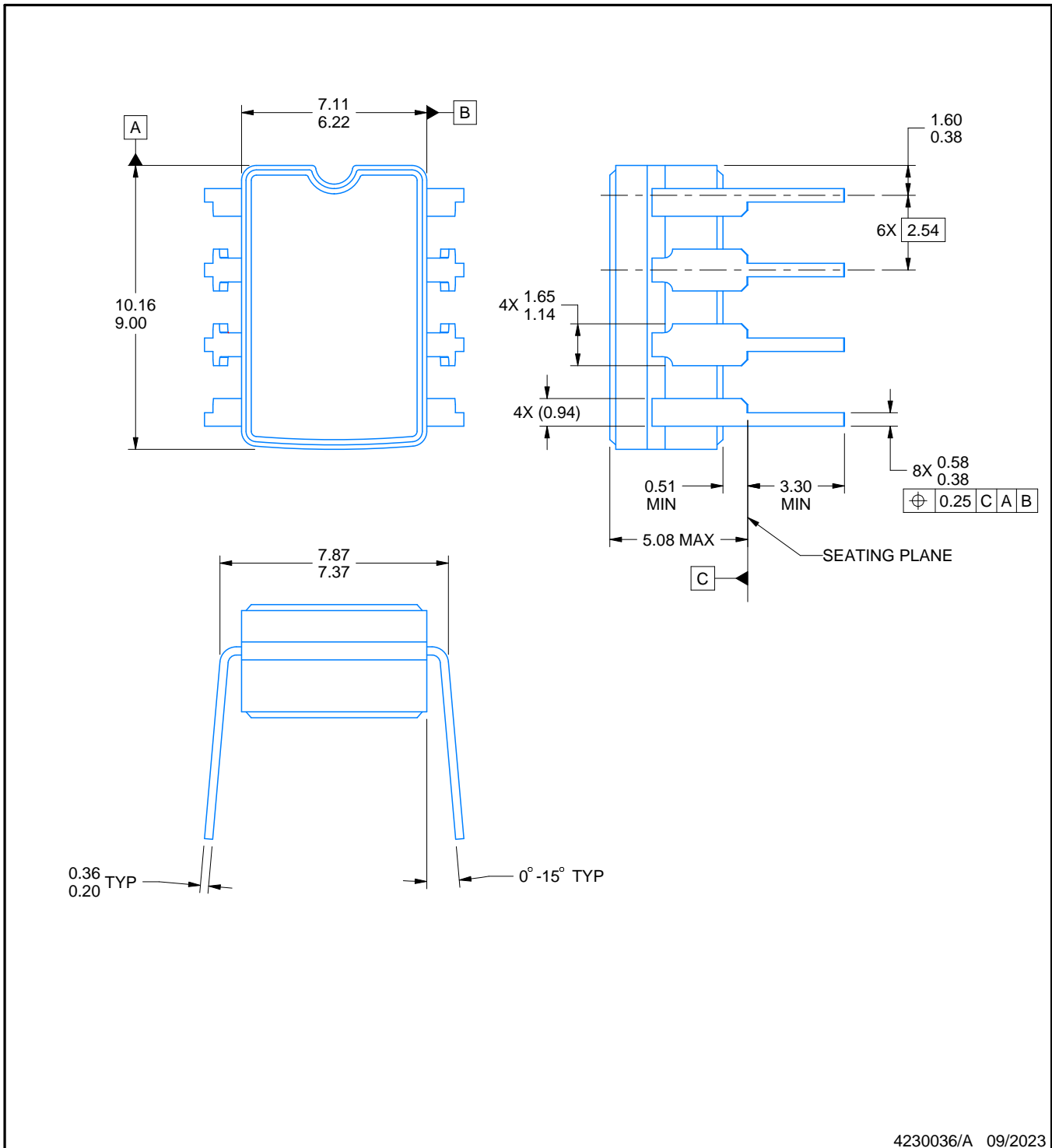


# PACKAGE OUTLINE

## JG0008A

### CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



#### NOTES:

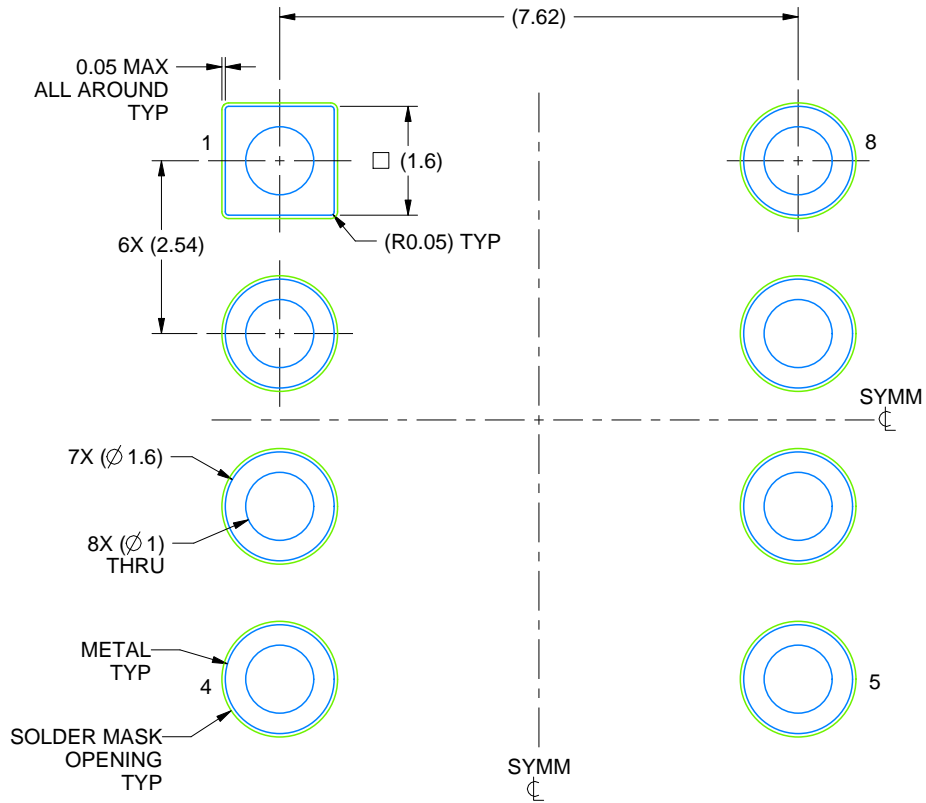
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

# EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE  
NON SOLDER MASK DEFINED  
SCALE: 9X

4230036/A 09/2023

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