

TLC2274M-MIL 高度なLinCMOSレール・ツー・レール・オペアンプ

1 特長

- 出カスイングに両方の電源レールを含む
- 低ノイズ: $f = 1\text{kHz}$ 時に $9\text{nV}/\sqrt{\text{Hz}}$ (標準値)
- 低い入力バイアス電流: 1pA (標準値)
- 単一電源と分割電源での動作を完全に規定
- 同相入力電圧範囲に負のレールを含む
- 高いゲイン帯域幅: 2.2MHz (標準値)
- 高いスルー・レート: $3.6\text{V}/\mu\text{s}$ (標準値)
- 低い入力オフセット電圧: $T_A = 25^\circ\text{C}$ 時に 2.5mV (最大値)
- マクロモデル内蔵
- TLC272およびTLC274の性能強化版
- Q-Temp車載用で利用可能

2 アプリケーション

- 白物家電(冷蔵庫、洗濯機)
- ハンドヘルド監視システム
- 構成制御と印刷のサポート
- トランスデューサ・インターフェイス
- バッテリ駆動のアプリケーション

3 概要

TLC2274M-MILデバイスは、テキサス・インスツルメンツ製のクワッド・オペアンプです。このデバイスはレール・ツー・レールの出力性能があり、単一および分割電源アプリケーションでダイナミック・レンジが増大します。

TLC2274M-MILデバイスは 2MHz の帯域幅と $3\text{V}/\mu\text{s}$ のスルー・レートを実現しており、高速アプリケーションに適しています。このデバイスは既存のCMOSオペアンプと同等のAC性能を備えながら、ノイズ、入力オフセット電圧、消費電力の点でCMOSオペアンプより優れています。

TLC2274M-MILデバイスのノイズ電圧は $9\text{nV}/\sqrt{\text{Hz}}$ で、競合ソリューションの半分です。

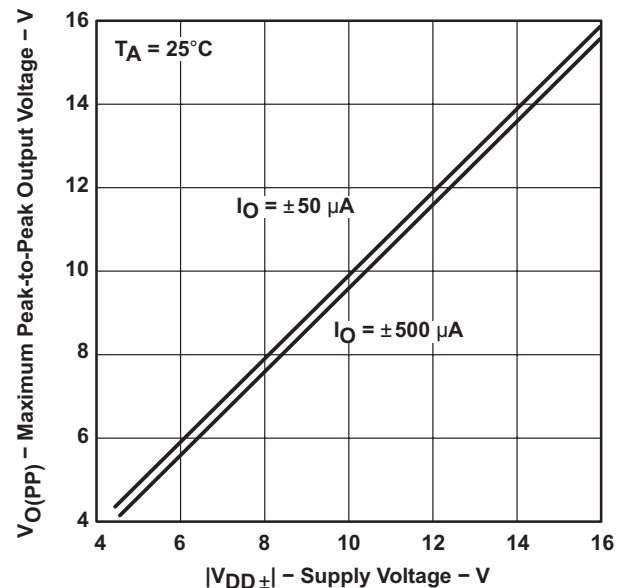
TLC2274M-MILデバイスは入力インピーダンスが高く、ノイズが低いため、圧電性トランスデューサなど高インピーダンスのソース用の小信号コンディショニングに最適です。Micropowerの消費電力レベルであるため、ハンドヘルドの監視機器やリモート・センシング・アプリケーションで適切に動作します。さらに、単一または分割電源でレール・ツー・レール出力が可能のため、このデバイスはA/Dコンバータ(ADC)と接続するための優れた選択肢です。高精度のアプリケーション向けには、最大入力オフセット電圧 $950\mu\text{V}$ のTLC2272AM-MILデバイスが利用可能です。このデバイスは 5V および $\pm 5\text{V}$ で完全に動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLC2274M-MIL	SOIC (14)	3.91mm×8.65mm
	CDIP (14)	6.67mm×19.56mm
	LCCC (20)	8.89mm×8.89mm
	CFP (14)	6.35mm×19.30mm
	PDIP (14)	6.35mm×19.30mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

最大ピーク・ツー・ピーク出力電圧と電源電圧との関係



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4 改訂履歴

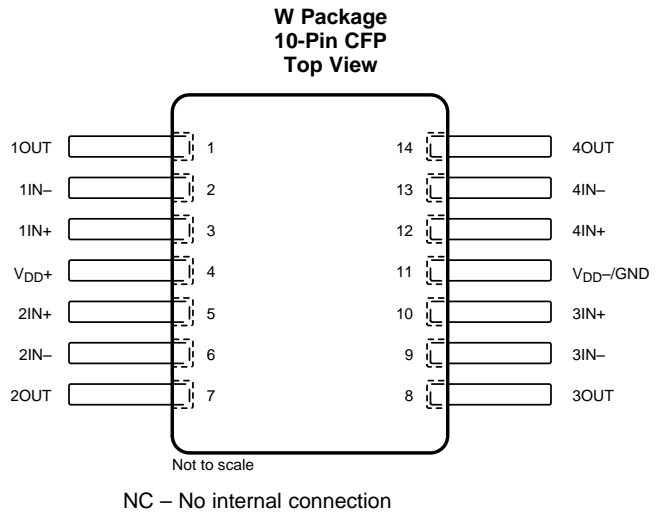
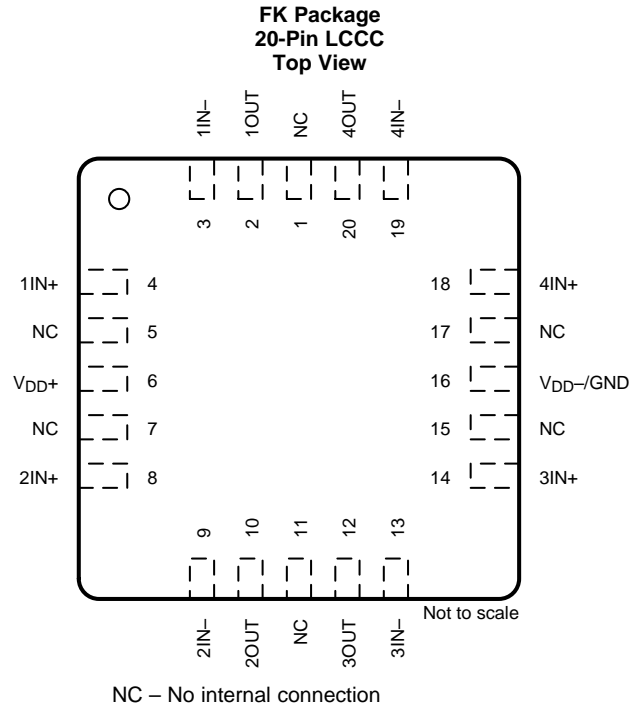
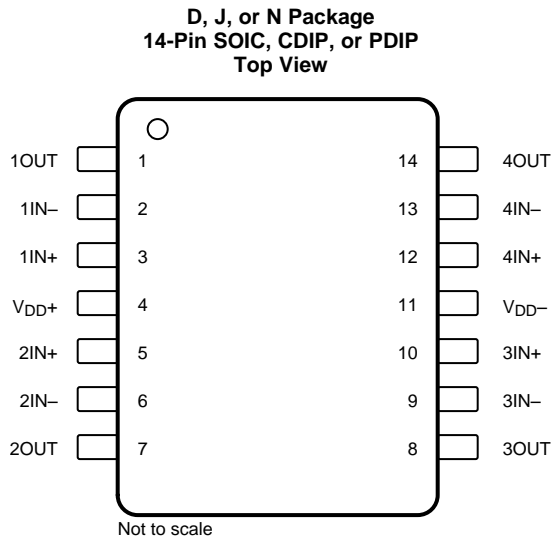
日付	改訂内容	注
2017年6月	*	初版

5 概要（続き）

TLC2274M-MIL デバイスは、標準設計における TLC272 のアップグレードとしても優れており、出力ダイナミック・レンジの増大、ノイズ電圧の低下、入力オフセット電圧の低下を実現できます。これらの拡張機能セットから、広範なアプリケーションで使用可能です。高い出力駆動能力と、広い入力電圧範囲を必要とするアプリケーション向けには、TLV2432 および TLV2442 デバイスを参照してください。

設計に必要なアンプが1つだけの場合は、TLV2211、TLV2221、TLV2231 ファミリーを参照してください。これらのデバイスは単一のレール・ツー・レール・オペアンプで、SOT-23 パッケージで供給されます。サイズが小さく、消費電力が低いため、高密度のバッテリー駆動機器に最適です。

6 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	NO.			
	D, J, N, or W	FK		
1IN+	3	4	I	Non-inverting input, Channel 1
1IN–	2	3	I	Inverting input, Channel 1
1OUT	1	2	O	Output, Channel 1
2IN+	5	8	I	Non-inverting input, Channel 2
2IN–	6	9	I	Inverting input, Channel 2
2OUT	7	10	O	Output, Channel 2
3IN+	10	14	I	Non-inverting input, Channel 3
3IN–	9	13	I	Inverting input, Channel 3
3OUT	8	12	O	Output, Channel 3
4IN+	12	18	I	Non-inverting input, Channel 4
4IN–	13	19	I	Inverting input, Channel 4
4OUT	14	20	O	Output, Channel 4
V _{DD} ⁺	4	6	—	Positive (highest) supply
V _{DD} [–]	11	16	—	Negative (lowest) supply
V _{DD} [–] /GND	—	—	—	Negative (lowest) supply
NC	—	1, 5, 7, 11, 15, 17	—	No connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{DD+} ⁽²⁾		8	V
V_{DD-} ⁽²⁾	-8		V
Differential input voltage, V_{ID} ⁽³⁾		±16	V
Input voltage, V_I (any input) ⁽²⁾	$V_{DD-} - 0.3$	V_{DD+}	V
Input current, I_I (any input)		±5	mA
Output current, I_O		±50	mA
Total current into V_{DD+}		±50	mA
Total current out of V_{DD-}		±50	mA
Duration of short-circuit current at (or below) 25°C ⁽⁴⁾		Unlimited	
Operating ambient temperature range, T_A	-55	125	
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
- (3) Differential voltages are at IN+ with respect to IN-. Excessive current will flow if input is brought below $V_{DD-} - 0.3$ V.
- (4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	Devices in D packages	±2000	V
	Charged-device model (CDM), per AEC Q100-011	Devices in D packages	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{DD±}$	Supply voltage	±2.2	±8	V
V_I	Input voltage	V_{DD-}	$V_{DD+} - 1.5$	V
V_{IC}	Common-mode input voltage	V_{DD-}	$V_{DD+} - 1.5$	V
T_A	Operating ambient temperature	-55	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TLC2274M-MIL					UNIT
	D (SOIC)	J (CDIP)	FK (LCCC)	N (PDIP)	W (CFP)	
	14-PIN	14-PIN	20-PIN	14-PIN	14-PIN	
$R_{θJA}$	Junction-to-ambient thermal resistance ⁽²⁾⁽³⁾	115.6	—	—	—	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance ⁽²⁾⁽³⁾	61.8	16.2	18	121.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	55.9	—	—	—	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	14.3	—	—	—	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	55.4	—	—	—	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	8.68	°C/W

- (1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
- (2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{θJA}$, and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{θJA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

7.5 TLC2274M-MIL Electrical Characteristics $V_{DD} = 5\text{ V}$

at specified ambient temperature, $V_{DD} = 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V_{IO}	Input offset voltage	$V_{IC} = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		300	2500	μV	
			$T_A = -55^\circ\text{C}$ to 125°C			3000		
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$	
	Input offset voltage long-term drift ⁽¹⁾	$V_{IC} = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$			0.002		$\mu\text{V}/\text{mo}$	
I_{IO}	Input offset current	$V_{IC} = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		0.5	60	pA	
			$T_A = -55^\circ\text{C}$ to 125°C			800		
I_{IB}	Input bias current	$V_{IC} = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		1	60	pA	
			$T_A = -55^\circ\text{C}$ to 125°C			800		
V_{ICR}	Common-mode input voltage	$R_S = 50\ \Omega$; $ V_{IO} \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$		-0.3	2.5	4	V
			$T_A = -55^\circ\text{C}$ to 125°C		0	2.5	3.5	
V_{OH}	High-level output voltage		$I_{OH} = -20\ \mu\text{A}$		4.99		V	
			$I_{OH} = -200\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	4.85	4.93		
				$T_A = -55^\circ\text{C}$ to 125°C	4.85			
			$I_{OH} = -1\text{ mA}$	$T_A = 25^\circ\text{C}$	4.25	4.65		
$T_A = -55^\circ\text{C}$ to 125°C	4.25							
V_{OL}	Low-level output voltage	$V_{IC} = 2.5\text{ V}$	$I_{OL} = 50\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	0.01		V	
				$T_A = -55^\circ\text{C}$ to 125°C	0.09	0.15		
			$I_{OL} = 500\ \mu\text{A}$	$T_A = 25^\circ\text{C}$		0.15		
				$T_A = -55^\circ\text{C}$ to 125°C	0.9	1.5		
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V}$ to 4 V , $R_L = 10\text{ k}\Omega^{(2)}$	$T_A = 25^\circ\text{C}$		15	35	V/mV	
			$T_A = -55^\circ\text{C}$ to 125°C		15			
		$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V}$ to 4 V ; $R_L = 1\text{ M}\Omega^{(2)}$			175			
r_{id}	Differential input resistance				10^{12}		Ω	
r_i	Common-mode input resistance				10^{12}		Ω	
c_i	Common-mode input capacitance	$f = 10\text{ kHz}$, P package			8		pF	
z_o	Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 10$			140		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ V}$ to 2.7 V , $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		70	75	dB	
			$T_A = -55^\circ\text{C}$ to 125°C		70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4\text{ V}$ to 16 V , $V_{IC} = V_{DD} / 2$, no load	$T_A = 25^\circ\text{C}$		80	95	dB	
			$T_A = -55^\circ\text{C}$ to 125°C		80			
I_{DD}	Supply current	$V_O = 2.5\text{ V}$, no load	$T_A = 25^\circ\text{C}$		4.4	6	mA	
			$T_A = -55^\circ\text{C}$ to 125°C			3		
SR	Slew rate at unity gain	$V_O = 0.5\text{ V}$ to 2.5 V , $R_L = 10\text{ k}\Omega^{(2)}$, $C_L = 100\text{ pF}^{(2)}$	$T_A = 25^\circ\text{C}$		2.3	3.6	$\text{V}/\mu\text{s}$	
			$T_A = -55^\circ\text{C}$ to 125°C		1.7			
V_n	Equivalent input noise voltage		$f = 10\text{ Hz}$		50		$\text{nV}/\sqrt{\text{Hz}}$	
			$f = 1\text{ kHz}$		9			
V_{NPP}	Peak-to-peak equivalent input noise voltage		$f = 0.1\text{ Hz}$ to 1 Hz		1		μV	
			$f = 0.1\text{ Hz}$ to 10 Hz		1.4			
I_n	Equivalent input noise current				0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = 0.5\text{ V}$ to 2.5 V , $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega^{(2)}$	$A_V = 1$		0.0013%			
			$A_V = 10$		0.004%			
			$A_V = 100$		0.03%			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega^{(2)}$, $C_L = 100\text{ pF}^{(2)}$			2.18		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega^{(2)}$, $C_L = 100\text{ pF}^{(2)}$			1		MHz	
t_s	Settling time	$A_V = -1$, $R_L = 10\text{ k}\Omega^{(2)}$, Step = 0.5 V to 2.5 V , $C_L = 100\text{ pF}^{(2)}$	T_o 0.1%		1.5		μs	
			T_o 0.01%		2.6			

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV .

(2) Referenced to 0 V .

TLC2274M-MIL Electrical Characteristics $V_{DD} = 5\text{ V}$ (continued)

 at specified ambient temperature, $V_{DD} = 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega^{(2)}$, $C_L = 100\text{ pF}^{(2)}$		50		$^\circ$
	Gain margin	$R_L = 10\text{ k}\Omega^{(2)}$, $C_L = 100\text{ pF}^{(2)}$		10		dB

7.6 TLC2274M-MIL Electrical Characteristics $V_{DD\pm} = \pm 5\text{ V}$

at specified ambient temperature, $V_{DD\pm} = \pm 5\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V_{IO}	Input offset voltage	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		300	2500	μV	
			$T_A = -55^\circ\text{C}$ to 125°C			3000		
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$			2		$\mu\text{V}/^\circ\text{C}$	
	Input offset voltage long-term drift	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$			0.002		$\mu\text{V}/\text{mo}$	
I_{IO}	Input offset current	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		0.5	60	pA	
			$T_A = -55^\circ\text{C}$ to 125°C					800
I_{IB}	Input bias current	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		1	60	pA	
			$T_A = -55^\circ\text{C}$ to 125°C					800
V_{ICR}	Common-mode input voltage	$R_S = 50\ \Omega$; $ V_{IO} \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$		-5.3	0	4	V
			$T_A = -55^\circ\text{C}$ to 125°C		-5	0	3.5	
V_{OM+}	Maximum positive peak output voltage	$V_{IC} = 0\text{ V}$	$I_O = -20\ \mu\text{A}$		4.99		V	
			$I_O = -200\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	4.85	4.93		
				$T_A = -55^\circ\text{C}$ to 125°C	4.85			
			$I_O = -1\text{ mA}$	$T_A = 25^\circ\text{C}$	4.25	4.65		
$T_A = -55^\circ\text{C}$ to 125°C	4.25							
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0\text{ V}$	$I_O = 50\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	-4.99		V	
				$T_A = -55^\circ\text{C}$ to 125°C	-4.85	-4.91		
			$I_O = 500\ \mu\text{A}$	$T_A = 25^\circ\text{C}$	-4.85			
				$T_A = -55^\circ\text{C}$ to 125°C	-3.5	-4.1		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$; $R_L = 10\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$		20	50	V/mV	
			$T_A = -55^\circ\text{C}$ to 125°C		20			
		$V_O = \pm 4\text{ V}$; $R_L = 1\ \text{M}\Omega$			300			
r_{id}	Differential input resistance				10^{12}		Ω	
r_i	Common-mode input resistance				10^{12}		Ω	
c_i	Common-mode input capacitance	$f = 10\ \text{kHz}$, P package			8		pF	
z_o	Closed-loop output impedance	$f = 1\ \text{MHz}$, $A_V = 10$			130		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = -5\text{ V}$ to 2.7 V , $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		75	80	dB	
			$T_A = -55^\circ\text{C}$ to 125°C		75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD\pm} = 2.2\text{ V}$ to $\pm 8\text{ V}$, $V_{IC} = 0\text{ V}$, no load	$T_A = 25^\circ\text{C}$		80	95	dB	
			$T_A = -55^\circ\text{C}$ to 125°C		80			
I_{DD}	Supply current	$V_O = 0\text{ V}$, no load	$T_A = 25^\circ\text{C}$		4.8	6	mA	
			$T_A = -55^\circ\text{C}$ to 125°C					6
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $R_L = 10\ \text{k}\Omega$, $C_L = 100\ \text{pF}$	$T_A = 25^\circ\text{C}$		2.3	3.6	$\text{V}/\mu\text{s}$	
			$T_A = -55^\circ\text{C}$ to 125°C		1.7			
V_n	Equivalent input noise voltage	$f = 10\ \text{Hz}$ $f = 1\ \text{kHz}$			50		$\text{nV}/\sqrt{\text{Hz}}$	
					9			
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\ \text{Hz}$ to $1\ \text{Hz}$ $f = 0.1\ \text{Hz}$ to $10\ \text{Hz}$			1		μV	
					1.4			
I_n	Equivalent input noise current				0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = \pm 2.3$, $f = 20\ \text{kHz}$, $R_L = 10\ \text{k}\Omega$	$A_V = 1$		0.0011%			
			$A_V = 10$		0.004%			
			$A_V = 100$		0.03%			
	Gain-bandwidth product	$f = 10\ \text{kHz}$, $R_L = 10\ \text{k}\Omega$, $C_L = 100\ \text{pF}$			2.25		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $A_V = 1$, $R_L = 10\ \text{k}\Omega$, $C_L = 100\ \text{pF}$			0.54		MHz	
t_s	Settling time	$A_V = -1$, $R_L = 10\ \text{k}\Omega$, Step = -2.3 V to 2.3 V , $C_L = 100\ \text{pF}$	$T_O = 0.1\%$		1.5		μs	
			$T_O = 0.01\%$		3.2			
ϕ_m	Phase margin at unity gain	$R_L = 10\ \text{k}\Omega$, $C_L = 100\ \text{pF}$			52		$^\circ$	
	Gain margin	$R_L = 10\ \text{k}\Omega$, $C_L = 100\ \text{pF}$			10		dB	

7.7 Typical Characteristics

Table 1. Table of Graphs

			FIGURE⁽¹⁾
V_{IO}	Input offset voltage	Distribution	1, 2
		vs Common-mode voltage	3, 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5, 6 ⁽²⁾
I_B / I_{IO}	Input bias and input offset current	vs Ambient temperature	7 ⁽²⁾
V_I	Input voltage	vs Supply voltage	8
		vs Ambient temperature	9 ⁽²⁾
V_{OH}	High-level output voltage	vs High-level output current	10 ⁽²⁾
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12 ⁽²⁾
V_{OM+}	Maximum positive peak output voltage	vs Output current	13 ⁽²⁾
V_{OM-}	Maximum negative peak output voltage	vs Output current	14 ⁽²⁾
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15
I_{OS}	Short-circuit output current	vs Supply voltage	16
		vs Ambient temperature	17 ⁽²⁾
V_O	Output voltage	vs Differential input voltage	18, 19
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	20
	Large-signal differential voltage amplification and phase margin	vs Frequency	21, 22
	Large-signal differential voltage amplification	vs Ambient temperature	23 ⁽²⁾ , 24 ⁽²⁾
z_0	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency	27
		vs Ambient temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	29, 30
		vs Ambient temperature	31 ⁽²⁾
I_{DD}	Supply current	vs Supply voltage	⁽²⁾ , 32 ⁽²⁾
		vs Ambient temperature	⁽²⁾ , 33 ⁽²⁾
SR	Slew rate	vs Load Capacitance	34
		vs Ambient temperature	35 ⁽²⁾
V_O	Inverting large-signal pulse response		36, 37
	Voltage-follower large-signal pulse response		38, 39
	Inverting small-signal pulse response		40, 41
	Voltage-follower small-signal pulse response		42, 43
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage over a 10-second period		46
	Integrated noise voltage	vs Frequency	47
THD+N	Total harmonic distortion + noise	vs Frequency	48
	Gain-bandwidth product	vs Supply voltage	49
		vs Ambient temperature	50 ⁽²⁾
ϕ_m	Phase margin	vs Load capacitance	51
	Gain margin	vs Load capacitance	52

(1) For all graphs where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

(2) Data at high and low temperatures are applicable only within the rated operating ambient temperature ranges of the various devices.

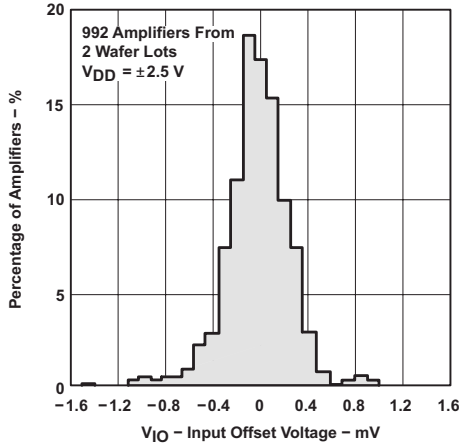


Figure 1. Distribution of Input Offset Voltage

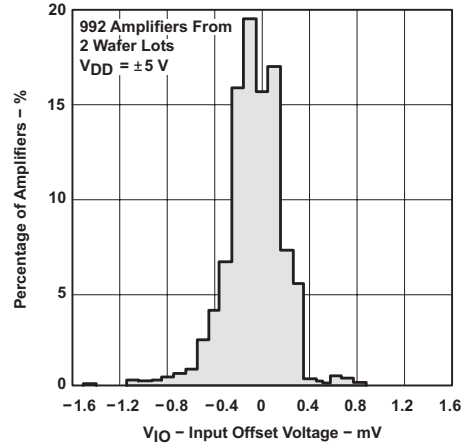


Figure 2. Distribution of Input Offset Voltage

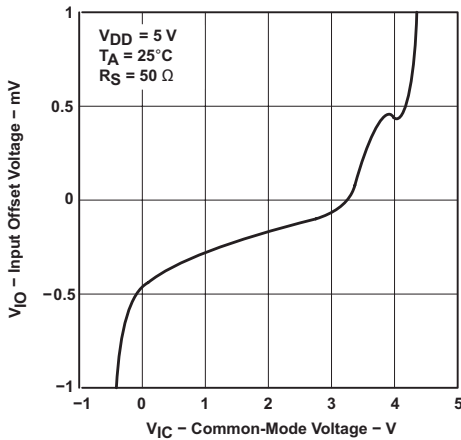


Figure 3. Input Offset Voltage vs Common-Mode Voltage

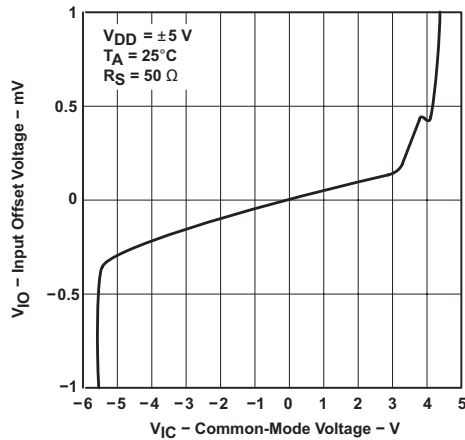


Figure 4. Input Offset Voltage vs Common-Mode Voltage

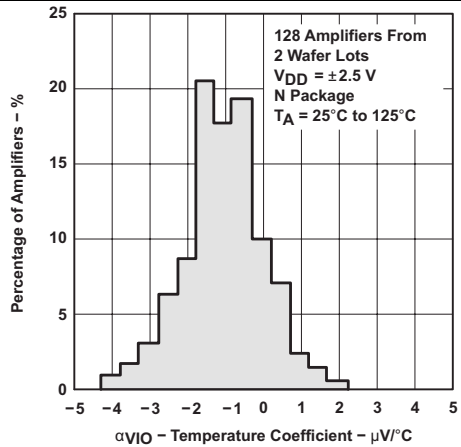


Figure 5. Distribution vs Input-Offset-Voltage Temperature Coefficient

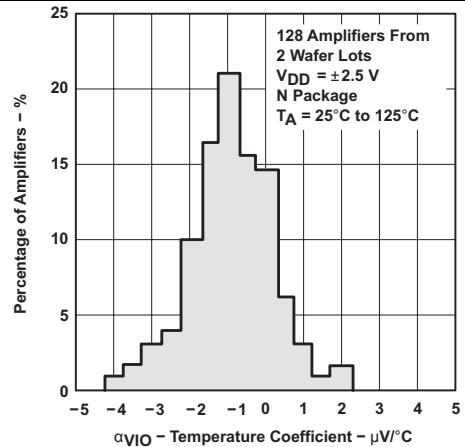


Figure 6. Distribution vs Input-Offset-Voltage Temperature Coefficient

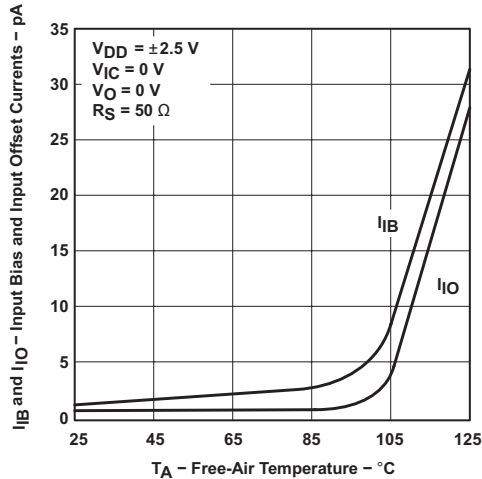


Figure 7. Input Bias and Input Offset Current vs Ambient Temperature

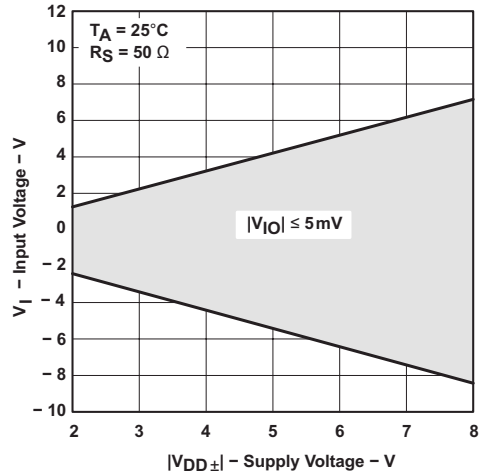


Figure 8. Input Voltage vs Supply Voltage

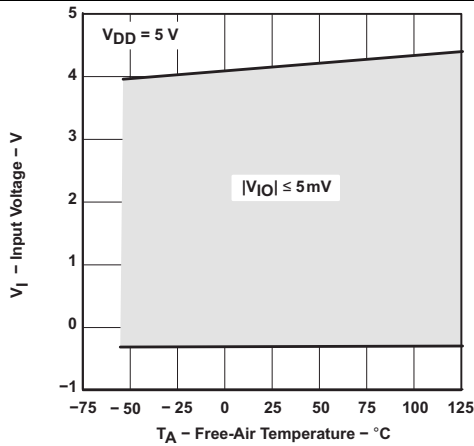


Figure 9. Input Voltage vs Ambient Temperature

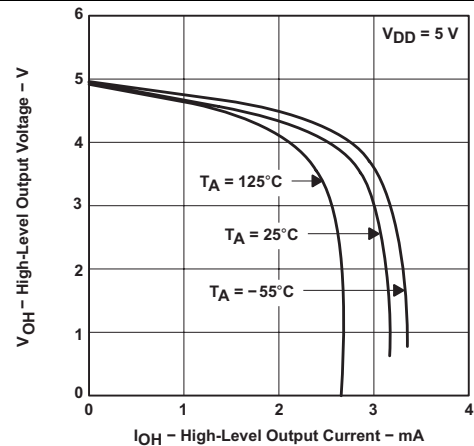


Figure 10. High-Level Output Voltage vs High-Level Output Current

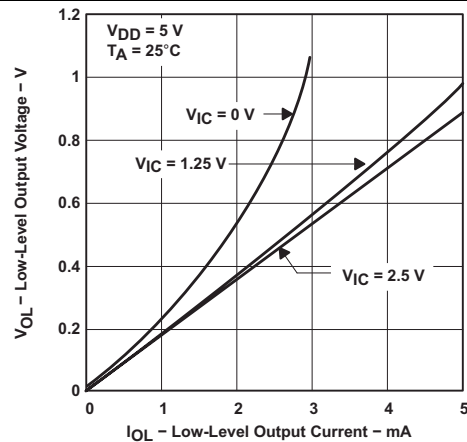


Figure 11. Low-Level Output Voltage vs Low-Level Output Current

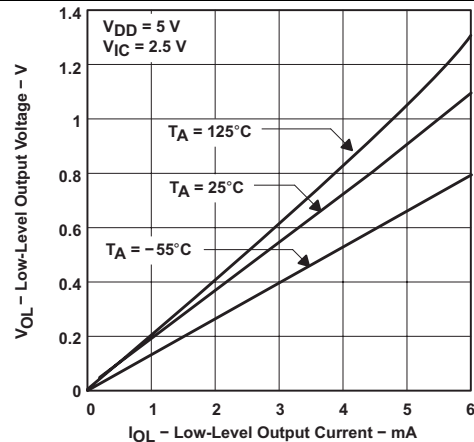


Figure 12. Low-Level Output Voltage vs Low-Level Output Current

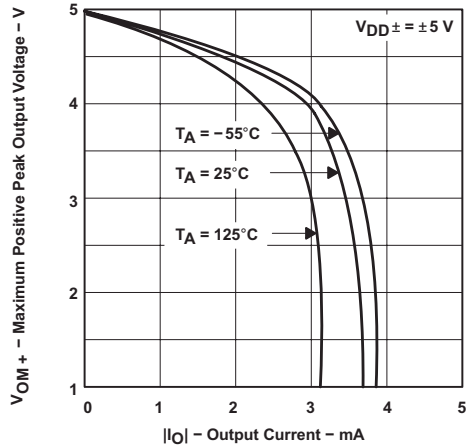


Figure 13. Maximum Positive Peak Output Voltage vs Output Current

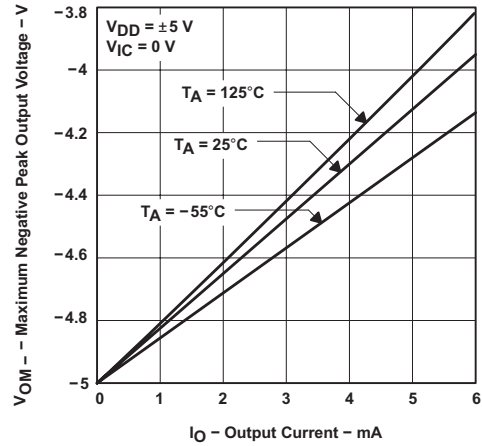


Figure 14. Maximum Negative Peak Output Voltage vs Output Current

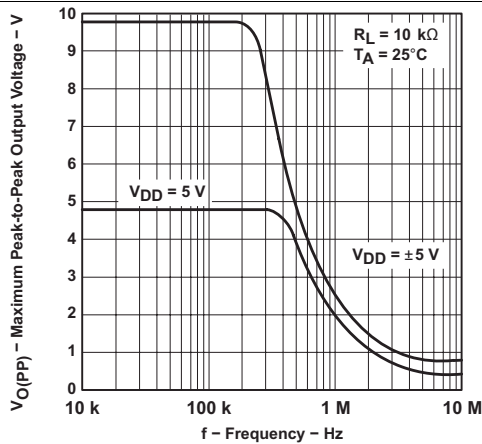


Figure 15. Maximum Peak-to-Peak Output Voltage vs Frequency

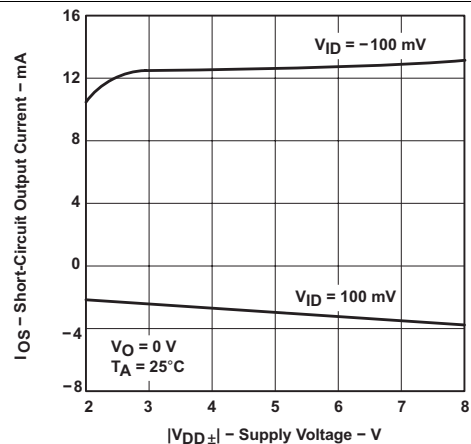


Figure 16. Short-Circuit Output Current vs Supply Voltage

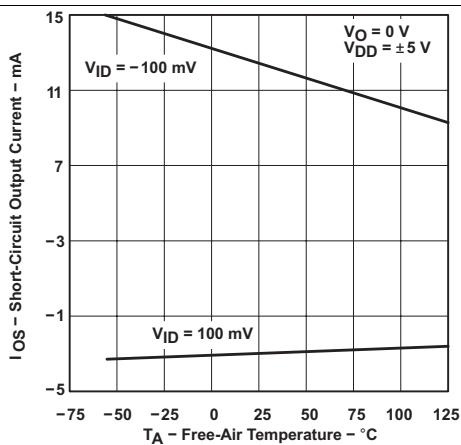


Figure 17. Short-Circuit Output Current vs Ambient Temperature

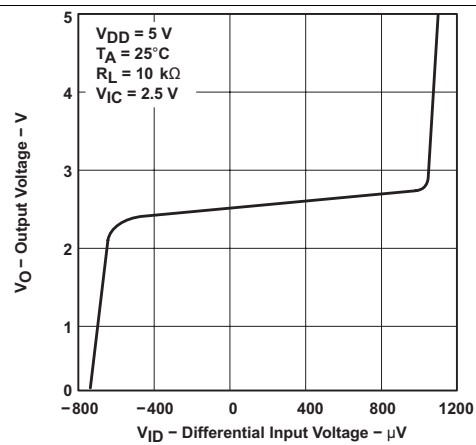


Figure 18. Output Voltage vs Differential Input Voltage

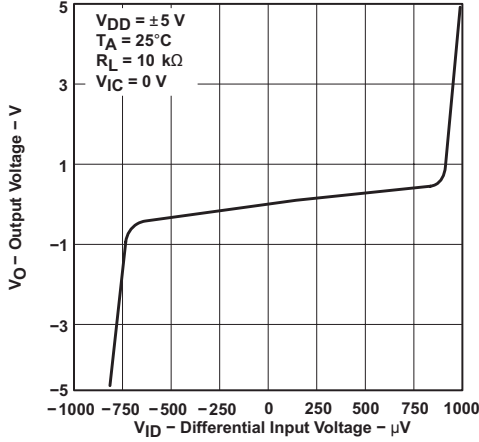


Figure 19. Output Voltage vs Differential Input Voltage

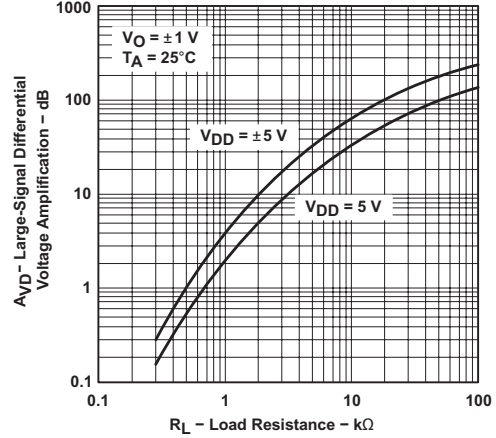


Figure 20. Large-Signal Differential Voltage Amplification vs Load Resistance

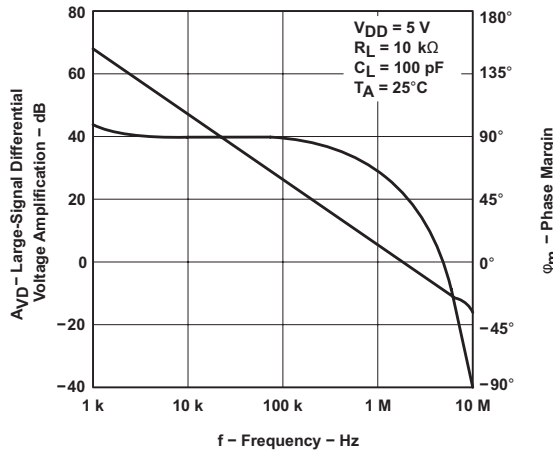


Figure 21. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

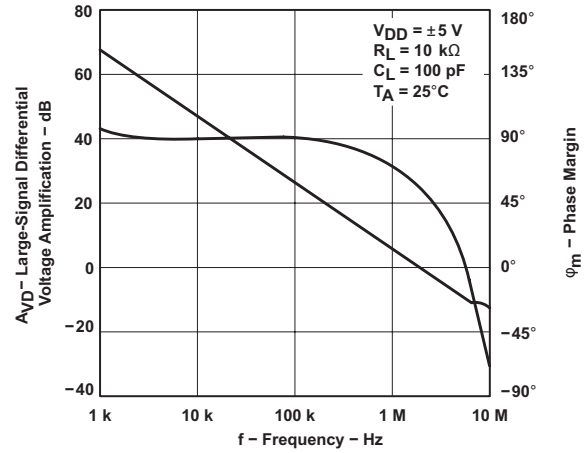


Figure 22. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

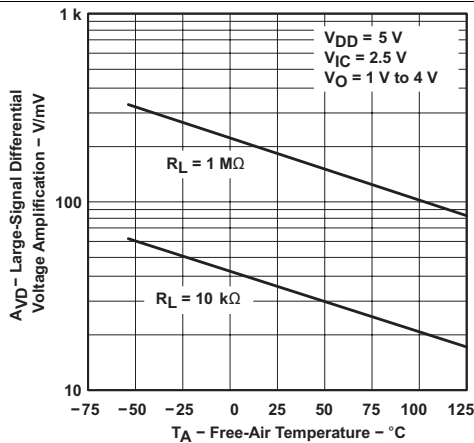


Figure 23. Large-Signal Differential Voltage Amplification vs Ambient Temperature

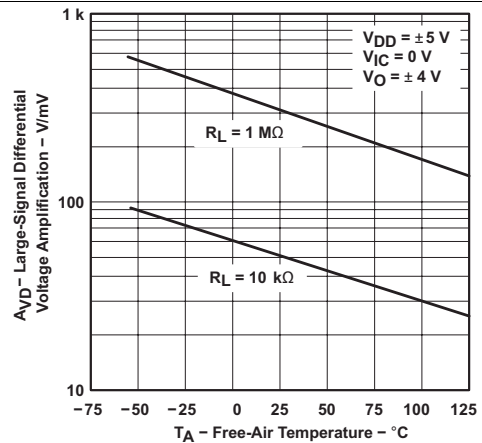


Figure 24. Large-Signal Differential Voltage Amplification vs Ambient Temperature

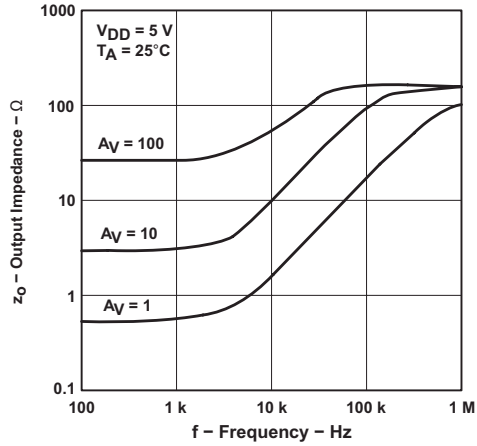


Figure 25. Output Impedance vs Frequency

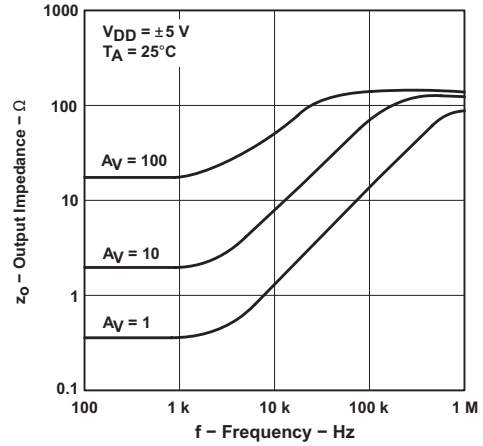


Figure 26. Output Impedance vs Frequency

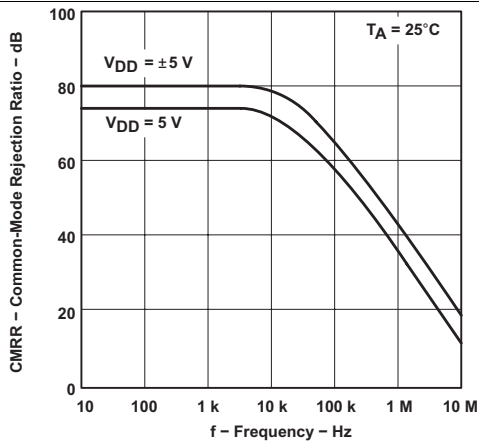


Figure 27. Common-Mode Rejection Ratio vs Frequency

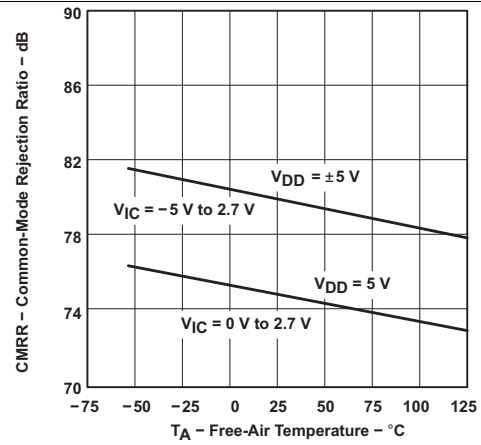


Figure 28. Common-Mode Rejection Ratio vs Ambient Temperature

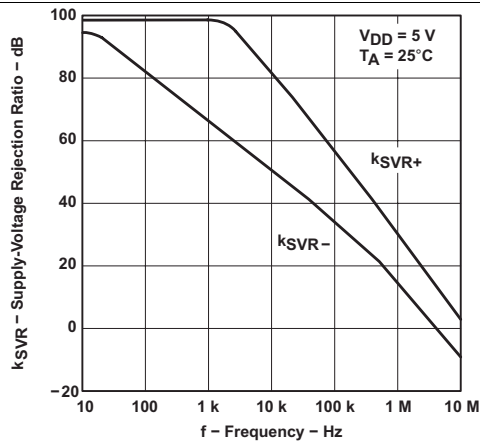


Figure 29. Supply-Voltage Rejection Ratio vs Frequency

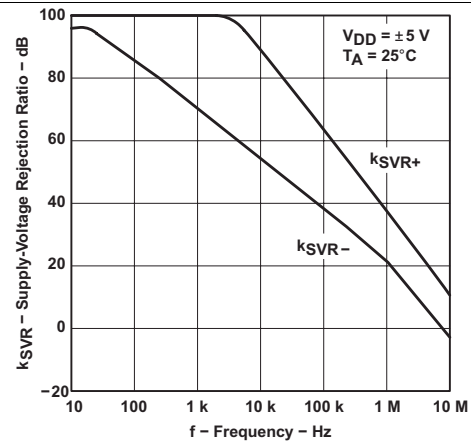


Figure 30. Supply-Voltage Rejection Ratio vs Frequency

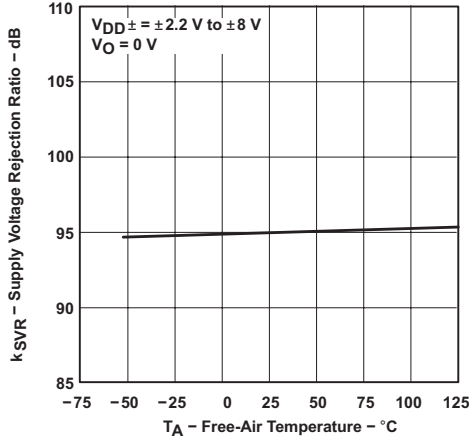


Figure 31. Supply-Voltage Rejection Ratio vs Ambient Temperature

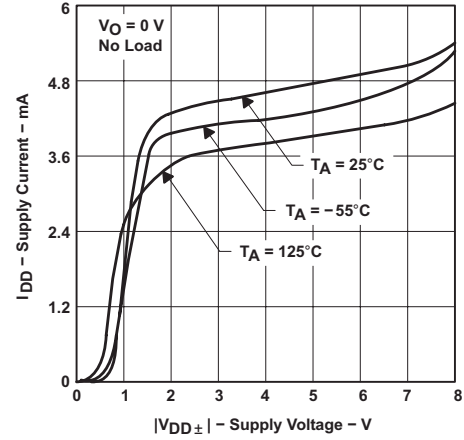


Figure 32. Supply Current vs Supply Voltage

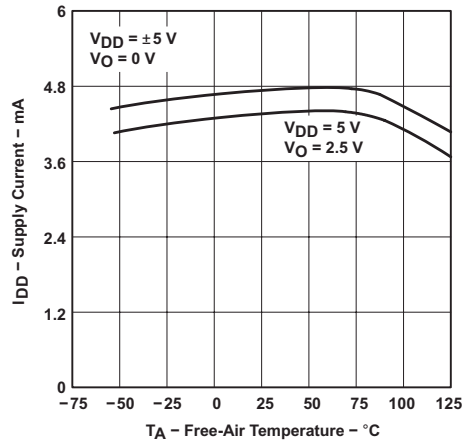


Figure 33. Supply Current vs Ambient Temperature

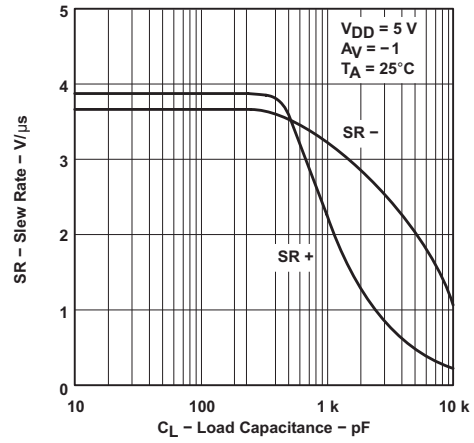


Figure 34. Slew Rate vs Load Capacitance

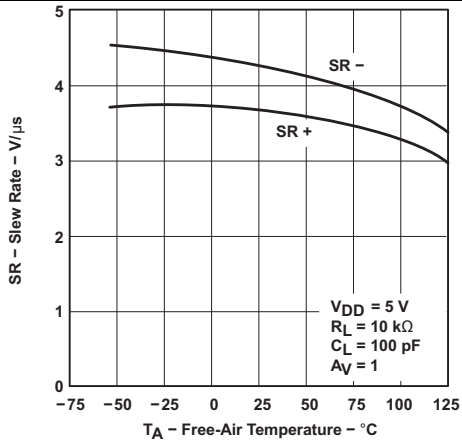


Figure 35. Slew Rate vs Ambient Temperature

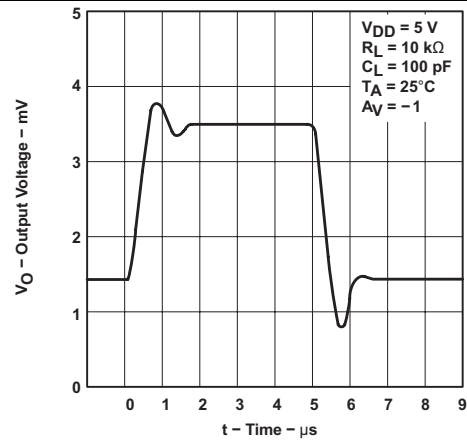


Figure 36. Inverting Large-Signal Pulse Response

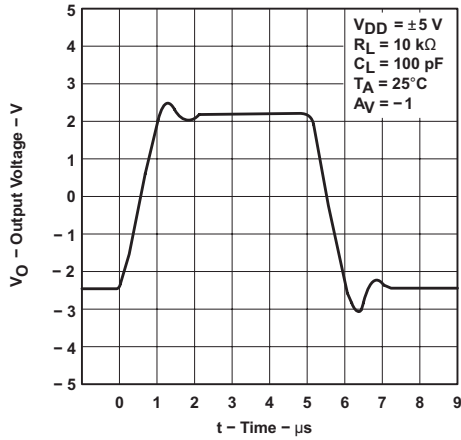


Figure 37. Inverting Large-Signal Pulse Response

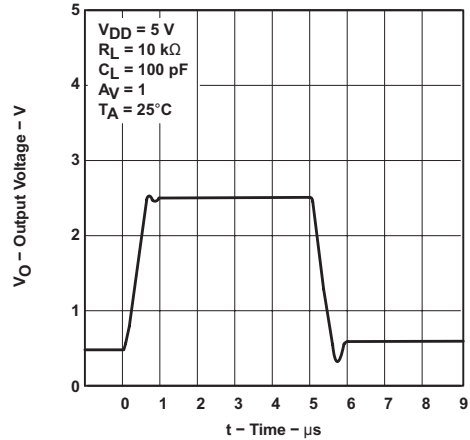


Figure 38. Voltage-Follower Large-Signal Pulse Response

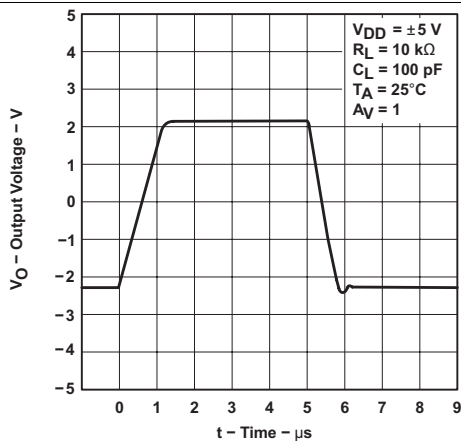


Figure 39. Voltage-Follower Large-Signal Pulse Response

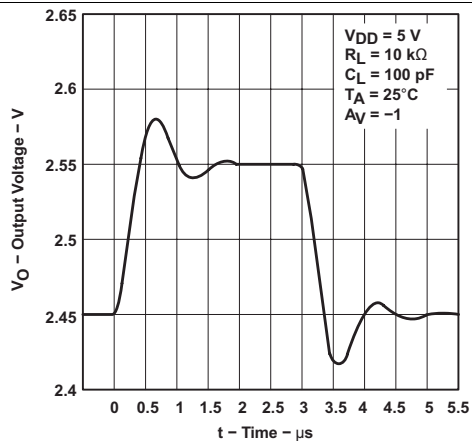


Figure 40. Inverting Small-Signal Pulse Response

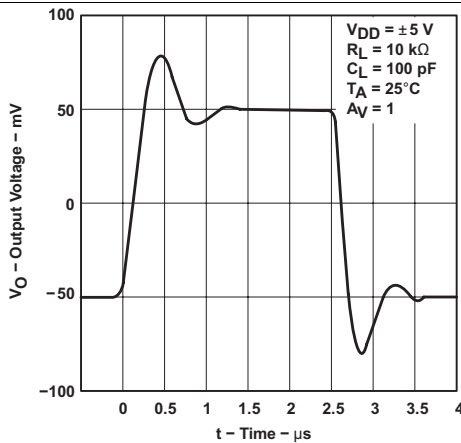


Figure 41. Inverting Small-Signal Pulse Response

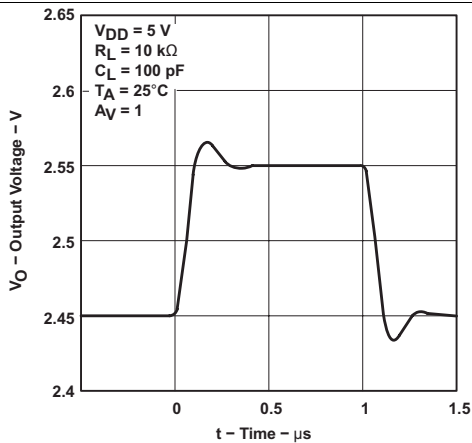


Figure 42. Voltage-Follower Small-Signal Pulse Response

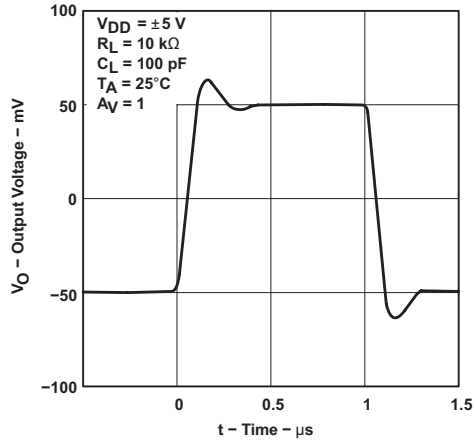


Figure 43. Voltage-Follower Small-Signal Pulse Response

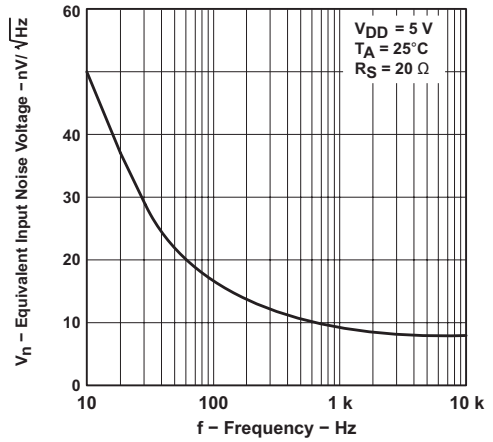


Figure 44. Equivalent Input Noise Voltage vs Frequency

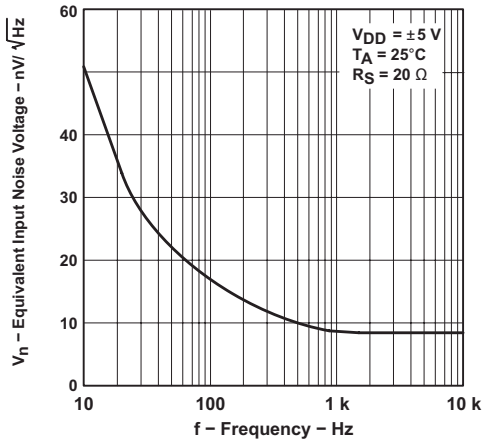


Figure 45. Equivalent Input Noise Voltage vs Frequency

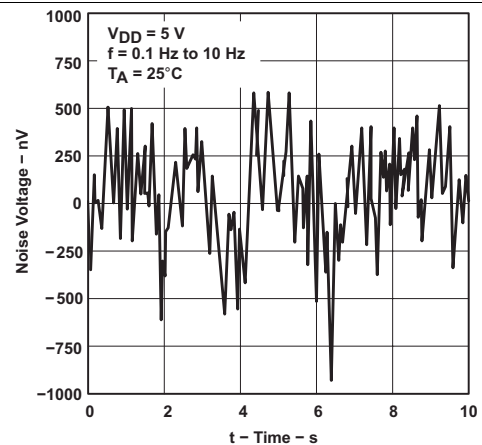


Figure 46. Noise Voltage Over a 10-Second Period

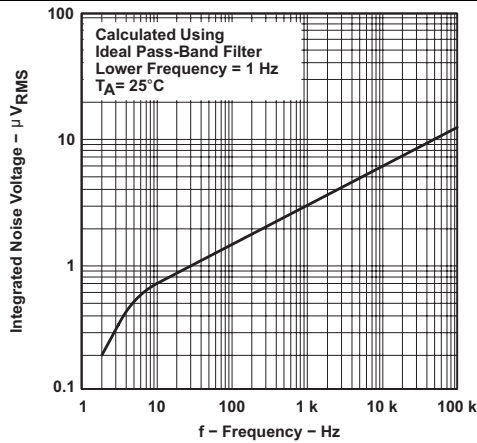


Figure 47. Integrated Noise Voltage vs Frequency

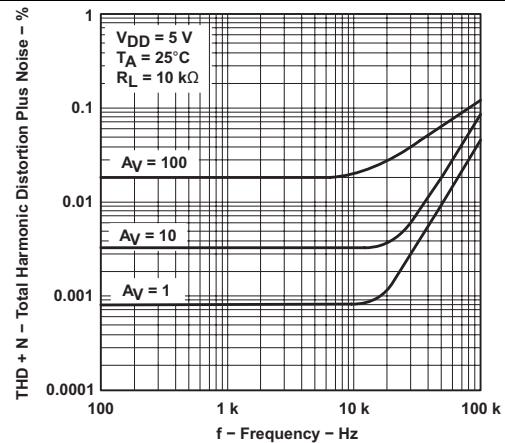


Figure 48. Total Harmonic Distortion + Noise vs Frequency

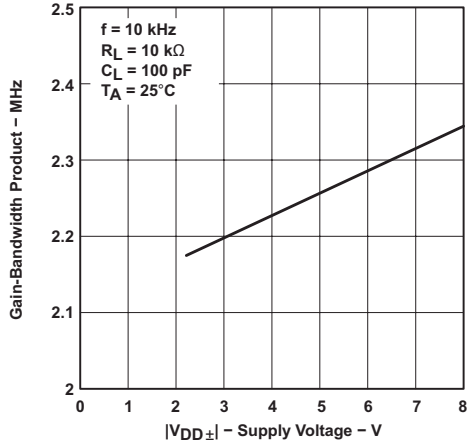


Figure 49. Gain-Bandwidth Product vs Supply Voltage

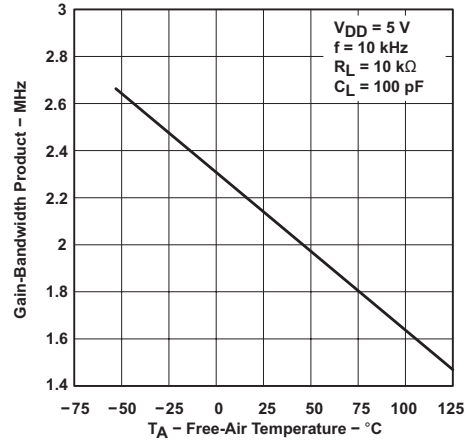


Figure 50. Gain-Bandwidth Product vs Ambient Temperature

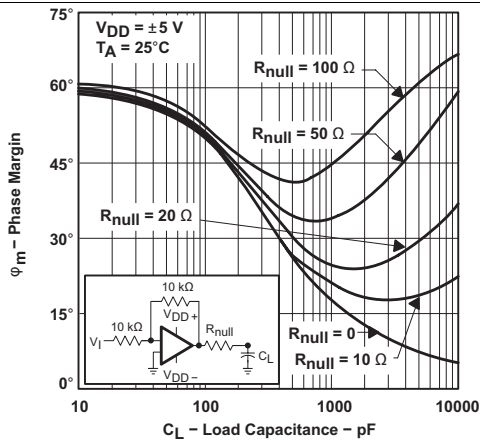


Figure 51. Phase Margin vs Load Capacitance

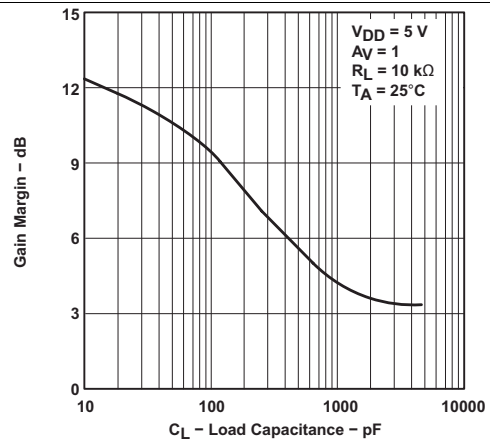


Figure 52. Gain Margin vs Load Capacitance

8 Detailed Description

8.1 Overview

The TLC2274M-MIL device is a rail-to-rail output operational amplifier. The device operates from a 4.4-V to 16-V single supply or ± 2.2 -V to ± 8 -V dual supply, is unity-gain stable, and is suitable for a wide range of general-purpose applications.

8.2 Functional Block Diagram

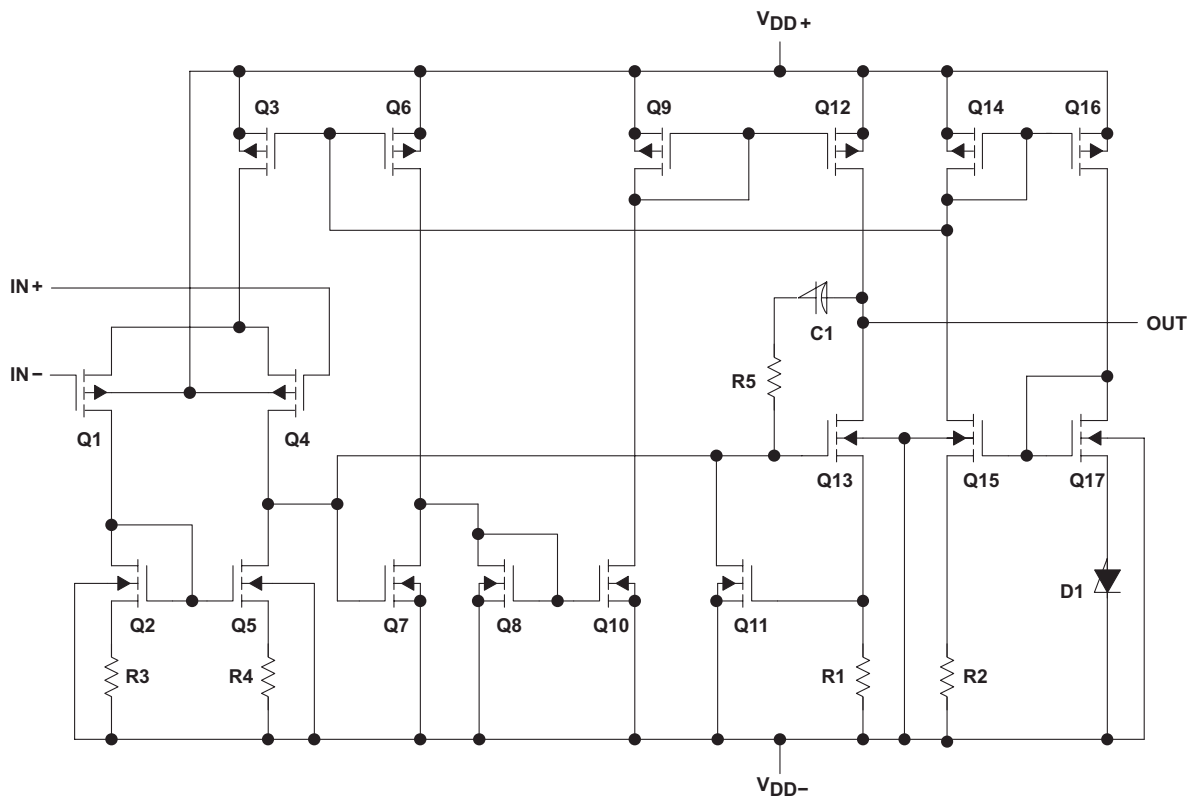


Table 2. Device Component Count⁽¹⁾

COMPONENT	COUNT
Transistors	76
Resistors	52
Diodes	18
Capacitors	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

8.3 Feature Description

The TLC2274M-MIL device features 2-MHz bandwidth and voltage noise of $9 \text{ nV}/\sqrt{\text{Hz}}$ with performance rated from 4.4 V to 16 V across a temperature range (-55°C to 125°C). LinMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

8.4 Device Functional Modes

The TLC2274M-MIL device is powered on when the supply is connected. The device may operate with single or dual supply, depending on the application. The device is in its full-performance mode once the supply is above the recommended value.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts™, the model generation software used with MicroSim PSpice™. The Boyle macromodel ⁽¹⁾ and subcircuit in Figure 53 were generated using the TLC2274M-MIL typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

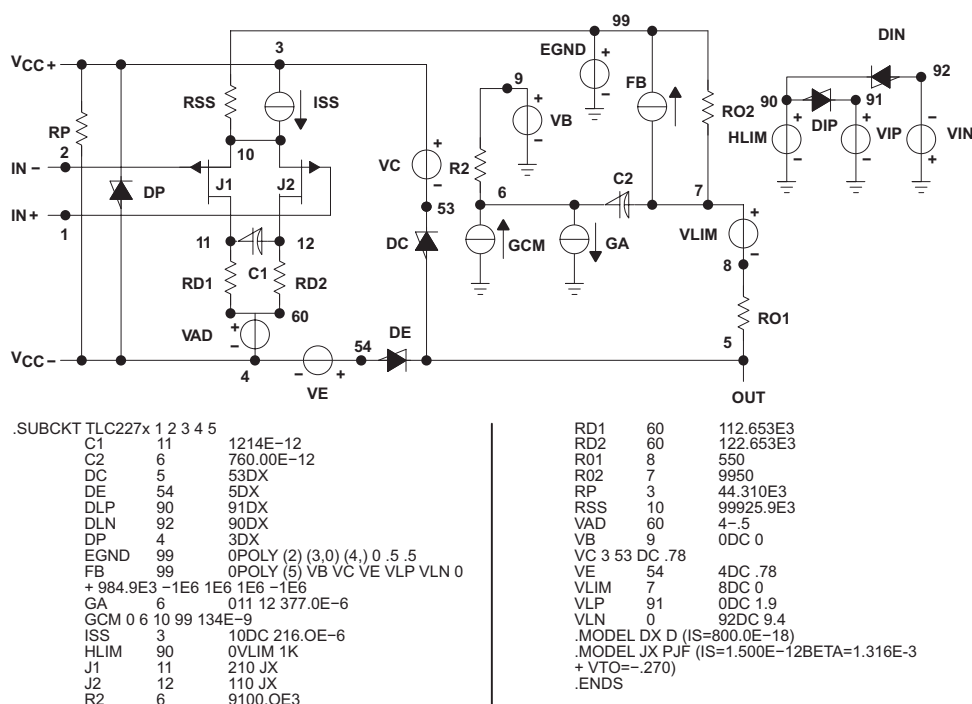


Figure 53. Boyle Macromodel and Subcircuit

(1) *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

9.2 Typical Application

9.2.1 High-Side Current Monitor

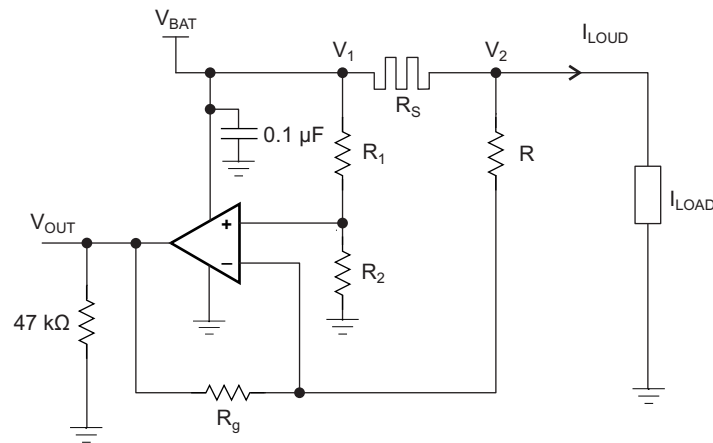


Figure 54. Equivalent Schematic (Each Amplifier)

9.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#) as the input parameters.

Table 3. Design Parameters

PARAMETER	VALUE
V_{BAT}	Battery voltage 12 V
R_{SENSE}	Sense resistor 0.1 Ω
I_{LOAD}	Load current 0 A to 10 A
Operational amplifier	Set in differential configuration with gain = 10

9.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

9.2.1.2.1 Differential Amplifier Equations

[Equation 1](#) and [Equation 2](#) are used to calculate V_{OUT} .

$$V_{OUT} = \frac{R_g}{R} \left(\frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times \frac{V_1 + V_2}{2} + \frac{1 + \frac{1}{2} \left(\frac{R_1}{R_2} + \frac{R}{R_g} \right)}{1 + \frac{R_1}{R_2}} (V_1 - V_2) \right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R} \left(\frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times V_{BAT} + \frac{1 + \frac{1}{2} \left(\frac{R_1}{R_2} + \frac{R}{R_g} \right)}{1 + \frac{R_1}{R_2}} \times R_S \times I_{LOAD} \right) \quad (2)$$

In an ideal case $R_1 = R$ and $R_2 = R_g$, and V_{OUT} can then be calculated using [Equation 3](#):

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \quad (3)$$

However, as the resistors have tolerances, they cannot be perfectly matched.

$$R_1 = R \pm \Delta R_1$$

$$R_2 = R_2 \pm \Delta R_2$$

$$R = R \pm \Delta R$$

$$R_g = R_g \pm \Delta R_g$$

$$\text{Tol} = \frac{\Delta R}{R} \tag{4}$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by [Equation 5](#).

$$V_{\text{OUT}} = \pm (4 \text{ Tol}) \frac{R_g}{R + R_g} \times V_{\text{BAT}} + \left(1 \pm 2 \text{ Tol} \left(1 + \frac{2R}{R + R_g} \right) \right) \frac{R_g}{R} \times R_S \times I_{\text{LOAD}}$$

where

- Tol = 0.01 for 1%
 - Tol = 0.001 for 0.1%
- (5)

If the resistors are perfectly matched, then Tol = 0 and V_{OUT} is calculated using [Equation 6](#).

$$V_{\text{OUT}} = \frac{R_g}{R} \times R_S \times I_{\text{LOAD}} \tag{6}$$

The highest error is from the common mode, as shown in [Equation 7](#).

$$4 (\text{Tol}) \frac{R_g}{R + R_g} \times V_{\text{BAT}} \tag{7}$$

Gain of 10, $R_g / R = 10$, and Tol = 1%:

$$\text{Common mode error} = ((4 \times 0.01) / 1.1) \times 12 \text{ V} = 0.436 \text{ V}$$

Gain of 10 and Tol = 0.1%:

$$\text{Common mode error} = 43.6 \text{ mV}$$

The resistors were chosen from 2% batches.

$$R_1 \text{ and } R \text{ 12 k}\Omega$$

$$R_2 \text{ and } R_g \text{ 120 k}\Omega$$

$$\text{Ideal Gain} = 120 / 12 = 10$$

The measured value of the resistors:

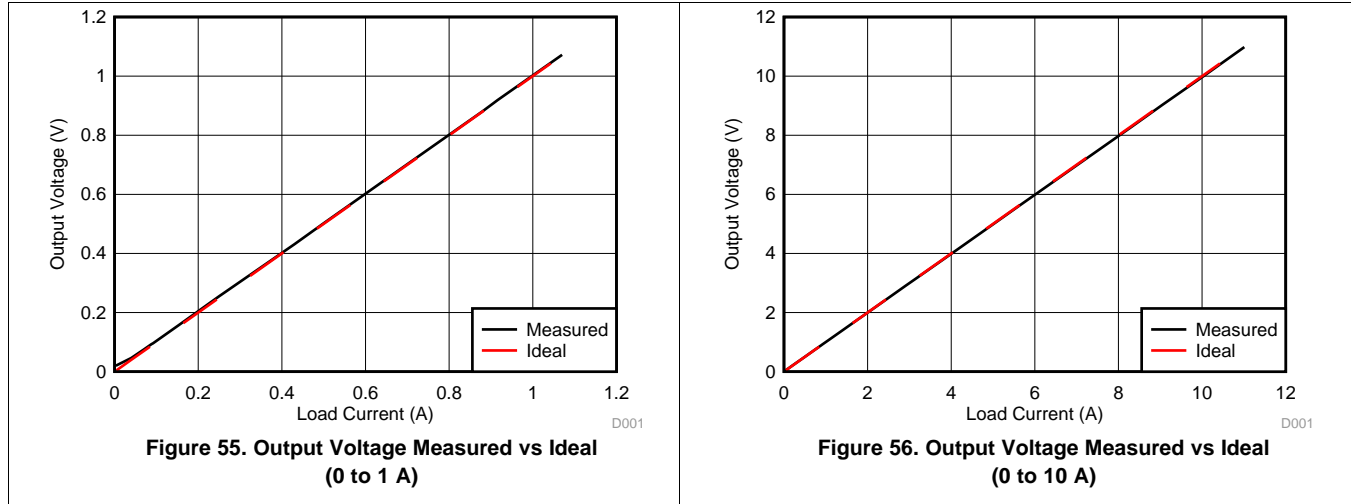
$$R_1 = 11.835 \text{ k}\Omega$$

$$R = 11.85 \text{ k}\Omega$$

$$R_2 = 117.92 \text{ k}\Omega$$

$$R_g = 118.07 \text{ k}\Omega$$

9.2.1.3 Application Curves



10 Power Supply Recommendations

Supply voltage for a single supply is from 4.4 V to 16 V, and from ± 2.2 V to ± 8 V for a dual supply. In the high-side sensing application, the supply is connected to a 12-V battery.

11 Layout

11.1 Layout Guidelines

The TLC2274M-MIL device is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1- μ F bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

11.2 Layout Example

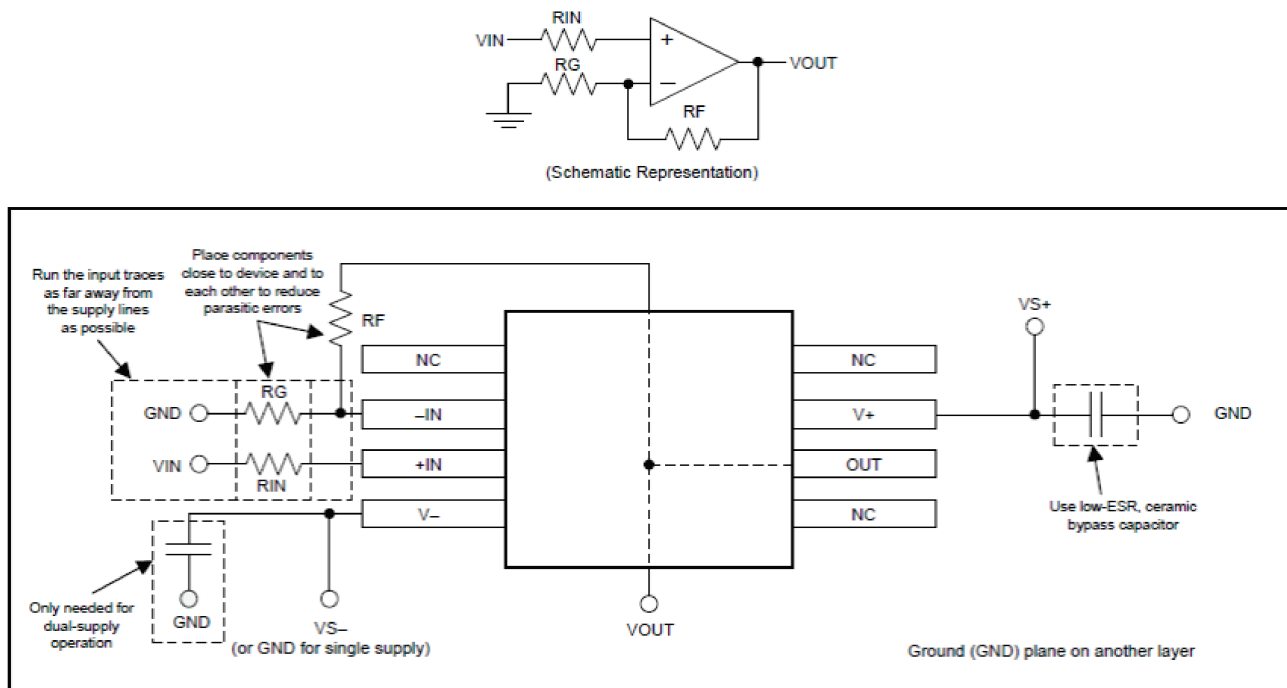


Figure 57. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.3 商標

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12.4 静電気放電に関する注意事項



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12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9318201M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9318201M2A TLC2274 MFKB	Samples
5962-9318201MCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318201MC A TLC2274MJB	Samples
5962-9318201QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318201QD A TLC2274MWB	Samples
TLC2274MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9318201M2A TLC2274 MFKB	Samples
TLC2274MJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TLC2274MJ	Samples
TLC2274MJB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318201MC A TLC2274MJB	Samples
TLC2274MWB	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318201QD A TLC2274MWB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

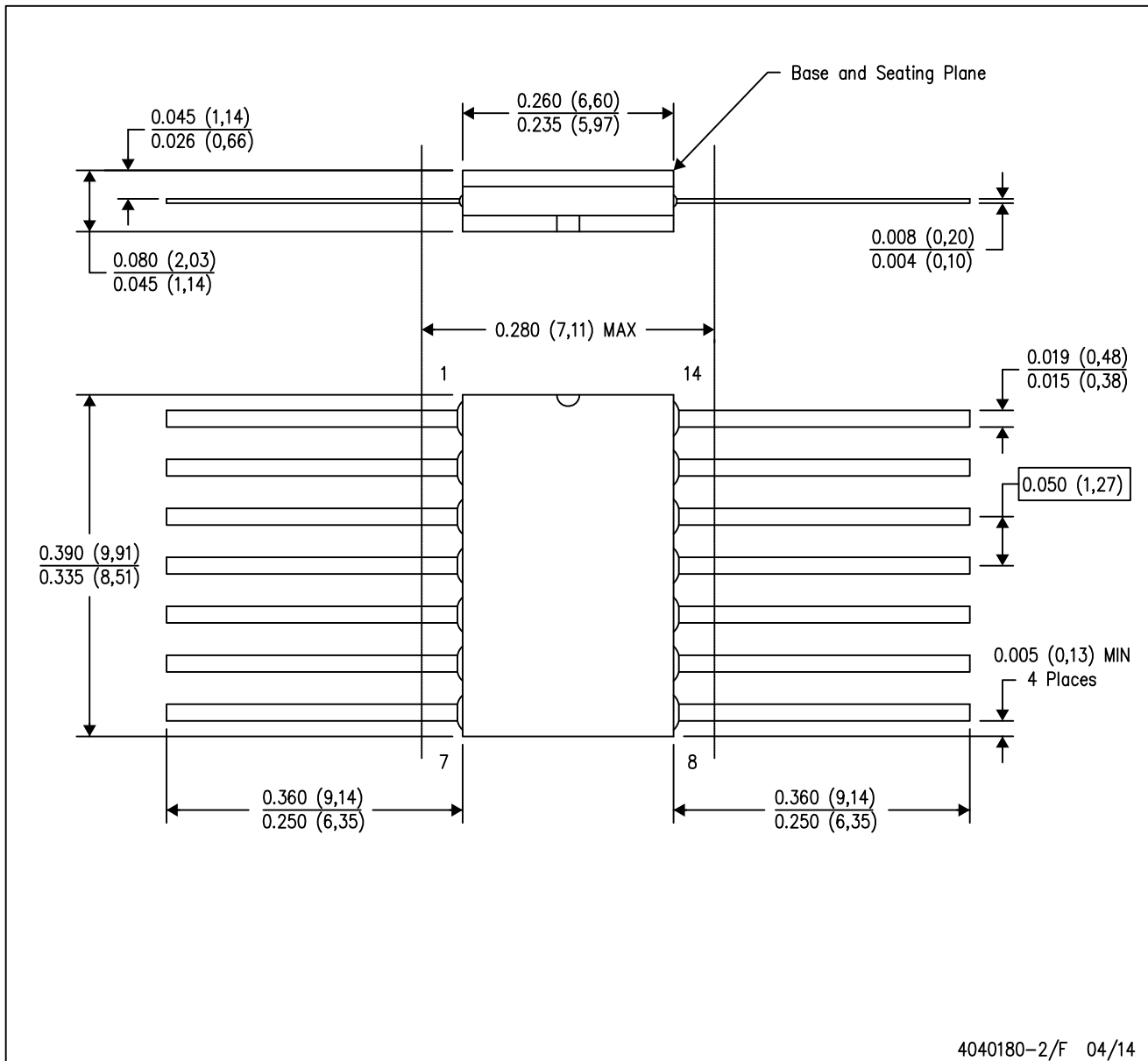
- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

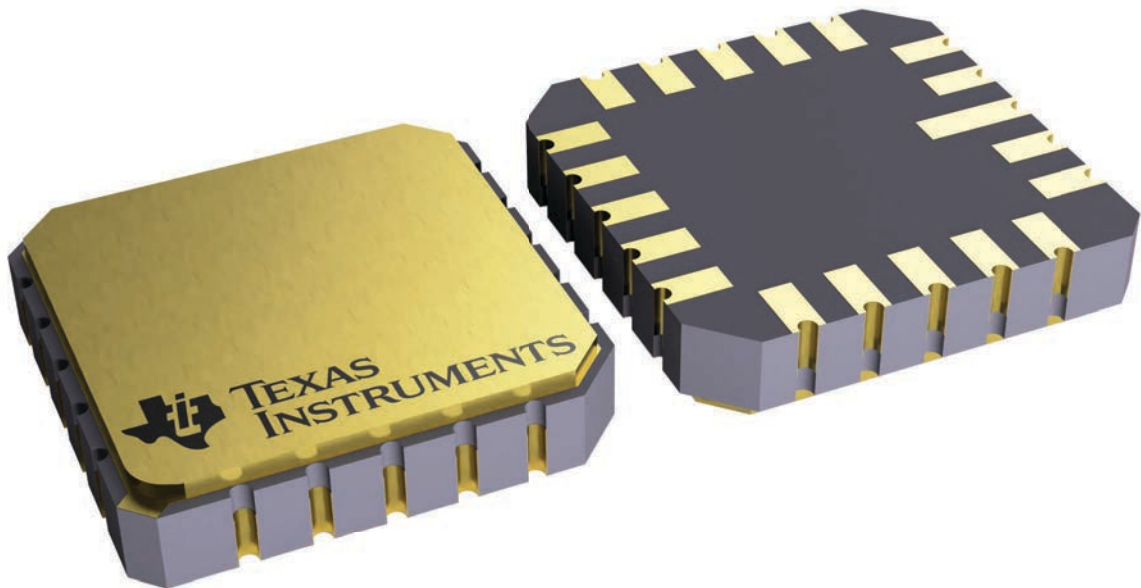
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

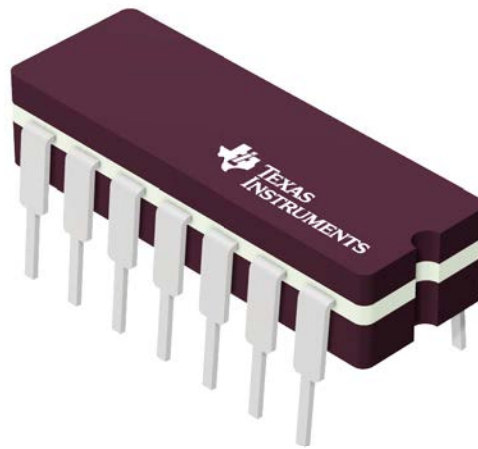
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

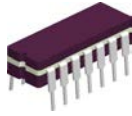
GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

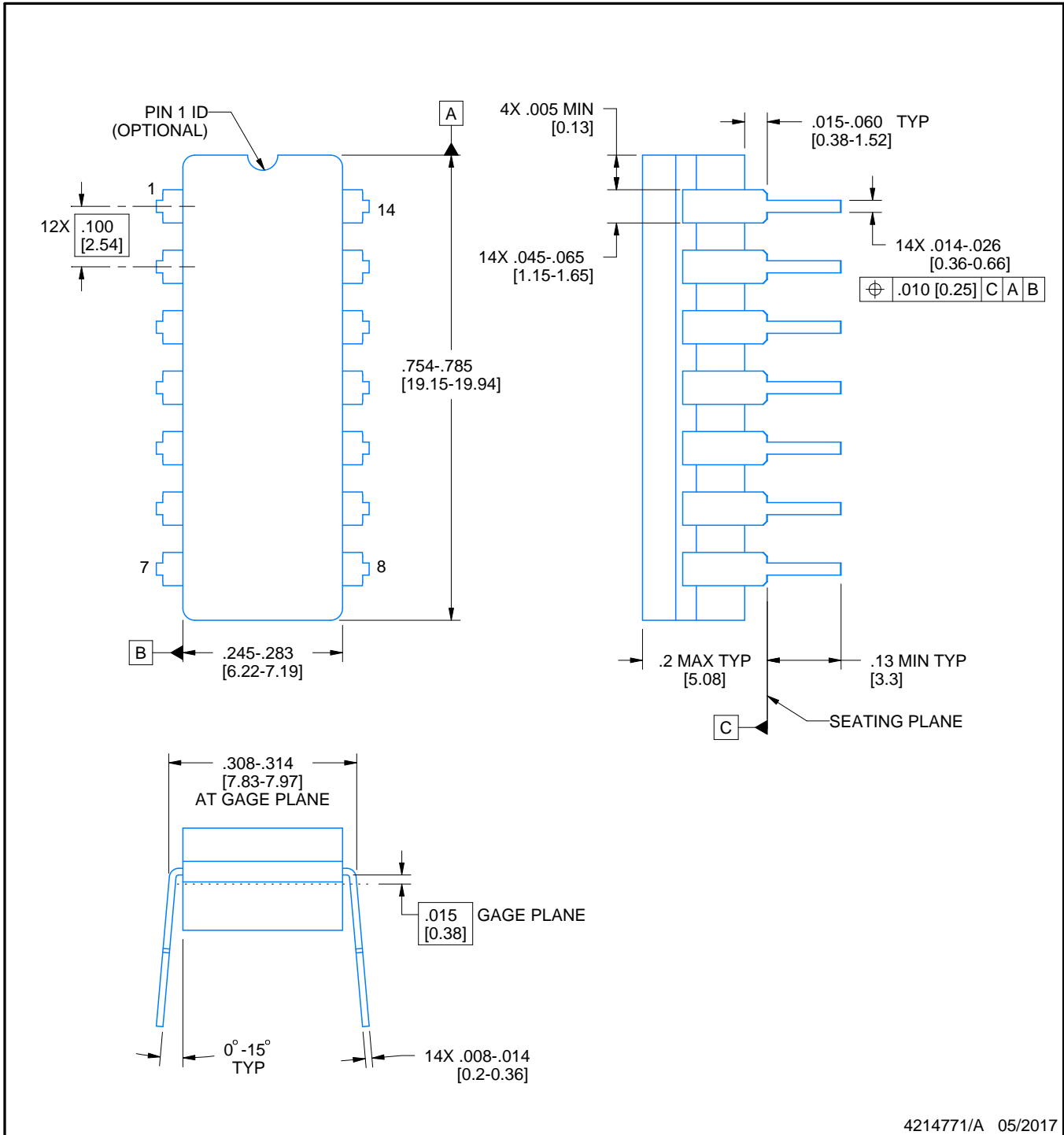
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

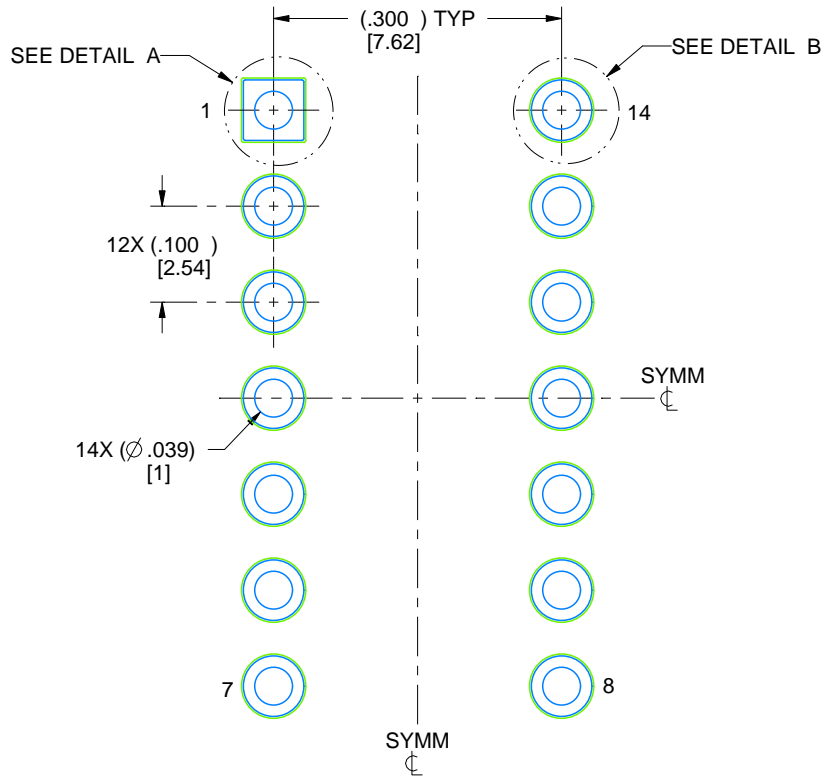
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

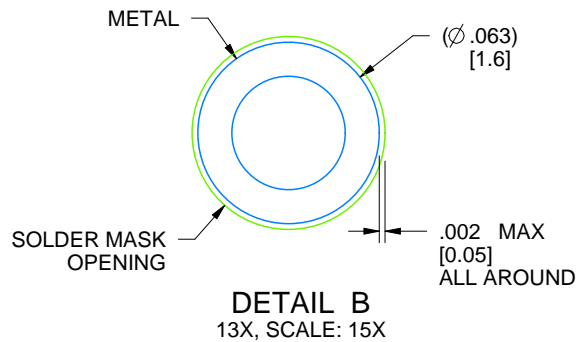
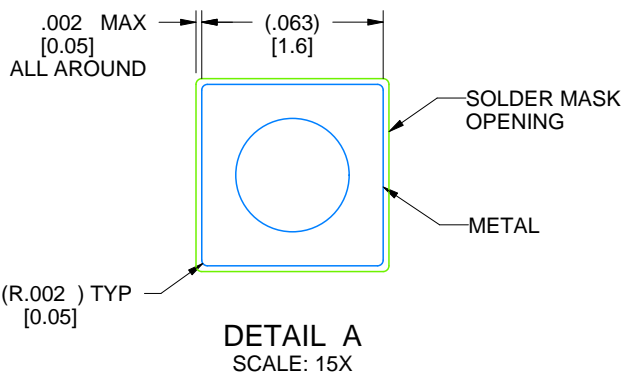
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

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