TLIN1431x-Q1 車載用 LIN SBC、ハイサイド・スイッチおよびウォッチドッグ内蔵

1 特長

- AEC-Q100 (グレード 1): 車載アプリケーション認定済み
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- LIN (Local Interconnect Network) 物理層仕様 (LIN 2.2A、ISO 17987–4:2016、SAE J2602:2021) に準拠
- ウォッチドッグ・スーパーバイザが内蔵され、ピンまたはシリアル・ペリフェラル・インターフェイス (SPI) により構成可能
- 12V アプリケーションをサポートする拡張機能
  - LIN バスのフォルト保護: ±58V
  - 12V 電源で 125mA をサポートする 3.3V (TLIN14313-Q1) または 5V (TLIN14315-Q1) LDO 出力
  - 10 ビット PWM またはタイマで制御された開放負荷および短絡検出機能を備えたハイサイド・スイッチ
  - ハイサイド・スイッチとして構成可能な LIMP ピン
  - 各種の入力スレッショルドまたは方法に対応した構成可能 WAKE ピン
  - スリープ・モード: 超低消費電流で、次のウェイクアップ・イベントに対応
    - LIN バス
    - WAKE 経由のローカル・ウェイクアップ
      - 周期的および静的センシング
- 保護機能
  - ESD 保護
  - V_{SUP} と V_{CC} の低電圧保護
  - TXD ドミナント・タイムアウト (DTO) 保護
  - サーマル・シャットダウン保護機能
- バッテリ電圧モニタ内蔵
- 自動光学検査 (AOI) に適したリードレス QFN (20) パッケージで供給

2 アプリケーション

- ボディ・エレクトロニクス / 照明
- ハイブリッド、電動、パワートレイン・システム
- インフォテインメントとクラスタ
- 家電製品

3 概要

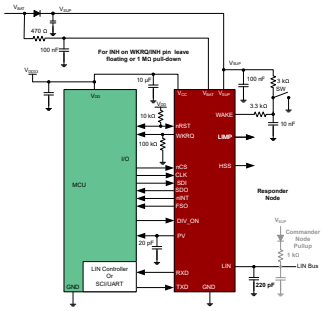
TLIN1431x-Q1 は、ウォッチドッグ、ハイサイド・スイッチ、リンプ・ホーム機能、詳細な設定が可能な WAKE 入力ピンを統合した LIN (Local Interconnect Network) システム・ベーシス・チップ (SBC)です。本デバイスは、制御方式 (ピンまたは シリアル・ペリフェラル・インターフェイス (SPI)) を起動時に自動的に決定します。いずれの制御方式でも、ウォッチドッグはデフォルトでウィンドウ・ウォッチドッグに設定されていますが、柔軟性を高めるために、SPI 制御を使う場合には、20 種類を超える時間ウィンドウを持つウィンドウ・ウォッチドッグまたはタイムアウト・ウォッチドッグとして本デバイスを設定できます。

本 LIN トランシーバは、エンドオブライン・プログラミング用に 200kbps の高速モードを備えています。オンボード LED 用として、診断機能付きハイサイド・スイッチが用意されています。高度に設定可能な WAKE ピンは、周期的センシング用にハイサイド・スイッチと組み合わせて使えるため、ECU のスリープ電流を低減できます。WKRQ/INH ピンは、デジタル・ウェイク出力 (WKRQ) として、または VSUP に基づく禁止 (INH) 信号による外部電源用イネーブル・ピンとして構成できます。

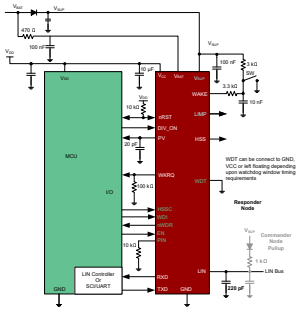
デバイス情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLIN1431x-Q1	VQFN (RGY)(20)	4.50mm x 3.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図、SPI 制御



概略回路図、ピン制御

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2022) to Revision A (December 2022)	Page
• データシートのステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

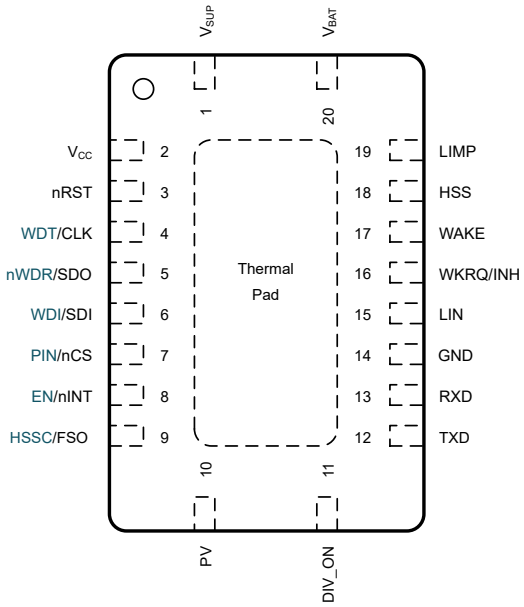


図 5-1. RGY Package, 20-Pin QFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
V_{SUP}	1	I	Device supply voltage (connected to battery in series with external reverse blocking diode)
V_{CC}	2	O	Output voltage from integrated voltage regulator
nRST	3	I/O	Reset input/output (active low)
WDT/CLK	4	I	Pin control: WDT - Programmable watchdog window set input (3 levels) SPI control: CLK - SPI clock input
nWDR/SDO	5	O	Pin control: nWDR - Watchdog failure output trigger SPI control: SDO - SPI serial data output
WDI/SDI	6	I	Pin control: WDI - Watchdog timer trigger input active on both rising and falling edges (Must be driven at all times) SPI control: SDI - SPI serial data input
PIN/nCS	7	I	Pin or SPI control selection pin at power up. Pin control: does not change SPI control: nCS - SPI chip select (active low)
EN/nINT	8	I/O	Pin control: EN - Device mode change input pin SPI control: nINT - Device interrupt output pin
HSSC/FSO	9	I/O	Pin control: HSSC - High side switch control input pin SPI control: FSO - Function output pin
PV	10	O	Internal V_{BAT} voltage divider output
DIV_ON	11	I	Input to turn on the internal V_{BAT} voltage divider, active high
TXD	12	I	TXD input interface to control state of LIN output
RXD	13	O	RXD output interface reporting state of LIN bus voltage
GND, Pad	14	—	Ground
LIN	15	I/O	LIN bus single-wire transmitter and receiver
WKRQ/INH	16	O	Digital output for wake or high voltage inhibit output depending upon state of pin at power up
WAKE	17	I	High voltage local wake up (LWU) pin
HSS	18	O	High side switch
LIMP	19	O	Used for LIMP home, watchdog event causes this pin to switch V_{SUP}
V_{BAT}	20	I	Supply voltage divider sense input (connected to battery)

6 Specifications

6.1 Absolute Maximum Ratings

Over recommended operating range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987)	–0.3	42	V
V_{BAT}	Battery sense input	–24	42	V
V_{LIN}	LIN Bus input voltage (ISO/DIS 17987)	–58	58	V
V_{CC50}	Regulated 5 V Output Supply	–0.3	6	V
V_{CC33}	Regulated 3.3 V Output Supply	–0.3	4.5	V
V_{WAKE}	WAKE pin input voltage range	–0.3	42	V
V_{HSS}	High side switch pin output voltage range	–0.3	42 and $V_O \le V_{SUP}+0.3$	V
V_{INH}	Inhibit pin output voltage range	–0.3	42 and $V_O \le V_{SUP}+0.3$	V
V_{LIMP}	LIMP pin output voltage range	–0.3	42 and $V_O \le V_{SUP}+0.3$	V
V_{nRST}	Reset output voltage	–0.3	V_{CC} + 0.3	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_O	Digital pin output current		8	mA
$I_{O(nRST)}$	Reset output current	–5	5	mA
T_J	Junction temperature	–40	160	°C
Storage temperature, T_{stg}	Storage temperature range	–65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level H2: V_{BAT}, V_{SUP}, LIN, and WAKE with respect to ground		±10000	V
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings, IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge per IEC 62228-2 (1)	Contact discharge (VSUP, WAKE, HSS, LIMP, LIN)	±8000	V
		Indirect ESD discharge (LIN)	±14000	
$V_{(ESD)}$	Powered electrostatic discharge SAE J2962-1(3)	Contact discharge	±8000	V
		Air discharge	±25000	
Transient	ISO 7637-2 and IEC 62215-3 Transients according to IBEE LIN EMC test spec(2)	Pulse 1	-100	V
		Pulse 2a	75	
		Pulse 3a	-150	
		Pulse 3b	100	

6.3 ESD Ratings, IEC Specification (continued)

			VALUE	UNIT
Transient	ISO 7637-3 Slow Transients Pulse (4)	Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	±30	V

(1) IEC 62228-2 ESD testing performed at third party. Different system-level configurations may lead to different results.
(2) ISO 7637-2 according to IEC 62228-2 are system-level transient tests. Different system-level configurations may lead to different results.
(3) SAE J2962-1 Testing performed at 3rd party US3 approved EMC test facility.
(4) ISO 7637-3 is a system-level transient test. Different system-level configurations may lead to different results.

6.4 Recommended Operating Conditions

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	5.5		28	V
V_{BAT}	Supply voltage	5.5		28	V
V_{LIN}	LIN bus input voltage	0		28	V
V_{LOGIC5}	Logic pin voltage	0		5.25	V
$V_{LOGIC33}$	Logic pin voltage	0		3.465	V
$I_{OH(DO)}$	Digital terminal HIGH level output current	-2			mA
$I_{OL(DO)}$	Digital terminal LOW level output current			2	mA
$I_{O(LIMP)}$	LIMP output current when configured as LIMP			1	mA
$I_{O(HSS)}$	High side switch output current; LIMP output current when configured as high side switch			100	mA
$I_{O(INH)}$	Inhibit output current			6	mA
$C_{(VSUP)}$	V_{SUP} supply capacitance	100			nF
$C_{(VCC)}$	V_{CC} supply capacitance; no load to full load	10			µF
ESR_{CO}	Output ESR capacitance requirements	0.001		2	Ω
Δt/ΔV	Input transition rise and fall rate (WDI, WDT, WDR)			100	ns/V
T_J	Operating junction temperature range	–40		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		TLIN1431x RGY 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Power Supply Characteristics

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
V_{BAT}	V_{BAT} sense pin voltage	470 Ω series resistor with 100nF cap to ground	5.5		28	V

6.6 Power Supply Characteristics (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BAT}	V_{BAT} sense pin current	470 Ω series resistor with 100nF cap to ground with DIV_ON high, V_{BAT} = 5.5 V to 28 V			220	µA
I_{BATREV}	V_{BAT} sense pin reverse current	470 Ω series resistor with 100nF cap to ground with DIV_ON high V_{BAT} = –24 V	–1			mA
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range	5.5		36	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10):	Normal(2) and Standby Modes	5.5		28	V
		Sleep Mode	5.5		28	V
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp Up	4.7		5.3	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp Down	4		4.6	V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.70		V
V_{nPORR}	V_{SUP} power on reset release rising threshold	Ramp Up	3.5		4.2	V
V_{nPORF}	V_{SUP} power on reset falling threshold	Ramp down	1.9		2.9	V
I_{SUP}	Transceiver and LDO supply current	Transceiver normal mode dominant plus LDO output; where LDO load current is 125 mA			135	mA
$I_{SUPTRXDOM}$	Supply current	Normal Mode: EN = V_{CC} (Pin control mode otherwise SPI enabled), bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF, LDO = no load		2.3	5.2	mA
		Standby Mode: EN = 0 V (Pin control mode otherwise SPI disabled), bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF, LDO = no load		1	1.9	mA
$I_{SUPTRXREC}$	Normal mode recessive supply current	Normal Mode: EN = V_{CC}, Bus recessive: LIN = V_{SUP}, LDO = no load		0.9	1.3	mA
$I_{SUPTRXREC}$	Standby mode recessive supply current	Standby Mode: EN = 0 V (Pin control mode otherwise SPI disabled), LIN = recessive = V_{SUP}, LDO = no load		210	350	µA
$I_{SUPTRXSLP}$	Sleep mode supply current	5.5 V < V_{SUP} ≤ 14 V, LIN = V_{SUP}, WAKE = GND, EN = 0 V (Pin control mode otherwise SPI disabled), TXD and RXD floating, LDO = no load		20	32	µA
		14 V < V_{SUP} ≤ 28 V, LIN = V_{SUP}, WAKE = $_{GND}$, EN = 0 V (Pin control mode otherwise SPI disabled), TXD and RXD floating, LDO = no load		25	36	µA
I_{SUPHSS}	High side switch current - no load	Additional standby mode current from high side switch, no load.			110	µA
$I_{SUPWKRQ\_INH}$	WKRQ/INH current due to pull-down	Additional standby mode current due to the pull-down resister on the WKRQ/INH pin to determine pin function, 100 kΩ for WKRQ or 1 MΩ for INH.			95	µA
Regulated Output V_{CC}						
V_{CC}	Regulated output	V_{SUP} = 5.5 to 28 V, I_{CC} = 1 to 125 mA	-2.5		2.5	%
$\Delta V_{CC(\Delta VSUP)}$	Line regulation	V_{SUP} = 5.5 to 28 V, ΔV_{CC}, I_{CC} = 10 mA			50	mV
$\Delta V_{CC(\Delta VSUPL)}$	Load regulation	I_{CC} = 1 to 125 mA, V_{SUP} = 14 V, ΔV_{CC}			50	mV
V_{DROP1}	Dropout voltage (5 V LDO output)	V_{SUP} – V_{CC}, I_{CC} = 15 mA		100	150	mV
V_{DROP2}	Dropout voltage (5 V LDO output)	V_{SUP} – V_{CC}, I_{CC} = 125 mA		550	650	mV
V_{SC}	V_{CC} short circuit threshold to enter sleep mode	V_{SUP} ≥ V_{POR}		2	2.5	V
UV_{CC5R}	Under voltage 5 V V_{CC} threshold	Ramp Up		4.7	4.9	V
UV_{CC5F}	Under voltage 5 V V_{CC} threshold	Ramp Down	4.1	4.45		V
UV_{CC33R}	Under voltage 3.3 V V_{CC} threshold	Ramp Up		2.9	3.1	V
UV_{CC33F}	Under voltage 3.3 V V_{CC} threshold	Ramp Down	2.5	2.75		V

6.6 Power Supply Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OV_{CC5R}	Over voltage 5 V VCC threshold (1)	Ramp Up		5.6	6.0	V
OV_{CC5F}	Over voltage 5 V VCC threshold (1)	Ramp Down	5.28	5.5		V
OV_{CC33R}	Over voltage 3.3 V VCC threshold (1)	Ramp Up		3.79	3.98	V
OV_{CC33F}	Over voltage 3.3 V VCC threshold (1)	Ramp Down	3.58	3.73		V
I_{CCOUT}	Output current	V_{CC} in regulation with 14V V_{SUP}	1		125	mA
I_{CCOUTL}	Output current limit	V_{CC} short to ground			275	mA
PSRR	Power supply rejection ripple rejection (1)	V_{RIP} = 0.5 V_{PP}, Load = 10 mA, f = 100 Hz, CO = 10 µF, V_{SUP} = 12 V and ambient temperature = 27 °C		60		dB
T_{SDR}	Thermal shutdown temperature (1)	Internal junction temperature; rising	160		185	°C
T_{SDF}	Thermal shutdown temperature (1)	Internal junction temperature; falling	150		170	°C
T_{SDHYS}	Thermal shutdown hysteresis (1)	V_{SUP} = 12 V		15		°C

(1) Specified by design
(2) Normal Mode: Ramp VSUP while LIN signal is a 10 kHz square wave with 50 % duty cycle and 18 V swing.

6.7 Electrical Characteristics

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OH}	High level output voltage	I_O = –2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
TXD Input Terminal						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{IH}	High level input leakage current	TXD = V_{IH}	–5	0	5	µA
R_{TXD}	Internal pull-up resistor value		125	350	800	kΩ
LIN Terminal (Referenced to V_{SUP})						
V_{OH}	HIGH level output voltage(5)	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 5.5 V to 28 V	0.85			V_{SUP}
V_{OL}	LOW level output voltage(5)	LIN dominant, TXD = low, V_{SUP} = 5.5 V to 28 V			0.2	V_{SUP}
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open V_{LIN} = 5.5 V to 45 V	–0.3		45	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 28 V, R_{MEAS} = 440 Ω, V_{SUP} = 28 V, V_{BUSdom} ≤ 0.251 * V_{SUP}	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0 V, V_{SUP} = 12 V Driver off/recessive	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} ≥ V_{SUP}, 5.5 V ≤ V_{SUP} ≤ 28 V Driver off			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = V_{SUP}, Driver off	–5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 12 V, 0 V ≤ V_{LIN} ≤ 28 V	–1		1	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 28 V, V_{SUP} = GND			10	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up); 図 7-2			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive; 図 7-2	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2; 図 7-2	0.475	0.5	0.525	V_{SUP}

6.7 Electrical Characteristics (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)(6)(7)	V_{HYS} = (V_{IL} - V_{IH}); 図 7-2			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R_{LIN}	Internal pull-up resistor to V_{SUP} on LIN (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 12 V, LIN = GND	–20		–2	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin	By design and characterization			25	pF
EN Input Terminal						
V_{IH}	High level input voltage		2		5.5	V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low level input current	EN = Low	–8		8	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIMP Output Terminal (High Voltage Open-drain Output)						
ΔV_H	Hi-level voltage drop for LIMP with respect to V_{SUP}	I_{LIMP} = –60 mA		0.42	1.2	V
R_{dson}	LIMP output drain-to-source on resistance	I_O = –60 mA		7	20	Ω
$I_{LKG(LIMP)}$	Leakage current	LIMP = 0 V, Sleep Mode	–1		1	µA
HSS, INH high voltage open drain output pin						
V_{DET_INH}	Voltage on INH/WKRQ pin during t_{DET_INH} time	VSUP = 14V			1.5	V
ΔV_{HINH}	Hi-level voltage drop for INH with respect to V_{SUP}	I_{INH} = –6 mA		0.5	1	V
ΔV_{HHSS}	Hi-level voltage drop for HSS with respect to V_{SUP}	I_{HSS} = –60 mA		0.42	1.2	V
R_{dson}	HSS output drain-to-source on resistance	I_O = –60 mA		7	17	Ω
$I_{O(HSS)}$	Output current support	VSUP = 14 V,		60	100	mA
$I_{OC(HSS)}$	HSS overcurrent limit	VSUP = 14 V	150		300	mA
$I_{OL(HSS)}$	HSS open load current	VSUP = 14 V	–2.5			mA
$I_{OLHYS(HSS)}$	HSS open load current hysteresis	VSUP = 14 V	0.05	0.45	1	mA
I_{lkg}	Leakage current	INH, HSS = 0 V, Sleep Mode	–1		1	µA
$t_{R/F}$	Output rise and fall times (HSS)	5.5 V ≤ V_{SUP} ≤ 28 V, I_{LOAD} = 60 mA, R_L = 220 Ω, 80%/20%	0.6		2.5	V/µs
t_{HSS_on}	Switching on delay (HSS) from SPI command to on	V_{SUP} = 14 V, I_{LOAD} = 60 mA, V_{OUT} = 80% of V_{SUP}			60	µs
t_{HSS_off}	Switching off delay (HSS) from SPI command to off	V_{SUP} = 14 V, I_{LOAD} = 60 mA, V_{OUT} = 20% of V_{SUP}			140	µs
t_{OCFLTR}	HSS overcurrent filter time(2)	V_{SUP} = 14 V		16		µs
t_{OLFLTR}	HSS open load filter time(2)	V_{SUP} = 14 V		64		µs
t_{OCOFF}	HSS overcurrent shut off time	$I_{O(HSS)}$ > $I_{OC(HSS)}$	200		300	µs
WAKE Input Terminal						
V_{IH}	High-level input voltage	Sleep or Standby Mode, WAKE pin enabled	4			V
V_{IL}	Low-level input voltage	Sleep or Standby Mode, WAKE pin enabled			2	V
I_{IL}	Low-level input leakage current	WAKE = 1 V		15	25	µA
t_{WAKE}	Wake up hold time from a wake edge on WAKE in standby or sleep mode for static sensing..	See 図 8-44 and 図 8-45	140			µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out in standby or sleep mode for static and cyclic sensing.	See 図 8-44 and 図 8-45			10	µs
WDI, SDI, CLK, nCS Input Terminal						
V_{IH}	High-level input voltage		2.19			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input leakage current	Inputs = V_{CC}	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{CC} = Active	–50			µA

6.7 Electrical Characteristics (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance	4 MHz		10	15	pF
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
R_{WDI_SDIpu}	Internal pull-up resistor on WDI/SDI pin		100	240	400	kΩ
R_{CLKpu}	Internal pull-up resistor on WDT/CLK pin	SPI control only for CLK	100	240	400	kΩ
R_{nCSpu}	Internal pull-up resistor on PIN/nCS pin	SPI control only for nCS	100	240	400	kΩ
WDT Input Terminal						
V_{IH}	High-level input voltage	Inputs = V_{CC}	0.8			V_{CC}
V_{IL}	Low-level input voltage	Inputs = V_{CC}			0.2	V_{CC}
$V_{IM(WDT)}$	WDT Mid-level input voltage(1)	Inputs = V_{CC}	0.4	0.5	0.6	V_{CC}
I_{IH}	High-level input leakage current	Inputs = V_{CC}	2.5		25	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{CC} = Active	–25		–2.5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–3		3	µA
SDO Output Terminal						
V_{OH}	High level output voltage	I_O = –2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
nRST Terminal; input/output reset (Open-drain)						
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, nRST = V_{CC}	–5		5	µA
V_{OL}	Low-level output voltage	Based upon external pull up to V_{CC}			0.2	V_{CC}
I_{OL}	Low-level output current, open drain	LIN = 0 V, nRST = 0.4 V	1.5			mA
$V_{th(sw)}$	Switching threshold voltage		0.25		0.75	V_{CC}
R_{PU}	Pull-up resistance		30	45	65	kΩ
nINT, nWDR, WKRQ Terminal						
V_{OH}	High level output voltage	I_O = –2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low-level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current (nINT and nWDR pins)	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
HSSC						
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{IL}	Low-level input current	V_{IN} = 0 V	–1		1	µA
R_{HSSC}	Pull-down resistor		150	350	800	kΩ
f_{SW}	Switching frequency	V_{HSS} = 14 V, $I_{O(HSS)}$ = 60 mA			400	Hz
WDI, WDT TIMING and SWITCHING CHARACTERISTIC (RL = 1 MΩ, CL = 50 pF and T_J = -40°C to 150°C)						
t_W	WDI pulse width; see 図 7-8	Filter time to avoid false input	30			µs
t_{WINDOW}	Closed Window + Open Window; See 図 7-8	WDT = GND	32	40	48	ms
		WDT = V_{CC}	480	600	720	ms
		WDT = Floating	4.8	6	7.2	s
DIV_ON						
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{IL}	Low-level input current	V_{DIV_ON} = 0 V	–1		1	µA
R_{DIV_ON}	Pull-down resistor		150	370	800	kΩ
PV						
Ratio	Divider ratio 5 V VCC	V_{BAT} = 5.5 V to 28 V		1:7		
Ratio	Divider ratio 3.3 V VCC	V_{BAT} = 5.5 V to 20 V		1:9		
ERR	Divider ratio error	V_{BAT} = 5.5 V to 28 V	–2		2	%
$V_{BATLIN5}$	Linear voltage range for V_{BAT} for 5 V LDO (3)	R_{LOAD} = 470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20%, 5.5 V ≤ V_{BAT} ≤ 28 V	0.735		4.05	V

6.7 Electrical Characteristics (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BATLIN3}$	Linear voltage range for V_{BAT} for 3.3 V LDO and when I/O is 3.3 V with 5 V LDO (4)	R_{LOAD} = 470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20%, 5.5 V ≤ V_{BAT} ≤ 20 V	0.561		2.27	V
V_{MAX5V}	Maximum V_{PVOUT}	28 V < V_{BAT} ≤ 42 V, 470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20%			5.1	V
$V_{MAX3.3V}$	Maximum V_{PVOUT} for 3.3 V LDO and when I/O is 3.3 V with 5 V LDO	20 V < V_{BAT} ≤ 42 V, 470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20%			3.36	V
V_{VCC5V_VIO3V}	Voltage when VCC = 5 V and I/O is at 3.3 V	R_{LOAD} = 470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20% and I/O voltage is ≤ 3.6 V			3.36	V
C_{PIN}	Pin capacitance			12		pF
t_{SET}	Settling time of the buffer	470 Ω ± 5% and C_{LOAD} = 10 nF ± 10%; When capacitive load only 20 pF ± 20%			50	µs
Duty Cycle Characteristics						
D1	Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery)(8) (9)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50/52 µs, D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 図 7-3, 図 7-4)	0.396			
D2	Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery)(8) (9)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7.6 V to 18 V, t_{BIT} = 50/52 µs, D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 図 7-3, 図 7-4)			0.581	
D3	Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery)(8) (9)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7.0 V to 18 V, t_{BIT} = 96 µs, D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See 図 7-3, 図 7-4)	0.417			
D4	Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery)(8) (9)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 7.6 V to 18 V, t_{BIT} = 96 µs, D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 図 7-3, 図 7-4)			0.59	
$D1_{LB}$	Duty Cycle 1 J2602 Low battery(9) (10)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 50/52 µs, D1 = $t_{BUS\_rec(min)/(2\ x\ tBIT)}$ (See 図 7-3, 図 7-4)	0.396			
$D2_{LB}$	Duty Cycle 2 J2602 Lowl battery(9) (10)	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 6.1 V to 7.6 V, t_{BIT} = 50/52 µs, D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 図 7-3, 図 7-4)			0.581	
$D3_{LB}$	Duty Cycle 3 J2602 Low battery(9) (10)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs, D1 = $t_{BUS\_rec(min)/(2\ x\ tBIT)}$ (See 図 7-3, 図 7-4)	0.417			
$D4_{LB}$	Duty Cycle 4 J2602 Lowl battery(9) (10)	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 6.1 V to 7.6 V, t_{BIT} = 96 µs, D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See 図 7-3, 図 7-4)			0.59	

(1) This is the measured voltage at the WDT pin when left floating. The WDT pin should be connected directly to V_{CC}, GND or left floating.
(2) Specified by design
(3) $V_{BATLIN5}$ = [(1/7) * V_{BAT}] +/- 50 mV for the linear range of the PV buffer
(4) $V_{BATLIN3}$ = [(1/9) * V_{BAT}] +/- 50 mV for the linear range of the PV buffer
(5) SAE J2602 loads include: commander node: 5.5 nF; 4 kΩ and for a responder node: 5.5 nF; 875 Ω
(6) V_{HYS} is defined for both ISO 17987 and SAE J2602-1.
(7) V_{HYS} = (V_{th_rec} - V_{th_dom}) where V_{th_rec} and V_{th_dom} are the actual voltage values from V_{BUSrec} and V_{BUSdom}
(8) ISO 17987 loads include 1 nF; 1 kΩ/ 6.8nF; 660 Ω/ 10 nF; 500 Ω; with t_{BIT} values of 50 µs and 96 µs
(9) SAE J2602 loads include: commander node: 5.5 nF; 4 kΩ/ 899 pF; 20 kΩ and for a responder node: 5.5 nF; 875 Ω/ 899 pF; 900 Ω; with t_{BIT} values of 52 µs and 96 µs

(10) ISO 17987 does not have a low battery specification. Using the ISO 17987 loads these low battery duty cycle parameters are covered for t_{BIT} values of 50 µs and 96 µs

6.8 AC Switching Characteristics

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See 図 7-3, 図 7-4)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See 図 7-3, 図 7-4)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See 図 7-6, 図 8-11 and 図 8-12	25	100	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See 図 8-12	10		60	µs
t_{TXD_DTO}	Dominant state time out		20	45	80	ms
t_{EN}	Enable pin deglitch time	Time enable pin state change before initiating mode change or sampling TXD pin	3		12	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin: See 図 7-5			100	µs
t_{DETECT}	Time to detect Pin vs SPI and I/O voltage level at power up(1)	Time from coming out of UV_{CC} and device determines these states			2	µs
t_{DET_INH}	Time to detect which output INH or WKRQ at power up	Time from coming out of UV_{CC} and device determines these states			25	µs
$t_{NOMINIT}$	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby mode to normal mode See 図 7-5			45	µs
t_{RSTN_act}	Time required for V_{CC} ≥ UV_{CC} to leave Restart mode	V_{CC} ≥ UV_{CC}	1.5	2	2.5	ms
t_{nRSTIN}	Input pulse required on the nRST pin to recognize a device reset.		120			µs
t_{NRST_TOG}	nRST pin output toggle high to low to high time	reg 29h[5] = 0 (Default value in SPI control. Value in pin control except for watchdog failure.)	1.5	2	2.5	ms
		reg 29h[5] = 1 (Value in pin control for watchdog failure.)	10	15	20	ms
t_{INITWD}	Initial long watchdog window time required to trigger first watchdog input trigger when entering Standby mode or Normal mode	WDI input trigger or SPI write command	150		200	ms
t_{INACT_FS}	Timer for inactivity coming out of sleep mode and when coming out of failsafe mode to determine if caused event has been cleared (1)	Default values and can be programmed to different values in SPI control.	4	5	6	min
t_{PWRUP}	Time from V_{SUP} exceeding UV_{SUP} until INH active	V_{CC} > UV_{CC}, INH = V_{SUP}, V_{CC} load of 50 mA @ 22 µF capacitance			3	ms
	Time from V_{SUP} exceeding UV_{SUP} and V_{CC} exceeding UV_{CC} until WKRQ active	V_{CC} > UV_{CC}, WKRQ = V_{CC}, V_{CC} load of 50 mA @ 22 µF capacitance			3	ms
t_{TOGGLE}	RXD pulse width when waking from sleep mode	register 'h12[2] = 1	5		15	µs
t_{UVFLTR}	Undervoltage detection delay time for V_{CC}		3		4	ms
t_{VSC}	Short to ground on VCC detection delay time		75	100	130	µs
t_{LDOON}	Time LDO is on to determine if a short circuit event is present after a previous uncleared detection		2		3	ms
$t_{MODE\_STBY\_NOM}$	Standby to normal mode change time based upon SPI write				70	µs
$t_{MODE\_NOM\_SLP}$	SPI write to go to sleep from normal	Time from SPI sleep command where LIN transceiver is off and RXD doesn't reflect the LIN bus			200	µs

6.8 AC Switching Characteristics (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode				70	µs
t_{WKRQ_SLP}	Time WKRQ turns on after a wake event when device is in sleep mode	Dependent upon LDO turning on and ramp time. Time provided is based upon 1 µs ramp and LDO being at 2 V.	450			µs
t_{INH_SLP}	Time INH turns on after a wake event when device is in sleep mode				210	µs
$t_{INH\_NOM\_SLP}$	SPI write to go to sleep from normal mode and INH turns off				70	µs
$t_{WK\_WIDTH\_MIN}$	Minimum WAKE pin pulse width (SPI mode only) (2) (3) (4)	Minimum WAKE Pin pulse width Register 8'h11[3:2] = 00b; See 図 8-46	10			ms
		Minimum WAKE Pin pulse width Register 8'h11[3:2] = 01b; See 図 8-46	20			ms
		Minimum WAKE Pin pulse width Register 8'h11[3:2] = 10b; See 図 8-46	40			ms
		Minimum WAKE Pin pulse width Register 8'h11[3:2] = 11b; See 図 8-46	80			ms
$t_{WK\_WIDTH\_INVALID}$	Maximum Pulse width that is considered invalid (SPI mode only) (2) (3)	Maximum WAKE Pin pulse width that is considered invalid Register 8'h11[3:2] = 00b; See 図 8-46			5	ms
		Maximum WAKE Pin pulse width that is considered invalid Register 8'h113:2] = 01b; See 図 8-46			10	ms
		Maximum WAKE Pin pulse width that is considered invalid Register 8'h11[3:2] = 10b; See 図 8-46			20	ms
		Maximum WAKE Pin pulse width that is considered invalid Register 8'h11[3:2] = 11b; See 図 8-46			40	ms
$t_{WK\_WIDTH\_MAX}$	Maximum WAKE pin pulse width to be considered valid (SPI mode only) (2)	Maximum WAKE Pin pulse window Register 8'h11[1:0] = 00b; See 図 8-46	750		950	ms
		Maximum WAKE Pin pulse window Register 8'h11[1:0] = 01b; See 図 8-46	1000		1250	ms
		Maximum WAKE Pin pulse window Register 8'h11[1:0] = 10b; See 図 8-46	1500		1875	ms
		Maximum WAKE Pin pulse window Register 8'h11[1:0] = 11b; See 図 8-46	2000		2500	ms
t_{WK_CYC}	Sampling window for cyclic sensing wake; Standby or Sleep mode; see 図 8-49	Register 8'h12[5] = 0	10	30	40	µs
		Register 8'h12[5] = 1	60	75	90	µs
Fast Mode						
DR	Data Rate	5.5 V ≤ V_{SUP} ≤ 18 V, R_{LIN} = 500 Ω and $C_{LIN(bus)}$ = 600 pF			200	kbps
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See 図 7-3, 図 7-4			5	µs
$t_{txr/f}$	LIN transmitter rise and fall time	5.5 V ≤ V_{SUP} ≤ 18 V, R_{LIN} = 500 Ω and $C_{LIN(bus)}$ = 600 pF, 80%/20%			1.5	µs
t_{FM_CHANGE}	Fast mode determination time for entering or leaving	Based upon EN and TXD voltage levels	70	90	110	µs
t_{FMTXD}	TXD pin pulse width to enter fast mode	Pulse must start after t_{EN} and finish before t_{FM_CHANGE}	5		25	µs
SPI Switching Characteristics						
f_{SCK}	SCK, SPI clock frequency (1)				4	MHz
t_{SCK}	SCK, SPI clock period (1)	See 図 7-7	250			ns
t_{RSCK}	SCK rise time (1)	See 図 7-7			40	ns
t_{FSCK}	SCK fall time (1)	See 図 7-7			40	ns
t_{SCKH}	SCK, SPI clock high (1)	See 図 7-7	125			ns
t_{SCKL}	SCK, SPI clock low (1)	See 図 7-7	125			ns

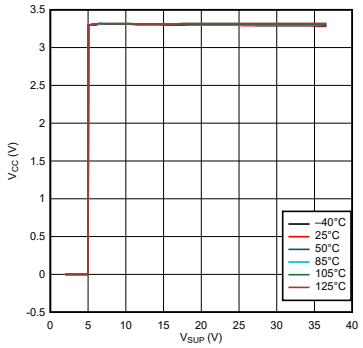
6.8 AC Switching Characteristics (continued)

parameters valid over –40℃ ≤ T_J ≤ 150 ℃ range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ACC}	First read access time from chip select (1)	See 図 7-7	50			ns
t_{CSS}	Chip select setup time (1)	See 図 7-7	100			ns
t_{CSH}	Chip select hold time (1)	See 図 7-7	100			ns
t_{CSD}	Chip select disable time (1)	See 図 7-7	50			ns
t_{SISU}	Data in setup time (1)	See 図 7-7	50			ns
t_{SIH}	Data in hold time (1)	See 図 7-7	50			ns
t_{SOV}	Data out valid (1)	See 図 7-7			80	ns
t_{RSO}	SO rise time (1)	See 図 7-7			40	ns
t_{FSO}	SO fall time (1)	See 図 7-7			40	ns

(1) Specified by design
(2) This parameter is valid only when register 11h[7:6] = 11b
(3) This is the minimum pulse width for a WAKE pin input that device will detect as a good pulse. Values between the min $t_{WK\_WIDTH\_MIN}$ and max $t_{WK\_WIDTH\_INVALID}$ is indeterminant and may or may not be considered valid.
(4) This parameter is set based upon the programmed value for $t_{WK\_WIDTH\_INVALID}$ register 11h[3:2]

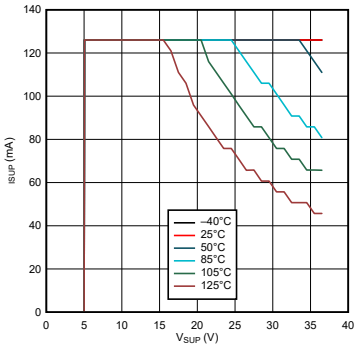
6.9 Typical Characteristics



V_{CC} = 3.3 V I_{CC} = 125 mA load Temperature = Ambient

Mode = Power up to Standby LIN = Recessive

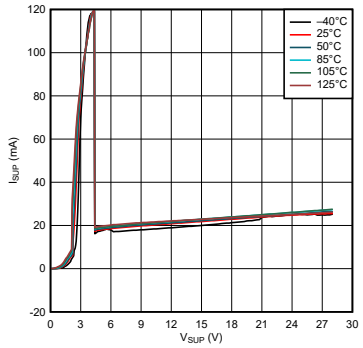
図 6-1. TLIN14313RGYQ1 V_{CC} versus V_{SUP} Ramping Up



V_{CC} = 3.3 V I_{CC} = 125 mA load Temperature = Ambient

Mode = Power up to Standby LIN = Recessive

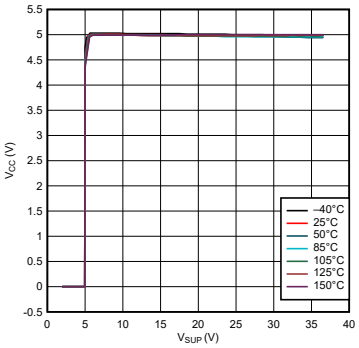
図 6-2. TLIN14313RGYQ1 I_{SUP} versus V_{SUP} Ramping Up



V_{CC} = Off I_{CC} = Off Temperature = Ambient

Mode = Sleep LIN = Recessive

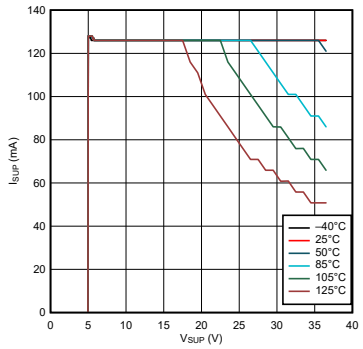
図 6-3. TLIN14313RGYQ1 I_{SUP} versus V_{SUP} Ramping Down



V_{CC} = 5 V I_{CC} = 125 mA load Temperature = Ambient

Mode = Power up to Standby LIN = Recessive

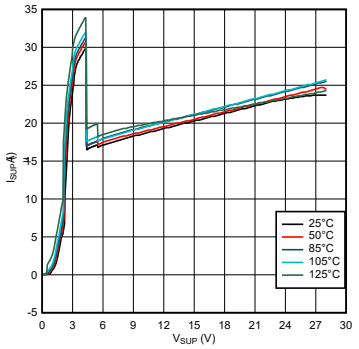
図 6-4. TLIN14315RGYQ1 V_{CC} versus V_{SUP} Ramping Up



V_{CC} = 5 V I_{CC} = 125 mA load Temperature = Ambient

Mode = Power up to Standby LIN = Recessive

図 6-5. TLIN14315RGYQ1 I_{SUP} versus V_{SUP} Ramping Up



V_{CC} = Off I_{CC} = Off Temperature = Ambient

Mode = Sleep LIN = Recessive

図 6-6. TLIN14315RGYQ1 I_{SUP} versus V_{SUP} Ramping Down

7 Parameter Measurement Information

7.1 Test Circuit: Diagrams and Waveforms

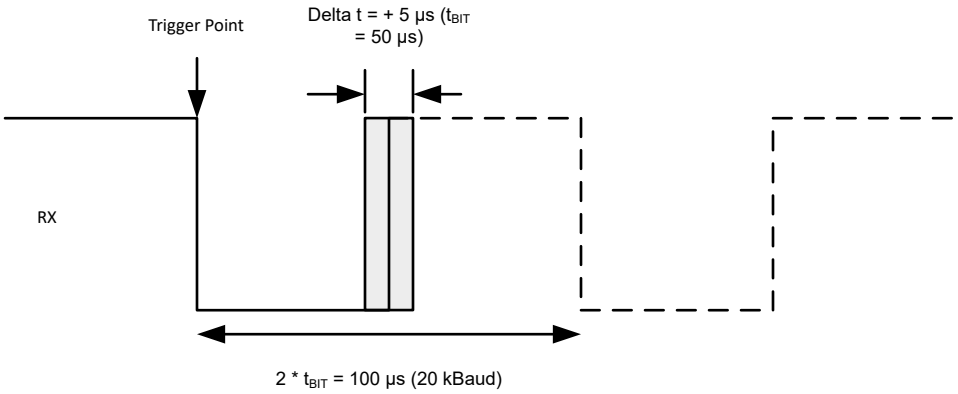


図 7-1. RX Response: Operating Voltage Range

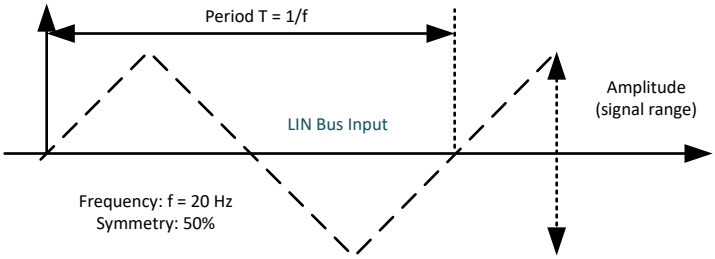


図 7-2. LIN Bus Input Signal

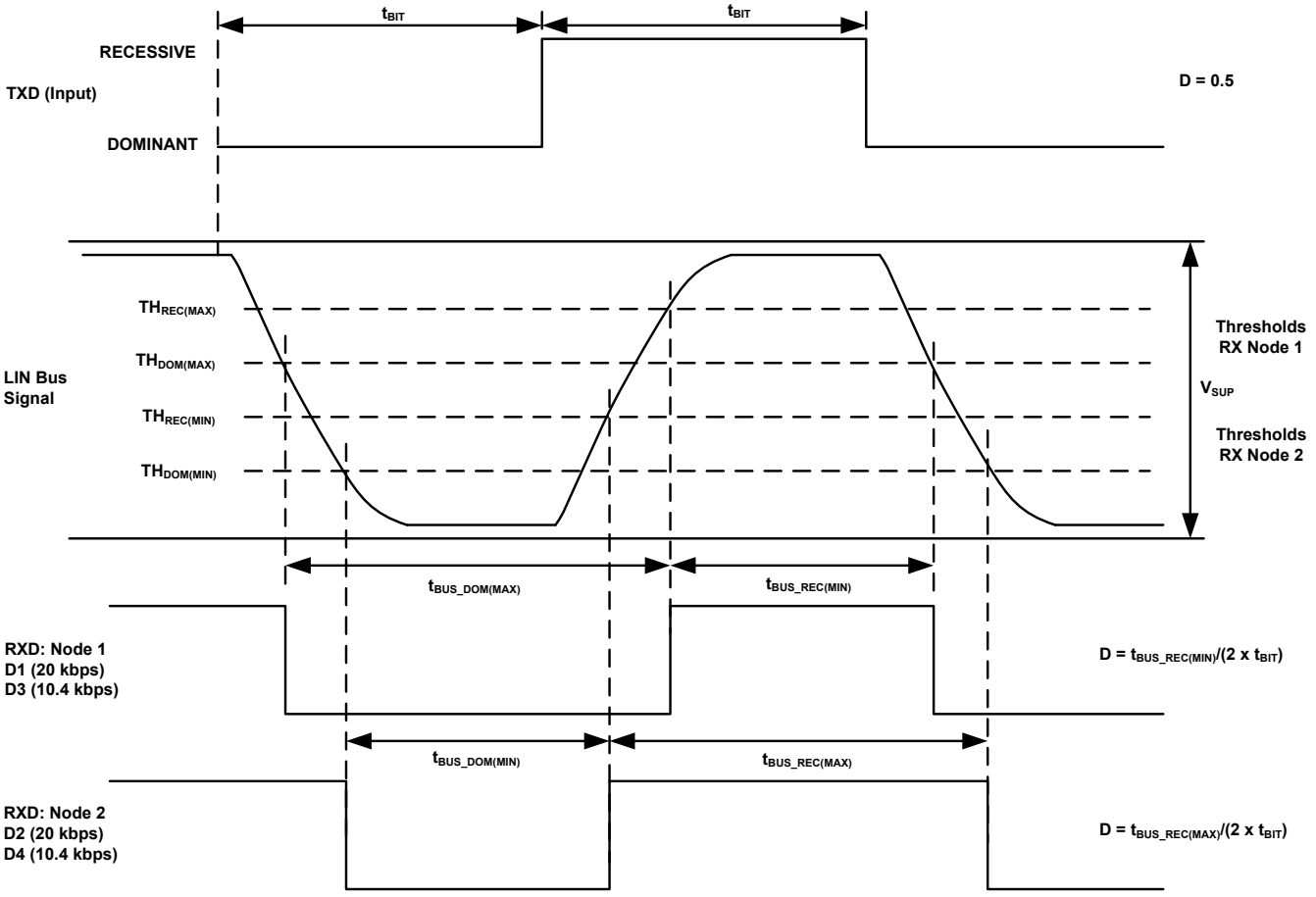


図 7-3. Definition of Bus Timing

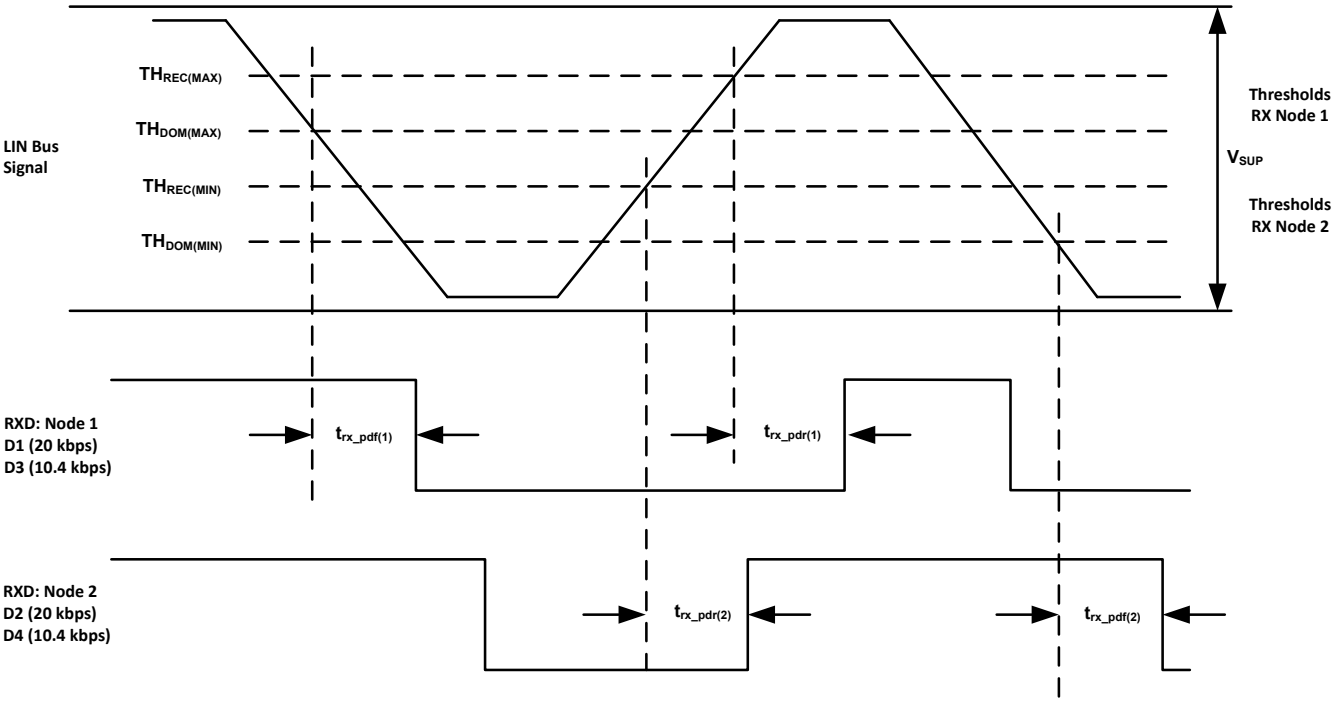


図 7-4. Propagation Delay

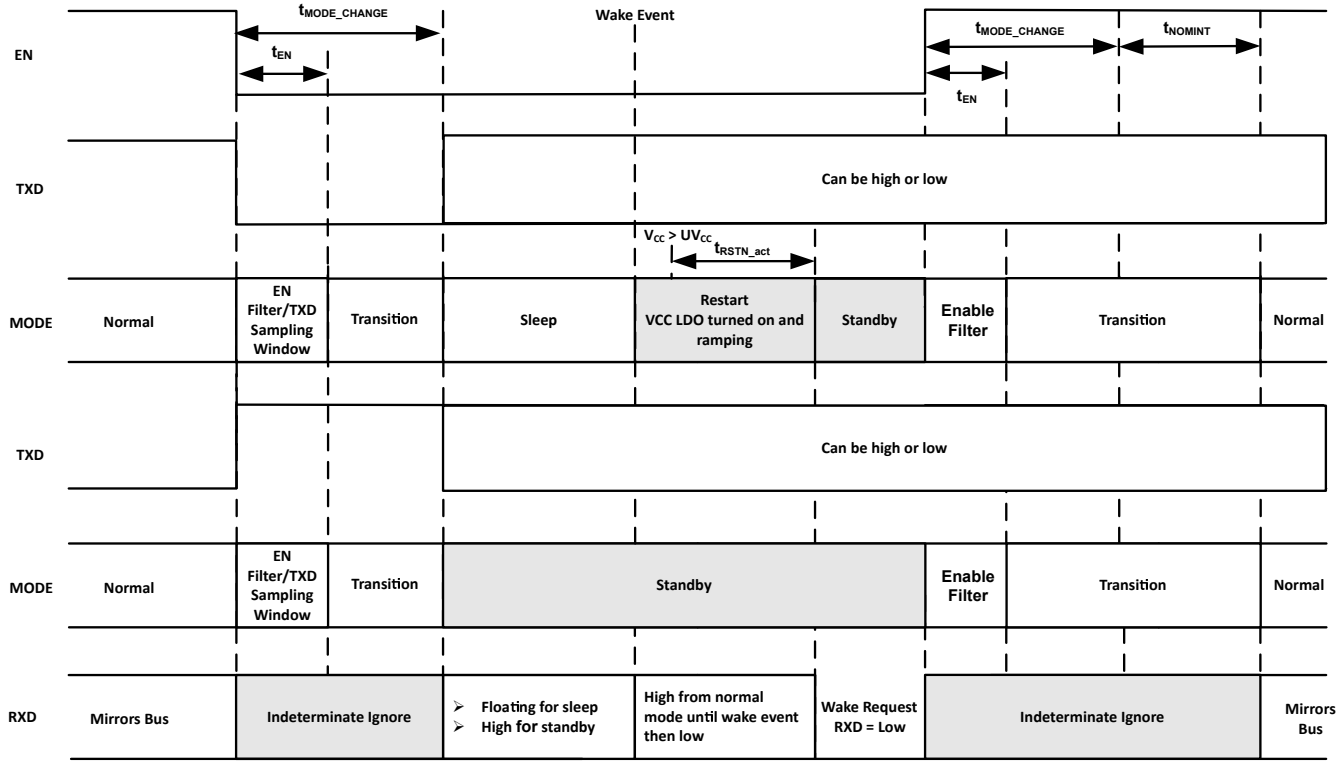


図 7-5. Mode Transitions (Pin Control)

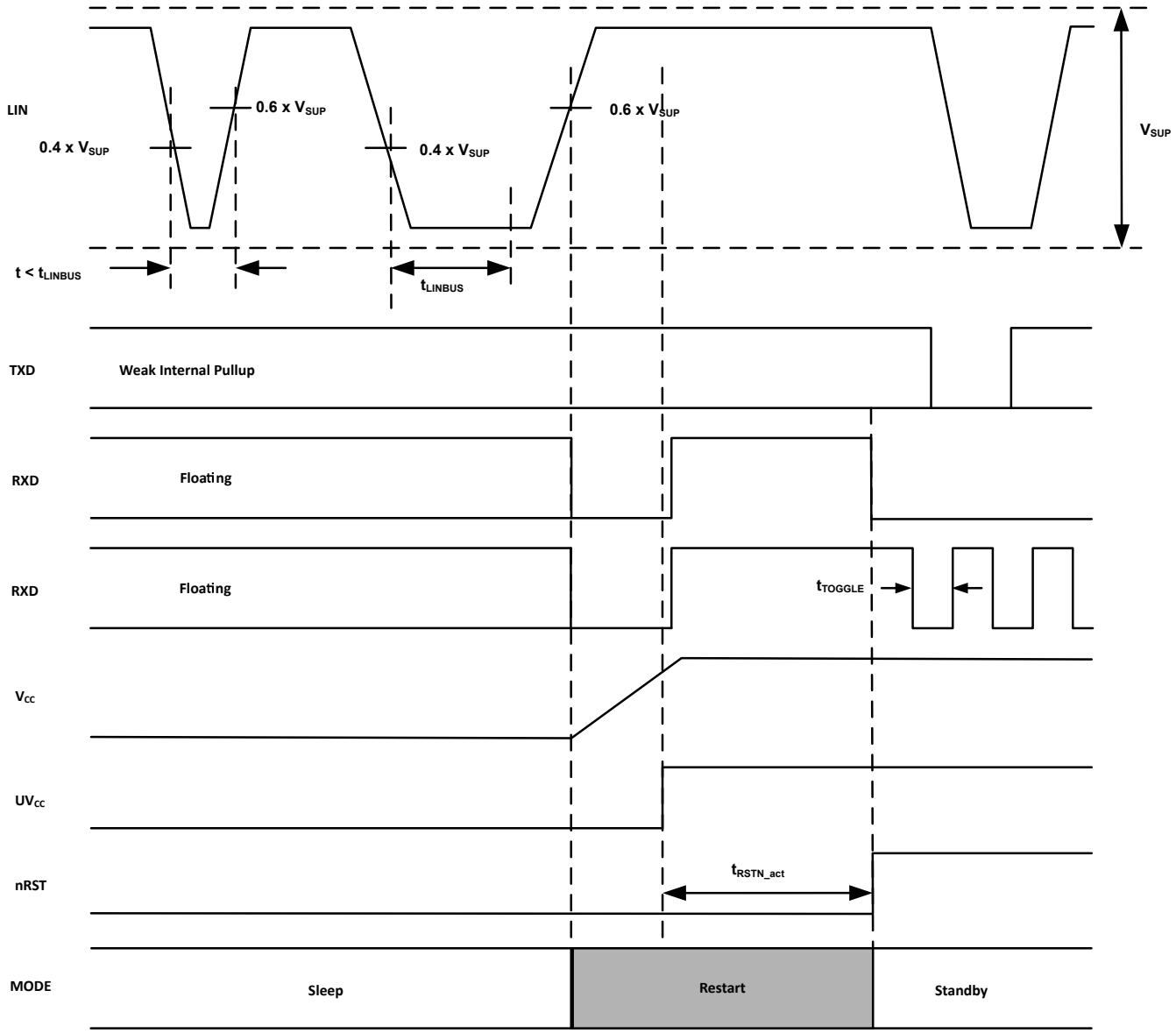


図 7-6. Wakeup through LIN

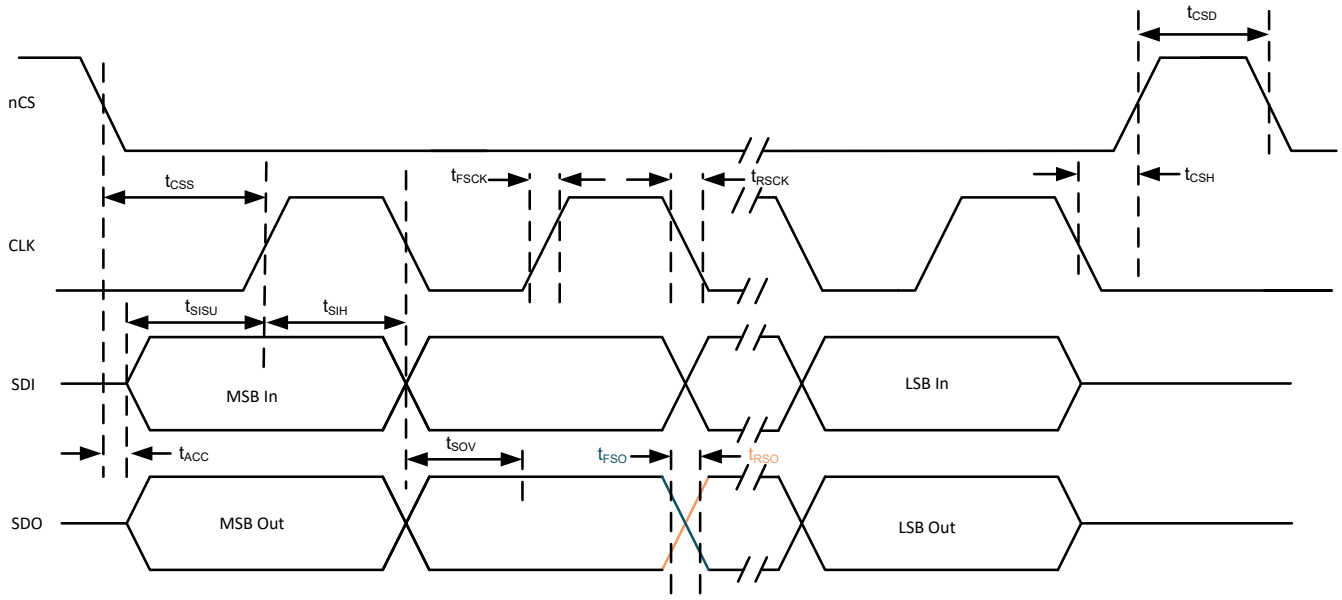


図 7-7. SPI AC Characteristic for Read and Write

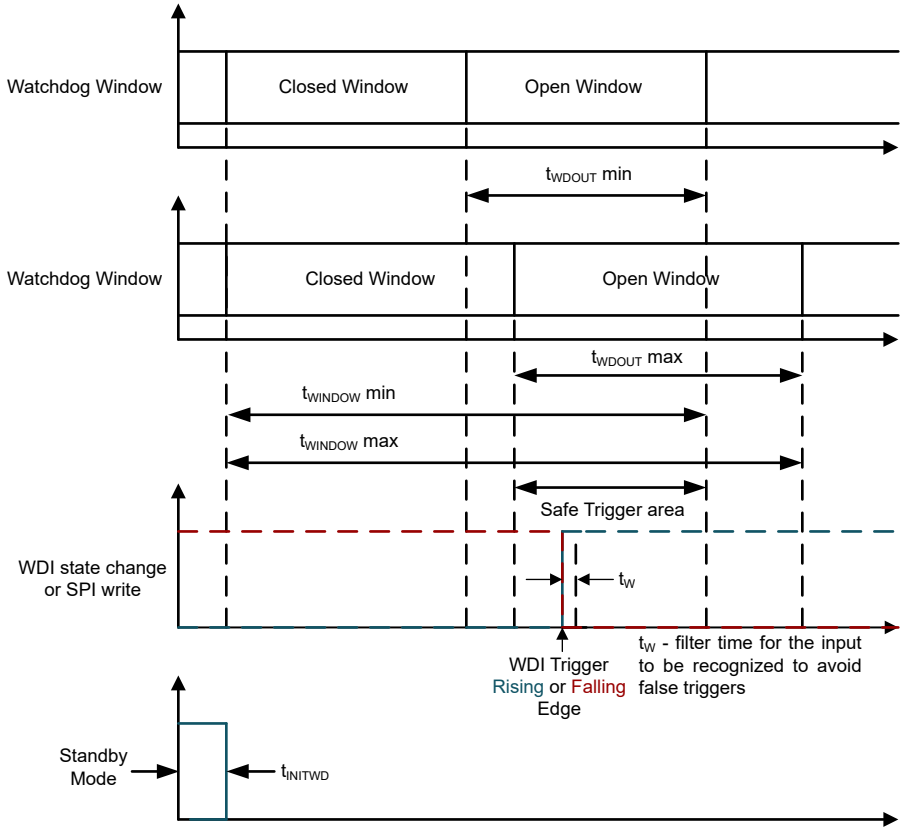


図 7-8. Watchdog Window Timing Diagram

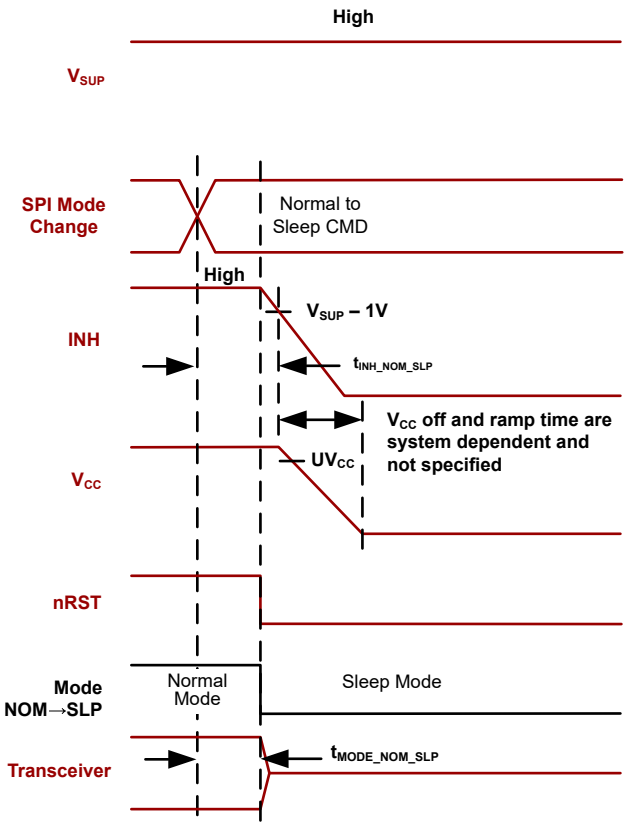


図 7-9. Normal to Sleep via SPI

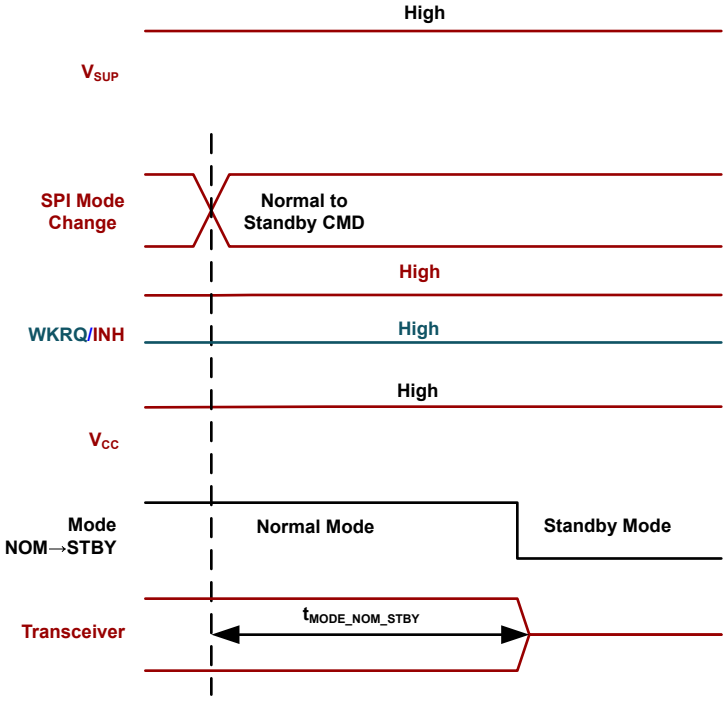


図 7-10. Normal to Standby via SPI

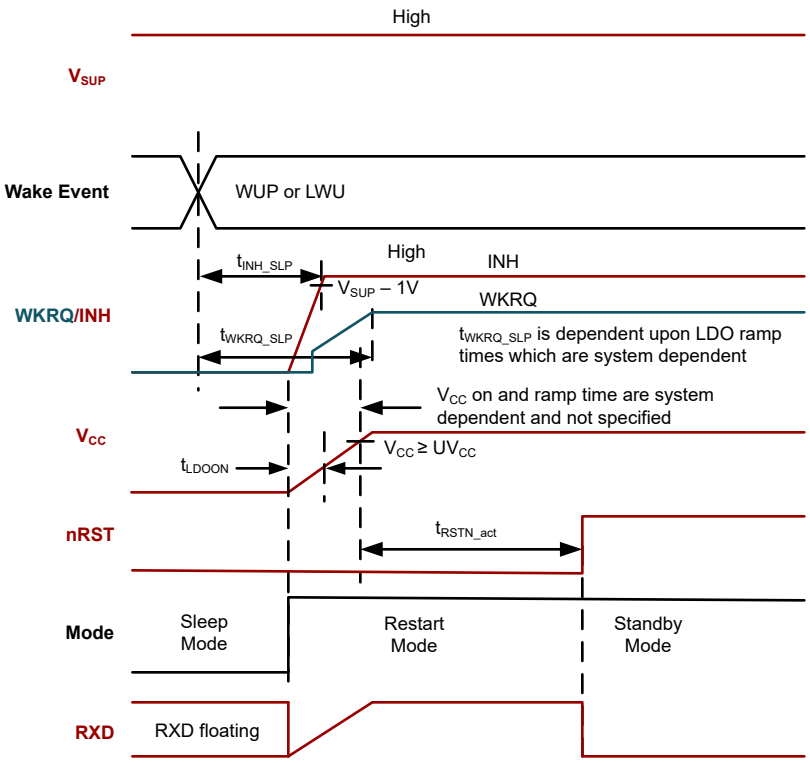


図 7-11. Sleep to Restart to Standby Mode from Wake Event

注

Throughout the document timing diagrams may have three colors associated to them.

- Red are signals on device pins
- Teal represent the WKRQ pin when configured as WKRQ
- Black will represent either internal signals or an external signal that will impact device behavior

8 Detailed Description

8.1 Overview

The TLIN1431x-Q1 LIN transceiver is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987–4:2016, and SAE J2602:2021 with integrated wake-up and protection features. The LIN bus is a single-wire, bi-directional bus that typically is used in low speed in-vehicle networks with data rates that range up to 20 kbps. The device LIN receiver works up to 100 kbps supporting in-line programming in normal mode. When the device is placed into fast mode, both the transmitter and receiver support up to 200 kbps. The device converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode.

Ultra-low current consumption is possible using the sleep mode. The TLIN1431x-Q1 provides three methods to wake up from sleep mode: EN pin, WAKE pin and LIN bus in pin control mode and two in SPI control mode, WAKE pin and LIN bus. The device integrates a low dropout voltage regulator with a wide input from V_{SUP} providing 5 V ±2.5% or 3.3 V ±2.5% with up to 125 mA of current depending upon system implementation.

The TLIN1431x-Q1 integrates a window-based watchdog supervisor which has a programmable delay and window ratio determined by pin strapping or SPI communication. The device watchdog is controlled by pin configuration or SPI depending upon the state of pin 7 at power up. During power up, if pin 7 is externally pulled to ground, the device is configured for pin control and all digital IO voltage levels will be dependent upon V_{CC}. If pin 7 is left floating or pulled up to V_{CC} the device is controlled by SPI communication and the pin becomes the nCS pin. For the 5 V V_{CC} version, the digital IO voltage levels are also determined during power up when the device is configured for SPI communication control. If pin 7 is left floating at power up, the internal pull up configures the device for 3.3 V SPI control. This means that all the digital IO for the device will be configured for 3.3 V electrical levels. If the processor needs 5 V IO, a 500 kΩ pull up resistor to the TLIN14315-Q1 V_{CC} pin will configure all digital IOs 5 V electrical levels. This allows the 5 V version of the device to work with both 3.3 V processors or 5 V processors. SPI communication is used for device configuration. This sets not only the SPI pins but also WKRQ, nRST, FSO, nINT, TXD and RXD pins. In pin configuration, nRST is asserted high when V_{CC} increases above UV_{CC} and stays high as long as V_{CC} is above this threshold and the device is not in restart mode.

When the watchdog is controlled by the device pins, the state of the WDT pin determines the window time. WDI is used as the watchdog input trigger which is expected in the open window. If a watchdog error event takes place, the nWDR pin goes low to reset the processors. When using SPI writing FFh to register 15h, WD_INPUT_TRIG, during the open window restarts the watchdog timer. The supervised processor must trigger the WDI pin or WD_INPUT_TRIG register within the defined window. When using SPI, the nRST pin can become the watchdog event output trigger for the processor if programmed this way, but the nRST function is lost. The watchdog timer has a long initial window when entering standby, normal and fast modes that a watchdog input trigger is expected.

8.2 Functional Block Diagram

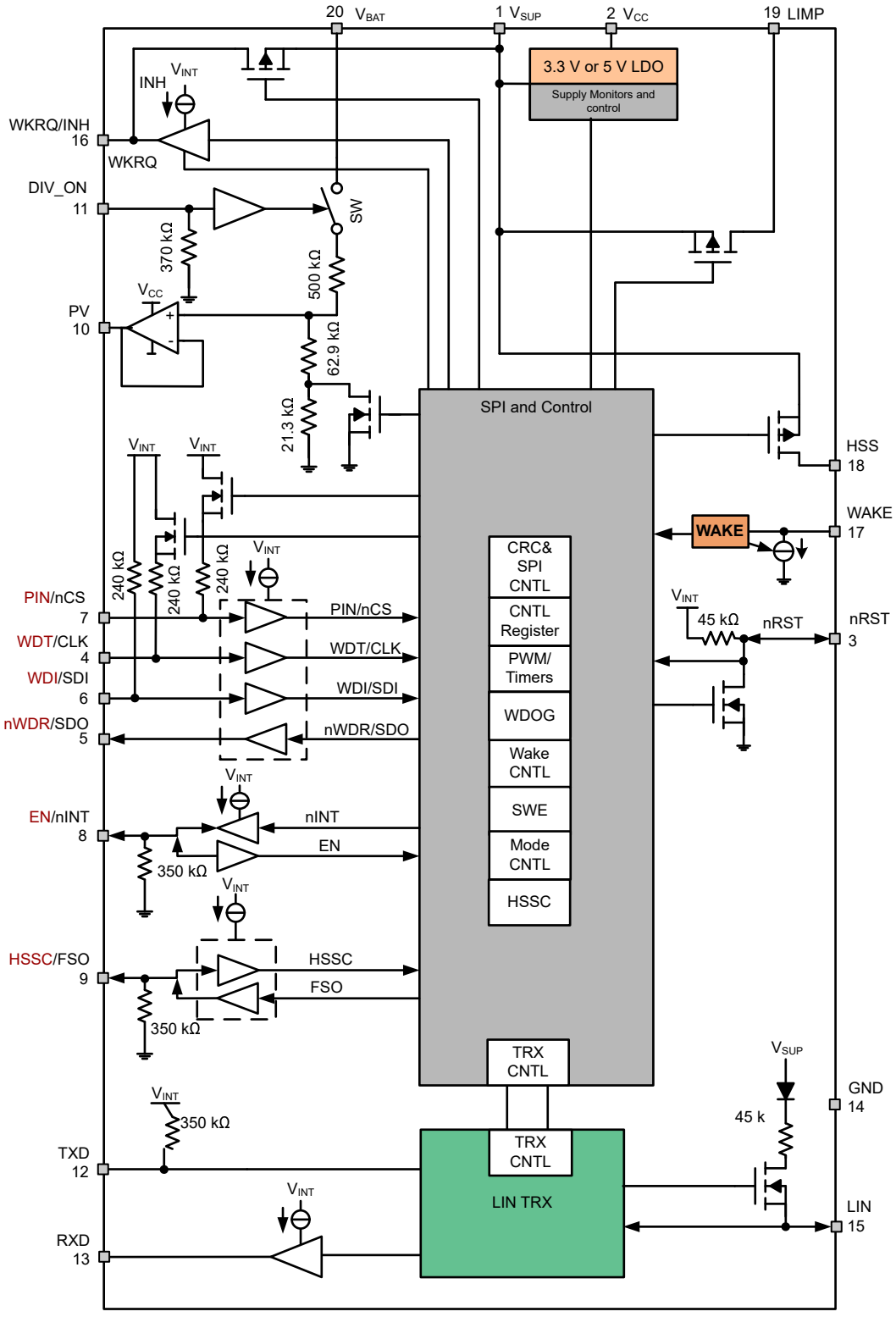


図 8-1. High Level Block Diagram

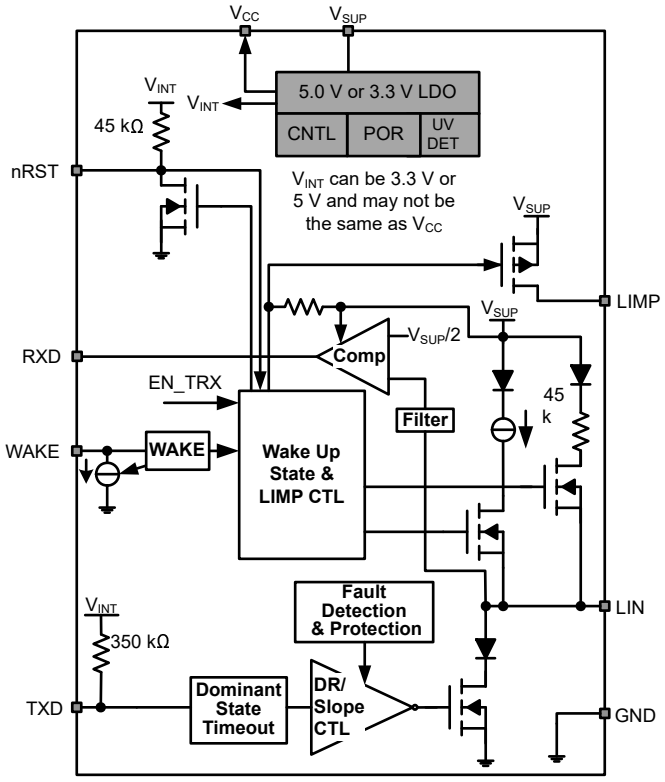


図 8-2. Transceiver plus VREG Functional Block Diagram

8.3 Feature Description

8.3.1 LIN (Local Interconnect Network) Bus

This high voltage input or output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 58 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

8.3.1.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a commander node application. In fast mode, the transmitter can support 200 kbps data rates.

8.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratiometric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (>100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1431x-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system. In fast mode the receiver can support 200 kbps.

8.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification (ISO 17987-4).

図 8-3 shows a Commander Node configuration and how the voltage levels are defined.

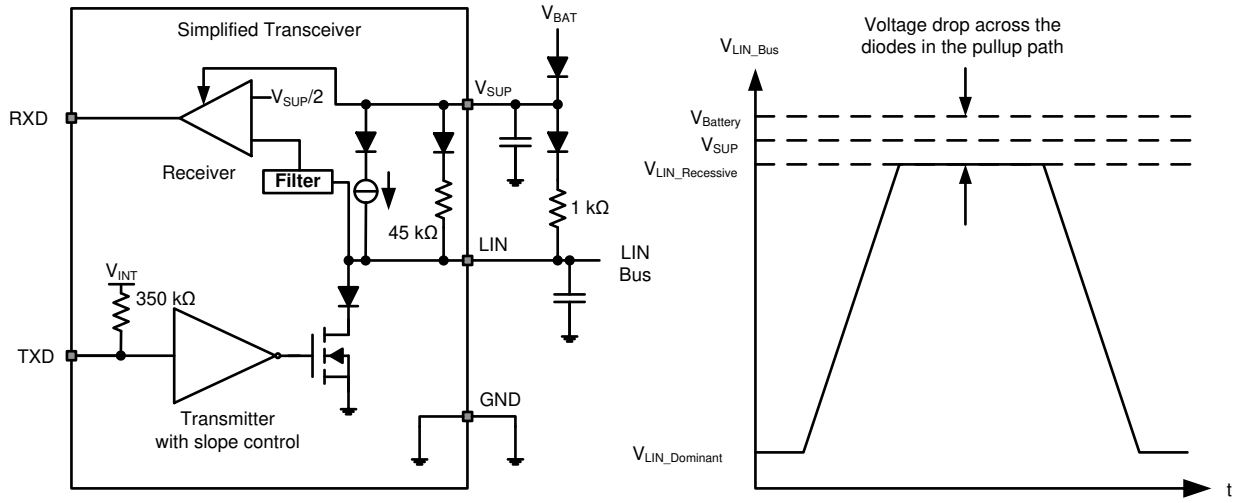


図 8-3. Commander Node Configuration with Voltage Levels

8.3.2 TXD (Transmit Input and Output)

TXD is the interface to the node processor LIN protocol controller that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near V_{SUP}). See 図 8-3. The TXD input structure is compatible with processors with 3.3 V and 5 V logic I/O. TXD has an internal pull-up resistor to an internal voltage rail that either matches the processor I/O voltage rail or the LDO output rail, V_{CC} which is determined by the state of pin 7 at power up. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timeout timer. The TXD pin is also used to help determine what mode to enter in pin control mode.

8.3.3 RXD (Receive Output)

RXD is the interface to the processors LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. This device architecture allows the device to be used with 3.3 V and 5 V I/O processors. The RXD pin is a push-pull buffer and as such an external pull-up is not needed. In restart mode, the RXD pin is driven high. When V_{CC} > UV_{CC} for t_{RSTN_act}, the device automatically transitions to standby mode causing RXD is then pulled low to indicate a wake-up request. The RXD pin can be programmed to toggle low or high to indicate a wake up request with a pulse width of t_{TOGGLE}, see 図 7-6 as an example of this feature.

8.3.4 WAKE (High Voltage Local Wake Up Input)

WAKE pin is used for a high voltage device local wake up (LWU). This function is explained further in Local Wake Up (LWU) via WAKE Terminal section. The pin is both rising and falling edge trigger, meaning it recognizes a LWU on either edge of WAKE pin transition. The pin can be configured to accept a pulse, see 図 8-46 for timing diagram of this behavior. WAKE pin is also used as part of the cyclic sensing wake, see Cyclic Sense Wake. Registers WAKE_PIN_CONFIG1 Register (Address = 11h) [reset = 04h] and WAKE_PIN_CONFIG2 Register (Address = 12h) [reset = 2h] provide the various configurations for the WAKE pin.

8.3.5 WDT or CLK (Pin Programmable Watchdog Delay Input or SPI Clock)

When configured for pin control, the WDT or CLK pin becomes the pin programmable watchdog delay input, WDT. This pin sets the upper boundary of the window watchdog. It can be connected to V_{CC}, connected to GND, or left floating. When connected directly to V_{CC} or GND or left open, the window frame takes on one of three value ranges: GND – 32 ms to 48 ms, V_{CC} – 480 ms to 720 ms or left open – 4.8 s to 7.2 s. The closed versus open windows are based upon 50%/50%.

When configured for SPI control, the WDT/CLK pin becomes the SPI input clock, CLK. When configured as the CLK pin there is a 240 kΩ pull-up to V_{INT} enabled.

8.3.6 WDI or SDI (Watchdog Timer Input or SPI Serial Data In)

When configured for pin control, the WDI or SDI pin becomes the watchdog timer input trigger, WDI. This resets the timer with either a positive or negative transition from the processor. A filter time of t_W is used to avoid false triggers.

When configured for SPI control, the WDI/SDI pin becomes the SPI serial data input pin, SDI.

8.3.7 PIN or nCS (Pin Watchdog Select or SPI Chip Select)

This pin determines if the TLIN1431x-Q1 watchdog and mode changes are controlled by pin or SPI. At power up, the device monitors this pin and determine which method is to be used. When tied to GND, the device is pin programmable, see 図 8-5. When connected to a high-Z processor IO pin or pulled up, the device is set up to support SPI, see 図 8-6. In SPI control mode, if the LDO is being used to power up circuitry other than the processor a mismatch can take place. An example of this is using the TLIN14315-Q1 V_{CC} to power up a 5 V sensor and the processor supports 3.3 V IO electrical levels. This is accomplished by letting the PIN/nCS pin float at power up which configures the internal IO electrical levels to V_{INT} which is 3.3 V. For the IO to be 5 V, an external 500 kΩ resistor needs to be pulled up to the 5 V V_{CC} pin. This makes the IO 5 V. See 図 8-4 to understand the three ways this pin can be connected for the 5 V LDO device.

注

The behavior of the microprocessor used must be understood if connecting to this pin to control whether the device is to be pin controlled or SPI controlled. There is an internal pull-up that sets the device in SPI control mode. If the processor pin drives low during power up, the device is in pin control mode. To specify pin control mode place and external pull-down resister to ground.

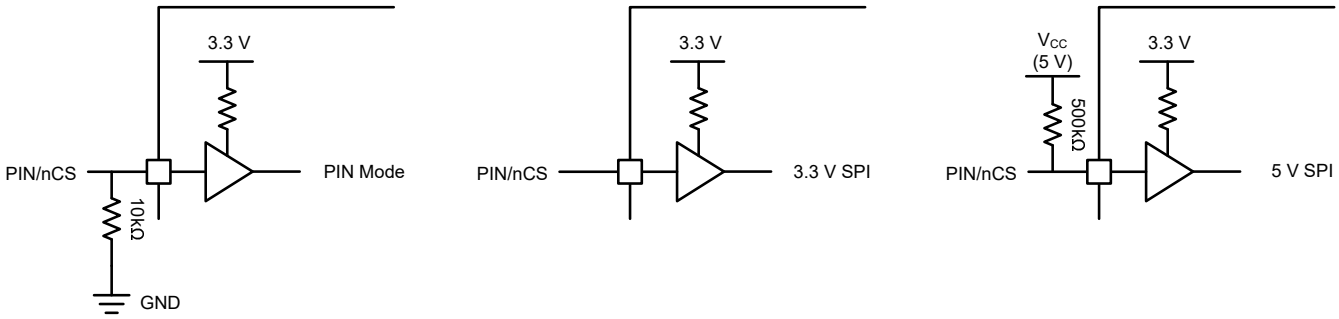


図 8-4. PIN/nCS configuration

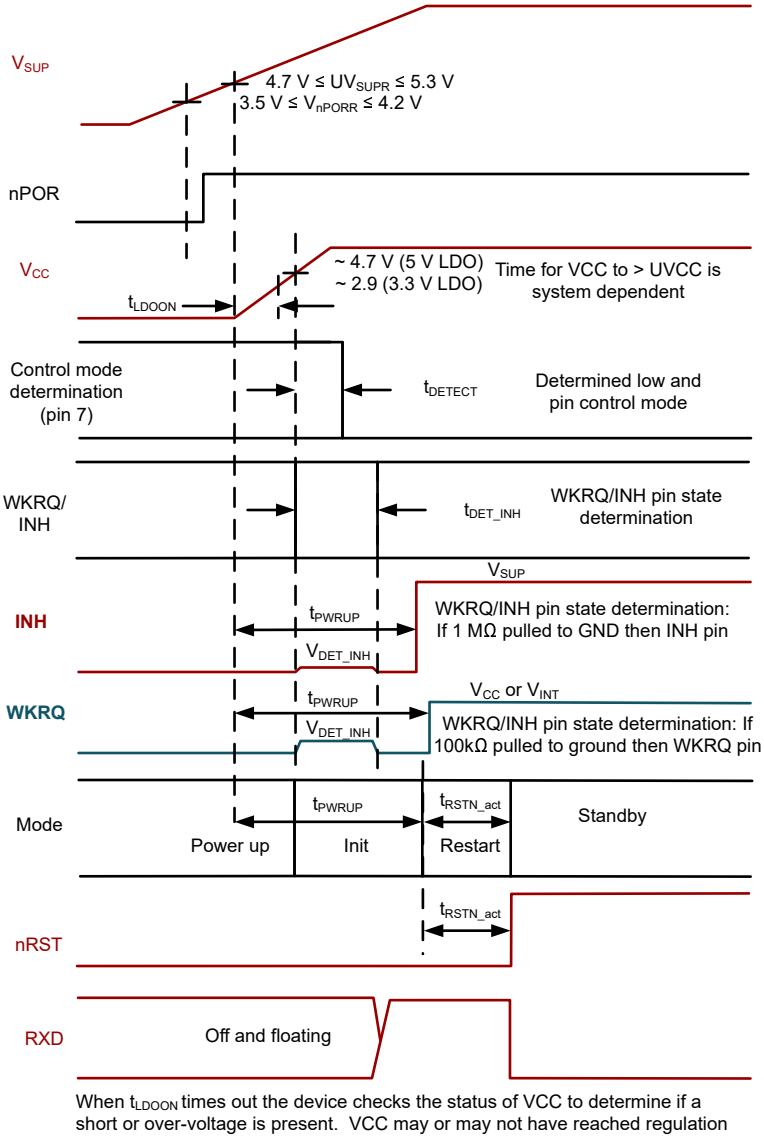


図 8-5. Power up timing diagram for pin 7 connected to ground

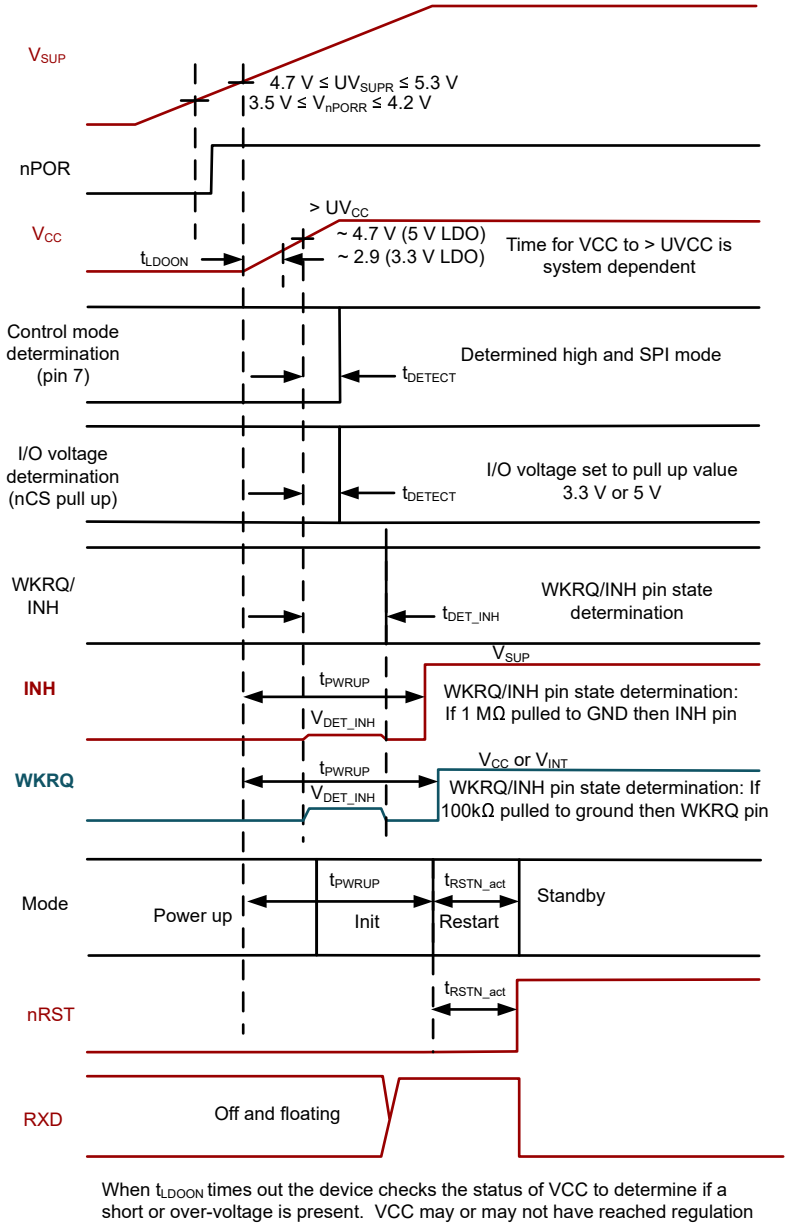


図 8-6. Power up timing diagram for pin 7 pulled high up

8.3.8 LIMP (Limp Home Output – High Voltage Open Drain Output)

The default configuration for the LIMP pin is used for the limp home function. When in the LIMP configuration, the pin is connected to external circuitry for a limp home function due to various fault conditions explained in the device functional mode sections. The LIMP pin can be configured as other functions in SPI control mode, but only performs the limp home function in pin control mode.

8.3.8.1 LIMP in Pin Control Mode

In pin control mode, LIMP is the only function the LIMP pin can perform. The LIMP pin turns on for all faults that cause the device to enter fail-safe mode to provide the limp home function. To exit fail-safe mode, a wake event must take place and the fault condition is cleared or the SWE timer times out. When any non-watchdog fault caused the device to enter fail-safe mode, the LIMP pin will turn off automatically after exiting fail-safe mode. When exiting fail-safe mode due to a watchdog fault, the LIMP pin is still on until the device transitions to standby mode and three correct watchdog input events take place thus turning off the LIMP pin. If this first event is missed, the device enters fail-safe.

8.3.8.2 LIMP in SPI Control Mode

In SPI control mode, the LIMP pin defaults to the limp home function. When fail-safe mode is enabled (default on) the pin behaves the same as stated in pin control mode with the exception of every watchdog error causing a reset. Programming register 8'h1A[3:2], LIMP_SEL_RESET, determines the condition for the LIMP pin to turn off. The three modes that the LIMP pin changes state is normal, fail-safe and standby mode. When in normal and standby mode the LIMP pin is off unless there is a watchdog failure event, which turns on the LIMP pin. When entering these two modes, there is an initial long window requiring a watchdog input trigger. This is treated as a WD failure and LIMP pin turns on if the window is missed. Any event that causes the device to enter fail-safe mode also turns on the LIMP pin. LIMP is turned off once the device enters standby mode from fail-safe mode except for a watchdog error as described previously. When fail-safe mode is disabled, a WD input failure causes the LIMP pin to turn on, and the device enters restart mode.

If the LIMP function is not needed, this pin can be configured to support either a high side switch in SPI mode by using register 8'h1B[7:6] = 01b or to the INH function by setting register 8'h1B[7:6] = 10b. When configured as a high side switch, the pin can support the same load as the HSS pin, but does not have the open load and over current detection features. When used as a high side switch, timing control is configurable using on/off, PWM or timer based. When using PWM, PWM1 or PWM2 can be assigned. When using the timer, timer1 or timer2 and be assigned.

8.3.9 nWDR/SDO (Watchdog Timeout Reset Output/SPI Serial Data Out)

When configured for pin control, the nWDR/SDO pin becomes the watchdog reset output pin, nWDR. When the watchdog times out, this pin goes low for time of 15 ms and then releases back to V_{CC}.

When configured for SPI control, the nWDR/SDO pin becomes the SPI serial data output pin, SDO.

8.3.10 HSS (High-side Switch)

This pin supports a high-side switch supporting up to a 100 mA load with 60 mA being typical with a 14 V V_{SUP}. In SPI mode, the HSS can be programmed to support a 200 Hz or 400 Hz 10-bit PWM. PWM1 or PWM2 can be assigned to the HSS. The HSS can be configured to use one of two timers that allows it to work with the WAKE pin. This supports cyclic sensing for sleep mode thus reducing sleep mode current. In pin mode this pin is controlled by the HSSC pin.

The switch supports open load detection and over current detection. When an over current is detected, there is a filter time, t_{OCFLTR}, to determine if over current is valid. If valid there is a shut off time, t_{OCOFF}, time for the HSS to shut off. When the HSS shuts off due to an over current event the HSS has to be re-enabled. This is accomplished differently depending upon whether the device is in pin control or SPI control. If in SPI control it will also depend upon how the HSS is configured.

Pin Control:

- HSS is controlled by the input signal on the HSSC pin.
- Once the over current fault is removed a high to low transition on the HSSC pin will re-enable the HSS output.

SPI Control and HSS_EN; 8'h1E[7] = 1b (enabled):

- When HSS is configured as On or HSSC controlled, HSS_CNTL 8'h1E[6:4] = 000b or 101b, the HSS will have to have the HSS_EN; 8'h1E[7] set to 0b (disabled) and then reset to 1b (enabled) or will turn on when HSSC receives the signal described above in "Pin Control."
- When HSS is configured utilizing a PWM or Timer, HSS_CNTL 8'h1E[6:4] = PWM1, PWM2, Timer1 or Timer2, the HSS will automatically turn on.

注

- For resistive loads, an external capacitor to ground in not required.
- For inductive loads, an external 100 nF capacitor to ground is needed.
- When using the 10-bit PWM with the HSS or LIMP configured as a HSS, it is possible to select values that are unrealizable due to the on and off times of the switch. An example of this would be 00 0000 0001b

8.3.11 HSSC or FSO (High-side Switch Control or Function Output)

In pin control mode, this pin is the high-side switch control pin. When in SPI control mode, the pin becomes a function output pin that can be selected from register 8'h29[3:1]. In SPI mode this pin can be switched back to HSSC input by using register 8'h1E[6:4] = 101b.

8.3.12 WKRQ or INH (Wake Request or Inhibit)

Upon power up, the state of this pin determines if it is WKRQ or INH. When externally pulled low with a 100 kΩ resistor, the WKRQ function is enabled which is an active high, digital output supporting the internal voltage rail (V_{INT}) or V_{CC} as described in PIN or nCS (Pin Watchdog Select or SPI Chip Select). When left floating or pulled low by a 1 MΩ resistor, this pin becomes the high voltage inhibit (INH) output which is used to support the enable pin of a power device. If a capacitor to ground is used off of this pin, it must be less than or equal to 50 pF. When WKRQ is selected, the pin behavior is based off of the LDO, so any event that causes the LDO to be turned off will turn off the WKRQ pin.

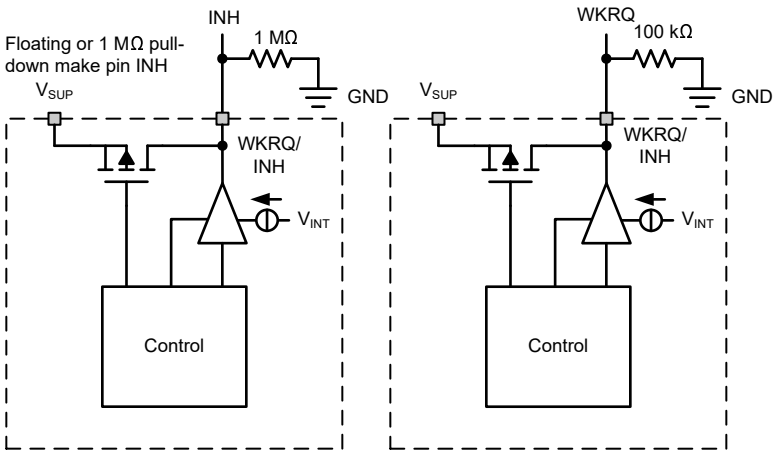


図 8-7. WKRQ or INH Pin Select

8.3.13 PV

This output pin is the divided down value from V_{BAT}. The output is buffered to keep the output from exceeding the specified values when V_{BAT} exceeds the recommended value. It is connected directly to the ADC of the microcontroller. It is connected by either an RC network or with just a capacitor to GND, see 図 8-8. It is switched on when a high is present on the DIV_ON pin. When off, the PV pin is in a high-Z state.

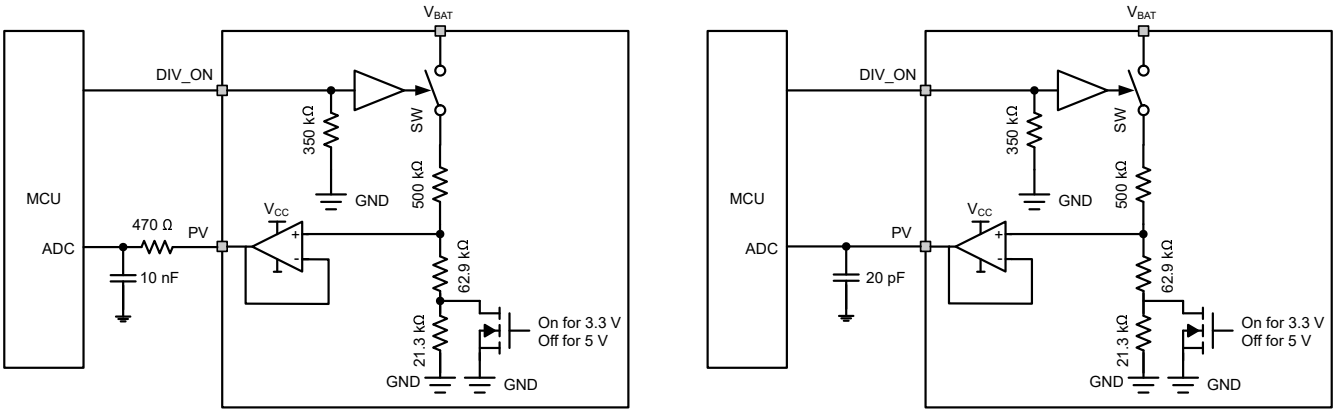


図 8-8. PV Connections to MCU

8.3.14 DIV_ON

This is a logic input pin used to enable the voltage divider PV output. This is an active high pin and is disabled in certain modes of operation.

8.3.15 V_{BAT} (Battery Voltage)

This pin is connected to the battery input prior to the reverse blocking diode. This pin is used in conjunction with the PV and DIV_ON pins.

8.3.16 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse battery-blocking diode (see 図 8-3). The V_{SUP} pin is a high-voltage-tolerant pin. Decoupling capacitors of 100 nF are recommended to be connected close to this pin to improve the transient performance. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied). When V_{SUP} drops low enough the regulated output drops out of regulation. The LIN bus works with a V_{SUP} as low as 5.5 V, but at a lower voltage, the performance is indeterminate and not guaranteed. If V_{SUP} voltage level drops enough, it triggers the UV_{SUP}, and if it keeps dropping, at some point it passes the POR threshold.

8.3.17 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

8.3.18 EN or nINT (Enable Input or Interrupt Output)

When configured as pin control, this pin becomes the transceiver enable control, EN. EN controls the operational modes of the device. When EN is high, the device can enter normal or fast operating modes allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device can enter standby or sleep mode depending upon the state of the TXD pin. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats. EN should be held low until V_{SUP} reaches the expected system voltage level.

When configured as SPI control, this pin becomes the processor interrupt pin. When the TLIN1431x-Q1 requires the attention of the processor, this pin is pulled low.

8.3.19 nRST (Reset Input and Reset Output)

The nRST pin is a bi-directional open-drain low side driver that serves three functions, a V_{CC} monitor output for under-voltage events, restart mode indicator and a device input reset. The pin is nRST in Pin Control Mode and the defaulted function for SPI mode. This pin is internally pulled up to V_{INT} by a 45 kΩ resistor. V_{INT} represents the TLIN1431-Q1 IO voltage level and may or may not be V_{CC}. It is recommended to use an external 10 kΩ pull-up to the processor IO voltage rail. The pin can determine when an input pulse of t_{nRSTIN} is applied causing the device to enter restart mode. When an under-voltage event takes place, the nRST is latched low after a 30 µs filter and the device transitions to restart mode, fail-safe mode disabled, or fail-safe mode after the t_{UVFLTR} has expired. When in restart and V_{CC} exceeds the UV_{CCR} threshold, the t_{RSTN_act} timer starts. After this timer times out, the device transitions to standby mode, and the nRST pin is released. If a thermal shutdown event takes place, the signal is pulled to ground. When the device is configured by SPI, the pin can be programmed to become the watchdog output trigger to reset the processor. When the watchdog times out, this signal is pulled low for time of t_{NRST_TOG} and then released back to V_{CC}. If both are needed for SPI configuration it is recommended to add an external circuit off the LIMP pin to serve as the watchdog output trigger to reset the processor. Note the LIMP pin output is a high voltage output based upon V_{SUP} and care must be taken when connecting to a lower voltage device.

8.3.20 V_{CC} (Supply Output)

The V_{CC} terminal is the regulated output based on the applicable voltage, 3.3 V or 5 V with up to 125 mA from 12 V supply voltage. This pin is used to power external devices and when using high-k boards and thermal management best practices full capability can be realized. The regulated voltage accuracy is ±2.5%.

When powering up the TLIN1431x-Q1, V_{CC} must be above UV_{CC} and without any faults. V_{CC} is used to determine the state of several pins that establishes several device functions, such as pin control or SPI control. If a fault, such as V_{CCSC}, is present at power up the device cannot determine the state of these pins. Fault needs to be cleared and power up performed again.

8.3.21 V_{BAT} Voltage Divider

The voltage divider is a reverse polarity protected resistor divider connected to V_{BAT} with fast response times. The divider is based upon the LDO value. For 5 V V_{CC}, the ratio is 1:7. For 3.3 V V_{CC}, the ratio is 1:9. The voltage divider is activated by a high on the DIV_ON pin. The divided output voltage is available on the PV pin for the microcontroller to read. See 表 8-1 for the modes that the DIV_ON functionality is enabled and disabled. When VBAT exceeds 28 V for the 5 V LDO and 20 V for the 3.3 V LDO the voltage is clamped to prevent damage to microcontroller. See 図 8-9 and 図 8-10 for the relationship between V_{BAT} and PV output voltage.

表 8-1. Voltage Divider Functionality Control by Mode

Mode of Operation	DIV_ON	PV Output State
Normal/Fail-Safe/Fast/ Standby	Low	Off
	High	On
Sleep/Pin Init/SPI Init/Restart	Low	Off
	High	Off

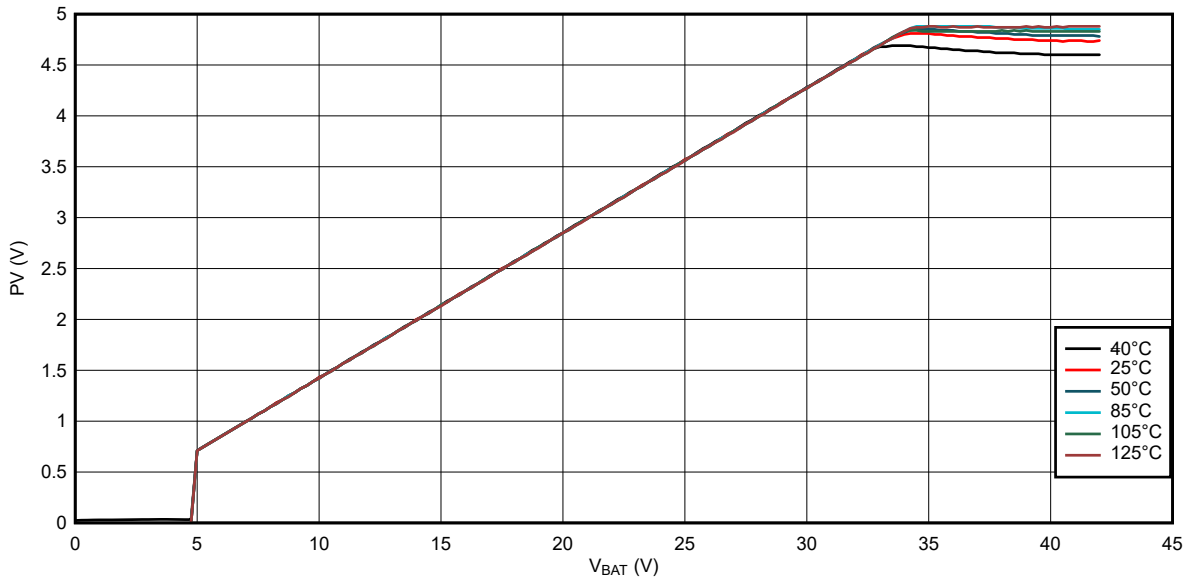


図 8-9. V_{BAT} vs PV for TLIN14315RGYQ1 for Different Ambient Temperatures

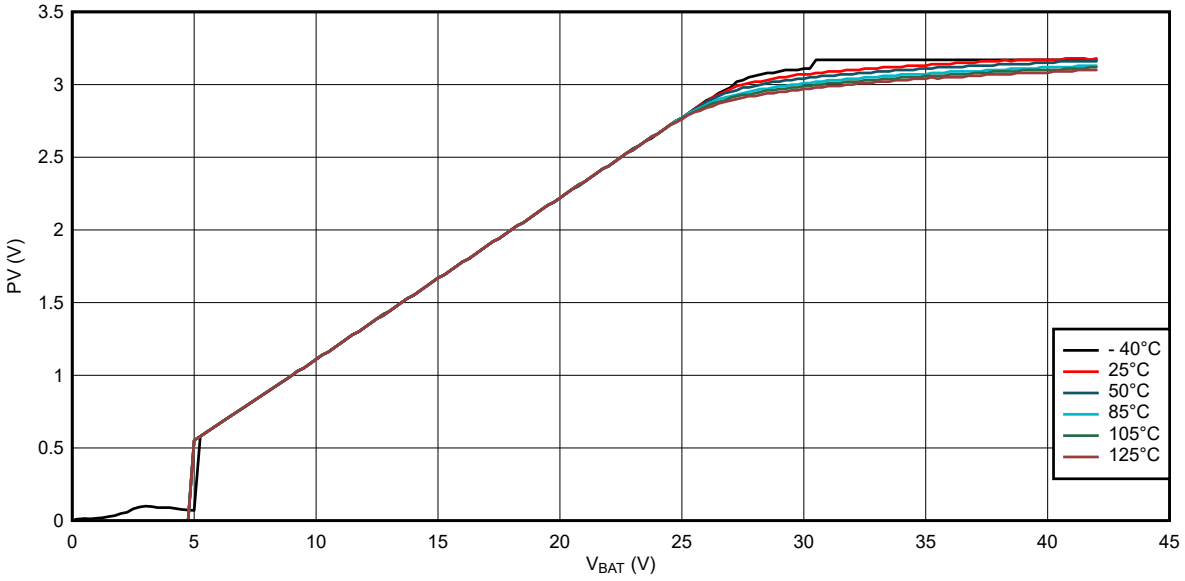


図 8-10. V_{BAT} vs PV for TLIN14315RGYQ1 for Different Ambient Temperatures

8.3.22 Protection Features

The device has several protections features that are described as follows.

8.3.22.1 Sleep Wake Error (SWE) Timer

The TLIN1431x-Q1 implements a sleep wake error timer, t_{INACT_FS}. The purpose of the SWE timer is to keep the device and the node from being stuck in a high-power state. This timer is used to place the device into fail-safe or sleep mode due to fault conditions. In Pin mode, the SWE timer starts automatically when entering fail-safe and restart modes. A wake event causes the device to move from sleep mode to restart mode and if V_{CC} does not exceed UV_{CC} before the SWE timer times out the device re-enters sleep mode. This happens in either SPI or pin control modes.

In SPI mode, the SWE timer, when enabled, automatically starts when the device enters fail-safe, restart and standby modes. When the device leaves restart mode and enters standby mode, the processor must initiate a SPI transaction before the SWE timer times out or the device will enter fail-safe mode if enabled or sleep mode. This timer can be disabled at register 8'h1C[7] = 1. If the SWE timer duration is changed, this is accomplished register 8'h1C[6:3]. It can be changed from default of 5 min to between 30 sec to 10 min.

8.3.22.2 Device Reset

The TLIN1431 device can be reset in various ways. In SPI mode, there are three methods to reset the device. Two are accomplished with SPI commands – soft reset and hard reset. Soft reset and hard reset are accomplished by writing 02h or 01h respectively to DEVICE_RST (Address 19h) register. nRST pin can also be used to reset the device by pulling nRST low for t_{nRSTIN} and releasing the pin. nRST pin reset works for both SPI and PIN mode.

When performing a soft reset (SPI Mode), the following takes place:

- Device transitions to restart mode, nRST pin is pulled low for t_{NRST_TOG} and then transitions to standby mode.
- All registers are reset to default values
- All pending interrupts are cleared (unless a fault persists). PWRON interrupt is not cleared by soft reset.
- V_{CC} stays in the same state it was in
- INH stays ON

When performing a hard reset (SPI Mode), the following takes place:

- Similar behavior as power-up

- Device transitions to Init mode – V_{CC} is re-enabled, INH/WKRQ is re-sampled, SPI/PIN mode determination is made
- All registers are reset to default values
- PWRON flag is set is with a hard reset (if previously cleared)

When pulling nRST pin low and releasing (SPI or PIN Mode), the following takes place:

- Device transitions to restart mode, nRST pin is pulled low for t_{NRST_TOG} and then transitions to standby mode.
- All registers retain the same value as before nRST reset
- V_{CC} stays in the same state it was in
- All pending interrupts are retained
- INH stays ON

8.3.22.3 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{TXD_DTO}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{TXD_DTO} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-up to make sure the device fails to a known recessive state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on. The TLIN1431x-Q1 can turn off TXD dominant state timeout when in SPI mode by using register 8'h1D[5] = 1b.

8.3.22.4 Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. 図 8-11 and 図 8-12 show the behavior of this protection.

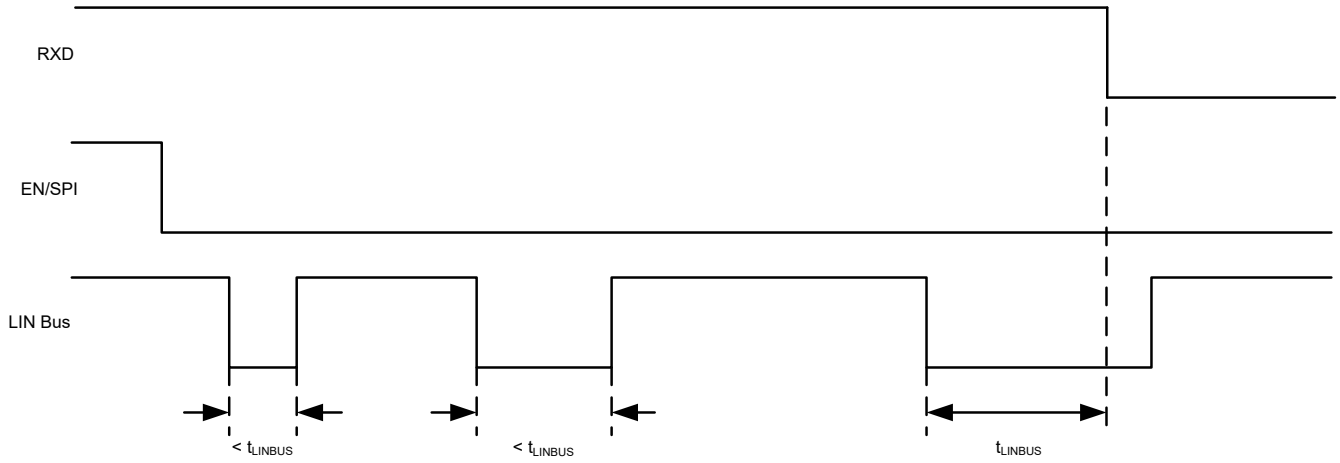


図 8-11. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake Up

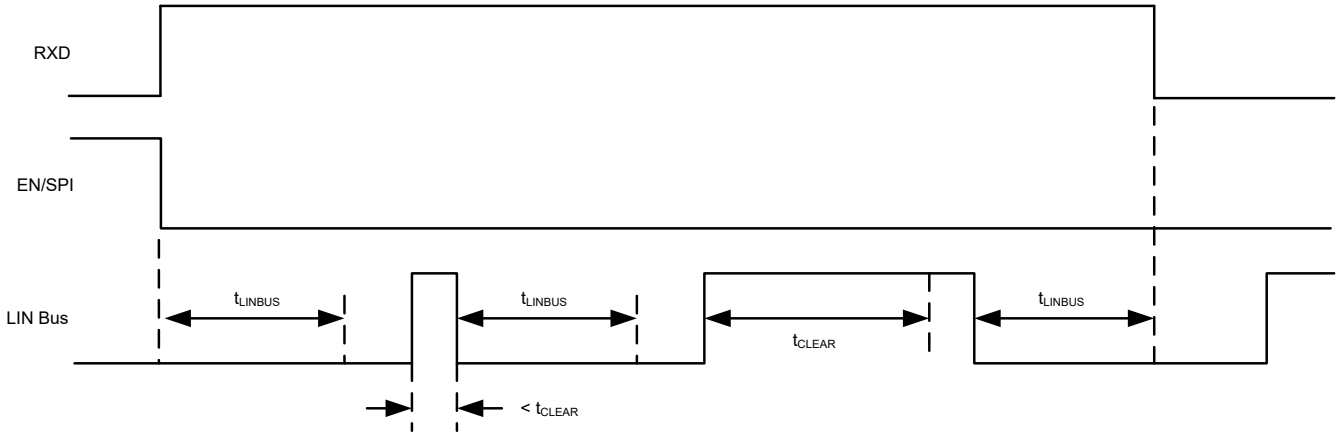


図 8-12. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake Up

8.3.22.5 Thermal Shutdown

The TLIN1431x-Q1 has multiple thermal sensors in the device to monitor the junction temperature of the die. The V_{CC} LDO, LIN transmitter, and high side switch/LIMP cells are monitored. Depending upon which cell's junction temperature are exceeded will determine the action taken by the device. Exceeding the maximum junction temperature for the LIN transmitter or LDO will cause the LIN transmitter into the recessive state and turns off the V_{CC} regulator. The nRST pin is pulled to ground during a LIN or V_{CC} LDO TSD event. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter can be re-enabled. Exceeding the max junction temperature of the high side switch or LIMP cells will cause the cells to be turned off.

In pin control mode, a TSD event on the LIN transceiver or V_{CC} LDO causes the device enters a fail-safe mode. Once the TSD fault has been removed and a wake event takes place, the device enters restart mode. If a wake event takes place and the TSD fault has not cleared, the device enters sleep mode immediately. Exceeding the max junction temperature for the high side switch and LIMP high side switch cause the switches to be turned off until junction temperature falls below T_{SDF}.

In SPI mode, there are two interrupts that can be set due to a thermal event. If the LIN transceiver or V_{CC} LDO junction temperature is exceeded, the TSD_VCC_LIN interrupt is set and the devices takes the action previously described. If the high side switch or LIMP high side switch max junction temperature is exceeded, the TSD_HSS_LIMP interrupt is set. The device takes the action previously described. In SPI mode, the device defaults to support fail-safe mode. The device enters fail-safe mode upon an TSD_VCC_LIN event and LIMP is turned on (see 図 8-25). Exiting fail-safe mode is the same as when the device is pin controlled. When fail-safe mode is disabled, the device enters sleep mode upon a TSD_VCC_LIN event.

8.3.22.6 Under-voltage on V_{SUP}

The device monitors V_{SUP} for two low voltage thresholds, UV_{SUP} and V_{nPOR}. When V_{SUP} drops below UV_{SUPF} and is above V_{nPORF}, the device is in an under-voltage power state. Once V_{SUP} ramps above UV_{SUPR}, the device enters restart mode and turns on the V_{CC} LDO, see Restart Mode. When V_{SUP} drops below V_{nPORF}, the device goes into a power off state. Once V_{SUP} ramps above V_{nPORR}, the device prepares the digital core to wake up. The device waits for V_{SUP} to rise above UV_{SUPR} and then turns on the V_{CC} LDO. Once V_{SUP} and V_{CC} are above their under-voltage levels, the device enters Init mode, see Init Mode. The described under-voltage events are also considered brown out events and more information can be found at Device Brownout information.

8.3.22.7 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

8.3.22.8 Floating Pins

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See 表 8-2 for details on terminal bias conditions.

表 8-2. Internal Pull-ups and Pull-downs on Device Pins

Pin	Pull-up or Pull-down	Typical Value	Comment
TXD	Pull-up	350 kΩ	
WDT/CLK	Pull-up	240 kΩ	When device configured for SPI control, CLK
WDI/SDI	Pull-up	240 kΩ	
PIN/nCS	Pull-up	240 kΩ	When device configure for SPI control, nCS
DIV_ON	Pull-down	370 kΩ	
LIN	Pull-up	45 kΩ	
EN/nINT	Pull-down	350 kΩ	
HSSC/FSO	Pull-down	350 kΩ	
nRST	Pull-up	45 kΩ	

8.3.22.9 V_{CC} Voltage Regulator

The device has an integrated high-voltage input LDO that operates over a 5.5 V to 28 V input voltage range for both 3.3 V and 5 V V_{CC}. The device has an output current capability of 125 mA and support fixed output voltages of 3.3 V (TLIN14313-Q1) or 5 V (TLIN14315-Q1). It features thermal shutdown and short-circuit protection to prevent damage during over-temperature and over current conditions

8.3.22.9.1 Under or Over Voltage and Short Circuit

The V_{CC} pin is the current limited regulated output based supporting an accuracy of ±2.5%. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UV_{SUP} threshold, the regulator turns off until the input voltage returns above the UV_{SUPR} level. When 5 V LDO is used, the device uses the voltage regulator during Init mode to determine the WKRQ/INH function, and the IO voltage. The device monitors V_{CC} for under-voltage, over-voltage, short to ground and thermal events. The device control method and whether fail-safe mode is enabled determine the behavior of the of the device for these events. Fail-safe mode is always active when the device is in pin control. In SPI control, the state diagram shows two paths: fail-safe mode enabled and fail-safe mode disabled. The path followed depends on whether fail-safe mode is enabled or disabled in 8'h17[0] FSM_DIS.

For an under-voltage event, V_{CC} is less than or equal to UV_{CCF}. After a 30us filter time, the device pulls nRST low and after the t_{UVFLTR} time, the interrupt flag is set and device transitions to restart mode, if fail-safe disabled, or fail-safe mode. When entering either mode, the SWE timer t_{INACT_FS} starts, and, in SPI control, the mode counter increments and the appropriate interrupt flags are set. To exit fail-safe mode, the under-voltage has to clear and a wake event takes place prior to the SWE timer timing out. If the under-voltage event has not cleared when the wake event takes place or if the SWE timer times out, the device enters sleep mode. 図 8-13 shows how a UV_{CC} event is handled..

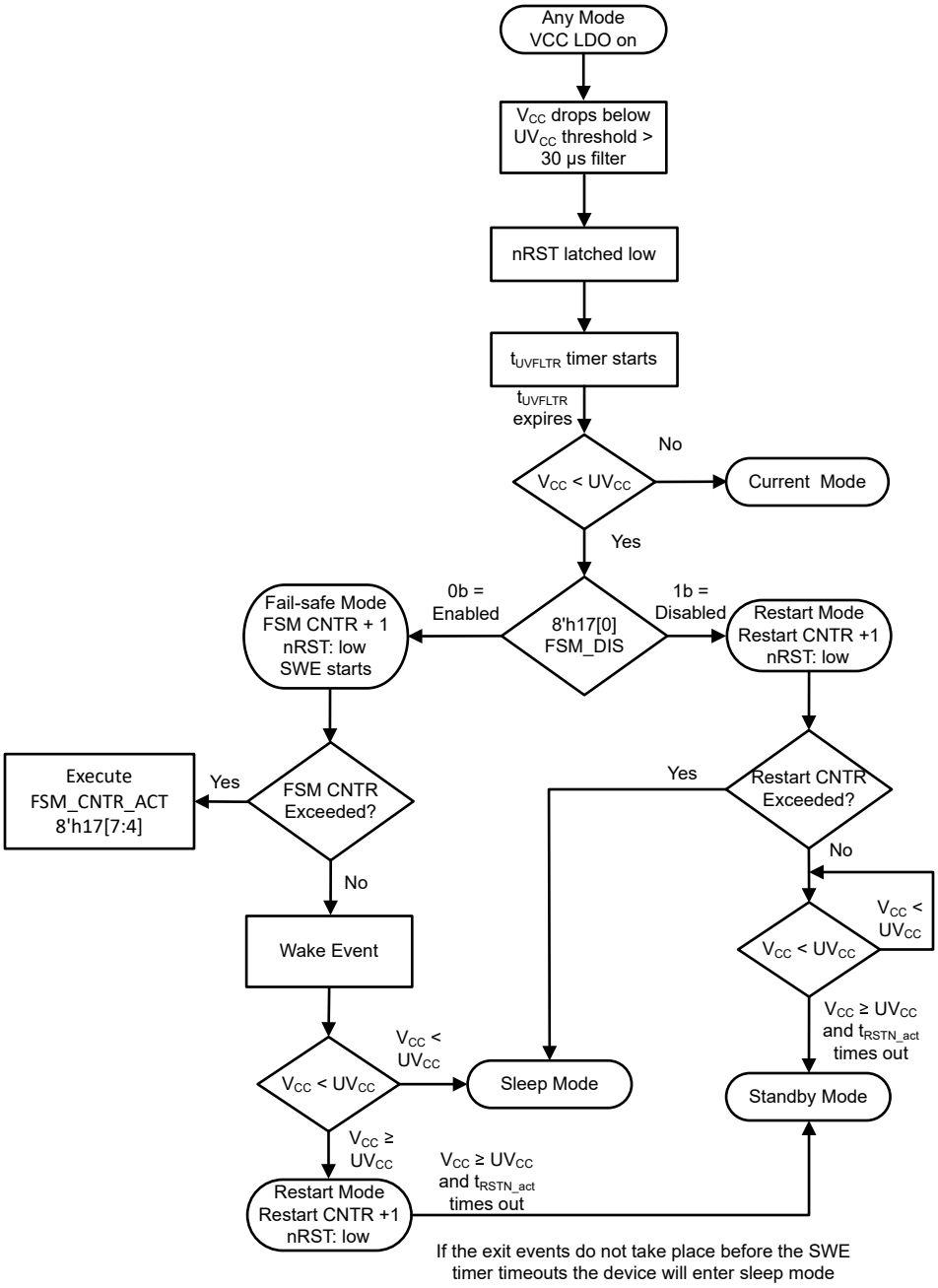


図 8-13. UV_{CC} flow chart

注

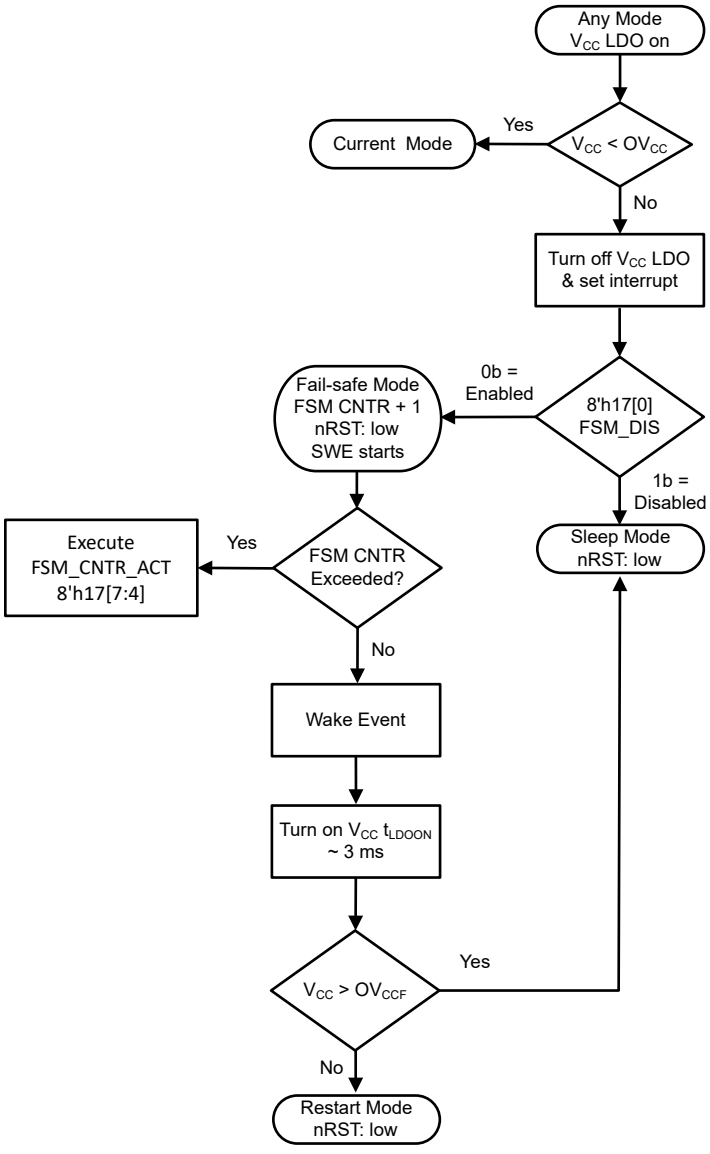
If an over-voltage or short circuit event takes place while the device is in fail-safe mode due to a under-voltage event on V_{CC}, the device will behave as shown in the OV_{CC} and VCC_{SC} flow charts.

For an over-voltage event, OV_{CC}, the device turns off the V_{CC} LDO, and transitions to either sleep mode, fail-safe mode disabled, or fail-safe mode. When a wake event takes place, the V_{CC} LDO is turned on for t_{LDOON} to determine if the over-voltage is still present. If cleared, the device enters restart mode from either sleep or fail-safe modes. When in fail-safe mode, if the over-voltage has not cleared when the wake event takes place the device transitions to sleep mode.

注

If an over-voltage event takes place while the device is in Init mode the following will happen:

- The device will sample the pins and determine whether the device is Pin or SPI control
- The device will determine the input/output voltage level if the TLIN14315-Q1
- The device will determine if WKRQ/INH pin is WKRQ or INH
- The device will transition to fail-safe mode



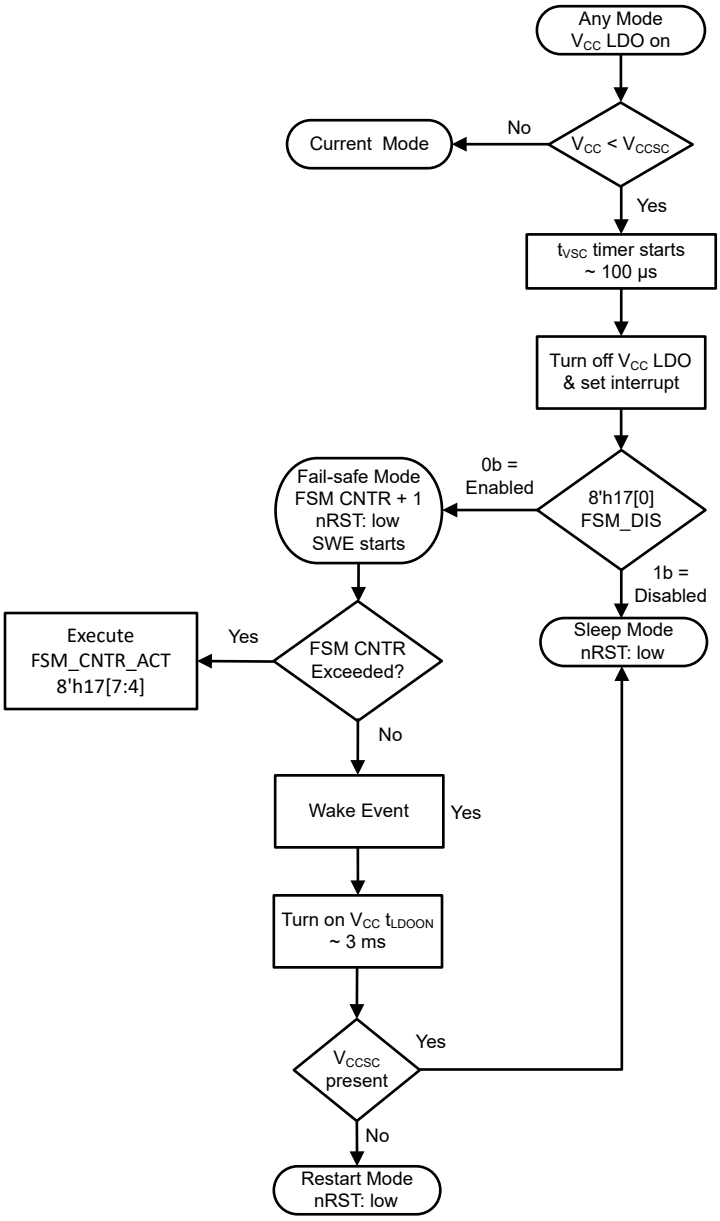
If the exit events do not take place before the SWE timer timeouts the device will enter sleep mode

図 8-14. OV_{CC} flow chart

For a short to ground event, V_{CCSC}, the device turns off the V_{CC} LDO and transitions to either sleep mode, fail-safe mode disabled, or fail-safe mode. When a wake event takes place, the V_{CC} LDO is turned on for t_{LDOON} to determine if the short to ground is still present. If cleared, the device enters restart mode from either sleep or fail-safe modes. When in fail-safe mode, if the short to ground has not cleared when the wake event takes place the device will transition to sleep mode.

注

If a short circuit event is detected while the device is in Init mode the device will transition to sleep mode. The device will not have determined the state of the pins and default to Pin control and will need to be powered cycled if the default state is different than what is expected.



If the exit events do not take place before the SWE timer timeouts the device will enter sleep mode

図 8-15. V_{CCSC}, short to ground

8.3.22.9.2 Output Capacitance Selection

For stable operation over the full temperature range and with load currents up to 125 mA on V_{CC}, a certain capacitance is expected, and depends upon the minimum load current. To support no load to full load, a value of 10 µF and ESR smaller than 2 Ω is needed. For 50 µA to full load, a smaller capacitance can be used but is system dependent and should be selected that will meet LIN to V_{CC} cross talk compliance during DPI testing. The low ESR recommendation is to improve the load transient performance.

8.3.22.9.3 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (IL) and switch resistor. This tracking allows for a smaller input capacitance and can possibly eliminate the need for a boost converter during cold-crank conditions.

8.3.22.9.4 Power Supply Recommendation

The device is designed to operate from an input-voltage supply range between 5.5 V and 28 V. This input supply must be well regulated, if the input supply is located more than a few inches from the device. The recommended minimum capacitance at the pin is 100 nF. The max voltage range is for the LIN functionality. Exceeding 24 V for the LDO reduces the effective current sourcing capability due to thermal considerations.

8.3.22.10 Watchdog

The TLIN1431x-Q1 has an integrated watchdog function. This can be programmed by pin control or SPI communication control based upon the state of the PIN or nCS pin at power up. The device defaults to windows based watchdog at power up. When entering normal and fast modes, the programmed watchdog timer starts based upon the pin configuration for pin mode or register configuration in SPI control mode. When entering standby mode from restart mode, there is a nRST transition from low to high. This transition starts the t_{INITWD} timer. A WD trigger input must take place prior to this initial long window times out. If WD is disabled in standby mode the same long window is implemented in normal mode. The LIMP pin provides a limp home capability when connected to external circuitry. When in sleep mode, the limp pin is off. When the error counter reaches the watchdog trigger event level, the LIMP pin turns on connecting V_{SUP} to the pin as described in the LIMP pin section and the device transitions to restart mode at which time the nRST pin will be pulled low.

8.3.22.10.1 Watchdog in Pin Control Mode

The state of the WDT pin determines the window watchdog timing for three different windows. Timeout watchdog is not available in pin control. The watchdog timer starts once the device has entered standby. The mode the device enters is based upon other pins, EN and TXD. Fast mode can be used as a software development mode as the WD is enabled but does not cause any action to take place. The watchdog feature cannot be disabled in pin control mode. See 図 8-16 for state diagrams on how the WD behaves.

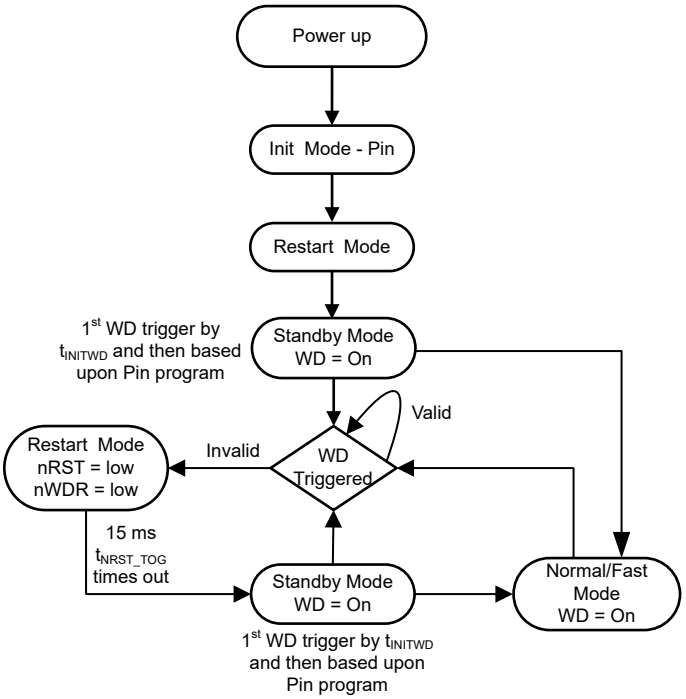


図 8-16. Watchdog state diagram in pin mode

8.3.22.10.2 Watchdog in SPI Control Mode

In SPI control, the window has extensive configurability including the ability to select the timeout watchdog. Watchdog is default enabled for standby mode, but can be disabled by setting register 8'h14[0] = 1b. Register 8'h13[7:6] can be set to 00b to disable the WD. There is a WD error counter available in SPI control mode, see Watchdog Error Counter for description of this counter. When a WD error occurs and if the WD error counter reaches programmed count, the device transitions to restart mode and pulls nRST low for t_{NRST_TOG}. Once this time has been met, the device transitions to standby mode and sets nRST pin high. See 図 8-17 and 図 8-18 for state diagrams on how the WD behaves.

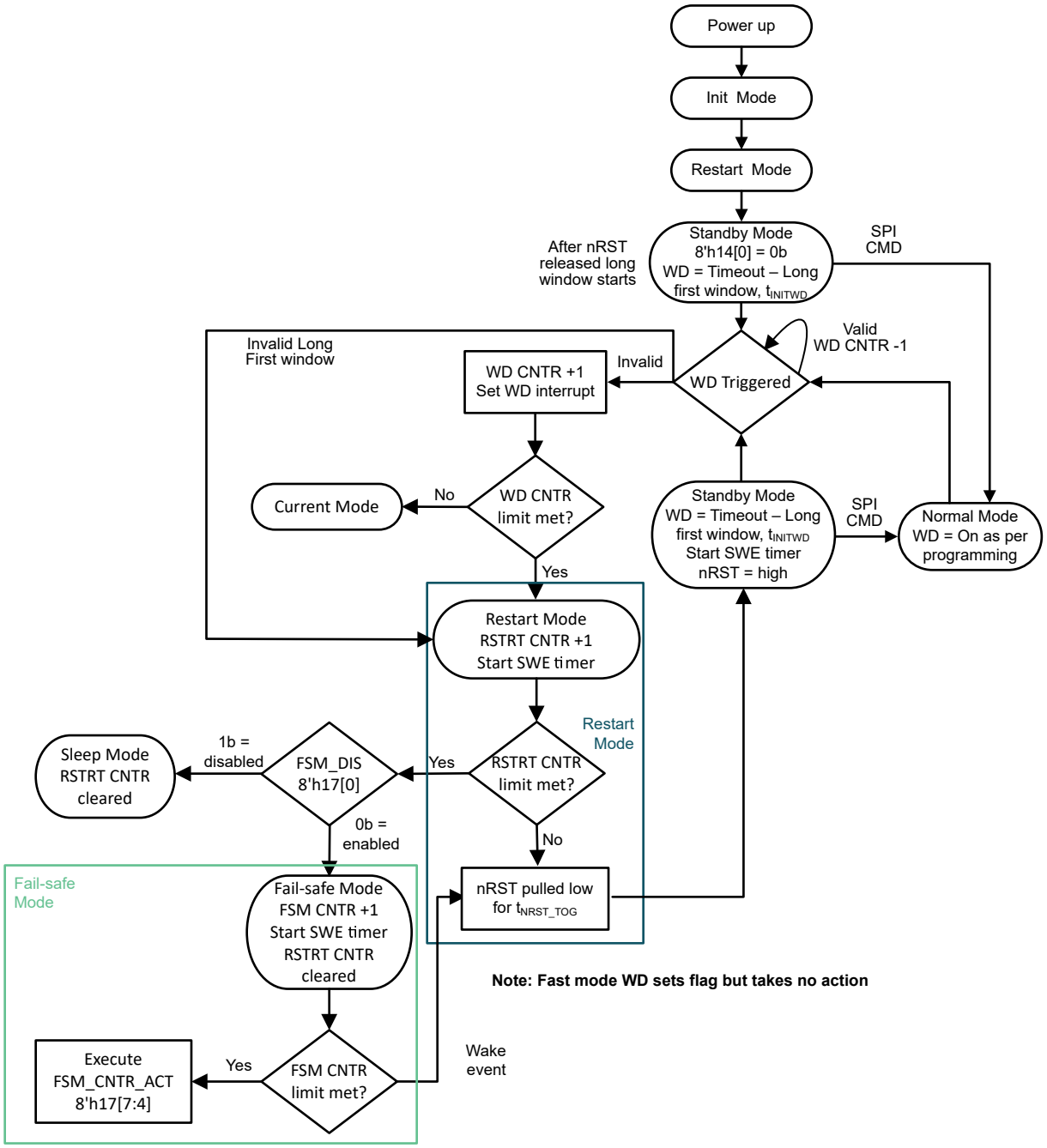


図 8-17. Watchdog state diagram in SPI mode; Standby Mode Enabled

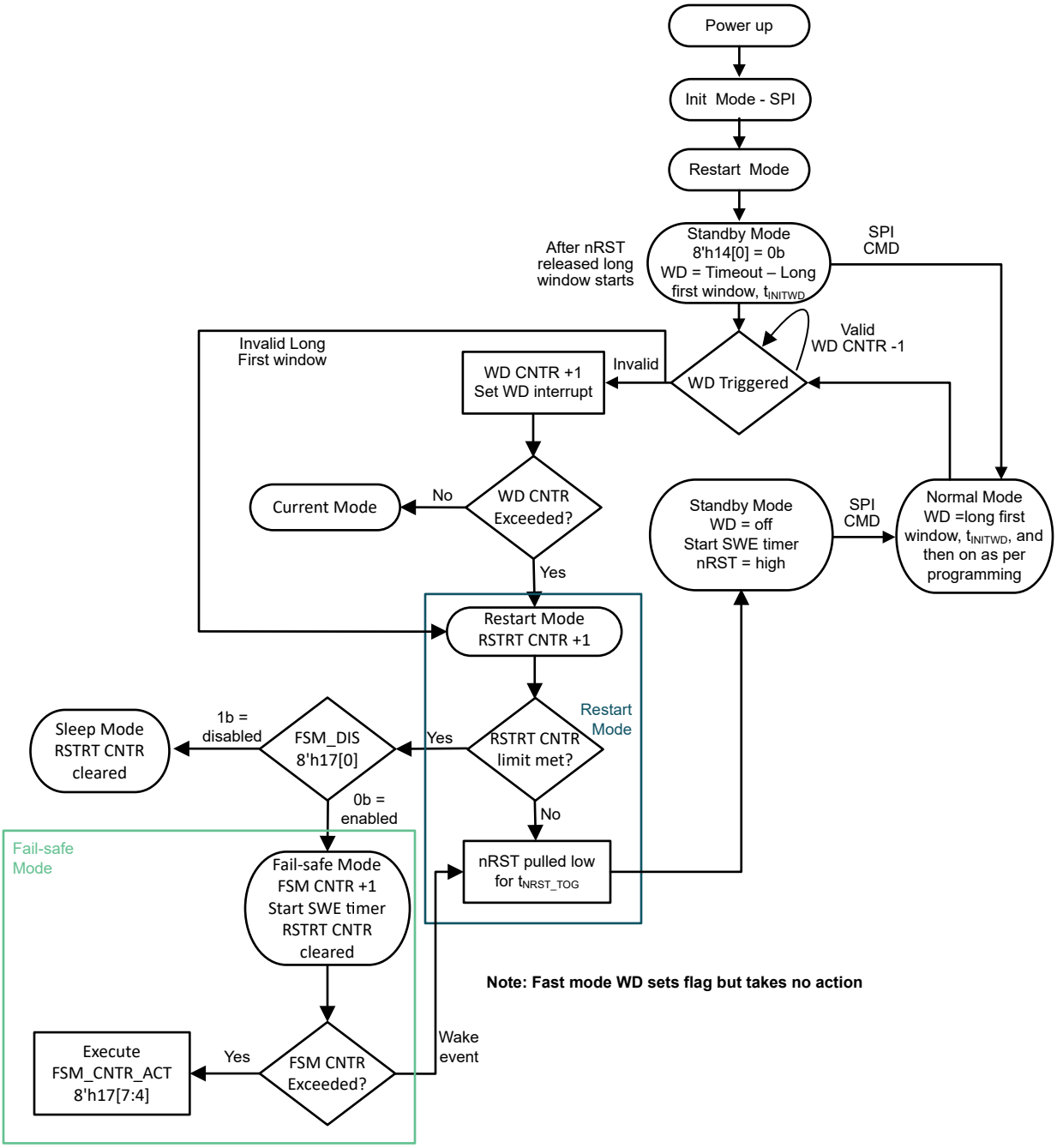


図 8-18. Watchdog state diagram in SPI mode; Standby Mode Disabled

注

- When the mode is changed while the timeout or window watchdog is running, it restarts once entering the new mode, fast, normal and standby.
- If the watchdog configuration is changed on-the-fly while the watchdog is running, it resets the error counter to 1 and resets the watchdog timers.

8.3.22.10.3 Watchdog Error Counter

The TLIN1431x-Q1 has a watchdog error counter used in SPI control mode. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. In SPI control, the error

counter is set at one by default. The counter decrements for every correct input trigger and increments on every incorrect input trigger, but it never drops below zero. When the programmed counter is reached, the device transitions to restart mode, error counter is reset back to one, and the nRST pin pulls low for t_{NRST_TOG}. At the end of this time, the device transitions back to standby mode releasing the nRST pin to high. This counter can be changed to 1 (every error), 5, 9, or 15 using 8'h16[7:6]. The error counter can be read at register 8'h14[4:1]. In pin control, nWDR is pulled low for every watchdog error.

If the watchdog error count is set at one, the first input failure causes the device to transition to restart. This allows the system to check the counter after the first input trigger to see if a valid input was sent. Every incorrect watchdog input causes the interrupt to be set and nINT is pulled low.

8.3.22.10.4 Pin Control Mode

When using pin control for programming the watchdog, the WDT pin is used for this function. WDT sets the total window size of the window watchdog. It can be connected to VCC, GND or left open. See セクション 8.3.5 or セクション 6.7 for details on window timings. The ratio between the upper (open window) and lower (closed window) is 50/50. WDI pin is used by the controller to trigger the watchdog input. The WDI input is an edge-triggered event and supports both rising and falling edges. A filter time of t_W is used to avoid noise or glitches causing a false trigger. A pulse would be treated as a two input trigger events and cause the nWDR and nRST pins to be pulled low. nWDR pin can connected to the controller reset pin and if a watchdog event happens this pin is pulled low. The nRST pin may also be used for this function but includes other possible errors, like under-voltage or entering restart mode.

8.3.22.10.5 SPI Control Programming

In SPI control, registers 8’h13 through 8’h16 control the watchdog function. The device watchdog can be set as a timeout watchdog or window watchdog by setting 8’h13[7:6] to the method of choice. The timer is based upon register 8’h13[5:4] WD prescaler and register 8’h14[7:5] WD timer and is in ms. See 表 8-3 for the achievable times.

8.3.22.10.6 Watchdog Register Relationship

表 8-3. Watchdog Window and Timeout Timer Configuration (ms)

WD_TIMER (ms)	Register 8'h13[5:4] WD_PRE			
Register 8'14[7:5]	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

8.3.22.10.7 Watchdog Timing

The TLIN1431x-Q1 provides two methods for setting up the watchdog when in SPI communication mode: window watchdog or timeout watchdog. If more frequent (i.e. <16 ms) input trigger events are desired it is suggested to use the timeout watchdog. When using timeout watchdog, the input trigger can occur anywhere before the timeout and is not tied to an open window.

When using the window watchdog, it is important to understand the closed and open window aspects. The device is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be considered. For example, using the 64 ms nominal total window provides a closed and open window that are each 32 ms. Taking the ±10% internal oscillator into account means the total window could range from 57.6 ms to 70.4 ms. The

closed and open window could then range from 22.4 ms to 35.2 ms. From the 57.6 ms total window and 35.2 ms closed window, the total open window is 22.4 ms. The trigger event needs to happen at 46.4 ms ± 11.2 ms. The same method is used for the other window values. 図 7-8 provides the above information graphically.

8.3.23 Channel Expansion

The TLIN1431x-Q1 has the ability to control an external LIN or CAN FD transceiver or a general purpose LIN or CAN FD SBC. The processor controls the mode of the external transceiver by using the FSO pin from the TLIN1431x-Q1 to the external transceiver. This is accomplished using the TLIN1431-Q1 SPI port, controlling the FSO pin as an EN/STB/nSTB/S output pin to the external transceiver. This capability allows the system designer to develop nodes with many different configurations, for example:

- Two LIN transceivers by using a simple eight pin LIN transceiver (see 図 8-19)
- Two LIN transceivers with two WAKE and INH capability by using an enhanced eight pin LIN transceiver (see 図 8-20)
- Two LIN transceivers with two LDO outputs by using an eight pin LIN SBC (see 図 8-21)
- One LIN and one CAN FD transceiver by using a simple eight pin CAN FD transceiver (see 図 8-22)
- One LIN and one CAN FD transceiver with two LDO outputs by using a CAN FD SBC (see 図 8-23)

8.3.23.1 Channel Expansion for LIN

The TLIN1431x-Q1 has the ability to control an external LIN transceiver like the TLIN1039-Q1 or TLIN1021A-Q1 or a general purpose LIN SBC like the TLIN1028x-Q1. The FSO pin is configured as a general purpose output pin. The FSO output level can be changed to meet the needs of the transceiver. The supply voltage of this transceiver can be connected to V_{SUP} or controlled by the HSS pin from the TLIN1431x-Q1. To configure the device to support an external LIN device the following registers and bits need to be configured:

- Register 8'h29[3:1] = 110b sets the FSO pin to a general-purpose output pin.
- Register 8'h29[4] sets the voltage level of the FSO pin when configured as a general-purpose output pin and can be used to control the EN pin of an external LIN transceiver or SBC.
- To use the high-side switch (HSS) as the power to the external transceiver, turn on HSS. Note that when the device enters sleep mode, the HSS pin is turned off.

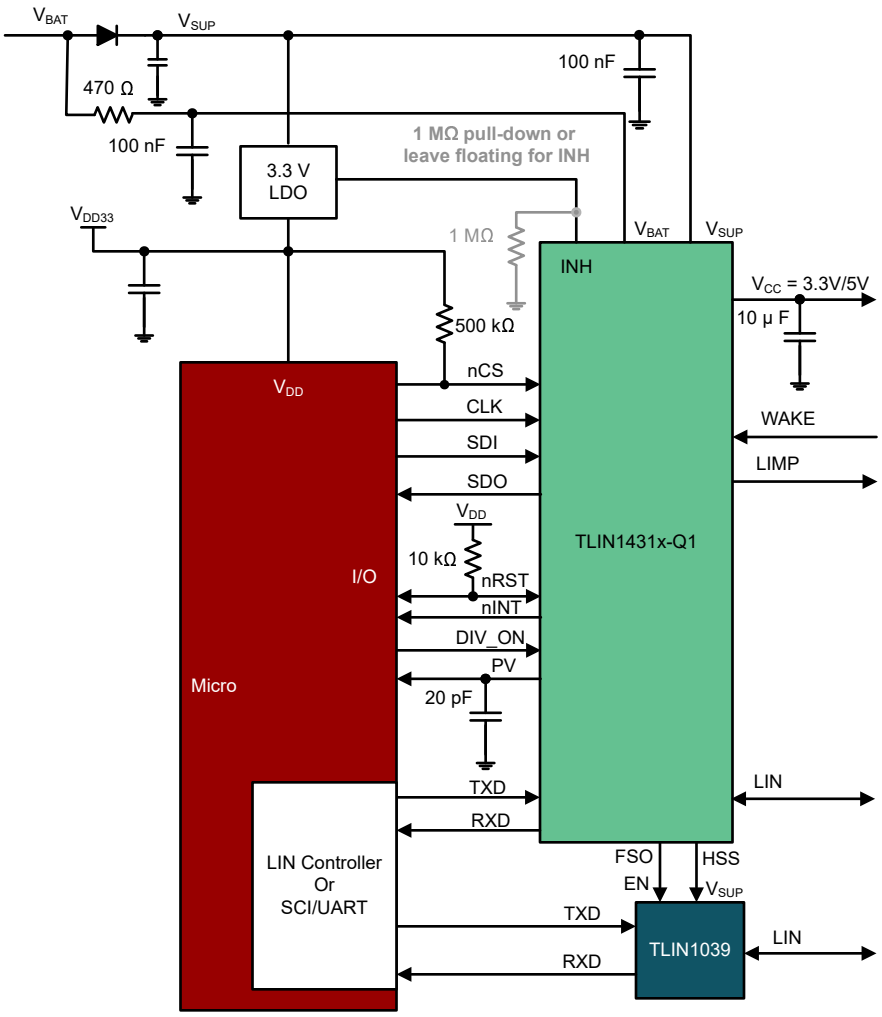


図 8-19. Channel Expansion: LIN Transceiver

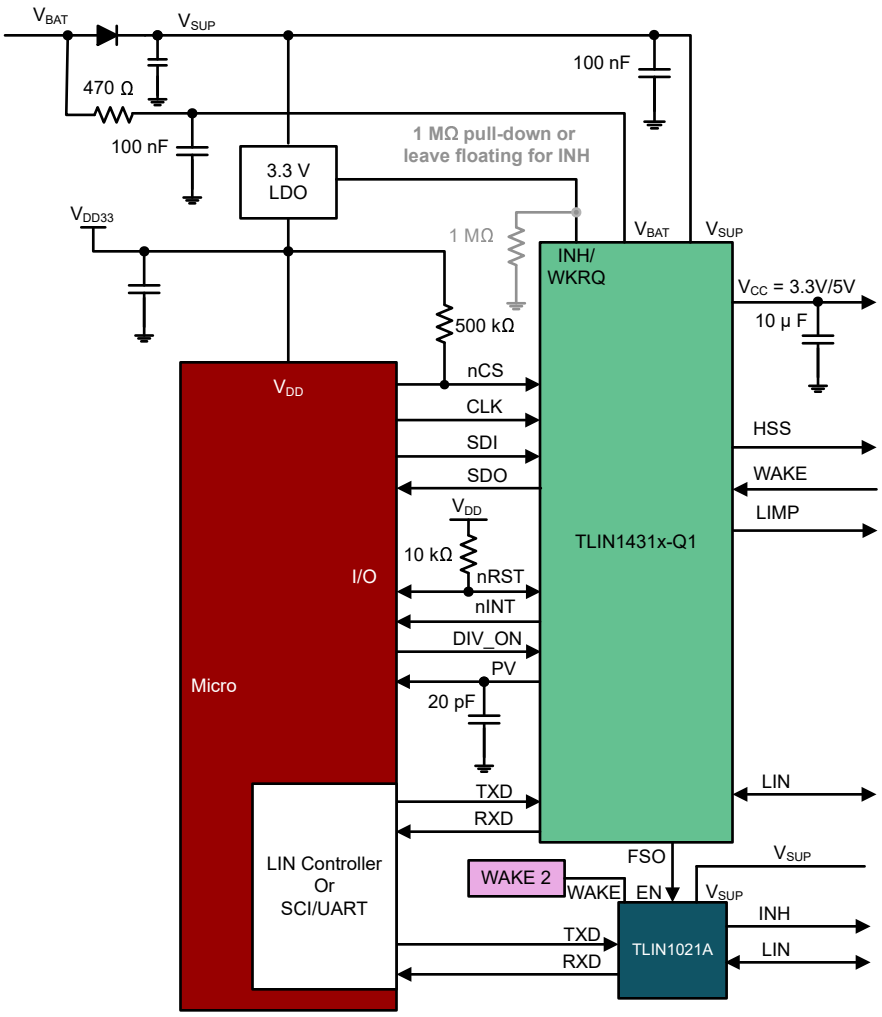


図 8-20. Channel Expansion: Enhanced LIN Transceiver

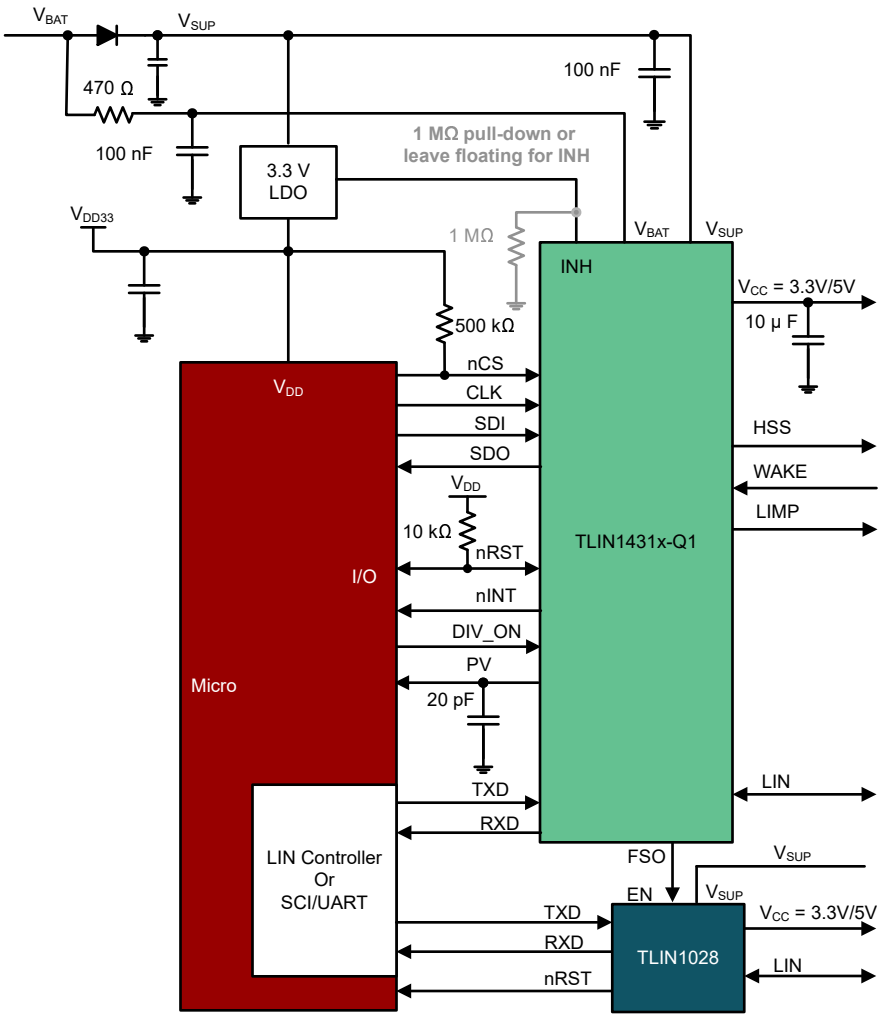


図 8-21. Channel Expansion: LIN SBC

8.3.23.2 Channel Expansion for CAN Transceiver

It is possible to add an external CAN transceiver or general purpose CAN SBC. For a simple CAN transceiver, the 5 V VCC from the TLIN14315-Q1 can power the external transceiver. When the TLIN14315-Q1 enters sleep mode the LDO is turned off which turns off the 5 V to the transceiver. There are other instances that this can take place depending upon various fault conditions like thermal shut down. Using the 3.3 V version of the device can power a 3.3 V CAN transceiver. If an external general purpose SBC is used, VCC can be used to power up other components as the SBC will also receive its input power from V_{SUP}. The FSO pin when configured as a general-purpose output pin is used as the STB/nSTB/S control pin in order to control the mode of the external CAN transceiver or SBC.

- Register 8'h29[3:1] = 110b sets the FSO pin as a general-purpose output pin EN/STB/nSTB/S pin.
- Register 8'h29[4] sets the level of the FSO pin and can be connected to the external CAN transceiver or SBC STB/nSTB/S pin.

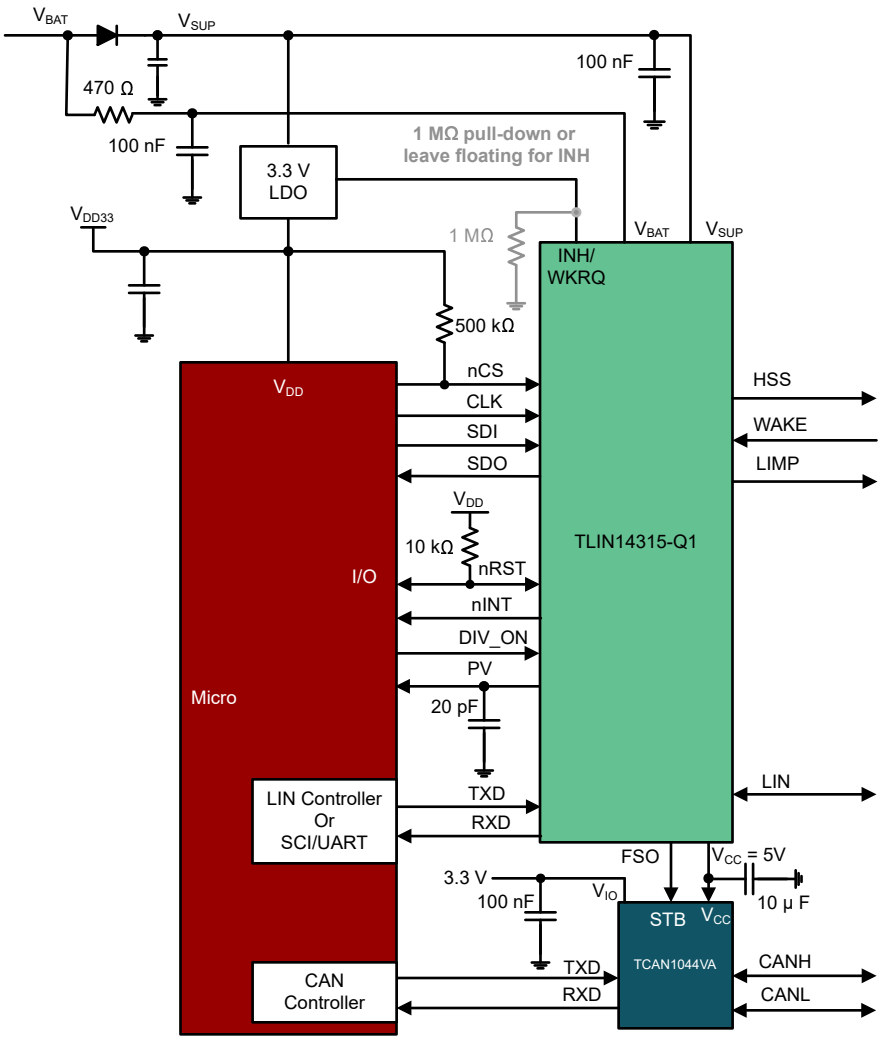


図 8-22. Channel Expansion: CAN Transceiver

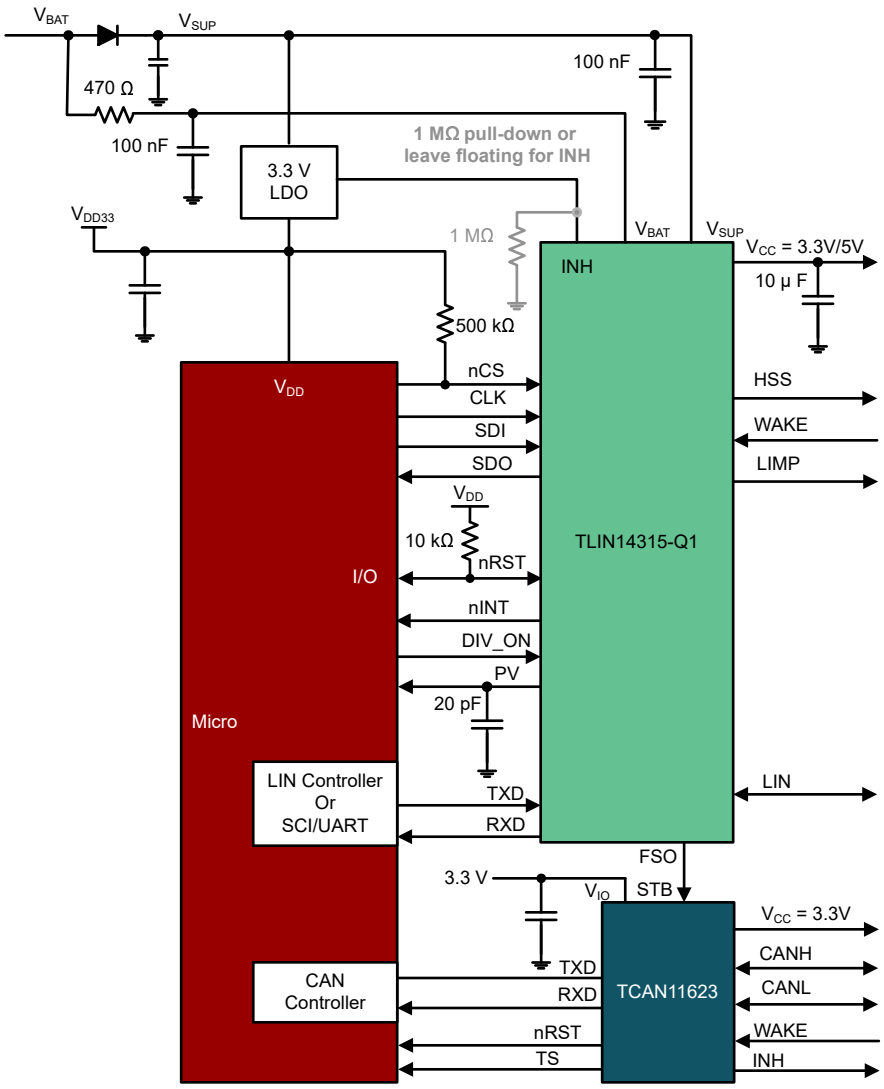


図 8-23. Channel Expansion: CAN SBC

8.4 Device Functional Modes

The TLIN1431x-Q1 has multiple functional modes of operation, Init, pin/SPI Init, normal, standby, sleep, restart and fail-safe. The next sections describe these modes as well as how the device moves between the different modes. 図 8-24 and 図 8-25 graphically shows the relationship while 表 8-4 and tables show the state of pins in each control mode. Upon power up, and once V_{CC} ≥ UV_{CC} prior to t_{INACT_FS} timing out the device enters an initialization mode (INIT). While in this mode, V_{CC} is ramping, nRST ramps with V_{CC}, all other pins are off except for monitoring the state of the Pin/nCS pin to determine which control method is being implemented. Once the control method is determined, the device follows the pin control or SPI control path of the state diagram.

表 8-4. Operating PIN Mode

Function	Restart Mode	Sleep Mode	Standby Mode	Normal Mode	Fail-safe Mode	Fast Mode
EN	NA	Low	Low	High	NA	Pulse then high
RXD	High	Floating	Low for a wake event and power up event otherwise high	Mirrors LIN bus	Floating	Mirrors LIN bus
LIN BUS Termination	Weak current pull-up	Weak current pull-up	45 kΩ (typical)	45 kΩ (typical)	Weak current pull-up	45 kΩ (typical)
Vbat Voltage Divider	Off	Off	On	On	Fault dependent	On
Transmitter	Off	Off	Off	On	Off	On (Slope control off)

表 8-4. Operating PIN Mode (continued)

Function	Restart Mode	Sleep Mode	Standby Mode	Normal Mode	Fail-safe Mode	Fast Mode
Watchdog	Off	Off	On with long first pulse	On	Off	On but only sets flag
nRST Pin	Low	Low	High	High	LDO state dependent	High
WAKE Pin	Off	On	On	Off	On	Off
WKRQ/INH	On	Off	On	On	INH - On; WKRQ - Fault dependent	On
LIMP	• Same as previous state when due to a WD fault • Turns off when exiting fail-safe mode due to any other fault	Off	Previous state prior to entering STBY due to WD fault	Previous state prior to entering normal mode due to WD fault	On	Previous state prior to entering fast mode due to WD fault
HSS	Off	Off	On and controlled by HSSC pin	On and controlled by HSSC pin	Off	On and controlled by HSSC pin
V_{CC}	Ramping	Off	On	On	Fault dependent	On
Comment		nRST is internally connected to the LDO output which in sleep mode is off	Wake up event detected, waiting on processors to set EN	LIN transmission up to 20 kbps	LDO off for TSD, V_{CCSC} or OV_{CC} events	LIN transmission up to 200 kbps

注

LDO state for fault dependent in fail-safe mode is as follows:

- Watchdog error - On
- Thermal shut down - Off
- UV_{CC} - On
- OV_{CC} over-voltage - Off
- V_{CCSC} - Off
- Restart counter exceeded - On
- SWE timer expiration - On

If TXD is held dominant when device enters normal or fast modes, the LIN transmitter does not turn on until the TXD pin goes recessive.

If V_{SUP} is ≤ UV_{SUP} WKRQ/INH is off.

WKRQ depends upon the LDO being on, so any event that causes the LDO to be turned off will turn off WKRQ.

Any WD failure in Fast Mode will only set interrupt and not take any other action (will not set LIMP, transition to Fail-safe or Restart or take any WD fail action)

- nRST depends upon the LDO state. When LDO is on, nRST reflects the LDO value.
  - When LDO is on, nRST reflects the LDO or I/O voltage value except for a UV_{CC} event where nRST is low.
  - When LDO is off, nRST is low.

表 8-5. Operating SPI Mode

Function	Restart Mode	Sleep Mode	Standby Mode	Normal Mode	Fail-safe Mode	Fast Mode
RXD	High	Floating	Low for a wake event and power up event otherwise high	Mirrors LIN bus	Fault dependent	Mirrors LIN bus
LIN BUS Termination	Weak current pull-up	Weak current pull-up	45 kΩ (typical)	45 kΩ (typical)	Weak current pull-up	45 kΩ (typical)
Vbat Voltage Divider	Off	Off	On	On	Fault dependent	On
Transmitter	Off	Off	Off	On	Off	On (Slope control off)

表 8-5. Operating SPI Mode (continued)

Function	Restart Mode	Sleep Mode	Standby Mode	Normal Mode	Fail-safe Mode	Fast Mode
Watchdog	Off	Off	Default on with long first window but programmable off	On If programmed off in standby mode when entering normal mode a long first window is implemented	Off	On but only sets flag
SPI pins	Off	Off	On	On	Fault dependent	On
nINT pin	Off	Off	On	On	Fault dependent	On
nRST pin	Low	Low	High	High	LDO state dependent	High
WAKE Pin	Off	On	On	Off	On	Off
WKRQ/INH	On	Off	On	On	INH - On; WKRQ - Fault dependent	On
LIMP	• Same as previous state when due to a WD fault • When exiting fail-safe mode due to any other fault how 8'h1A[3:2] is programmed determines how LIMP is cleared	Off	Previous state prior to entering STBY due to WD fault	Previous state prior to entering normal mode due to WD fault	On	Previous state prior to entering fast mode due to WD fault
HSS	Off	Off unless cyclic sensing enabled	On	On	Off	On
V_{CC}	Ramping	Off	On	On	Fault dependent	On
Comment		nRST is internally connected to the LDO output which in sleep mode is off	Wake up event detected, waiting on processors	LIN transmission up to 20 kbps	LDO off for TSD, V_{CCSC} or OV_{CC} events	LIN transmission up to 200 kbps

注

Function status when in fail-safe mode that states fault dependent are defined in 表 8-6

If TXD is held dominant when device enters normal or fast modes, the LIN transmitter does not turn on until the TXD pin goes recessive.

If V_{SUP} is ≤ UV_{SUP} WKRQ/INH is off.

WKRQ depends upon the LDO being on, so any event that causes the LDO to be turned off will turn off WKRQ.

Any WD failure in Fast Mode will only set interrupt and not take any other action (will not set LIMP, transition to Fail-safe or Restart or take any WD fail action)

表 8-6. Fault Dependent States In Fail-safe Mode

Function	Watchdog Error	Thermal Shutdown	UV_{CC}	V_{CC} Over Voltage	V_{CCSC}	Restart Counter Exceeded
LDO (2)	On	Off	On	Off	Off	On (1)
INH	Programmed	On	On	On	On	On
WKRQ	Programmed	Off	Off	Off	Off	On
SPI	On	Off	On	Off	Off	On

(1) LDO is on in fail-safe mode if the restart counter causes the change when fail-safe mode is enabled.
(2) LDO is on in fail-safe mode if the SWE timer times out causing the device to enter fail-safe mode if enabled.

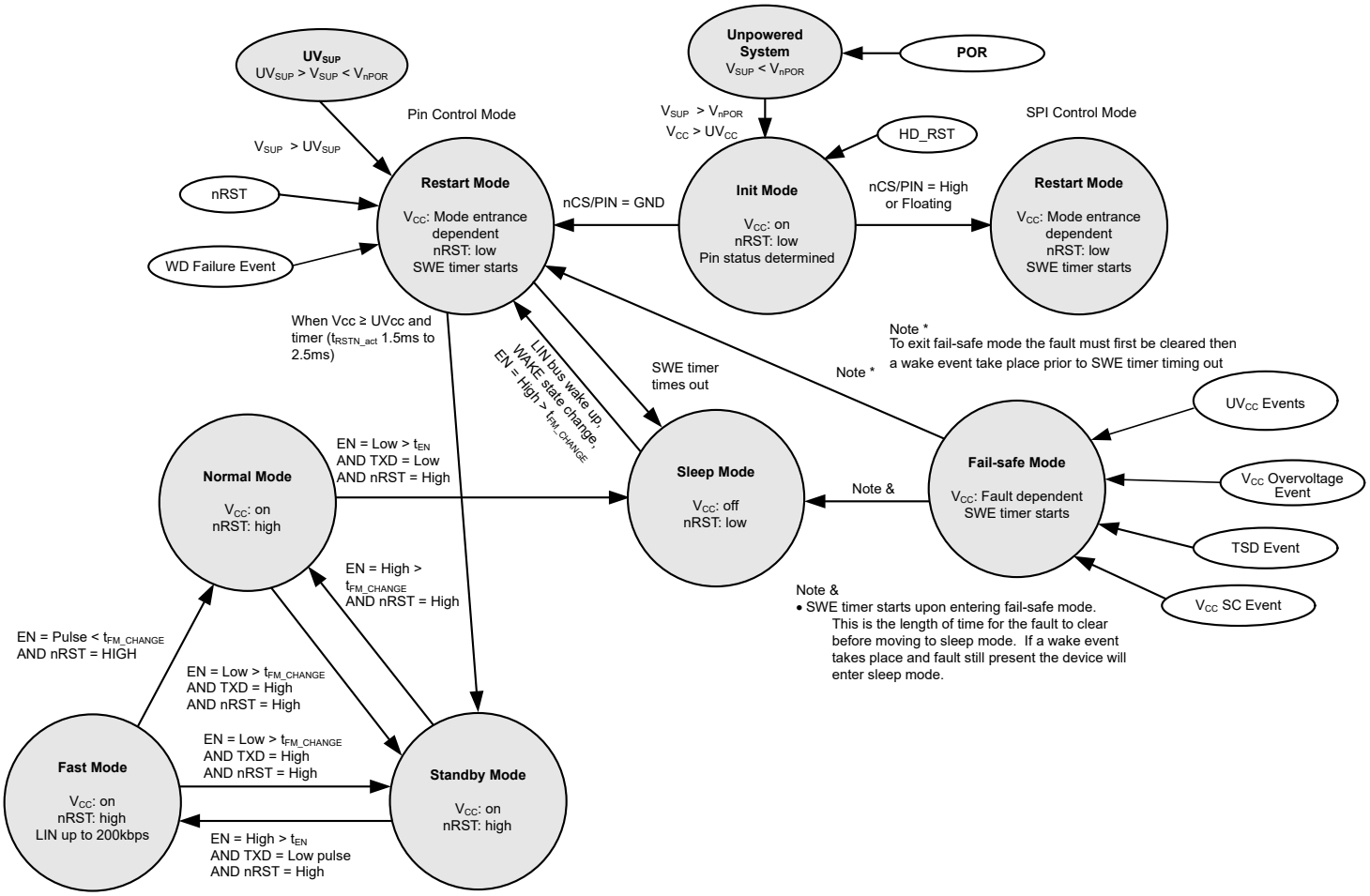


図 8-24. Pin control state diagram

注

Normal mode can be entered from Fast mode with TXD in either state:

- TXD = high, EN = pulse < t_{FM_CHANGE} and nRST = high
- TXD = low, nRST = high and EN pulse can be any width

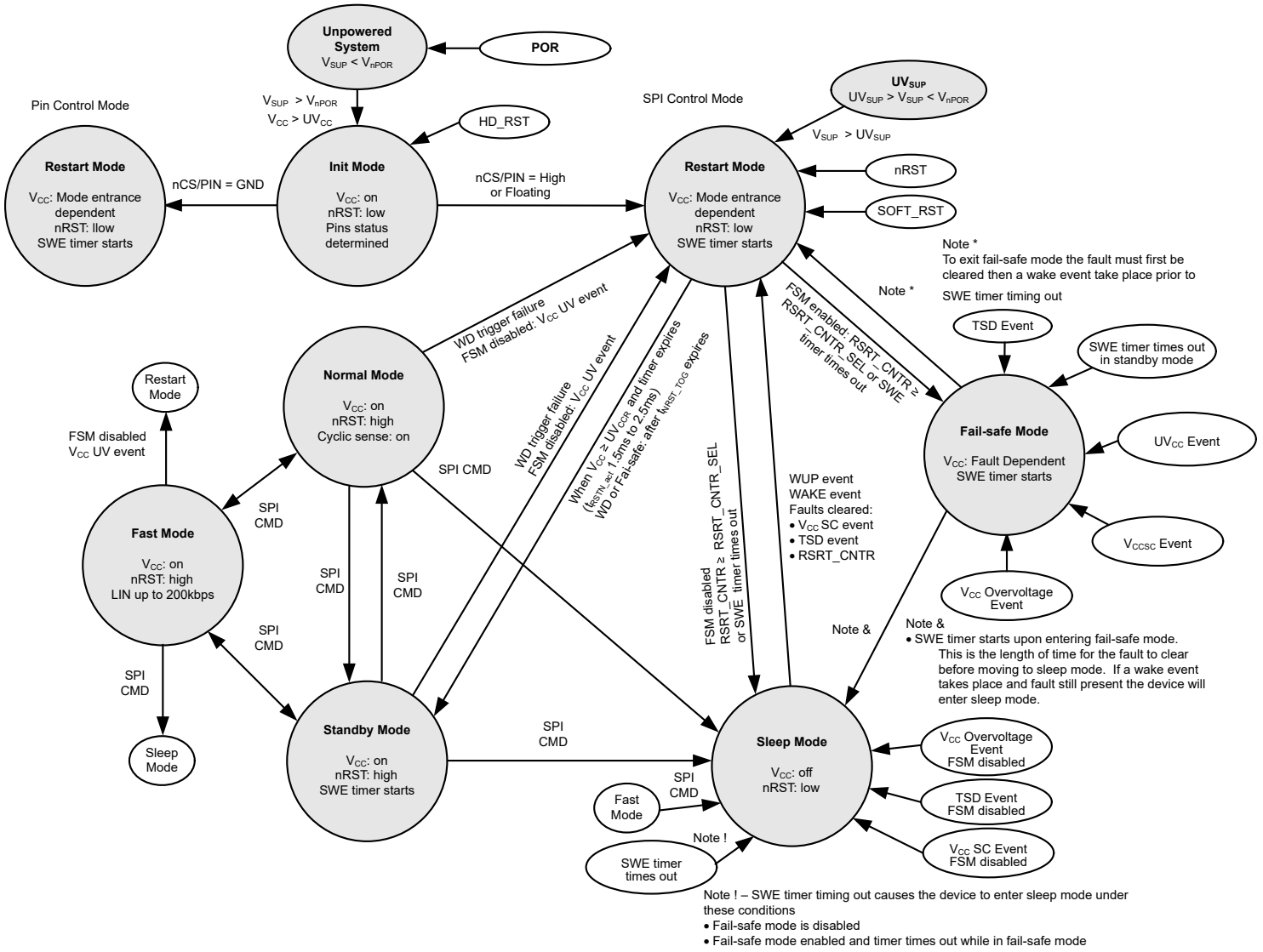


図 8-25. SPI control state diagram

8.4.1 Init Mode

This is the initial mode of operation upon powering up. This is a transitional mode that is entered once V_{CC} ≥ UV_{CC}. The device is in this mode for ≤ 350 µs as it determines the states of pin 7, PIN/nCS and pin 16, WKRQ/INH; see 図 8-5 and 図 8-6. The V_{CC} fault monitoring will be active to determine if there is a TSD, OV_{CC} or V_{CCSC} faults which takes approximately 2.5 ms. If one of these faults are detected, the device will perform as described in セクション 8.3.22.5 and セクション 8.3.22.9.1. If V_{CC} < UV_{CC}, The device will remain in Init mode until V_{CC} > UV_{CC}. If a fault takes place that keeps the device from determining the state of the pins, the device will default to pin control.

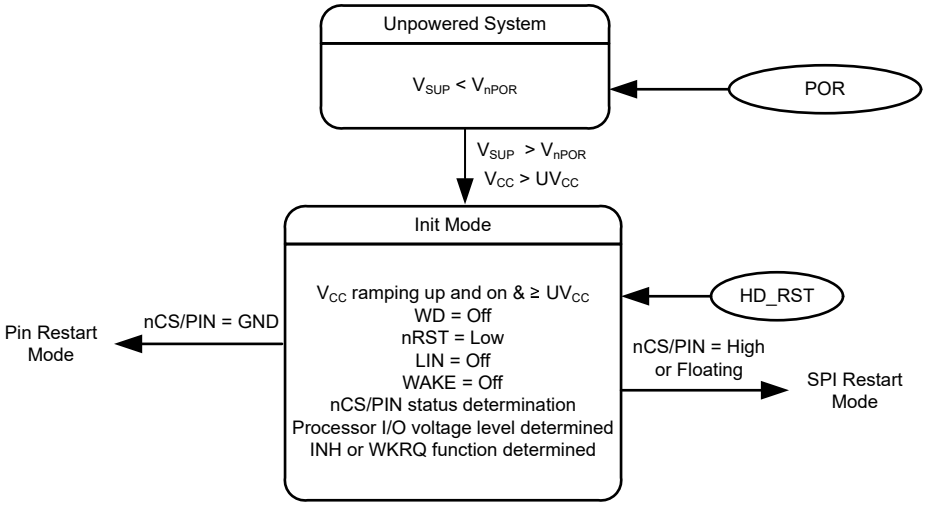


図 8-26. Init Mode

8.4.2 Normal Mode

In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominant signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. When entering normal mode, it takes t_{MODE_CHANGE} before data on RXD pin reflects the LIN bus. Normal mode can be entered from Fast mode and standby mode. See 図 8-24 for the conditions necessary to enter normal mode when in pin control.

In SPI control mode, Normal mode is entered by SPI commands at register 8'h1D[7:6] = 10b. See 図 8-25 for the conditions necessary to enter normal mode when in pin control.

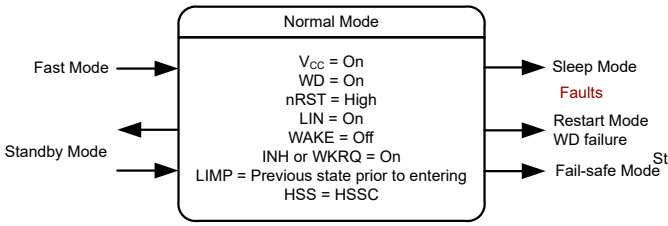


図 8-27. Normal Mode Pin Control

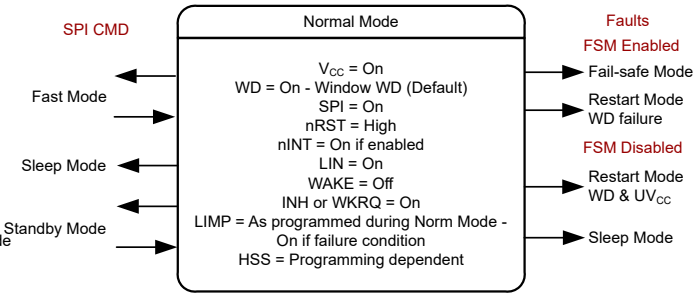


図 8-28. Normal Mode SPI Control

8.4.3 Fast Mode

Fast mode removes the slope control for the LIN transmitter allowing the LIN bus to support data rates up to 200 kbps. Fast mode is also the system software programing mode and debug mode. The watchdog is active but only indicates a WD failure and does not cause any resets or mode changes. Fast mode can be entered in either SPI or pin control modes. In SPI mode it is entered from normal or standby modes. In pin mode, it can be entered from standby mode. To enter fast mode from standby, the EN pin must be high with a high-low-high pulse on the TXD pin of duration t_{FMTXD} takes place prior to t_{FM_CHANGE} timing out, see 図 8-31. In pin control mode, to leave fast mode the enable pin and TXD pins are used. If TXD pin is high and the EN pin is pulsed from high too low too high for t_{FM_CHANGE}, the device enters standby mode, see 図 8-32. If the EN pin is pulsed high too low too high with the pulse being < t_{FM_CHANGE}, the device enters normal mode, see 図 8-33.

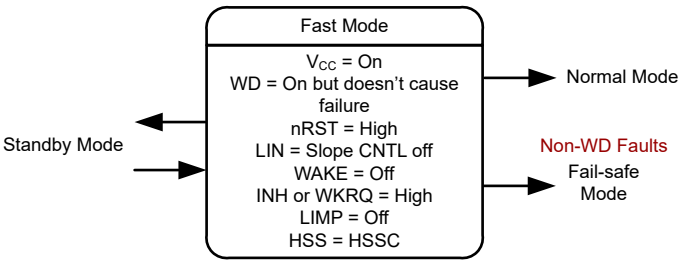


図 8-29. Fast Mode Pin Control

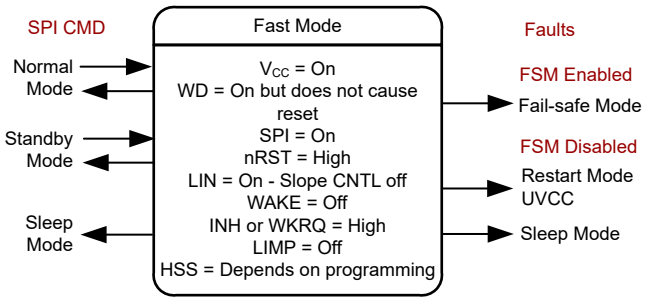


図 8-30. Fast Mode SPI Control

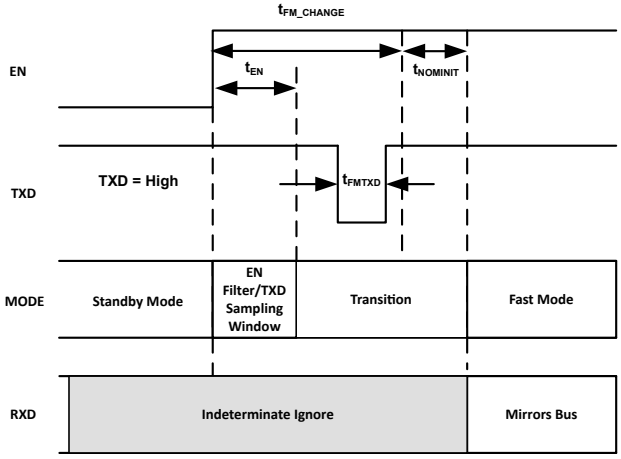


図 8-31. Entering Fast Mode from Standby Mode

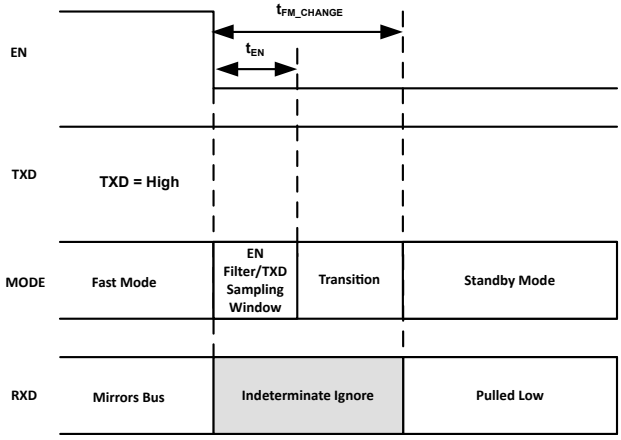


図 8-32. Exiting Fast Mode to Standby Mode

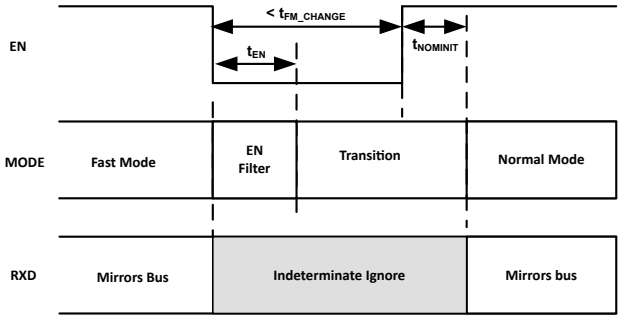


図 8-33. Exiting Fast Mode to Normal Mode

8.4.4 Sleep Mode

Sleep Mode is the power saving mode for the TLIN1431x-Q1. Even with extremely low current consumption in this mode, the device can still wake up from the LIN bus through a wake up signal or local wake via WAKE pin. Upon a wake event the SWE timer, t_{INACT_FS}, starts and the device enters restart mode. If UV_{CC} is still present after this time, the device re-enters sleep mode. The LIN bus is filtered to prevent false wake up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

In pin control mode, sleep mode is entered by setting EN low for longer than t_{EN} and TXD pin is low when entered from normal mode.

In SPI control mode, setting register 8'h1D[7:6] = 01b transitions the device into sleep mode. If the reset counter exceeds three, the device enters sleep mode from restart mode. The reset counter increments on an UV_{CC} event, or a watchdog error event that causes the device to enter restart mode when fail-safe mode is disabled. The reset counter must be cleared through a SPI command.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- LIN wake up receiver is active.
- WAKE pin is active.

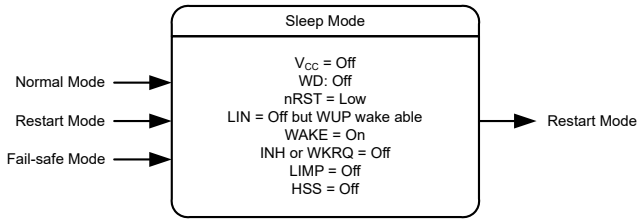


図 8-34. Sleep Mode Pin Control

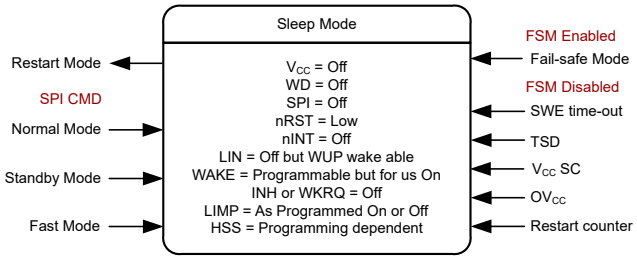


図 8-35. Sleep Mode SPI Control

8.4.5 Standby Mode

This mode is entered from various other modes based upon which control method is implemented, the pin control 図 8-24 or SPI control 図 8-25. The LIN bus responder node termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See *Standby Mode Application Note* for more application information.

When EN (in Pin Control Mode) is set high for longer than t_{FM_CHANGE} while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

During power up, the device automatically enters standby mode from restart mode. EN has an internal pull-down resistor ensuring EN is pulled low if the pin is left floating in the system.

In both pin and SPI modes, the watchdog is default on in standby mode. There is a long timeout initial window that is t_{INITWD} that a WD trigger event must take place. In SPI mode, watchdog can be disabled when entering standby mode except for cases that the device has had a POR event.

The device automatically enters standby mode from restart mode when $V_{CC} \geq UV_{CC}$ and t_{RSTN_act} time has expired. When in SPI communication mode, the TLIN1431x-Q1 can enter standby mode by writing a 00 to register 8'h1D[7:6] from normal or fast modes. The watchdog function is default on in standby mode. When using SPI to configure the device, the watchdog function can be configured.

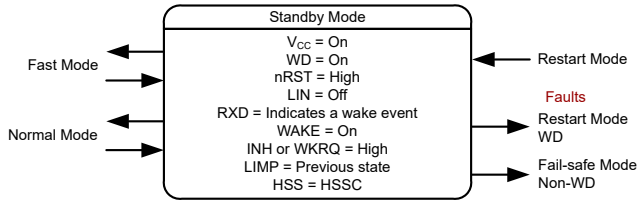


図 8-36. Standby Mode Pin Control

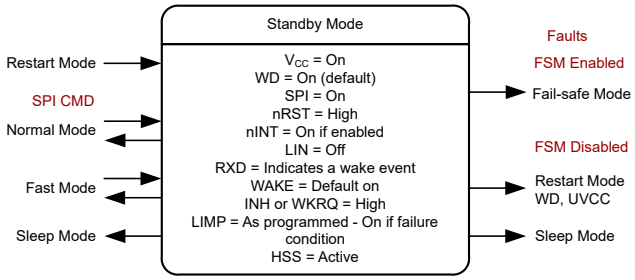


図 8-37. Standby Mode SPI Control

8.4.6 Restart Mode

Restart mode is a transitional mode. This mode can be entered from any of the other modes depending upon whether fail-safe mode is disabled. In this mode, the LDO is ramping when coming from sleep mode or fail-safe mode where the LDO was turned off, like a TSD event. Once V_{CC} ≥ UV_{CC} for t_{RSTN_act} (~2 ms), the device enters standby mode. While in restart mode, the nRST pin is latched low. Each time restart mode is entered the restart mode counter is incremented.

注

The SWE timer starts when the device enters restart mode. If the SWE timer times out, the device enters fail-safe mode. If fail-safe mode is disabled, the device enters sleep mode.

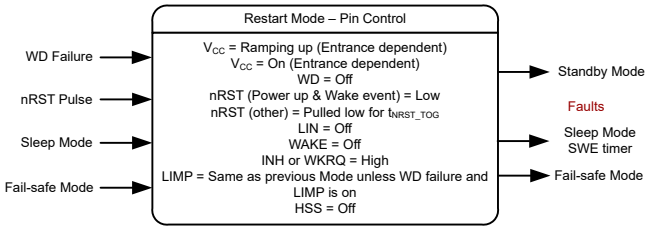


図 8-38. Restart Mode Pin Control

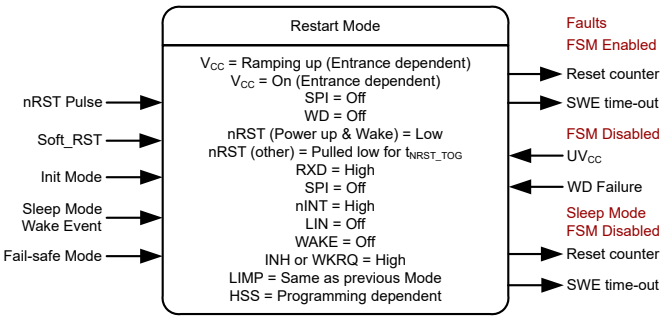
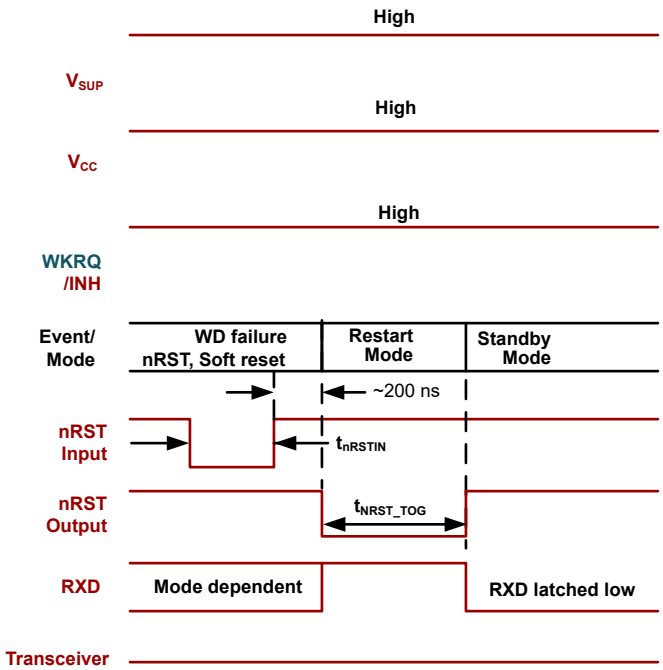


図 8-39. Restart Mode SPI Control



注

- A watchdog failure, soft reset or nRST event resets t_{NRST_TOG} to default value of typically 2 ms
- The typical time between the release of a nRST input pulse for device to enter restart mode is ~ 200 ns

図 8-40. Entering Restart Mode

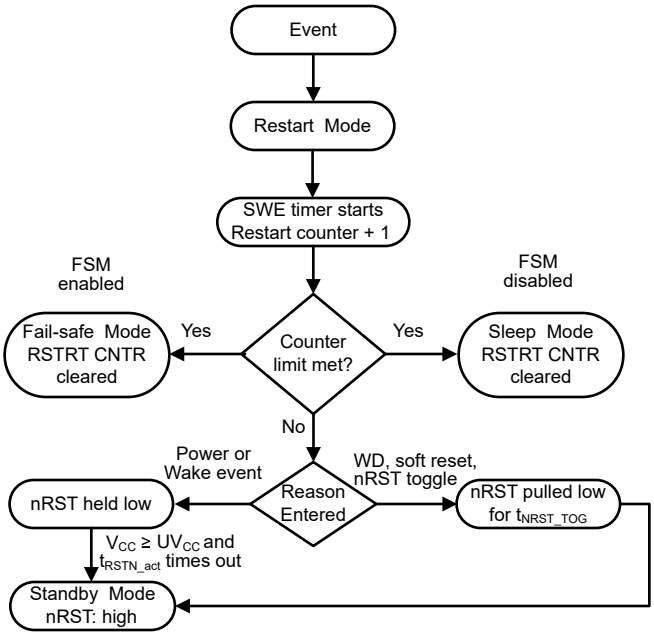
8.4.6.1 Restart Counter

This counter is programed by register 8'h28[7:4] which sets the number of times restart can be entered before transitioning to sleep or fail-safe mode, up to 14 times but should be programmed for greater than 1 to avoid possible loops. The default value is 4. Register 8'h28[3:0] is the counter. To prevent the transition to sleep or fail-safe mode, the counter should be cleared periodically. Entering sleep mode or fail-safe mode due to a meeting the restart counter automatically clears the restart counter.

8.4.6.2 nRST Behavior in Restart Mode

The nRST output pin behavior depends upon the reason the device entered restart mode. When entered from other modes due to a watchdog failure, soft reset or an external nRST toggle, the nRST pin is pulled low for t_{nRST_TOG} which is a default pulse width of 2 ms. This pulse width can be configured to 15 ms by changing register 8'h29[5] = 1b. In pin control, the pulse width on nRST is always nominally 15 ms for a watchdog failure. Once the timer expires, the device enters standby mode. From power up, sleep and certain fail-safe modes, the nRST behaves like the UV_{CC} event, pulling nRST low until V_{CC} > UV_{CC} and t_{RSTN_act} times out. See 図 8-41 on how the nRST pin behaves when entering restart mode.

The nRST pin is also a TLIN1431x-Q1 reset input which transitions the device into restart mode when the pin is pulled low for t_{nRSTIN}.



Note:
1. Wake event means entered from sleep or fail-safe modes
2. If SWE timer times out device will enter sleep or fail-safe mode
3. nRST toggle reason is an external toggle of nRST pin to reset device
4. A soft reset or external nRST toggle will reset t_{NRST_TOG} to default value, typically 2 ms

図 8-41. nRST Behavior in Restart Mode

8.4.7 Fail-safe Mode

When the TLIN1431x-Q1 has certain fault conditions, the device enters a fail-safe mode (FSM). This feature can be disabled in SPI control mode, but is always on in pin control mode. This mode turns on LIMP and brings all other function into lower power mode states. Fault conditions are over-voltage on V_{CC}, thermal shutdown, V_{CC} under-voltage events and reaching restart counter limit in SPI control mode. When entering FSM, a fail-safe mode counter is incremented. The counter limit is set at register 8'h18[7:4], FSM_CNTR_SET and should be set to greater than 1. To avoid unwanted actions the counter should be cleared by writing 0h to 8'h18[3:0]. If the limit is reached a programmed action will be executed, register 8'h17[7:4], FSM_CNTR_ACT. Once the fault conditions are cleared, the device can be put back into restart mode from a wake event. If a fault condition is still in effect after the wake event the device enters sleep. If no wake event takes place, the device enters sleep mode after the programmed SWE timer, t_{INACT_FS}, times out.

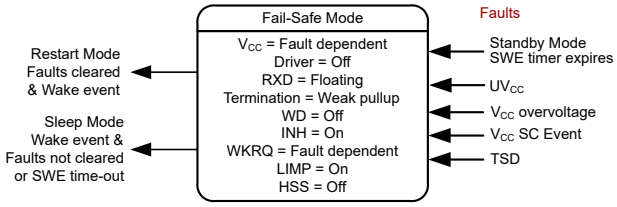


図 8-42. Fail-safe Mode Pin Control

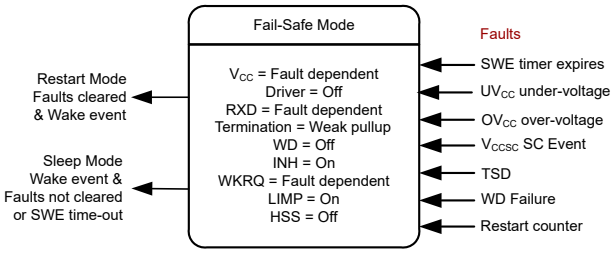


図 8-43. Fail-safe Mode SPI Control

注

When the device enters fail-safe mode, the SWE timer automatically starts.

- If SWE timer times out, the device enters sleep mode
- If a wake event takes place prior to the SWE timer timing out, the device determines if fault is still present.
  - If fault is present, the device enters sleep mode.
  - If fault has cleared, the device enters restart mode.

When fail-safe mode is entered due to a thermal shutdown (TSD), V_{CC} over-voltage (OV_{CC}) or a V_{CC} short circuit (V_{CCSC}) event the following takes place:

- LDO is turned off
- If the device receives a wake event, the LDO is turned on for t_{LDOON} to determine if the TSD, OV_{CC} or V_{CCSC} event is still present.
  - During this window, if a TSD or OV_{CC} is detected the device immediately enters sleep mode.
  - At the end of t_{LDOON} window, if a V_{CCSC} is detected the device enters sleep mode.
- If fault is cleared, the device enters restart mode.

  If the device enters fail-safe mode and V_{CC} is on, the t_{LDOON} timer is started and expires before the device transitions to restart mode.

8.4.8 Wake Up Events

There are three ways to wake-up from sleep mode depending upon control mode, pin or SPI:

1. Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake-up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground. Active for both pin and SPI control modes.
2. Local wake up through EN being set high for longer than t_{MODE_CHANGE}. Active for pin control mode.
3. Local wake up through WAKE pin
   - Being set high or low for longer than t_{MODE_CHANGE}. Active for both pin and SPI mode.
   - Only active during on-time cyclic sense period. Active for SPI mode.

注

- Remote and local wake up are also valid wake events when the device enters fail-safe mode. The EN pin will not wake the device if it has entered fail-safe mode.
- When a wake event takes place and INH is selected, it is turned on with in t_{INH_SLP}.
- When WKRQ is used, a wake event requires the LDO to be on and the voltage level to exceed 2 V. Once this happens, the WKRQ pin ramps with V_{CC} until it expected voltage level.

8.4.8.1 Wake Up Request (RXD)

When the TLIN1431x-Q1 encounters a wake up event from the LIN bus the device transitions to restart mode. In restart mode, the LDO is turned on and ramps until $V_{CC} > UV_{CC}$ at which time the device enters either Normal mode, Fast mode or Standby mode depending upon the device control method. In Restart mode, RXD is pulled high. After V_{CC} has exceeded UV_{CC} for t_{RSTN_act}, the device transitions to standby mode and RXD is latched low. Once the device enters normal mode, the $\overline{RXD}$ pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus. RXD can be programmed to toggle low or high when in standby mode from a wake event.

8.4.8.2 Local Wake Up (LWU) via WAKE Terminal

The WAKE terminal is a ground referenced input terminal supporting high voltage wake inputs used for local wake up (LWU) request via a voltage transition. The terminal triggers an LWU event on either a low to high or high to low transition as it has bi-directional input thresholds. This terminal may be used with a switch to VSUP

or ground. If the terminal is not used it should be pulled to ground to avoid unwanted parasitic wake up events. There are two methods for using the WAKE pin:

1. Static wake
2. Cyclic sensing wake

8.4.8.2.1 Static WAKE

The WAKE terminal defaults to bi-directional input but can be configured for rising edge and falling edge transitions by using register 8'h11[7:6] WAKE_CONFIG (see 図 8-44 and 図 8-45). Once the device enters sleep mode the WAKE terminal voltage level needs to be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input can be determined. A pulse width less than $t_{WAKE\_INVALID}$ is filtered out.

The LWU circuitry is active in sleep mode, standby and fail-safe modes. If a valid LWU event occurs, the device transitions to restart mode. The LWU circuitry is not active in normal, fast and restart modes. To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of t_{WAKE}. A constant low level on WAKE has an internal pull-down to ground. On power up, this may look like a LWU event and could be flagged as such. The device provides a WAKE pin status change update using register 8'h11[5:4]. The status change will lock in a change in the WAKE pin and needs to be cleared.

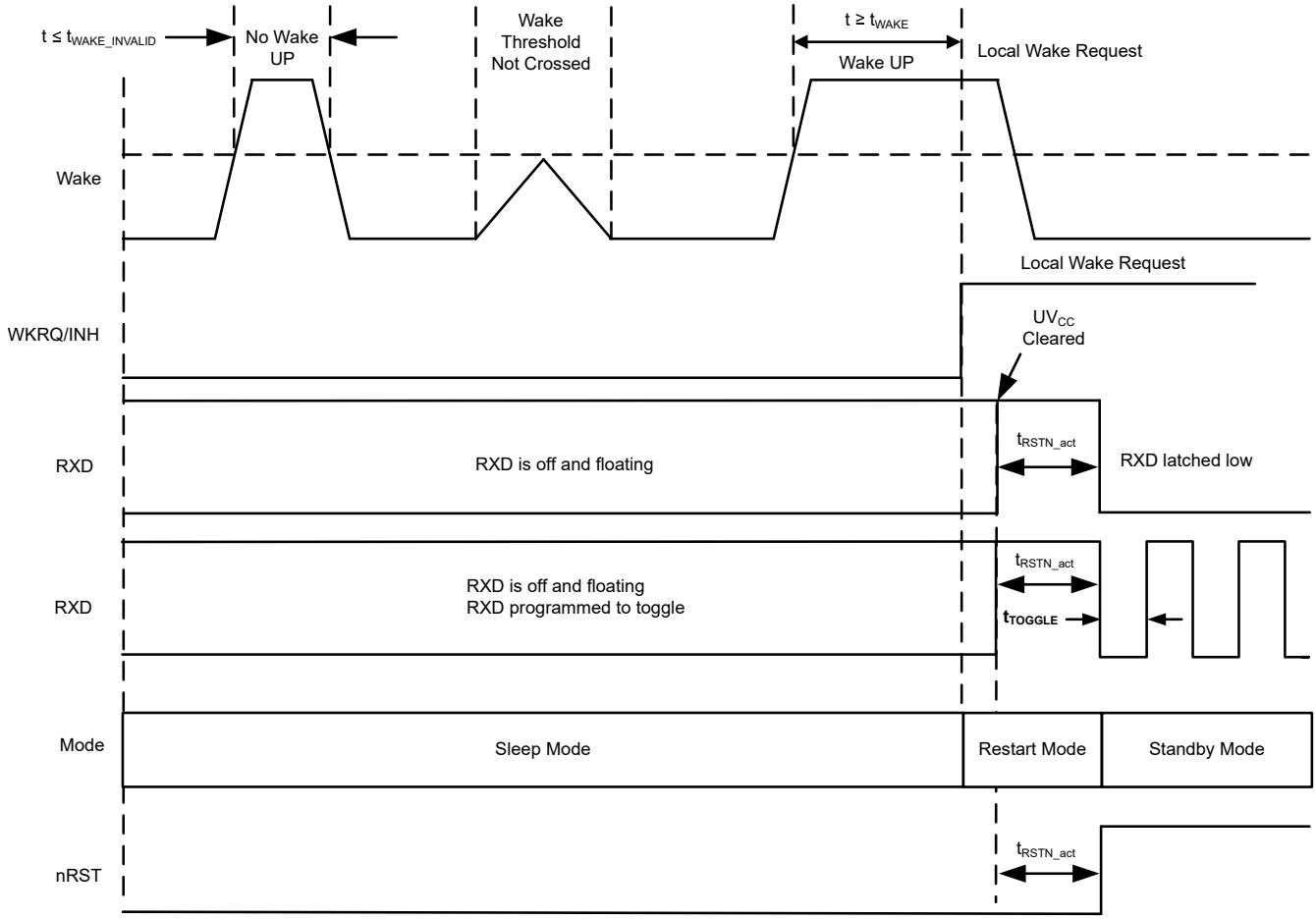


図 8-44. Local Wake Up (LWU) - Rising Edge

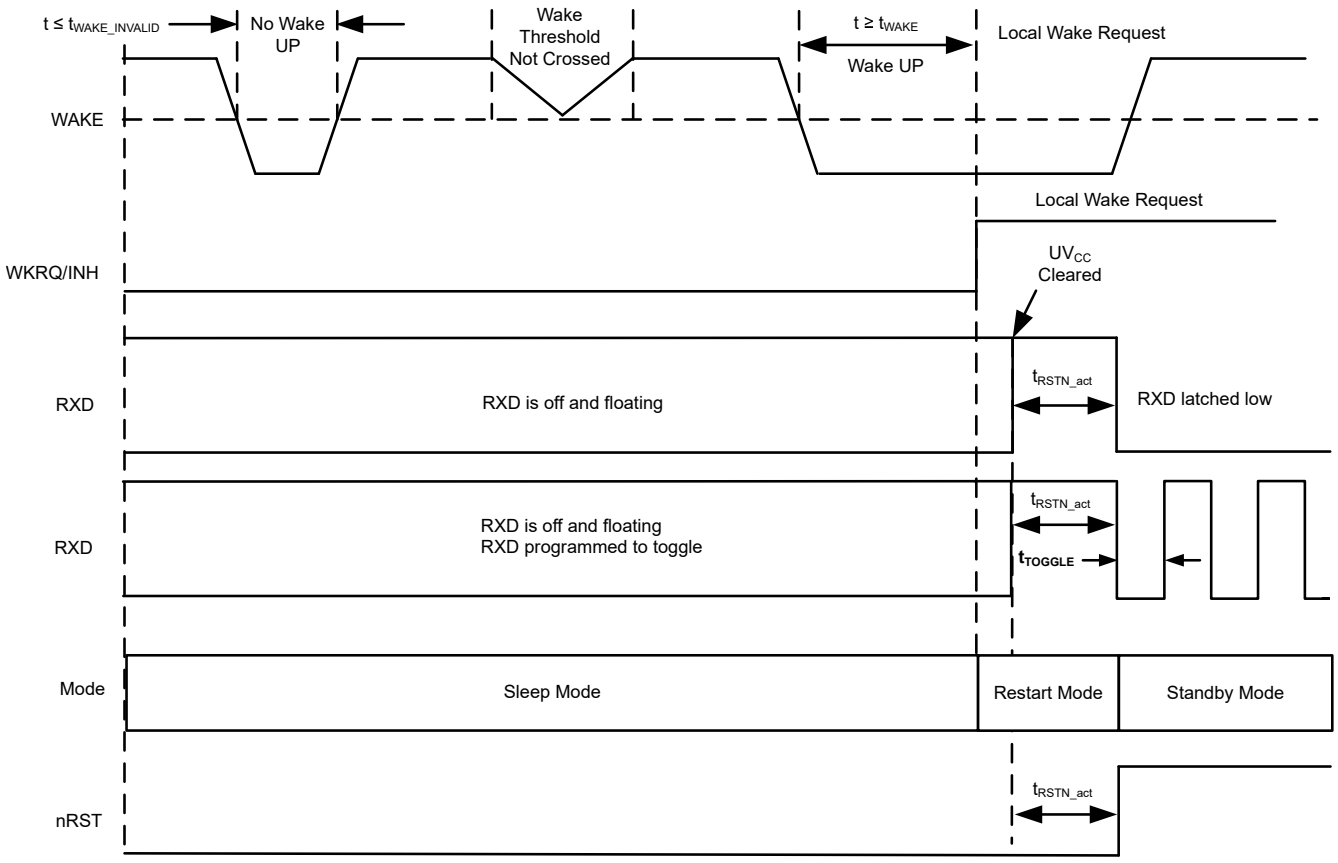


図 8-45. Local Wake Up (LWU) - Falling Edge

注

These figures show the state of the RXD pin after a WAKE pin event. The transition to standby mode is shown in the state diagrams but is based upon the following:

- PIN Mode: All must take place
  - WAKE pin event recognized
  - V_{CC} goes above UV_{CC} for > t_{RSTN_act}
  - EN pin is High for > t_{EN}
- SPI Mode: All must take place
  - WAKE pin event recognized
  - V_{CC} goes above UV_{CC} for > t_{RSTN_act}

The WAKE terminal can be configured for a pulse, see 図 8-46, by using WAKE_CONFIG register 11h[7:6]. The terminal can be configured to work off a pulse only. The pulse must be between $t_{WK\_WIDTH\_MIN}$ and $t_{WK\_WIDTH\_MAX}$, see 図 8-46. This figure provides three examples of pulses and whether the device will wake or not wake. $t_{WK\_WIDTH\_MIN}$ is determined by the value for $t_{WK\_WIDTH\_INVALID}$ is set to in register 8'h11[3:2]. There are two regions where a pulse may or may not be detected. By using register 8'h1B[1], WAKE_WIDTH_MAX_DIS, the pulse mode can be configured as a filtered wake input. Writing a 1b to this bit disables $t_{WK\_WIDTH\_MAX}$, and the WAKE input is based upon the configuration of register 8'h11[3:2] which selects a $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$ value. A WAKE input of less than $t_{WK\_WIDTH\_INVALID}$ is filtered out, and if longer than $t_{WK\_WIDTH\_MIN}$ INH turns on and device enters standby mode. The region between the two may or may not be counted, see 図 8-47. Register 8'h12[7] determines the direction of the pulse or filter edge that is recognized. The status of the WAKE pin can be determined from register 8'h11[5:4]. When a WAKE pin change takes place, the device registers the change as a rising edge or falling edge. This is latched until a 00b is written to the bits.

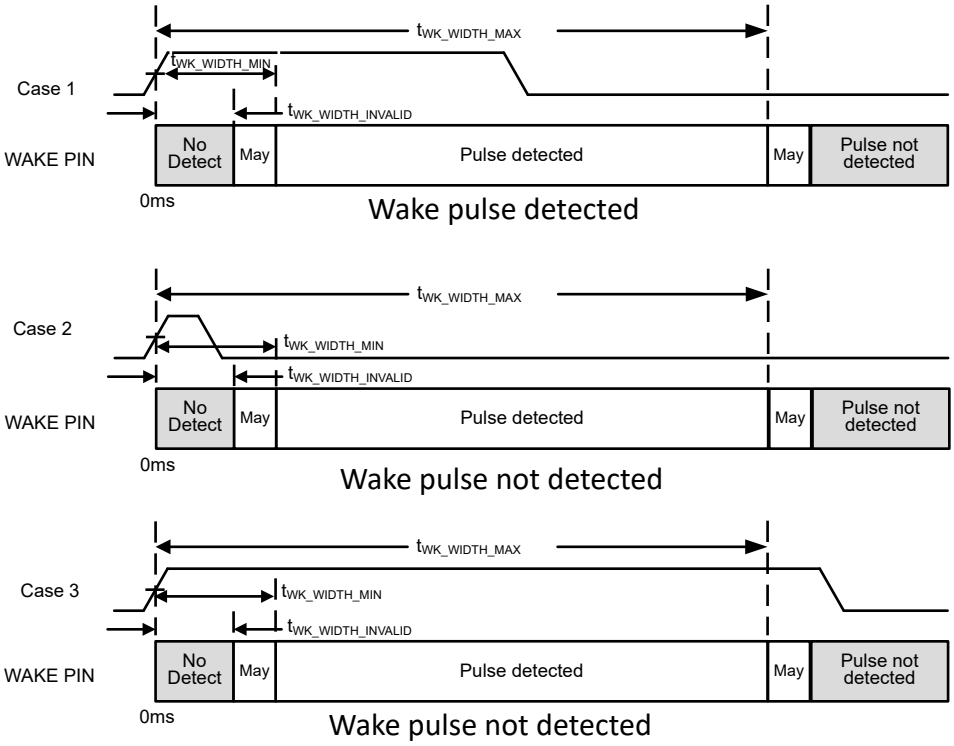


図 8-46. WAKE Pin Pulse Behavior

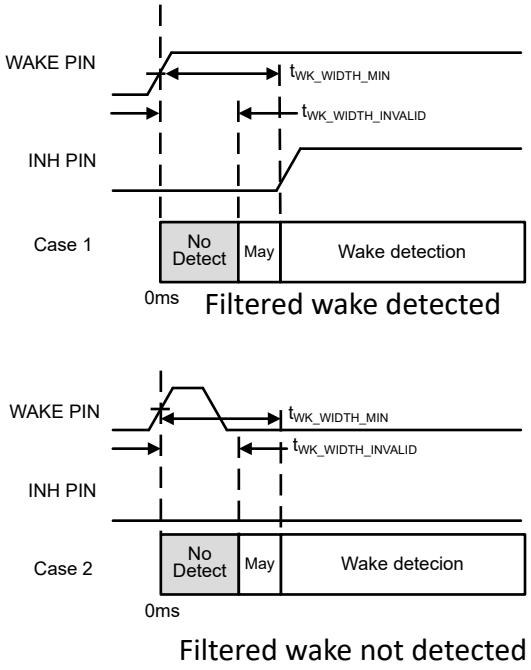


図 8-47. WAKE Pin Filtered Behavior

8.4.8.2.2 Cyclic Sense Wake

Cyclic sense wake is a method using the high-side switch with the WAKE input pin to periodically check for a WAKE pin state change in standby and sleep modes. In sleep mode, cyclic sense wake reduces the quiescent current of the device by reducing the WAKE circuitry to be active only during the on time of the HSS pin, see 図 8-48 as an example for this. Periodically, the HSS pin turns on applying V_{SUP} to the external local wake circuitry and the device samples the state of the WAKE pin. Each time the WAKE pin is sampled, the current state is

compared to the previous state. If there has been a state change, the device wakes up and transitions to restart mode; otherwise, it remains in sleep mode. See 図 8-49 for the timing diagram. In standby mode, the same process is followed for determining a state change on the WAKE pin. A state change on the WAKE pin causes the device to initiate an interrupt and the RXD pin is latched low. When entering standby or sleep mode, this process is reset with the first HSS on time being the initial WAKE pin state and does not cause a wake event.

The wake time is based upon t_{WK_CYC}, which is the sampling window, as shown in Static WAKE. This HSS period and on time are determined by setting timer1 register, 8'h25[7:0] or timer 2 register 8'h26[7:0]. The sampling window, t_{WK_CYC}, is determined by register 8'h12[5].

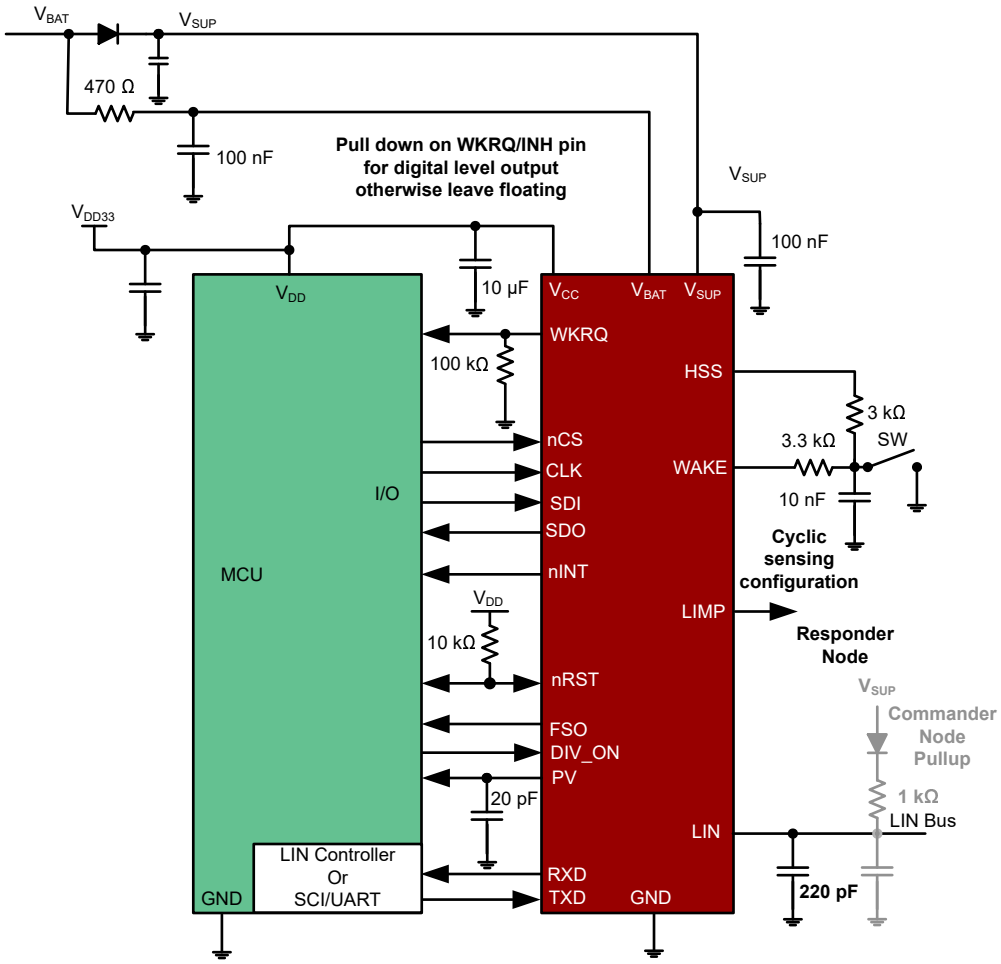


図 8-48. Application Cyclic Sense Configuration

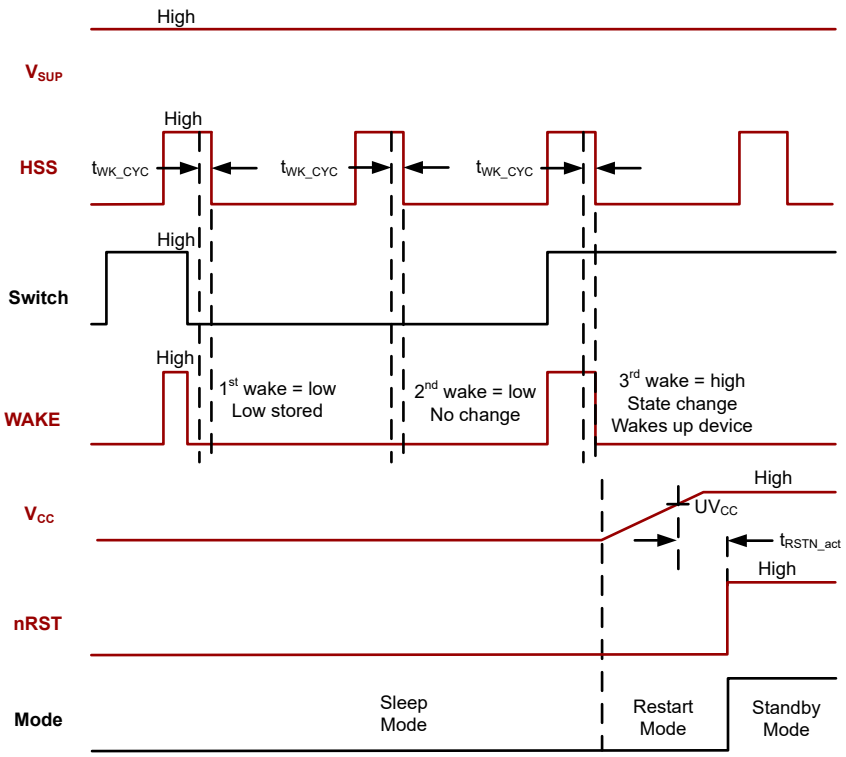


図 8-49. Cyclic Sensing Timing

注

When the device enters fail-safe mode and turns off the HSS pin, the WAKE pin reverts to static mode, and must be reprogrammed for cyclic sensing when the device enters standby or normal mode.

8.4.9 Mode Transitions

When the device is transitioning between modes, the device needs the time t_{MODE_CHANGE} and $t_{NOMINIT}$ to allow the change to fully propagate from the EN pin through the device into the new state.

8.5 Programming

The TLIN1431x-Q1 is 7-bit address access SPI communication port.

表 8-9 shows a list of the registers in the device along with their respective addresses.

8.5.1 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and CLK (SPI Clock). Each SPI transaction is initiated by a seven bit address with a R/W bit.

The SPI data input data on SDI is sampled on the low to high edge of CLK. The SPI output data on SDO is changed on the high to low edge of CLK.

See 図 8-50 and 図 8-51 for read and write method.

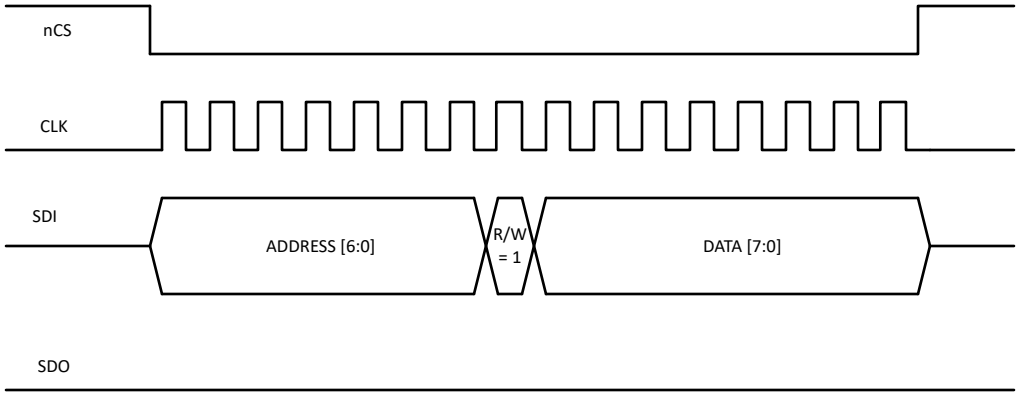


図 8-50. SPI Write

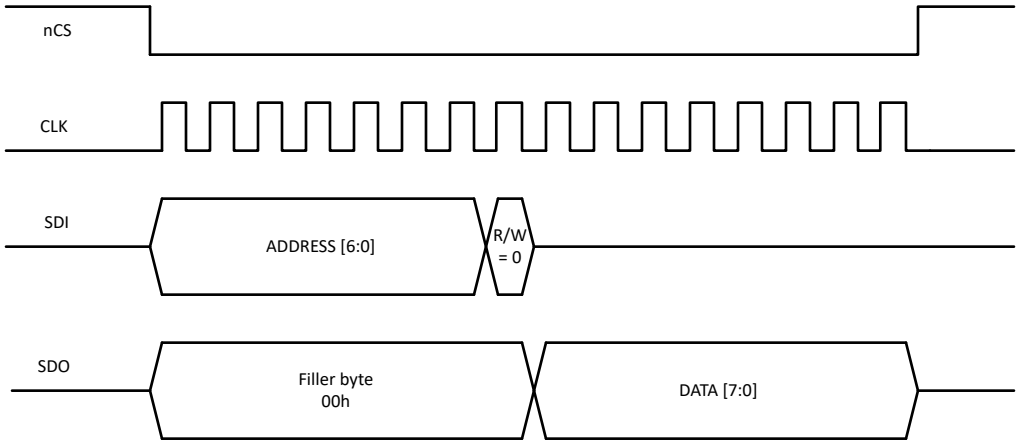


図 8-51. SPI Read

8.5.1.1 Cyclic Redundancy Check

The TLIN1431x supports cyclic redundancy check (CRC) for SPI transactions and is default disabled. Register 8'h0A[0] can be used to enable this feature. The default polynomial supports AutoSAR CRC8H2F, $X^8 + X^5 + X^3 + X^2 + X + 1$, see 表 8-7. CRC8 according to SAE J1850 is also supported and can be selected at register 8'h0B[0].

When CRC is enabled, a filler byte of 00h is used to calculate the CRC value during a read/write operation, see 図 8-52 and 図 8-53.

表 8-7. CRC8H27

SPI Transactions	
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	DFh
Magic Check	42h

表 8-8. CRC8 SAE J1850

SPI Transactions	
CRC result width	8 bits
Polynomial	1Dh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	4Bh
Magic Check	C4h

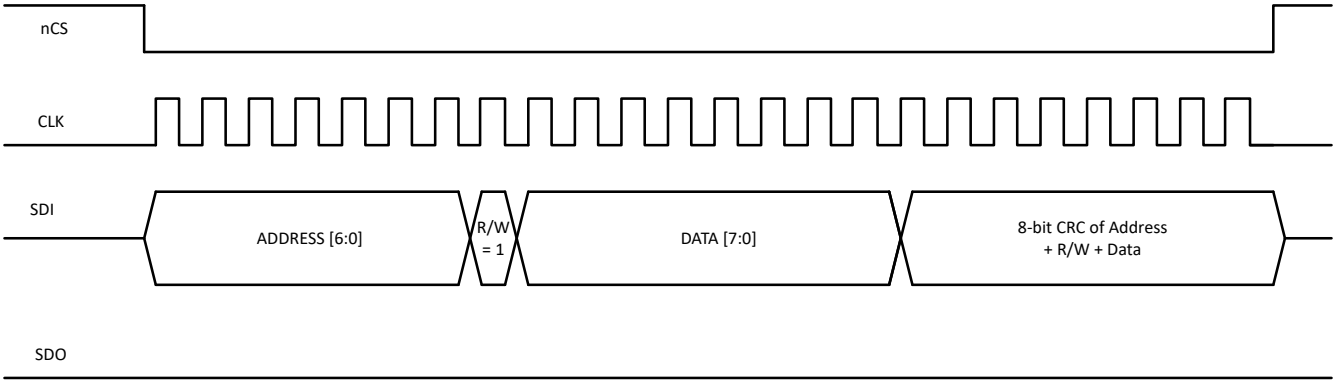


図 8-52. CRC SPI Write

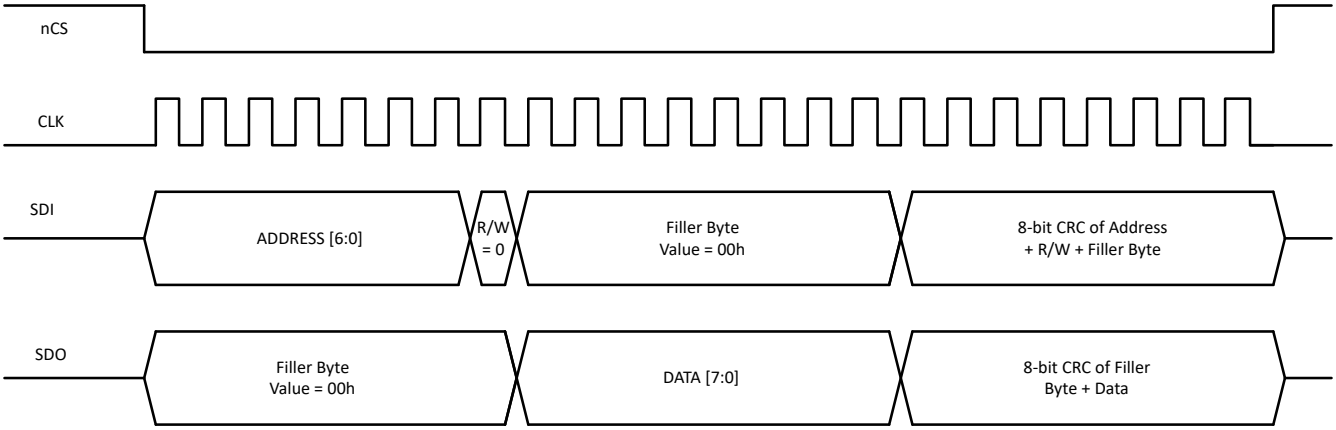


図 8-53. CRC SPI Read

8.5.1.2 Chip Select Not (nCS)

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low, the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction.

8.5.1.3 Serial Clock Input (CLK)

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of CLK and the SPI Data Output is changed on the falling edge of the CLK. See 図 8-54 .

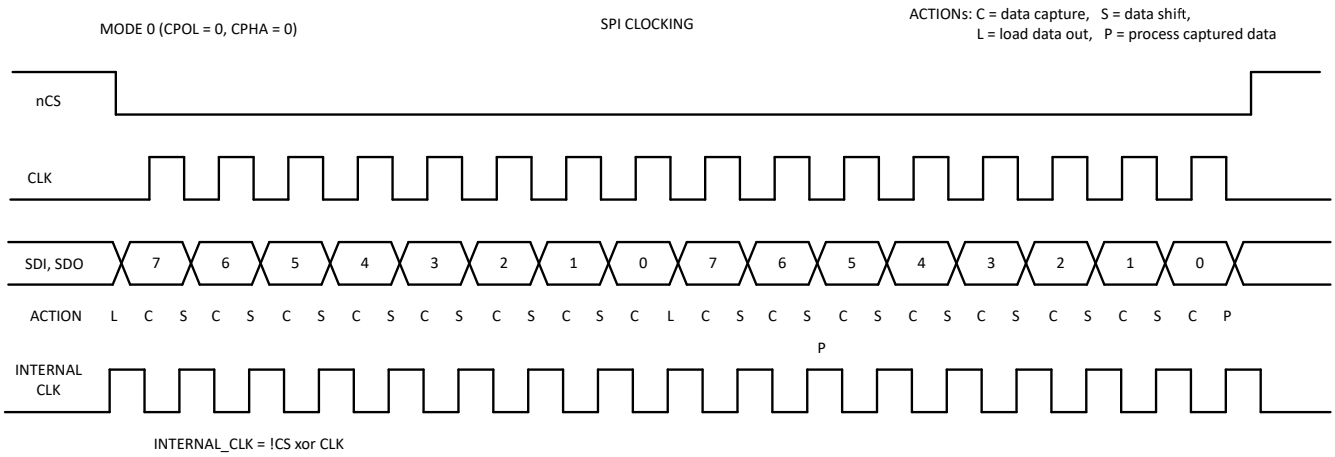


図 8-54. SPI Clocking

8.5.1.4 Serial Data Input (SDI)

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (SCK). The data is shifted into an 8-bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code is a write, the new data is written into the addressed register. When nCS has a falling edge, there will be 16-bits (CRC disabled) or 24-bits (CRC enabled) shifted in by CLK, at which time the nCS has a rising edge to deselect the device. 16 Clock cycles are required to shift 16-bits (CRC disabled) and 24 clock cycles for 24-bits (CRC enabled) during one SPI transaction (nCS is low). If more or less clock cycles than these are used, the SPIERR flag will be set. If CRC was enabled the CRCERR flag will be set. When writing to the device, any transaction other than 16 or 24 clock cycles could result in behavior that is outside of the specification.

8.5.1.5 Serial Data Output (SDO)

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS and a read command given, on the first falling edge of CLK, the shifting out of the data with each falling edge on CLK until all 8 bits have been shifted out the shift register.

8.6 Registers

The following tables contain the registers that the device use during SPI communication.

表 8-9 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in 表 8-9 should be considered as reserved locations and the register contents should not be modified.

表 8-9. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Go
8h	REV_ID_MAJOR	Major Revision	Go
9h	REV_ID_MINOR	Minor Revision	Go
Ah	CRC_CNTL	SPI CRC control	Go
Bh	CRC_POLY_SET	Sets SPI CRC polynomial	Go
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Go
11h	WAKE_PIN_CONFIG1	WAKE pin configuration 1	Go
12h	WAKE_PIN_CONFIG2	WAKE pin configuration 2	Go
13h	WD_CONFIG_1	Watchdog configuration 1	Go
14h	WD_CONFIG_2	Watchdog configuration 2	Go
15h	WD_INPUT_TRIG	Watchdog input trigger	Go
16h	WD_RST_PULSE	Watchdog output pulse width	Go
17h	FSM_CONFIG	Fail safe mode configuration	Go
18h	FSM_CNTR	Fail safe mode counter	Go
19h	DEVICE_RST	Device reset	Go
1Ah	DEVICE_CONFIG1	Device configuration 1	Go
1Bh	DEVICE_CONFIG2	Device configuration 2	Go
1Ch	SWE_TIMER	Sleep wake error timer configuration	Go
1Dh	LIN_CNTL	LIN transceiver control	Go
1Eh	HSS_CNTL	High side switch 1 and 2 control	Go
1Fh	PWM1_CNTL1	Pulse width modulation frequency select	Go
20h	PWM1_CNTL2	Pulse width modulation duty cycle two MSB select	Go
21h	PWM1_CNTL3	Pulse width modulation duty cycle eight LSB select	Go
22h	PWM2_CNTL1	Pulse width modulation frequency select	Go
23h	PWM2_CNTL2	Pulse width modulation duty cycle two MSB select	Go
24h	PWM2_CNTL3	Pulse width modulation duty cycle eight LSB select	Go
25h	TIMER1_CONFIG	High side switch timer 1 configuration	Go
26h	TIMER2_CONFIG	High side switch timer 2configuration	Go
28h	RSRT_CNTR	Restart counter configuration	Go
29h	nRST_CNTL	nRST and FSO pin control	Go
50h	INT_GLOBAL	Global Interrupts	Go
51h	INT_1	Interrupts	Go
52h	INT_2	Interrupts	Go
53h	INT_3	Interrupts	Go
56h	INT_EN_1	Interrupt enable for INT_1	Go
57h	INT_EN_2	Interrupt enable for INT_2	Go
58h	INT_EN_3	Interrupt enable for INT_3	Go
5Ah	INT_4	Interrupts	Go
5Eh	INT_EN_4	Interrupt enable for INT_4	Go

Complex bit access types are encoded to fit into small table cells. 表 8-10 shows the codes that are used for access types in this section.

表 8-10. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	H R	Set or cleared by hardware Read
Write Type		
H	H	Set or cleared by hardware
W	W	Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

8.6.1 DEVICE_ID_y Register (Address = 0h + formula) [reset = 0h]

DEVICE_ID_y is shown in 図 8-55 and described in 表 8-11.

Return to Summary Table.

Device Part Number

Offset = 0h + y; where y = 0h to 7h

図 8-55. DEVICE_ID_y Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-0b							

表 8-11. DEVICE_ID_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	0b	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address Address 00h = 54h = T Address 01h = 4Ch = L Address 02h = 49h = I Address 03h = 31h = 1 Address 04h = 34h = 4 Address 05h = 33h = 3 Address 06h = 31h = 1 Address 07h = 33h = 3 for 3.3 V LDO Address 07h = 35h = 5 for 5 V LDO

8.6.2 REV_ID_MAJOR Register (Address = 8h) [reset = 01h]

REV_ID_MAJOR is shown in 図 8-56 and described in 表 8-12.

Return to Summary Table.

Major Revision

図 8-56. REV_ID_MAJOR Register

7	6	5	4	3	2	1	0
Major_Revision							
R-01h							

表 8-12. REV_ID_MAJOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Major_Revision	R	01h	Major die revision

8.6.3 REV_ID_MINOR Register (Address = 9h) [reset = 0h]

REV_ID_MINOR is shown in 図 8-57 and described in 表 8-13.

Return to Summary Table.

Minor Revision

図 8-57. REV_ID_MINOR Register

7	6	5	4	3	2	1	0
Minor_Revision							
R-0b							

表 8-13. REV_ID_MINOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Minor_Revision	R	0b	Minor die revision

8.6.4 CRC_CNTL Register (Address = Ah) [reset = 0h]

CRC_CNTL is shown in 図 8-58 and described in 表 8-14.

Return to Summary Table.

SPI CRC register controls the CRC function. CRC_DIS bit can disable the CRC function.

図 8-58. CRC_CNTL Register

7	6	5	4	3	2	1	0
CRC_CNTL_RSVD							CRC_EN

図 8-58. CRC_CNTL Register (continued)

R-0b	R/W-0b

表 8-14. CRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	CRC_CNTL_RSVD	R	0b	CRC control reserved bits
0	CRC_EN	R/W	0b	CRC enable 0b = Disable 1b = Enable

8.6.5 CRC_POLY_SET (Address = Bh) [reset = 00h]

CRC_POLY_SET is shown 図 8-59 and described in 表 8-15.

Return to Summary Table.

This register will set which polynomial will be set for CRC. Defaults to AutoSAR 8-bit 0x2F.

図 8-59. CRC_POLY_SET Register

7	6	5	4	3	2	1	0
RSVD							POLY_8_SET
R							R/W-0b

表 8-15. CRC_POLY_SET Register Field Description

Bit	Field	Type	Reset	Description
7-1	RSVD	R	00h	Reserved
0	POLY_8_SET	R/W	0b	CRC polynomial select 0b = X^8 + X^5 + X^3 + X^2 + X + 1 (0x2F) 1b = X^8 + X^4 + X^3 + X^2 + 1 (0x1D SAE J1850)

8.6.6 Scratch_Pad_SPI Register (Address = Fh) [reset = 0h]

Scratch_Pad_SPI is shown in 図 8-60 and described in 表 8-16.

Return to Summary Table.

Read and Write Test Register SPI

図 8-60. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-0b							

表 8-16. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	0b	Read and Write Test Register SPI

8.6.7 WAKE_PIN_CONFIG1 Register (Address = 11h) [reset = 04h]

WAKE_PIN_CONFIG1 is shown in 図 8-61 and described in 表 8-17.

Return to Summary Table.

Register to configure the behavior of the WAKE pin.

図 8-61. WAKE_PIN_CONFIG1 Register

7	6	5	4	3	2	1	0
WAKE_CONFIG		WAKE_STAT		WAKE_WIDTH_INVALID		WAKE_WIDTH_MAX	

図 8-61. WAKE_PIN_CONFIG1 Register (continued)

R/W-00b	R/W0C/H-00b	R/W-01b	R/W-00b

表 8-17. WAKE_PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	Wake pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Pulse
5-4	WAKE_STAT	R/W0C/H	00b	Wake pin status 00b = No change 01b = Rising edge 10b = Falling edge 11b = Pulse
3-2	WAKE_WIDTH_INVALID	R/W	01b	Pulses less than or equal to these pulses are considered invalid 00b = 5 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 10 ms 01b = 10 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 20 ms 10b = 20 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 40 ms 11b = 40 ms and sets $t_{WAKE\_WIDTH\_MIN}$ to 80 ms
1-0	WAKE_WIDTH_MAX	R/W	00b	Maximum WAKE pin input pulse width to be considered valid. 00b = 750 ms 01b = 1000 ms 10b = 1500 ms 11b = 2000 ms

8.6.8 WAKE_PIN_CONFIG2 Register (Address = 12h) [reset = 2h]

WAKE_PIN_CONFIG2 is shown in 図 8-62 and described in 表 8-18.

Return to Summary Table.

Device wake configuration register

図 8-62. WAKE_PIN_CONFIG2 Register

7	6	5	4	3	2	1	0
WAKE_PULSE_CONFIG	WAKE_SENSE	TWK_CYC_SET	nINT_SEL		RXD_WK_CONFIG	WAKE_LEVEL	
R/W-0b	R/W/H-0b	R/W-0b	R/W-0b		R/W-0b	R/W-10b	

表 8-18. WAKE_PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE_PULSE_CONFIG	R/W	0b	Set WAKE pin expected pulse direction 0b = Low –> High –> Low 1b = High –> Low –> High
6	WAKE_SENSE	R/W/H	0b	WAKE pin configured for static or cyclic sensing wake 0b = Static 1b = Cyclic **注** When Cyclic sensing is selected and the device goes to fail-safe mode it will automatically change to static sensing. If cyclic sensing is needed it will have to be reprogrammed.

表 8-18. WAKE_PIN_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TWK_CYC_SET	R/W	0b	Sets the t_{WK_CYC} time (µs) for sampling the WAKE pin status (used for cyclic sensing) 0b = 30 1b = 75 注 NOTE: $t_{WK\_CYC\_SET}$ works with timer1 and timer2. When using 75 µs t_{WK_CYC}, 100 µs TIMER1/2_ON_WIDTH cannot be used.
4-3	nINT_SEL	R/W	00b	nINT configuration selection: active low 00b = Global interrupt 01b = Watchdog failure output 10b = Reserved 11b = Wake request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	WAKE_LEVEL	R/W	10b	WAKE pin threshold level; Mid-point value in 2 V window. 00b = 2.5 V 01b = 2.8 V 10b = 3 V 11b = 3.3 V

8.6.9 WD_CONFIG_1 Register (Address = 13h) [reset = 90h]

WD_CONFIG_1 is shown in 図 8-63 and described in 表 8-19.

Return to Summary Table.

Watchdog configuration register.

図 8-63. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		RSVD			
R/W-10b		R/W-01b		R-0000b			

表 8-19. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	10b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Reserved
5-4	WD_PRE	R/W	01b	Watchdog prescalar 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3-0	RSVD	R	0000b	Reserved

8.6.10 WD_CONFIG_2 Register (Address = 14h) [reset = 02h]

WD_CONFIG_2 is shown in 図 8-64 and described in 表 8-20.

Return to Summary Table.

Watchdog timer and error counter register.

図 8-64. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				WD_STBY_DIS
R/W-000b			RH-0001b				R/W-0b

表 8-20. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	000b	Sets window or timeout times based upon the WD_PRE setting See WD_TIMER table
4-1	WD_ERR_CNT	RH	0001b	Watchdog error counter Running count of errors up to 15 errors
0	WD_STBY_DIS	R/W	0b	Watchdog disable in standby mode 0b = Enabled 1b = Disabled

8.6.11 WD_INPUT_TRIG Register (Address = 15h) [reset = 0h]

WD_INPUT_TRIG is shown in 図 8-65 and described in 表 8-21.

Return to Summary Table.

Writing FFh resets WD timer if accomplished at appropriate time.

図 8-65. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
R/W1C-00h							

表 8-21. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

8.6.12 WD_RST_PULSE Register (Address = 16h) [reset = 40h]

WD_RST_PULSE is shown in 図 8-66 and described in 表 8-22.

Return to Summary Table.

Sets the watchdog error counter value.

図 8-66. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
WD_ERR_CNT_SET		RSVD					
R/W-01b		R-000000b					

表 8-22. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ERR_CNT_SET	R/W	01b	Sets the watchdog event error counter that upon reaching the count value, will cause the watchdog action. 00b = Immediate trigger on each WD fail 01b = Triggers when counter reaches 5 10b = Triggers when counter reaches 9 11b = Triggers when counter reaches 15
5-0	RSVD	R	000000b	Reserved

8.6.13 FSM_CONFIG Register (Address = 17h) [reset = 0h]

FSM_CONFIG is shown in 図 8-67 and described in 表 8-23.

Return to Summary Table.

Configures the fail-safe mode

図 8-67. FSM_CONFIG Register

7	6	5	4	3	2	1	0
FS_CNTR_ACT				FS_STAT			FSM_DIS
R/W-0000b				RH-000b			R/W-0b

表 8-23. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_ACT	R/W	0000b	Action if fail safe counter exceeds programmed value 000b = Disabled 0001b = Pull WKRQ/INH low for 1 s 0010b = Perform soft reset 0011b = Perform hard reset - POR 0100b = Stop responding to wake events and go to sleep until power cycle reset 0101b = Reserved 0110b = Reserved 0111b = Reserved 1001b = Turn off VCC for 300 ms and set interrupt 注 • If LIMP is configured as INH then 0001b will impact cause the LIMP pin to go low for 1 s. • All other values reserved
3-1	FSM_STAT	RH	000b	Reason for entering failsafe mode 000b = Not in FS mode 001b = Thermal shut down event 010b = Reserved 011b = UV_{CC} 100b = OV_{CC} 101b = V_{CCSC} 110b = Watchdog failure 111b = Restart counter exceeded These values are held until cleared by writing 0h to FSM_CNTR_STAT
0	FSM_DIS	R/W	0b	Fail safe mode disable: Excludes power up fail safe 0b = Enabled 1b = Disabled

8.6.14 FSM_CNTR Register (Address = 18h) [reset = 0h]

FSM_CNTR is shown in 図 8-68 and described in 表 8-24.

Return to Summary Table.

Set fail safe counter and status

図 8-68. FSM_CNTR Register

7	6	5	4	3	2	1	0
FSM_CNTR_SET				FSM_CNTR_STAT			
R/W-0h				RH-0h			

表 8-24. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0h	Sets the number of times FS mode enters before action taken. Value is one less than the number of times FS mode is entered. Range is 0-15, representing entering fail-safe mode 1-16 times.

表 8-24. FSM_CNTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	FSM_CNTR_STAT	RH	0h	Reads back the number of time FSM has been entered in a row up to 15. Can be cleared by writing 0h.

8.6.15 DEVICE_RST Register (Address = 19h) [reset = 0h]

DEVICE_RST is shown in 図 8-69 and described in 表 8-25.

Return to Summary Table.

Forces a soft or hard reset.

図 8-69. DEVICE_RST Register

7	6	5	4	3	2	1	0
RESERVED						SF_RST	HD_RST
R-00h						R/W1C-0b	R/W1C-0b

表 8-25. DEVICE_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	00h	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers return to default values while keeping INH on.
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset when writing a 1. 注 NOTE: This will set the PWRON interrupt flag.

8.6.16 DEVICE_CONFIG (Address = 1Ah) [reset = 80h]

DEVICE_CONFIG is shown in 図 8-70 and described in 表 8-26

Return to Summary Table.

Enables SPI to work in sleep mode if V_{IO} is available.

WKRQ/INH and LIMP pin configuration.

図 8-70. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
WKRQ_POL_SEL	WKRQ_INH_DIS	INH_LIMP_SEL	LIMP_DIS	LIMP_SEL_RESET		LIMP_RESET	RSVD
R/W-1b	R/W-0b	R/W - 0b	R/W - 0b	R/W - 00b		R/W1C - 0b	R - 0b

表 8-26. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WKRQ_POL_SEL	R/W	1b	Selects the polarity for the WKRQ pin 0b = Low 1b = High
6	WKRQ_INH_DIS	R/W	0b	WKRQ/INH pin disable 0b = Enabled 1b = Disabled
5	INH_LIMP_SEL	R/W	0b	Pin function select function of INH pin 0b = INH 1b = LIMP Note: This only works if WKRQ/INH pin is configured for INH at power-up. If pin is WKRQ writing to this bit will be ignored.

表 8-26. DEVICE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LIMP_DIS	R/W	0b	LIMP pin disable 0b = Enabled 1b = Disabled
3-2	LIMP_SEL_RESET	R/W	0b	Selects the method to reset/turnoff the LIMP pin 00b = On third successful input trigger the error counter receives 01b = First correct input trigger 10b = SPI write to 8'h1A[1] = 1 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset Writing a one to this location resets the LIMP pin to off state and bit automatically clears
0	RSVD	R	0b	Reserved

8.6.17 DEVICE_CONFIG2 (Address = 1Bh) [reset = 0h]

DEVICE_CONFIG2 is shown in 図 8-71 and described in 表 8-27

Return to Summary Table.

LIMP pin configuration and control.

図 8-71. DEVICE_CONFIG2 Register

7	6	5	4	3	2	1	0
LIMP_HSS_SEL		LIMP_HSS_CNTL			LIMP_HSS_ON	WAKE_WIDTH_MAX_DIS	RSVD
R/W-00b		R/W-000b			R/W-0b	R/W-0b	R-0b

表 8-27. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIMP_HSS_SEL	R/W	00b	Selects LIMP pin function 00b = LIMP 01b = High side switch 10b = INH 11b = Reserved
5-3	LIMP_HSS_CNTL	R/W	000b	Selects the method of control for the LIMP pin when configured as a high side switch 000b = On/Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b - 111b = Reserved
2	LIMP_HSS_ON	R/W	0b	When LIMP is configured as HSS and control is On/Off this bit turns on or off the LIMP pin. 0b = Off 1b = On
1	WAKE_WIDTH_MAX_DIS	R/W	0b	Disables the Max limit, $t_{WK\_PULSE\_WIDTH\_MAX}$ detection when pulse is selected for WAKE pin wake up. 0b = Enabled 1b = Disabled
0	RSVD	R	0b	Reserved

8.6.18 SWE_TIMER (Address = 1Ch) [reset = 30h]

SWE_TIMER is shown in 図 8-72 and described in 表 8-28

Return to Summary Table.

Sleep wake error timer configuration. Power up always sets to default value.

図 8-72. SWE_TIMER Register

7	6	5	4	3	2	1	0
SWE_DIS	SWE_TIMER_SET				RSVD		
R/W-0b	R/W-0110b				R		

表 8-28. SWE_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_DIS	R/W	0b	Sleep wake error disable: NOTE: This disables the device from starting the t_{INACT_FS} timer. If enabled, a SPI read or write must take place within this window or the device will go back to sleep. 0b = Enabled 1b = Disabled
6-3	SWE_TIMER_SET	R/W	0110b	Sets the timer used for t_{INACT_FS} (minutes) 0000b = 2 0001b = 2.5 0010b = 3 0011b = 3.5 0100b = 4 0101b = 4.5 0110b = 5 (default) 0111b = 5.5 1000b = 6 1001b = 6.5 1010b = 8 1011b = 8.5 1100b = 10 1101b = 0.5 1111b = 1
2-0	RSVD	R	0b	Reserved

8.6.19 LIN_CNTL (Address = 1Dh) [reset = 00h]

LIN_CNTL is shown in 図 8-73 and described in 表 8-29

Return to Summary Table.

LIN transceiver mode and DTO control. Port 1 is the TLIN1431x-Q1 LIN control.

図 8-73. LIN_CNTL Register

7	6	5	4	3	2	1	0
LIN_MODE		LIN_DTO_DIS	LIN_RSVD				
R/W/H-00b		R/W - 0b	R - 00000b				

表 8-29. LIN_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIN_MODE	R/W/H	00b	Port 1 LIN mode control 00b = Standby mode 01b = Sleep Mode 10b = Normal Mode 11b = Fast Mode
5	LIN_DTO_DIS	R/W	0b	Port 1 LIN dominant state timeout disable 0b = Enabled 1b = Disabled
4-0	LIN_RSVD	R	00000b	Reserved

8.6.20 HSS_CNTL (Address = 1Eh) [reset = 0h]

HSS_CNTL is shown in 図 8-74 and described in 表 8-30

Return to Summary Table.

HSS high side switch control.

図 8-74. HSS_CNTL Register

7	6	5	4	3	2	1	0
HSS_EN	HSS_CNTL			HSS_RSVD			
R/W-0b	R/W-000b			R-0000b			

表 8-30. HSS_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS_EN	R/W	0b	High side switch, HSS, enable 0b = Disabled 1b = Enabled
6-4	HSS_CNTL	R/W	000b	Control for HSS 000b = On/Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = HSSC 110b - 111b = Reserved Note: selecting HSSC control disables FSO output capability
3-0	HSS_RSVD	R/W	0000b	Reserved

8.6.21 PWM1_CNTL1 (Address = 1Fh) [reset = 0h]

PWM1_CNTL1 is shown in 図 8-75 and described in 表 8-31

Return to Summary Table.

Sets the pulse width modulation frequency, PWM1.

図 8-75. PWM1_CNTL1 Register

7	6	5	4	3	2	1	0
PWM1_FREQ	PWM1_FREQ_RSVD						
R/W-0b	R-0b						

表 8-31. PWM1_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM1_FREQ_RSVD	R	0b	Reserved

8.6.22 PWM1_CNTL2 (Address = 20h) [reset = 0h]

PWM1_CNTL2 is shown in 図 8-76 and described in 表 8-32

Return to Summary Table.

Set the two most significant bit for the 10-bit PWM1. These work with register h'21 PWM1_CNTL3.

図 8-76. PWM1_CNTL2 Register

7	6	5	4	3	2	1	0
PWM1_RSVD						PWM1_DC_MSB	

図 8-76. PWM1_CNTL2 Register (continued)

R-0b	R/W-00b

表 8-32. PWM1_CNTL2L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM1_RSVD	R	0b	Reserved
1-0	PWM1_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM1 duty cycle select. Works with 'h21[7:0] 00b = 100% off when used with 'h21[7:0] and it is 00h xxb = on time with an increase of ~ 0.1% when used with 'h21[7:0] 11b = 100% of when used with 'h21[7:0] and it is FFh

注

Minimum on-time during PWM is limited to the on and off-time of the high side switch. This will make certain PWM values unusable like 00 0000 0001.

8.6.23 PWM1_CNTL3 (Address = 21h) [reset = 00h]

PWM1_CNTL3 is shown in 図 8-77 and described in 表 8-33

Return to Summary Table.

Bits 0 - 7 of the 10-bit PWM1. Used with register h'20[1:0] PWM1_CNTL2.

図 8-77. PWM1_CNTL3 Register

7	6	5	4	3	2	1	0
PWM1_DC							
R/W-00h							

表 8-33. PWM1_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM1 00h = 100% off when used with 'h20[1:0] = 00b xxh = On time with an increase of ~ 0.1% when used with 'h20[1:0] FFh = 100% on when used with 'h20[1:0] = 11b

8.6.24 PWM2_CNTL1 (Address = 22h) [reset = 0h]

PWM2_CNTL1 is shown in 図 8-78 and described in 表 8-34

Return to Summary Table.

Sets the pulse width modulation frequency, PWM2.

図 8-78. PWM2_CNTL1 Register

7	6	5	4	3	2	1	0
PWM2_FREQ	PWM2_FREQ_RSVD						
R/W-0b	R-0b						

表 8-34. PWM2_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM2_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM2_FREQ_RSVD	R	0b	Reserved

8.6.25 PWM2_CNTL2 (Address = 23h) [reset = 0h]

PWM2_CNTL2 is shown in 図 8-79 and described in 表 8-35

Return to Summary Table.

Set the two most significant bit for the 10-bit PWM2. These work with register h'24 PWM2_CNTL3.

図 8-79. PWM2_CNTL2 Register

7	6	5	4	3	2	1	0
PWM2_RSVD						PWM2_DC_MSB	
R-0b						R/W-00b	

表 8-35. PWM2_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM2_RSVD	R	0b	Reserved
1-0	PWM2_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM2 duty cycle select. Works with 'h24[7:0] 00b = 100% off when used with 'h24[7:0] and it is 00h xxb = on time with an increase of ~ 0.1% when used with 'h24[7:0] 11b = 100% of when used with 'h24[7:0] and it is FFh

8.6.26 PWM2_CNTL3 (Address = 24h) [reset = 0h]

PWM2_CNTL3 is shown in 図 8-80 and described in 表 8-36

Return to Summary Table.

Bits 0 - 7 of the 10-bit PWM2. Used with register h'23[1:0] PWM2_CNTL2.

図 8-80. PWM2_CNTL3 Register

7	6	5	4	3	2	1	0
PWM2_DC							
R/W-00h							

表 8-36. PWM2_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM2_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM2 00h = 100% off when used with 'h23[1:0] = 00b xxh = On time with an increase of ~ 0.1% when used with 'h23[1:0] FFh = 100% on when used with 'h23[1:0] = 11b

注

Minimum on-time during PWM is limited to the on and off-time of the high side switch. This will make certain PWM values unusable like 00 0000 0001.

8.6.27 TIMER1_CONFIG (Address = 25h) [reset = 00h]

TIMER1_CONFIG is shown in 図 8-81 and described in 表 8-37

Return to Summary Table.

Sets timer 1 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible.

図 8-81. TIMER1_CONFIG Register

7	6	5	4	3	2	1	0
TIMER1_ON_WIDTH				TIMER1_RSVD	TIMER1_PERIOD		

図 8-81. TIMER1_CONFIG Register (continued)

R/W-0h	R-0b	R/W-000b

表 8-37. TIMER1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER1_ON_WIDTH	R/W	0b	Sets the high side switch on time (ms) for timer 1 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%) 注 NOTE: t_{WK_CYC} which is set by $t_{WK\_CYC\_SET}$ works with these times to determine if a state change has taken place on the WAKE pin. When t_{WK_CYC} is set at 65 µs the 100 µs on width time cannot be used.
3	TIMER1_RSVD	R	0b	Reserved
2-0	TIMER1_PERIOD	R/W	0b	Sets the timer period (ms) for timer 1 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

8.6.28 TIMER2_CONFIG (Address = 26h) [reset = 00h]

TIMER2_CONFIG is shown in 図 8-82 and described in 表 8-38

Return to Summary Table.

Sets timer 2 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible.

図 8-82. TIMER2_CONFIG Register

7	6	5	4	3	2	1	0
TIMER2_ON_WIDTH				TIMER2_RSVD	TIMER2_PERIOD		
R/W-0h				R-0b	R/W-000b		

表 8-38. TIMER2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER2_ON_WIDTH	R/W	0b	Sets the high side switch on time (ms) for timer 2 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%) 注 NOTE: t_{WK_CYC} which is set by $t_{WK\_CYC\_SET}$ works with these times to determine if a state change has taken place on the WAKE pin. When t_{WK_CYC} is set at 65 µs the 100 µs on width time cannot be used.
3	TIMER2_RSVD	R	0b	Reserved
2-0	TIMER2_PERIOD	R/W	0b	Sets the timer period (ms) for timer 2 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

8.6.29 RSRT_CNTR (Address = 28h) [reset = 40h]

RSRT_CNTR is shown in 図 8-83 and described in 表 8-39

Return to Summary Table.

Restart mode counter set and counter. Determines the number of times the device has entered restart mode and when it will transition to sleep mode once programmed counter value has been reached. Counter should be reset often to avoid this transition.

図 8-83. RSRT_CNTR Register

7	6	5	4	3	2	1	0
RSRT_CNTR_SEL				RSRT_CNTR			
R/W-4h				R/W1C-0h			

表 8-39. RSRT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSRT_CNTR_SEL	R/W	4h	Selects the number of times the device can enter restart mode prior to device entering sleep mode. Range is 0-15, representing entering restart mode 1-16 times.
3-0	RSRT_CNTR	R/W1C	0h	Provides the number of times the device has entered restart mode and should be cleared prior to reaching the RSRT_CNTR_SEL value

8.6.30 nRST_CNTL (Address = 29h) [reset = 00h]

nRST_CNTL is shown in 図 8-84 and described in 表 8-40

Return to Summary Table.

Configures nRST pin and FSO pin.

図 8-84. nRST_CNTL Register

7	6	5	4	3	2	1	0
RSVD		nRST_PULSE_WIDTH	FSO_POL_SEL	FSO_SEL			RSVD
R-00b		R/W-0b	R/W-0b	R/W/H-000b			R-0b

表 8-40. nRST_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Reserved
5	nRST_PULSE_WIDTH	R/W	0b	Sets the pulse width for toggling nRST from high-->low-->high when device enters restart mode (ms) 0b = 2 1b = 15
4	FSO_POL_SEL	R/W	0b	Selects the polarity for the FSO pin 0b = Active low 1b = Active high 注 Selects the output level when register 8'h29[3:1] = 110b making the pin a general-purpose output pin; 0 = Low and 1 = High
3-1	FSO_SEL	R/W/H	000b	Selects the information that will cause this pin to be pulled to the state selected by 'h29[4] 000b = V_{CC} Interrupt (overvoltage, undervoltage or short) 001b = WD interrupt event 010b = Reserved 011b = Local wake request (LWU) 100b = Bus wake request (WUP) 101b = Fail-safe mode entered 110b = General purpose output 111b = Reserved
0	RSVD	R	0b	Reserved

8.6.31 INT_GLOBAL Register (Address = 50h) [reset = A0h]

INT_GLOBAL is shown in 図 8-85 and described in 表 8-41.

Return to Summary Table.

Logical OR of all to certain interrupts.

図 8-85. INT_GLOBAL Register

7	6	5	4	3	2	1	0
GLOBALERR	INT_1	INT_2	INT_3	RSVD	INT_4	RSVD	RSVD
RH-1b	RH-0b	RH-1b	RH-0b	RH-0b	RH-0b	R-0b	R-0b

表 8-41. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBALERR	RH	1b	Logical OR of all interrupts
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	1b	Logical OR of INT_2 register

表 8-41. INT_GLOBAL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT_3	RH	0b	Logical OR of INT_3 register
3	RSVD	RH	0b	Reserved
2	INT_4	RH	0b	Logical OR of INT_4 register
1	RSVD	RH	0b	Reserved
0	RSVD	RH	0b	Reserved

8.6.32 INT_1 Register (Address = 51h) [reset = 0h]

INT_1 is shown in 図 8-86 and described in 表 8-42.

Return to Summary Table.

図 8-86. INT_1 Register

7	6	5	4	3	2	1	0
WD	RSVD	LWU	WKERR	RSVD			
R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R-0b			

表 8-42. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. NOTE: This interrupt bit will be set for every watchdog error event and does not rely upon the Watchdog error counter
6	RSVD	R	0b	Reserved
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3-0	RSVD	R	0b	Reserved

8.6.33 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in 図 8-87 and described in 表 8-43.

Return to Summary Table.

図 8-87. INT_2 Register

7	6	5	4	3	2	1	0
SMS	PWRON	OVCC	UVSUP	RSVD	UVCC	TSD_VCC_LIN	TSD_HSS_LIMP
R/W1C-0b	R/W1C-1b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

表 8-43. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Only sets when sleep mode is entered by a fault
6	PWRON	R/W1C	1b	Power on
5	OVCC	R/W1C	0b	V_{CC} overvoltage
4	UVSUP	R/W1C	0b	V_{SUP} undervoltage
3	RSVD	R	0b	Reserved
2	UVCC	R/W1C	0b	V_{CC} undervoltage
1	TSD_VCC_LIN	R/W1C	0b	Thermal Shutdown due to VCC or LIN
0	TSD_HSS_LIMP	R/W1C	0b	Thermal Shutdown due to HSS or LIMP

8.6.34 INT_3 Register (Address 53h) [reset = 0h]

INT_3 is shown in 図 8-88 and described in 表 8-44.

Return to Summary Table.

図 8-88. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	RSVD	FSM	CRCERR	VCCSC	RSRT_CNT	RSVD	
R/W1C-0b	R-0b	R/W1C-0b	R/W1C/U-0b	R/W1C/U-0b	R/W1C/U-0b	R-0b	

表 8-44. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description0b
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	RSVD	R	0b	Reserved
5	FSM	R/W1C	0b	Entered fail-safe mode. Can be cleared while in failsafe mode.
4	CRCERR	R/W1C/U	0b	SPI CRC error detected
3	VCCSC	R/W1C/U	0b	V_{CC} short detected
2	RSRT_CNT	R/W1C/U	0b	Restart counter exceeded programmed count
1-0	RSVD	R	0b	Reserved

8.6.35 INT_EN_1 Register (Address = 56h) [reset = B0h]

INT_EN_1 is shown in 図 8-89 and described in 表 8-45.

Return to Summary Table.

Interrupt mask for INT_1.

図 8-89. INT_EN_1 Register

7	6	5	4	3	2	1	0
WD_EN	RSVD	LWU_EN	WKERR_EN	RSVD			
R/W-1b	R-0b	R/W-1b	R/W-1b	R-0000b			

表 8-45. INT_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN	R/W	1b	Watchdog event interrupt enable
6	RSVD	R/W	0b	Reserved
5	LWU_EN	R/W	1b	Local wake up enable
4	WKERR_EN	R/W	1b	Wake error enable
3-0	RSVD	R	0000b	Reserved

8.6.36 INT_EN_2 Register (Address = 57h) [reset = 37h]

INT_EN_2 is shown in 図 8-90 and described in 表 8-46.

Return to Summary Table.

Interrupt mask for INT_2.

図 8-90. INT_EN_2 Register

7	6	5	4	3	2	1	0
RSVD		OVCC_EN	UVSUP_EN	RSVD	UVCC_EN	TSD_VCC_LIN_EN	TSD_HSS_LMIP_EN
R-0b		R/W-1b	R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b

表 8-46. INT_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0b	Reserved
5	OVCC_EN	R/W	1b	V_{CC} over voltage enable
4	UVSUP_EN	R/W	1b	V_{SUP} undervoltage enable
3	RSVD	R	0b	Reserved
2	UVCC_EN	R/W	1b	V_{CC} undervoltage enable
1	TSD_VCC_LIN_EN	R/W	1b	Thermal shutdown enable for VCC and LIN
0	TSD_HSS_LIMP_EN	R/W	1b	Thermal shutdown due to HSS or LIMP enable

8.6.37 INT_EN_3 Register (Address =58h) [reset = BCh]

INT_EN_3 is shown in 図 8-91 and described in 表 8-47.

Return to Summary Table.

Interrupt mask for INT_3.

図 8-91. INT_EN_3 Register

7	6	5	4	3	2	1	0
SPIERR_EN	RSVD	FSM_EN	CRCERR_EN	VCCSC_EN	RSRT_CNT_EN	RSVD	
R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b	

表 8-47. INT_EN_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_EN	R/W	1b	SPI error interrupt enable
6	RSVD	R	0b	Reserved
5	FSM_EN	R/W	1b	Fail-safe mode interrupt enable
4	CRCERR_EN	R/W	1b	SPI CRC error interrupt enable
3	VCCSC_EN	R/W	1b	VCC short circuit interrupt enable
2	RSRT_CNT_EN	R/W	1b	Exceeding programmed restart counter interrupt enable
1-0	RSVD	R	0b	Reserved

8.6.38 INT_4 Register (Address = 5Ah) [reset = 0h]

INT_4 is shown in 図 8-92 and described in 表 8-48.

Return to Summary Table.

Interrupt for LIN and high side switch.

図 8-92. INT_4 Register

7	6	5	4	3	2	1	0
LIN_WUP	LIN_DTO	RSVD		HSSOC	HSSOL	RSVD	
R/W1C-0b	R/W1C-0b	R-00b		R/W1C-0b	R/W1C-0b	R-00b	

表 8-48. INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN_WUP	R/W1C	0b	LIN bus wake
6	LIN_DTO	R/W1C	0b	LIN dominant state timeout
5-4	RSVD	R	00b	Reserved
3	HSSOC	R/W1C	0b	High side switch over current
2	HSSOL	R/W1C	0b	High side switch open load

表 8-48. INT_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	RSVD	R	00b	Reserved

8.6.39 INT_EN_4 Register (Address = 5Eh) [reset = CCh]

INT_EN_4 is shown in 図 8-93 and described in 表 8-49.

Return to Summary Table.

Interrupt mask for INT_4.

図 8-93. INT_EN_4 Register

7	6	5	4	3	2	1	0
LIN_WUP_EN	LIN_DTO_EN	RSVD		HSSOC_EN	HSSOL_EN	RSVD	
R/W-1b	R/W-1b	R-00b		R/W-1b	R/W-1b	R-00b	

表 8-49. INT_EN_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN_WUP_EN	R/W	1b	LIN bus wake interrupt enable
6	LIN_DTO_EN	R/W	1b	LIN dominant state timeout interrupt enable
5-4	RSVD	R	00b	Reserved
3	HSSOC_EN	R/W	1b	High side switch over current interrupt enable
2	HSSOL_EN	R/W	1b	High side switch open load interrupt enable
1-0	RSVD	R	00b	Reserved

8.6.40 Reserved Registers

All other registers not provided up to 'h7F are reserved.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TLIN1431x-Q1 can be used in both responder node and commander node applications in a LIN network. The device comes with the ability to support remote wake up request and local wake up request. It can provide the power to the local processor as well as providing watchdog supervision for the processor.

9.1.1 Device Brownout Information

During a brownout condition where V_{SUP} stays above V_{nPORF}, the device pin and mode behavior is as per 図 9-1. When V_{SUP} falls below V_{nPORF}, the device enters power-on reset as per 図 9-2

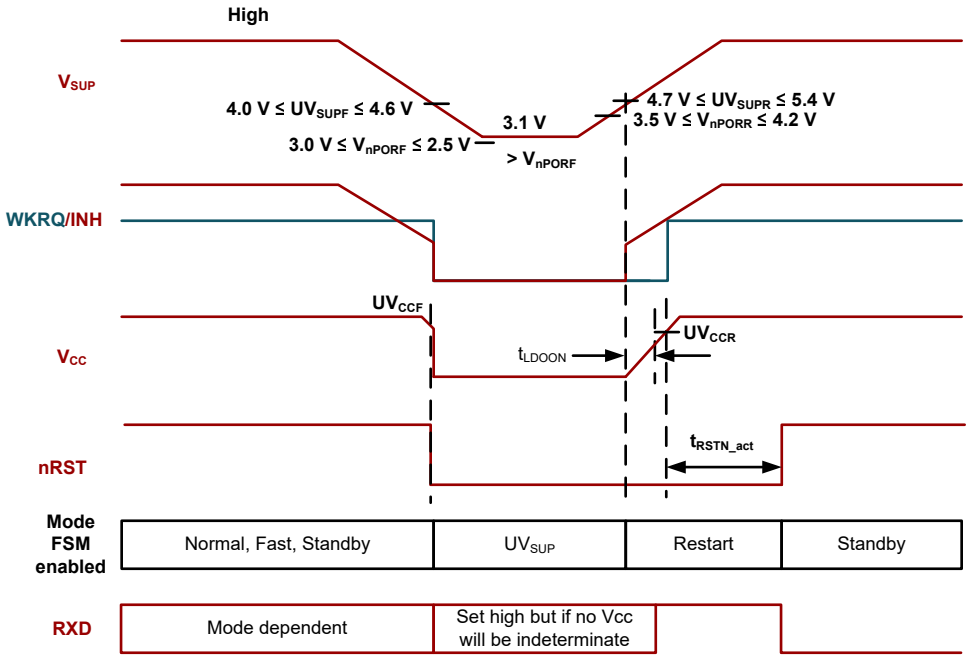


図 9-1. Brownout Above V_{nPORF}

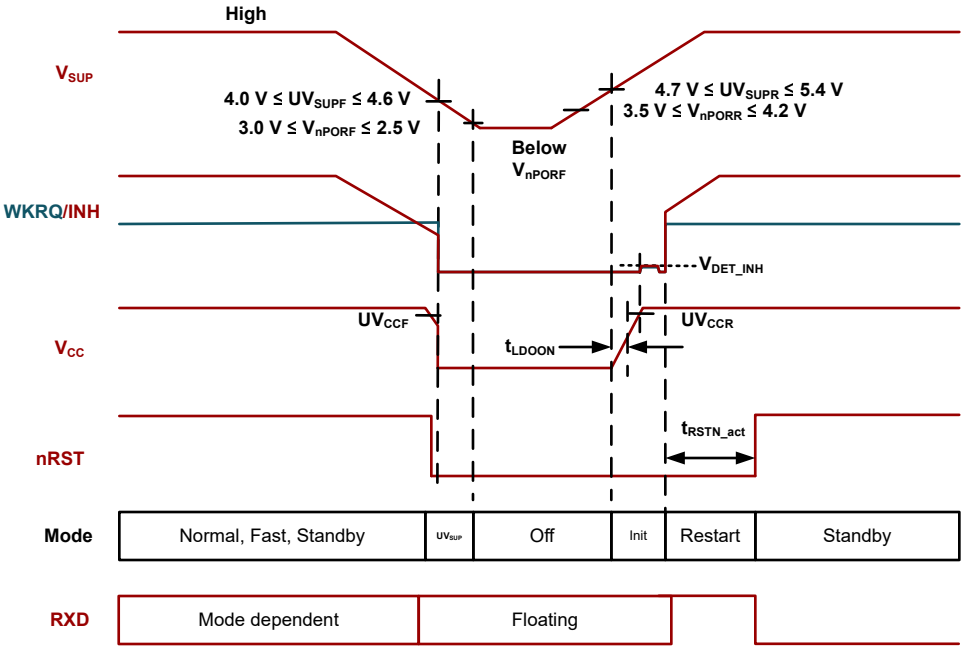


図 9-2. Brownout Below V_{nPORF}

9.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for responder node applications. For commander node applications, an external 1 kΩ pull-up resistor with series blocking diode can be used. 図 9-3 shows the device in SPI control mode in a responder node application. 図 9-4 shows the device in pin control mode for a responder node application.

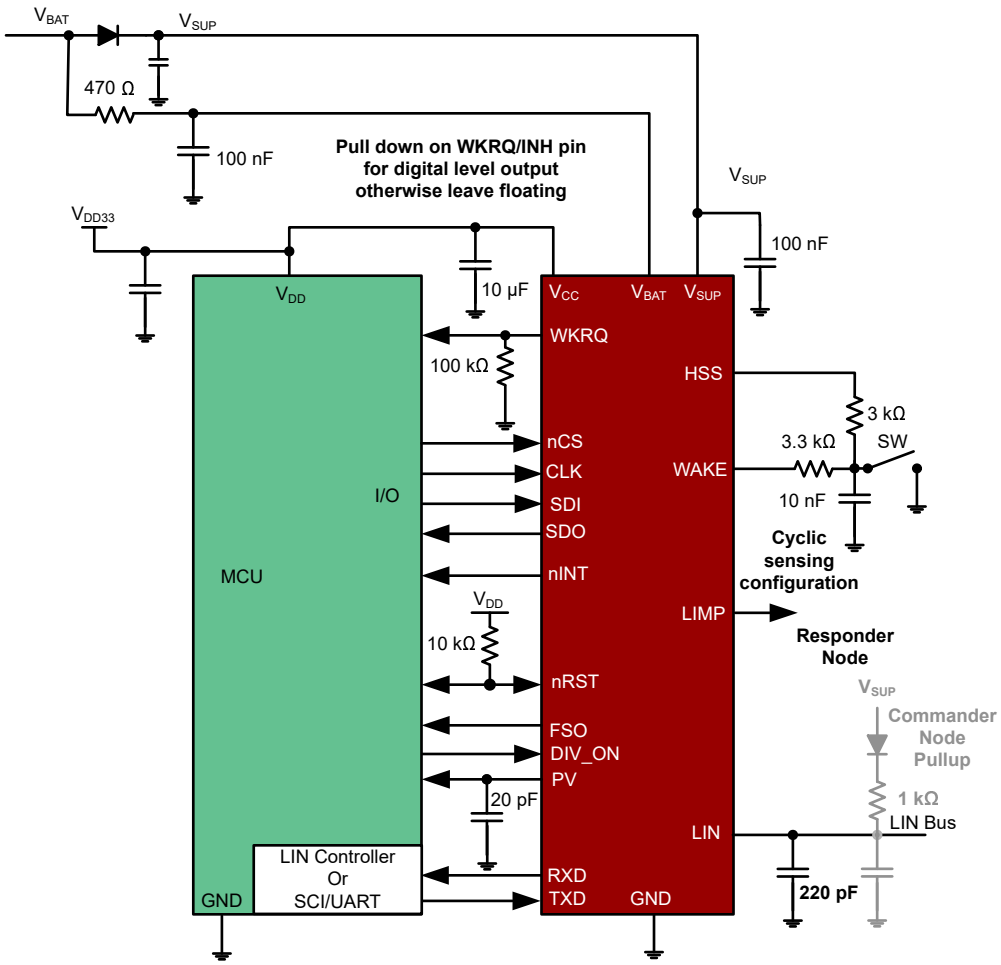


図 9-3. Typical LIN Responder Node in SPI Control Mode

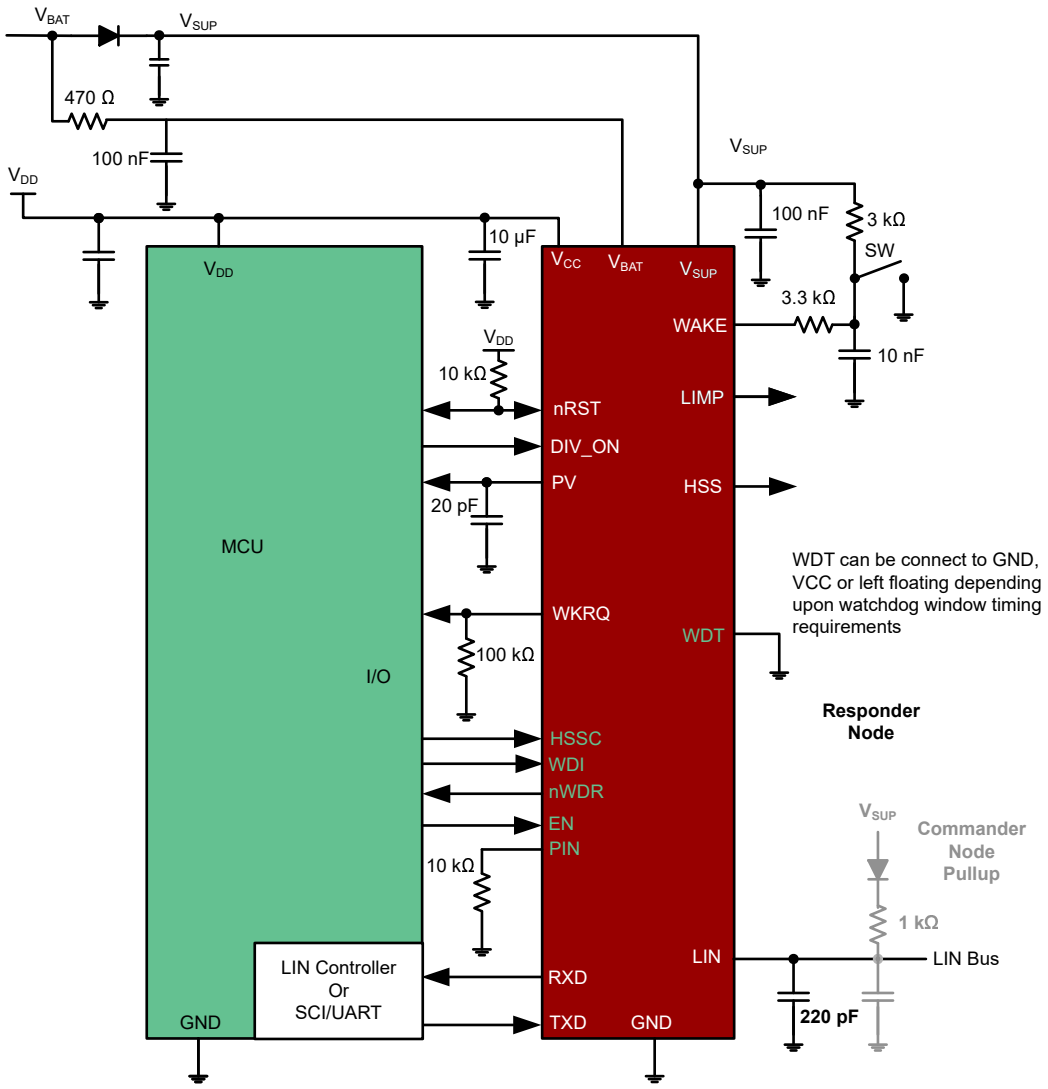


図 9-4. Typical LIN Responder Node in Pin Control Mode

9.2.1 Design Requirements

9.2.1.1 Normal Mode Application Note

When using the TLIN1431x-Q1 in systems which are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE}. This is shown in 図 7-5. When transitioning to normal mode, there is an initialization period shown as $t_{NOMINIT}$.

9.2.1.2 Standby Mode Application Note

If the TLIN1431x-Q1 detects an under-voltage on V_{SUP}, the RXD pin transitions low, and signals to the software that the device is in standby mode and should be returned to sleep mode for the lowest power state.

9.2.1.3 TXD Dominant State Timeout Application Note

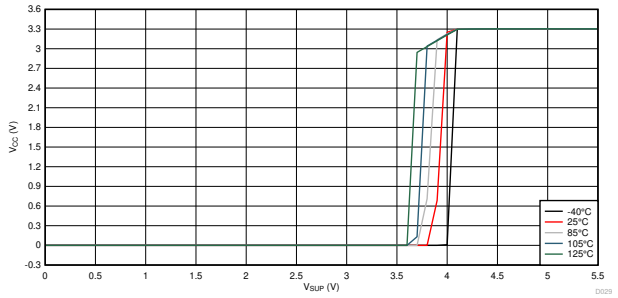
The minimum dominant TXD time allowed by the minimum t_{TXD_DTO} limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander and responder node applications. Thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

9.2.2 Detailed Design Procedures

Commander node applications require and external 1 kΩ pull-up resistor and serial diode.

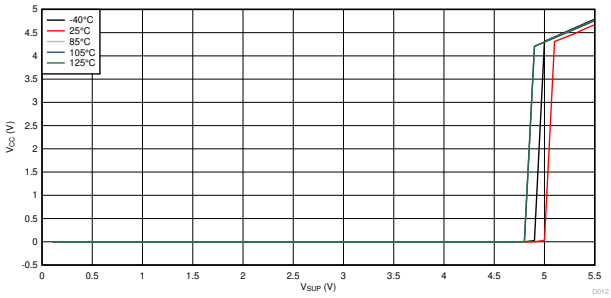
9.2.3 Application Curves

The characteristic curves show the LDO performance between 0 V and 5.5 V when ramping up and ramping down.



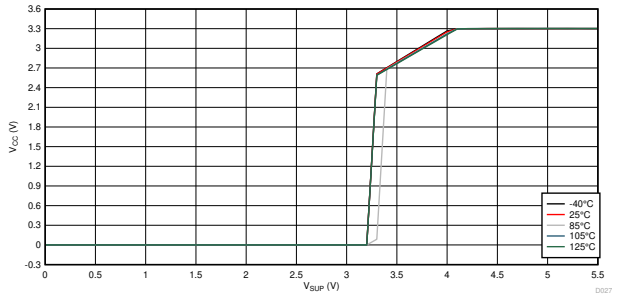
V_{CC} = 3.3 V I_{CC} Load = 125 mA Ramp Up

図 9-5. V_{CC} vs V_{SUP} Across Temperature



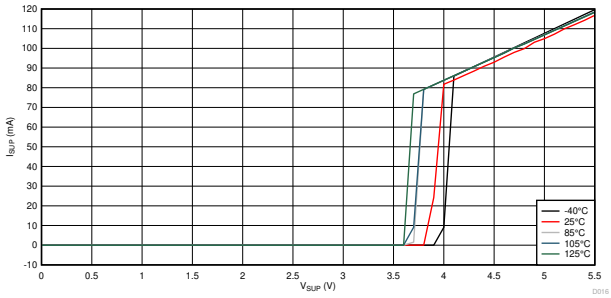
V_{CC} = 5 V I_{CC} Load = 125 mA Ramp Down

図 9-6. V_{CC} vs V_{SUP} Across Temperature



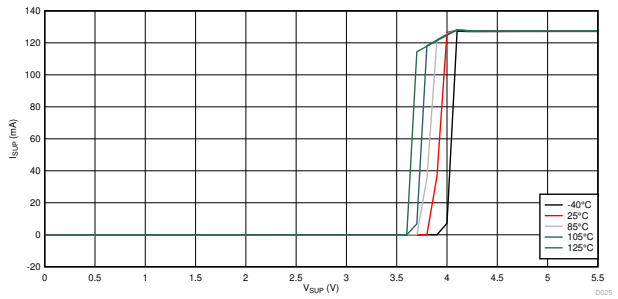
V_{CC} = 3.3 V I_{CC} Load = 125 mA Ramp Down

図 9-7. V_{CC} vs V_{SUP} Across Temperature



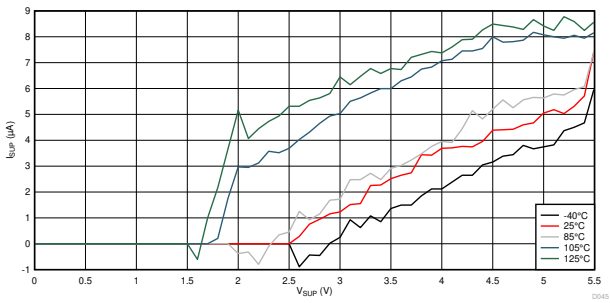
V_{CC} = 5 V I_{CC} Load = 125 mA Ramp Up

図 9-8. I_{SUP} vs V_{SUP} Across Temperature



V_{CC} = 3.3 V I_{CC} Load = 125 mA Ramp Up

図 9-9. I_{SUP} vs V_{SUP} Across Temperature



V_{CC} = 5 V Sleep Mode Ramp Down

図 9-10. I_{SUP} vs V_{SUP} Across Temperature

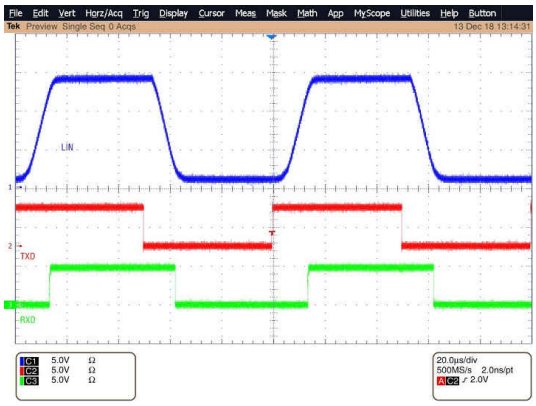


図 9-11. LIN Bus Performance

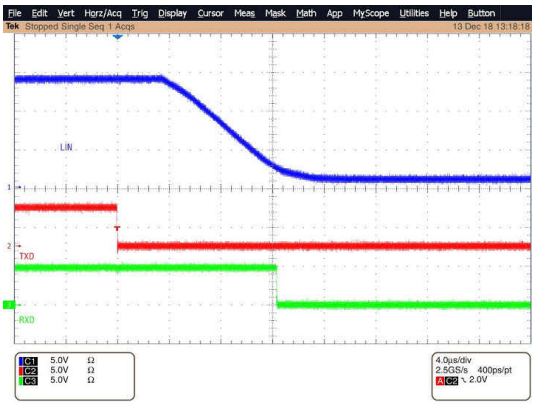


図 9-12. Recessive to Dominant Propagation Delay

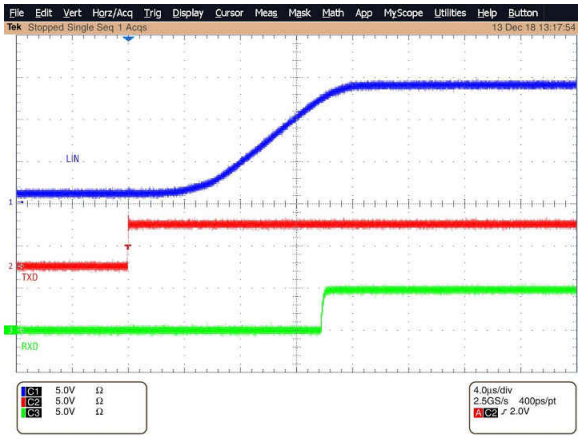


図 9-13. Dominant to Recessive Propagation Delay

9.3 Power Supply Recommendations

The TLIN1431x-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5.5 V to 28 V. A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

9.4 Layout

PCB design should start with design of the protection and filtering circuitry because ESD and EFT have a wide frequency bandwidth from approximately 3 MHz to 3 GHz. High frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

9.4.1 Layout Guidelines

The layout example and information below are for a responder node with the following configuration: See 図 9-14.

- Responder node
- SPI control
- WKRQ
- WAKE and High-side switch configured for cyclic sensing

The following are the layout guidelines based upon the provided configuration:

- **Pin 1 (V_{SUP}):** This is the supply pin for the device. A 100 nF decoupling capacitor (C1) should be placed as close to the device as possible. Other bulk decoupling capacitance should be considered.
- **Pin 2 (V_{CC}):** Output source, either 3.3 V or 5 V depending upon the version of the device and has a 10 µF decoupling capacitor (C2) to ground as close to the device as possible. This pin is connected to external circuitry for a limp home mode if the watchdog has timed out causing a reset
- **Pin 3 (nRST):** This pin connects to the processors and functions in one of two manners; as a reset pin for the TLIN1431x-Q1 or an indicator to the processor of an under-voltage and watchdog failure event. The pin has a 10 kΩ resistor (R1) pulled up to the processor I/O voltage rail.
- **Pin 4 (WDT/CLK):** In SPI control mode, this pin (CLK) is connected directly to the processor as the SPI CLK input to the TLIN1431x-Q1.
- **Pin 5 (nWDR/SDO):** In SPI control mode, this pin (SDO) is connected directly to the processor as the SPI serial data output from the TLIN1431x-Q1.
- **Pin 6 (WDI/SDI):** In SPI control mode, this pin (SDI) is connected directly to the processor as the SPI serial data input into the TLIN1431x-Q1.
- **Pin 7 (PIN/nCS):** For SPI control mode, this pin (nCS) should be connected directly to the processor as the SPI chip select to the TLIN1431x-Q1.
- **Pin 8 (EN/nINT):** In SPI control mode, this pin becomes an output interrupt pin that is provided to the processor.
- **Pin 9 (HSSC/FSO):** In SPI control mode, this pin (FSO) is connected directly to the processor, external transceiver or general purpose SBC as a selectable interrupt or control pin.
- **Pin 10 (PV):** This pin is connected directly to a processor ADC and has a 20 pF capacitor (C3) to GND.
- **Pin 11 (DIV_ON):** The pin is connected to a processor which controls when the V_{BAT} monitoring in the TLIN1431x-Q1 is enabled.
- **Pin 12 (TXD):** The TXD pin is the LIN transceiver input from the processors. A series resistor can be placed to limit the input current to the device in the event of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise. These are system level dependent and not covered here as usually not needed.
- **Pin 13 (RXD):** The RXD is the LIN transceiver receive output to the processor. The pin is a push-pull output and can be connected directly to the processor without external pull-ups.
- **Pin 14 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 15 (LIN):** This pin connects to the LIN bus. For responder nodes, a 220 pF capacitor (C4) to ground is implemented. For commander nodes, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin.
- **Pin 16 (WKRQ/INH):** This pin can be the high-voltage inhibit output pin or the digital wake output pin. The example shows the pin configured as WKRQ which requires a 100 kΩ resistor (R2) to ground at power up.
- **Pin 17 (WAKE):** This pin connects to V_{SUP} through a resistor divider (R3 and R4) with the center tap connected to a switch to ground or V_{SUP} and is used as the local wake up pin. A 10 nF capacitor (C5) to

ground should be placed at this center tap as shown in the application drawings. In the layout example, the pin is configured to work with the HSS pin using the cyclic sensing wake capability of the device.

- **Pin 18 (HSS):** This pin is the high-side switch output
- **Pin 19 (LIMP):** This pin as a high-side switch that is used for a limp home function that provides V_{SUP} to an external circuit which is not shown.
- **Pin 20 (VBAT):** This pin is used for battery monitoring is comes from the battery prior to the blocking diode. It has a 470 Ω resistor (R5) in series and a 100 nF capacitor (C6) to GND.

注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

9.4.2 Layout Example

This is a layout example for the TLIN1431x-Q1 configured for SPI control supporting following:

- Cyclic Sensing using the WAKE pin and HSS pin
- Digital wake output, WKRQ pin.

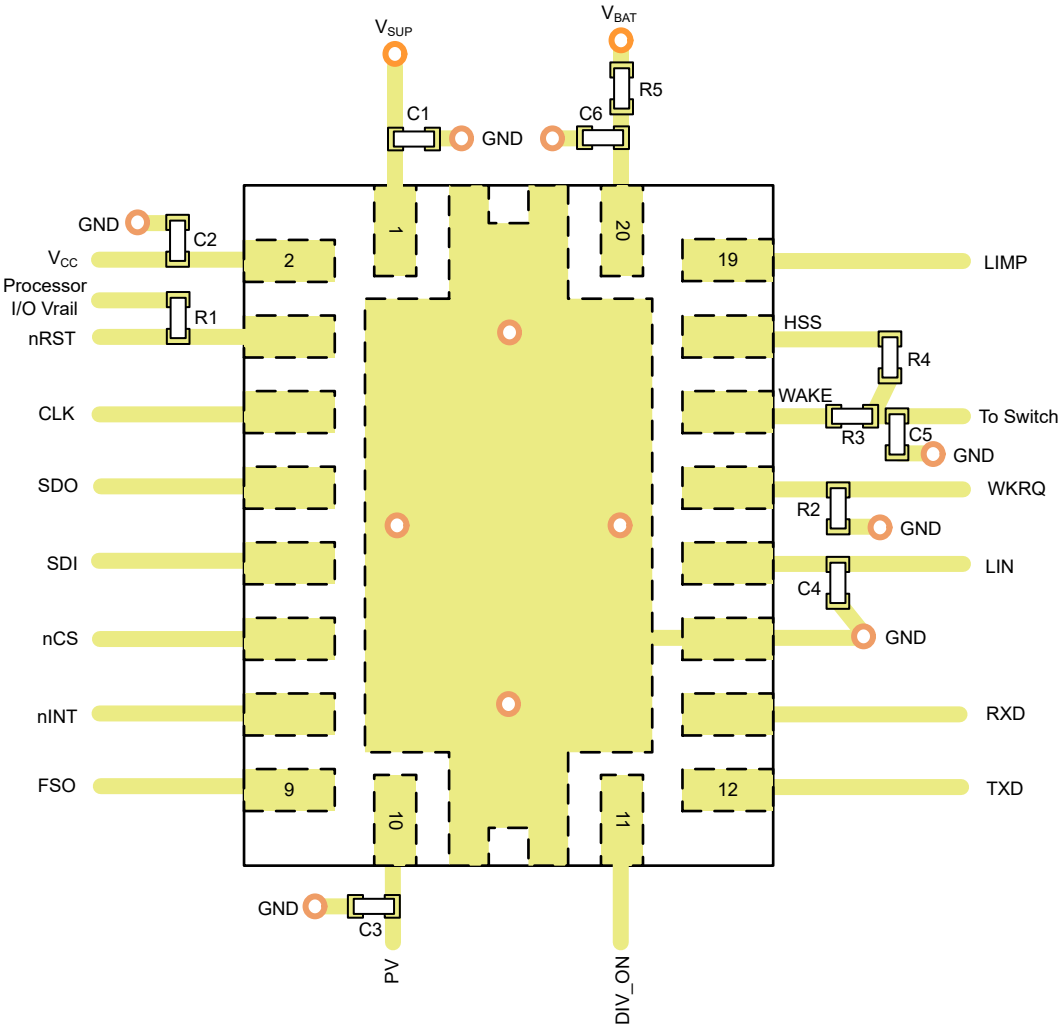


図 9-14. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- LIN Standards:
  - ISO 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
  - ISO 17987-4:2016: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
  - SAEJ2602-1:2021: LIN Network for Vehicle Applications
  - LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification
- EMC requirements:
  - SAE J2962-2:
  - HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for LIN
  - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
  - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
  - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
  - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
  - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
  - IEC 61000-4-2
  - IEC 61967-4
  - CISPR25
- Conformance Test requirements:
  - ISO 17987-7: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
  - SAE J2602-2:2021: LIN Network for Vehicle Applications Conformance Test

Application Notes:

TLINx441 LDO Performance, SLLA427

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.4 商標

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLIN14313RGYRQ1	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL313	Samples
TLIN14315RGYRQ1	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL315	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265