

## 6.25-Gbps Cable and PC Board Equalizer

Check for Samples: [TLK6201EA](#)

### FEATURES

- **Multirate Operation up to 6.25 Gbps**
- **Compensates for up to 13-dB Loss on the Receive Side and up to 12-dB Loss on the Transmit Side at 3.125 GHz**
- **Suitable to Receive and Transmit 6.25-Gbps Data Over up to 60 Inches (1.5 Meters) of FR4 PC Boards**
- **Suitable to Receive and Transmit 6.25-Gbps Data Over up to 63 Feet (19.2 Meters) of 24-AWG Cable**
- **Ultralow Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable/Squelch Function**
- **Loss of Signal Detection**
- **Output Swing Select**
- **Output De-Emphasis Select**
- **Output Polarity Select**
- **CML Data Outputs**
- **Single 3.3-V Supply**
- **Surface-Mount, Small-Footprint, 3-mm × 3-mm, 16-Pin QFN Package**

### APPLICATIONS

- **High-Speed Links in Communication and Data Systems**
- **Backplane, Daughtercard, and Cable Interconnects for PCI Express, InfiniBand, SAS, CEI, XAUI, Fibre Channel, and Ethernet**

### DESCRIPTION

The TLK6201EA is a versatile, high-speed, limiting equalizer for applications in digital high-speed links with data rates up to 6.25 Gbps.

This device provides a high-frequency boost of 13 dB on the received data at 3.125 GHz, as well as sufficient gain to ensure a fully differential output swing for input signals as low as 100 mVp-p (at the input of a lossy interconnect line).

Four de-emphasis levels can be selected on the transmit side to provide up to 12 dB of additional high-frequency loss compensation.

The high input-signal dynamic range ensures low-jitter output signals even when overdriven with input signal swings as high as 2000 mVp-p.

The TLK6201EA implements fixed loss-of-signal detection, which can be used to implement a squelch function by connecting the LOS output to the adjacent DIS input.

The TLK6201EA is available in a small-footprint, 3-mm × 3-mm, 16-pin QFN package. It requires a single 3.3-V supply.

This power-efficient equalizer is characterized for operation from –40°C to 85°C.



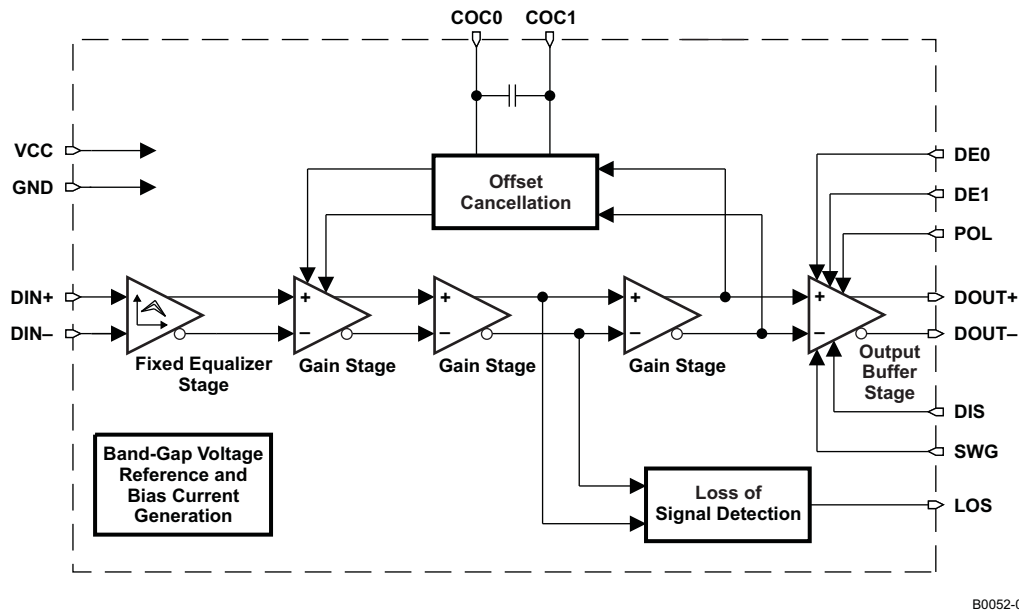
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## BLOCK DIAGRAM

A simplified block diagram of the TLK6201EA is shown in Figure 1. This compact, low-power, 6.25-Gbps equalizer consists of a high-speed data path with offset cancellation circuitry, a loss-of-signal detection block, and a band-gap voltage reference and bias current generation block. The equalizer requires a single 3.3-V  $\pm 10\%$  supply voltage. All circuit parts are described in detail as follows.



B0052-04

Figure 1. Simplified Block Diagram of the TLK6201EA

## HIGH-SPEED DATA PATH

The high-speed data signal with frequency-dependent loss is applied to the data path by means of the input signal pins DIN+/DIN-. The data path consists of the fixed equalizer input stage, three gain stages which provide the required gain to ensure a limited-output signal, and an output buffer stage. The equalized and amplified data output signal is available at the output pins DOUT+/DOUT-, which provide  $2 \times 50\text{-}\Omega$  back-termination to VCC. The output stage also includes a data polarity-switching function, which is controlled by the POL input, and a disable function, controlled by the signal applied to the DIS input pin.

The output swing can be increased 50% by applying a high-level signal to the SWG pin.

Up to 12 dB of output signal de-emphasis can be selected using the pins DE0 and DE1.

An offset cancellation compensates the inevitable internal offset voltages and thus ensures proper operation even for very small input data signals.

The low-frequency cutoff is as low as 3.5 kHz with the built-in filter capacitor. For applications which require even lower cutoff frequencies, an additional external filter capacitor can be connected to the COC0/COC1 pins.

## LOSS-OF-SIGNAL DETECTION

The output signal of the second gain stage is monitored by the loss-of-signal detection circuitry. In this block, the input signal is compared to a fixed threshold. If the low frequency components of the input signal fall below this threshold, a loss of signal is indicated at the LOS pin.

A squelch function can be easily implemented by connecting the LOS output to the adjacent DIS input. This measure avoids chattering of the output when no input signal is present.

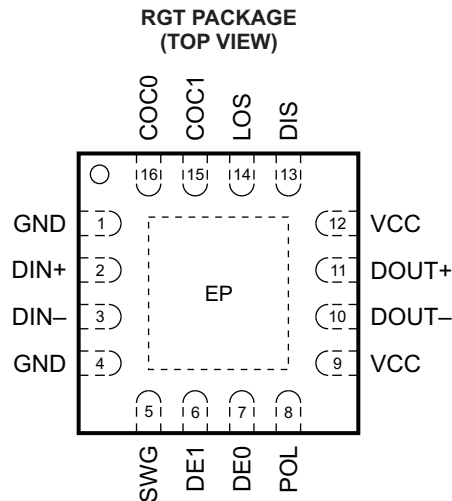
## BAND-GAP VOLTAGE AND BIAS GENERATION

The TLK6201EA equalizer is supplied by a single 3.3-V  $\pm 10\%$  supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip band-gap voltage circuit generates a supply-voltage-independent reference from which all internally required voltages and bias currents are derived.

## DEVICE INFORMATION

The TLK6201EA is available in a small-footprint, 3-mm  $\times$  3-mm, 16-pin QFN package, with a lead pitch of 0.5 mm. The pinout is shown in [Figure 2](#).



P0019-04

Figure 2. Pinout of TLK6201EA

Table 1. PIN FUNCTIONS

| PIN   |          | TYPE      | DESCRIPTION  |
|-------|----------|-----------|--|
| NAME  | NO.      |           |  |
| COC0  | 16       | Analog    | Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 15). To disable the offset cancellation loop, connect COC1 and COC0 (pins 15 and 16). |
| COC1  | 15       | Analog    | Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC0 (pin 16). To disable the offset cancellation loop, connect COC1 and COC0 (pins 15 and 16). |
| DE0   | 7        | CMOS in   | Selects 4 dB of output signal de-emphasis when set to high level. Internally pulled up.  |
| DE1   | 6        | CMOS in   | Selects 8 dB of output signal de-emphasis when set to high level. Internally pulled up.  |
| DIN+  | 2        | Analog in | Noninverted data input. On-chip load terminated to ground. Connect a 100- $\Omega$ differential transmission line to terminals DIN+ and DIN-.  |
| DIN-  | 3        | Analog in | Inverted data input. On-chip load terminated to ground. Connect a 100- $\Omega$ differential transmission line to terminals DIN+ and DIN-.   |
| DIS   | 13       | CMOS in   | Disables CML output stage when set to high level. Internally pulled down.  |
| DOUT+ | 11       | CML out   | Noninverted data output. On-chip 50- $\Omega$ back-terminated to VCC.  |
| DOUT- | 10       | CML out   | Inverted data output. On-chip 50- $\Omega$ back-terminated to VCC.   |
| GND   | 1, 4, EP | Supply    | Circuit ground. Exposed die pad (EP) must be grounded.   |
| LOS   | 14       | CMOS out  | High level indicates that the input signal amplitude is below the fixed threshold level.   |
| POL   | 8        | CMOS in   | Output data signal polarity select (internally pulled up): Setting to high level or leaving pin open selects normal polarity. Low level selects inverted polarity.   |
| SWG   | 5        | CMOS in   | Output swing control. The output swing is increased by 50% when set to high level. Internally pulled down.   |
| VCC   | 9, 12    | Supply    | 3.3-V, $\pm 10\%$ supply voltage   |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|  |   | VALUE <sup>(1)</sup> | UNIT |
|--|---|----------------------|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                                 | –0.3 to 4            | V    |
| V <sub>DIN+</sub> , V <sub>DIN–</sub>  | Voltage at DIN+, DIN– <sup>(2)</sup>                          | 0.5 to 4             | V    |
| V <sub>DIS</sub> , V <sub>POL</sub> , V <sub>DE1</sub> ,<br>V <sub>DE0</sub> , V <sub>SWG</sub> , V <sub>COC1</sub> ,<br>V <sub>COC0</sub> | Voltage at DIS, POL, DE1, DE0, SWG, COC1, COC0 <sup>(2)</sup> | –0.3 to 4            | V    |
| V <sub>COC,DIFF</sub>  | Differential input voltage between COC1 and COC0              | ±1                   | V    |
| V <sub>DIN,DIFF</sub>  | Differential input voltage between DIN+ and DIN–              | ±2.5                 | V    |
| I <sub>DIN+</sub> , I <sub>DIN–</sub> , I <sub>DOUT+</sub> ,<br>I <sub>DOUT–</sub>   | Continuous current at inputs and outputs                      | ±25                  | mA   |
| ESD  | ESD ratings at all pins, human body model (HBM)               | 3                    | kV   |
| T <sub>J,max</sub>   | Maximum junction temperature                                  | 125                  | °C   |
| T <sub>stg</sub>   | Storage temperature range                                     | –65 to 150           | °C   |
| T <sub>A</sub>   | Characterized free-air operating temperature range            | –40 to 85            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                 |                                | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|-----|------|
| V <sub>CC</sub> | Supply voltage                 | 3   | 3.3 | 3.6 | V    |
| T <sub>A</sub>  | Free-air operating temperature | –40 |     | 85  | °C   |
| V <sub>IH</sub> | High-level input voltage, CMOS | 2   |     |     | V    |
| V <sub>IL</sub> | Low-level input voltage, CMOS  |     |     | 0.8 | V    |

## DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                     | MIN                        | TYP | MAX | UNIT |
|------------------|---|----------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage                                      | 3                          | 3.3 | 3.6 | V    |
| I <sub>CC</sub>  | DIS = SWG = low (includes CML output current)       |                            | 45  | 54  | mA   |
|                  | DIS = low, SWG = high (includes CML output current) |                            | 55  | 67  |      |
| R <sub>OUT</sub> | Output resistance, data                             |                            | 50  |     | Ω    |
|                  | LOS high voltage                                    | I <sub>source</sub> = 1 mA | 2.5 |     | V    |
|                  | LOS low voltage                                     | I <sub>sink</sub> = 1 mA   |     | 0.5 | V    |

## AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

| PARAMETER                     |  | TEST CONDITIONS   | MIN              | TYP            | MAX              | UNIT              |
|-------------------------------|--|---|------------------|----------------|------------------|-------------------|
| Low frequency –3-dB bandwidth |  | $C_{OC} = \text{open}$  |                  | 3.5            | 10               | kHz               |
|                               |  | $C_{OC} = 100\text{ nF}$  |                  | 0.8            |                  |                   |
| Maximum data rate             |  |   | 6.25             |                |                  | Gbps              |
| $V_{IN,MIN}$                  | Data input sensitivity <sup>(1)</sup>              | BER < $10^{-12}$ , K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4, including two through-hole SMA connectors. Voltage measured at the input of the interconnect line.                                  |                  | 40             | 50               | mV <sub>P-P</sub> |
| $V_{IN,MAX}$                  | Data input overload                                | Voltage at the input of an interconnect line  | 2000             |                |                  | mV <sub>P-P</sub> |
|                               | High-frequency boost                               | $f = 3.125\text{ GHz}$ (fixed input equalizer)  | 12               | 14             | 17               | dB                |
| $V_{OD}$                      | Differential data output voltage swing             | DIS = low, SWG = low  | 600              | 800            | 1000             | mV <sub>P-P</sub> |
|                               |  | DIS = low, SWG = high   | 900              | 1200           | 1500             |                   |
| $V_{RIP}$                     | Differential output ripple                         | DIS = high, 50% transitions of K28.5 pattern at 6.25 Gbps, no interconnect line, $V_{IN} = 2000\text{ mVp-p}$   |                  | 0.25           | 10               | mV <sub>RMS</sub> |
| $V_{CM,OUT}$                  | Data output, common-mode voltage                   | DIS = low, SWG = low, dc-coupled 50 $\Omega$ to $V_{CC}$ , single-ended terminations  | $V_{CC} - 0.25$  | $V_{CC} - 0.2$ | $V_{CC} - 0.15$  | V                 |
|                               |  | DIS = low, SWG = high, dc-coupled 50 $\Omega$ to $V_{CC}$ , single-ended terminations   | $V_{CC} - 0.375$ | $V_{CC} - 0.3$ | $V_{CC} - 0.225$ |                   |
| DE                            | Output de-emphasis (see <a href="#">Figure 3</a> ) | DE0 = low, DE1 = low  |                  | 0              |                  | dB                |
|                               |  | DE0 = high, DE1 = low   |                  | –4             |                  |                   |
|                               |  | DE0 = low, DE1 = high   |                  | –8             |                  |                   |
|                               |  | DE0 = high, DE1 = high  |                  | –12            |                  |                   |
| DJ                            | Deterministic jitter                               | K28.5 pattern at 6.25 Gbps, no interconnect line, $V_{IN} = 400\text{ mVp-p}$ , DE0 = low, DE1 = low, SWG = low   |                  | 8              |                  | ps <sub>P-P</sub> |
|                               |  | K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors, $V_{IN} = 400\text{ mVp-p}$ (voltage at the input of the interconnect line), DE0 = low, DE1 = low, SWG = low |                  | 12             |                  |                   |
| RJ                            | Random jitter                                      | K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors, $V_{IN} = 400\text{ mVp-p}$ (voltage at the input of the interconnect line), DE0 = low, DE1 = low, SWG = low |                  | 1              |                  | ps <sub>RMS</sub> |
| $t_r$                         | Output rise time                                   | 20% to 80%, no interconnect line, DE0 = low, DE1 = low  |                  | 35             | 55               | ps                |
| $t_f$                         | Output fall time                                   | 20% to 80%, no interconnect line, DE0 = low, DE1 = low  |                  | 35             | 55               | ps                |
| S11                           | Input return loss                                  | 10 Hz < $f$ < 3.1 GHz   |                  | –15            |                  | dB                |
| S22                           | Output return loss                                 | 10 Hz < $f$ < 3.1 GHz   |                  | –12            |                  | dB                |

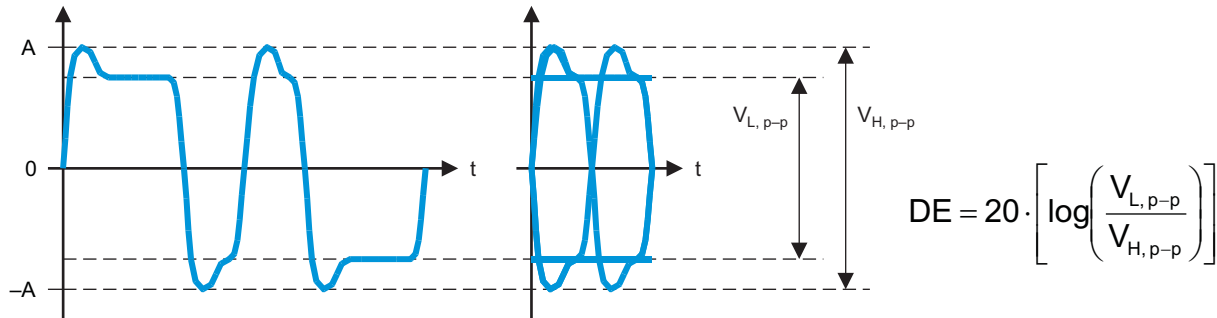
(1) The given differential input signal swing is valid for the low-frequency components of the input signal. The high-frequency components may be attenuated by up to 13 dB at 3.125 GHz.

**AC ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)  
 Typical operating condition is at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

| PARAMETER                                 | TEST CONDITIONS   | MIN | TYP | MAX | UNIT              |
|---|---|-----|-----|-----|-------------------|
| $V_{AS}$ LOS assert threshold voltage     | K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors. Voltage measured at the input of the interconnect line. <sup>(2)</sup> | 40  | 75  |     | mV <sub>P-P</sub> |
| $V_{DAS}$ LOS de-assert threshold voltage | K28.5 pattern at 6.25 Gbps over a 36-inch, 7-mil-wide stripline on standard FR4 including two through-hole SMA connectors. Voltage measured at the input of the interconnect line. <sup>(2)</sup> |     | 130 | 250 | mV <sub>P-P</sub> |
| LOS hysteresis                            | $20 \log(V_{DAS}/V_{AS})$ <sup>(2)</sup>  | 2   | 4.5 |     | dB                |
| $t_{AS/DAS}$ LOS assert/de-assert time    |   | 2   |     | 100 | $\mu\text{s}$     |
| $t_{DIS}$ Disable response time           |   |     | 20  |     | ns                |
| Latency                                   | From DIN+/DIN– to DOUT+/DOUT–   |     | 150 |     | ps                |

(2) This specification is for 0°C to 85°C. Depending on the interconnect line length and performance, the bit pattern, and the data rate, the assert and de-assert threshold voltage levels vary. For more information, see the *Typical Characteristics* section.



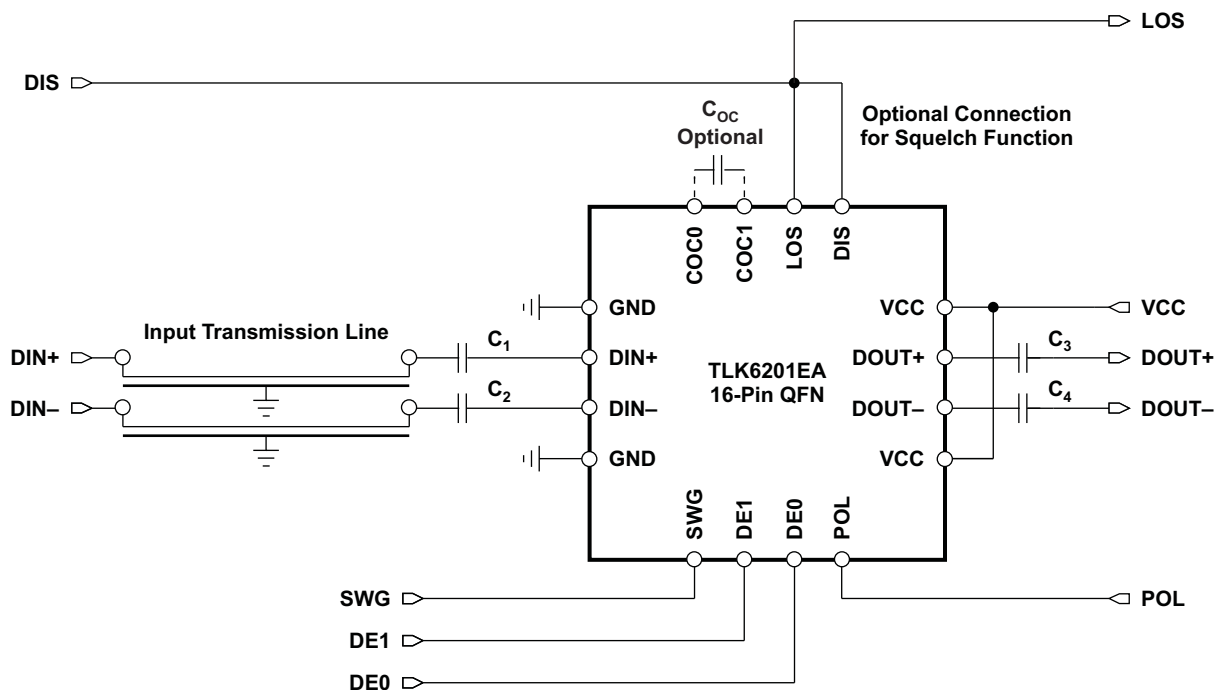
T0157-01

**Figure 3. Output Signal De-Emphasis**

APPLICATION INFORMATION

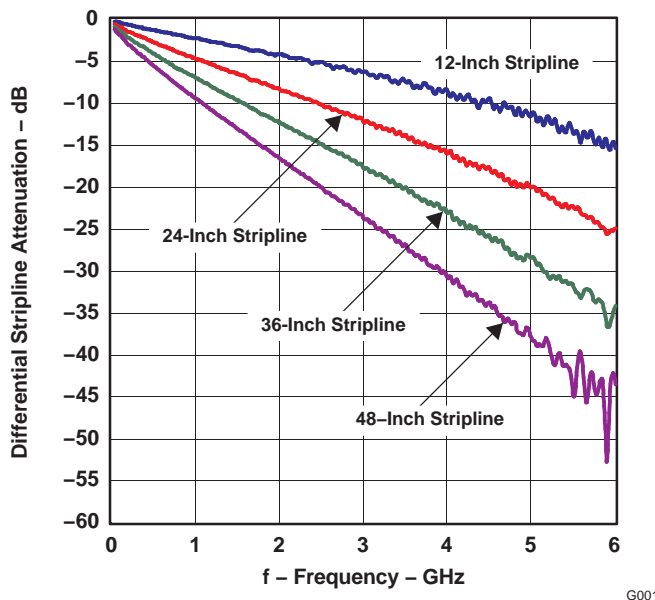
Figure 4 shows the TLK6201EA connected with an ac-coupled interface to the data signal source via a stripline transmission line on FR4 material. The output load is ac-coupled as well.

The ac-coupling capacitors C<sub>1</sub> through C<sub>4</sub> in the input and output data signal lines are the only required external components. In addition, if a very low cutoff frequency is required, as an option, an external filter capacitor C<sub>OC</sub> may be used.



S0072-04

Figure 4. Basic Application Circuit with AC-Coupled I/Os



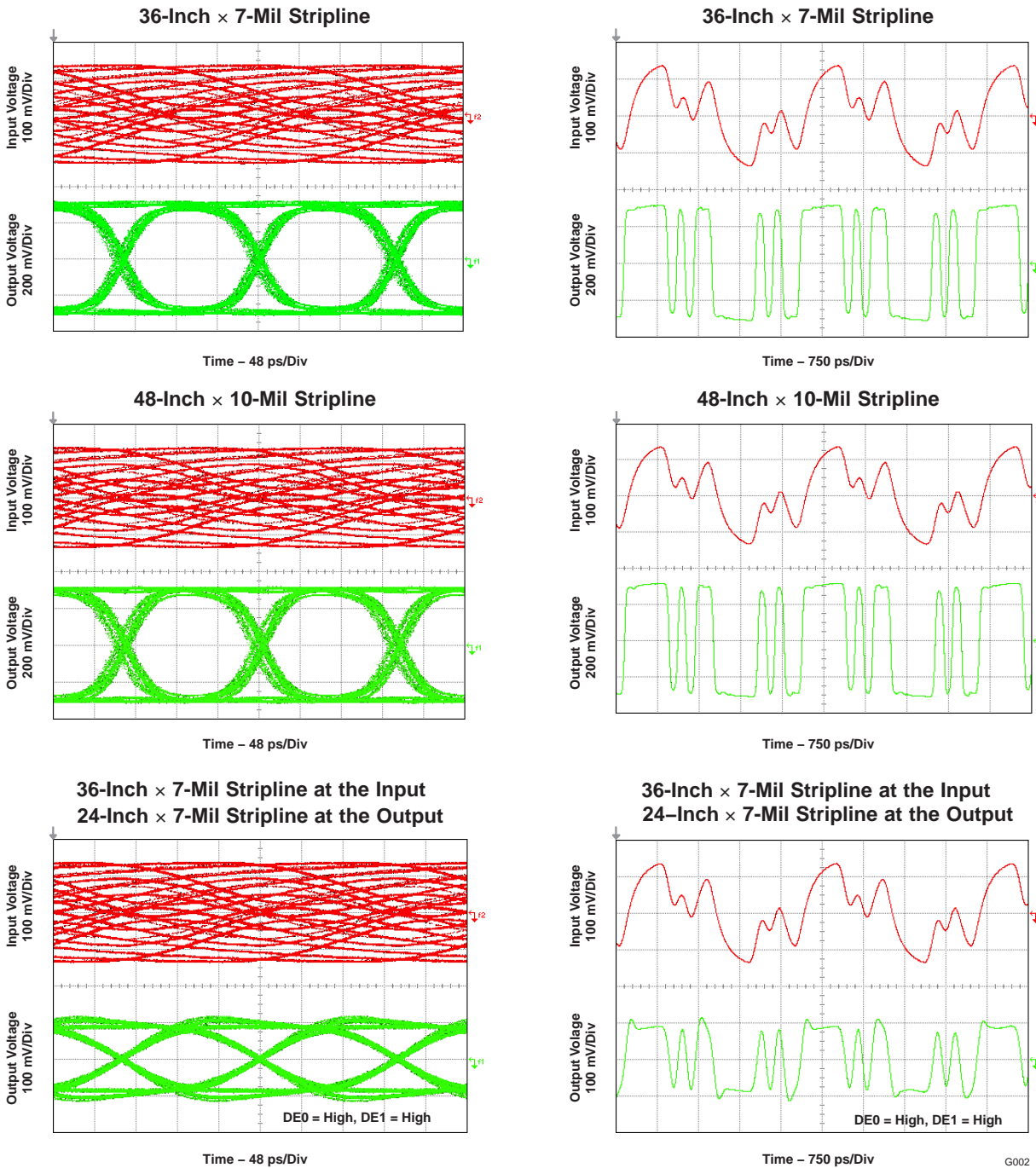
G001

Figure 5. Attenuation Characteristics of Stripline Interconnect Lines

**TYPICAL CHARACTERISTICS**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 400\text{ mVp-p}$ ,  $DE0 = \text{low}$ ,  $DE1 = \text{low}$ ,  $SWG = \text{low}$ , and no interconnect line at the output (unless otherwise noted).

**DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 6.25 GBPS USING A K28.5 PATTERN**



**Figure 6. Equalizer Input and Output Signals With Different Interconnect Lines at 6.25 Gbps**



**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 400\text{ mVp-p}$ , DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

**DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 4.25 GBPS USING A K28.5 PATTERN**

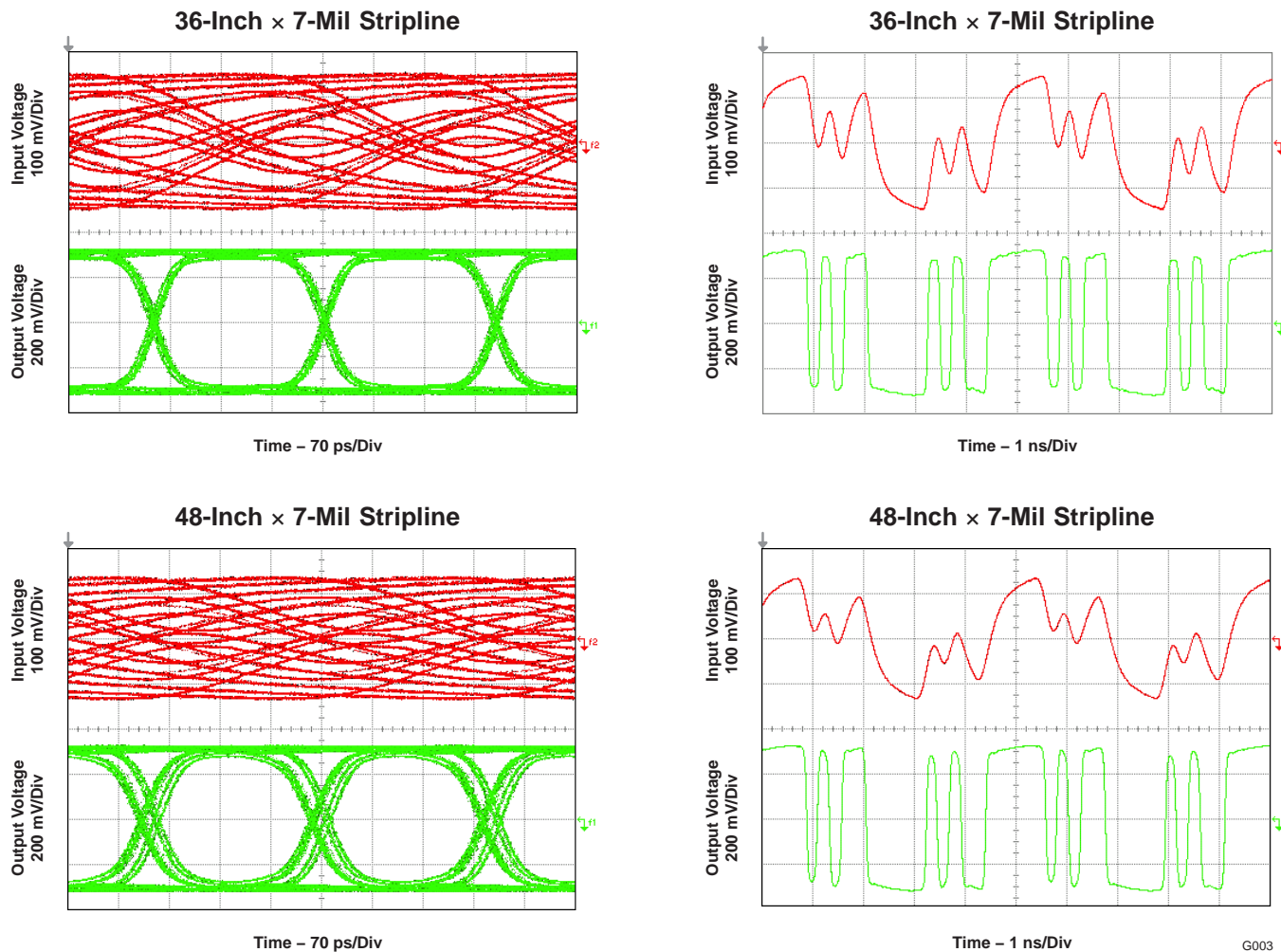
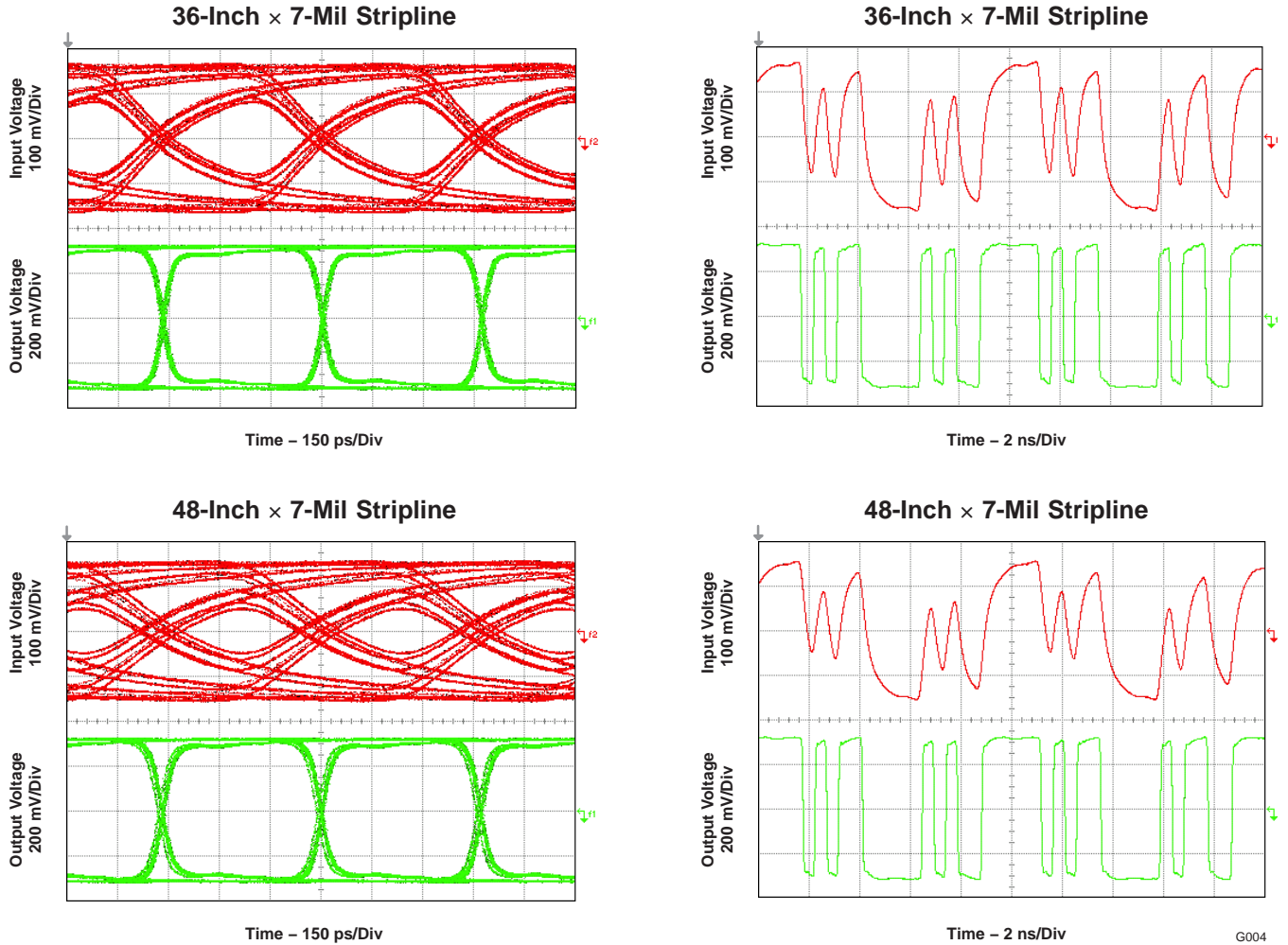


Figure 7. Equalizer Input and Output Signals With Different Interconnect Lines at 4.25 Gbps

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 400\text{ mVp-p}$ , DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

**DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 2.125 GBPS USING A K28.5 PATTERN**



**Figure 8. Equalizer Input and Output Signals With Different Interconnect Lines at 2.125 Gbps**

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 400\text{ mVp-p}$ , DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

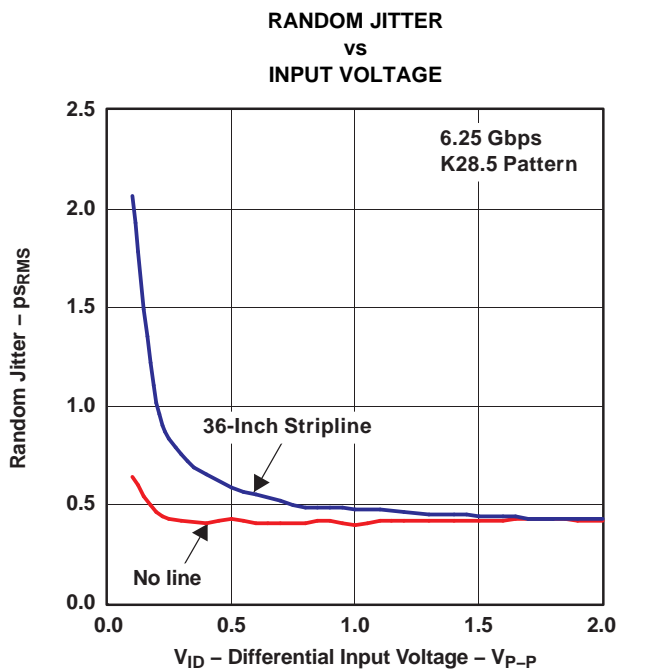


Figure 9.

G005

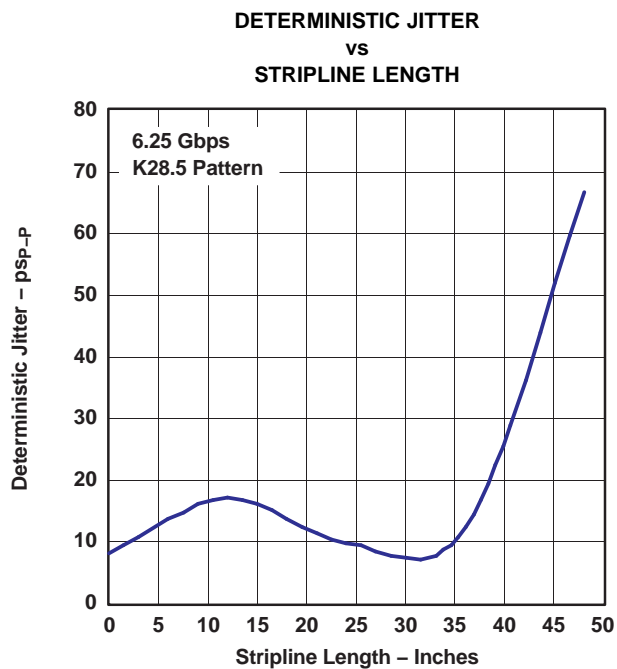


Figure 10.

G006

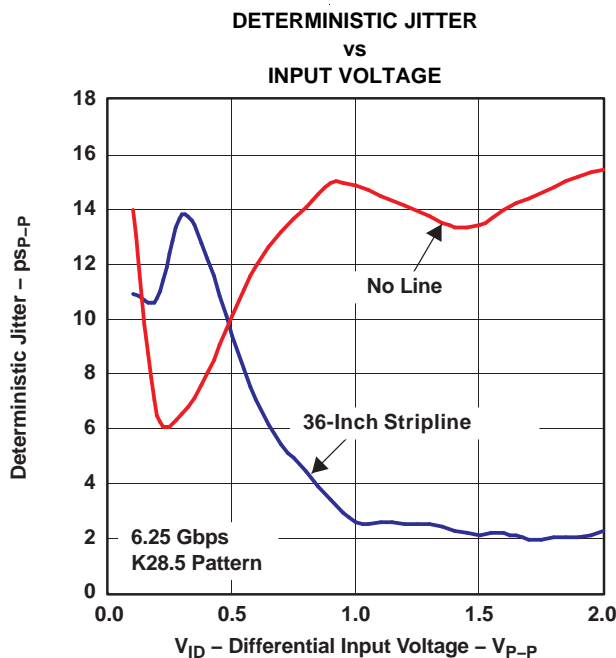


Figure 11.

G007

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , DE0 = low, DE1 = low, SWG = low, and no interconnect line at the output (unless otherwise noted).

**DIFFERENTIAL INPUT RETURN LOSS  
vs  
FREQUENCY**

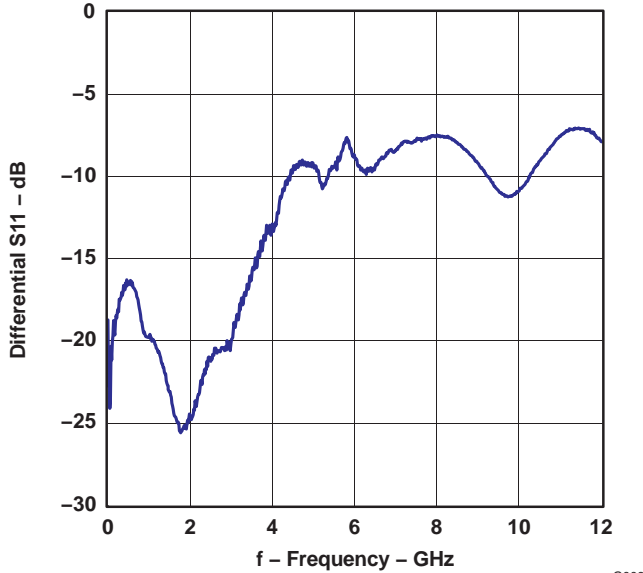


Figure 12.

G008

**DIFFERENTIAL OUTPUT RETURN LOSS  
vs  
FREQUENCY**

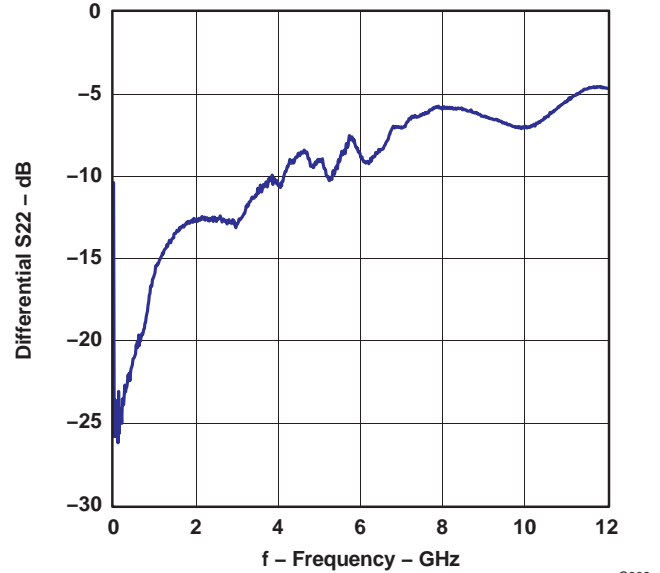


Figure 13.

G009

**LOS ASSERT THRESHOLD VOLTAGE  
vs  
DATA RATE**

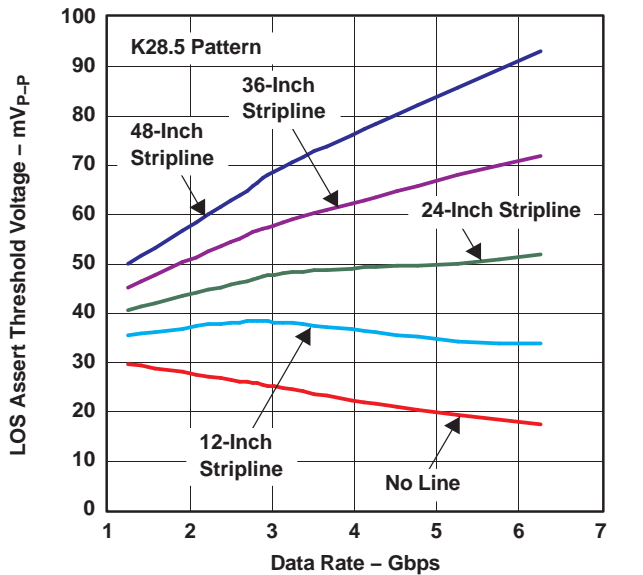


Figure 14.

G010

**LOS DE-ASSERT THRESHOLD VOLTAGE  
vs  
DATA RATE**

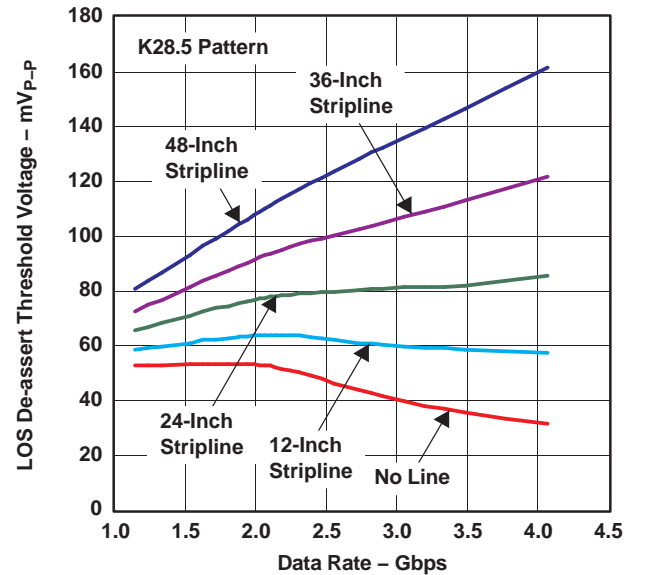


Figure 15.

G011

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**REVISION HISTORY**

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**Changes from Original (August 2006) to Revision A** **Page**

- 
- Changed the LOS hysteresis MIN value From: 2.5 dB To: 2 dB ..... [6](#)
- 

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**Changes from Revision A (October 2007) to Revision B** **Page**

- 
- Changed the  $T_{\text{stg}}$ , storage temperature range From: -65 to 85°C To: -65 to 150°C ..... [4](#)
-

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TLK6201EARGTR    | OBSOLETE      | VQFN         | RGT             | 16   |             | TBD             | Call TI                              | Call TI              | -40 to 85    | 620E                    |         |
| TLK6201EARGTT    | OBSOLETE      | VQFN         | RGT             | 16   |             | TBD             | Call TI                              | Call TI              | -40 to 85    | 620E                    |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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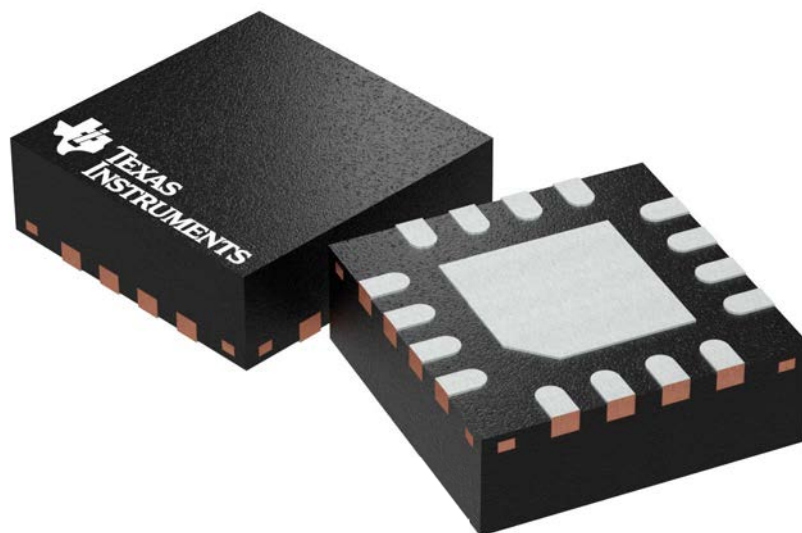
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**RGT 16**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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