

# TLV181x および TLV182x プッシュプルまたはオープン・ドレイン出力オプションを持つ 40V レール・ツー・レール入力コンパレータ・ファミリ

## 1 特長

- 2.4V~40V の広い電源電圧範囲
- レール・ツー・レール入力
- 既知のスタートアップへのパワーオン・リセット (POR)
- 低い入力オフセット電圧: 500 $\mu$ V
- 420ns (標準値) の伝搬遅延
- 低い静止電流: チャンネルごとに 5 $\mu$ A
- 低い入力バイアス電流: 150fA
- オープン・ドレイン出力オプション (TLV182x)
- プッシュプル出力オプション (TLV181x)
- 全温度範囲 (-40°C~+125°C)
- ESD 保護: 2kV
- 機能安全対応
  - 機能安全準拠のシステム設計に役立つ資料を利用可能

## 2 アプリケーション

- 家電製品
- ファクトリ・オートメーションおよび制御
- モーター・ドライブ
- インフォテインメントおよびクラスタ

## 3 概要

TLV181x および TLV182x は、複数の出力オプションを備えた 40V シングル、デュアル、クワッド・チャンネル・コンパレータのファミリです。このファミリは、プッシュプルまたはオープン・ドレイン出力オプションを持つレール・ツー・レール入力を提供します。このファミリは速度と消費電力の組み合わせが非常に優れており、伝搬遅延は 420ns、完全電源電圧範囲は 2.4V~40V、チャンネルあたりの静止電流はわずか 5 $\mu$ A です。

すべてのデバイスに、パワーオン・リセット (POR) 機能が搭載されています。これにより、出力が入力に応答する

前、最小電源電圧に達するまでの間、出力が既知の状態であることが保証されるため、システムの電源オンおよび電源オフ時に誤った出力が発生することを防止できます。

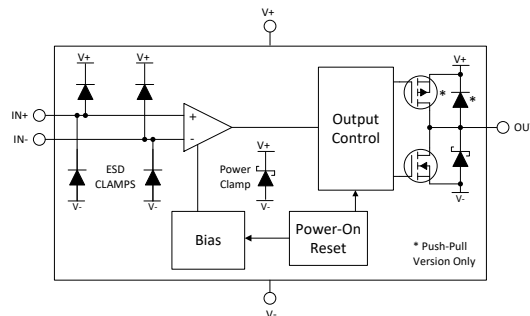
TLV181x コンパレータは、LED の制御、または MOSFET ゲートなどの容量性負荷の駆動を行うときに数ミリアンペアの電流をシンクおよびソースできるプッシュプル出力段を備えています。

TLV182x コンパレータは、コンパレータの電源電圧に関係なく最大 40V までプルアップできるオープン・ドレイン出力段を備えています。

### 製品情報

| 部品番号                                     | パッケージ <sup>(1)</sup> | 本体サイズ (公称)      |
|--|----------------------|-----------------|
| TLV1811、<br>TLV1821<br>(シングル)            | SC-70 (6)            | 1.25mm x 2.00mm |
|  | SOT-23 (5)           | 1.60mm x 2.90mm |
| TLV1811L、<br>TLV1821L<br>(シングル - 代替ピン配置) | SC-70 (5)            | 1.25mm x 2.00mm |
|  | SOT-23 (5)           | 1.60mm x 2.90mm |
| TLV1812、<br>TLV1822<br>(デュアル)            | SOIC (8)             | 3.91mm x 4.90mm |
|  | TSSOP (8)            | 3.00mm x 4.40mm |
|  | VSSOP (8)            | 3.00mm x 3.00mm |
|  | WSON (8)             | 2.00mm x 2.00mm |
|  | SOT-23 (8)           | 1.60mm x 2.90mm |
| TLV1814、<br>TLV1824<br>(クワッド)            | SOIC (14)            | 3.91mm x 8.65mm |
|  | TSSOP (14) (プレビュー)   | 4.40mm x 5.00mm |
|  | SOT-23 (14) (プレビュー)  | 4.20mm x 2.00mm |
|  | WQFN (16) (プレビュー)    | 3.00mm x 3.00mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TLV18xx のブロック図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

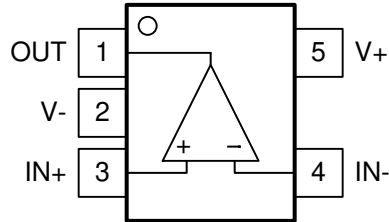
| <b>Changes from Revision B (December 2022) to Revision C (September 2023)</b> | <b>Page</b> |
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| • 複数のデュアルおよびクワッド SOIC リリースのプレビューを削除.....                                      | 1           |

| <b>Changes from Revision A (November 2022) to Revision B (December 2022)</b> | <b>Page</b> |
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| • TLV1811/21 シングル・リリースのプレビューを削除.....   | 1           |

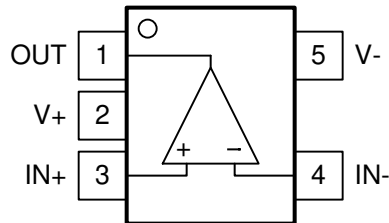
| <b>Changes from Revision * (September 2022) to Revision A (November 2022)</b> | <b>Page</b> |
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| • TLV1812/22 デュアル SOIC リリースのプレビューを削除.....                                     | 1           |

## 5 Pin Configuration and Functions

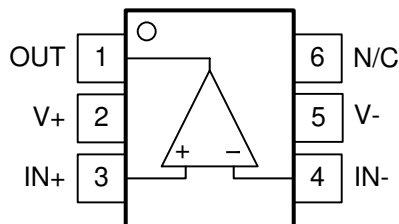
### Pin Functions: TLV18x1 and TLV18x1L



**TLV1811 and TLV1821**  
Standard "North West" pinout  
DBV, DCK Packages,  
SOT-23-5, SC-70-5  
Top View



**TLV1811L and TLV1821L DBV Package,**  
"LMC72x1/TLV72x1 type" pinout with reversed supplies  
SOT-23-5,  
Top View



**TLV1811L and TLV1821L DCK Package,**  
"TLV72x1 6-pin type" pinout with reversed supplies and shifted V-  
SC-70-6,  
Top View

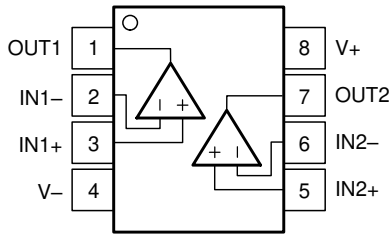
**表 5-1. Pin Functions: TLV1811, TLV1821, TLV1811L and TLV1821L**

| NAME | TLV1811, TLV1821 |       | TLV1811L, TLV1821L |       | I/O | DESCRIPTION             |
|------|------------------|-------|--------------------|-------|-----|-------------------------|
|      | PINS             |       | PINS               |       |     |                         |
|      | SOT-23           | SC-70 | SOT-23             | SC-70 |     |                         |
| OUT  | 1                | 1     | 1                  | 1     | O   | Output                  |
| V-   | 2                | 2     | 5                  | 5     | -   | Negative Supply Voltage |
| IN+  | 3                | 3     | 3                  | 3     | I   | Non-Inverting (+) Input |
| IN-  | 4                | 4     | 4                  | 4     | I   | Inverting (-) Input     |
| V+   | 5                | 5     | 2                  | 2     | -   | Positive Supply Voltage |

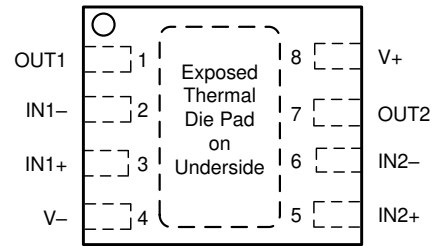
**表 5-1. Pin Functions: TLV1811, TLV1821, TLV1811L and TLV1821L (continued)**

| NAME | TLV1811, TLV1821 |       | TLV1811L, TLV1821L |       | I/O | DESCRIPTION   |
|------|------------------|-------|--------------------|-------|-----|---------------|
|      | PINS             |       | PINS               |       |     |               |
|      | SOT-23           | SC-70 | SOT-23             | SC-70 |     |               |
| N/C  | -                | -     | -                  | 6     | -   | No Connection |

**Pin Functions: TLV1812 and TLV1822**



**D, DGK, PW, DDF Packages  
8-Pin SOIC, VSSOP, TSSOP, SOT-23-8  
Top View**



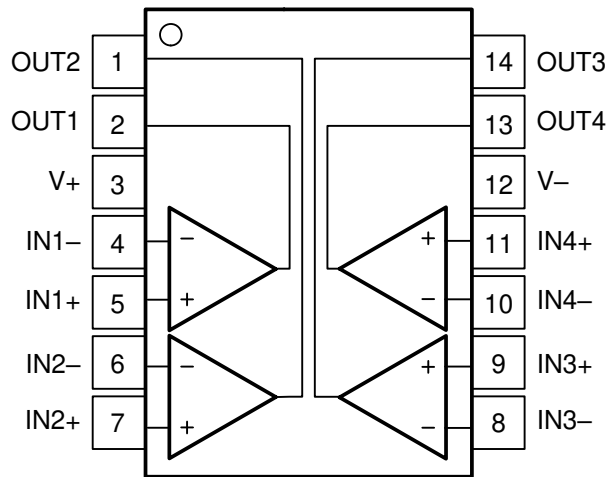
NOTE: Connect exposed thermal pad directly to V- pin.

**DSG Package,  
8-Pad WSON With Exposed Thermal Pad,  
Top View**

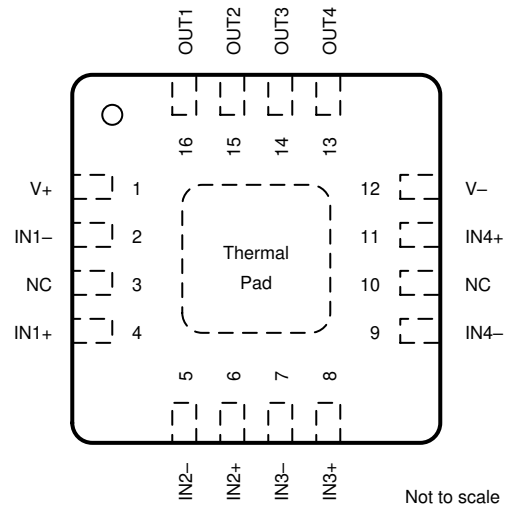
**表 5-2. Pin Functions: TLV1812 and TLV1822**

| PIN         |     | I/O | DESCRIPTION                            |
|-------------|-----|-----|--|
| NAME        | NO. |     |  |
| OUT1        | 1   | O   | Output pin of the comparator 1         |
| IN1-        | 2   | I   | Inverting input pin of comparator 1    |
| IN1+        | 3   | I   | Noninverting input pin of comparator 1 |
| V-          | 4   | —   | Negative (low) supply                  |
| IN2+        | 5   | I   | Noninverting input pin of comparator 2 |
| IN2-        | 6   | I   | Inverting input pin of comparator 2    |
| OUT2        | 7   | O   | Output pin of the comparator 2         |
| V+          | 8   | —   | Positive supply                        |
| Thermal Pad | —   | —   | Connect directly to V- pin             |

### Pin Functions: TLV1814 and TLV1824



**D, PW, DYY Package, 14-Pin SOIC, TSSOP, SOT-23,  
Top View**



NOTE: Connect exposed thermal pad directly to V- pin.  
**RTE Package, 16-Pad WQFN With Exposed  
Thermal Pad, Top View**

**表 5-3. Pin Functions: TLV1814 and TLV1824**

| NAME                | PIN  |      | I/O | DESCRIPTION                                    |
|---------------------|------|------|-----|--|
|                     | SOIC | WQFN |     |  |
| OUT2 <sup>(1)</sup> | 1    | 15   | O   | Output pin of the comparator 2                 |
| OUT1 <sup>(1)</sup> | 2    | 16   | O   | Output pin of the comparator 1                 |
| V+                  | 3    | 1    | —   | Positive supply                                |
| IN1-                | 4    | 2    | I   | Negative input pin of the comparator 1         |
| IN1+                | 5    | 4    | I   | Positive input pin of the comparator 1         |
| IN2-                | 6    | 5    | I   | Negative input pin of the comparator 2         |
| IN2+                | 7    | 6    | I   | Positive input pin of the comparator 2         |
| IN3-                | 8    | 7    | I   | Negative input pin of the comparator 3         |
| IN3+                | 9    | 8    | I   | Positive input pin of the comparator 3         |
| IN4-                | 10   | 9    | I   | Negative input pin of the comparator 4         |
| IN4+                | 11   | 11   | I   | Positive input pin of the comparator 4         |
| V-                  | 12   | 12   | —   | Negative supply                                |
| OUT4                | 13   | 13   | O   | Output pin of the comparator 4                 |
| OUT3                | 14   | 14   | O   | Output pin of the comparator 3                 |
| NC                  | —    | 3    | —   | No Internal Connection - Leave floating or GND |
| NC                  | —    | 10   | —   | No Internal Connection - Leave floating or GND |
| Thermal Pad         | —    | PAD  | —   | Connect directly to V- pin.                    |

(1) Some manufacturers transpose the names of channels 1 and 2. Electrically the pinouts are identical, just a difference in channel naming convention.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|  | MIN  | MAX        | UNIT |
|--|------|------------|------|
| Supply voltage: $V_S = (V+) - (V-)$                        | -0.3 | 42         | V    |
| Input pins (IN+, IN-) from (V-) <sup>(2)</sup>             | -0.3 | (V+) + 0.3 | V    |
| Current into Input pins (IN+, IN-)                         | -10  | 10         | mA   |
| Output (OUT) voltage (Open-Drain) from (V-) <sup>(4)</sup> | -0.3 | 42         | V    |
| Output (OUT) voltage (Push-Pull) from (V-)                 | -0.3 | (V+) + 0.3 | V    |
| Output (OUT) current <sup>(4) (5) (6)</sup>                | -10  | 10         | mA   |
| Junction temperature, $T_J$                                |      | 150        | °C   |
| Storage temperature, $T_{stg}$                             | -65  | 150        | °C   |

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- Input terminals are diode-clamped to (V-). Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
- Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN-) as long as it is within the -0.3 V to 42 V range
- The output is diode-clamped to (V-) for both output options, and diode clamped to (V+) for the push-pull output option. The open drain version does not have a clamp to V+. Please see the *Outputs* and *ESD Protection* section of the *Application Information* Section for more information.
- Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absolute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply voltage below (V-) for both output options, or above (V+) for the push-pull option.
- Short-circuit from output to (V-) or (V+). Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

### 6.2 ESD Ratings

|             |                         | VALUE  | UNIT  |
|-------------|-------------------------|--|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup> | ±500  |

- JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                     |            | MIN  | MAX        | UNIT |
|-------------------------------------|------------|------|------------|------|
| Supply voltage: $V_S = (V+) - (V-)$ |            | 2.4  | 40         | V    |
| Input voltage range from (V-)       |            | -0.2 | (V+) + 0.2 | V    |
| Output voltage range from (V-)      | Open Drain | -0.2 | 40         | V    |
|                                     | Push Pull  | -0.2 | (V+) + 0.2 | V    |
| Ambient temperature, $T_A$          |            | -40  | 125        | °C   |

## 6.4 Thermal Information - Single

| THERMAL METRIC <sup>(1)</sup> |  | TLV18x1 and TLV18x1L |                |                 | UNIT |
|-------------------------------|--|----------------------|----------------|-----------------|------|
|                               |  | DCK<br>(SC-70)       | DCK<br>(SC-70) | DBV<br>(SOT-23) |      |
|                               |  | 5 PINS               | 6 PINS         | 5 PINS          |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 226.6                | 185.6          | 203.4           | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 129.5                | 137.6          | 105.4           | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 78.6                 | 76.5           | 106.6           | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 51.5                 | 59.8           | 54.0            | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 78.3                 | 76.2           | 106             | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –                    | –              | –               | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

## 6.5 Thermal Information - Dual

| THERMAL METRIC <sup>(1)</sup> |  | TLV18x2     |               |                 |               |                | UNIT |
|-------------------------------|--|-------------|---------------|-----------------|---------------|----------------|------|
|                               |  | D<br>(SOIC) | PW<br>(TSSOP) | DDF<br>(SOT-23) | DSG<br>(WSON) | DGK<br>(VSSOP) |      |
|                               |  | 8 PINS      | 8 PINS        | 8 PINS          | 8 PINS        | 8 PINS         |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 136.1       | 187.5         | 170.4           | 79.9          | 178.3          | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 76.8        | 76.7          | 90.3            | 100.1         | 66.4           | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 79.7        | 118.1         | 88.1            | 46.4          | 100.0          | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 26.8        | 14.4          | 7.5             | 5.3           | 9.2            | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 78.9        | 116.4         | 87.6            | 46.4          | 98.3           | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –           | –             | –               | 21.6          | –              | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.

## 6.6 Thermal Information - Quad

| THERMAL METRIC <sup>(1)</sup> |  | TLV18x4     |               |                 |               | UNIT |
|-------------------------------|--|-------------|---------------|-----------------|---------------|------|
|                               |  | D<br>(SOIC) | PW<br>(TSSOP) | DYY<br>(SOT-23) | RTE<br>(WQFN) |      |
|                               |  | 14 PINS     | 14 PINS       | 14 PINS         | 16 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 104.2       | 124.1         | 119.9           | 53.8          | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 60.3        | 52.4          | 60.6            | 58.6          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 60.2        | 67.2          | 79.0            | 29.0          | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 20.7        | 7.5           | 3.3             | 2.2           | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 59.8        | 66.6          | 41.2            | 28.9          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –           | –             | –               | 13.1          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) report.



## 6.7 Electrical Characteristics

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 12\text{ V}$ ,  $V_{CM} = V_S / 2$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

| PARAMETER                      |  | TEST CONDITIONS   | MIN          | TYP  | MAX          | UNIT                         |
|--------------------------------|--|---|--------------|------|--------------|------------------------------|
| <b>OFFSET VOLTAGE</b>          |  |   |              |      |              |                              |
| $V_{OS}$                       | Input offset voltage                           |   | -3           | ±0.5 | 3            | mV                           |
|                                |  | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   | -4           |      | 4            | mV                           |
| $dV_{IO}/dT$                   | Input offset voltage drift                     | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   |              | ±1.2 |              | $\mu\text{V}/^\circ\text{C}$ |
| PSRR                           | Power supply rejection ratio                   | $V_S = 2.4\text{ V}$ to $40\text{ V}$ , $V_{CM} = (V-)$   |              | 100  |              | dB                           |
| <b>POWER SUPPLY</b>            |  |   |              |      |              |                              |
| $I_Q$                          | Quiescent current, No Load                     | Output Low, $T_A = 25^\circ\text{C}$<br>TLV1811 Only  |              | 6    | 7.5          | $\mu\text{A}$                |
|                                |  | Output Low, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$<br>TLV1811 Only                             |              |      | 8.5          |                              |
|                                |  | Output High, $T_A = 25^\circ\text{C}$<br>TLV1811 Only   |              | 8    | 10           |                              |
|                                |  | Output High, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$<br>TLV1811 Only                            |              |      | 11           |                              |
| $I_Q$                          | Quiescent current per comparator, No Load      | Output Low, $T_A = 25^\circ\text{C}$  |              | 5    | 6.5          | $\mu\text{A}$                |
|                                |  | Output Low, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   |              |      | 7.5          |                              |
|                                |  | Output High, $T_A = 25^\circ\text{C}$   |              | 7    | 9            |                              |
|                                |  | Output High, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$  |              |      | 10           |                              |
| $V_{POR}$                      | Power On Reset Voltage                         |   |              | 1.7  |              | V                            |
| <b>INPUT BIAS CURRENT</b>      |  |   |              |      |              |                              |
| $I_B$                          | Input bias current <sup>(1)</sup>              |   |              | 150  |              | fA                           |
|                                |  | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$   | -1.2         |      | 1.2          | nA                           |
| $I_{OS}$                       | Input offset current <sup>(1)</sup>            |   |              | 10   |              | fA                           |
| <b>INPUT CAPACITANCE</b>       |  |   |              |      |              |                              |
| $C_{ID}$                       | Input Capacitance, Differential                |   |              | 2    |              | pF                           |
| $C_{IC}$                       | Input Capacitance, Common Mode                 |   |              | 8    |              | pF                           |
| <b>INPUT COMMON MODE RANGE</b> |  |   |              |      |              |                              |
| $V_{CM\text{-Range}}$          | Common-mode voltage range                      | $V_S = 2.4\text{ V}$ to $40\text{ V}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , Rail to Rail | $(V-) - 0.2$ |      | $(V+) + 0.2$ | V                            |
| <b>OUTPUT</b>                  |  |   |              |      |              |                              |
| $V_{OL}$                       | Voltage swing from $(V-)$                      | $I_{SINK} = 4\text{ mA}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                             |              |      | 250          | mV                           |
| $V_{OH}$                       | Voltage swing from $(V+)$ (for Push-Pull only) | $I_{SOURCE} = 4\text{ mA}$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$                           |              |      | 250          | mV                           |
| $I_{LKG}$                      | Open-drain output leakage current              | $V_{ID} = +0.1\text{ V}$ , $V_{PULLUP} = (V+)$<br>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$       |              | 0.1  |              | nA                           |
| $I_{OL}$                       | Short-circuit current                          | Sinking   | 15           | 30   |              | mA                           |
| $I_{OH}$                       | Short-circuit current                          | Sourcing (for Push-Pull only)   | 15           | 30   |              | mA                           |

(1) This parameter is ensured by design and/or characterization and is not tested in production .

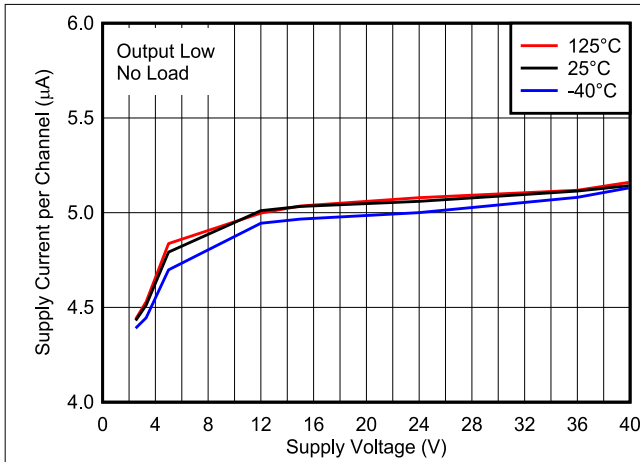
## 6.8 Switching Characteristics

For  $V_S$  (Total Supply Voltage) =  $(V+) - (V-) = 12\text{ V}$ ,  $V_{CM} = V_S / 2$  at  $T_A = 25^\circ\text{C}$  (Unless otherwise noted)

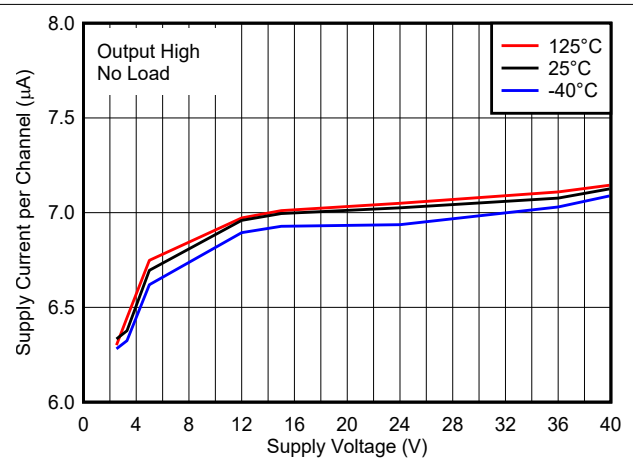
| PARAMETER            |   | TEST CONDITIONS                                 | MIN | TYP | MAX | UNIT          |
|----------------------|---|---|-----|-----|-----|---------------|
| <b>OUTPUT</b>        |   |   |     |     |     |               |
| $T_{PD-HL}$          | Propagation delay time, high-to-low                   | $V_{OD} = 10\text{ mV}$ , $C_L = 50\text{ pF}$  |     | 900 |     | ns            |
| $T_{PD-HL}$          | Propagation delay time, high-to-low                   | $V_{OD} = 100\text{ mV}$ , $C_L = 50\text{ pF}$ |     | 450 |     | ns            |
| $T_{PD-LH}$          | Propagation delay time, low-to-high, push-pull output | $V_{OD} = 10\text{ mV}$ , $C_L = 50\text{ pF}$  |     | 900 |     | ns            |
| $T_{PD-LH}$          | Propagation delay time, low-to-high, push-pull output | $V_{OD} = 100\text{ mV}$ , $C_L = 50\text{ pF}$ |     | 420 |     | ns            |
| $T_{RISE}$           | Output Rise Time, 20% to 80%, push-pull output        | $C_L = 50\text{ pF}$                            |     | 15  |     | ns            |
| $T_{FALL}$           | Output Fall Time, 80% to 20%                          | $C_L = 50\text{ pF}$                            |     | 15  |     | ns            |
| $F_{TOGGLE}$         | Toggle Frequency                                      | $V_{ID} = 100\text{ mV}$ , $C_L = 50\text{ pF}$ |     | 500 |     | kHz           |
| <b>POWER ON TIME</b> |   |   |     |     |     |               |
| $P_{ON}$             | Power on-time   |   |     | 200 |     | $\mu\text{s}$ |

## 7 Typical Characteristics

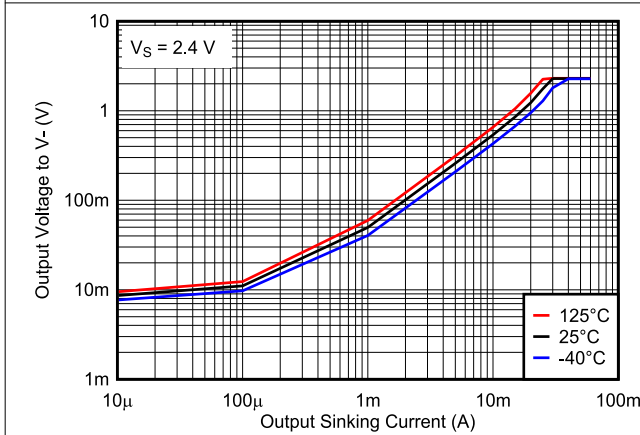
$T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}$ ,  $C_L = 20\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.



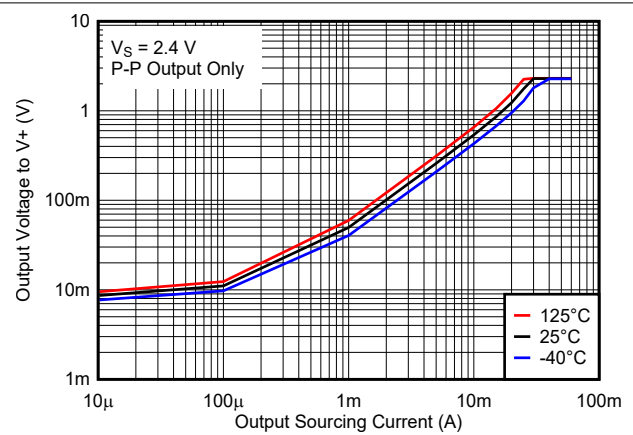
**7-1. Supply Current per Channel vs. Supply Voltage, Output Low**



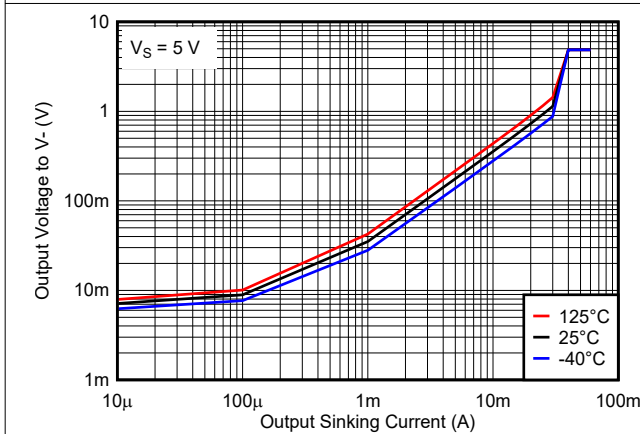
**7-2. Supply Current per Channel vs. Supply Voltage, Output High**



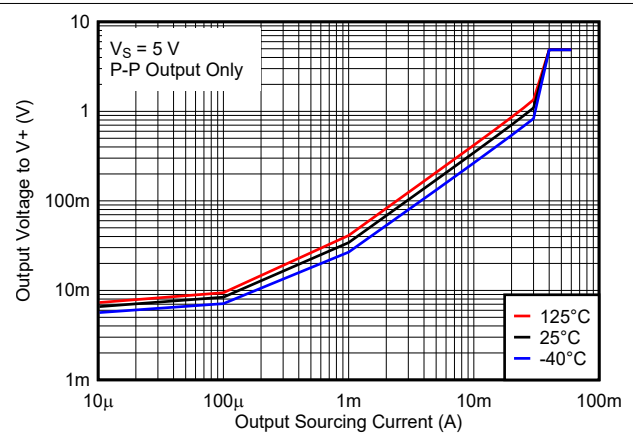
**7-3. Output Voltage vs. Output Sinking Current, 2.4 V**



**7-4. Output Voltage vs. Output Sourcing Current, 2.4 V**



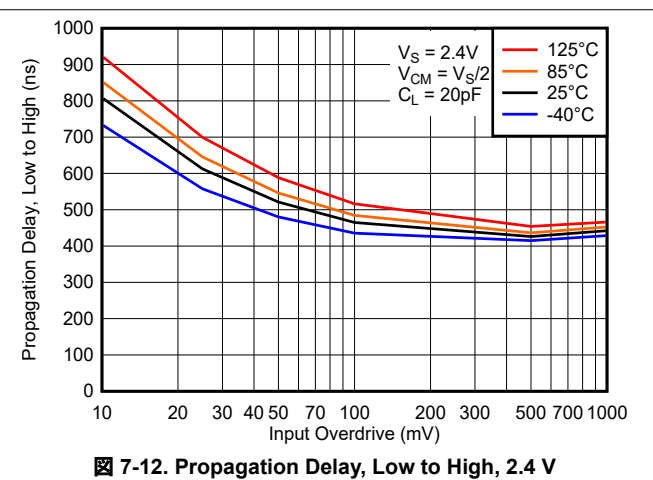
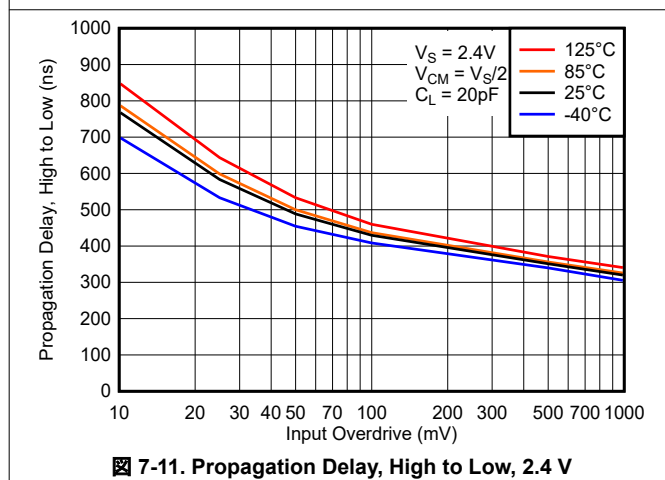
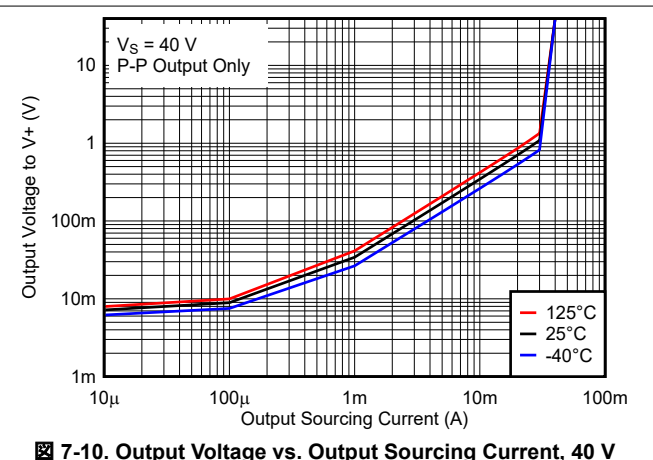
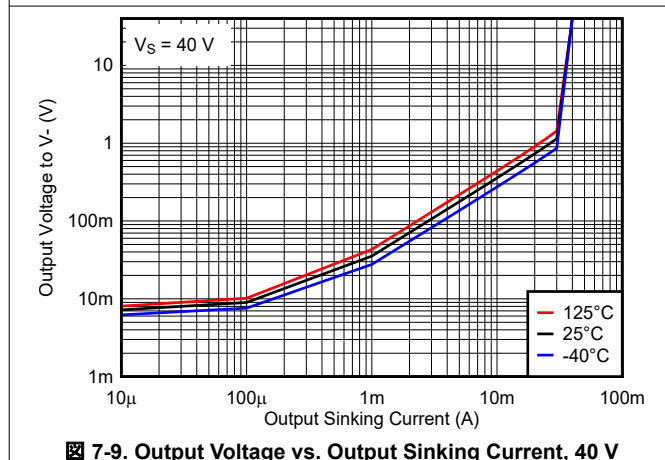
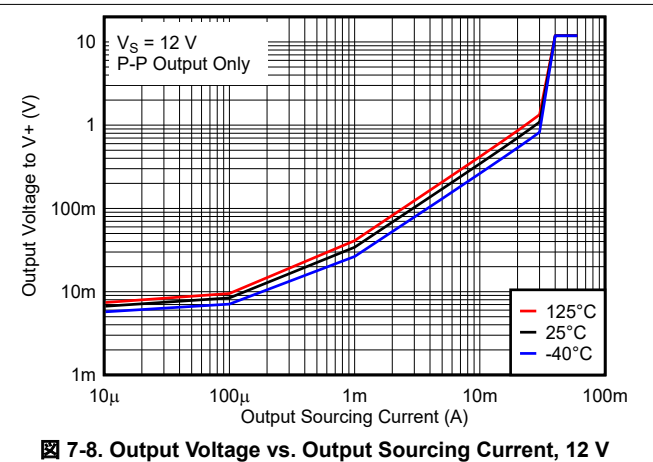
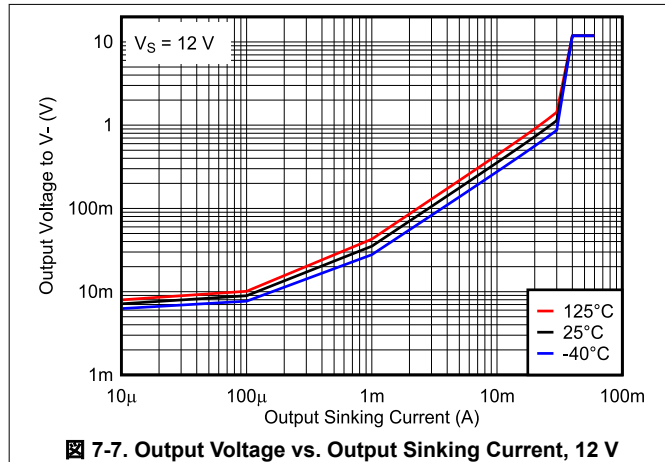
**7-5. Output Voltage vs. Output Sinking Current, 5 V**



**7-6. Output Voltage vs. Output Sourcing Current, 5 V**

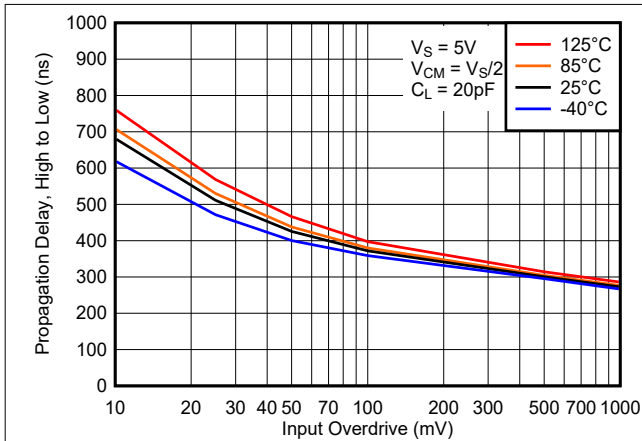
## 7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}$ ,  $C_L = 20\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.

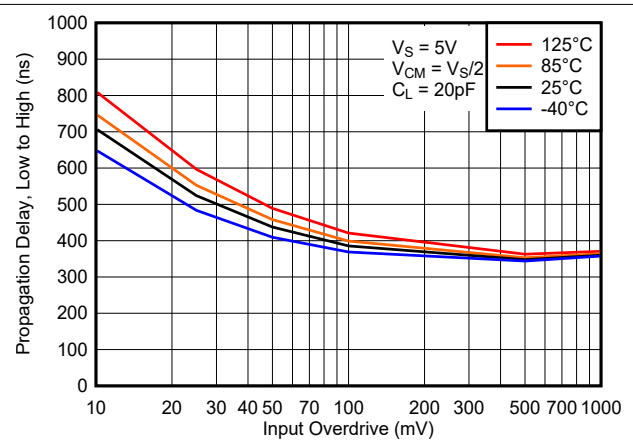


## 7 Typical Characteristics (continued)

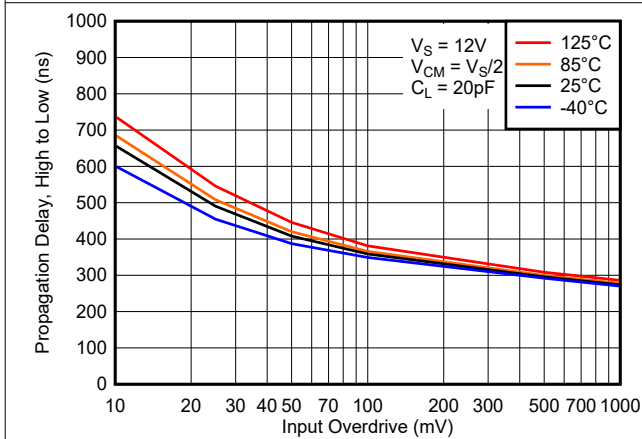
$T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{ V}$ ,  $R_{\text{PULLUP}} = 2.5\text{ k}$ ,  $C_L = 20\text{ pF}$ ,  $V_{\text{CM}} = 0\text{ V}$ ,  $V_{\text{UNDERDRIVE}} = 100\text{ mV}$ ,  $V_{\text{OVERDRIVE}} = 100\text{ mV}$  unless otherwise noted.



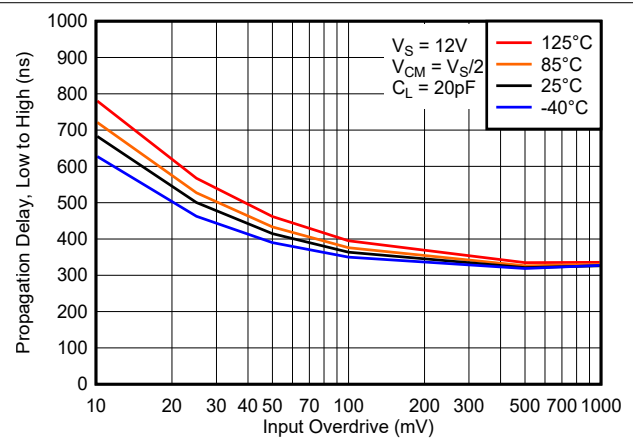
7-13. Propagation Delay, High to Low, 5 V



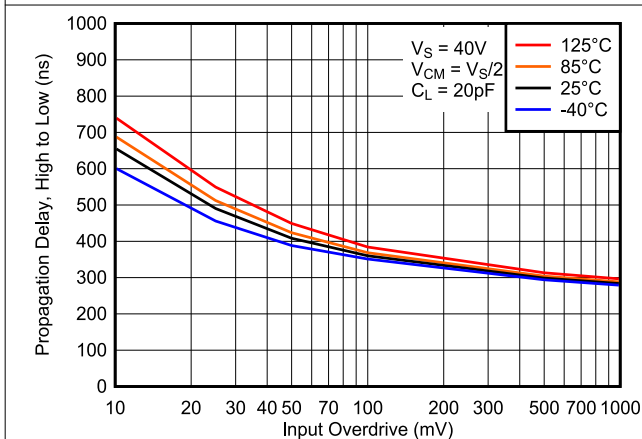
7-14. Propagation Delay, Low to High, 5 V



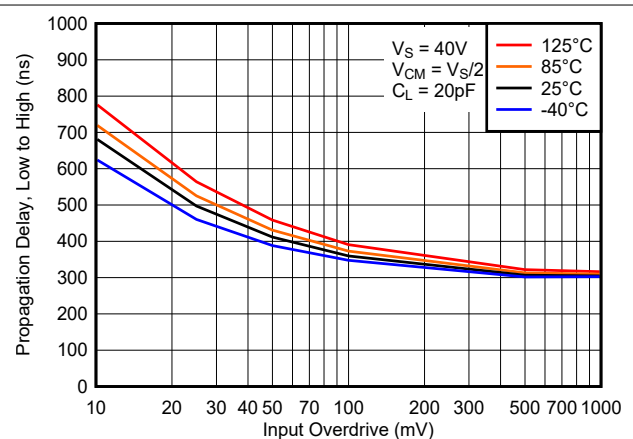
7-15. Propagation Delay, High to Low, 12 V



7-16. Propagation Delay, Low to High, 12 V



7-17. Propagation Delay, High to Low, 40 V



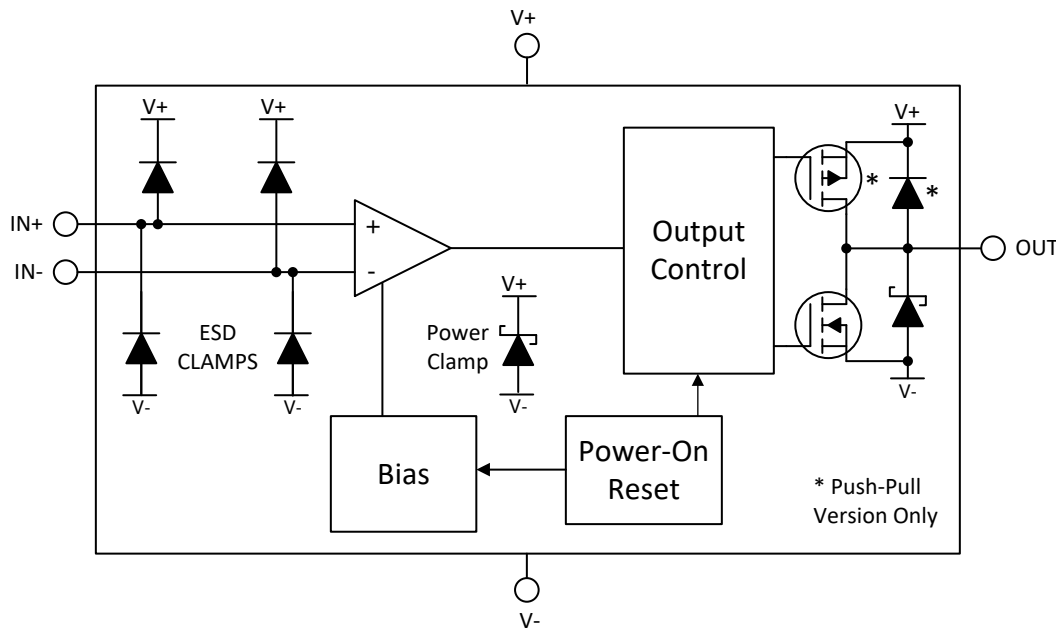
7-18. Propagation Delay, Low to High, 40 V

## 8 Detailed Description

### 8.1 Overview

The TLV181x and TLV182x devices are micro-power comparators with push-pull and open-drain output options. Operating down to 2.4 V while only consuming only 5  $\mu\text{A}$  per channel, the TLV181x and TLV182x are well suited for portable, automotive and industrial applications. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down.

### 8.2 Functional Block Diagrams



8-1. TLV18xx Block Diagram

### 8.3 Feature Description

#### TLV18xx Family Options

The TLV18xy family consists of several output and pinout options, all featuring 40 V operation, micro-power 5  $\mu\text{A}$  supply currents, 420 ns propagation delay, and a Power-On Reset (POR) function.

The TLV18xx family has two output options:

The TLV181x has a **push-pull** (sink-source) output.

The TLV182x has a **open-drain** (sink only) output, capable of being pulled-up to any voltage up to 40 V, independent of comparator supply voltage.

The TLV1811L and TLV1821L are alternate pinouts of the TLV1811 and TLV1821 that allow upgrading older devices such as the TLV7211, TLV7221, LMC7211 and LMC7221 family.

### 8.4 Device Functional Modes

#### 8.4.1 Inputs

##### 8.4.1.1 TLV18xx Rail-to-Rail Input

The TLV18xx input voltage range extends from 200 mV below  $V_-$  to 200 mV above  $V_+$ . The differential input voltage ( $V_{ID}$ ) may be any voltage within these limits. No phase-inversion of the comparator output will occur when the input voltages stay within the specified range.

The Rail-to-Rail input does have an ESD clamp to the V+ supply line and therefore the input voltage must not exceed the supply voltages by more than 200mV. It is not recommended to apply signals to the rail to rail inputs with no supply voltage.

#### **8.4.1.2 ESD Protection**

The TLV181x open-drain output ESD protection consists of a snapback ESD clamp between the output and V- to allow the output to be pulled above V+ to a maximum of 40 V. There is no "upper" ESD clamp diode between the output and V+ on the open-drain output. There is a "lower" clamp between V- and the output.

The TLV182x push-pull output ESD protection contains a conventional diode-type "upper" ESD clamp between the output and V+, and a "lower" ESD clamp between the output and V-. The output must not exceed the supply rails by more than 200mV.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10 mA or less, though TI recommends limiting the current to 1mA or less. This series resistance may be part of any resistive input dividers or networks.

#### **8.4.1.3 Unused Inputs**

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together may cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50 mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ (as long as the input is directly connected to the V+ pin to avoid transients).

### **8.4.2 Outputs**

#### **8.4.2.1 TLV181x Push-Pull Output**

The TLV181x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail (V+ when output "low" or V- when output "High") can result in thermal runaway and eventual device destruction at high (>12 V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

#### **8.4.2.2 TLV182x Open-Drain Output**

The TLV182x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0 V up to 40 V, independent of the comparator supply voltage (V+). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values will help increase the rising edge rise-time, but at the expense of increasing  $V_{OL}$  and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 M $\Omega$ ) will create an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to V+ can result in thermal runaway and eventual device destruction at high (>12 V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs may be left floating, or may be tied to the V- pin if floating pins are not desired.

#### **8.4.3 Power-On Reset (POR)**

The TLV18xx family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for up to 200  $\mu$ s

after the minimum supply voltage threshold of 2.4 V is crossed, or immediately when the supply voltage drops below 2.4 V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input ( $V_{ID}$ ).

For the TLV181x push-pull output devices, the output is held low during the POR period ( $t_{on}$ ).

For the TLV182x open drain output option the POR circuit will keep the output high impedance (Hi-Z) during the POR period ( $t_{on}$ ).

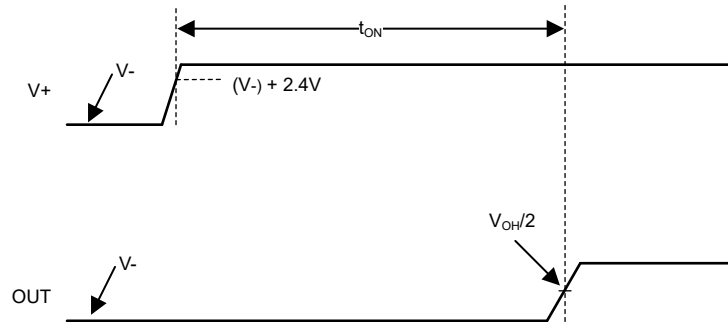


图 8-2. Power-On Reset Timing Diagram

Note: The output voltage rises with the pull-up voltage during the POR period.

#### 8.4.4 Hysteresis

The TLV18xx family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, it is possible for the output to "chatter" when the absolute differential voltage is near zero as the comparator triggers on its own internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See [セクション 9.1.2](#) in the following section.



## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Basic Comparator Definitions

##### 9.1.1.1 Operation

The basic comparator compares the input voltage ( $V_{IN}$ ) on one input to a reference voltage ( $V_{REF}$ ) on the other input. In the [Figure 9-1](#) example below, if  $V_{IN}$  is less than  $V_{REF}$ , the output voltage ( $V_O$ ) is logic low ( $V_{OL}$ ). If  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is at logic high ( $V_{OH}$ ). [Table 9-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

表 9-1. Output Conditions

| Inputs Condition | Output   |
|------------------|--|
| $IN+ > IN-$      | HIGH ( $V_{OH}$ )  |
| $IN+ = IN-$      | Indeterminate (chatters - see <a href="#">Hysteresis</a> ) |
| $IN+ < IN-$      | LOW ( $V_{OL}$ )   |

##### 9.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to-low and low-to-high input transitions. This is shown as  $t_{pLH}$  and  $t_{pHL}$  in [Figure 9-1](#) and is measured from the mid-point of the input to the midpoint of the output.

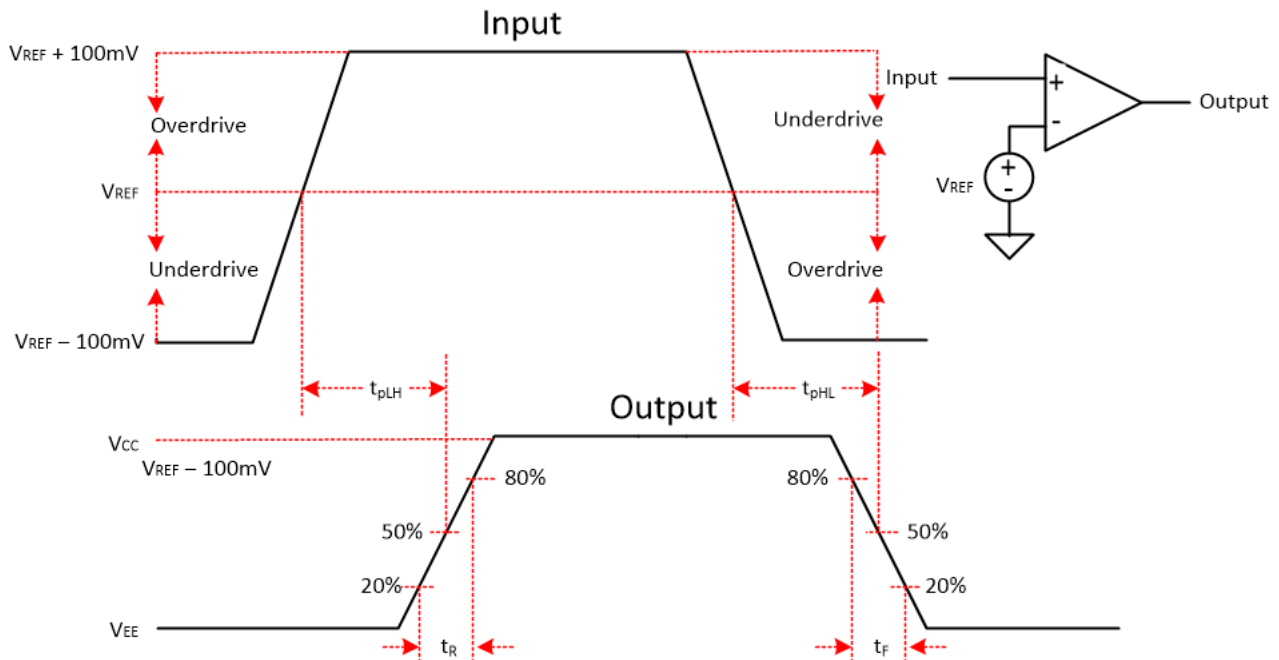


Figure 9-1. Comparator Timing Diagram

### 9.1.1.3 Overdrive Voltage

The overdrive voltage,  $V_{OD}$ , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100 mV as shown in the [Figure 9-1](#) example. The overdrive voltage can influence the propagation delay ( $t_p$ ). The smaller the overdrive voltage, the longer the propagation delay, particularly when  $<100\text{mV}$ . If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime ( $t_r$ ) and falltime ( $t_f$ ) is the time from the 20% and 80% points of the output waveform.

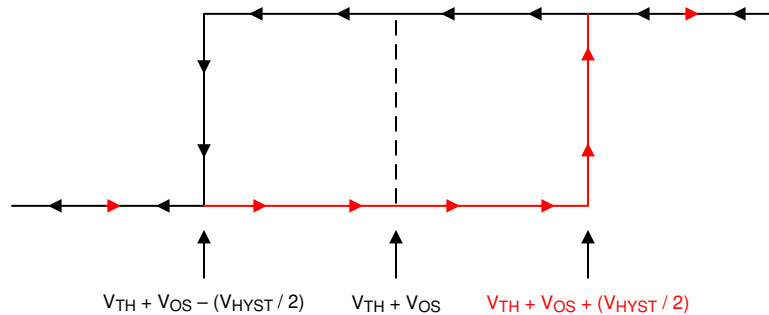
### 9.1.2 Hysteresis

The basic comparator configuration may oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in [Figure 9-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

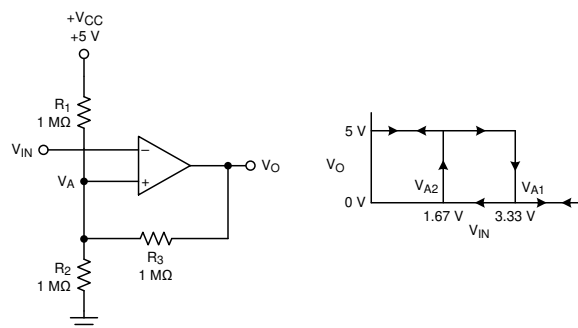


**Figure 9-2. Hysteresis Transfer Curve**

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

#### 9.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage ( $V_{CC}$ ), as shown in [Figure 9-3](#).



**Figure 9-3. TLV181xin an Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 9-3](#).

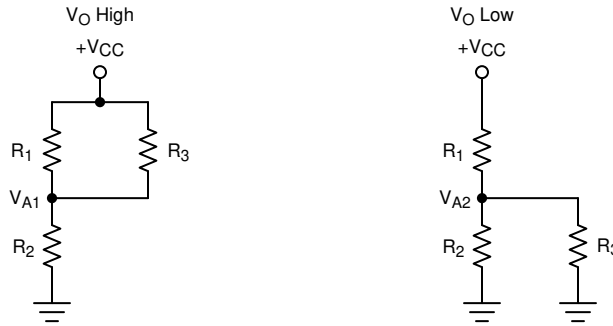


图 9-4. Inverting Configuration Resistor Equivalent Networks

When  $V_{IN}$  is less than  $V_A$ , the output voltage is high (for simplicity, assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R1 \parallel R3$  in series with  $R2$ , as shown in 图 9-4.

式 1 below defines the high-to-low trip voltage ( $V_{A1}$ ).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When  $V_{IN}$  is greater than  $V_A$ , the output voltage is low. In this case, the three network resistors can be presented as  $R2 \parallel R3$  in series with  $R1$ , as shown in 式 2.

Use 式 2 to define the low to high trip voltage ( $V_{A2}$ ).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

### 9.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference ( $V_{REF}$ ) at the inverting input, as shown in 图 9-5,

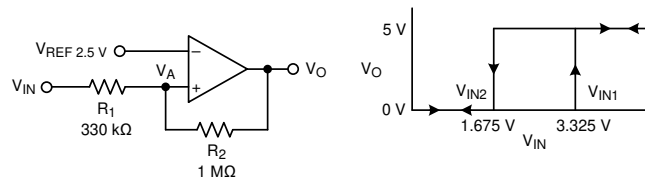


图 9-5. TLV181x in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in 图 9-6.

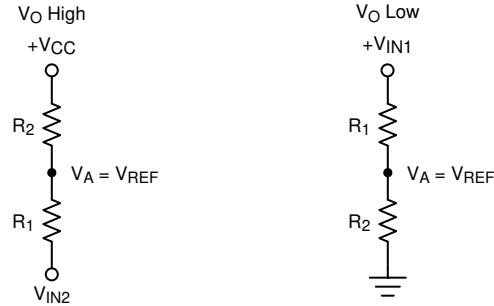


图 9-6. Non-Inverting Configuration Resistor Networks

When  $V_{IN}$  is less than  $V_{REF}$ , the output is low. For the output to switch from low to high,  $V_{IN}$  must rise above the  $V_{IN1}$  threshold. Use 式 4 to calculate  $V_{IN1}$ .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When  $V_{IN}$  is greater than  $V_{REF}$ , the output is high. For the comparator to switch back to a low state,  $V_{IN}$  must drop below  $V_{IN2}$ . Use 式 5 to calculate  $V_{IN2}$ .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

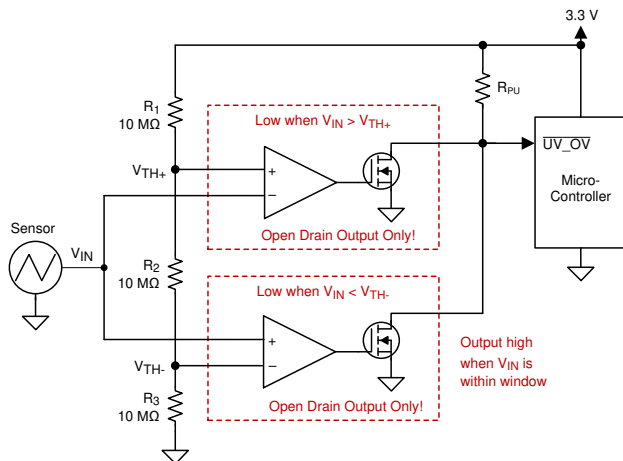
### 9.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV182x, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as  $R2 + R_{PULLUP}$ . TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

## 9.2 Typical Applications

### 9.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 图 9-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV182x) if the outputs are directly connected together.



9-7. Window Comparator

### 9.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

### 9.2.1.2 Detailed Design Procedure

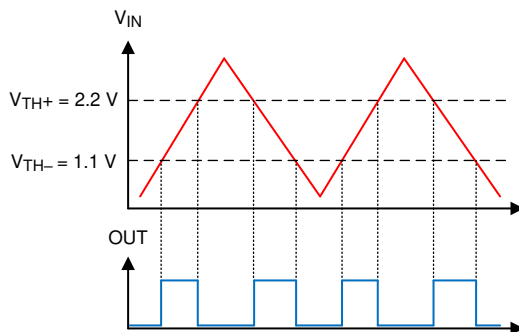
Configure the circuit as shown in 9-7. Connect  $V_{CC}$  to a 3.3-V power supply and  $V_{EE}$  to ground. Make R1, R2 and R3 each 10-M $\Omega$  resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ( $V_{TH+}$  and  $V_{TH-}$ ).

With each resistor being equal,  $V_{TH+}$  is 2.2 V and  $V_{TH-}$  is 1.1 V. Large resistor values such as 10-M $\Omega$  are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. The respective comparator outputs will be high when the sensor is in the range of 1.1 V to 2.2 V (within the "window"), as shown in 9-8.

### 9.2.1.3 Application Curve

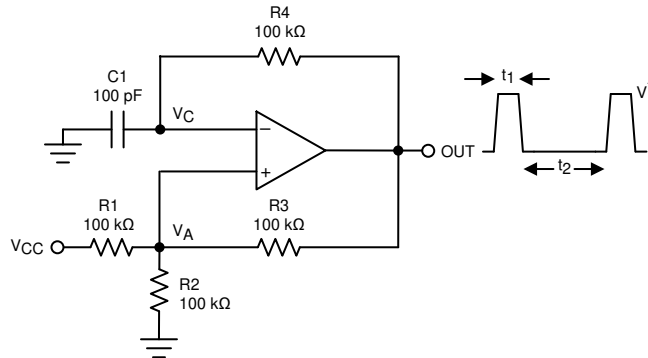


9-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

## 9.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV181x) is recommended for best symmetry.



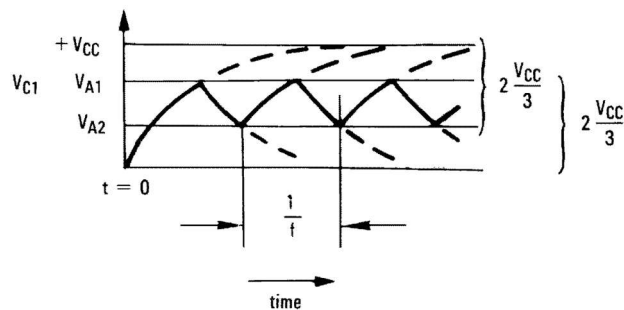
**9-9. Square-Wave Oscillator**

### 9.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor  $C_1$  and resistor  $R_4$ . The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space. TI recommends that  $R_4$  be over several kilohms to minimize loading of the output.

### 9.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.



**9-10. Square-Wave Oscillator Timing Thresholds**

First consider the output of Figure 9-9 as high, which indicates the inverted input  $V_C$  is lower than the noninverting input ( $V_A$ ). This causes the  $C_1$  to be charged through  $R_4$ , and the voltage  $V_C$  increases until it is equal to the noninverting input. The value of  $V_A$  at the point is calculated by 式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 + R_3} \quad (7)$$

if  $R_1 = R_2 = R_3$ , then  $V_{A1} = 2 V_{CC} / 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of  $V_A$  at this point is calculated by 式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3} \quad (8)$$

if  $R_1 = R_2 = R_3$ , then  $V_{A2} = V_{CC}/3$

The  $C_1$  now discharges through the  $R_4$ , and the voltage  $V_{CC}$  decreases until it reaches  $V_{A2}$ . At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for  $C_1$  from  $2V_{CC}/3$  to  $V_{CC}/3$  then back to  $2V_{CC}/3$ , which is given by  $R_4 C_1 \times \ln 2$  for each trip. Therefore, the total time duration is calculated as  $2 R_4 C_1 \times \ln 2$ .

The oscillation frequency can be obtained by 式 9:

$$f = 1 / (2 R_4 \times C_1 \times \ln 2) \quad (9)$$

### 9.2.2.3 Application Curve

Figure 9-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
- $C_1 = 100 \text{ pF}$ ,  $C_L = 20 \text{ pF}$
- $V_+ = 5 \text{ V}$ ,  $V_- = \text{GND}$
- $C_{\text{stray}}$  (not shown) from  $V_A$  TO GND =  $10 \text{ pF}$

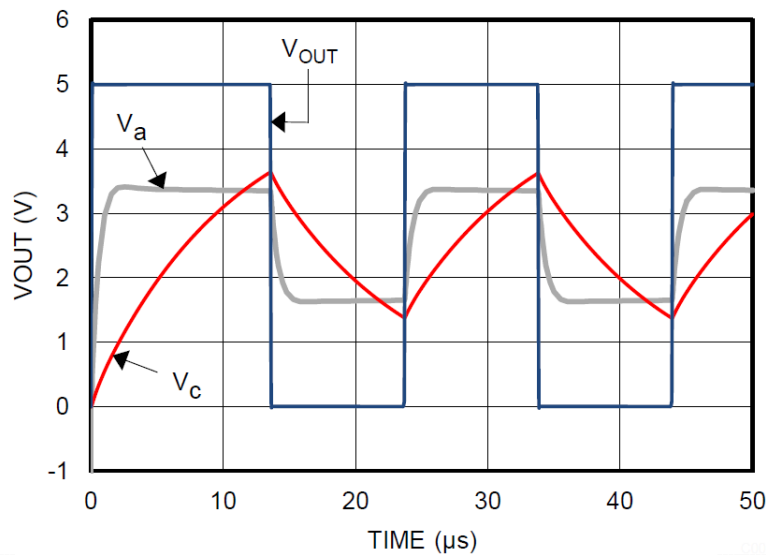
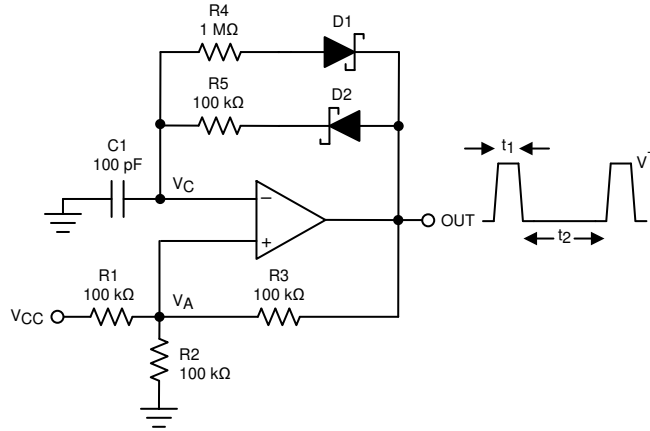


Figure 9-11. Square-Wave Oscillator Output Waveform

### 9.2.3 Adjustable Pulse Width Generator

Figure 9-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

$R_4$  and  $R_5$  provide separate charge and discharge paths for the capacitor  $C$  depending on the output state.



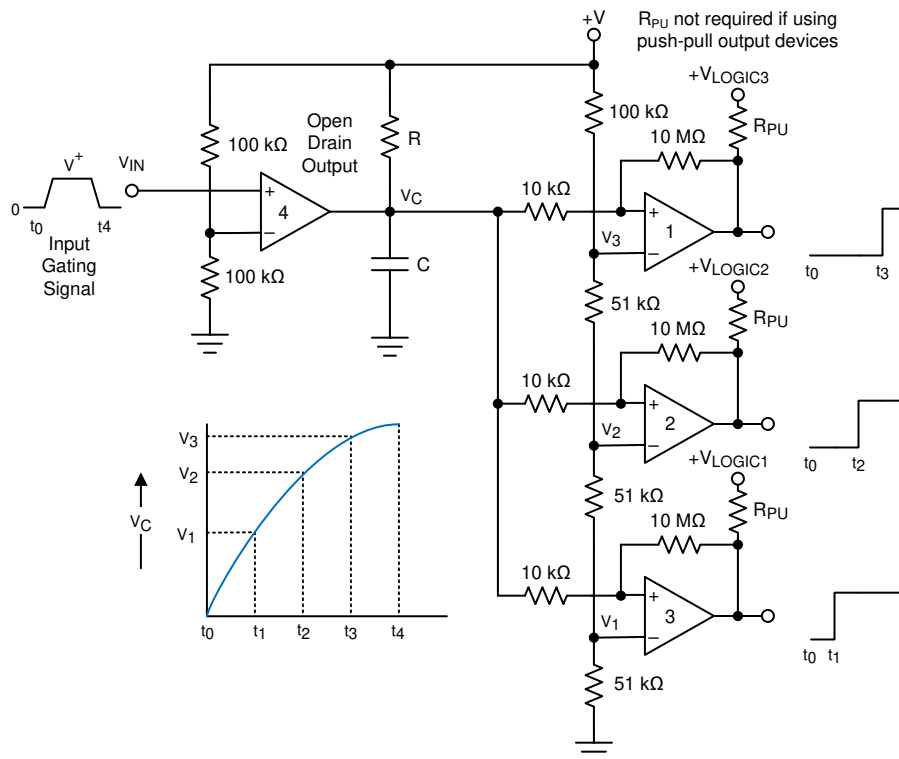
**9-12. Adjustable Pulse Width Generator**

The charge path is set through  $R_5$  and  $D_2$  when the output is high. Similarly, the discharge path for the capacitor is set by  $R_4$  and  $D_1$  when the output is low.

The pulse width  $t_1$  is determined by the RC time constant of  $R_5$  and  $C$ . Thus, the time  $t_2$  between the pulses can be changed by varying  $R_4$ , and the pulse width can be altered by  $R_5$ . The frequency of the output can be changed by varying both  $R_4$  and  $R_5$ . At low voltages, the effects of the diode forward drop (0.8 V, or 0.15 V for Schottky) must be taken into account by altering output high and low voltages in the calculations.

### 9.2.4 Time Delay Generator

The circuit shown in **9-13** provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0 V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.



**9-13. Time Delay Generator**



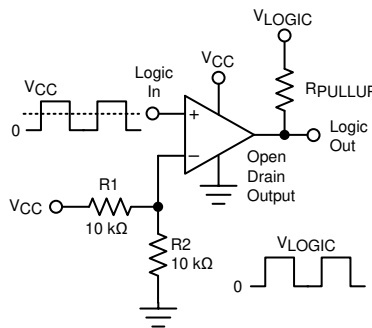
Consider the case of  $V_{IN} = 0$ . The output of comparator 4 is also at ground, "shorting" the capacitor and holding it at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when  $V_C$  rises above the reference voltages  $V_1$ ,  $V_2$  and  $V_3$ . A small amount of hysteresis has been provided by the 10 k $\Omega$  and 10 M $\Omega$  resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is  $R = 100$  k $\Omega$  and  $C = 0.01$   $\mu$ F to 1  $\mu$ F.

All outputs will immediately go low when  $V_{IN}$  falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV182x), whereas comparators 1 though 3 may be either open drain or push-pull output, depending on system requirements.  $R_{PU}$  is not required for push-pull output devices.

### 9.2.5 Logic Level Shifter

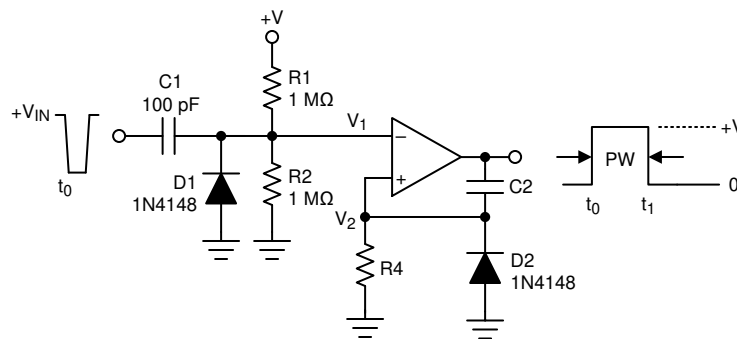
The output of the TLV182x is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.



**FIG 9-14. Universal Logic Level Shifter**

The two 10 k $\Omega$  resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and may be connected to any pull-up voltage between 0 V and 5.5 V. The pullup voltage should match the driven logic input "high" level.

### 9.2.6 One-Shot Multivibrator

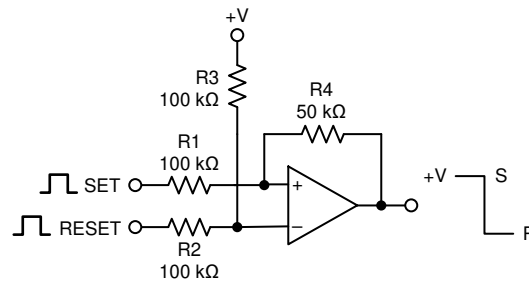


**FIG 9-15. One-Shot Multivibrator**

A monostable multivibrator has one stable state in which it can remain indefinitely. It can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of  $C_2$  and  $R_4$ . The resistor divider of  $R_1$  and  $R_2$  can be used to determine the magnitude of the input trigger pulse. The output will change state when  $V_1 < V_2$ . Diode  $D_2$  provides a rapid discharge path for capacitor  $C_2$  to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

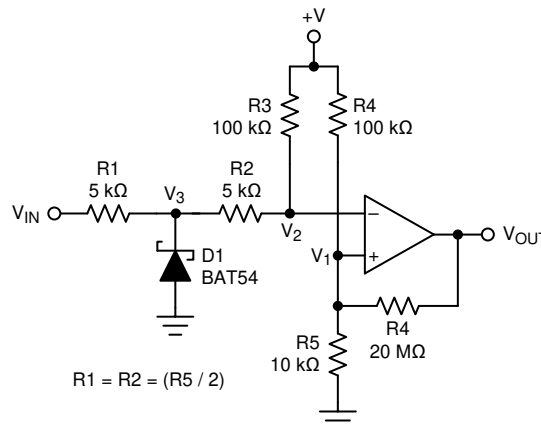
### 9.2.7 Bi-Stable Multivibrator



**9-16. Bi-Stable Multivibrator**

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of  $R_2$  and  $R_3$ . A pulse applied to the SET terminal will switch the output of the comparator high. The resistor divider of  $R_1$  and  $R_4$  now sets the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET will now toggle the output low.

### 9.2.8 Zero Crossing Detector



**9-17. Zero Crossing Detector**

A voltage divider of  $R_4$  and  $R_5$  establishes a reference voltage  $V_1$  at the non-inverting input. By making the series resistance of  $R_1$  and  $R_2$  equal to  $R_5$ , the comparator will switch when  $V_{IN} = 0$ . Diode  $D_1$  insures that  $V_3$  clamps near ground. The voltage divider of  $R_2$  and  $R_3$  then prevents  $V_2$  from going below ground. A small amount of hysteresis is setup to ensure rapid output voltage transitions.

### 9.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of  $R_1$  and  $C_1$  establishes an mean reference voltage  $V_{REF}$ , which tracks the mean amplitude of the  $V_{IN}$  signal. The non-inverting input is directly connected to  $V_{REF}$  through  $R_2$ .  $R_2$  and  $R_3$  are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, it is recommended that the data be encoded in NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs may suffer from timing distortions caused by the changing  $V_{REF}$  average voltage.

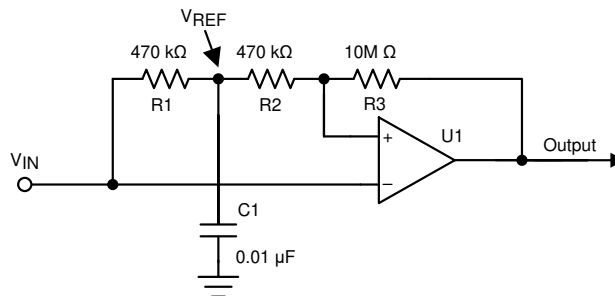


Figure 9-18. Pulse Slicer

For this design, follow these design requirements:

- The RC constant value ( $R_2$  and  $C_1$ ) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with  $R_2$  and  $R_{43}$  helps to avoid spurious output toggles.

The TLV182x may also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 9-19 shows the results of a 9600 baud data signal riding on a varying baseline.

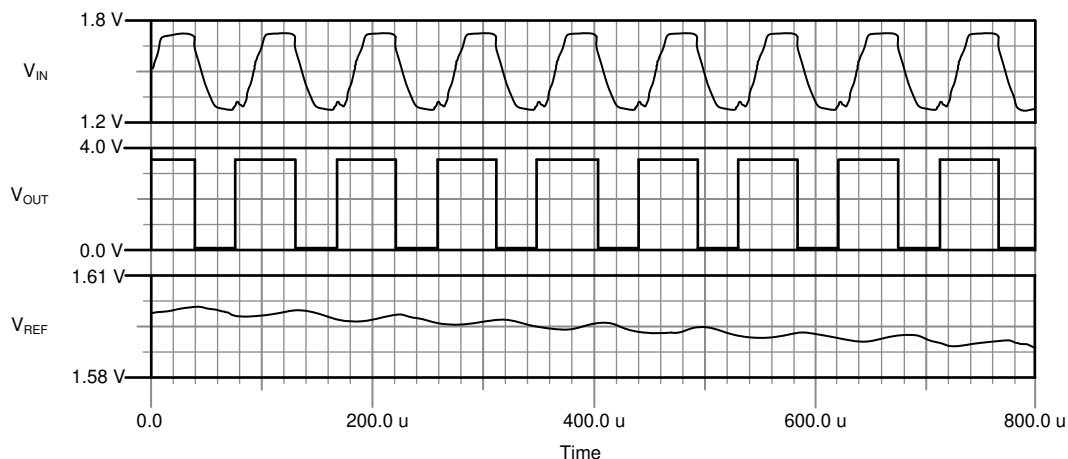


Figure 9-19. Pulse Slicer Waveforms

## 9.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1  $\mu\text{F}$  ceramic bypass capacitor directly between  $V_{CC}$  pin and ground pins. Narrow, peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from both "split" supplies ( $V+$  and  $V-$ ), or "single" supplies ( $V+$  and GND), with GND applied to the  $V-$  pin. Input signals must stay within the specified input range (between  $V+$  and  $V-$ ) for either type. Note that with a "split" supply the output will now swing "low" ( $V_{OL}$ ) to  $V-$  potential and not GND.

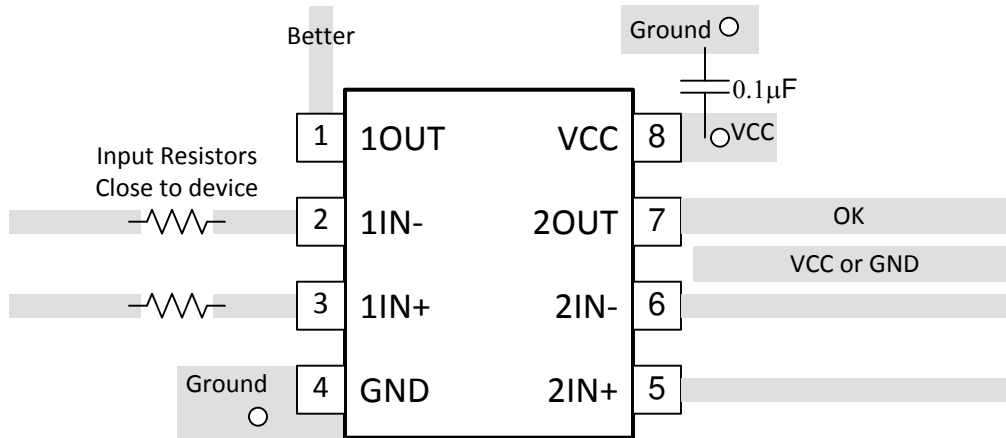
## 9.4 Layout

### 9.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the  $V_{CC}$  and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V<sub>CC</sub> or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

### 9.4.2 Layout Example



 9-20. Dual Layout Example

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

[Analog Engineers Circuit Cookbook: Amplifiers \(See Comparators section\) - SLYY137](#)

[Precision Design, Comparator with Hysteresis Reference Design— TIDU020](#)

[Window comparator circuit - SBOA221](#)

[Reference Design, Window Comparator Reference Design— TIPD178](#)

[Comparator with and without hysteresis circuit - SBOA219](#)

[Inverting comparator with hysteresis circuit - SNOA997](#)

[Non-Inverting Comparator With Hysteresis Circuit - SBOA313](#)

[Zero crossing detection using comparator circuit - SNOA999](#)

[PWM generator circuit - SBOA212](#)

[How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41](#)

[A Quad of Independently Func Comparators - SNOA654](#)

### 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 10.4 Trademarks

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### 10.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV1811DBVR      | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | 2XJT                    | <a href="#">Samples</a> |
| TLV1811DCKR      | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2XST                    | <a href="#">Samples</a> |
| TLV1811LDBVR     | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | 2XNT                    | <a href="#">Samples</a> |
| TLV1811LDCKR     | ACTIVE        | SC70         | DCK             | 6    | 3000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | 2XTT                    | <a href="#">Samples</a> |
| TLV1812DDFR      | ACTIVE        | SOT-23-THIN  | DDF             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 32EF                    | <a href="#">Samples</a> |
| TLV1812DGKR      | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 31US                    | <a href="#">Samples</a> |
| TLV1812DR        | ACTIVE        | SOIC         | D               | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TL1812                  | <a href="#">Samples</a> |
| TLV1812DSGR      | ACTIVE        | WSON         | DSG             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 1OD                     | <a href="#">Samples</a> |
| TLV1812PWR       | ACTIVE        | TSSOP        | PW              | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TL1812                  | <a href="#">Samples</a> |
| TLV1814DR        | ACTIVE        | SOIC         | D               | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TLV1814D                | <a href="#">Samples</a> |
| TLV1814DYR       | ACTIVE        | SOT-23-THIN  | DYY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TLV1814B1               | <a href="#">Samples</a> |
| TLV1814RTER      | ACTIVE        | WQFN         | RTE             | 16   | 5000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | T1814B                  | <a href="#">Samples</a> |
| TLV1821DBVR      | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | 2XLT                    | <a href="#">Samples</a> |
| TLV1821DCKR      | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   |              | 2XUT                    | <a href="#">Samples</a> |
| TLV1821LDBVR     | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | 2XMT                    | <a href="#">Samples</a> |
| TLV1822DDFR      | ACTIVE        | SOT-23-THIN  | DDF             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 32DF                    | <a href="#">Samples</a> |
| TLV1822DGKR      | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 31VS                    | <a href="#">Samples</a> |
| TLV1822DR        | ACTIVE        | SOIC         | D               | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TL1822                  | <a href="#">Samples</a> |
| TLV1822DSGR      | ACTIVE        | WSON         | DSG             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 1OE                     | <a href="#">Samples</a> |
| TLV1822PWR       | ACTIVE        | TSSOP        | PW              | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TL1822                  | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV1824DR        | ACTIVE        | SOIC         | D               | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TLV1824D                | <a href="#">Samples</a> |
| TLV1824DYR       | ACTIVE        | SOT-23-THIN  | DYY             | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TLV1824DYR              | <a href="#">Samples</a> |
| TLV1824PWR       | ACTIVE        | TSSOP        | PW              | 14   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | T1824B1                 | <a href="#">Samples</a> |
| TLV1824RTER      | ACTIVE        | WQFN         | RTE             | 16   | 5000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | T1824B                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF TLV1811, TLV1812, TLV1814, TLV1821, TLV1822, TLV1824 :**

- Automotive : [TLV1811-Q1](#), [TLV1812-Q1](#), [TLV1814-Q1](#), [TLV1821-Q1](#), [TLV1822-Q1](#), [TLV1824-Q1](#)
- Enhanced Product : [TLV1812-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV1811DBVR  | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV1811DCKR  | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV1811LDBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV1811LDCKR | SC70         | DCK             | 6    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV1812DDFR  | SOT-23-THIN  | DDF             | 8    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV1812DGKR  | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV1812DR    | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV1812DSGR  | WSO          | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TLV1812PWR   | TSSOP        | PW              | 8    | 3000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLV1814DR    | SOIC         | D               | 14   | 3000 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLV1814DYR   | SOT-23-THIN  | DYY             | 14   | 3000 | 330.0              | 12.4               | 4.8     | 3.6     | 1.6     | 8.0     | 12.0   | Q3            |
| TLV1814RTER  | WQFN         | RTE             | 16   | 5000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TLV1821DBVR  | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV1821DCKR  | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV1821LDBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV1822DDFR | SOT-23-THIN  | DDF             | 8    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TLV1822DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV1822DR   | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV1822DSGR | WSON         | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TLV1822PWR  | TSSOP        | PW              | 8    | 3000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLV1824DR   | SOIC         | D               | 14   | 3000 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLV1824DYR  | SOT-23-THIN  | DYY             | 14   | 3000 | 330.0              | 12.4               | 4.8     | 3.6     | 1.6     | 8.0     | 12.0   | Q3            |
| TLV1824PWR  | TSSOP        | PW              | 14   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLV1824RTER | WQFN         | RTE             | 16   | 5000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV1811DBVR  | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1811DCKR  | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1811LDBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1811LDCKR | SC70         | DCK             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1812DDFR  | SOT-23-THIN  | DDF             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TLV1812DGKR  | VSSOP        | DGK             | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| TLV1812DR    | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 35.0        |
| TLV1812DSGR  | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TLV1812PWR   | TSSOP        | PW              | 8    | 3000 | 356.0       | 356.0      | 35.0        |
| TLV1814DR    | SOIC         | D               | 14   | 3000 | 356.0       | 356.0      | 35.0        |
| TLV1814DYR   | SOT-23-THIN  | DYY             | 14   | 3000 | 336.6       | 336.6      | 31.8        |
| TLV1814RTER  | WQFN         | RTE             | 16   | 5000 | 367.0       | 367.0      | 35.0        |
| TLV1821DBVR  | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1821DCKR  | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1821LDBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV1822DDFR  | SOT-23-THIN  | DDF             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TLV1822DGKR  | VSSOP        | DGK             | 8    | 2500 | 356.0       | 356.0      | 35.0        |
| TLV1822DR    | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 35.0        |

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| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV1822DSGR | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TLV1822PWR  | TSSOP        | PW              | 8    | 3000 | 356.0       | 356.0      | 35.0        |
| TLV1824DR   | SOIC         | D               | 14   | 3000 | 356.0       | 356.0      | 35.0        |
| TLV1824DYYR | SOT-23-THIN  | DYY             | 14   | 3000 | 336.6       | 336.6      | 31.8        |
| TLV1824PWR  | TSSOP        | PW              | 14   | 3000 | 356.0       | 356.0      | 35.0        |
| TLV1824RTER | WQFN         | RTE             | 16   | 5000 | 367.0       | 367.0      | 35.0        |

# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

### NOTES:

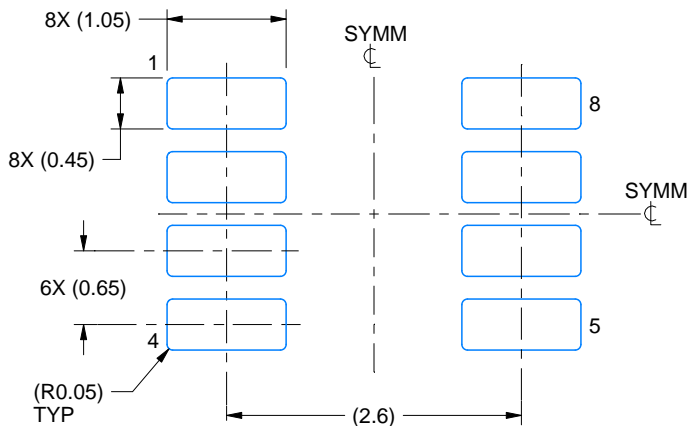
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

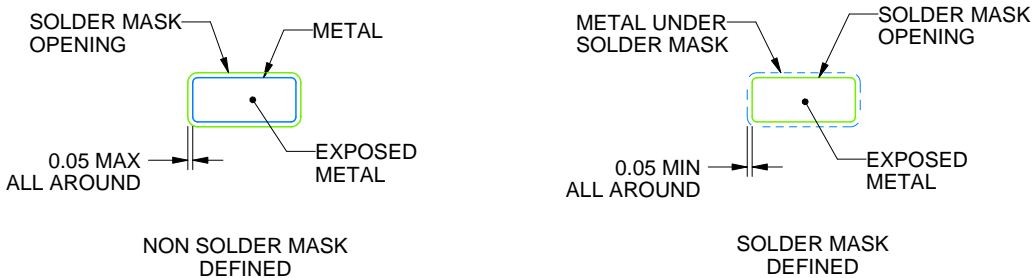
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

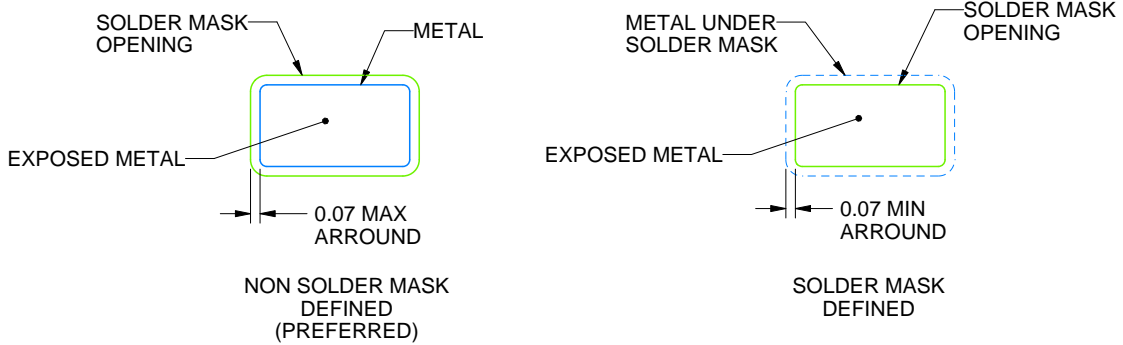
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

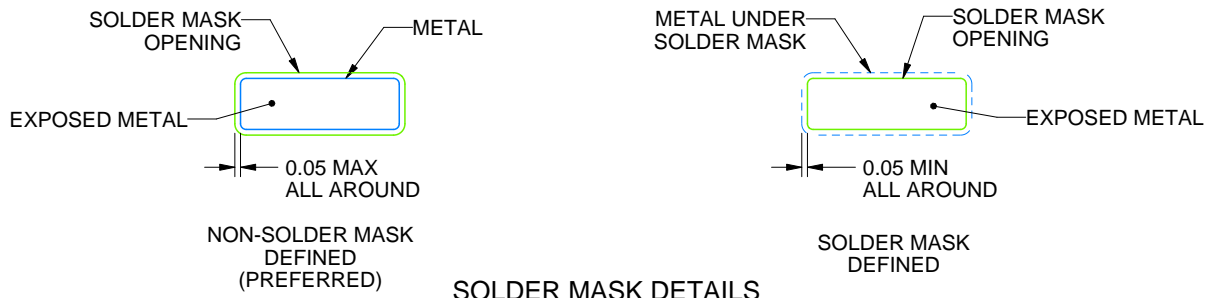
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

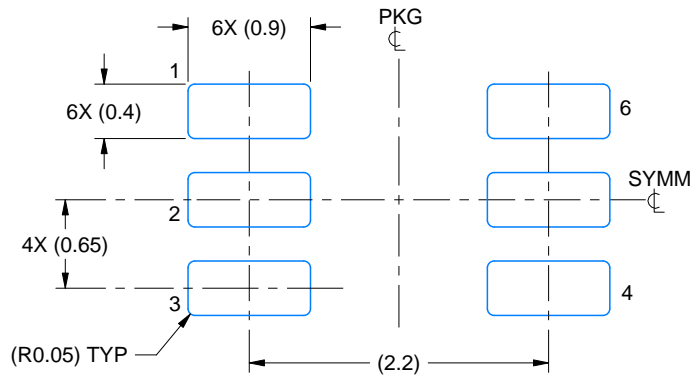
4214862/A 04/2023

NOTES: (continued)

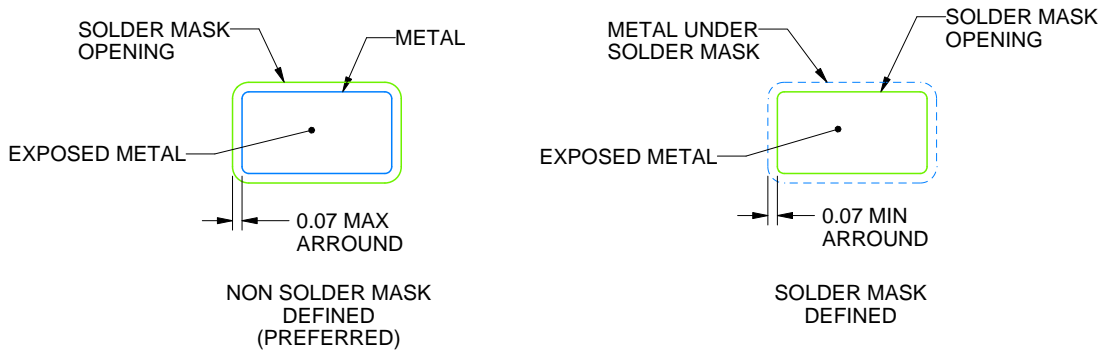
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.







LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

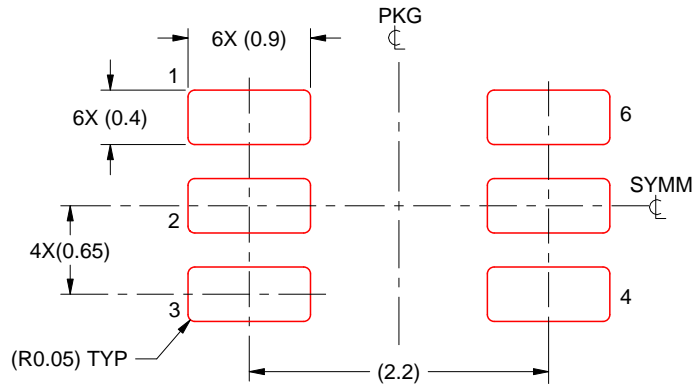


SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

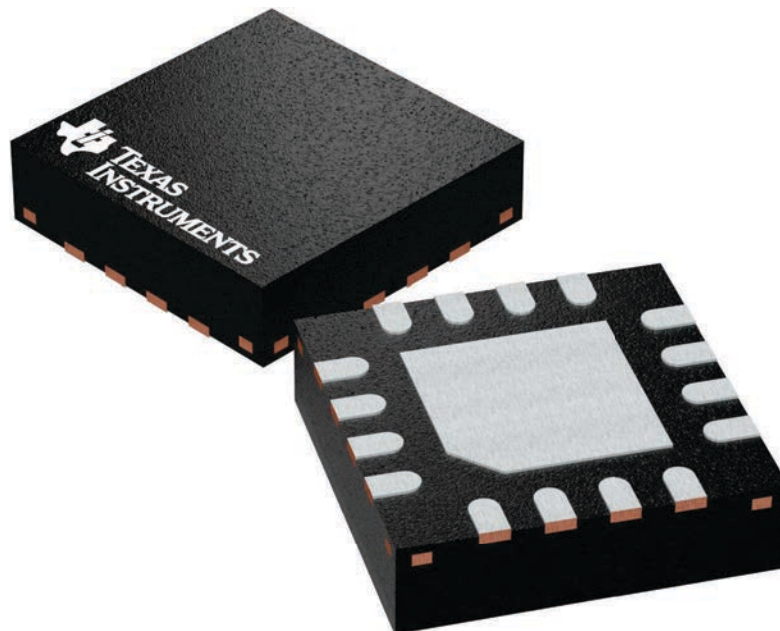
**RTE 16**

**WQFN - 0.8 mm max height**

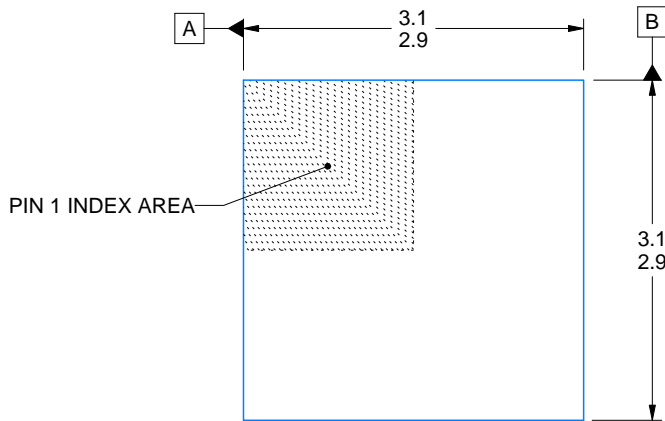
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

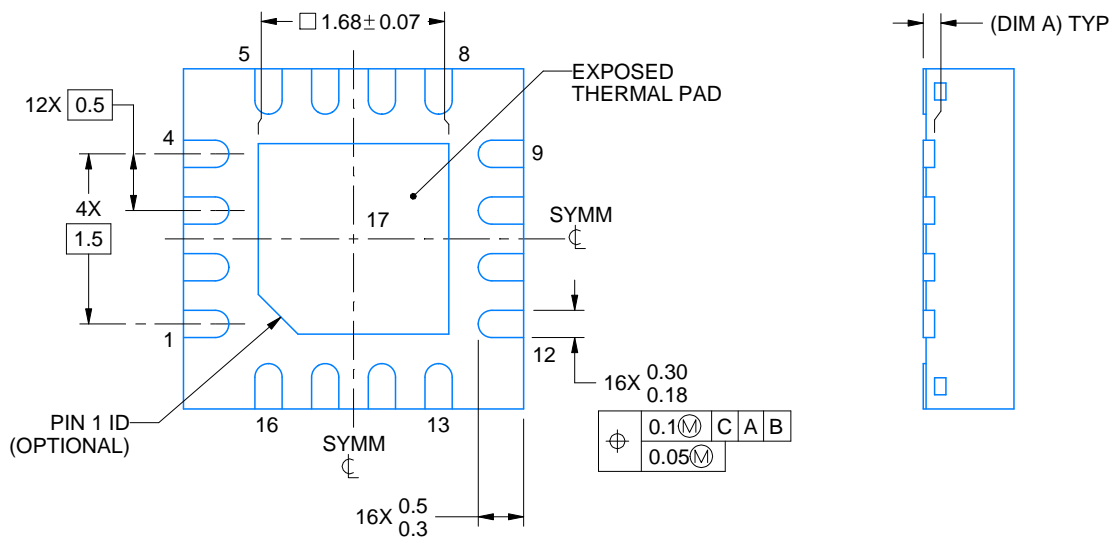
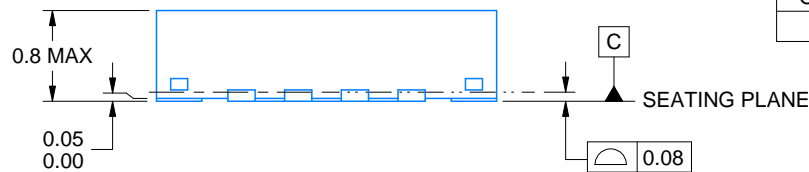
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A



| SIDE WALL METAL THICKNESS DIM A |          |
|---------------------------------|----------|
| OPTION 1                        | OPTION 2 |
| 0.1                             | 0.2      |



4219117/B 04/2022

NOTES:

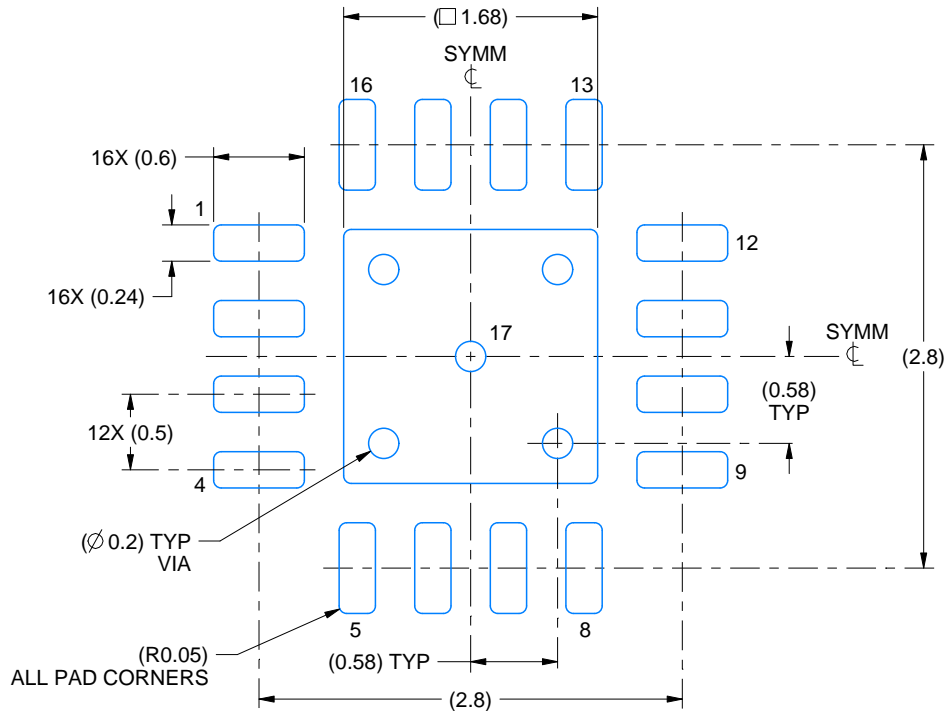
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

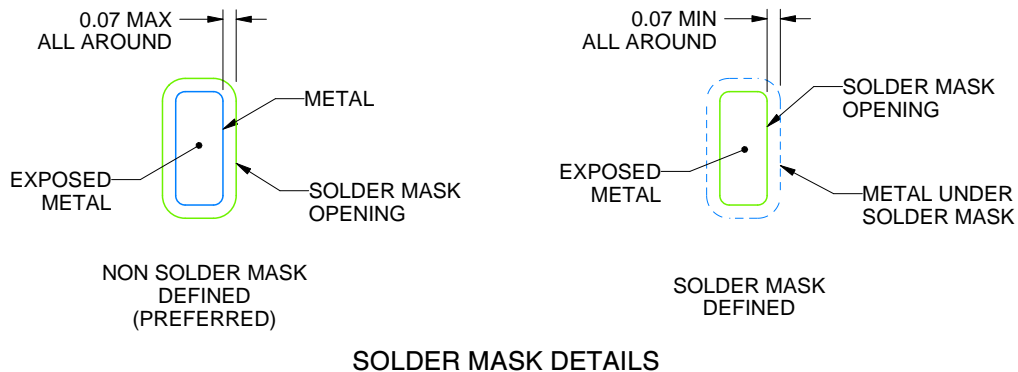
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

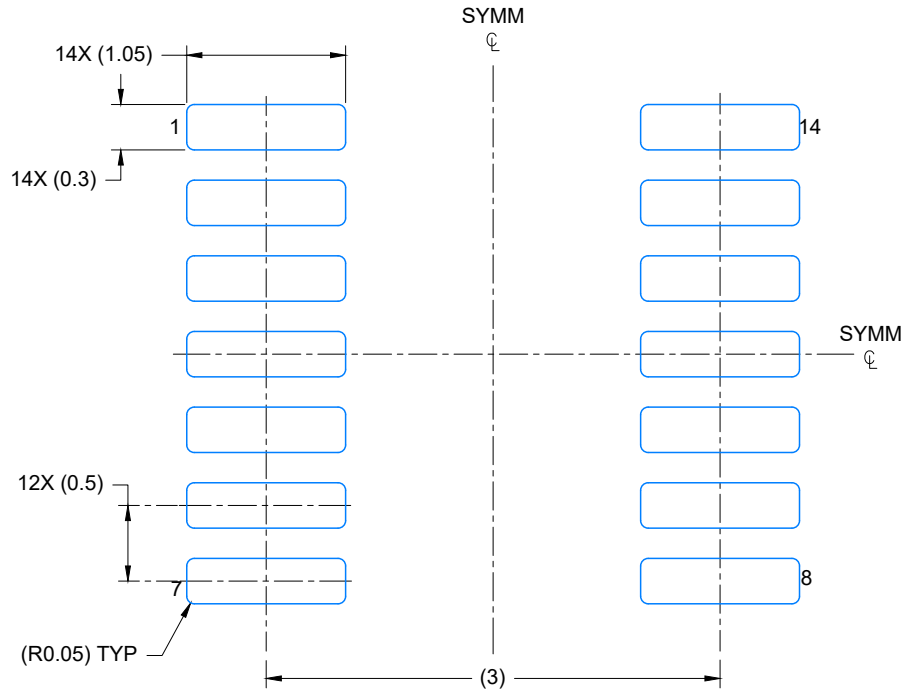
4219117/B 04/2022

NOTES: (continued)

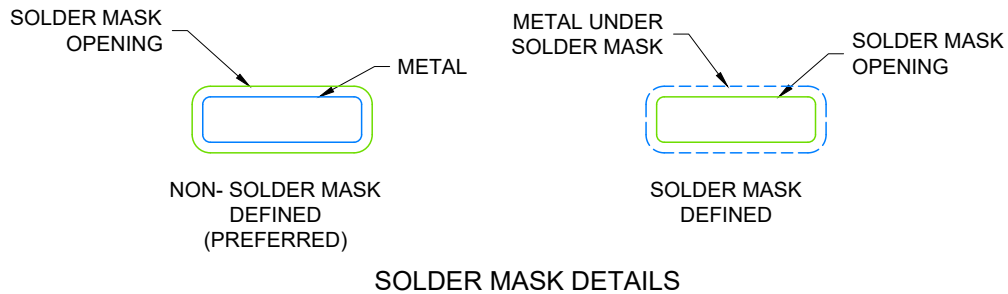
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

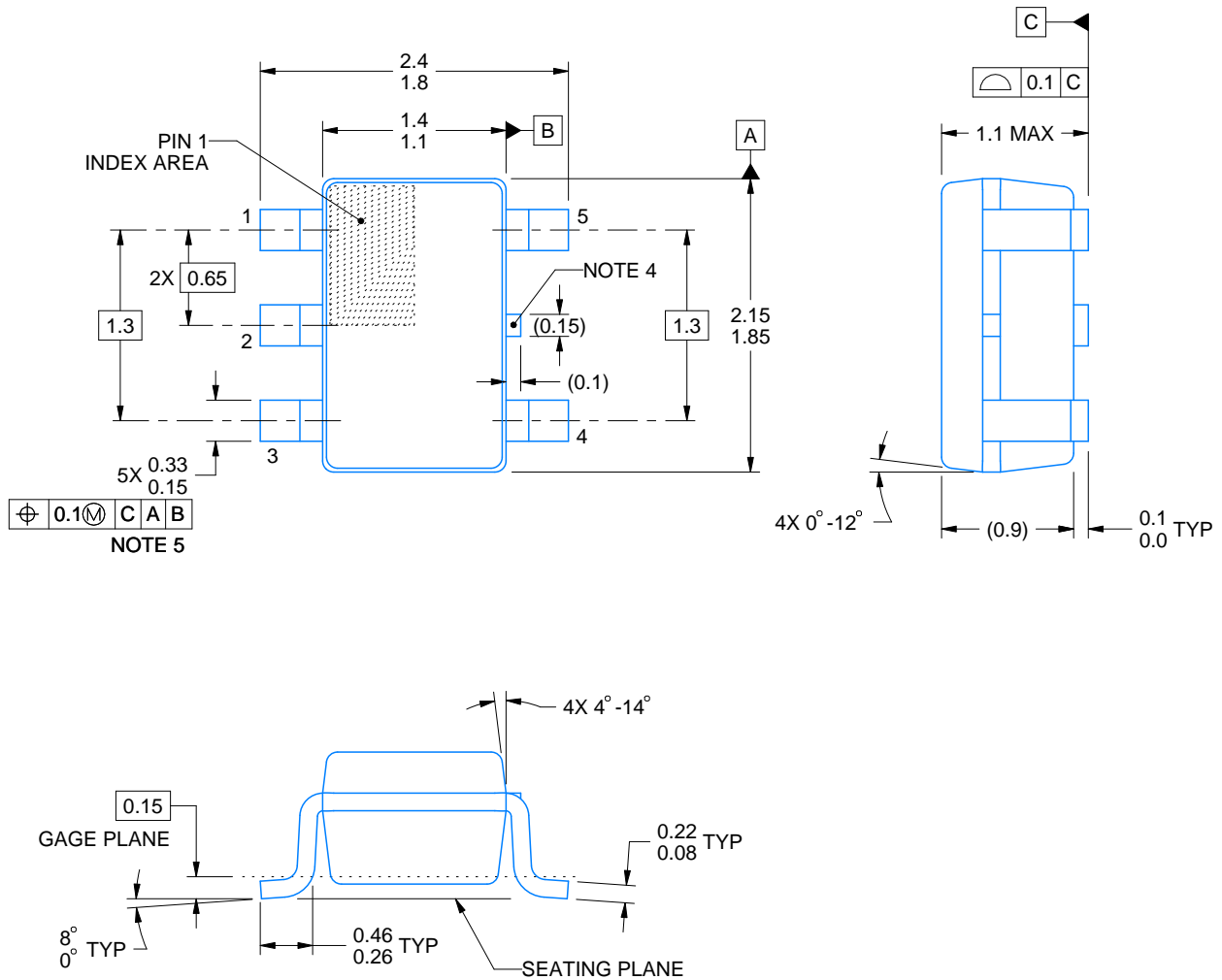
# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/F 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

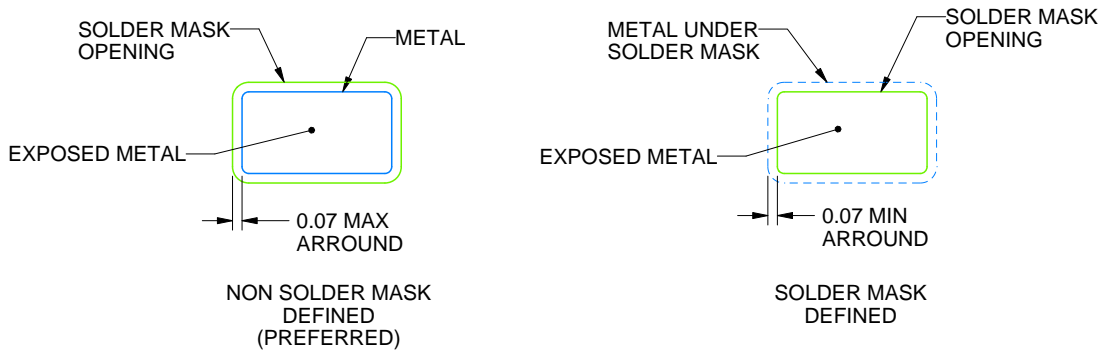
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

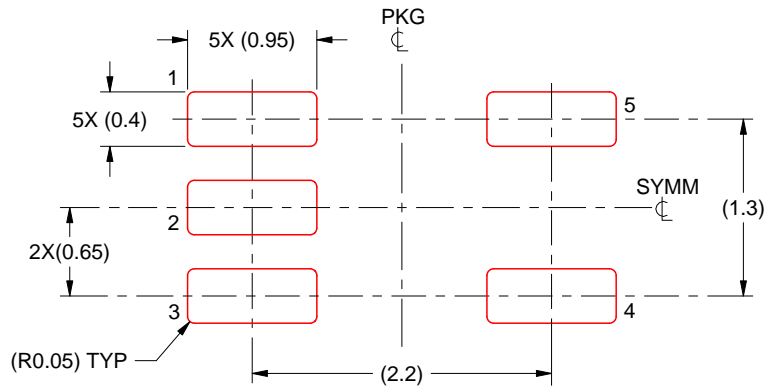
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

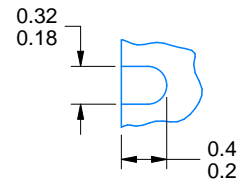
# DSG0008A



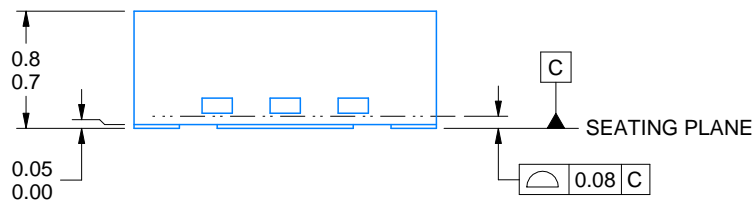
# PACKAGE OUTLINE

## WSON - 0.8 mm max height

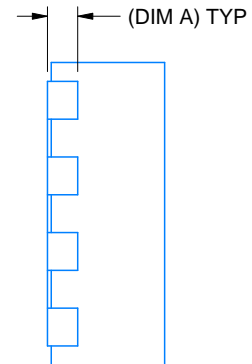
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



| SIDE WALL METAL THICKNESS DIM A |          |
|---------------------------------|----------|
| OPTION 1                        | OPTION 2 |
| 0.1                             | 0.2      |



4218900/E 08/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

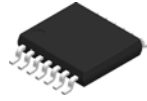
EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

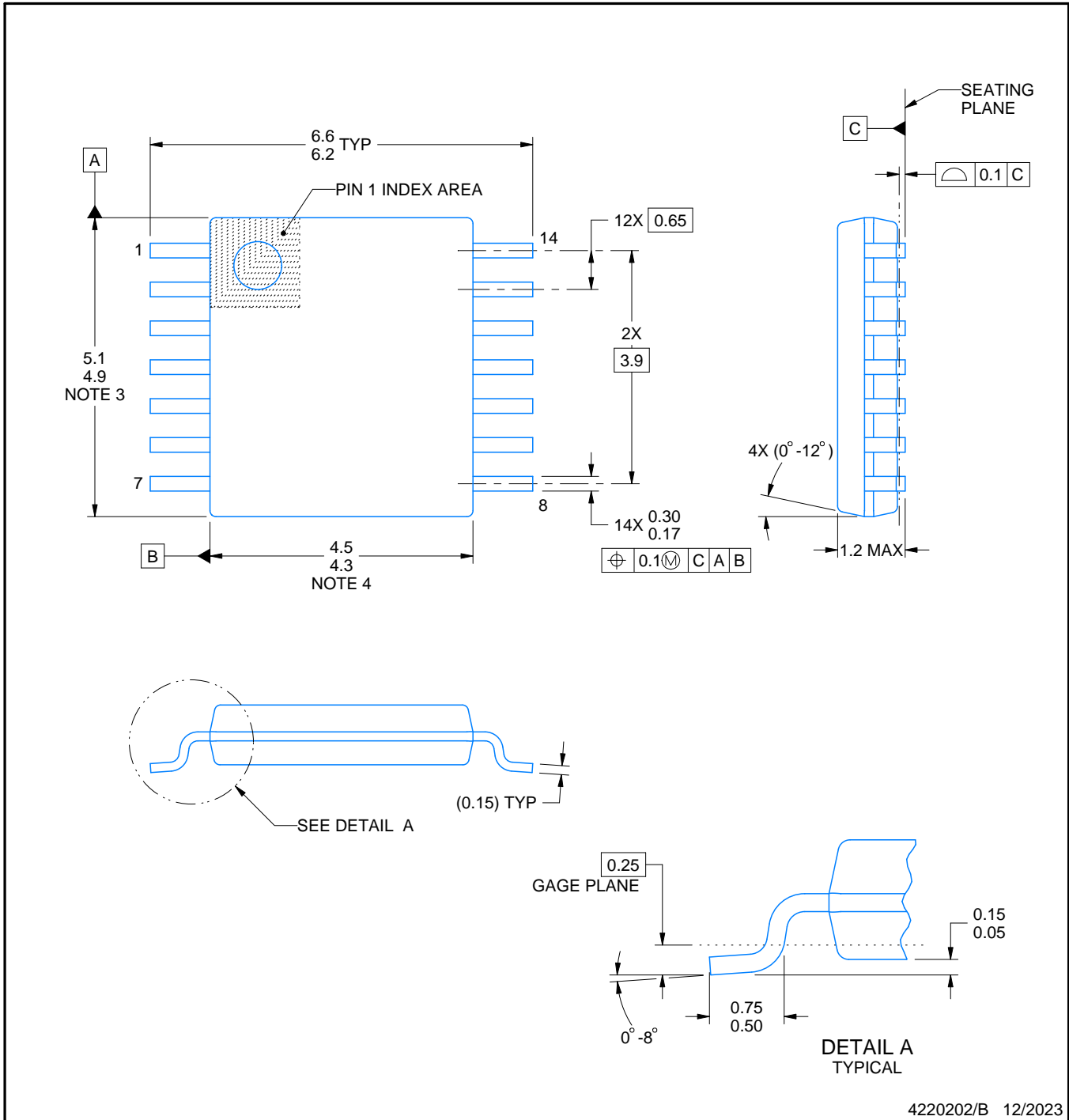
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.





# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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