TLV3011-EP および TLV3012-EP エンハンスド製品、低消費電力コンパレータ、1.24V 基準電圧内蔵

1 特長

- VID V62/07604-01XE (TLV3011-EP)
- VID V62/23603-01XE (TLV3012-EP)
- 管理されたベースライン
  - 単一のアセンブリ - テスト施設
  - 単一の製造施設
  - 長い製品ライフ・サイクル
- 拡張 DMS (Diminishing Manufacturing Sources) サポート
- -55℃～125℃の拡張温度範囲
- 低静止電流:3.1μA (最大値)
- シリーズ基準電圧内蔵:1.242V
- 入力同相範囲:レールの 200mV 外まで
- 基準電圧の初期精度:1%
- オープン・ドレイン出力 (TLV3011-EP)
- プッシュプル出力 (TLV3012-EP)
- 相互ヒステリシス (TLV3012-EP のみ)
- フェイルセーフ入力 (TLV3012-EP のみ)
- パワーオン・リセット (TLV3012-EP のみ)
- 電源電圧範囲:1.65V～5.5V (TLV3012-EP のみ)
- 迅速な応答時間:2μs
- 超小型パッケージ:SOT-23-6

2 アプリケーション

- バッテリ駆動の液面検出
- データ・アクイジション
- システム監視
- 発振器
- センサ・システム

3 概要

TLV3011-EP は低消費電力オープン・ドレイン出力のコンパレータです。TLV3012-EP はプッシュプル出力のコンパレータです。どちらのデバイスも、不確定なオンチップ基準電圧を採用しており、静止電流が 3.1μA (最大値)、電源レールを上回る 200mV 入力同相範囲、1.65V～5.5V の単一電源で動作します。

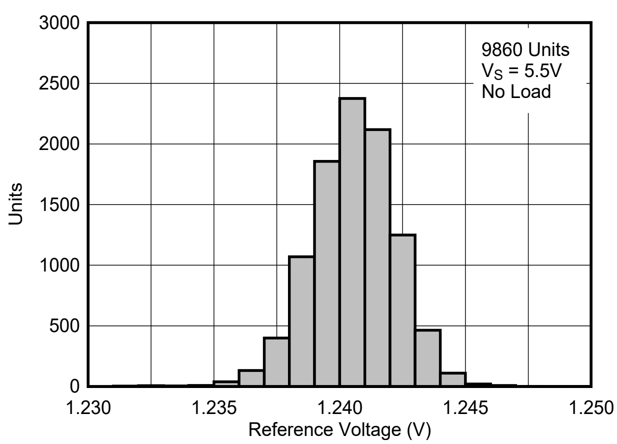
内蔵 1.242V シリーズ基準電圧は、100ppm/℃ (最大値) の低ドリフトを実現し、最大 10nF の容量性負荷で安定しており、最大 0.5mA (標準値) の出力電流をシンクまたはソースできるため、外部回路を駆動できます。

TLV3011-EP および TLV3012-EP は、スペースに制約のある設計向けの小型 SOT-23-6 パッケージで供給されます。これらのデバイスは、-55℃～125℃の拡張温度範囲で動作が規定されています。

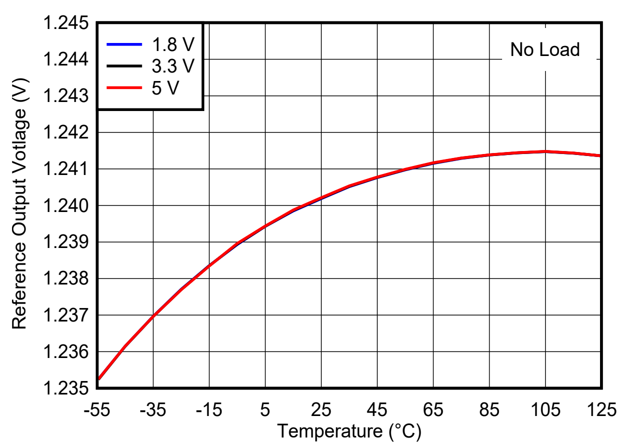
表 3-1. 製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLV3011-EP、TLV3012-EP	SOT-23 (6)	2.90mm × 1.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TLV3012-EP 基準電圧の分布



TLV3012-EP 基準電圧と温度との関係

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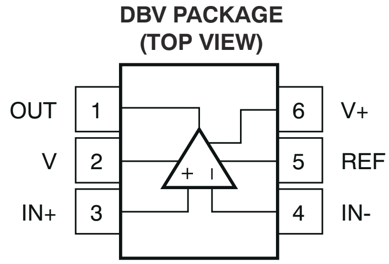
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2006) to Revision A (May 2023) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新.......... 1
- TLV3012-EP デバイスを追加.......... 1
- 新しいデバイスの「特長」、「概要」、「製品情報」表を更新 1
- Added TLV3012-EP *Electirical Characteristics* Tables.......... 4
- Added TLV3012-EP *Typical Characteristics* graphs.......... 12
- Updated *Detailed Description* section.......... 18

5 Pin Configuration and Functions



DBV Package
6-Pin SOT-23
Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUT	1	O	Comparator Output
V-	2	P	Negative Supply Voltage
IN+	3	I	Non-Inverting (Positive) Input
IN-	4	I	Inverting (Negative) Input
REF	5	O	Reference Voltage Output
V+	6	P	Positive Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings - TLV3011-EP

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
	Supply voltage			7	V
	Signal input terminals	Voltage[(2)]	–0.5	(V+) +0.5	V
		Current[(2)]		±10	mA
	Output short circuit[(3)]			Continous	
	Operating temperature range		–55	125	°C
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Short circuit to ground

6.2 Absolute Maximum Ratings - TLV3012-EP

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.5	7	V
Input pins (IN+, IN–) from (V–)[(2)]	–0.5	7	V
Output (OUT) (Push-Pull) from (V–)	–0.5	(V+) + 0.5	V
Output short circuit current[(3)]		10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to (V–). Inputs (IN+, IN–) can be greater than (V+) as long as within the –0.5 V to 7 V range. Inputs beyond –0.3 V must be current-limited to less than –10 mA, while inputs beyond 7 V must be externally voltage clamped.
(3) Short-circuit to (V–) or (V+).

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)] (TLV3012-EP Only)	±1000	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Resistance Characteristics

THERMAL METRIC[1]		TLV3011-EP DBV (SOT-23) 6 PINS	TLV3012-EP DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.9	162.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.9	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.7	42.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.2	21.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.2	41.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* report.

6.5 Recommended Operating Conditions - TLV3011-EP

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.8	5.5	V
Input voltage range from (V–)	–0.2	(V+) + 0.2	V
Output voltage range from (V–)	–0.2	≤ V+	V
Ambient temperature, T_A	–55	125	°C

6.6 Recommended Operating Conditions - TLV3012-EP

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	Supply voltage: V_S = (V+) – (V–)	1.65	5.5	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Ambient temperature, T_A		–55	125	°C

6.7 Electrical Characteristics - TLV3011-EP

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Voltage							
V_{OS}	Input offset voltage		V_{CM} = 0 V, I_O = 0 V		0.5	15	mV
dV_{OS}/dT	Input offset voltage vs temperature		T_A = –55°C to 125°C		±12		μV/°C
PSRR	Power supply rejection ratio		V_S = 1.8 V to 5.5 V		100	1000	μV/V
Input Bias Current							
I_S	Input bias current		$V_{CM} = V_S/2$		±10		pA
I_{OS}	Input offset current		$V_{CM} = V_S/2$		±10		pA
Input Voltage Range							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio		V_{CM} = –0.2 V to (V+) – 1.5 V	60	74		dB
			V_{CM} = –0.2 V to (V+) + 0.2 V	54	62		
Input Impedance							
	Common mode				10^{13} ‖ 2		Ω ‖ pF
	Differential				10^{13} ‖ 4		Ω ‖ pF
Switching Characteristics							
t_{pd}	Propagation delay time	Low to high	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		12		μs
			f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6		
		High to low	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		13.5		
			f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6.5		
t_r	Rise time		C_L = 10 pF		(1)		
t_f	Fall time		C_L = 10 pF		100		ns
Output							
V_{OL}	Voltage output low from rail		V_S = 5 V		160	200	mV
Voltage Reference							
V_{OUT}	Output voltage			1.208	1.242	1.276	V
	Initial accuracy					±1%	
dV_{OUT}/d_T	Temperature drift		–55°C ≤ T_A ≤ 125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load regulation	Sourcing	0 mA < I_{SOURCE} ≤ 0.5 mA		0.36	1	mV/mA
		Sinking	0 mA < I_{SINK} ≤ 0.5 mA		6.6		
I_{LOAD}	Output current				0.5		mA
dV_{OUT}/dV_{IN}	Line regulation		1.8 V ≤ V_{IN} ≤ 5.5 V		10	100	μV/V
Noise							
	Reference voltage noise		f = 0.1 Hz to 10 Hz		0.2		mV_{PP}
Power Supply							
V_S	Specified voltage			1.8		5.5	V
	Operating voltage range			1.8		5.5	V
I_Q	Quiescent current		V_S = 5 V, V_O = High		2.8	5	μA

(1) t_r dependent on R_{PULLUP} and C_{LOAD}.

6.8 Electrical Characteristics - TLV3012-EP

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V–)	–6	±0.3	6	mV
V_{OS}	Input offset voltage	V_{CM} = (V–) T_A = –55°C to +125°C	–9		9	mV
dV_{IO}/dT	Input offset voltage drift	V_{CM} = (V–) T_A = –55°C to +125°C		±12		µV/°C
PSRR	power supply rejection ratio	V_{CM} = (V–) V_S = 1.65 V to 5.5 V T_A = –55°C to +125°C		100	1000	µV/V
V_{HYS}	Input hysteresis voltage	T_A = –55°C to +125°C	2	6	8	mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S /2	–10(1)	±4.5	10(1)	pA
I_{OS}	Input offset current	V_{CM} = V_S /2	–10(1)	±1	10(1)	pA
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8 V to 5.5 V T_A = –55°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common mode rejection ratio	V_{CM} = (V–) + 1.5V to (V+) + 0.2V T_A = –55°C to +125°C	60	74		dB
CMRR	Common mode rejection ratio	V_{CM} = (V–) - 0.2V to (V+) + 0.2V T_A = –55°C to +125°C	54	62		dB
R_{CM}	Input Common Mode Resistance			10^{13}		Ω
C_{IC}	Input Common Mode Capacitance			2		pF
INPUT IMPEDANCE						
R_{DM}	Input Differential Mode Resistance			10^{13}		Ω
C_{ID}	Input Differential Mode Capacitance			4		pF
OUTPUT						
V_{OL}	Voltage swing from (V–)	V_S = 5 V I_{SINK} = 5 mA T_A = –55°C to +125°C		160	200	mV
V_{OH}	Voltage swing from (V+)	V_S = 5 V I_{SOURCE} = 5 mA T_A = –55°C to +125°C		90	200	mV
VOLTAGE REFERENCE						
V_{OUT}	Reference Voltage		1.223	1.242	1.260	V
	Accuracy			±0.25%	±1.5%	
dV_{OUT}/d_T	Temperature Drift	T_A = –55°C to +125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load Regulation, Sourcing	0 mA < I_{SOURCE} ≤ 0.5 mA		0.36	1(1)	mV/mA
	Load Regulation, Sinking	0 mA < I_{SINK} ≤ 0.5 mA		6.6		mV/mA
ILOAD	Output Current			0.5		mA
dV_{OUT}/dV_S	Line Regulation	1.65 V ≤ V_S ≤ 5.5 V		10	100(1)	µV/V
V_{noise}	Noise	f = 0.1 Hz to 10 Hz		0.2		mV_{PP}

6.8 Electrical Characteristics - TLV3012-EP (continued)

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per comparator	Output is logic high		2.4	3.1	µA
I_Q	Quiescent current per comparator	Output is logic high T_A = –55°C to +125°C			3.6	µA

(1) Ensured by characterization

6.9 Switching Characteristics - TLV3012-EP

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8 V and 5.5 V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-LH}	Propagation delay time, low-to-high (push-pull output)	f = 10 kHz, V_{STEP} = 200mV, V_{OD} = 100 mV, C_L = 10 pF		2	4	µs
T_{PD-HL}	Propagation delay time, high-to-low	f = 10 kHz, V_{STEP} = 200mV, V_{OD} = 100 mV, C_L = 10 pF		2	4	µs
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 10 pF		10		ns
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 10 pF		10		ns
T_{FALL}	Output Fall Time, 80% to 20%, open-drain output	R_L = 10 kΩ, C_L = 10 pF		10		ns
t_{ON}	Power on-time			1.9		ms

6.10 Typical Characteristics - TLV3011-EP

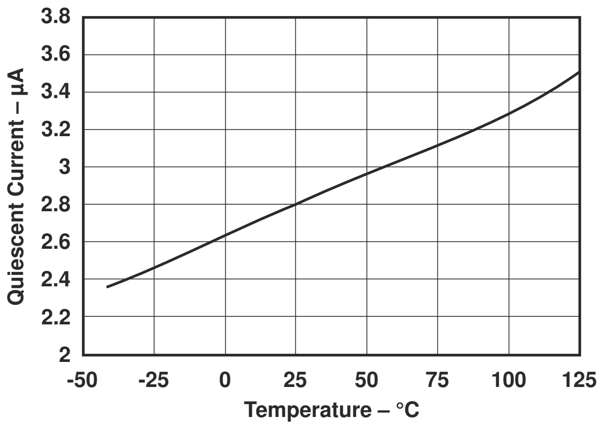


図 6-1. QUIESCENT CURRENT vs TEMPERATURE

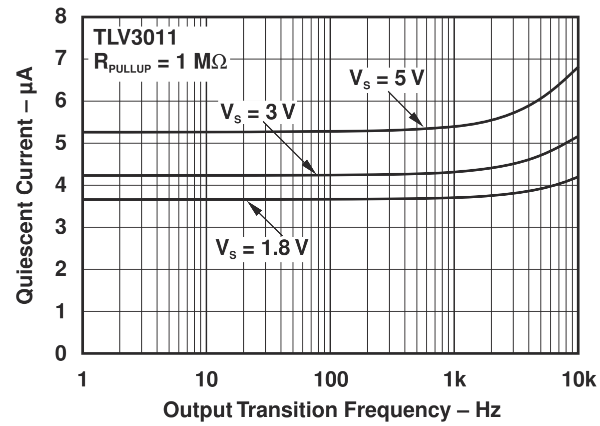


図 6-2. QUIESCENT CURRENT vs OUTPUT SWITCHING FREQUENCY

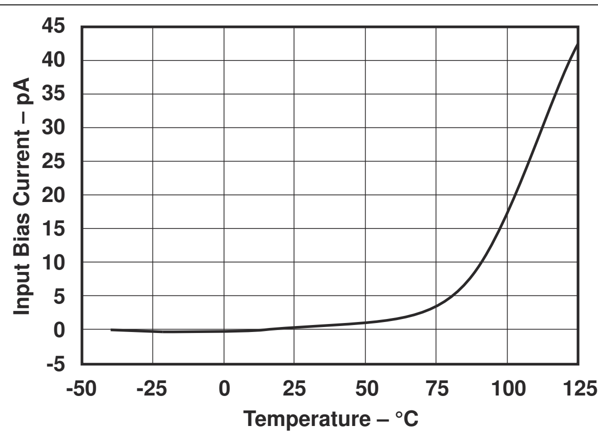


図 6-3. INPUT BIAS CURRENT vs TEMPERATURE

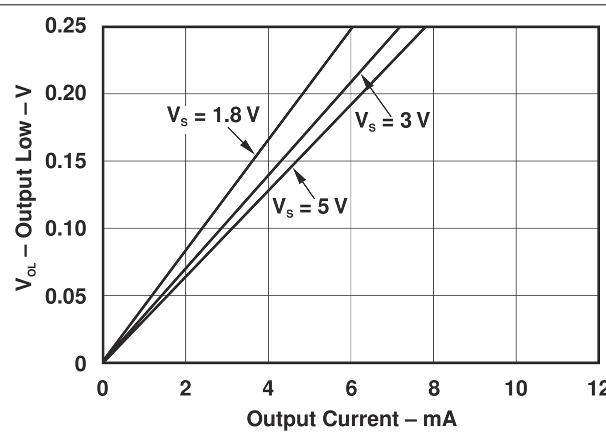


図 6-4. OUTPUT LOW vs OUTPUT CURRENT

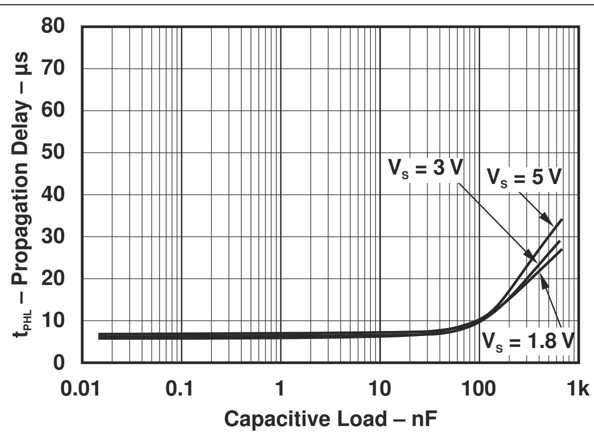


図 6-5. PROPAGATION DELAY (t_{PHL}) vs CAPACITIVE LOAD

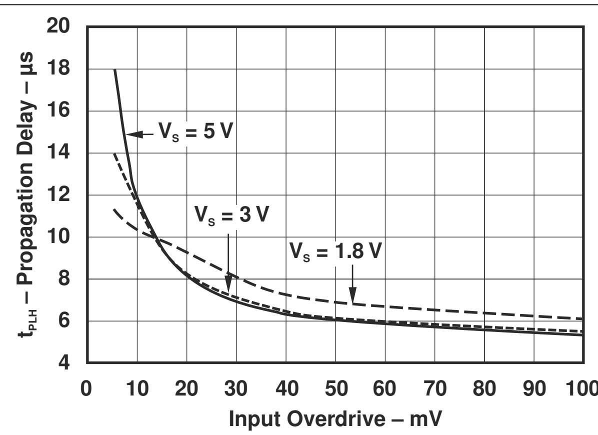


図 6-6. PROPAGATION DELAY (t_{PLH}) vs INPUT OVERDRIVE

6.10 Typical Characteristics - TLV3011-EP (continued)

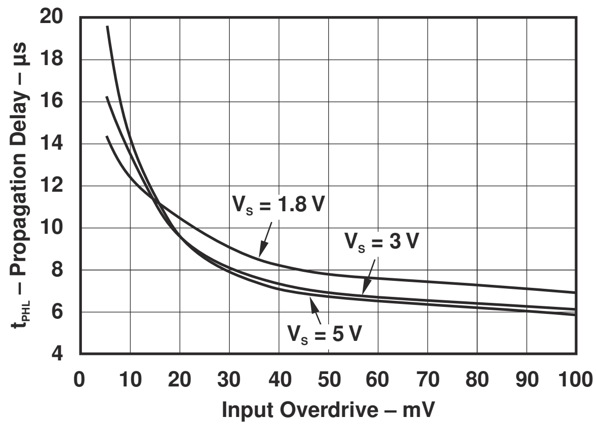


図 6-7. PROPAGATION DELAY (t_{PHL}) vs INPUT OVERDRIVE

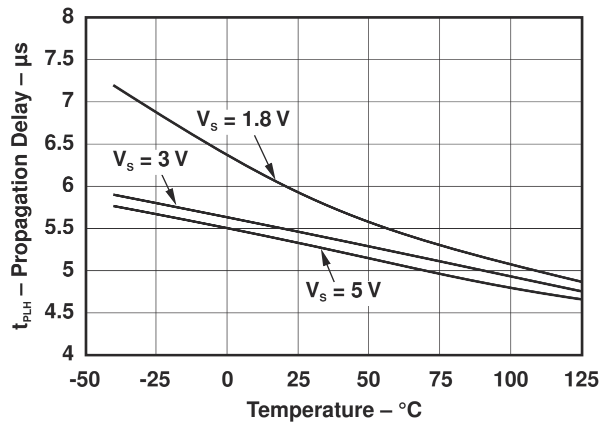


図 6-8. PROPAGATION DELAY (t_{PLH}) vs TEMPERATURE

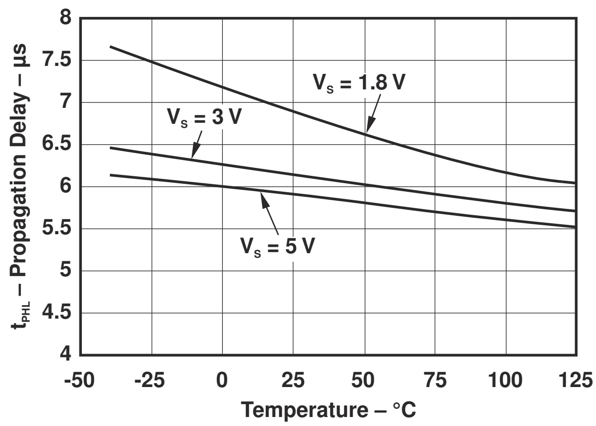


図 6-9. PROPAGATION DELAY (t_{PHL}) vs TEMPERATURE

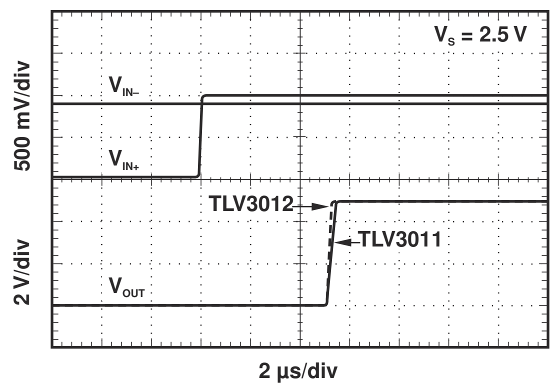


図 6-10. PROPAGATION DELAY (t_{PLH})

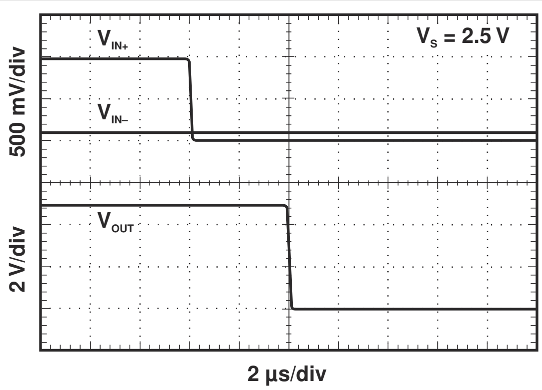


図 6-11. PROPAGATION DELAY (t_{PHL})

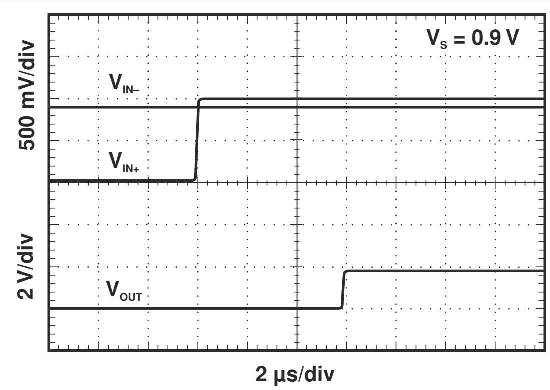


図 6-12. PROPAGATION DELAY (t_{PLH})

6.10 Typical Characteristics - TLV3011-EP (continued)

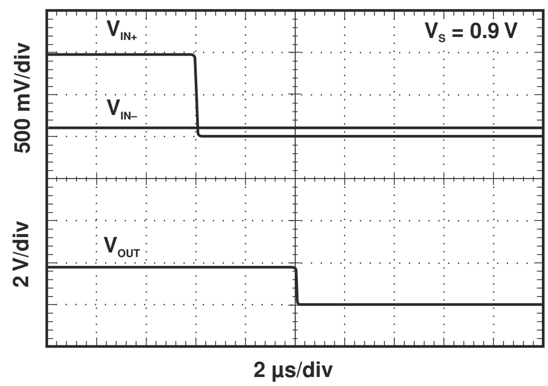


図 6-13. PROPAGATION DELAY (t_{PHL})

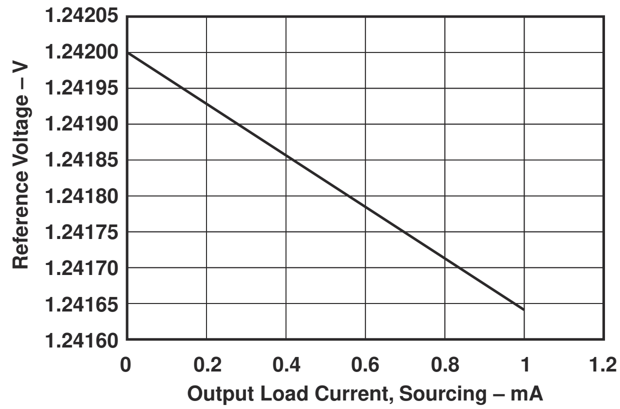


図 6-14. REFERENCE VOLTAGE vs OUTPUT LOAD CURRENT (SOURCING)

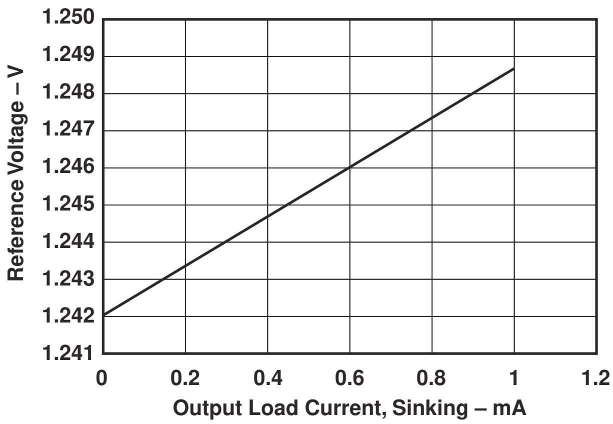


図 6-15. REFERENCE VOLTAGE vs OUTPUT LOAD CURRENT (SINKING)

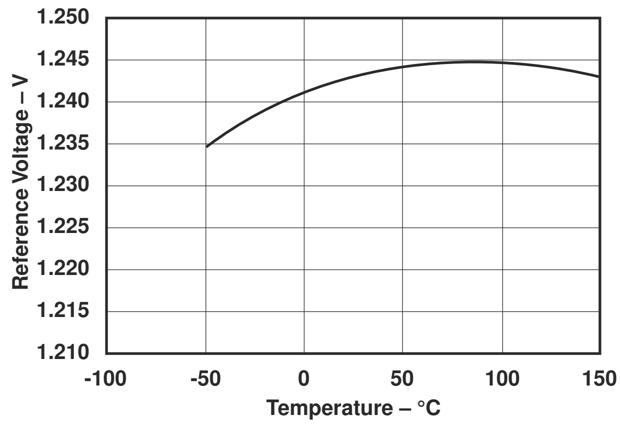


図 6-16. REFERENCE VOLTAGE vs TEMPERATURE

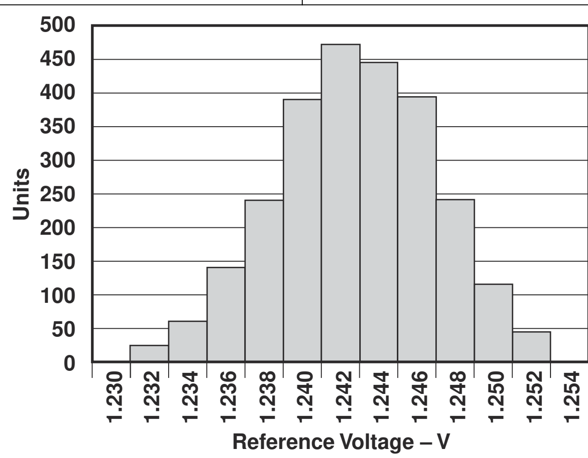


図 6-17. REFERENCE VOLTAGE DISTRIBUTION

6.11 Typical Characteristics - TLV3012-EP

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

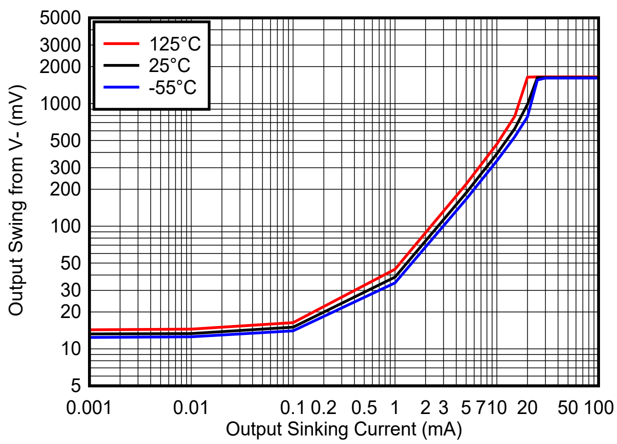


図 6-18. Output Swing vs. Output Sinking Current - 1.8V

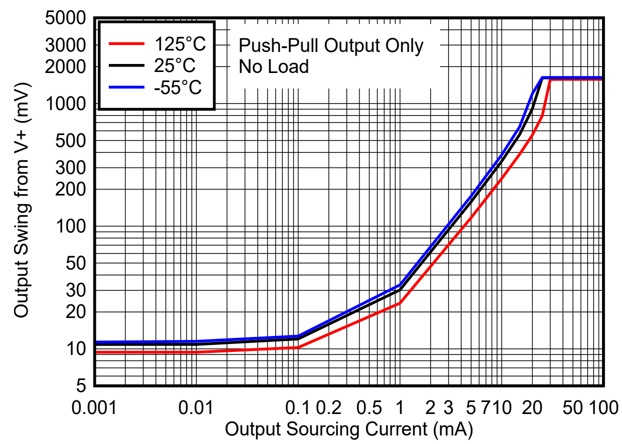


図 6-19. Output Swing vs. Output Sourcing Current - 1.8V

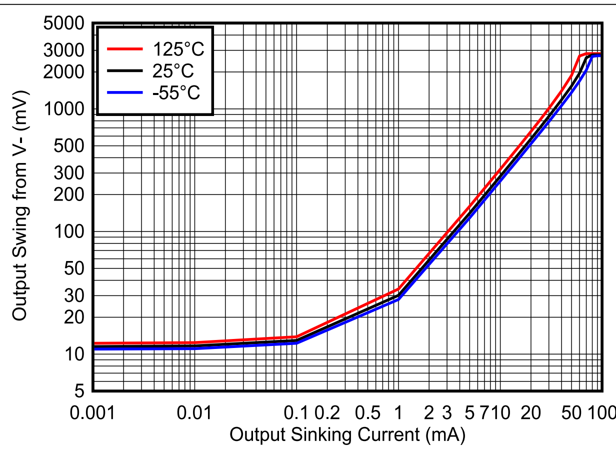


図 6-20. Output Swing vs. Output Sinking Current - 3.3V

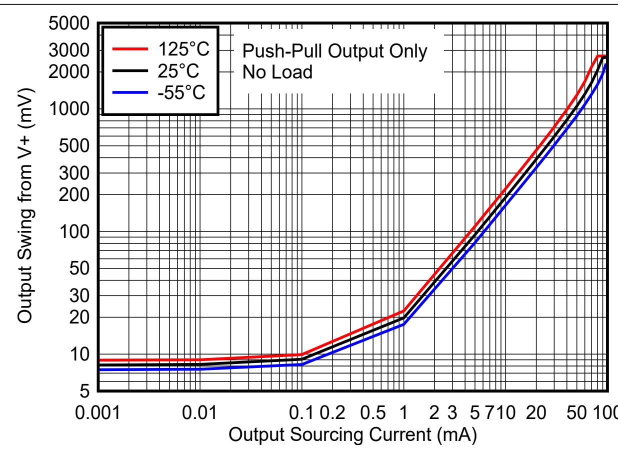


図 6-21. Output Swing vs. Output Sourcing Current - 3.3V

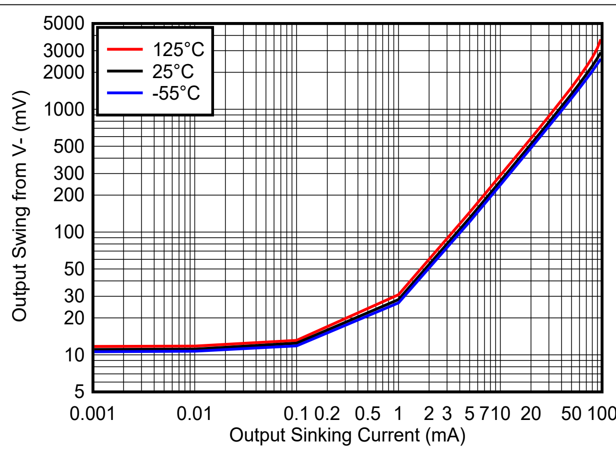


図 6-22. Output Swing vs. Output Sinking Current - 5V

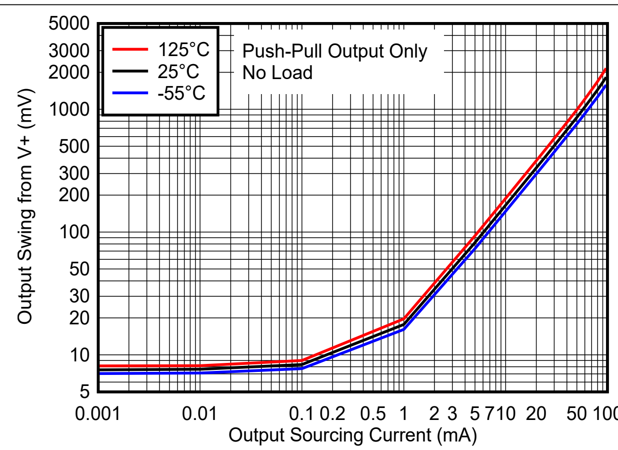


図 6-23. Output Swing vs. Output Sourcing Current - 5V

6.11 Typical Characteristics - TLV3012-EP (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

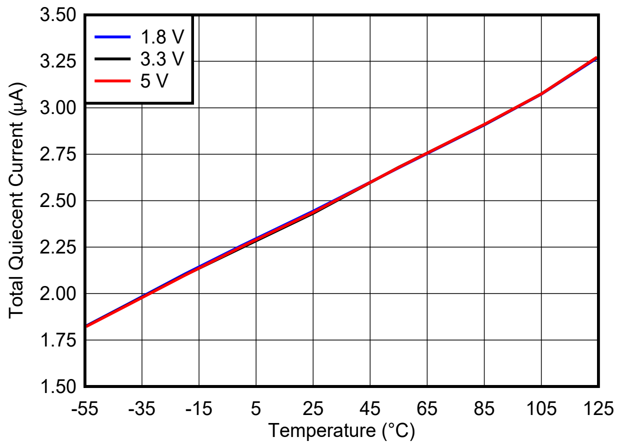


図 6-24. Supply Current vs. Temperature

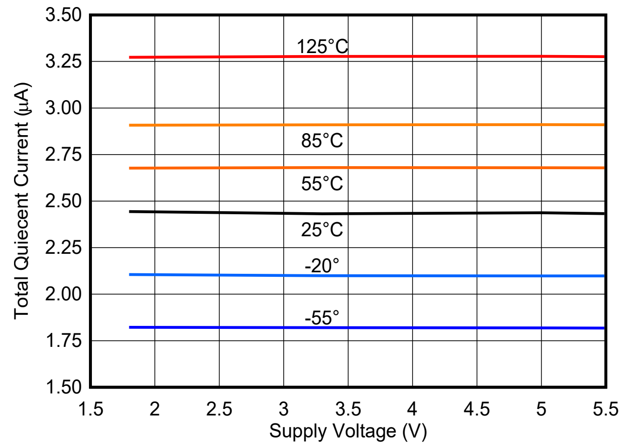


図 6-25. Supply Current vs. Supply Voltage

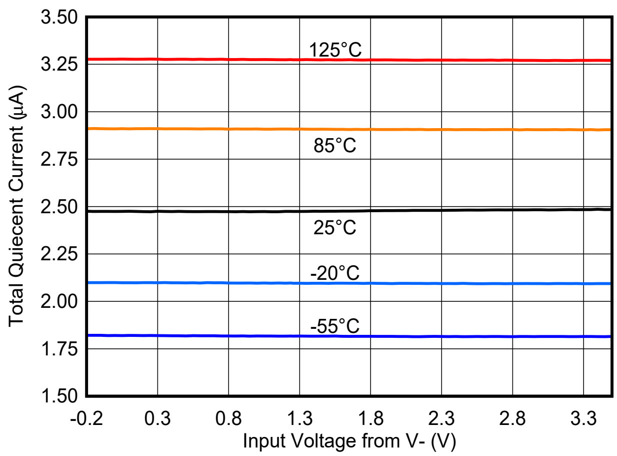


図 6-26. Supply Current vs. Common Mode - 3.3V

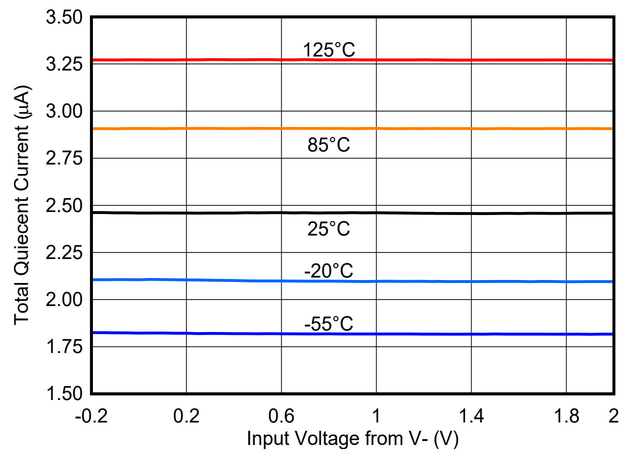


図 6-27. Supply Current vs. Common Mode - 1.8V

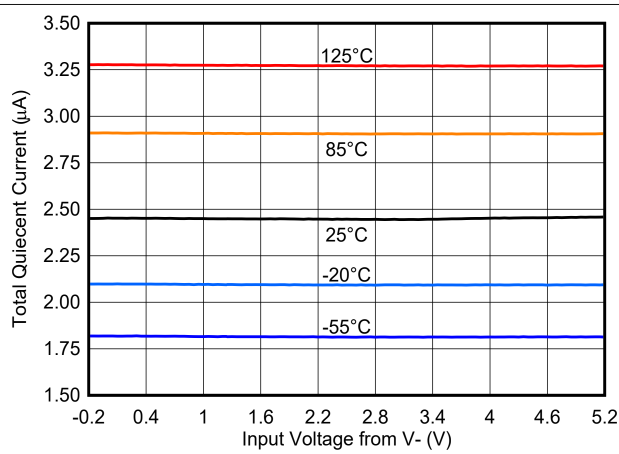


図 6-28. Supply Current vs. Common Mode - 5V

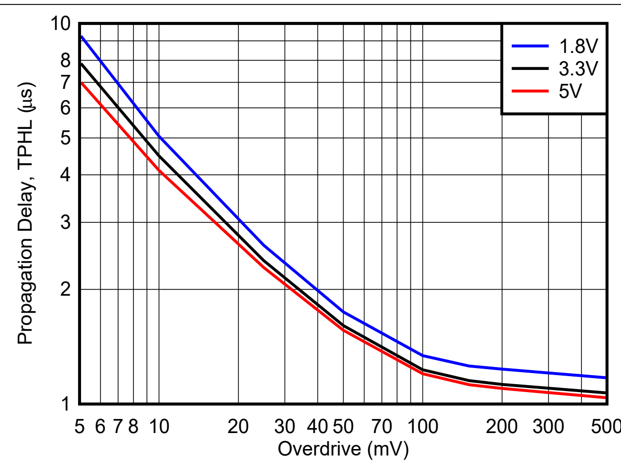


図 6-29. High to Low Propagation Delay vs. Overdrive

6.11 Typical Characteristics - TLV3012-EP (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

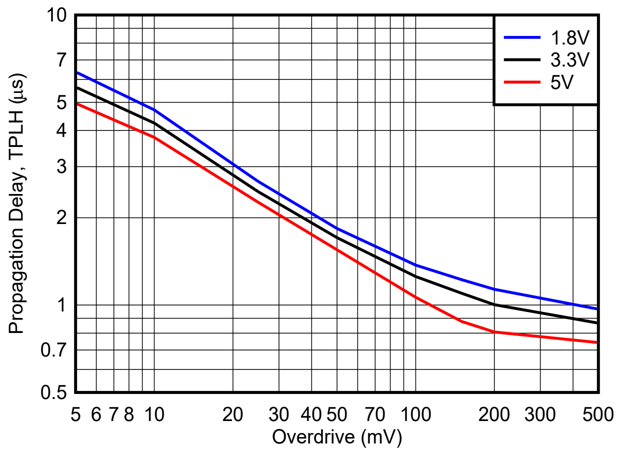


図 6-30. Low to High Propagation Delay vs. Overdrive

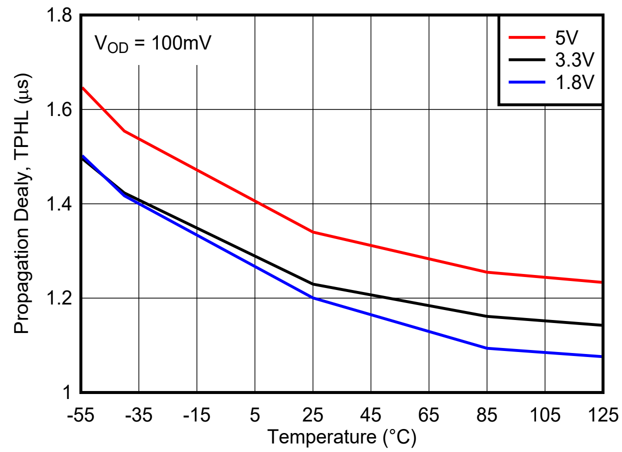


図 6-31. High to Low Propagation Delay vs. Temperature

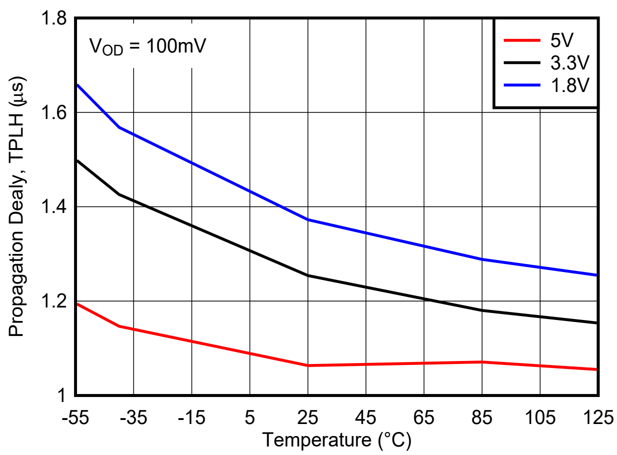


図 6-32. Low to High Propagation Delay vs. Temperature

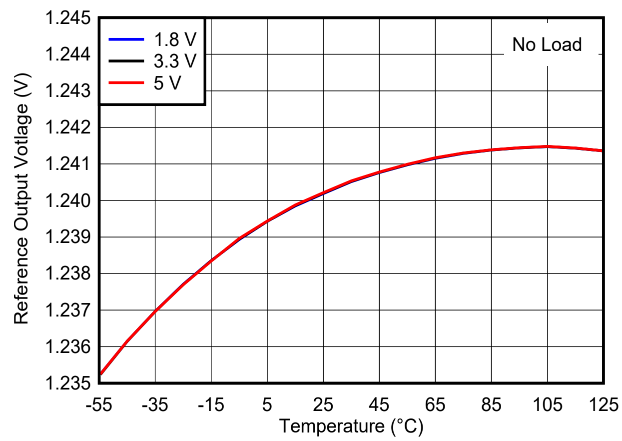


図 6-33. Reference Voltage vs. Temperature

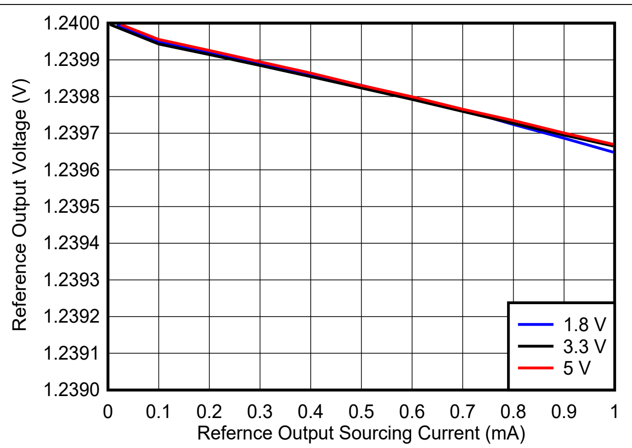


図 6-34. Reference Voltage vs. Reference Output Sourcing Current

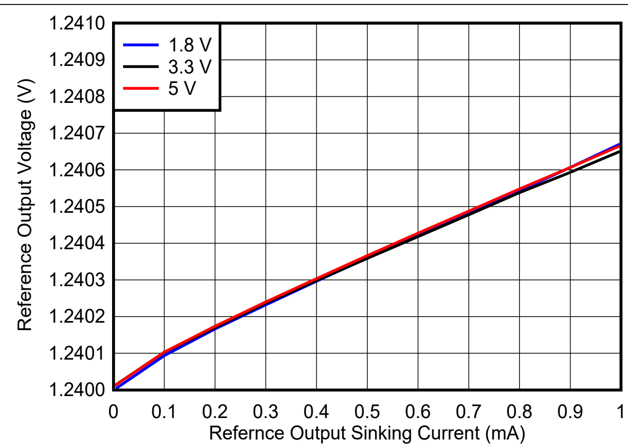


図 6-35. Reference Voltage vs. Reference Output Sinking Current

6.11 Typical Characteristics - TLV3012-EP (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

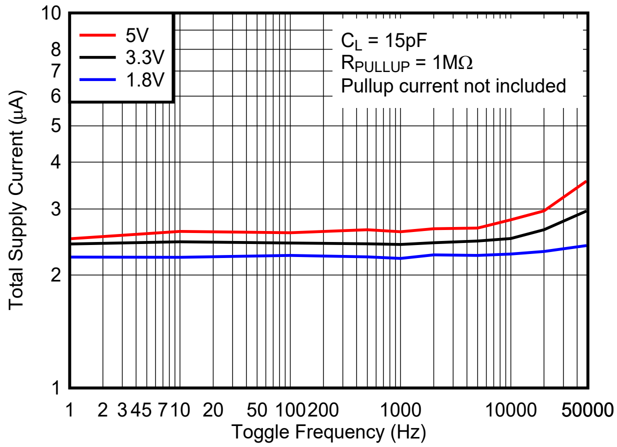


図 6-36. Supply Current vs. Toggle Frequency - Open Drain Output

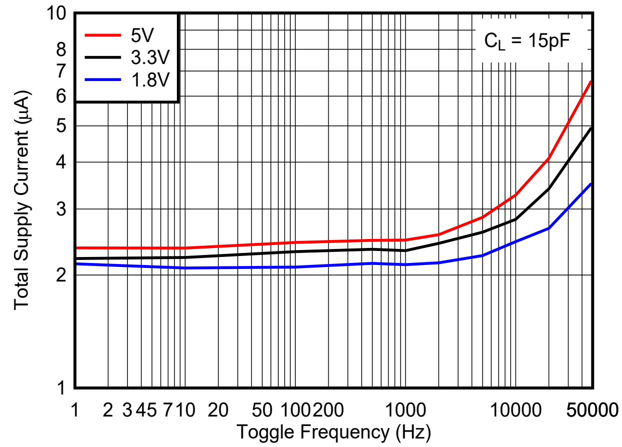


図 6-37. Supply Current vs. Toggle Frequency - Push-Pull Output

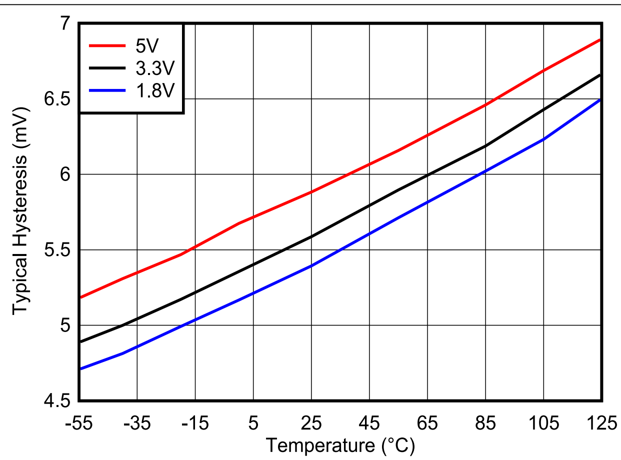


図 6-38. Hysteresis Voltage vs. Temperature

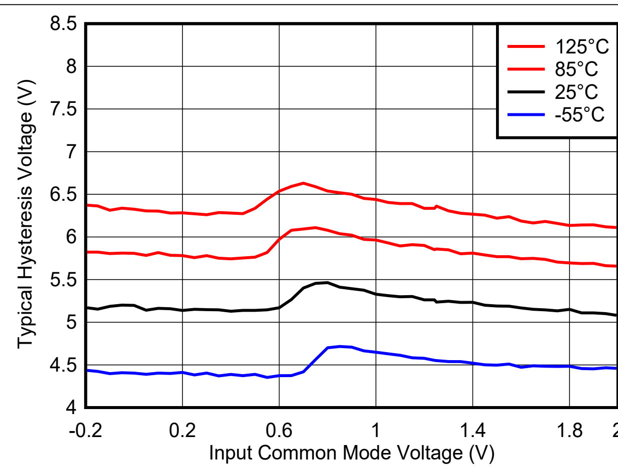


図 6-39. Hysteresis Voltage vs. Common Mode, 1.8V

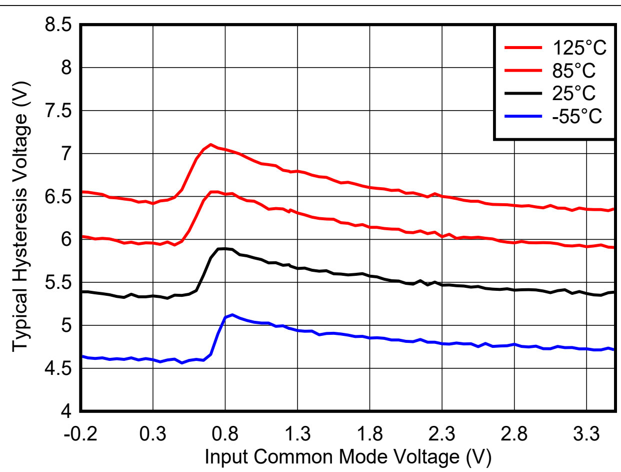


図 6-40. Hysteresis Voltage vs. Common Mode, 3.3V

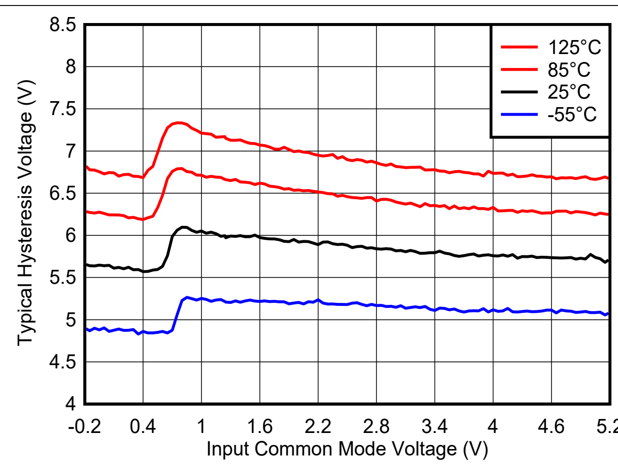


図 6-41. Hysteresis Voltage vs. Common Mode, 5V

6.11 Typical Characteristics - TLV3012-EP (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

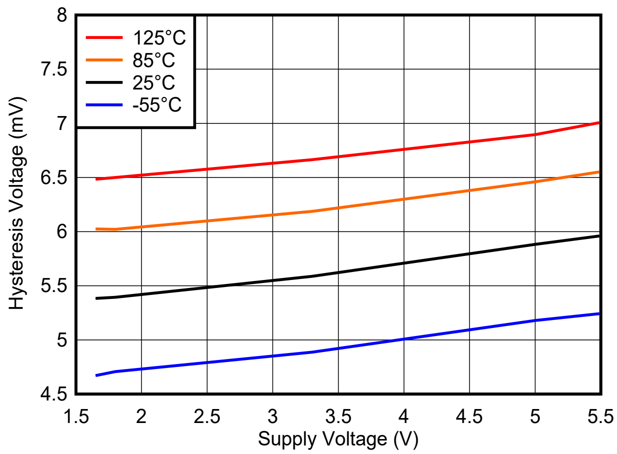


図 6-42. Hysteresis Voltage vs. Supply Voltage

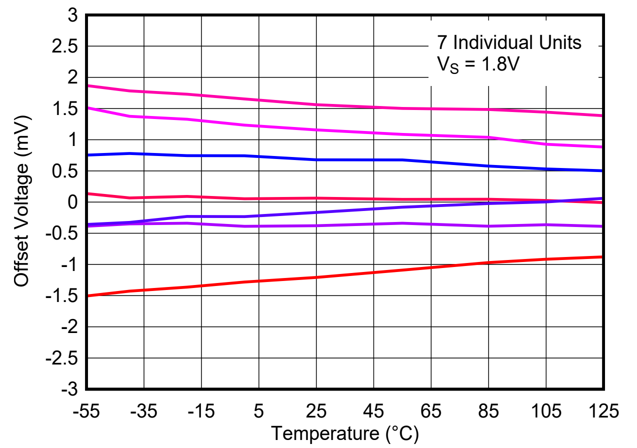


図 6-43. Offset Voltage vs. Temperature, 1.8 V

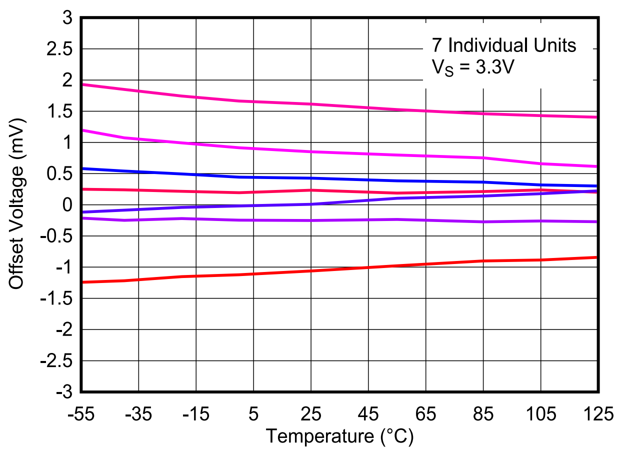


図 6-44. Offset Voltage vs. Temperature, 3.3 V

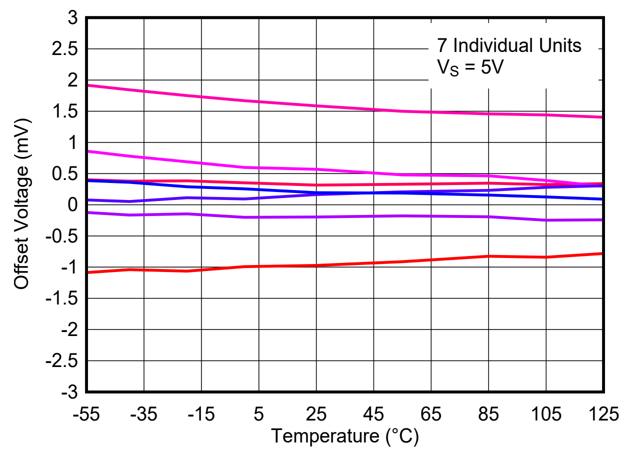


図 6-45. Offset Voltage vs. Temperature, 5 V

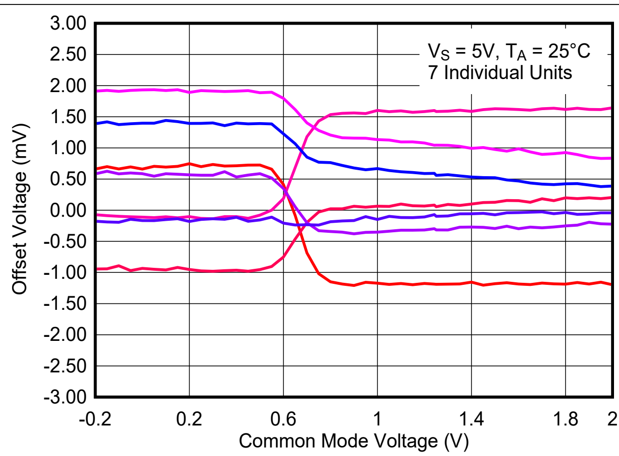


図 6-46. Offset Voltage vs. Common Mode Voltage, 1.8 V

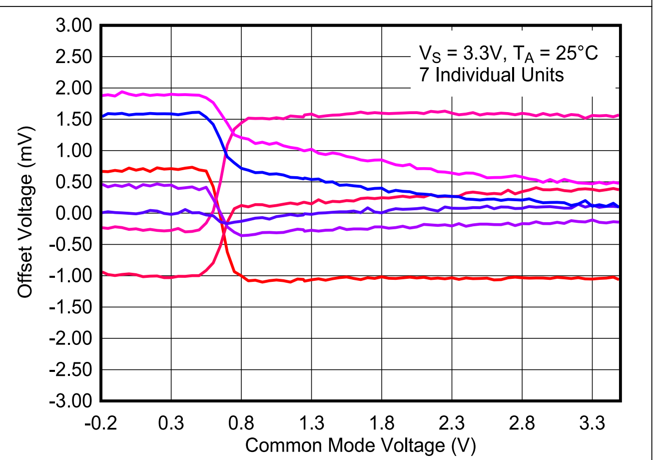


図 6-47. Offset Voltage vs. Common Mode Voltage, 3.3 V

6.11 Typical Characteristics - TLV3012-EP (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

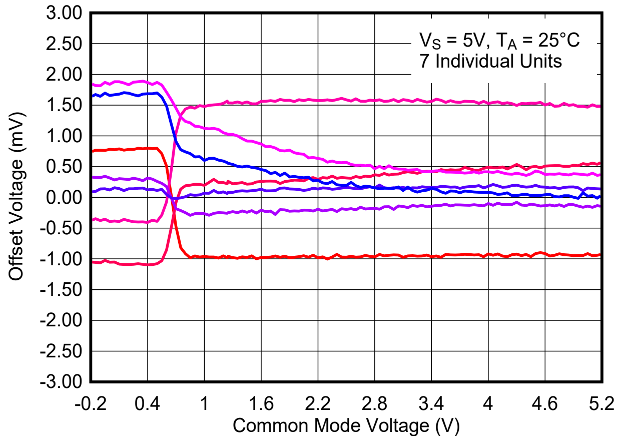


図 6-48. Offset Voltage vs. Common Mode Voltage, 5 V

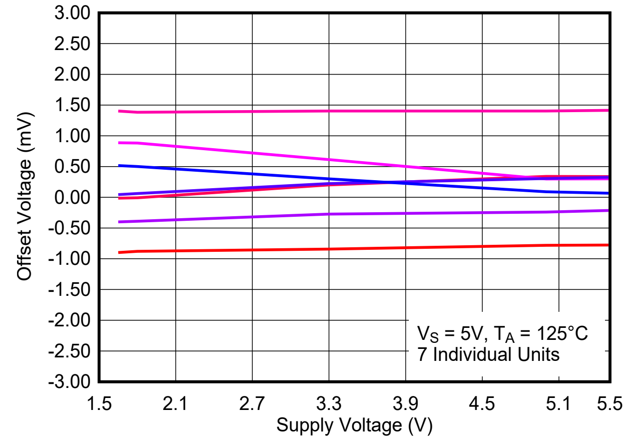


図 6-49. Offset Voltage vs. Supply Voltage, 125°C

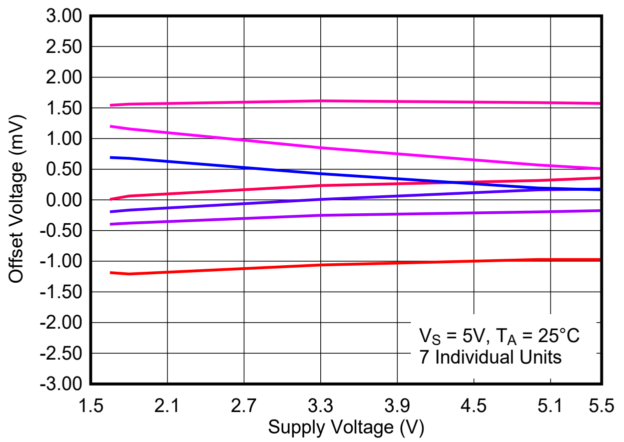


図 6-50. Offset Voltage vs. Supply Voltage, 25°C

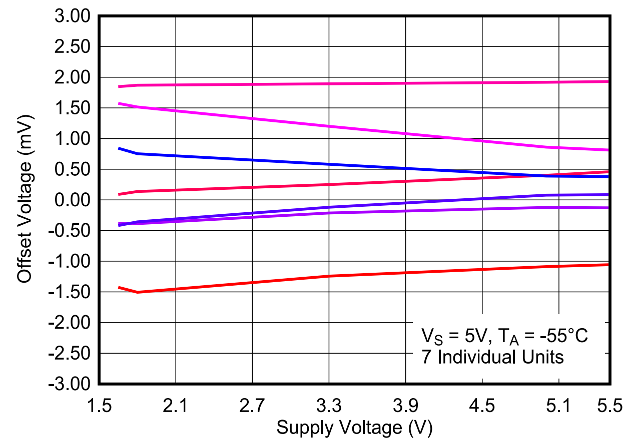


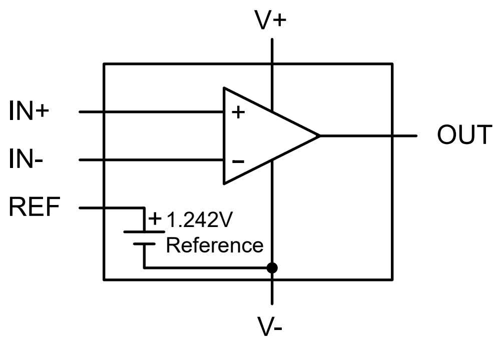
図 6-51. Offset Voltage vs. Supply Voltage, -55°C

7 Detailed Description

7.1 Overview

The TLV301x-EP is a MicroPower comparator with an integrated reference that is well suited for compact, low-current, precision voltage detection applications. With a high-accuracy, internal reference of 1.242 V and 5 uA of quiescent current, the TLV301x-EP enables power conscious systems to monitor and respond quickly to fault conditions.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV301x-EP is comprised of a rail-to-rail input comparator with open-drain or push-pull output options and a voltage reference that is externally available.

7.4 Device Functional Modes

The TLV3011-EP requires an operating voltage between 1.8 V and 5.5 V for the comparator output to reflect the voltage applied to the inputs. Similarly, the reference output (REF) will also be valid over the same operating voltage range.

7.4.1 Open Drain Output (TLV3011-EP)

The TLV3011-EP features an Open-Drain (sinking only) output that allows multiple devices to be driven by a single pull-up resistor to accomplish an OR function, making the TLV3011-EP useful for logic applications. The value of the pull-up resistor and supply voltage used will affect current consumption due to additional current drawn when the output is in a low state. This effect can be seen in the typical curve Quiescent Current vs Output Switching Frequency.

The pull-up voltage should NOT exceed the V+ suppply.

7.4.2 Push Pull Output (TLV3012-EP)

The TLV3012-EP has a "Push-Pull" output capable of both sinking and sourcing current. The push-pull output stage is optimal for reduced power budget applications by eliminating the need for a pull-up resistor and features no shoot-through current.

Do not tie push-pull outputs together.

7.4.3 Voltage Reference

The TLV301x-EP requires an operating voltage between 1.8 V and 5.5 V for the comparator output to reflect the voltage applied to the inputs. Similarly, the reference output (REF) will also be valid over the same operating voltage range.

The integrated 1.242-V voltage reference offers low 100-ppm/°C (maximum) drift provided on a seporate output pin that allows use of external dividers or to provide a reference voltage for other external circuitry. The reference is stable with up to a 10-nF capacitive load and can sink or source up to 500µA (typical) of output current.

7.4.4 Fail-Safe Input (TLV3012-EP Only)

This section does **NOT** apply to the open drain output TLV3011-EP.

The TLV3012-EP inputs are Fail-Safe up to 5.5V independent of V+ voltage. Fail-Safe is defined as maintaining the same high input impedance when V+ is unpowered or within the recommended operating ranges.

The Fail-Safe inputs can be any value between 0 V and 5.5 V, even while V+ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges.

This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct. The specified input voltage range is -0.2 V to (V+) + 0.2 V.

The following is a summary of the TLV3012-EP device input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output state is **indeterminate** (random). *Do not* operate in this region.

Because the inputs do not have upper ESD diode clamps to V+, input voltages must be externally clamped to below 5.5 V if the source could possibly exceed 5.5 V. A current limiting resistor in series with the input is also recommend in case of input transients.

7.4.5 Power-On Reset (POR) (TLV3012-EP Only)

This section does **NOT** apply to the open-drain output TLV3011-EP.

The TLV3012-EP has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for up to 1.9ms after the minimum supply voltage threshold is crossed, or immediately when the supply voltage drops below minimum supply. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}). This delay is long enough to allow the reference output to stabilize with up to a 10nF capacitive load.

During the POR period (t_{on}), the outputs will be low (sinking)

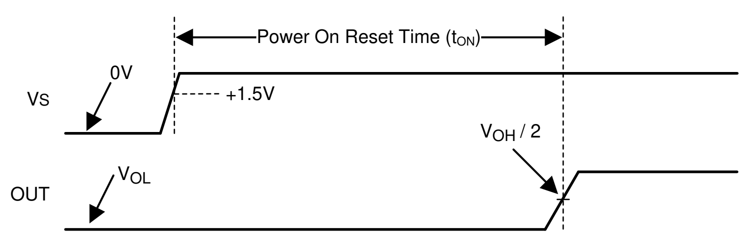


図 7-1. Power-On Reset Example Timing Diagram for TLV3012-EP

8 Application and Implementation

注

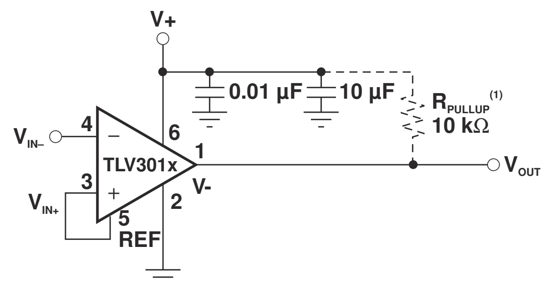
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV301x-EP comparator family with on-chip 1.242-V series reference with the choice of either open-drain or push-pull output stages.

A typical supply current of 2.8 µA and small packaging combine with 1.8-V supply requirements to make the TLV301x-EP devices optimal for battery and portable designs.

図 8-1 shows the typical connections for the TLV301x-EP device.



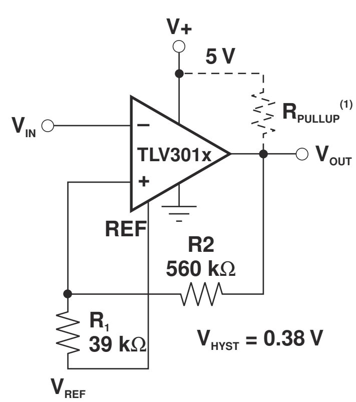
(1) Use R_{PULLUP} with the TLV3011 only.

図 8-1. Basic Connections of the TLV301x-EP

8.1.1 External Hysteresis

Comparator inputs have no noise immunity within the range of specified offset voltage (±12 mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV301x-EP is ±0.5 mV. To prevent multiple switching within the comparason threshold of the comparator, external hysteresis may be added by connecting a small amount of feedback to the positive input. 図 8-2 shows a typical topology used to introduce hysteresis, described by this equation:

$$V_{HYST} = \frac{V+ \times R1}{R1 + R2}$$



(1) Use R_{PULLUP} with the TLV3011 only.

図 8-2. Adding Hysteresis

V_{HYST} sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

8.2 Typical Application

8.2.1 Under Voltage Detection

Under-voltage detection is frequently required to alert the system that a battery voltage has dropped below the usable voltage level. 図 8-3 shows a simple under-voltage detection circuit using the TLV3012-EP which is configured as a non-inverting comparator with the integrated 1.242 V reference is externally connected to the inverting input pin (IN-).

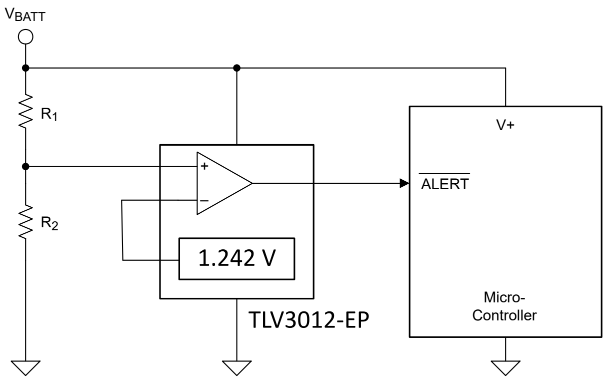


図 8-3. Under-Voltage Detection

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 8-3. Connect (V+) to V_{BAT} which also powers the microcontroller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0 V. When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses V_{REF}, the 1.242 V reference threshold of the TLV3012-EP. This causes the comparator output to transition from a logic high to a logic low. The push-pull output of the TLV3012-EP is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal.

式 1 is derived from the analysis of 図 8-3.

$$V_{REF} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \tag{1}$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to IN+
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{REF} is the falling edge threshold where the comparator output changes state from high to low

Rearranging 式 1 and solving for R_1 yields 式 2.

$$R_1 = \frac{(V_{BAT} - V_{REF})}{V_{REF}} \times R_2 \quad (2)$$

For the specific undervoltage detection of 2.0 V using the TLV3012-Q1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.242)}{1.242} \times 1M = 610\ k\Omega \quad (3)$$

where:

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{REF} is set to1.242 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

8.2.1.3 Application Performance Plots

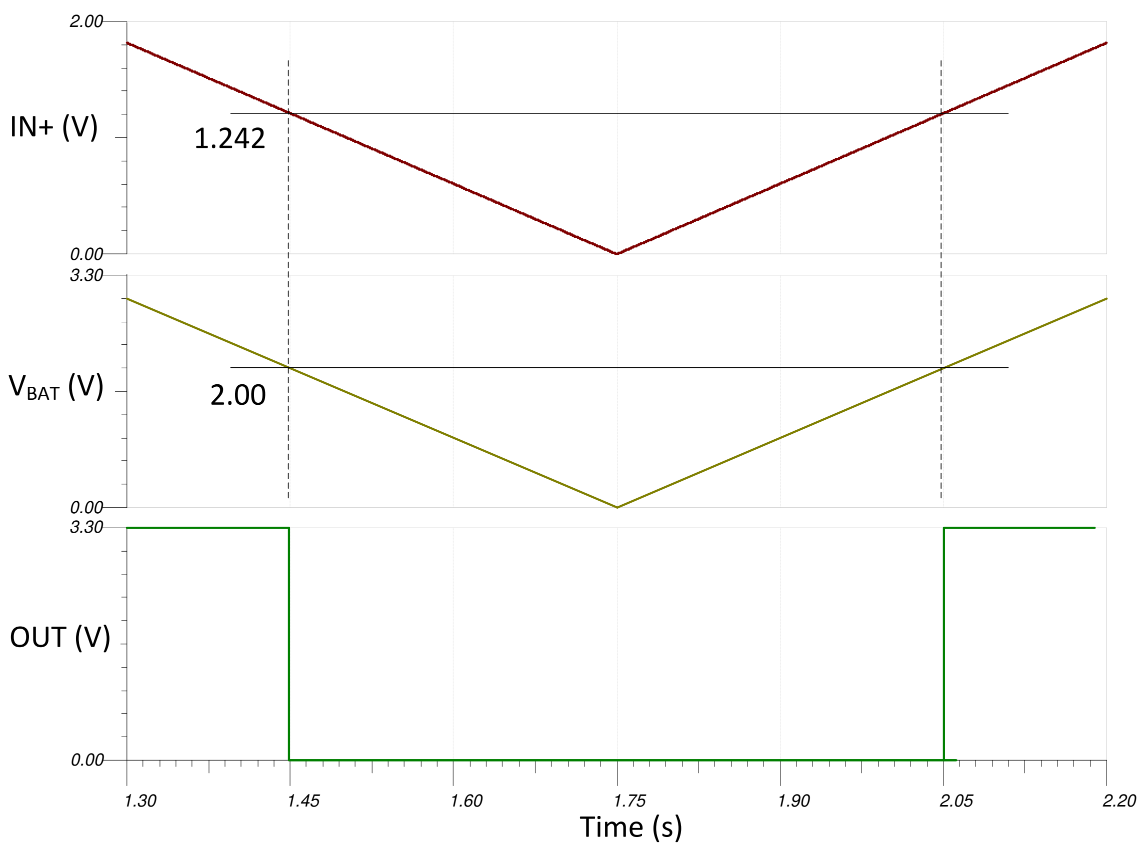


図 8-4.

8.3 Power Supply Recommendations

The TLV3012x-EP has a recommended operating voltage range (V_S) of 1.8 V to 5.5 V. V_S is defined as (V+) – (V-).

Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S.

However, when bipolar supply voltages are used, it is important to realize that the reference (REF) and logic low level of the comparator output is referenced to (V-). Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current in the EC Table.

8.4 Layout

8.4.1 Layout Guidelines

To minimize supply noise, power supplies should be capacitively decoupled by a 0.1-µF ceramic capacitor. Comparators are sensitive to input noise and precautions such as proper grounding (use of ground plane), supply bypassing, and guarding of high-impedance nodes minimize the effects of noise and help to ensure specified performance.

8.4.2 Layout Example

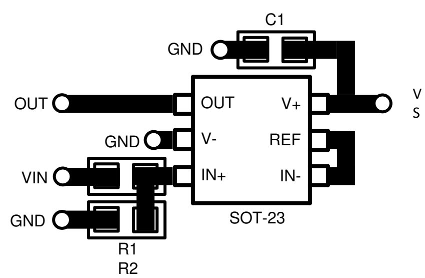


図 8-5. Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3011AMDBVREP	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTV	Samples
TLV3012AMDBVREP	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2QDF	Samples
V62/07604-01XE	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTV	Samples
V62/23603-01XE	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2QDF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3011-EP, TLV3012-EP :

- Catalog : TLV3011, TLV3012

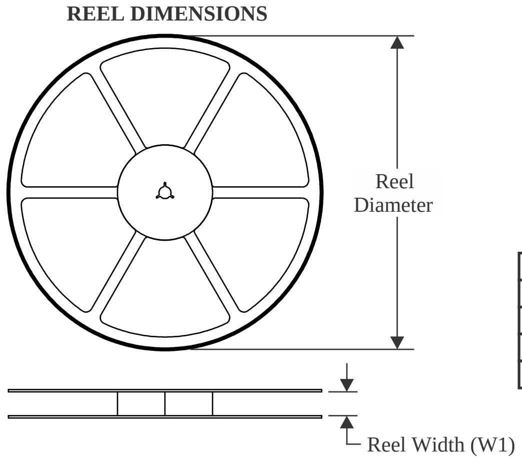
- Automotive : TLV3011-Q1, TLV3012-Q1

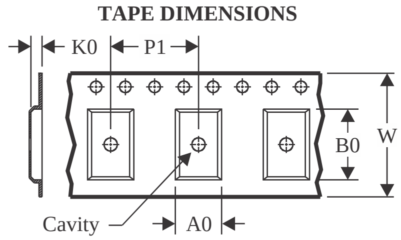
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

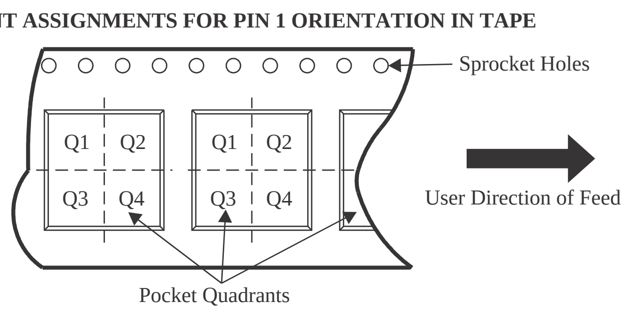
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





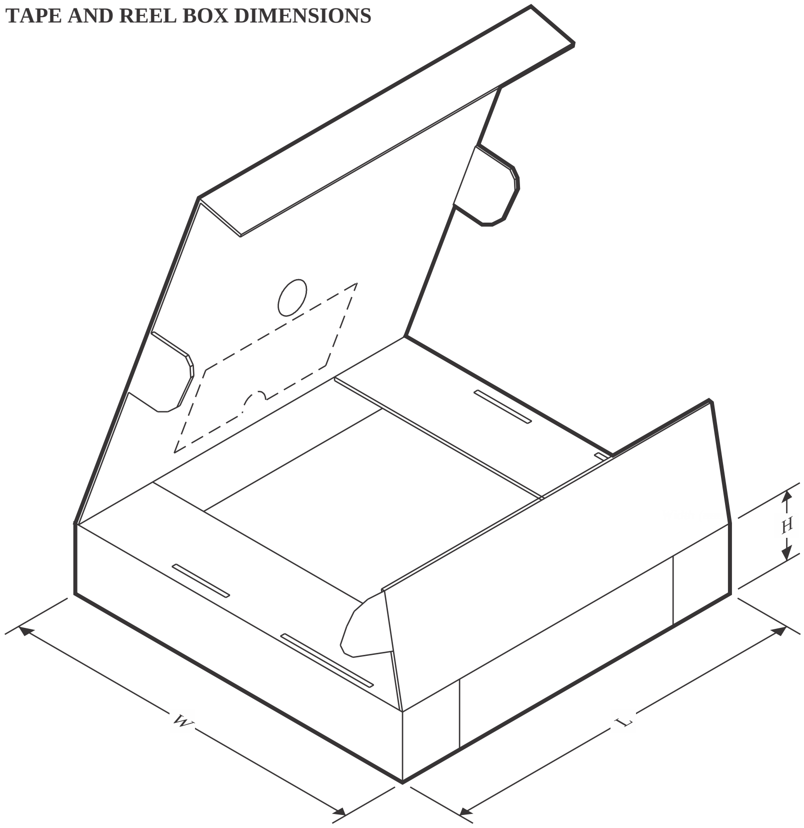
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

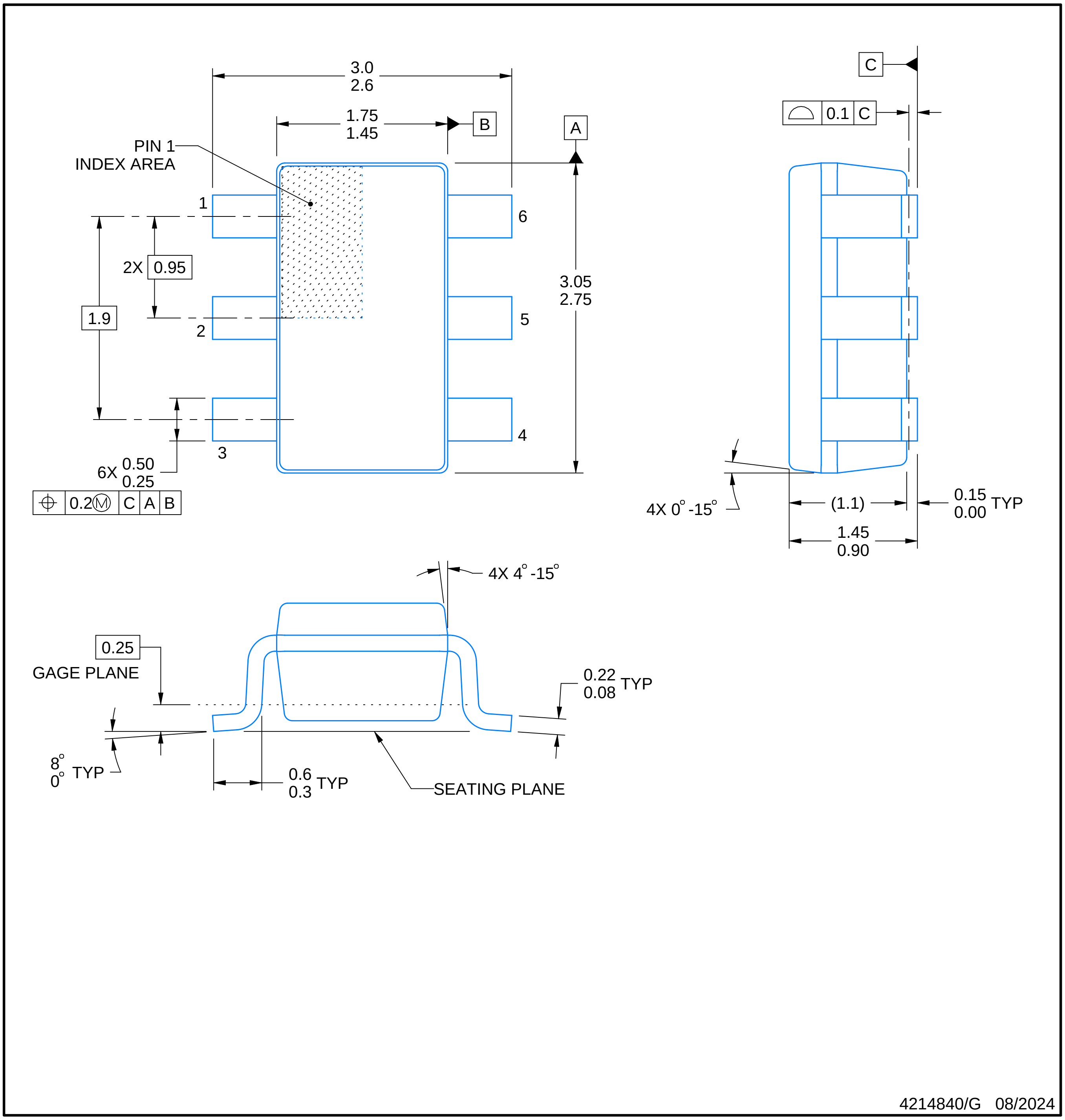
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3011AMDBVREP	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3012AMDBVREP	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



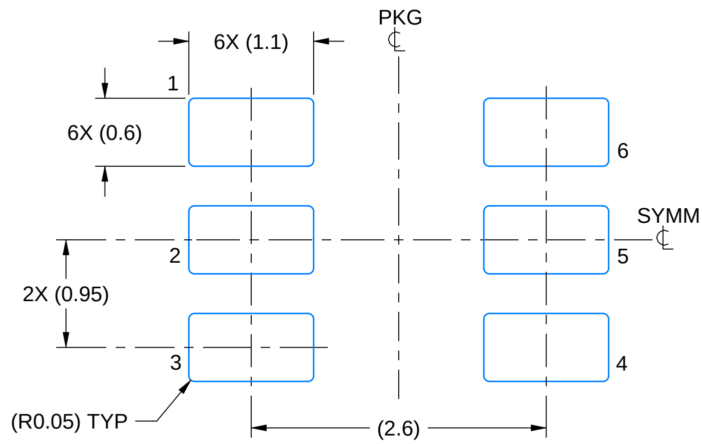
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3011AMDBVREP	SOT-23	DBV	6	3000	200.0	183.0	25.0
TLV3012AMDBVREP	SOT-23	DBV	6	3000	210.0	185.0	35.0

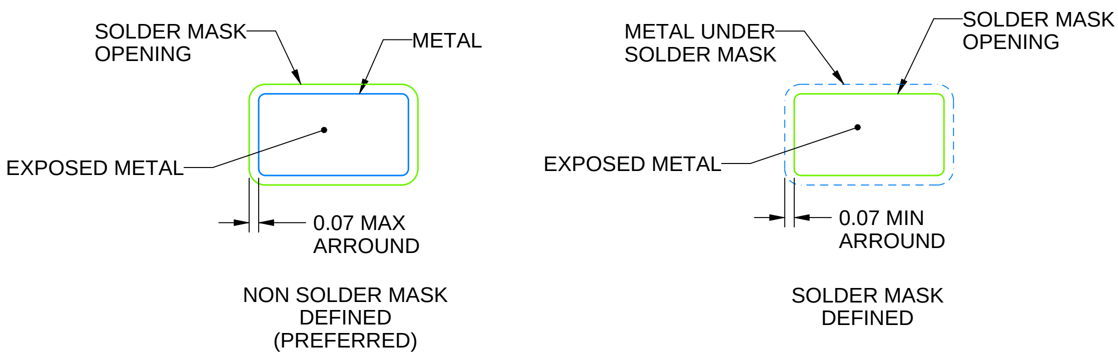


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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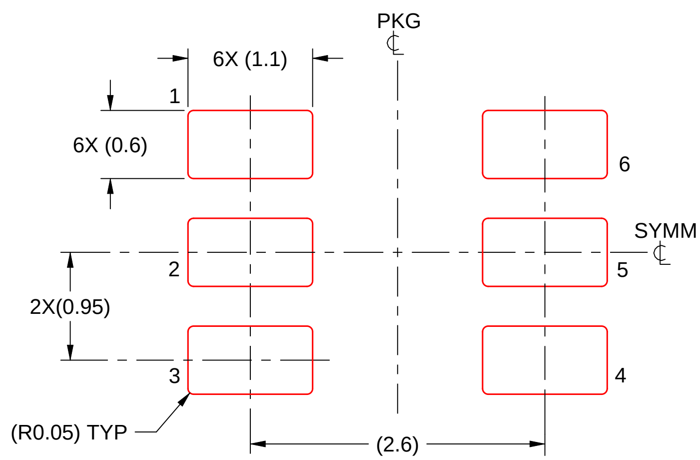
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

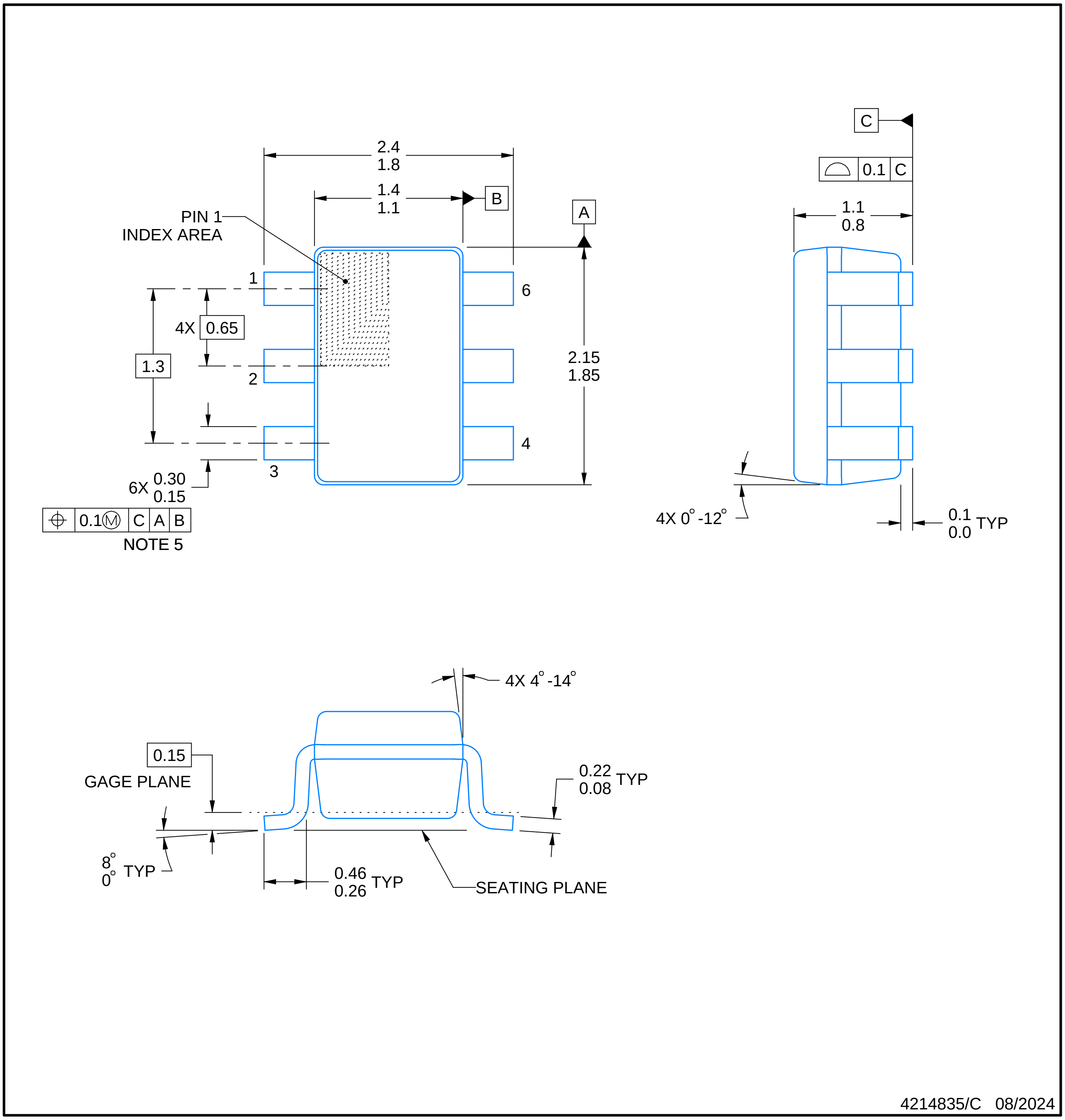


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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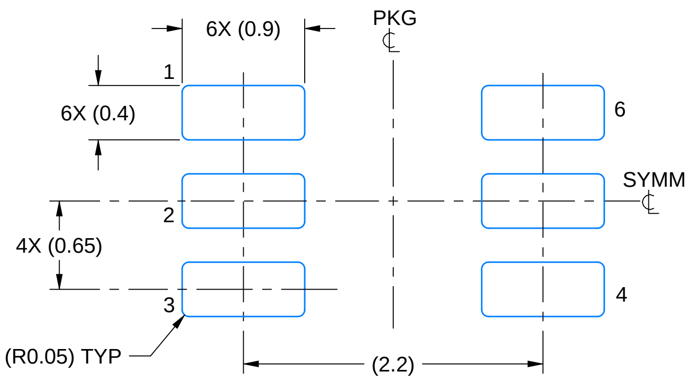
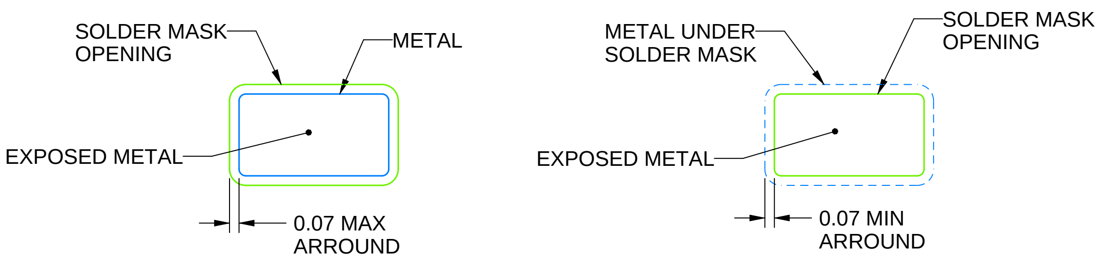
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK DEFINED (PREFERRED)

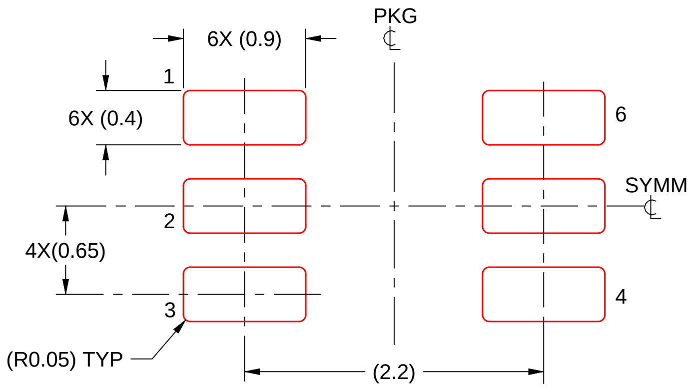
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項