TLV354x 200MHz、 レール・ツー・レールI/O、コスト制限の厳しいシステム向けのCMOSオペアンプ

1 特長

- 低コストのシステム用の広帯域アンプ
- ユニティ・ゲイン帯域幅: 200MHz
- 高いスルー・レート: 150V/μs
- 低ノイズ: 7.5nV/√Hz
- レール・ツー・レールI/O
- 高い出力電流: 100mA超
- 非常に優れたビデオ性能
  - 差動ゲイン: 0.02%、差動位相: 0.09°
  - 0.1dBのゲイン・フラットネス(40MHz)
- 低い入力バイアス電流: 3pA
- 静止電流: 5.2mA
- サーマル・シャットダウン
- 電源電圧範囲: 2.5V～5.5V

2 アプリケーション

- 高分解能のADCドライバ・アンプ
- IRタッチ
- 低電圧、高周波数の信号処理
- ビデオ処理
- トランシーバ基地局
- 光ネットワーク、調節可能なレーザー
- フォトダイオード・トランスインピーダンス・アンプ
- バーコード・スキャナ
- 高速電流センス・アンプ
- 超音波イメージング

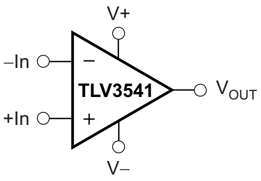


図 1. 概略回路図

3 概要

TLV3541、TLV3542、TLV3544はシングル、デュアル、クワッド・チャネルで低消費電力(チャネルごとに5.2mA)、高速、ユニティ・ゲイン安定、レール・ツー・レール入力/出力のオペアンプであり、広い帯域幅を必要とするビデオやその他のアプリケーション用に設計されています。

これらのデバイスは、電源からわずか6.5mA (最大値)の電流しか消費せず、200MHzのゲイン帯域幅積、150V/μsのスルー・レート、およびf = 1MHzにおいて7.5 nV/√Hzの低い入力ノイズを実現しています。高帯域幅、高いスルー・レート、低いノイズを併せ持つため、TLV354xファミリは低電圧、高速の信号コンディショニング・システムに適しています。

TLV354xシリーズのオペアンプは、最低2.5V (±1.25V)、最高5.5V (±2.75V)のシングルまたはデュアル電源で動作するよう最適化されています。同相入力範囲は電源の範囲よりも拡大されています。出力スイングはレールから100mV以内で、広いダイナミックレンジに対応しています。

TLV354xデバイスは、-40℃～+125℃での動作が規定されています。TLV354xファミリは、市販されている多くの広帯域オペアンプのプラグイン代替品として使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV3541	SOIC (8)	3.91mm×4.90mm
	SOT-23 (5)	2.90mm×1.60mm
TLV3542	SOIC (8)	3.91mm×4.90mm
	VSSOP (8)	3.00mm×3.00mm
TLV3544	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

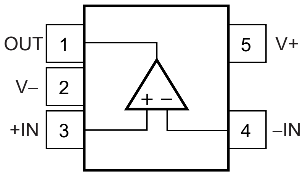
目次

4 改訂履歴

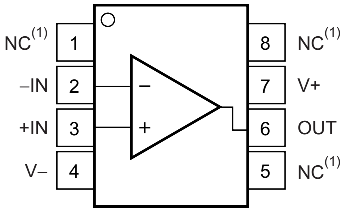
日付	改訂内容	注
2016年10月	*	初版

5 Pin Configuration and Functions

TLV3541: DBV Package
5-Pin SOT-23
Top View



TLV3541: D Package
8-Pin SOIC
Top View

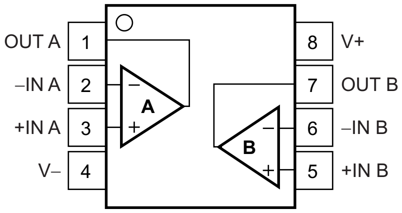


(1) NC means no internal connection.

Pin Functions: TLV3541

PIN			I/O	DESCRIPTION
NAME	**DBV (SOT-23)**	**D (SOIC)**		
–IN	4	2	I	Inverting input
+IN	3	3	I	Noninverting input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) supply
V+	5	7	—	Positive (highest) supply

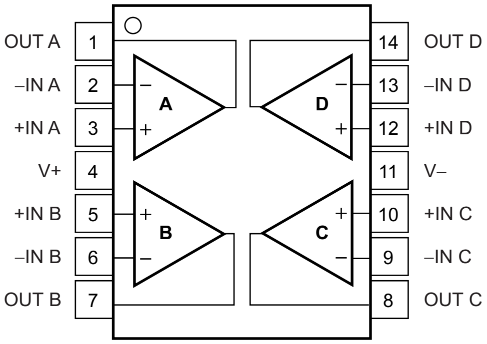
TLV3542: DGK and D Packages
8-Pin VSSOP, SOIC
Top View



Pin Functions: TLV3542

PIN		I/O	DESCRIPTION
NAME	**NO.**		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply

TLV3544: D and PW Packages
14-Pin SOIC, TSSOP
Top View



Pin Functions: TLV3544

PIN			I/O	DESCRIPTION
NAME	TLV3544			
	D (SOIC)	PW (TSSOP)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	9	9	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) supply
V+	4	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V−		7.5	V
	Signal input terminals(2)	(V–) – (0.5)	(V+) + 0.5	V
Current	Signal input terminals(2)	–10	10	mA
	Output short circuit(3)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J	–65	150	°C
	Storage, T_{stg}		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V– to V+	2.5		5.5	V
	Specified temperature range	–40		125	°C

6.4 Thermal Information: TLV3541

THERMAL METRIC[1]		TLV3541		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.8	216.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.7	84.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.5	43.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.0	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.0	42.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Thermal Information: TLV3542

THERMAL METRIC[1]		TLV3542		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.9	175.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.4	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.1	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.1	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.6	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.6 Thermal Information: TLV3544

THERMAL METRIC[1]		TLV3544		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.7 Electrical Characteristics: V_S = 2.7 V to 5.5 V Single-Supply

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V, at T_A = 25°C		±2	±10	mV
dV_{OS}/dT	Input offset voltage vs temperature	V_S = 5 V, at T_A = −40°C to +125°C		±4.5		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 5.5 V, V_{CM} = (V_S / 2) − 0.55 V	60	70		dB
INPUT BIAS CURRENT						
I_B	Input bias current			3		pA
I_{OS}	Input offset current			±1		pA
NOISE						
e_n	Input voltage noise density	f = 1 MHz		7.5		nV/√Hz
i_n	Current noise density	f = 1 MHz		50		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, –0.1 V < V_{CM} < 3.5 V, at T_A = 25°C	66	80		dB
		V_S = 5.5 V, –0.1 V < V_{CM} < 5.6 V, at T_A = 25°C	56	68		dB
INPUT IMPEDANCE						
	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = 5 V, 0.3 V < V_O < 4.7 V, at T_A = 25°C	92	108		dB
FREQUENCY RESPONSE						
$f_{–3dB}$	Small-signal bandwidth	At G = +1, V_O = 10 mV R_F = 25 Ω		200		MHz
		At G = +2, V_O = 10 mV		90		MHz
GBW	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness	At G = +2, V_O = 10 mV		40		MHz
SR	Slew rate	V_S = 5 V, G = +1, 4-V step		150		V / µs
		V_S = 5 V, G = +1, 2-V step		130		V / µs
	Rise-and-fall time	At G = +1, V_O = 200 mV_{PP}, 10% to 90%		2		ns
		At G = +1, V_O = 2 V_{PP}, 10% to 90%		11		ns
	Settling time	0.1%, V_S = 5 V, G = +1, 2-V output step		30		ns
		0.01%, V_S = 5 V, G = +1, 2-V output step		60		ns
	Overload recovery time	V_{IN} × Gain = V_S		5		ns

Electrical Characteristics: V_S = 2.7 V to 5.5 V Single-Supply (continued)

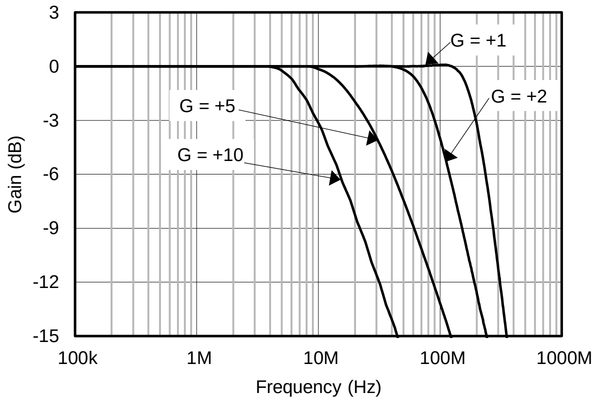
at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE, continued							
	Harmonic distortion	Second harmonic	At G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–75		dBc
		Third harmonic	At G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–83		dBc
	Differential gain error		NTSC, R_L = 150 Ω		0.02%		
	Differential phase error		NTSC, R_L = 150 Ω		0.09		°
	Channel-to-channel crosstalk	TLV3542	f = 5 MHz		–100		dB
		TLV3544			–84		dB
OUTPUT							
	Voltage output swing from rail		V_S = 5 V, R_L = 1 kΩ at T_A = 25°C		0.1	0.3	V
I_O	Output current, single, dual, quad (1)(2)		V_S = 5 V	100			mA
			V_S = 3 V		50		mA
	Closed-loop output impedance		f < 100 kHz		0.05		Ω
R_O	Open-loop output resistance				35		Ω
POWER SUPPLY							
V_S	Specified voltage range			2.7		5.5	V
	Operating voltage range			2.5		5.5	V
I_Q	Quiescent current (per amplifier)		At T_A = 25°C, V_S = 5 V, I_O = 0		5.2	6.5	mA
TEMPERATURE RANGE							
	Specified range			–40		125	°C
	Operating range (3)			–55		150	°C
	Storage range			–65		150	°C
THERMAL SHUTDOWN							
	Shutdown temperature				160		°C
	Reset from shutdown				140		°C

(1) See typical characteristic curves, *Output Voltage Swing vs Output Current* (図 14 and 図 15).
(2) Specified by design.
(3) Operating in this temperature range will not damage the part. However, degraded performance may be observed.

6.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, unless otherwise noted.



R_F = 604 Ω V_O = 10 mV_{pp}

図 2. Noninverting Small-Signal Frequency Response

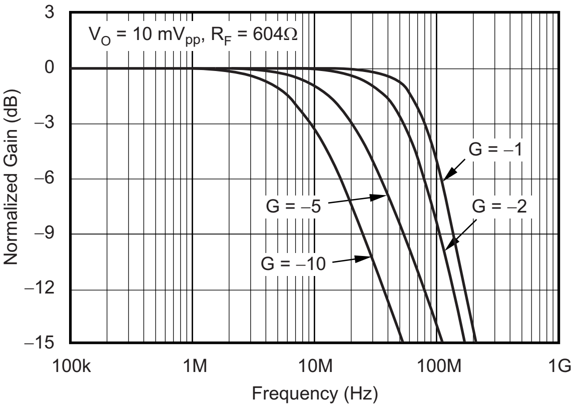


図 3. Inverting Small-Signal Frequency Response

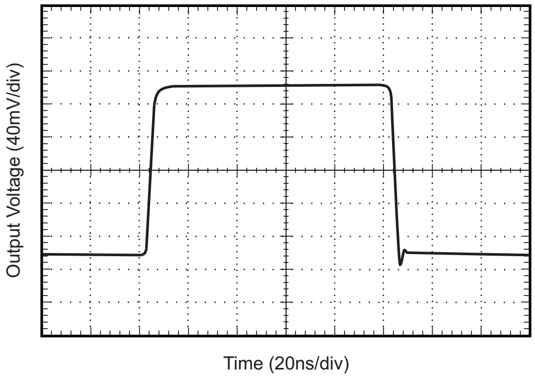


図 4. Noninverting Small-Signal Step Response

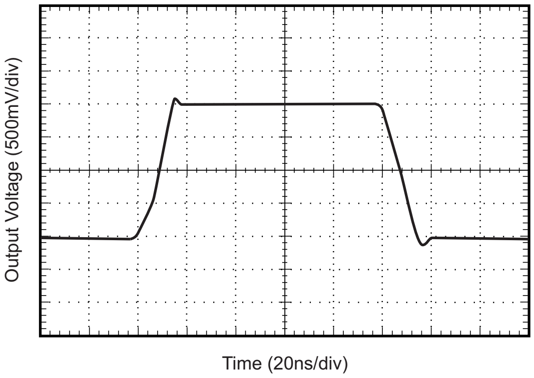
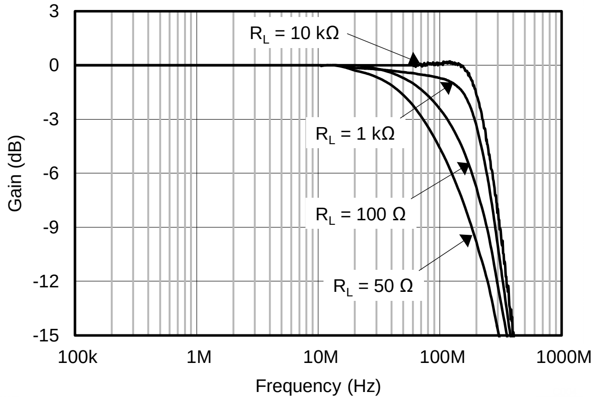
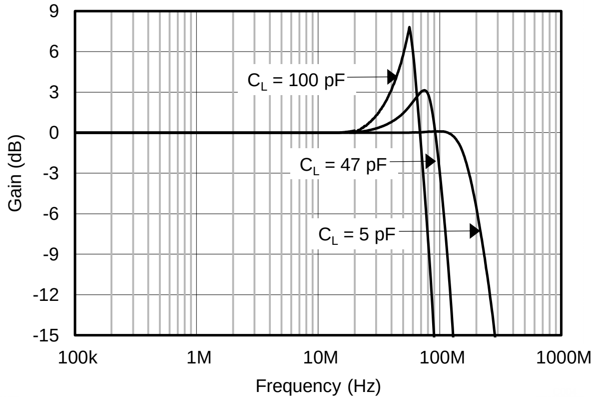


図 5. Noninverting Large-Signal Step Response



G = +1, R_F = 0 Ω V_O = 10 mV_{pp} C_L = 0 pF

図 6. Frequency Response for Various R_L



G = +1, R_S = 0 Ω V_O = 10 mV_{pp}

図 7. Frequency Response for Various C_L

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, unless otherwise noted.

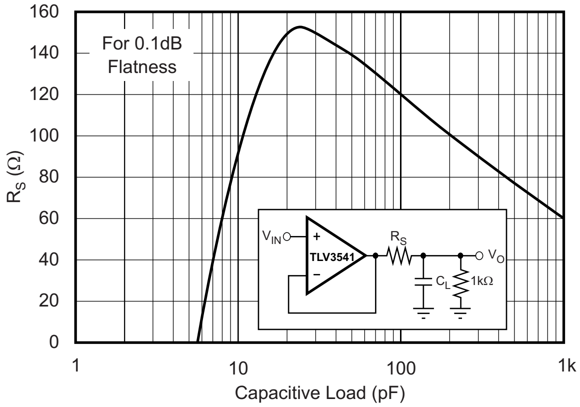
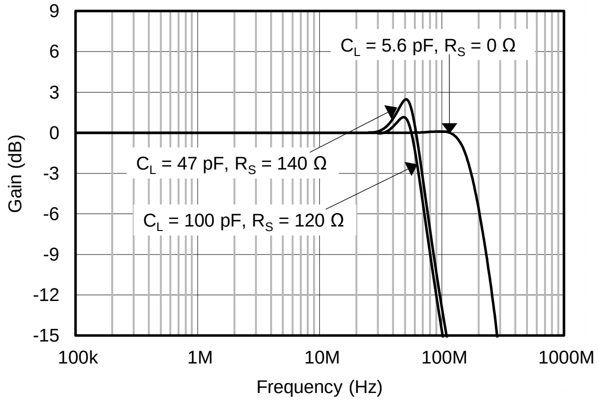


図 8. Recommended R_S vs Capacitive Load



G = +1, V_O = 10 mV_{pp}

図 9. Frequency Response vs Capacitive Load

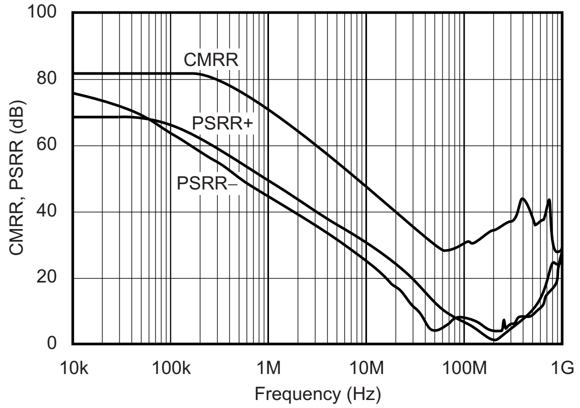


図 10. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

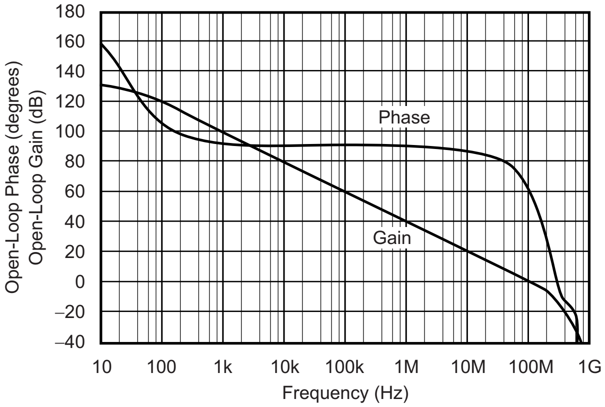


図 11. Open-Loop Gain and Phase

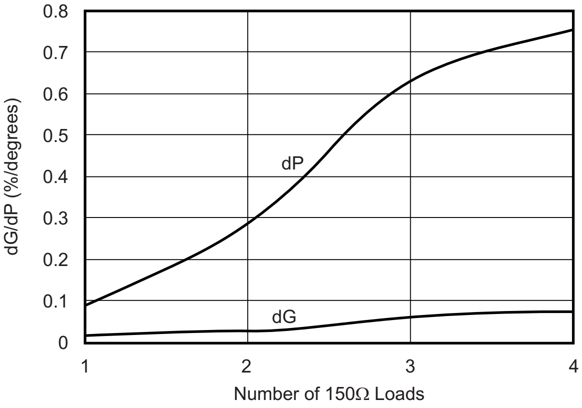


図 12. Composite Video Differential Gain and Phase

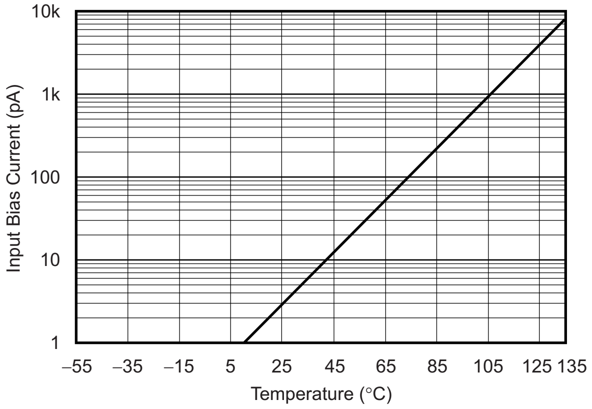


図 13. Input Bias Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, unless otherwise noted.

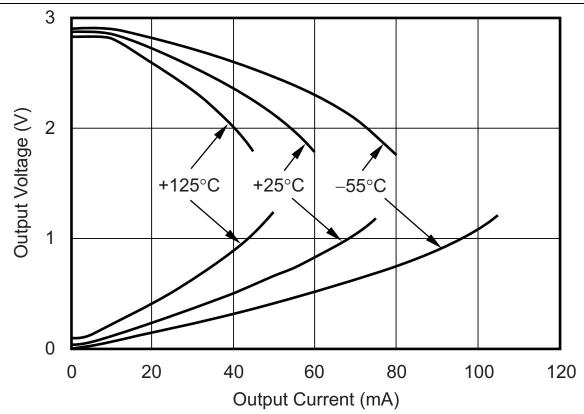


図 14. Output Voltage Swing vs Output Current for V_S = 3 V

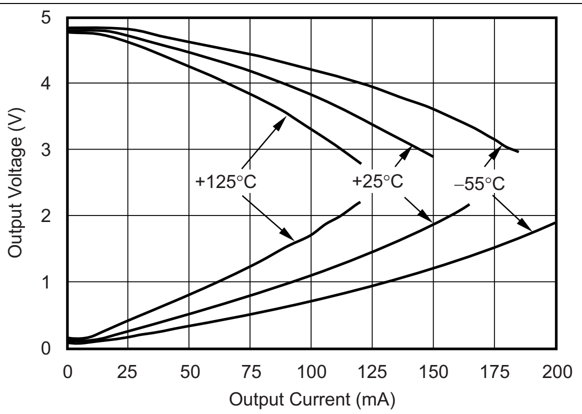


図 15. Output Voltage Swing vs Output Current for V_S = 5 V

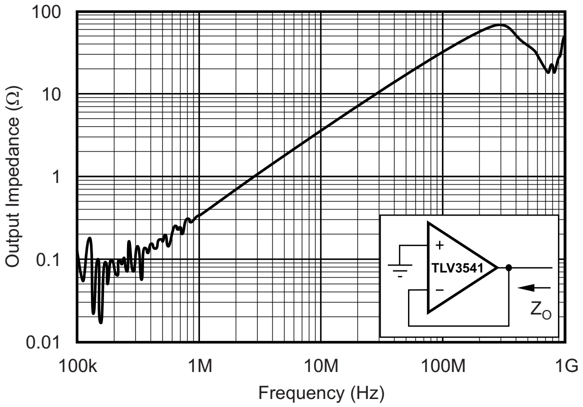


図 16. Closed-Loop Output Impedance vs Frequency

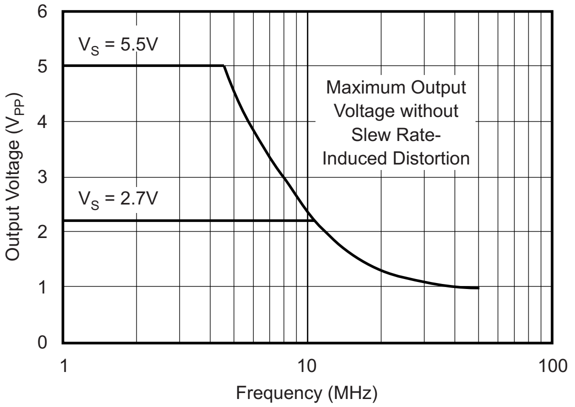


図 17. Maximum Output Voltage vs Frequency

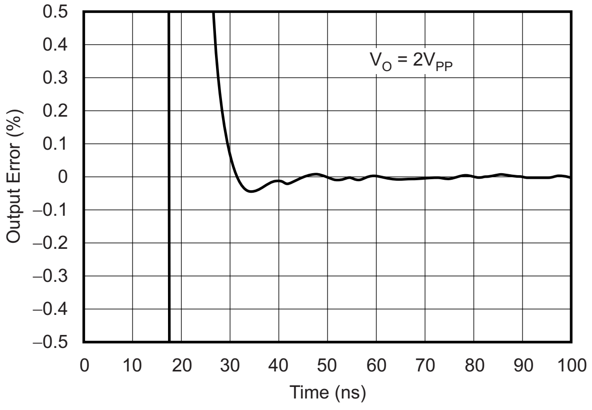


図 18. Output Settling Time to 0.1%

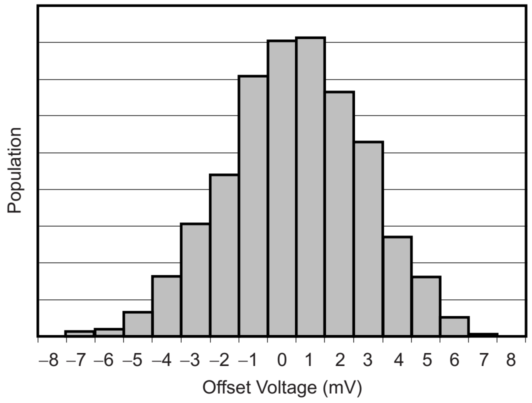


図 19. Offset Voltage Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, unless otherwise noted.

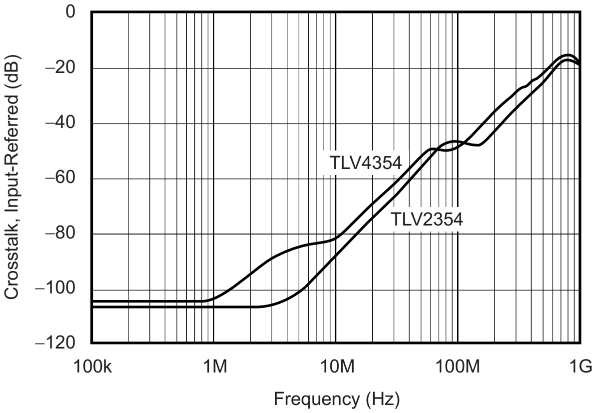


図 20. Channel-to-Channel Crosstalk

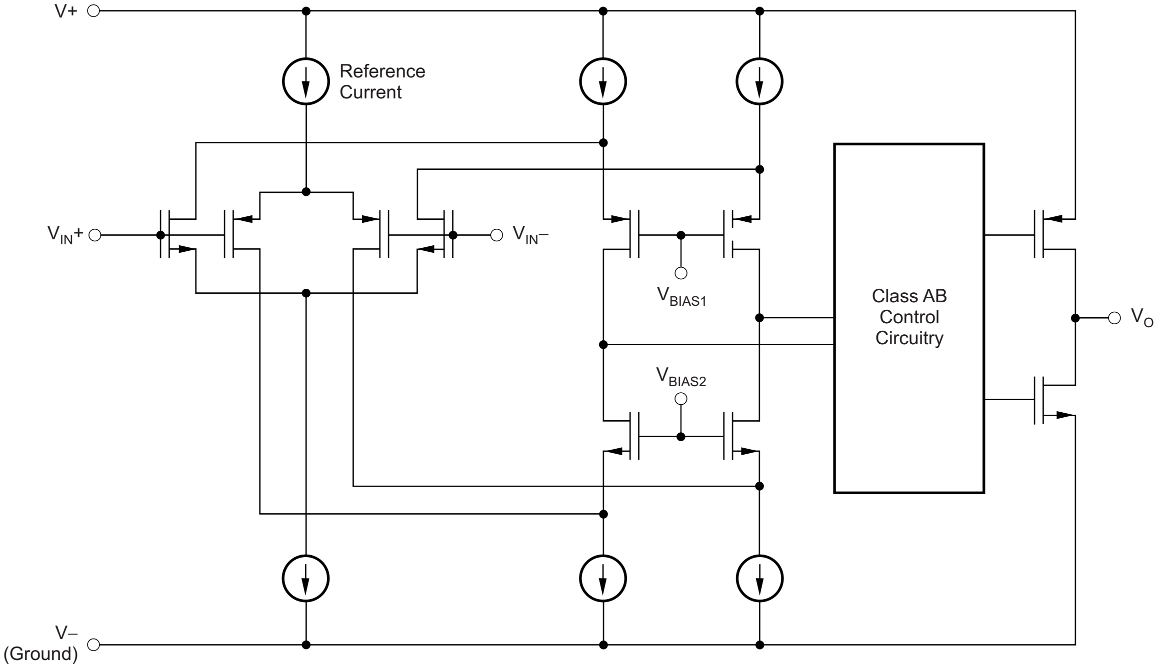
7 Detailed Description

7.1 Overview

The TLV354x is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The device is available as a single, dual, or quad op amp.

The amplifier features a 100-MHz gain bandwidth and a 150-V/µs slew rate, but the amplifier is unity-gain stable and operates as a +1-V/V voltage follower.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV354x is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section.

7.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the TLV354x extends 100 mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) − 1.2 V. There is a small transition region, typically (V+) − 1.5 V to (V+) − 0.9 V, in which both pairs are on. This 600-mV transition region can vary ±500 mV with process variation. Thus, the transition region (with both input stages on) can range from (V+) − 2.0 V to (V+) − 1.5 V on the low end, up to (V+) − 0.9 V to (V+) − 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

7.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing can be achieved while maintaining high open-loop gain. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (図 14 and 図 15).

7.3.4 Output Drive

The TLV354x output stage can supply a continuous output current of ±100 mA and yet provide approximately 2.7 V of output swing on a 5-V supply, as shown in 図 21. For maximum reliability, it is not recommended to run a continuous DC current in excess of ±100 mA. Refer to the typical characteristic curves, *Output Voltage Swing vs Output Current* (図 14 and 図 15). For supplying continuous output currents greater than ±100 mA, the TLV354x may be operated in parallel, as shown in 図 22.

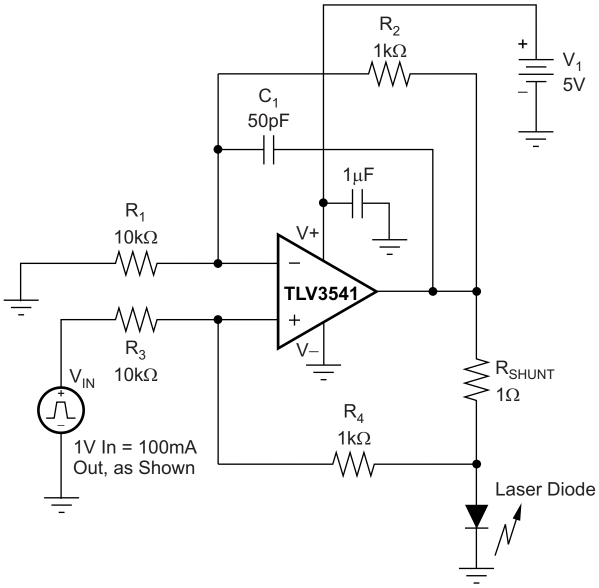


図 21. Laser Diode Driver

Feature Description (continued)

The TLV354x provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the TLV354x from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below +140°C.

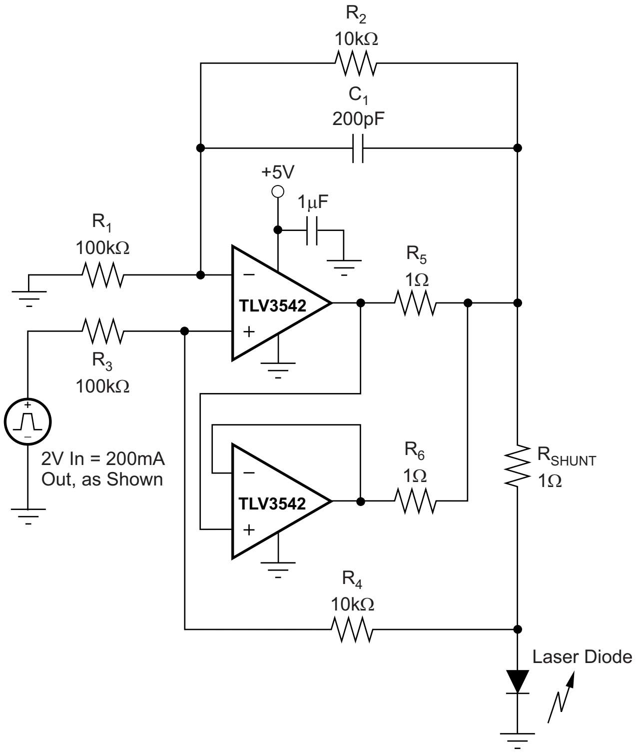


図 22. Parallel Operation

7.3.5 Video

The TLV354x output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in 図 23. By back-terminating a transmission line, the device does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the device presents a 150-Ω resistive load to the TLV354x output.

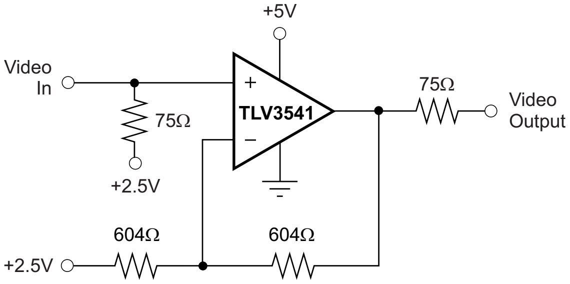
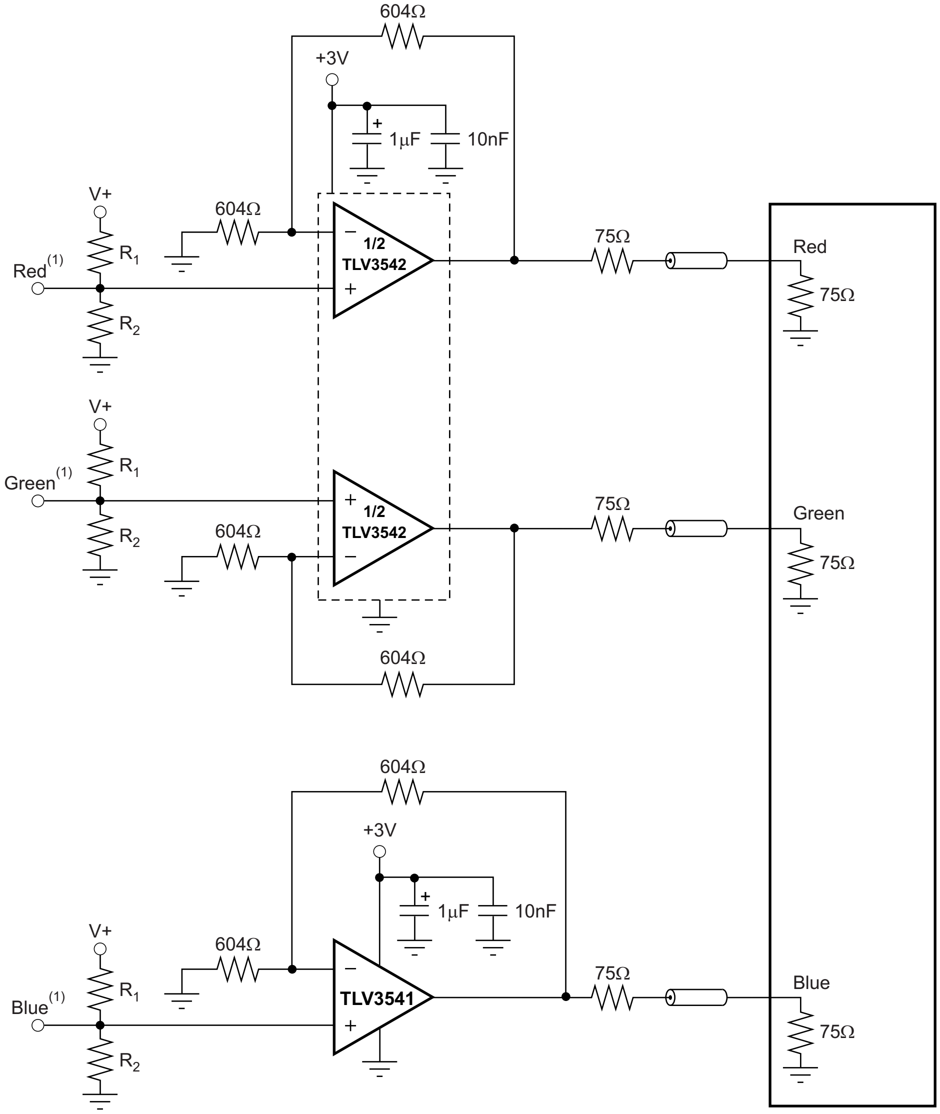


図 23. Single-Supply Video Line Driver

The TLV3542 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See 図 24.

Feature Description (continued)



(1) Source video signal offsets 300 mV above ground to accommodate op amp swing−to−ground capability.

図 24. RGB Cable Driver

Feature Description (continued)

7.3.6 Driving Analog-to-Digital Converters

The TLV354x series op amps offer 60 ns of settling time to 0.01%, making them a good choice for driving high- and medium-speed sampling A/D converters and buffering reference circuits. The TLV354x series provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, TI recommends using the OPA350 series.

図 25 illustrates the TLV3541 driving an A/D converter. With the TLV3541 in an inverting configuration, a capacitor across the feedback resistor can filter high-frequency noise in the signal.

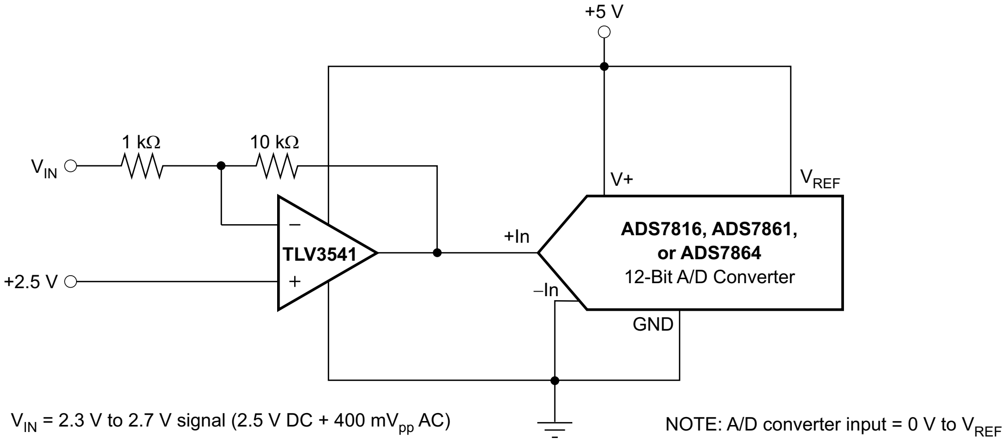


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図 25. The TLV3541 in Inverting Configuration Driving the ADS7816

7.3.7 Capacitive Load and Stability

The TLV354x series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. Refer to the typical characteristic curve, *Frequency Response for Various* C_L (図 7) for details.

The TLV354x topology enhances the ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. Refer to the typical characteristic curves, *Recommended* R_S *vs Capacitive Load* (図 8) and *Frequency Response vs Capacitive Load* (図 9) for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in 図 26. This configuration significantly reduces ringing with large capacitive loads. See the typical characteristic curve, *Frequency Response vs Capacitive Load* (図 9). However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is an error of approximately 0.2% at the output.

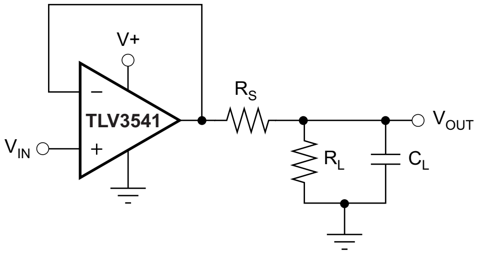


図 26. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

Feature Description (continued)

7.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, and low input voltage and current noise make the TLV354x a suitable wideband photodiode transimpedance amplifier for low-voltage, single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in 図 27, are the expected diode capacitance (including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the TLV354x), the desired transimpedance gain (R_F), and the Gain-Bandwidth Product (GBW) for the TLV354x (100 MHz, typical). With these three variables set, the feedback capacitor value (C_F) may be set to control the frequency response.

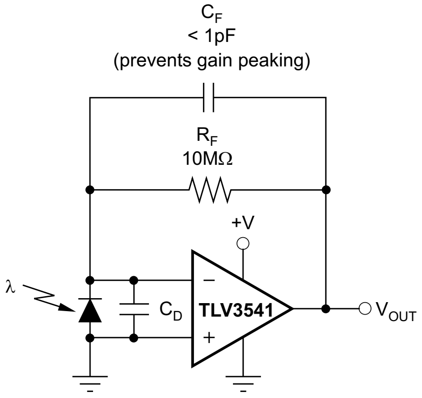


図 27. Transimpedance Amplifier

To achieve a flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in 式 1:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{1}$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by 式 2:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}}\ \text{Hz} \tag{2}$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200-MHz GBW) or the OPA655 (400-MHz GBW) may be used.

7.4 Device Functional Modes

The TLV354x has dual functional modes and is operational when the power-supply voltage is greater than 2.5 V (±1.25 V). The maximum power-supply voltage for the TLV354x is 5.5 V (±2.75 V). At +160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below +140°C.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV354x are wide bandwidth, low-noise, rail-to-rail input and output amplifiers. These devices operate from 2.5 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications The input common-mode voltage range includes both rails, and allows the TLV354x device to be used in any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving analog-to-digital converters (ADCs).

The TLV354x family of devices features a 200-MHz bandwidth and 150-V/µs slew rate with only 7.5 nV/√Hz of broadband noise.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in 図 28. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F.

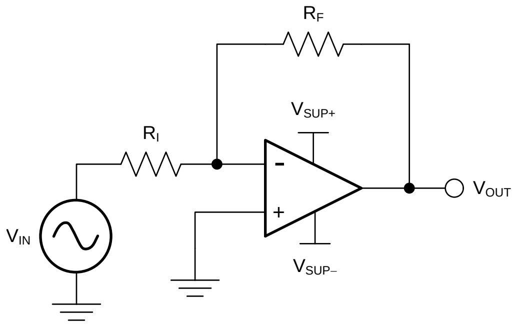


図 28. Application Schematic

8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using 式 3 and 式 4:

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{4}$$

Typical Application (continued)

When the desired gain is determined, select a value for R_I or R_F. Selecting a value in the kilo ohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that large resistors (100s of kilo ohms) draw the smallest current but generate the highest noise. Small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 kΩ for R_I, meaning 36 kΩ is used for R_F. These values are determined by 式 5:

$$A_V = -\frac{R_F}{R_I} \tag{5}$$

8.2.3 Application Curve

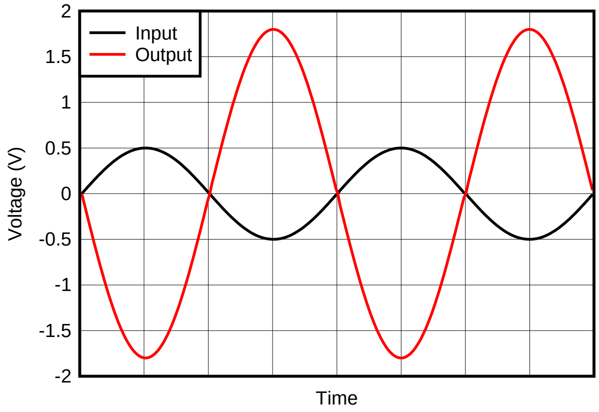
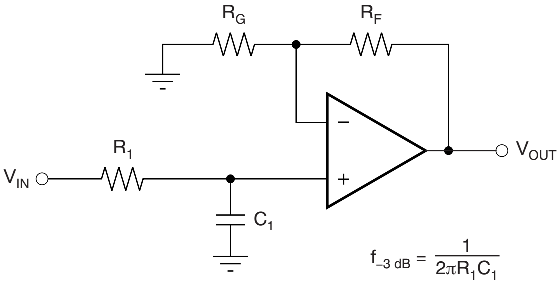


図 29. Inverting Amplifier Input and Output

8.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in 図 30.



$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

図 30. Single-Pole, Low-Pass Filter

System Examples (continued)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as shown in 図 31. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

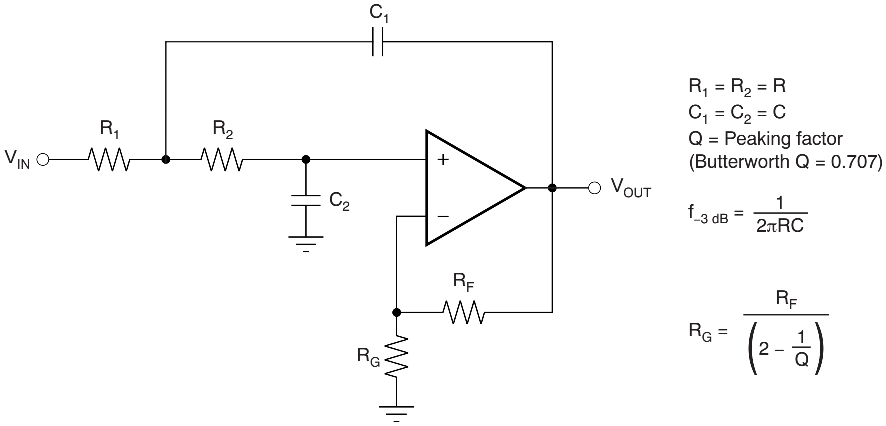


図 31. Two-Pole, Low-Pass, Sallen-Key Filter

9 Power Supply Recommendations

The TLV354x family is specified from 2.7 V to 5.5 V (±1.35 V to ±2.75 V), although the devices can operate from 2.5 V to 5.5 V (±1.25 V to ±2.75 V); many specifications apply from –40°C to +125°C. *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages larger than 7.5 V can permanently damage the device. (See the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

9.1 Input and ESD Protection

The TLV354x family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the *Absolute Maximum Ratings* table. 図 32 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input, which must be kept to a minimum in noise-sensitive applications.

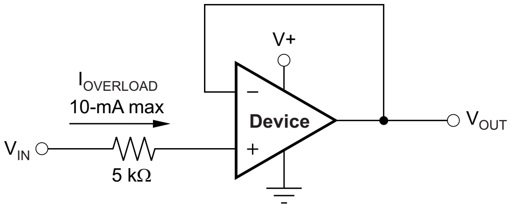


図 32. Input Current Protection

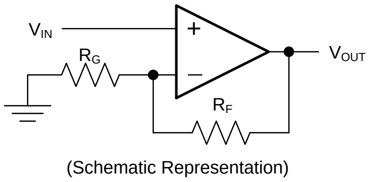
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise propagates into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input to minimize parasitic capacitance, as shown in 図 33.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



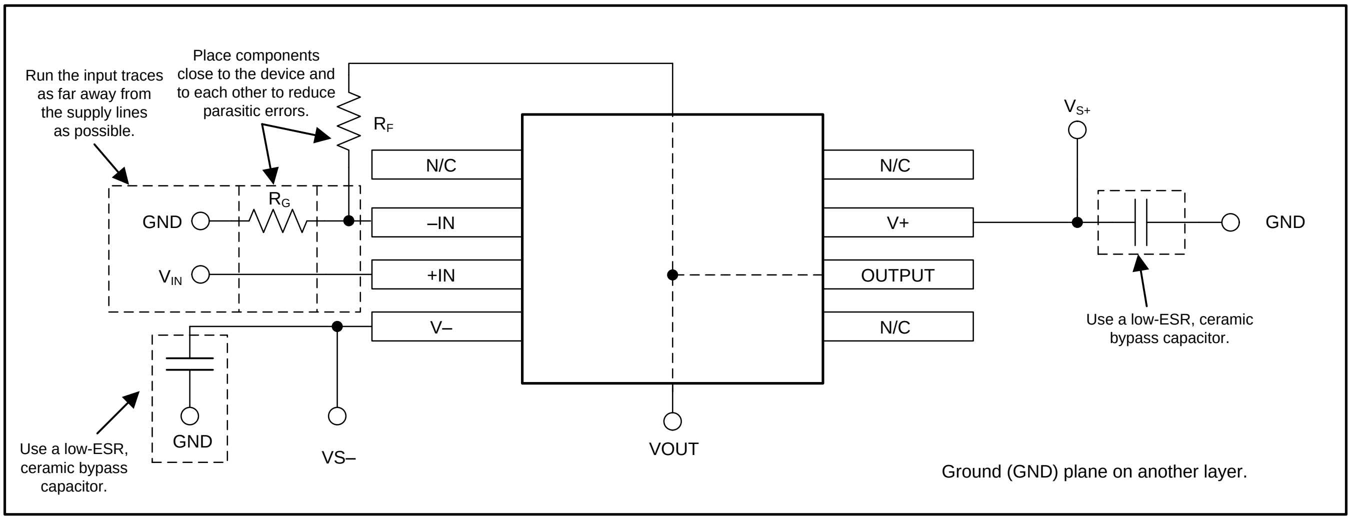


図 33. Operational Amplifier Board Layout for Noninverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

TLV354xデバイスについて、以下の参照資料の使用をお勧めします。すべてのドキュメントは、特に記述のない限りwww.ti.comからダウンロードできます。

- *『オペアンプ・アプリケーション・ハンドブック』*(SBOA092)
- *『アナログ・エンジニアのためのポケット・リファレンス』*(SLYW038)

11.2 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV3541	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV3542	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV3544	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3541IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD	Samples
TLV3541IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD	Samples
TLV3541IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3541	Samples
TLV3542IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	18TE	Samples
TLV3542IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	18TE	Samples
TLV3542IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3542	Samples
TLV3544IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV3544A	Samples
TLV3544IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3544	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

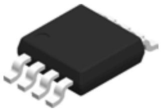
OTHER QUALIFIED VERSIONS OF TLV3544 :

- Automotive : TLV3544-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

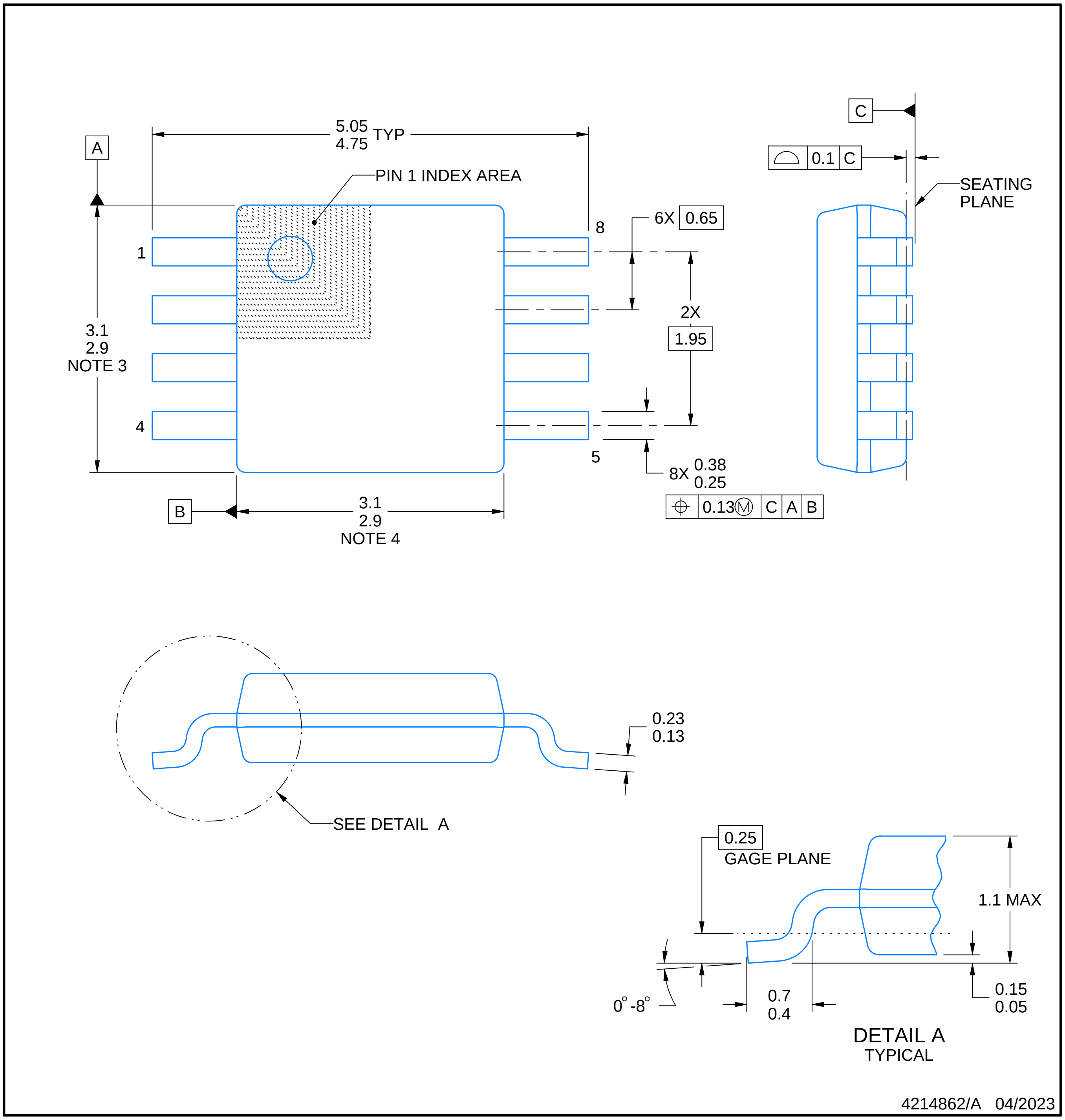
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

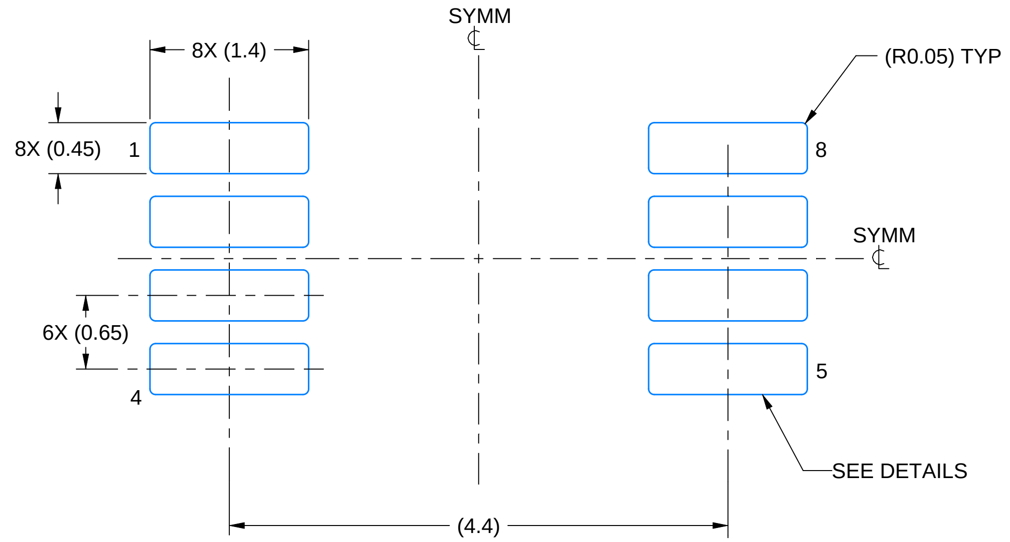


4214862/A 04/2023

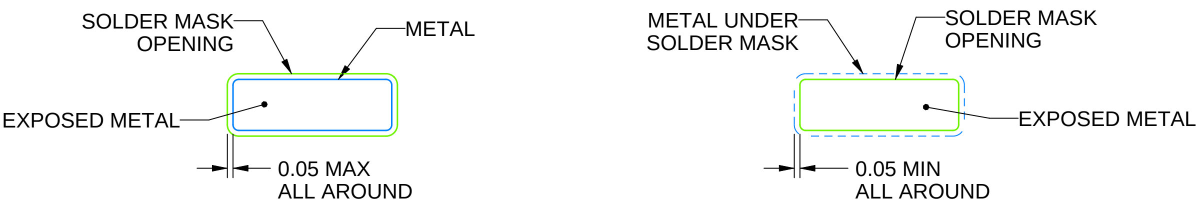
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

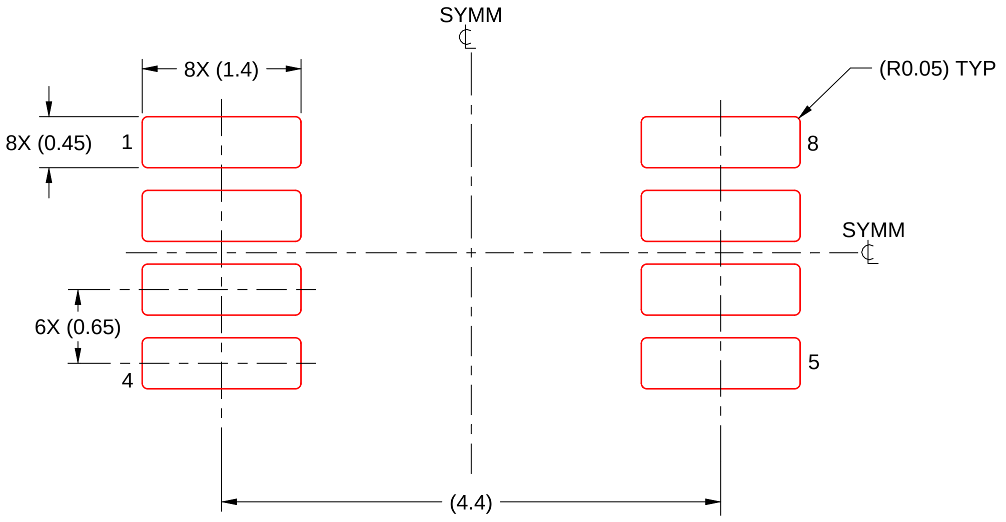
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

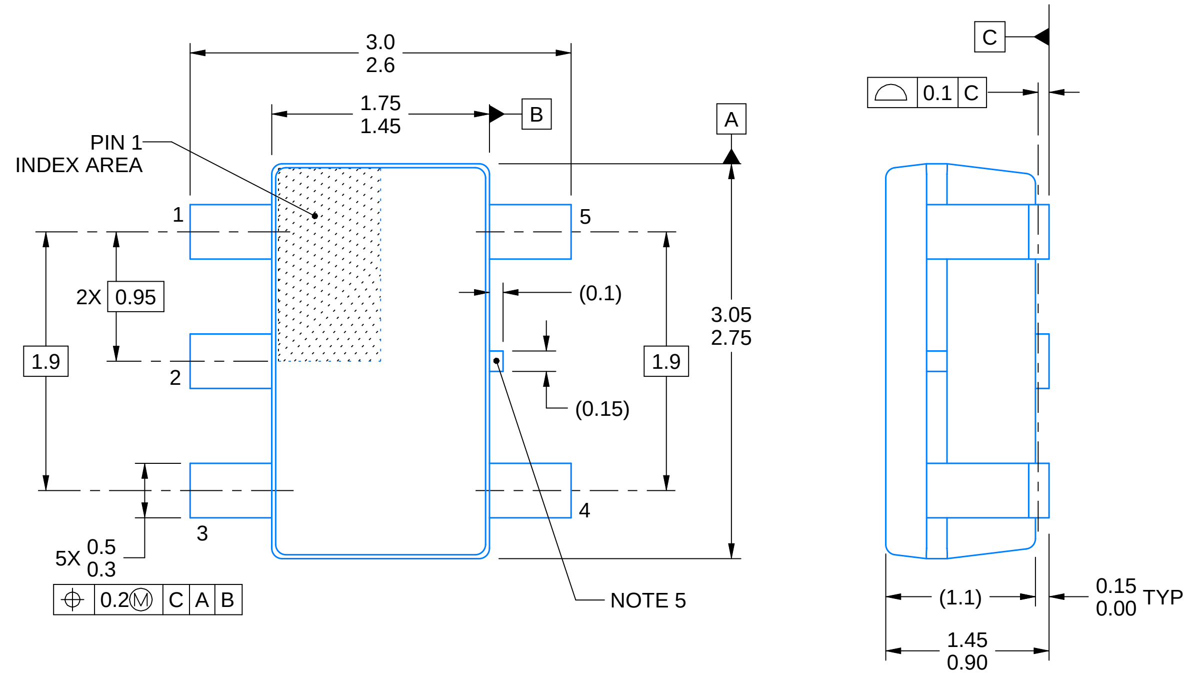
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

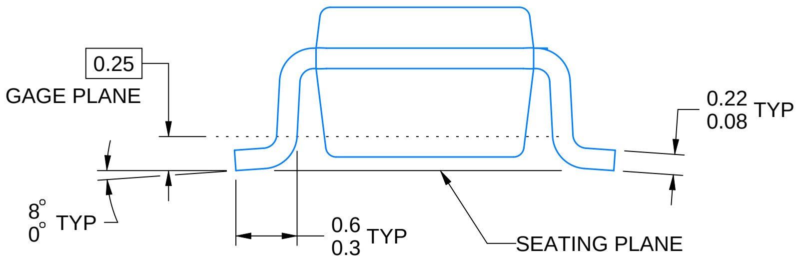


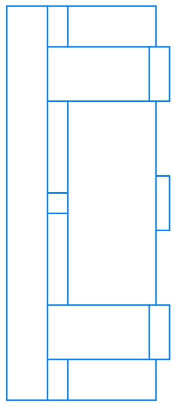
SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.





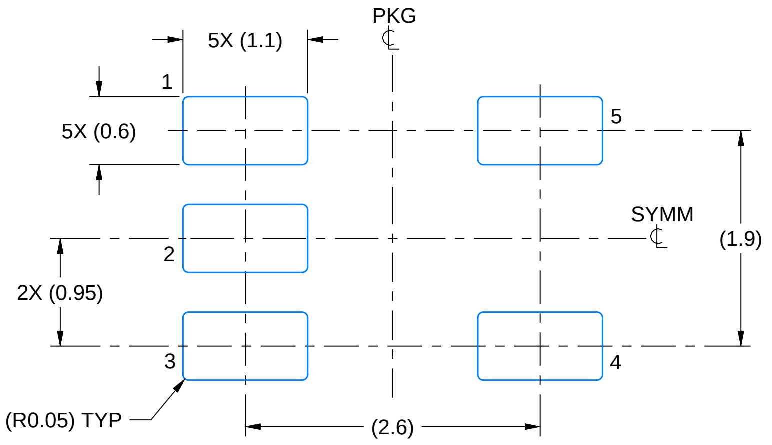


ALTERNATIVE PACKAGE SINGULATION VIEW

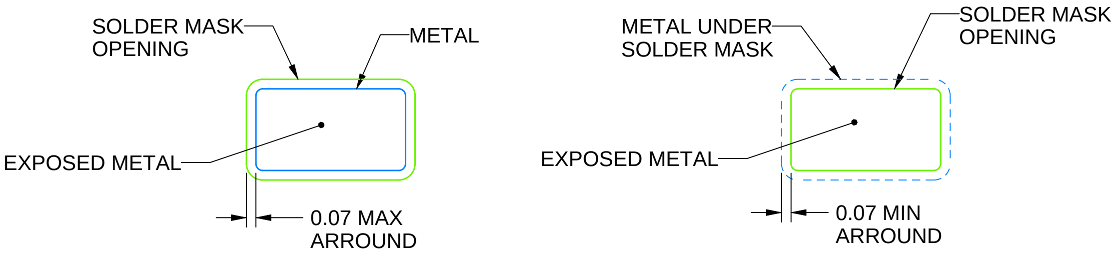
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



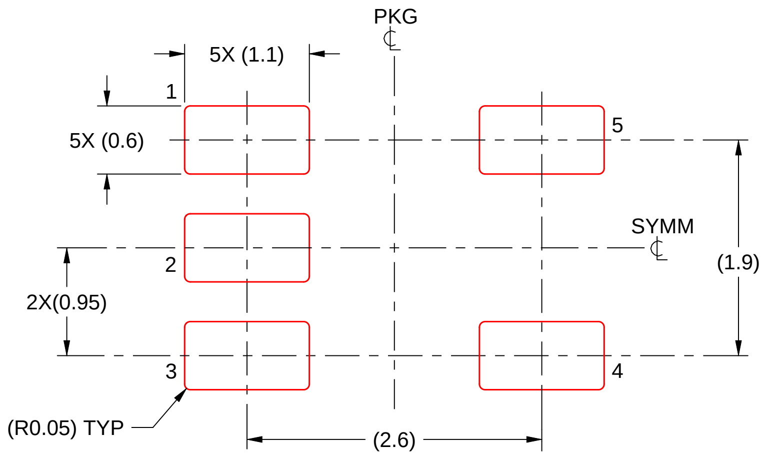
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

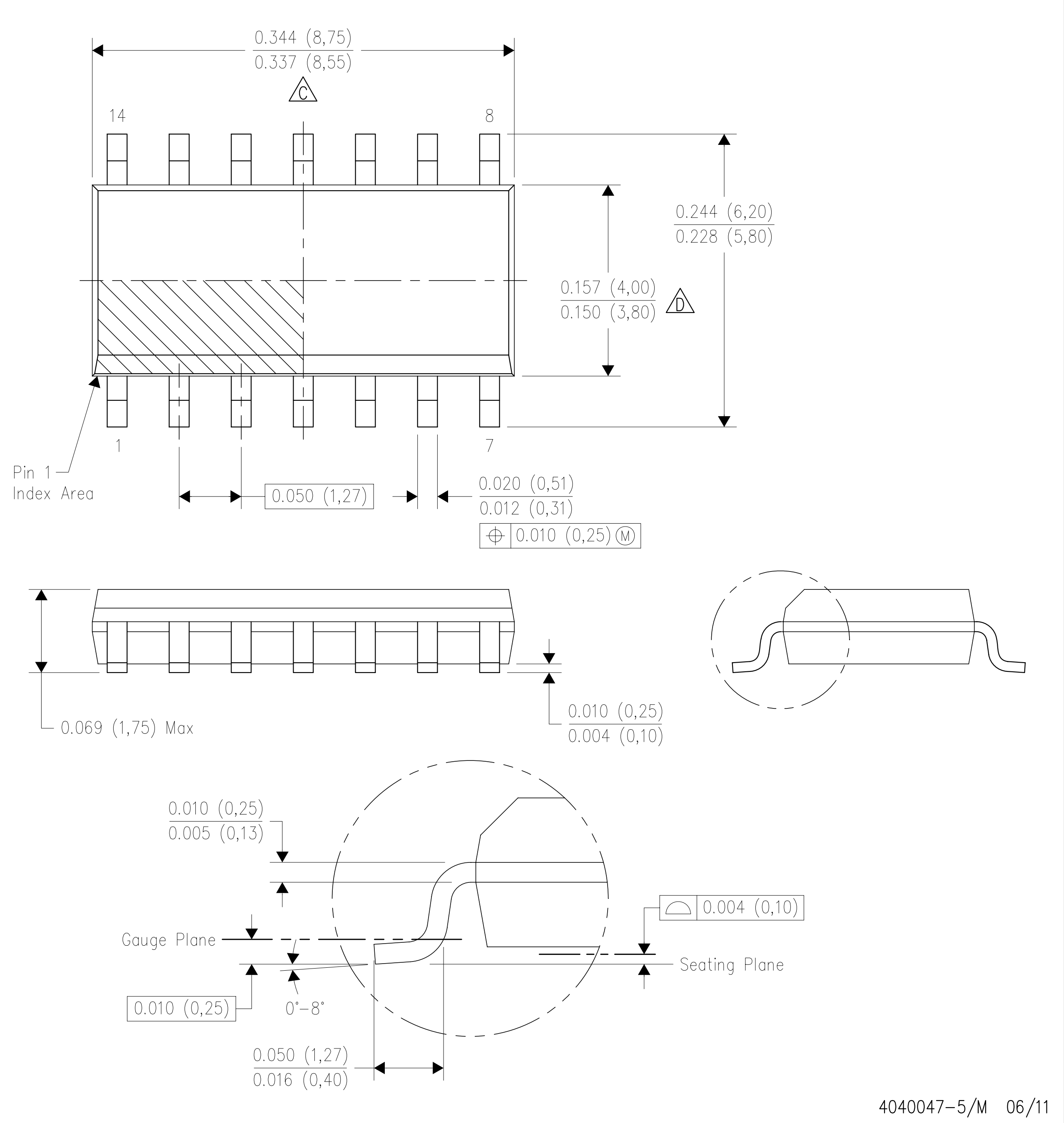


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

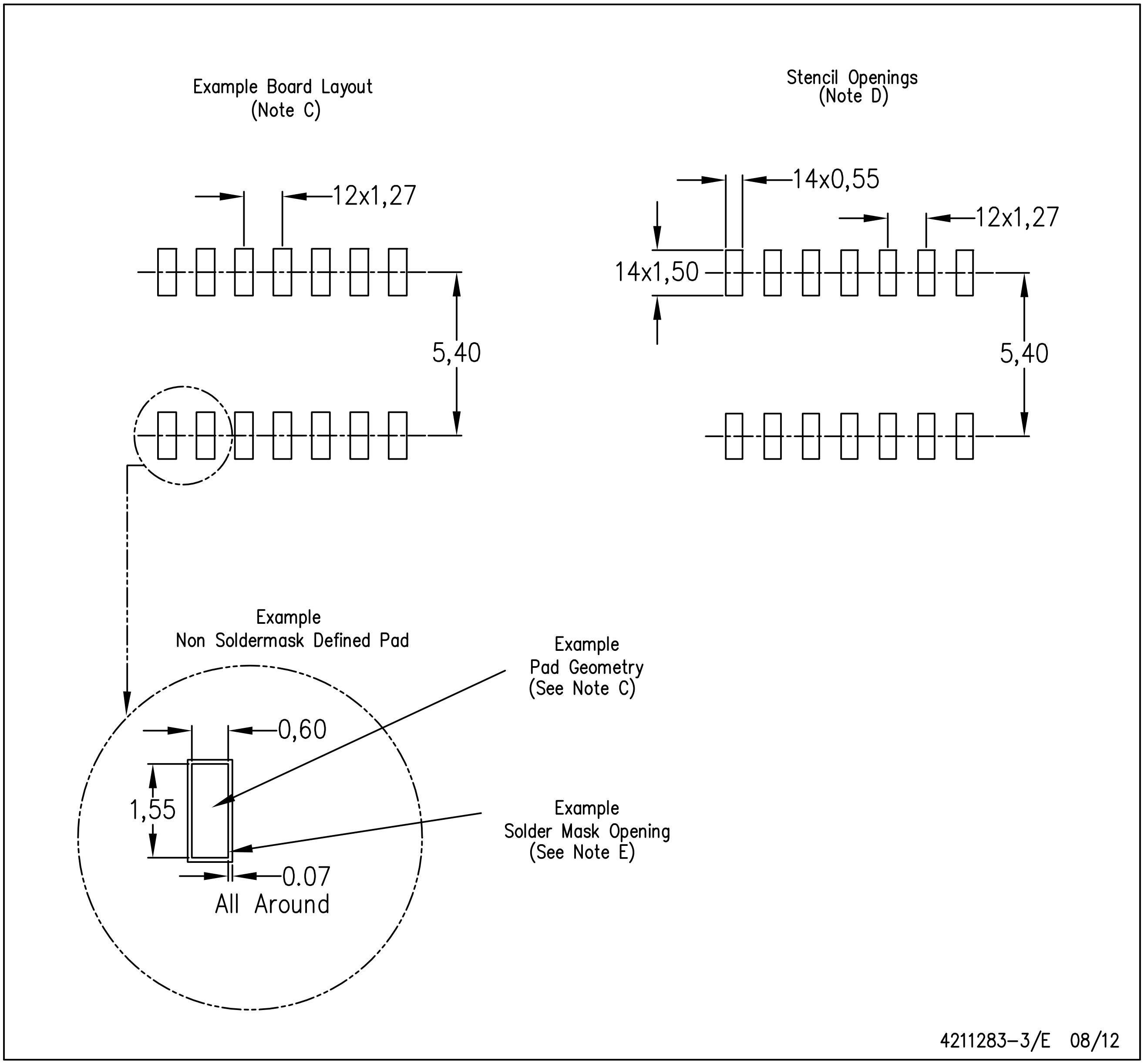
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



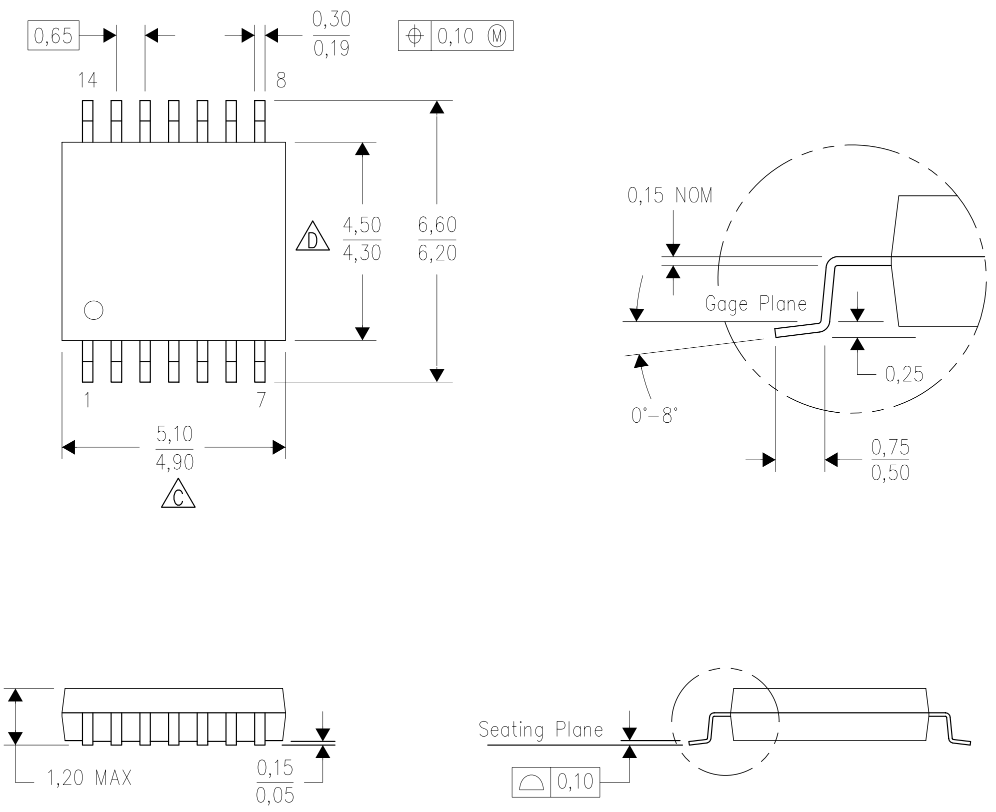
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

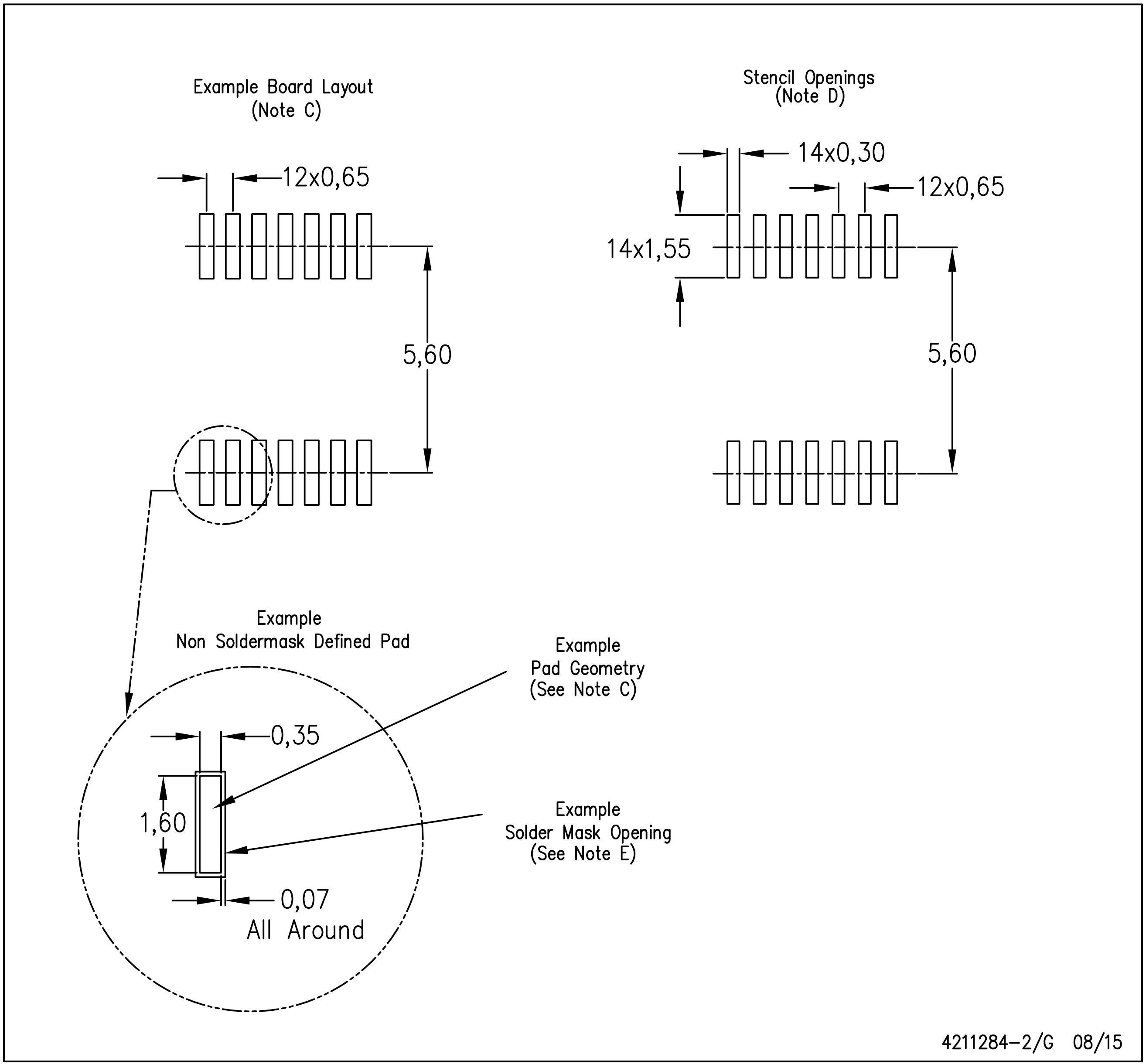
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



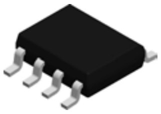
4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



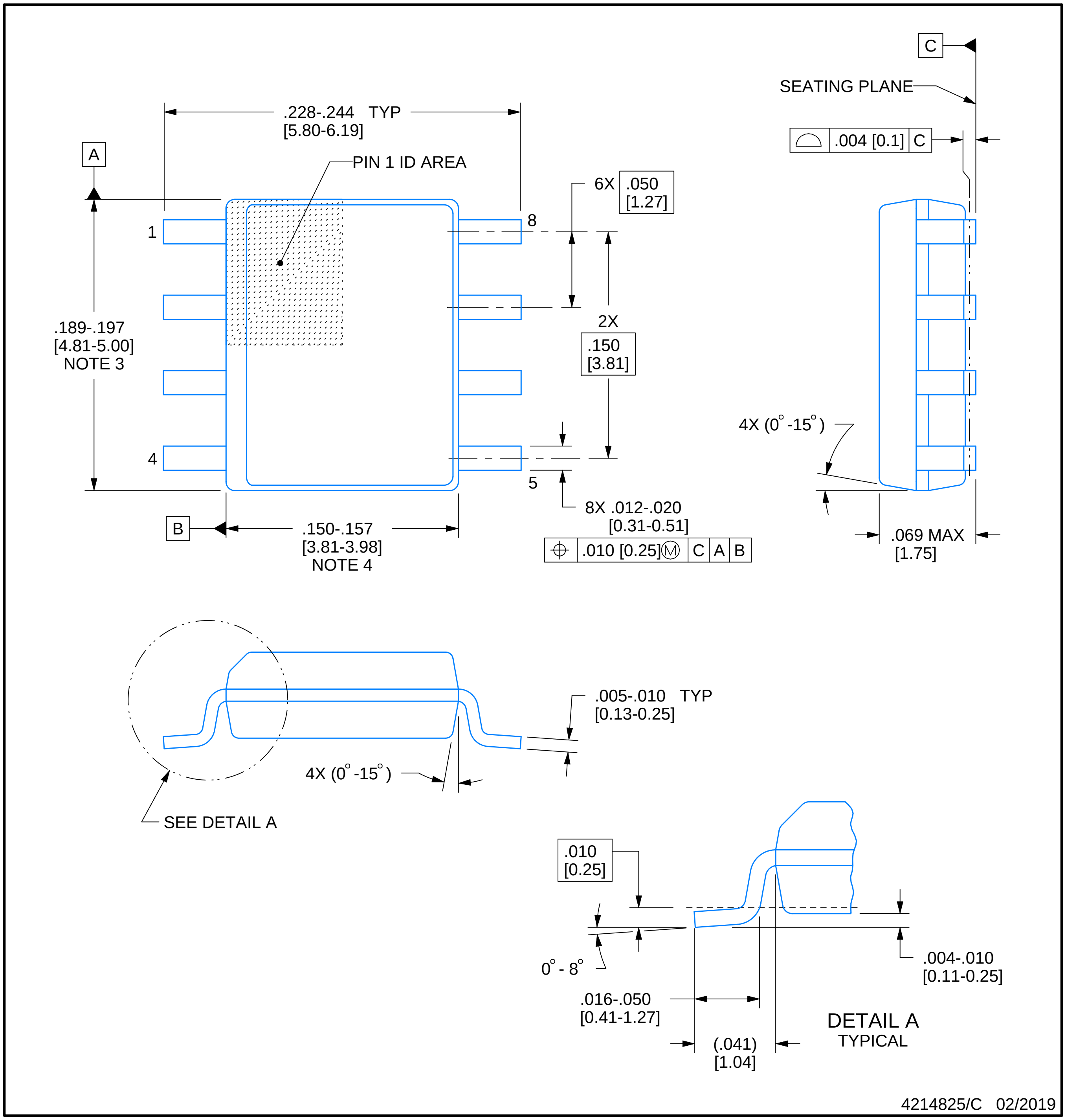
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

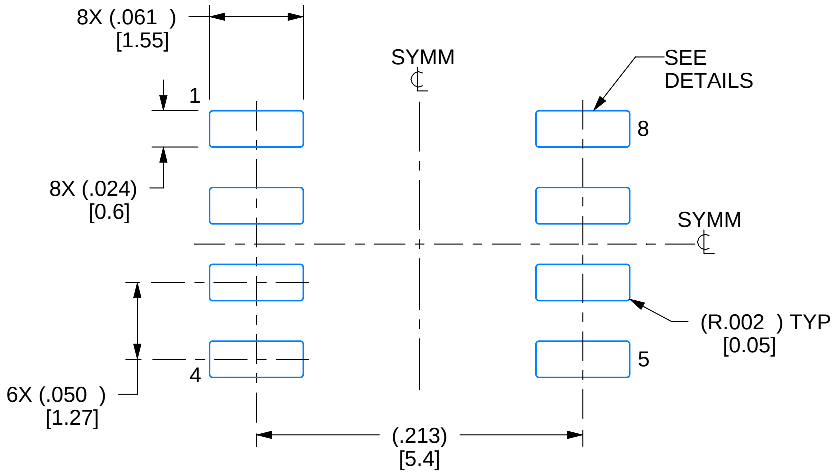
SMALL OUTLINE INTEGRATED CIRCUIT



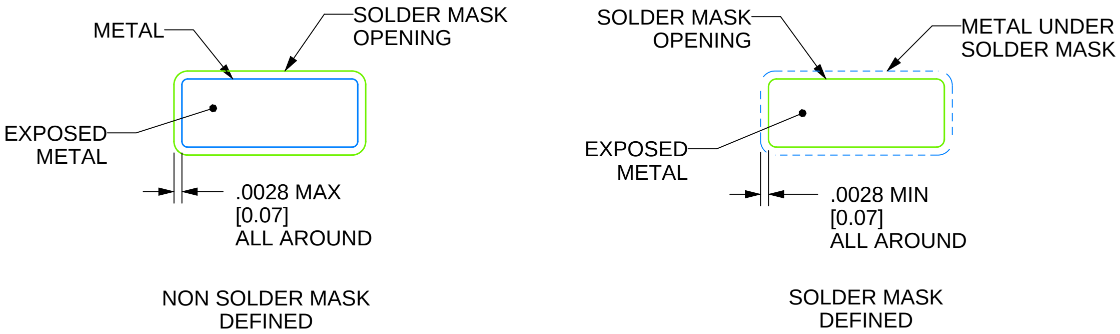
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



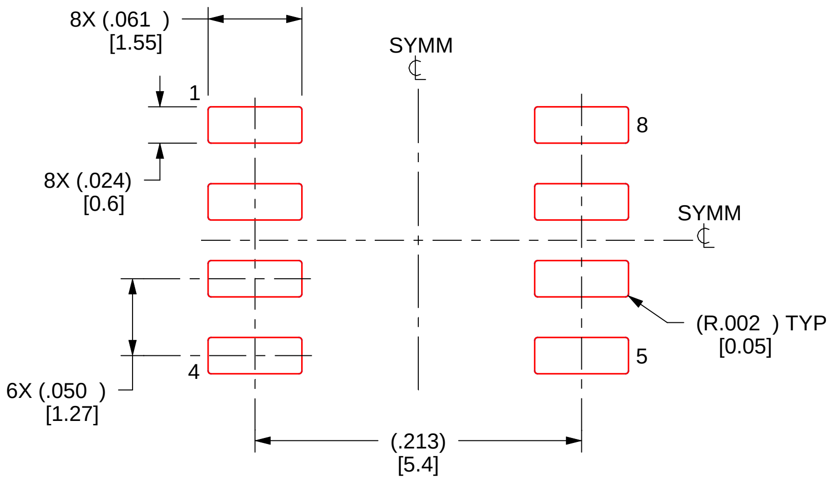
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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