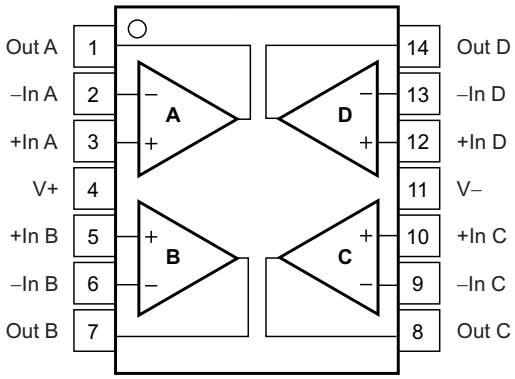
TEXAS INSTRUMENTS

TLV3544-Q1 250MHz、レール・ツー・レールI/O、CMOS車載用オペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード1: 動作時周囲温度範囲T_A -40℃～+125℃
  - デバイスHBM ESD分類レベル1C
  - デバイスCDM ESD分類レベルC3
- ユニティ・ゲイン帯域幅: 250MHz
- 広い帯域幅: 100MHz GBW
- 高いスルー・レート: 150V/µs
- 低ノイズ: 7.5nV/√Hz
- レール・ツー・レールI/O
- 高い出力電流: 100mA超
- 非常に優れたビデオ性能
  - 差動ゲイン: 0.02%、差動フェーズ: 0.09°
  - 0.1dBのゲイン・フラットネス(40MHz)
- 低い入力バイアス電流: 3pA
- 静止電流: 5.2mA
- サーマル・シャットダウン
- 電源電圧範囲: 2.5V～5.5V

簡略ブロック図



2 アプリケーション

- 電流センス・アンプ
- インバータおよびモータ制御
- エンジン管理
- バッテリ管理
- ナビゲーションおよびラジオ・システム
- 尿素レベルおよび濃度センサ
- 死角検知
- 短距離から中距離のレーダー
- サラウンド・ビューおよびバックアップ・カメラの映像処理
- 自動車のパワートレイン・センサ・システム用のSAR ADCドライバ

3 概要

TLV3544-Q1シリーズの高速、電圧帰還型CMOSオペアンプは、広い帯域幅を必要とするビデオおよびその他のアプリケーション用に設計されています。これらはユニティ・ゲイン安定で、大きな出力電流を駆動できます。差動ゲインは0.02%、差動位相は0.09°です。静止電流はチャネルごとにわずか4.9mAです。

TLV3544-Q1クワッド・チャネル・オペアンプは、最低2.5V (±1.25V)、最高5.5V (±2.75V)のシングルまたはデュアル電源で動作するよう最適化されています。同相入力範囲は電源の範囲よりも拡大されています。出力スイングはレールから100mV以内で、広いダイナミック・レンジに対応しています。

マルチチャネル・バージョンは、完全に独立した回路により、クロストークを最小化し、干渉の発生を防止しています。すべての仕様は、拡張温度範囲の-40℃～+125℃で規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV3544-Q1	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

目次

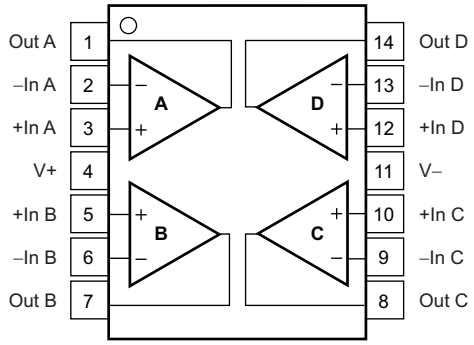
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年10月	*	初版

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–In A	2	I	Inverting input, channel A
+In A	3	I	Noninverting input, channel A
–In B	6	I	Inverting input, channel B
+In B	5	I	Noninverting input, channel B
–In C	9	I	Inverting input, channel C
+In C	10	I	Noninverting input, channel C
–In D	13	I	Inverting input, channel D
+In D	12	I	Noninverting input, channel D
Out A	1	O	Output, channel A
Out B	7	O	Output, channel B
Out C	8	O	Output, channel C
Out D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply
V+	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V−		7.5	V
	Signal input terminals(2)	(V−) − (0.5)	(V+) + 0.5	
Current	Signal input terminals(2)	–10	10	mA
	Output short circuit(3)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.5	5.5	V
	Specified temperature	–40	125	°C

6.4 Thermal Information: TLV3544-Q1

THERMAL METRIC		TLV3544-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

6.5 Electrical Characteristics: V_S = 2.7 V to 5.5 V Single-Supply

At T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V, at T_A = 25°C		±2	±10	mV
dV_{OS}/dT	Input offset voltage vs temperature	V_S = 5 V, at T_A = −40°C to +125°C		±4.5		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 5.5 V, V_{CM} = (V_S/2) − 0.55 V		±200	±800	µV/V
		V_S = 2.7 V to 5.5 V, V_{CM} = (V_S/2) − 0.55 V, at T_A = −40°C to +125°C			±900	
INPUT BIAS CURRENT						
I_B	Input bias current			3		pA
I_{OS}	Input offset current			±1		pA
NOISE						
e_n	Input voltage noise density	f = 1 MHz		7.5		nV/√Hz
i_n	Current noise density	f = 1 MHz		50		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, –0.1 V < V_{CM} < 3.5 V, at T_A = 25°C	66	80		dB
		V_S = 5.5 V, –0.1 V < V_{CM} < 5.6 V, at T_A = 25°C	56	68		
INPUT IMPEDANCE						
	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = 5.5 V, 0.3 V < V_O < 4.7 V, at T_A = 25°C	94	110		dB
		V_S = 5 V, 0.4 V < V_O < 4.6 V, at T_A = –40°C to +125°C	90			
FREQUENCY RESPONSE						
$f_{–3dB}$	Small-signal bandwidth	At G = +1, V_O = 100 mV_{PP}, R_F = 25 Ω		250		MHz
		At G = +2, V_O = 100 mV_{PP}		90		
GBW	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness	At G = +2, V_O = 100 mV_{PP}		40		MHz
SR	Slew rate	V_S = 5 V, G = +1, 4-V step		150		V/µs
		V_S = 5 V, G = +1, 2-V step		130		
		V_S = 3 V, G = +1, 2-V step		110		
	Rise-and-fall time	At G = +1, V_O = 200 mV_{PP}, 10% to 90%		2		ns
		At G = +1, V_O = 2 V_{PP}, 10% to 90%		11		
	Settling time	0.1%, V_S = 5 V, G = +1, 2-V output step		30		ns
		0.01%, V_S = 5 V, G = +1, 2-V output step		60		
	Overload recovery time	V_{IN} × Gain = V_S		5		ns

Electrical Characteristics: V_S = 2.7 V to 5.5 V Single-Supply (continued)

At T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE, continued							
	Harmonic distortion	Second harmonic	At G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–75		dBc
		Third harmonic	At G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–83		
	Differential gain error		NTSC, R_L = 150 Ω		0.02%		
	Differential phase error		NTSC, R_L = 150 Ω		0.09		°
	Channel-to-channel crosstalk	TLV3544-Q1	f = 5 MHz		–84		dB
OUTPUT							
	Voltage output swing from rail		V_S = 5 V, R_L = 1 kΩ, A_{OL} > 94 dB, at T_A = 25°C		0.1	0.3	V
I_O	Output current (1) (2)		V_S = 5 V	100			mA
			V_S = 3 V		50		mA
	Closed-loop output impedance		f < 100 kHz		0.05		Ω
R_O	Open-loop output resistance				35		Ω
POWER SUPPLY							
V_S	Specified voltage			2.7		5	V
	Operating voltage			2.5		5.5	
I_Q	Quiescent current (per amplifier)		At T_A = 25°C, V_S = 5 V, enabled, I_O = 0		5.2	6.5	mA
THERMAL SHUTDOWN – JUNCTION TEMPERATURE							
	Shutdown				160		°C
	Reset from shutdown				140		°C
THERMAL RANGE							
	Specified			–40		125	°C
	Operating			–55		150	°C
	Storage			–65		150	°C

(1) See typical characteristic curves, *Output Voltage Swing vs Output Current* (図 20 and 図 22).
(2) Specified by design.

6.6 Typical Characteristics

At T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

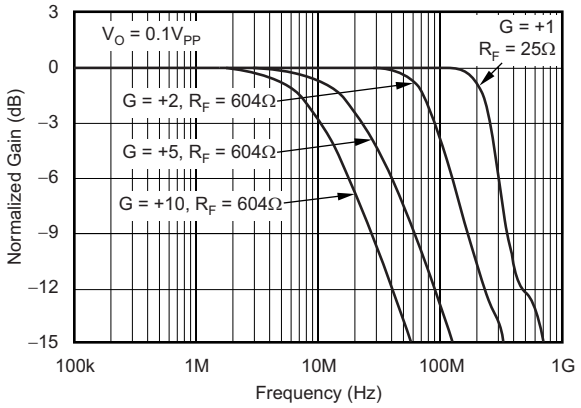


図 1. Noninverting Small-Signal Frequency Response

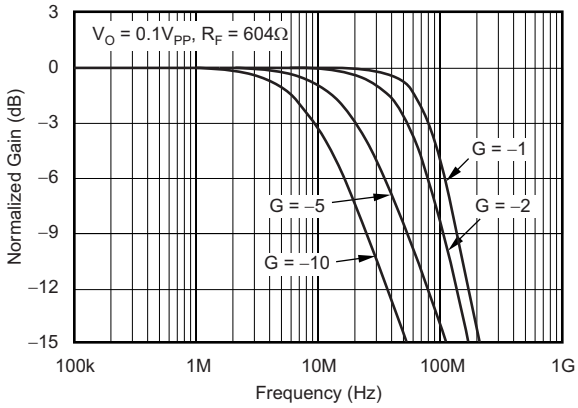


図 2. Inverting Small-Signal Frequency Response

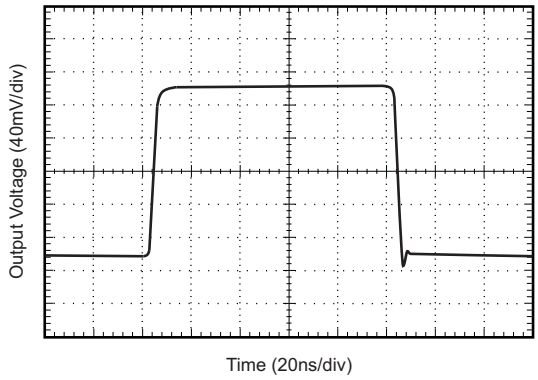


図 3. Noninverting Small-Signal Step Response

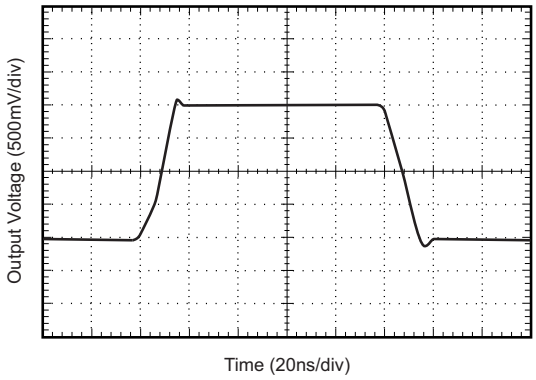


図 4. Noninverting Large-Signal Step Response

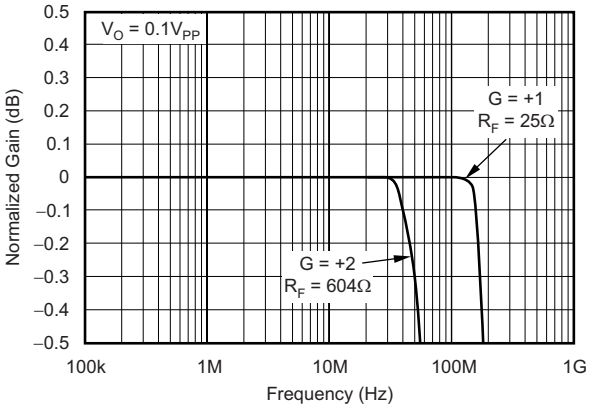


図 5. 0.1-dB Gain Flatness

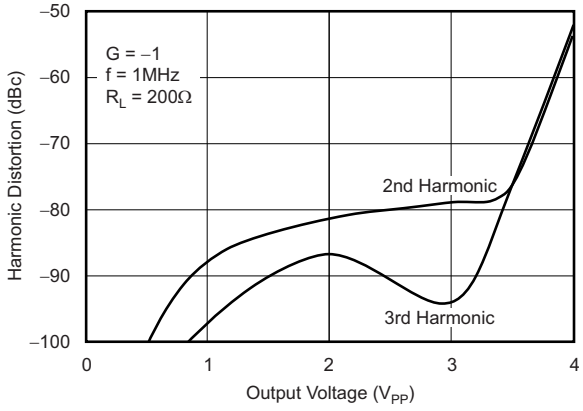


図 6. Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

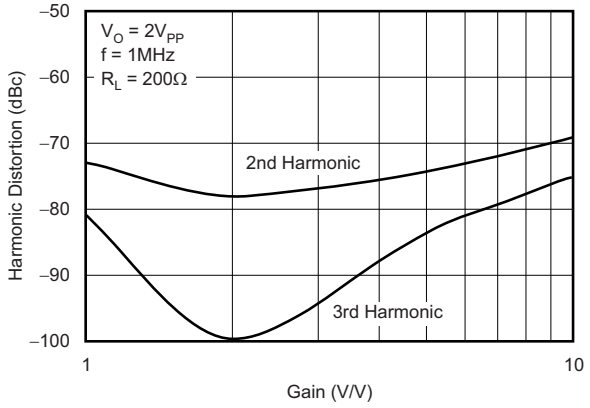


図 7. Harmonic Distortion vs Noninverting Gain

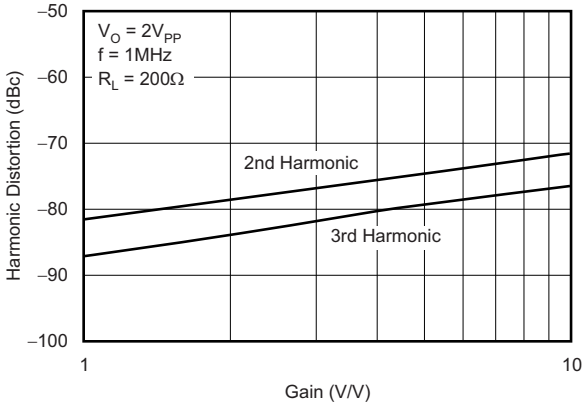


図 8. Harmonic Distortion vs Inverting Gain

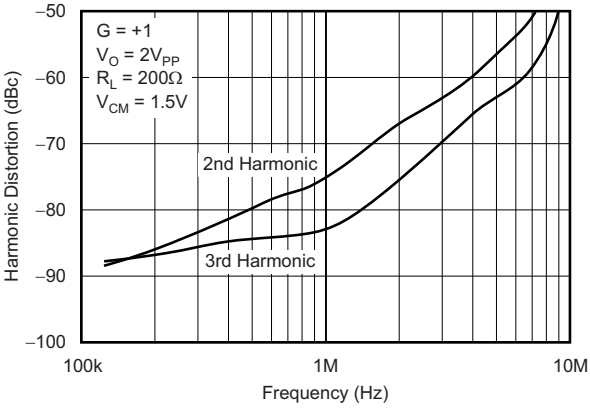


図 9. Harmonic Distortion vs Frequency

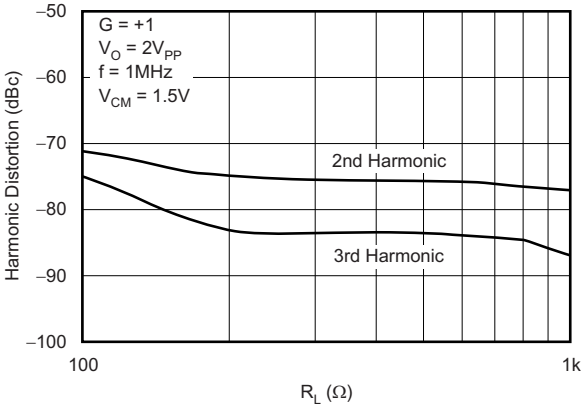


図 10. Harmonic Distortion vs Load Resistance

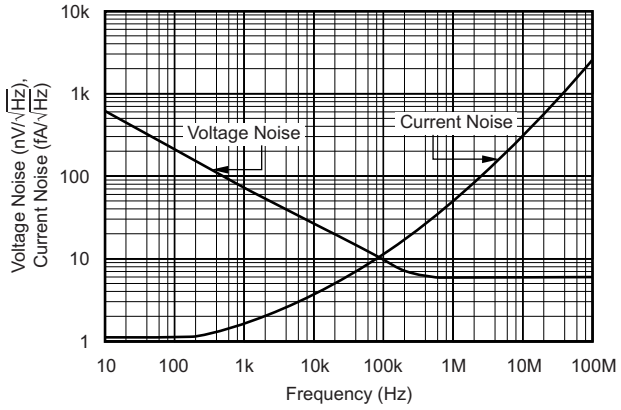


図 11. Input Voltage and Current Noise Spectral Density vs Frequency

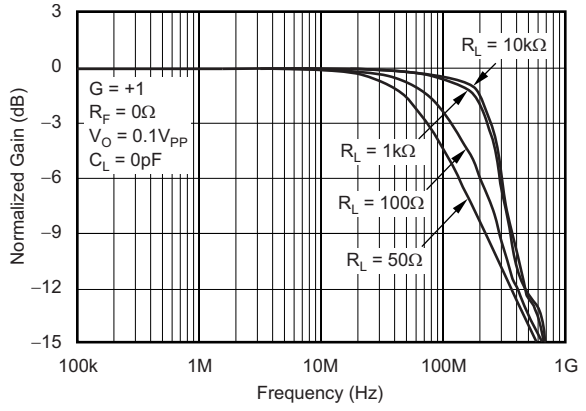


図 12. Frequency Response for Various R_L

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

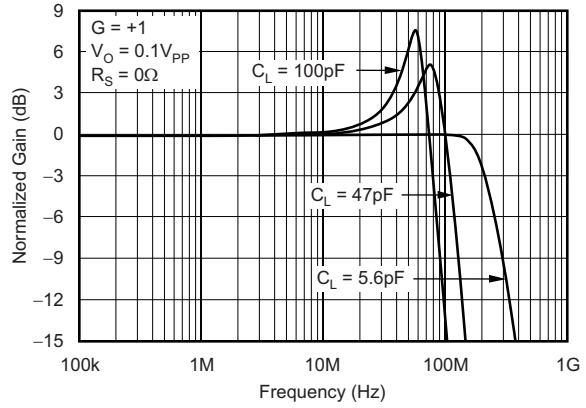


図 13. Frequency Response for Various C_L

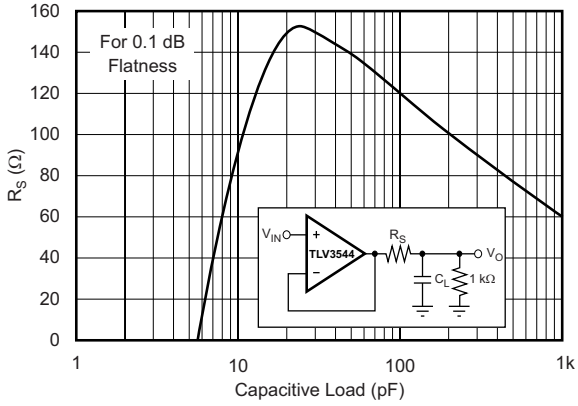


図 14. Recommended R_S vs Capacitive Load

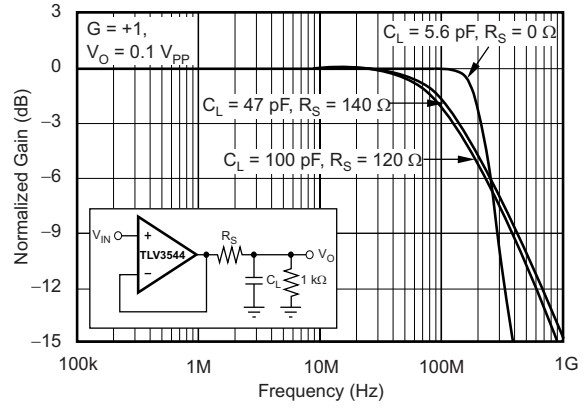


図 15. Frequency Response vs Capacitive Load

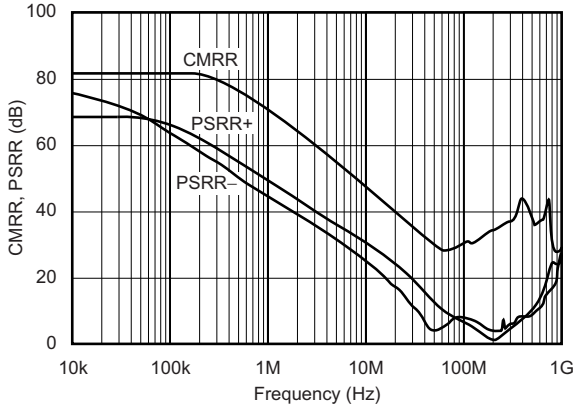


図 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

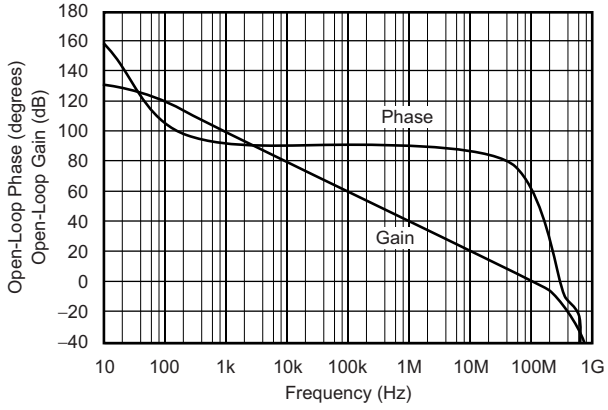


図 17. Open-Loop Gain and Phase

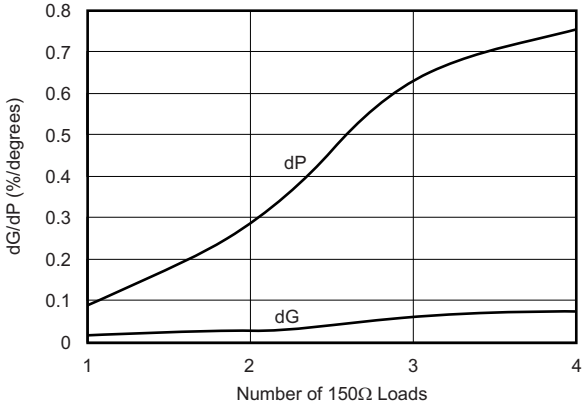


図 18. Composite Video Differential Gain and Phase

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

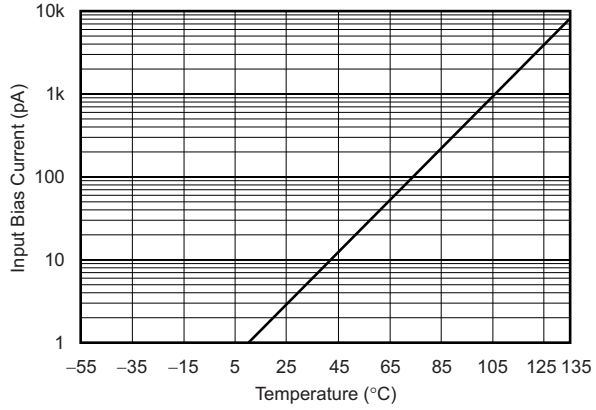


図 19. Input Bias Current vs Temperature

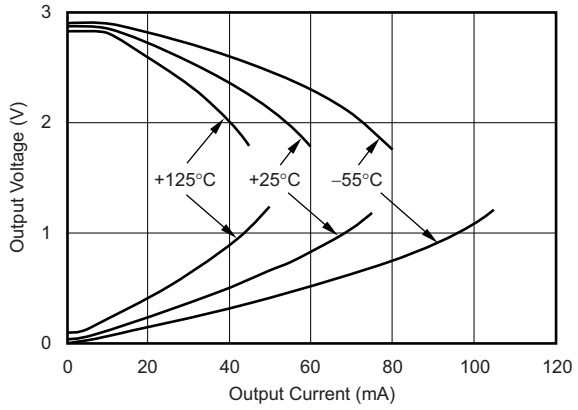


図 20. Output Voltage Swing vs Output Current for V_S = 3 V

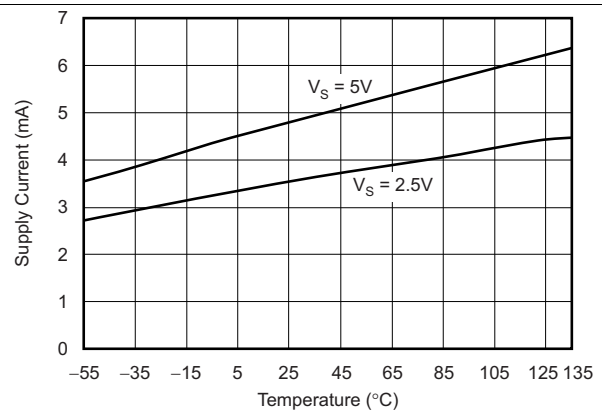


図 21. Supply Current vs Temperature

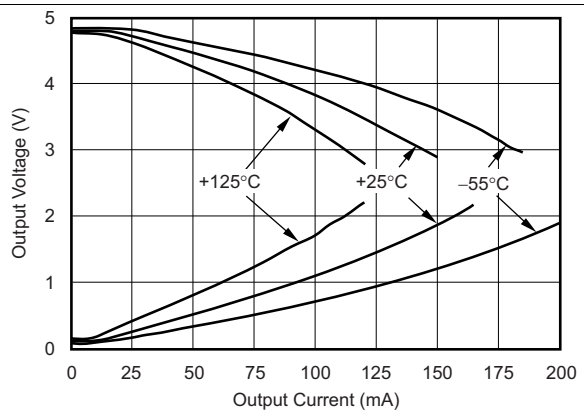


図 22. Output Voltage Swing vs Output Current for V_S = 5 V

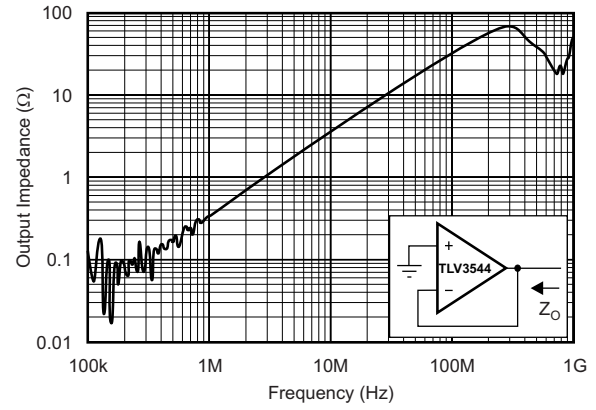


図 23. Closed-Loop Output Impedance vs Frequency

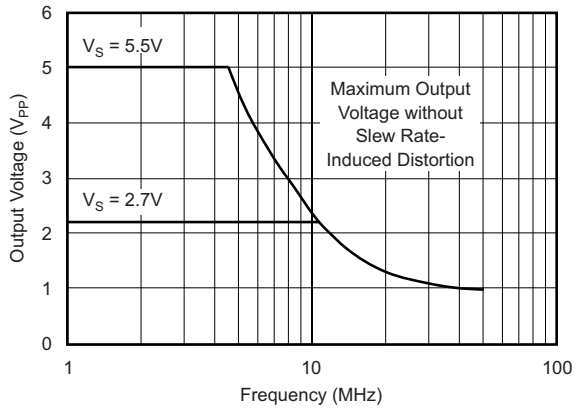


図 24. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S/2, unless otherwise noted.

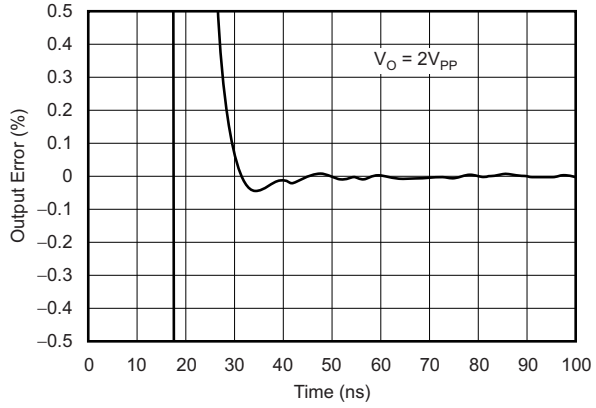


図 25. Output Settling Time to 0.1%

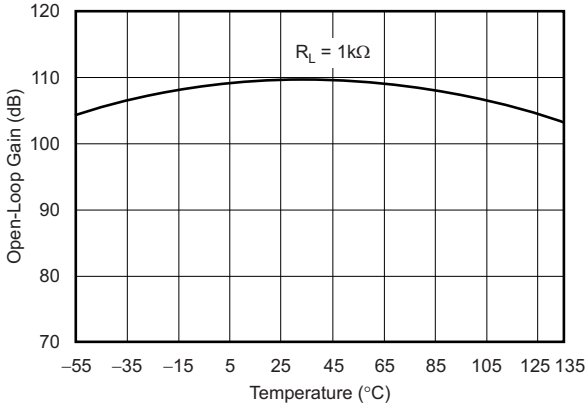


図 26. Open-Loop Gain vs Temperature

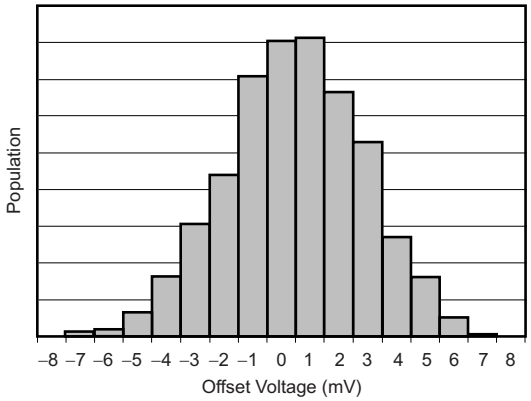


図 27. Offset Voltage Production Distribution

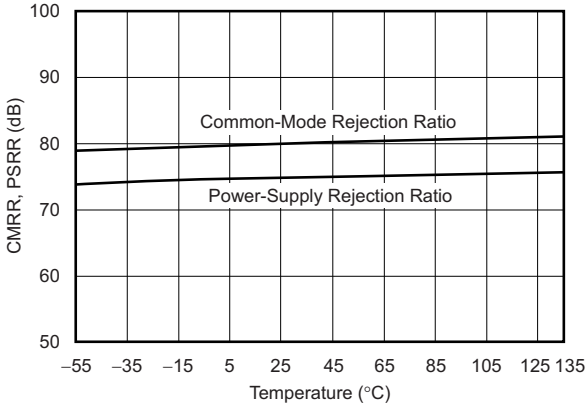


図 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

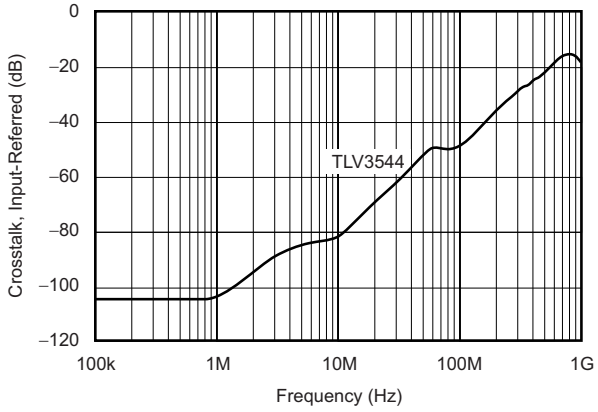


図 29. Channel-to-Channel Crosstalk

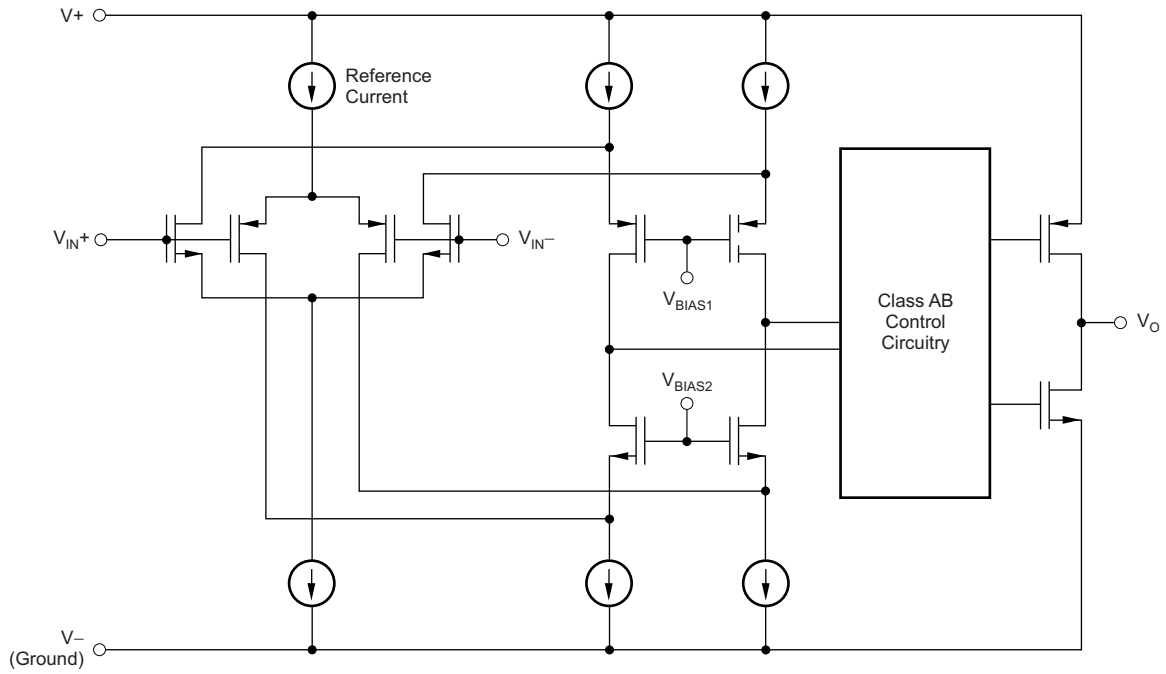
7 Detailed Description

7.1 Overview

The TLV3544-Q1 is a quad-channel CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications.

The amplifier features a 100-MHz gain bandwidth and 150-V/µs slew rate, but it is unity-gain stable and can be operated as a +1-V/V voltage follower.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 TLV3544-Q1 Comparison

表 1 lists several members of the device family that includes the TLV3544-Q1.

表 1. Device Family Comparison

FEATURES	PRODUCT
Shutdown Version of TLV3544 Family	OPAx357
200-MHz GBW, Rail-to-Rail Output, CMOS, Shutdown	OPAx355
200-MHz GBW, Rail-to-Rail Output, CMOS	OPAx356
38-MHz GBW, Rail-to-Rail Input/Output, CMOS	OPAx350/OPAx353
75-MHz BW G = 2, Rail-to-Rail Output	OPA2631
150-MHz BW G = 2, Rail-to-Rail Output	OPA2634
100-MHz BW, Differential Input/Output, 3.3-V Supply	THS412x

7.3.2 Operating Voltage

The TLV3544-Q1 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V).

> **注意**
>
> Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in *Typical Characteristics* of this data sheet.

7.3.3 Rail-to-Rail Input

The specified input common-mode voltage range of the TLV3544-Q1 extends 100 mV beyond the supply rails. This extended range is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) − 1.2 V. There is a small transition region, typically (V+) − 1.5 V to (V+) − 0.9 V, in which both pairs are on. This 600-mV transition region can vary ±500 mV with process variation. Thus, the transition region (both input stages on) can range from (V+) − 2 V to (V+) − 1.5 V on the low end, up to (V+) − 0.9 V to (V+) − 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

7.3.4 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing can be achieved while maintaining high open-loop gain. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (図 20 and 図 22).

7.3.5 Output Drive

The TLV3544-Q1 output stage can supply a continuous output current of ±100 mA and yet provide approximately 2.7 V of output swing on a 5-V supply, as shown in 図 30. For maximum reliability, TI does not recommend running a continuous DC current in excess of ±100 mA. Refer to the typical characteristic curves, *Output Voltage Swing vs Output Current* (図 20 and 図 22). For supplying continuous output currents greater than ±100 mA, the TLV3544-Q1 may be operated in parallel, as shown in 図 31.

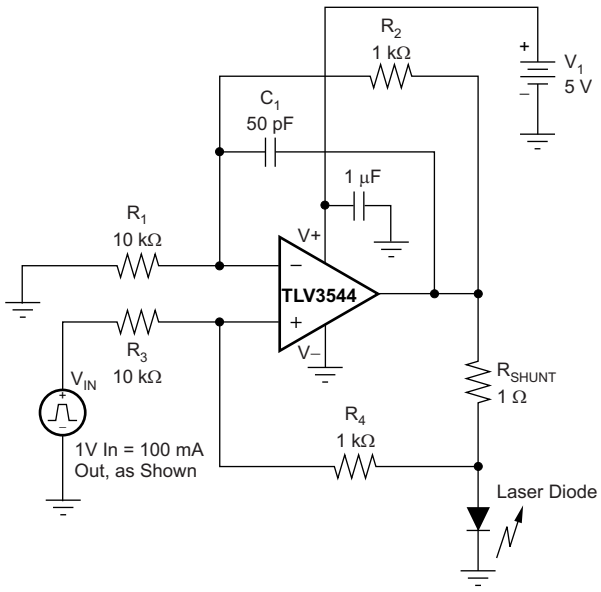


図 30. Laser Diode Driver

The TLV3544-Q1 provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the TLV3544-Q1 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

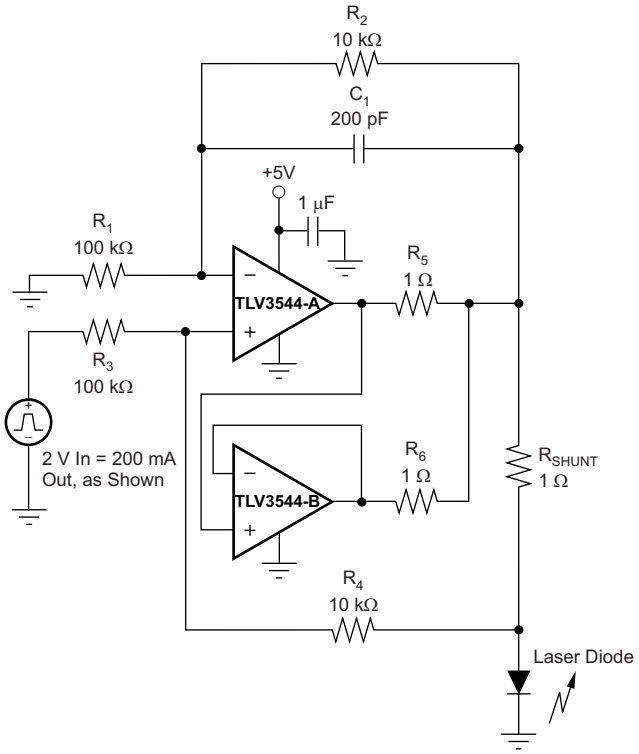


図 31. Parallel Operation

7.3.6 Video

The TLV3544-Q1 output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in 図 32. By back-terminating a transmission line, it does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; it presents only a 150-Ω resistive load to the TLV3544-Q1 output.

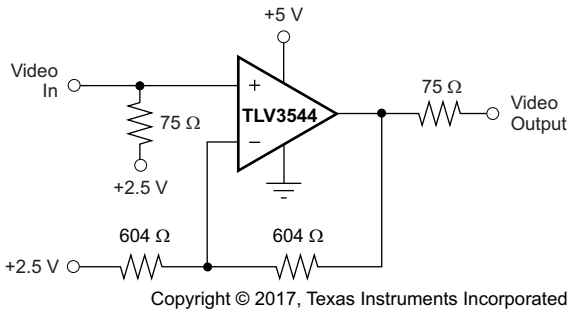
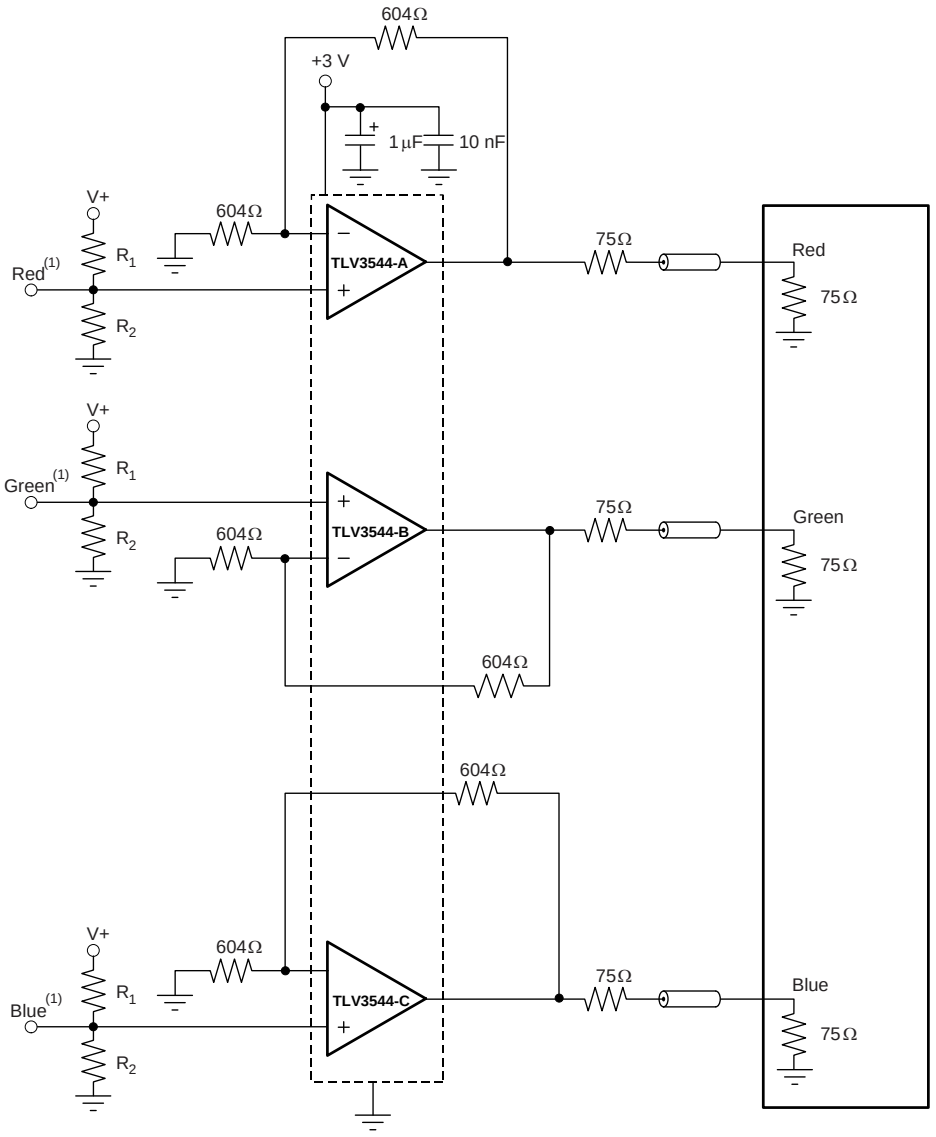


図 32. Single-Supply Video Line Driver

The TLV3544-Q1 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See 図 33.



(1) Source video signal offset 300 mV above ground to accommodate op amp swing−to−ground capability.

図 33. RGB Cable Driver

7.3.7 Driving Analog-to-Digital converters

The TLV3544-Q1 series op amps offer 60 ns of settling time to 0.01%, making them a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The TLV3544-Q1 provides an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, the OPA350 series is recommended.

図 34 illustrates the TLV3544-Q1 driving an A/D converter. With the TLV3544-Q1 in an inverting configuration, a capacitor across the feedback resistor can be used to filter high-frequency noise in the signal.

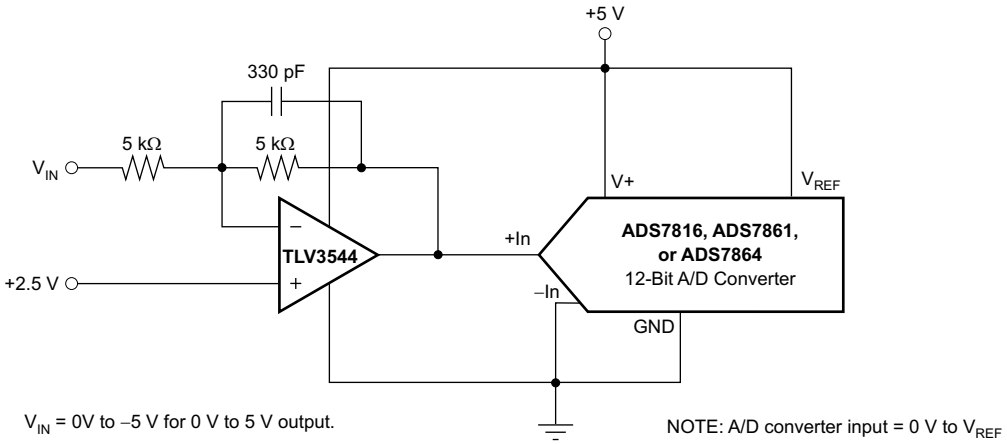


図 34. The TLV3544-Q1 in Inverting Configuration Driving the ADS7816

7.3.8 Capacitive Load and Stability

The TLV3544-Q1 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. Refer to the typical characteristic curve, *Frequency Response for Various C_L* (図 13) for details.

The TLV3544-Q1 topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. Refer to the typical characteristic curves, *Recommended R_S vs Capacitive Load* (図 14) and *Frequency Response vs Capacitive Load* (図 15) for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in 図 35. This configuration significantly reduces ringing with large capacitive loads—see the typical characteristic curve, *Frequency Response vs Capacitive Load* (図 15). However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is approximately a 0.2% error at the output.

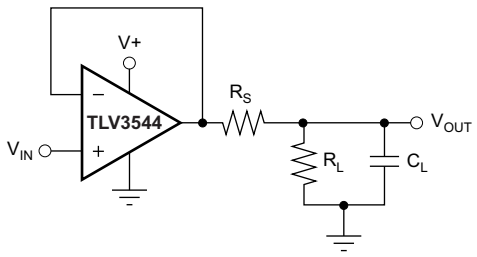


図 35. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

7.3.9 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, low input voltage, and current noise make the TLV3544-Q1 an ideal wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in 図 36, are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the TLV3544-Q1], the desired transimpedance gain (R_F), and the Gain-Bandwidth Product (GBW) for the TLV3544-Q1 (100 MHz typical). With these three variables set, the feedback capacitor value (C_F) may be set to control the frequency response.

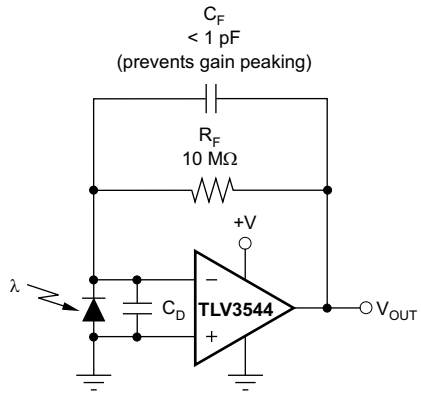


図 36. Transimpedance Amplifier

To achieve a maximally flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in 式 1:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by 式 2:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200-MHz GBW) or the OPA655 (400-MHz GBW) may be used.

7.4 Device Functional Modes

The TLV3544-Q1 is powered on when the supply is connected. The devices can be operated as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices can also be used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV3544-Q1 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but it is unity-gain stable and can be operated as a 1-V/V voltage follower.

8.2 Typical Application

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the TLV3544-Q1 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in 図 37, are the expected diode capacitance, which include the parasitic input common-mode and differential-mode input capacitance; the desired transimpedance gain; and the gain-bandwidth (GBW) for the TLV3544-Q1 (20 MHz). With these three variables set, the feedback capacitor value can be set to control the frequency response. Feedback capacitance includes the stray capacitance of, which is 0.2 pF for a typical surface-mount resistor.

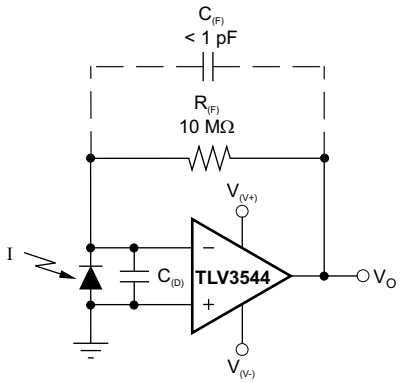


図 37. Dual-Supply Transimpedance Amplifier

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage, $V_{(V+)}$	2.5 V
Supply voltage, $V_{(V-)}$	–2.5 V

$C_{(F)}$ is optional to prevent gain peaking. $C_{(F)}$ includes the stray capacitance of $R_{(F)}$.

8.2.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using 式 3.

$$\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (3)$$

Calculate the bandwidth using 式 4.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (4)$$

8.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select $R_{(F)}$ to create the total required gain. Using a lower value for $R_{(F)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(F)}$ increases with the square-root of $R_{(F)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.

2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(F)}$ to limit bandwidth, even if not required for stability.

4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

8.2.3 Application Curve

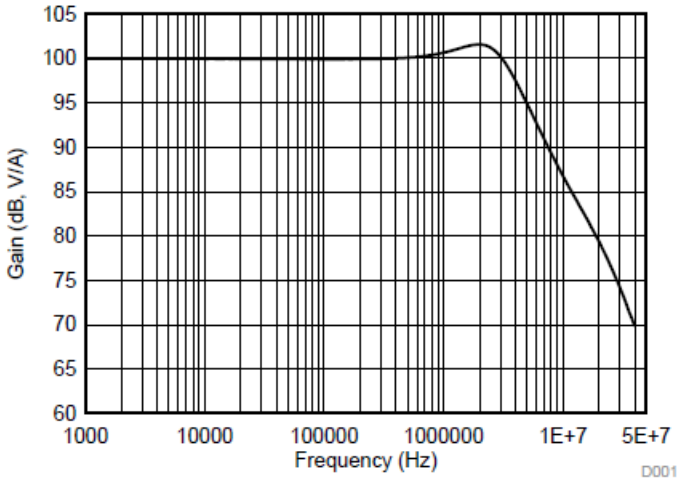


図 38. AC Transfer Function

9 Power Supply Recommendations

The TLV3544-Q1 is specified for operation from 2.5 V to 5.5 V (±1.25 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown *Typical Characteristics*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be employed for the TLV3544-Q1. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin assure clean, stable operation. Large areas of copper also provides a means of dissipating heat that is generated in normal operation.

TI does not recommend using sockets with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

10.2 Layout Example

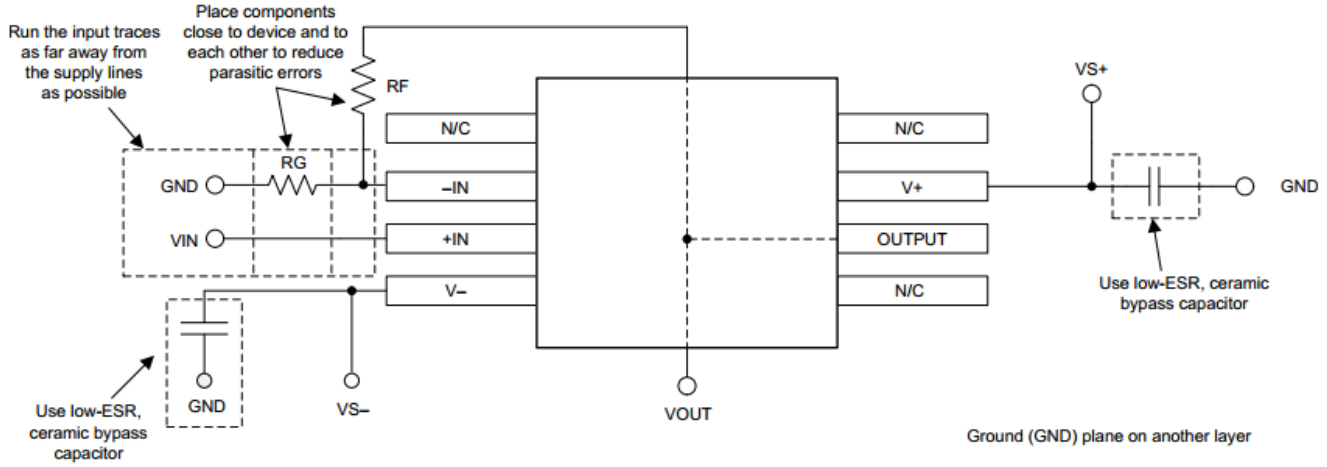


図 39. Operational Amplifier Board Layout for Noninverting Configuration

10.3 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. AB-039 *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads, and can be found at www.ti.com.

Power Dissipation (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

関連資料については、以下を参照してください。

- *『ADS8326 16ビット、高速、2.7V～5.5V、microPowerサンプリングA/Dコンバータ』*
- *『基板のレイアウト技法』*
- *『トランスインピーダンス・アンプの直感的な補正』*
- *『FilterPro™ユーザー・ガイド』*
- *『高速オペアンプの雑音解析』*
- *『OPA380およびOPA2380 高精度、高速トランスインピーダンス・アンプ』*
- *『OPA355、OPA2355、OPA3355 シャットダウン機能付き200MHz CMOSオペアンプ』*
- *『OPA656 広帯域、ユニティ・ゲイン安定、FET入力オペアンプ』*
- *『パワー・アンプのストレスと電力処理の制限』*
- *『放熱特性の優れたPowerPADパッケージ』*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

E2E is a trademark of Texas Instruments.
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11.5 静電気放電に関する注意事項

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3544QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	3544Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

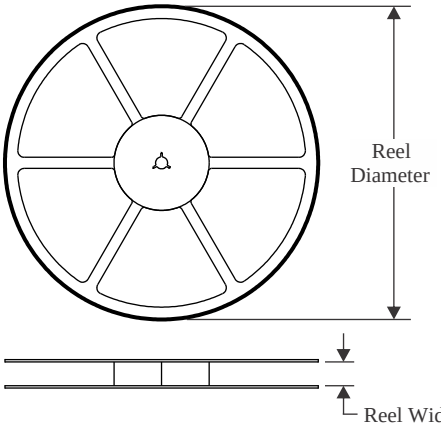
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

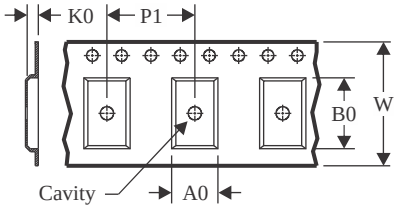
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

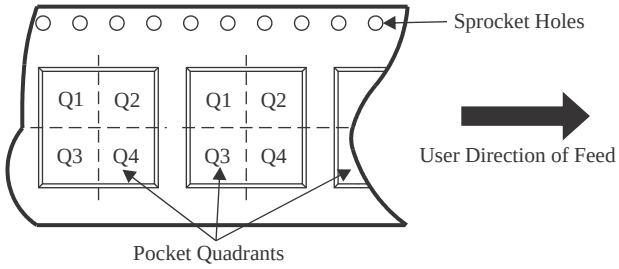


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

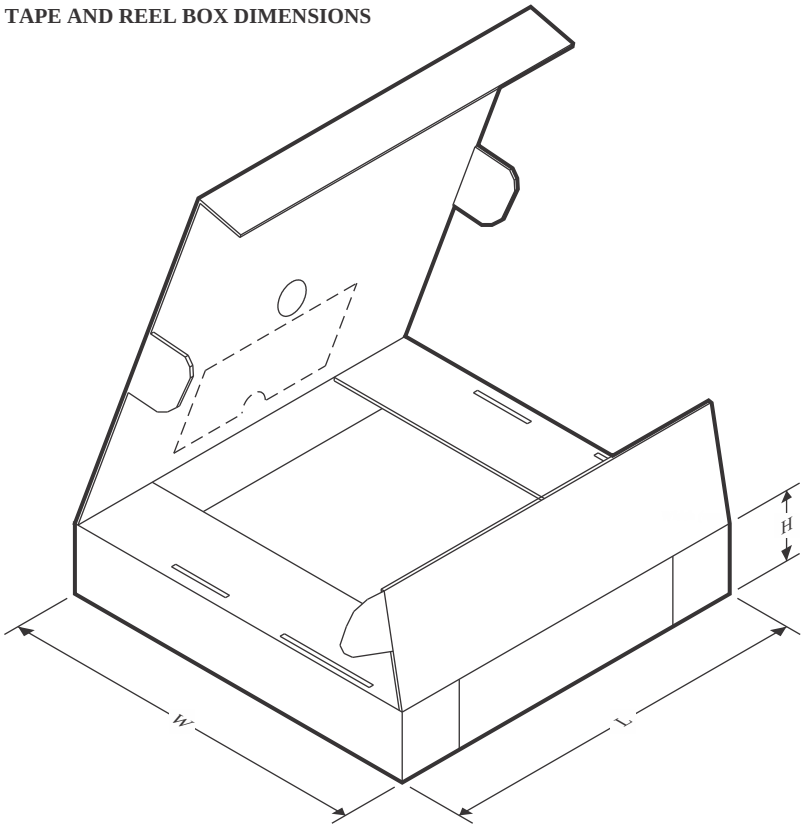
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3544QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

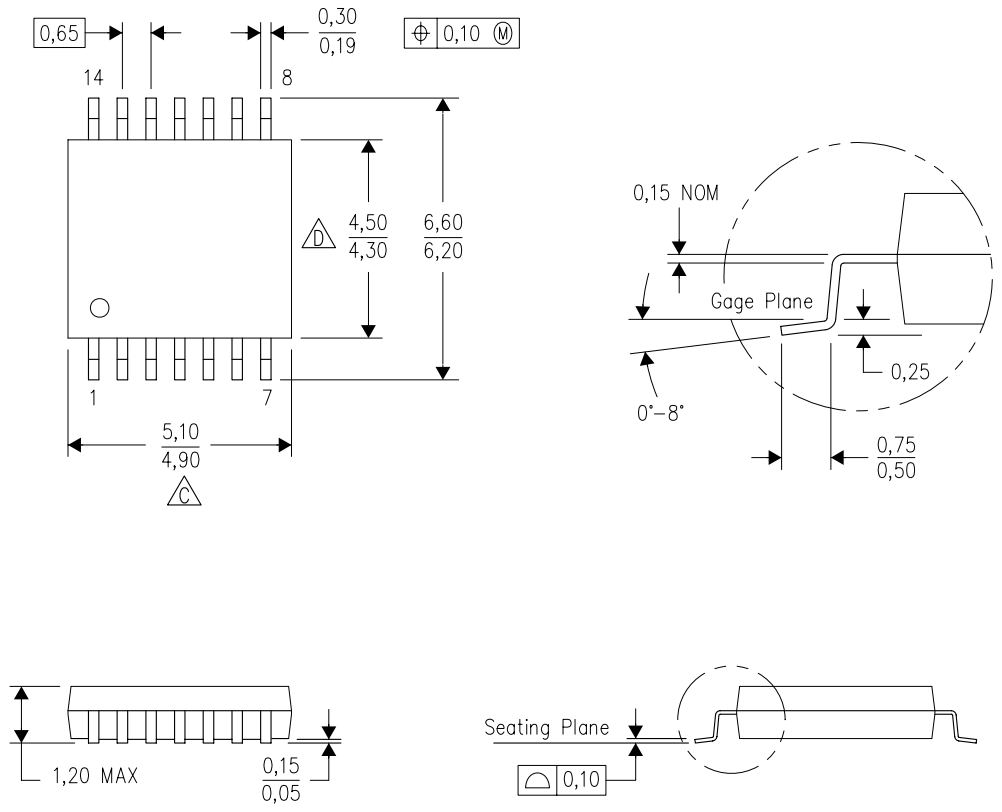
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3544QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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