TLV3604, TLV3605, TLV3607
JAJSJH6E – AUGUST 2020 – REVISED JULY 2023

TLV3604、TLV3605、TLV3607 800ps 高速レール・ツー・レール入力コンパレータ、LVDS 出力付き

1 特長

- 小さい伝搬遅延時間:800ps
- 小さいオーバードライブ分散:350ps
- 静止電流:12.1mA
- 高いトグル周波数:1.5GHz/3.0Gbps
- 狭パルス幅検出性能:600ps
- LVDS 出力
- 電源電圧範囲:2.4V～5.5V
- 両方のレールから 200mV 拡張された入力同相モード範囲
- 低い入力オフセット電圧:±5mV
- シングル・チャネルおよびデュアル・チャネル選択可能

2 アプリケーション

- LIDAR の距離センシング
- タイム・オブ・フライト (ToF) センサ
- オシロスコープとロジック・アナライザの高速トリガ機能
- 高速差動ライン・レシーバ
- ドローン・ビジョン

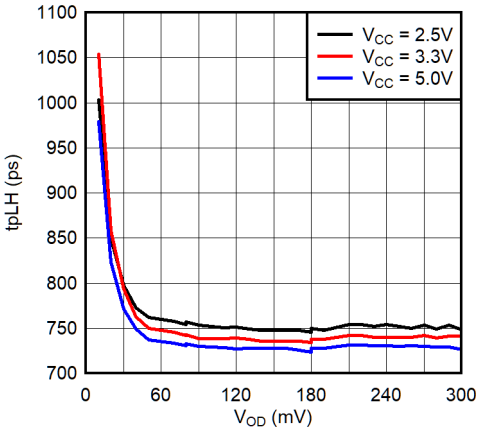
3 概要

TLV3604、TLV3605 (シングル・チャネル)、および TLV3607 (デュアル・チャネル) は、LVDS 出力とレール・ツー・レール入力を備えた 800ps の高速コンパレータです。これらの特長と、2.4V～5.5V の動作電圧範囲、3Gbps の高いトグル周波数により、LIDAR、クロック / データの回復アプリケーション、試験および測定システムに最適です。

また、TLV3604、TLV3605 および TLV3607 は、350ps の強力な入力オーバードライブ性能を有しており、わずか 600ps 幅の狭いパルスを検出できます。入力オーバードライブによって伝搬遅延の変動が小さいことと、狭いパルスを検出できることから、システム性能が向上し、タイム・オブ・フライト (ToF) アプリケーションの距離範囲が拡大します。

TLV3604、TLV3605、および TLV3607 の低電圧差動信号 (LVDS) 出力は、データ・スループットの向上と消費電力の最適化にも役立ちます。相補出力で各出力の同相ノイズを抑制することにより、EMI が低減されます。LVDS 出力は、高速 FPGA や CPU など、標準 LVDS 入力を受け入れる下流デバイスの直接駆動およびインターフェイスを可能にします。

TLV3604 は超小型の 6 ピン SC-70 パッケージで提供されているため、光学センサ・モジュールなどスペースの制約が厳しいアプリケーションを容易に実現できます。TLV3605 (シングル) および TLV3607 (デュアル) は TLV3604 と同じ性能を維持し、可変ヒステリシス制御、シャットダウン、ラッチ機能が 12 ピン QFN および 16 ピン WQFN パッケージで供給されるため、試験および測定アプリケーションに最適です。

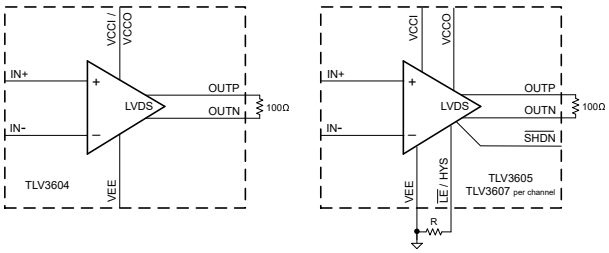


TpLH とオーバードライブ分散との関係

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TLV3604	SC70 (6)	1.25mm × 2.00mm
TLV3605	QFN (12)	3.00mm × 3.00mm
TLV3607	WQFN (16)	4.00mm × 4.00mm

1. 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (June 2021) to Revision E (July 2023) **Page**

- データシート全体にわたってデュアル・チャネル TLV3607 を追加 1

Changes from Revision C (April 2021) to Revision D (June 2021) **Page**

- Update Hysteresis Curve 15

Changes from Revision B (December 2020) to Revision C (April 2021) **Page**

- Updated Typical Performance Curves 9
- Updated Latch Functionality 14

Changes from Revision A (August 2020) to Revision B (December 2020) **Page**

- APL から RTM へのリリース 1

5 Pin Configuration and Functions

Pin Configurations: TLV3604 and TLV3605

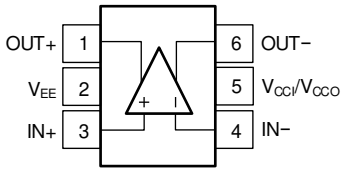


図 5-1. DCK Package
6-Pin SC70
Top View

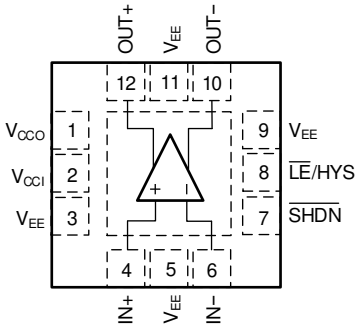


図 5-2. RVK Package
12-Pin QFN
Top View

表 5-1. Pin Functions: TLV3604 and TLV3605

PIN			I/O	DESCRIPTION
NAME	TLV3604	TLV3605		
IN+	3	4	I	Non-inverting input
IN–	4	6	I	Inverting input
OUT+	1	12	O	Non-inverting output
OUT–	6	10	O	Inverting output
V_{EE}	2	3, 5, 9, 11	I	Negative power supply
V_{CCI}	5	2	I	Positive input section power supply
V_{CCO}	5	1	I	Positive output section power supply
$\overline{SHDN}$	-	7	I	Shutdown control, active low
$\overline{LE}$/HYS	-	8	I	Adjustable hysteresis control and latch

5.1 Pin Configuration: TLV3607

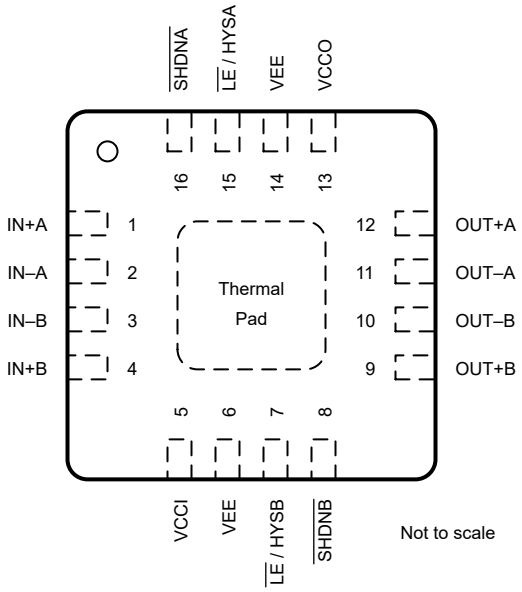


図 5-3. RTE Package
16-Pin WQFN with Exposed Thermal Pad
Top View

表 5-2. Pin Functions: TLV3607

PIN		I/O	DESCRIPTION
NAME	TLV3607		
IN+A	1	I	Channel A non-inverting input
IN–A	2	I	Channel A inverting input
IN–B	3	I	Channel B inverting input
IN+B	4	I	Channel B non-inverting input
OUT+A	12	O	Channel A non-inverting output
OUT–A	11	O	Channel A inverting output
OUT–B	10	O	Channel B inverting output
OUT+B	9	O	Channel B non-inverting output
V_{EE}	6, 14	I	Negative power supply
V_{CCI}	5	I	Positive input section power supply
V_{CCO}	13	I	Positive output section power supply
$\overline{SHDNA}$	16	I	Channel A shutdown control (active low)
$\overline{SHDNB}$	8	I	Channel B shutdown control (active low)
$\overline{LE}$/HYSA	15	I	Channel A latch enable (active low) and adjustable hysteresis control
$\overline{LE}$/HYSB	7	I	Channel B latch enable (active low) and adjustable hysteresis control

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input Supply Voltage: $V_{CCI} – V_{EE}$	–0.3	6	V
Output Supply Voltage: $V_{CCO} – V_{EE}$	–0.3	6	V
Supply Voltage Difference: $V_{CCI} – V_{CCO}$	–6	6	V
Input Voltage (IN+, IN–)(2)	V_{EE} – 0.3	V_{CCI} + 0.3	V
Differential Input Voltage (V_{DI} = IN+, IN–)	–(V_{CCI} + 0.3)	+(V_{CCI} + 0.3)	V
Output Voltage (OUT+, OUT–)(3)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Shutdown Enable ($\overline{SHDN}$)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Current into Input pins (IN+, IN–, $\overline{SHDN}$, $\overline{LE}$/HYS)(2)	–10	+10	mA
Current into Output pins (OUT+, OUT–)(3)	–10	+10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails or 6 V, whichever is lower, must be current-limited to 10 mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	TLV3604 Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		TLV3605, TLV3607 Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standaed ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Supply Voltage: $V_{CCI} – V_{EE}$	2.4	5.5	V
Output Supply Voltage: $V_{CCO} – V_{EE}$	2.4	5.5	V
Input Voltage Range (IN+, IN–)	V_{EE} – 0.3	V_{CCI} + 0.3	V
Shutdown Enable ($\overline{SHDN}$)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Latch and Hysteresis Control ($\overline{LE}$/HYS)	V_{EE} – 0.3	V_{CCO} + 0.3	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC		TLV3604 DCK (SC70) 6 PINS	TLV3605 RVK (WQFN) 12 PINS	TLV3607 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.3	85.8	72.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.5	71.6	53.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	15.1	35.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.3	52.7	45.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	43.7	4.1	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.1	52.7	45.9	°C/W

6.5 Electrical Characteristics (V_{CCI} = V_{CCO} = 2.5 V to 5 V)

V_{CCI} = V_{CCO} = 2.5 to 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, R_{LOAD} = 100 Ω, C_L = 1 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO} (1)	Input offset voltage	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	-5	±0.5	5	mV
V_{CM}	Input common mode voltage range	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	V_{EE} – 0.2		V_{CCI} + 0.2	V
V_{HYST}	Input hysteresis voltage			0		mV
C_{IN}	Input capacitance			1		pF
R_{DM}	Input differential mode resistance			67		kΩ
R_{CM}	Input common mode resistance			5		MΩ
I_B	Input bias current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	-5	-1	5	uA
I_{OS}	Input offset current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	-1		1	uA
CMRR (1)	Common-mode rejection ratio	V_{CCI} = V_{CCO} = 2.5 V and 5 V V_{CM} = V_{EE} – 0.2V to V_{CCI} + 0.2V, T_A = –40°C to +125°C	50	80		dB
PSRR (1)	Power-supply rejection ratio	V_{CCI} = V_{CCO} = 2.5 V to 5 V, T_A = –40°C to +125°C	55	80		dB
DC Output Characteristics						
V_{OCM}	Output common mode voltage	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	1.125	1.2	1.375	V
ΔV_{OCM}	Output common mode voltage mismatch	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			50	mV
V_{OCM_PP}	Peak-to-Peak output common mode voltage			20		mVpp
V_{OD}	Differential output voltage	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	250	350	450	mV
ΔV_{OD}	Differential output voltage mismatch	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			10	mV
Power Supply						
I_{CC} (TLV3604)	Total quiescent current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		12.1	16.5	mA
I_{CCI} (TLV3605)	Input stage quiescent current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		7.5	10.5	mA
I_{CCO} (TLV3605)	Output stage quiescent current	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		5.2	7.0	mA
I_{CCI} (TLV3607)	Input stage quiescent current per channel	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		7.5	10.5	mA
I_{CCO} (TLV3607)	Output stage quiescent current per channel	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C		5.2	7.0	mA
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		800		ps
t_{PD} (TLV3607 only)	Propagation delay	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		875		ps
t_{PD_SKEW}	Propagation delay skew	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		40		ps
Δt_{PD} (TLV3607 only)	Channel-to-channel propagation delay skew(2)	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV, 50 MHz Squarewave		10		ps
$t_{CM\_DISPERSION}$	Common dispersion	V_{CM} varied from V_{EE} to V_{CCI}		200		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 250 mV		350		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Underdrive varied from 10mV to 250 mV		200		ps
t_R	Rise time	20% to 80%		350		ps

6.5 Electrical Characteristics (V_{CCI} = V_{CCO} = 2.5 V to 5 V) (continued)

V_{CCI} = V_{CCO} = 2.5 to 5 V, V_{EE} = 0 V, V_{CM} = V_{EE} + 300 mV, R_{LOAD} = 100 Ω, C_L = 1 pF probe capacitance, typical at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_F	Fall time	80% to 20%		350		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		1.5		GHz
TR	Toggle rate	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		3.0		Gbps
f_{TOGGLE} (TLV3607 only)	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		1.2		GHz
TR (TLV3607 only)	Toggle rate	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		2.4		Gbps
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		600		ps
Latching/Adjustable Hysteresis (TLV3605 and TLV3607)						
V_{HYST}	Input hysteresis voltage	R_{HYST} = Floating		0		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 150 kΩ		30		mV
V_{HYST}	Input hysteresis voltage	R_{HYST} = 56 kΩ		60		mV
V_{IH_LE}	$\overline{LE}$ pin input high level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	1.5			V
V_{IL_LE}	$\overline{LE}$ pin input low level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			0.35	V
I_{IH_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{CCO} T_A = –40°C to +125°C			3.5	uA
I_{IL_LE}	$\overline{LE}$ pin input leakage current	V_{LE} = V_{EE}, T_A = –40°C to +125°C			40	uA
t_{SETUP}	Latch setup time			–3		ns
t_{HOLD}	Latch hold time			6		ns
t_{PL}	Latch to Q and $\overline{Q}$ delay			4		ns
Shutdown Characteristics (TLV3605 and TLV3607)						
V_{IH_SD}	$\overline{SHDN}$ pin input high level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C	1.5			V
V_{IL_SD}	$\overline{SHDN}$ pin input low level	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			0.4	V
I_{IH_SD}	$\overline{SHDN}$ pin input leakage current	V_{CCI} = V_{CCO} = 2.5 V and 5 V V_{SD} = V_{CCO}, T_A = –40°C to +125°C			2	uA
I_{IL_SD}	$\overline{SHDN}$ pin input leakage current	V_{CCI} = V_{CCO} = 2.5 V and 5 V V_{SD} = V_{EE}, T_A = –40°C to +125°C			30	uA
I_{CCI_SD}	Input stage quiescent current per channel in Shutdown mode	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			1.5	mA
I_{CCO_SD}	Output stage quiescent current per channel in Shutdown mode	V_{CCI} = V_{CCO} = 2.5 V and 5 V T_A = –40°C to +125°C			100	uA
t_{SLEEP}	Sleep time from Active to Shutdown mode	10% output swing		8		ns
t_{WAKEUP}	Wake up time from Shutdown mode	V_{OD} = 50 mV, output valid		100		ns

(1) For TLV3605 and TLV3607, the V_{IO} is tested with R_{HYST} = 150 KΩ
(2) Differential propagation delay is defined as the larger of the two:
ΔtPDLH = tPDLH(MAX) – tPDLH(MIN)
ΔtPDHL = tPDHL(MAX) – tPDHL(MIN)
where (MAX) and (MIN) denote the maximum and minimum values of a given measurement across the different comparator channels.

6.6 Typical Characteristics

At T_A = 25°C, V_{CCI}/V_{CCO} = 2.5 V to 5.0 V, V_{CM} = 0.3V, and input overdrive/underdrive = 50 mV unless otherwise noted.

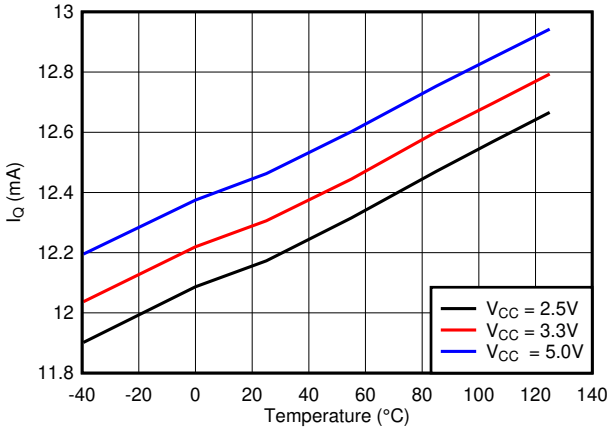


図 6-1. I_Q vs Temperature

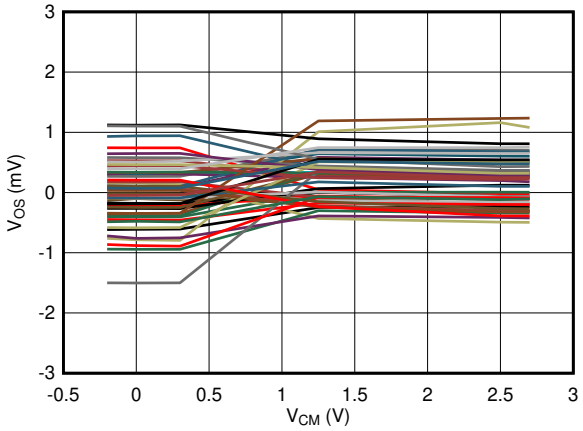


図 6-2. V_{OS} vs V_{CM} @ V_{CC} =2.5V - 50 Devices

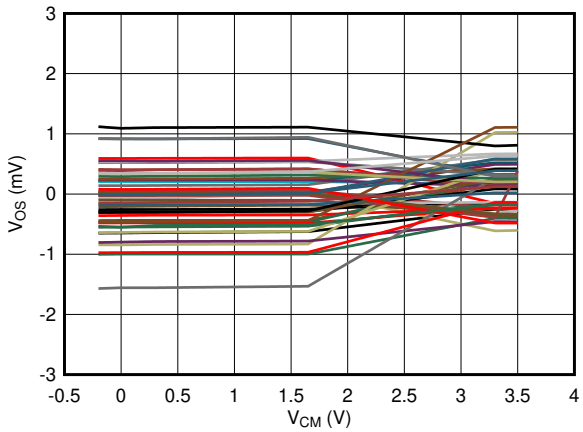


図 6-3. V_{OS} vs V_{CM} @ V_{CC} =3.3V - 50 Devices

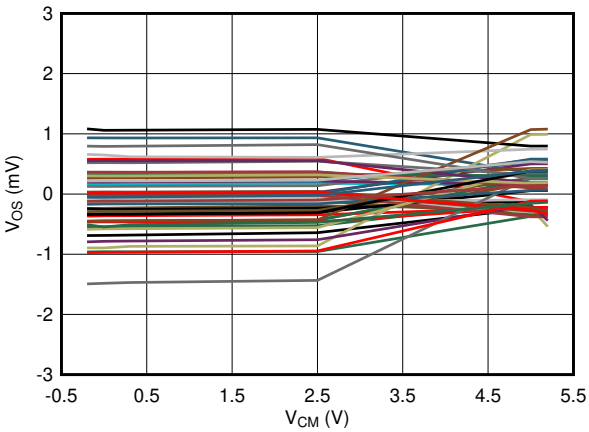


図 6-4. V_{OS} vs V_{CM} @ V_{CC} =5.0V - 50 Devices

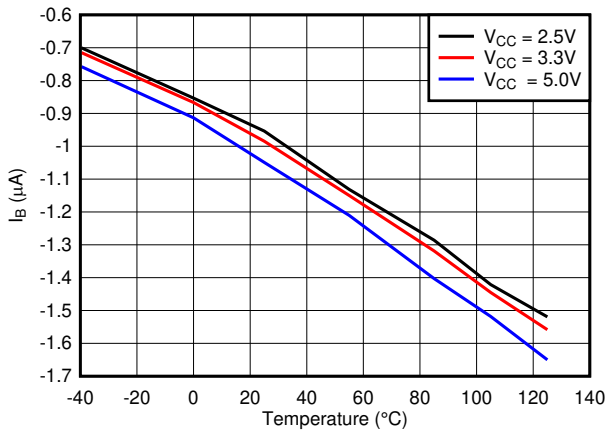


図 6-5. Bias Current vs Temperature

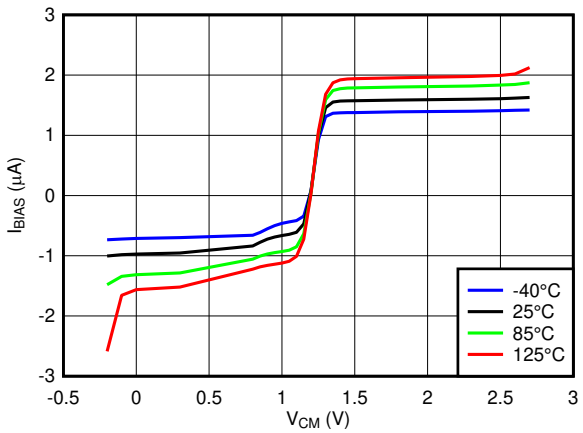


図 6-6. Input Bias Current vs V_{CM} @ VCC = 2.5V

6.6 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI}/V_{CCO} = 2.5 V to 5.0 V, V_{CM} = 0.3V, and input overdrive/underdrive = 50 mV unless otherwise noted.

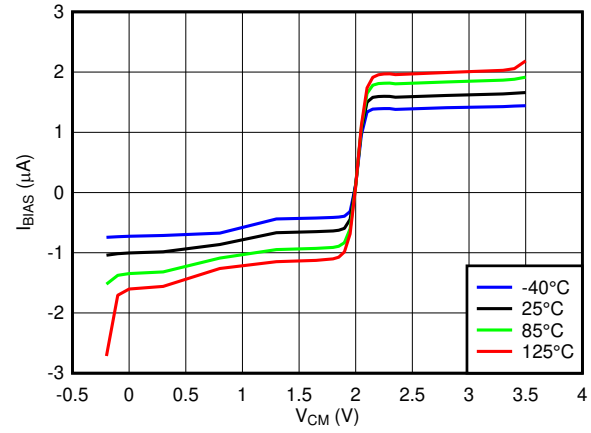


図 6-7. Input Bias Current vs V_{CM} @ VCC = 3.3V

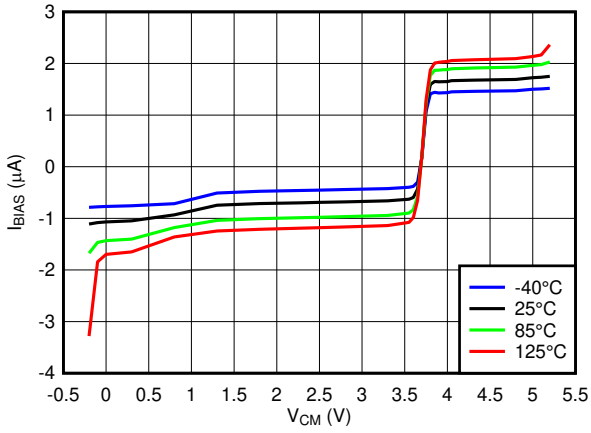


図 6-8. Input Bias Current vs V_{CM} @ VCC = 5.0V

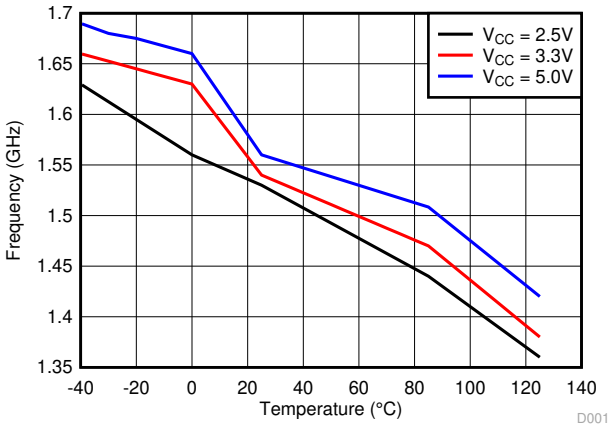


図 6-9. FToggle vs Temperature

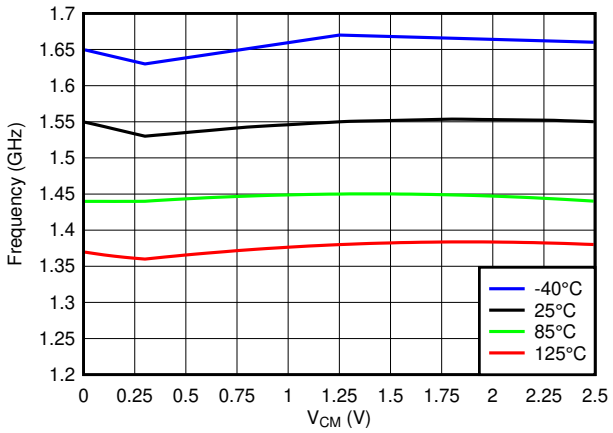


図 6-10. Ftoggle vs V_{CM} @ VCC = 2.5V

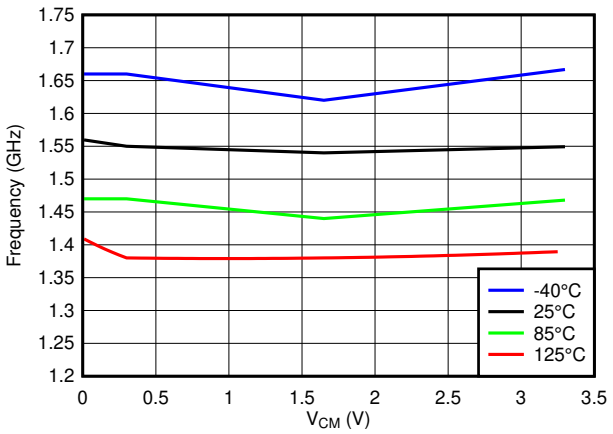


図 6-11. Ftoggle vs V_{CM} @ VCC = 3.3V

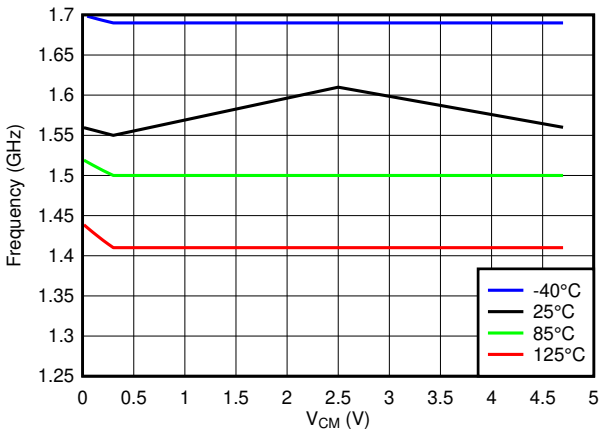


図 6-12. Ftoggle vs V_{CM} @ VCC = 5.0V

6.6 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI}/V_{CCO} = 2.5 V to 5.0 V, V_{CM} = 0.3V, and input overdrive/underdrive = 50 mV unless otherwise noted.

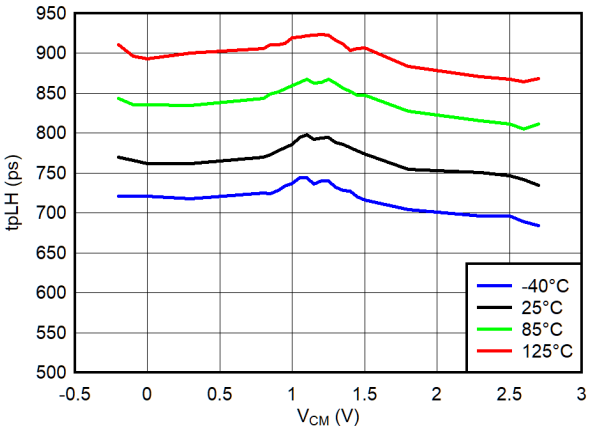


図 6-13. T_{PLH} vs V_{CM} @ VCC = 2.5V

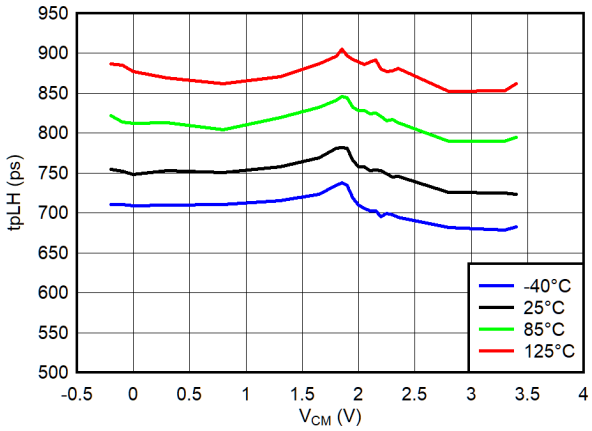


図 6-14. T_{PLH} vs V_{CM} @ VCC = 3.3V

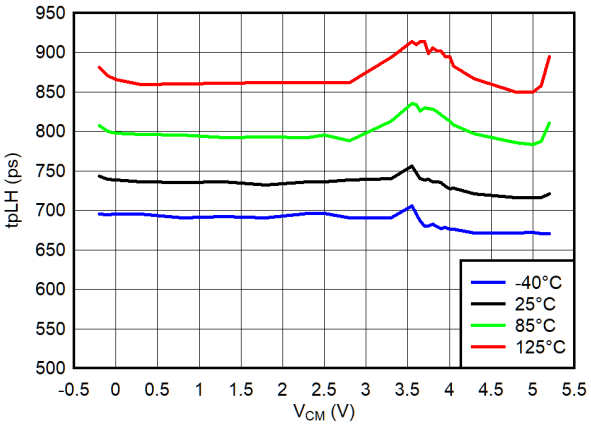


図 6-15. T_{PLH} vs V_{CM} @ VCC = 5.0V

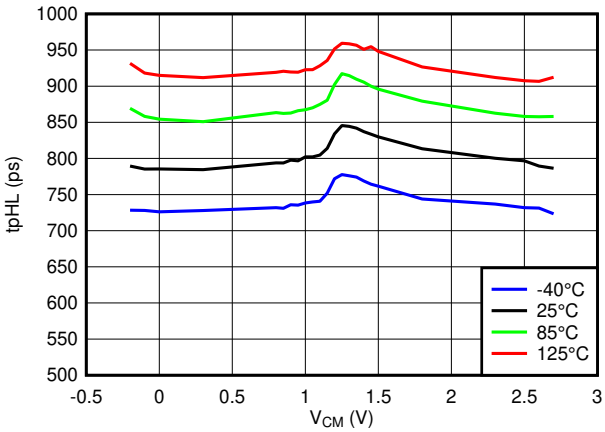


図 6-16. T_{PHL} vs V_{CM} @ VCC = 2.5V

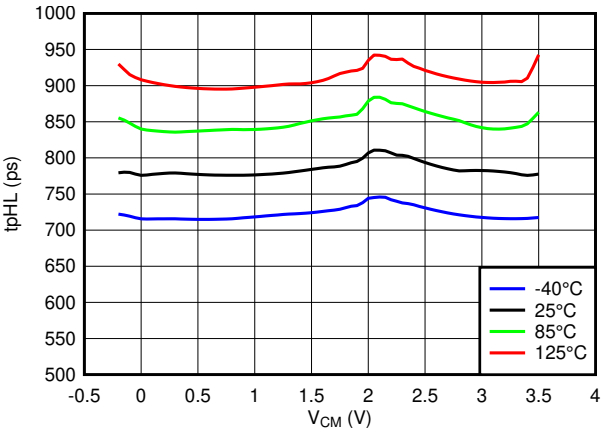


図 6-17. T_{PHL} vs V_{CM} @ VCC = 3.3V

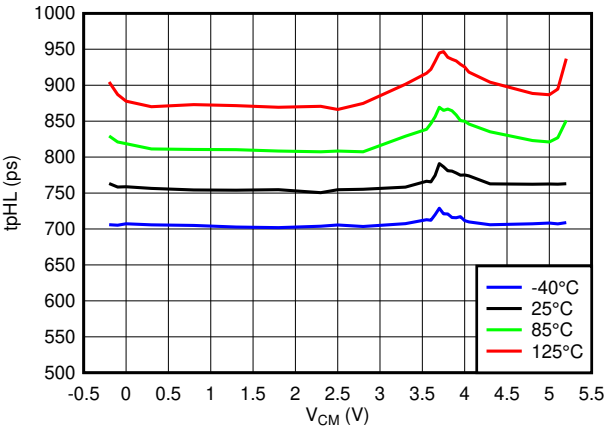


図 6-18. T_{PHL} vs V_{CM} @ VCC = 5.0V

6.6 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI}/V_{CCO} = 2.5 V to 5.0 V, V_{CM} = 0.3V, and input overdrive/underdrive = 50 mV unless otherwise noted.

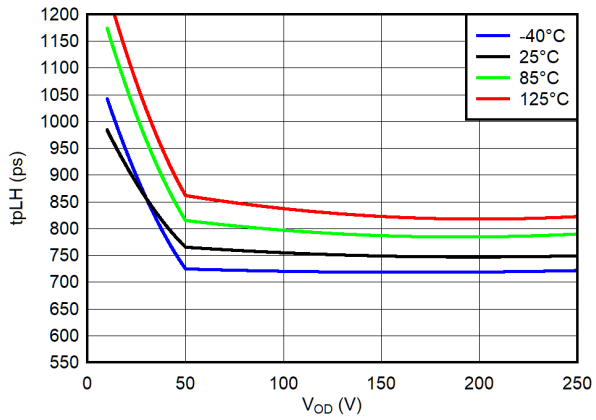


図 6-19. T_{PLH} vs Input Overdrive @ VCC = 2.5V

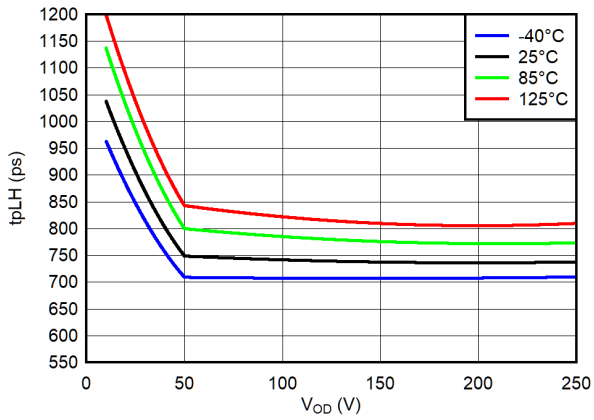


図 6-20. T_{PLH} vs Input Overdrive @ VCC = 3.3V

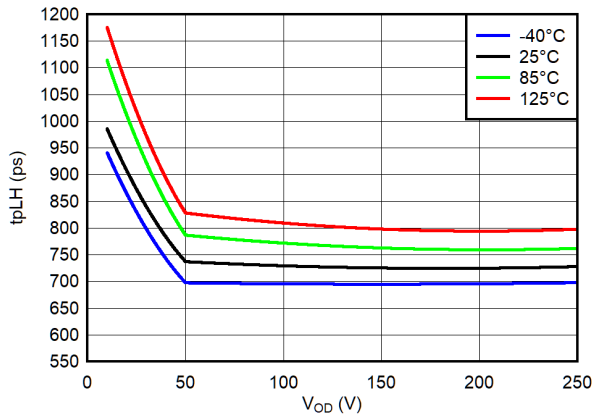


図 6-21. T_{PLH} vs Input Overdrive @ VCC = 5.0V

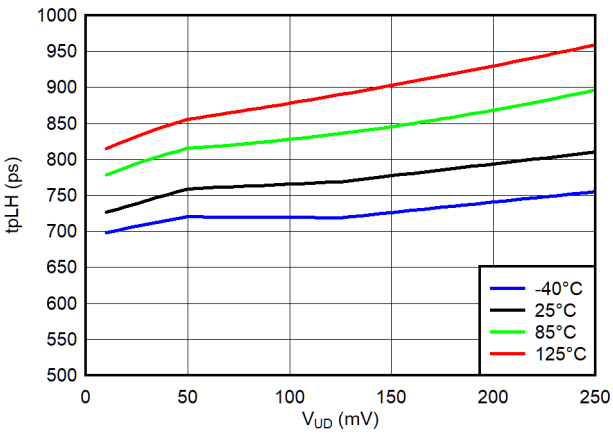


図 6-22. T_{PLH} vs Input Underdrive @ VCC = 2.5V

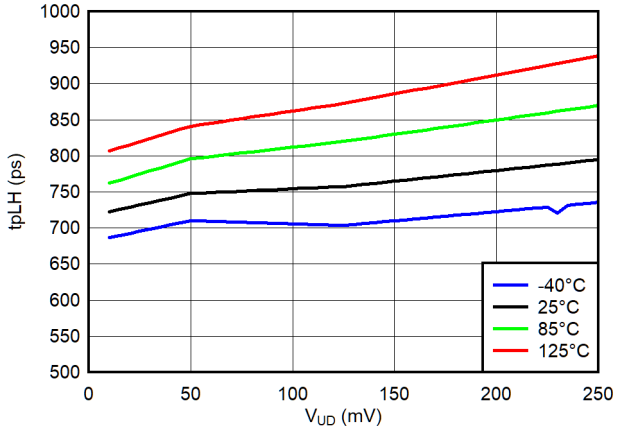


図 6-23. T_{PLH} vs Input Underdrive @ VCC = 3.3V

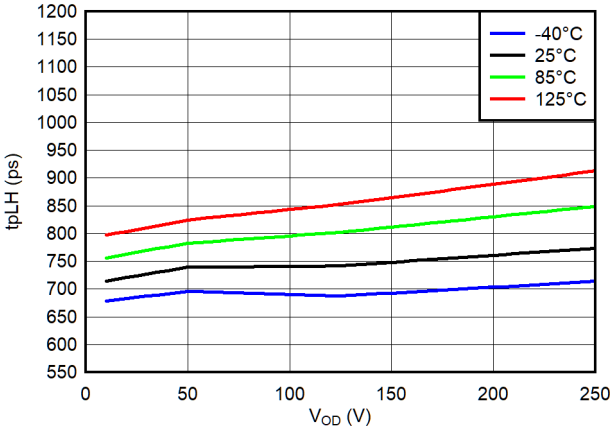


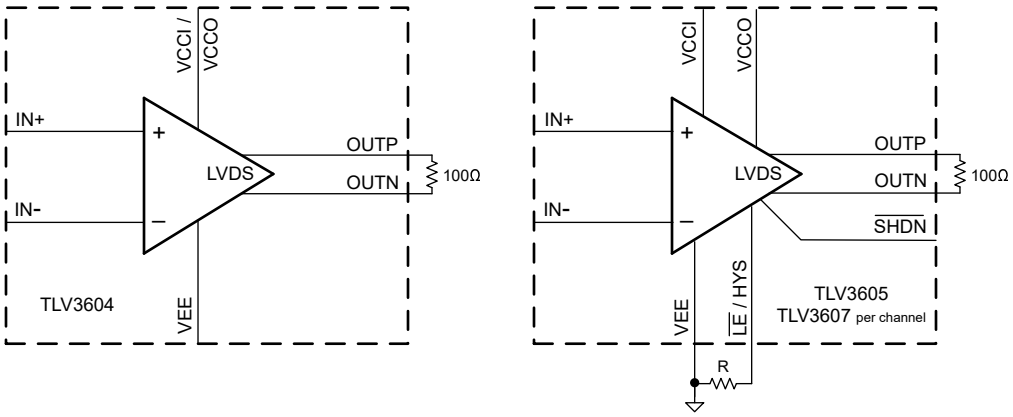
図 6-24. T_{PLH} vs Input Underdrive @ VCC = 5.0V

7 Detailed Description

7.1 Overview

The TLV3604 and TLV3605 are 800-ps, high-speed comparators with LVDS outputs and rail-to-rail inputs. These features, along with an operating voltage range of 2.4 V to 5.5 V and a high toggle frequency of 3 Gbps, make the TLV3604 and TLV3605 well suited for LIDAR, clock and data recovery applications, and test and measurement systems.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3604 and TLV3605 (single channel) and TLV3607 (dual channel) are high-speed comparators with rail-to-rail inputs and LVDS outputs. The rail-to-rail input stage is capable of operating up to 200 mV beyond each power supply rail with minimal input offset. The TLV3605 (single) and TLV3607 (dual) have similar performance as the TLV3604 while providing adjustable hysteresis, latching function, and shutdown mode.

7.4 Device Functional Modes

The TLV3604 has a single functional mode and is operational when the power supply voltage is greater than the minimum operating voltage. On the other hand, the TLV3605 and TLV3607 have an active and shutdown mode. The TLV3605 and TLV3607 are in shutdown mode when the $\overline{\text{SHDN}}$ pin is logic low. To allow for easy interface with 1.8V FPGAs and CPUs, the $\overline{\text{SHDN}}$ pin is 1.8 V logic compliant and independent of the comparator power supply.

7.4.1 Rail-to-Rail Inputs

The TLV3604, TLV3605, and TLV3607 feature input stages capable of operating 200mV below or above the power supply rails, allowing for zero cross detection and maximizing input dynamic range. With low input offset voltage, the comparators improve system performance in high sensitivity signal detection.

7.4.2 LVDS Output

The TLV3604, TLV3605, and TLV3607 outputs are LVDS compliant. When the input of the downstream device is terminated with a 100 Ω resistor, it provides a ±350 mV LVDS swing. Fully differential outputs enable fast digital toggling and reduce EMI compared to single-ended output standards.

8 Application and Implementation

注

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8.1 Application Information

The TLV3604, TLV3605, and TLV3607 comparators feature rail-to-rail inputs and a LVDS output stage that is well-suited for high speed applications that require low power consumption. The 800 ps propagation delay of the comparators improve performance and extend the range for applications involving optical reception, triggers for test and measurement systems, and transceivers that require a high speed signal to be carried over a certain distance.

8.1.1 Comparator Inputs

The TLV3604, TLV3605, and TLV3607 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies.

8.1.2 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay. However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.3 Latch Functionality

The latch pin for the TLV3605 and TLV3607 holds the output state of the device when the voltage at the LEB/HYST pin is less than 800mV above V_{EE}. This is particularly useful when the output state is intended to remain unchanged. An important consideration of the latch functionality is the latch hold time. Latch hold time is the minimum time (after the latch pin is asserted) required for properly latching the comparator output.

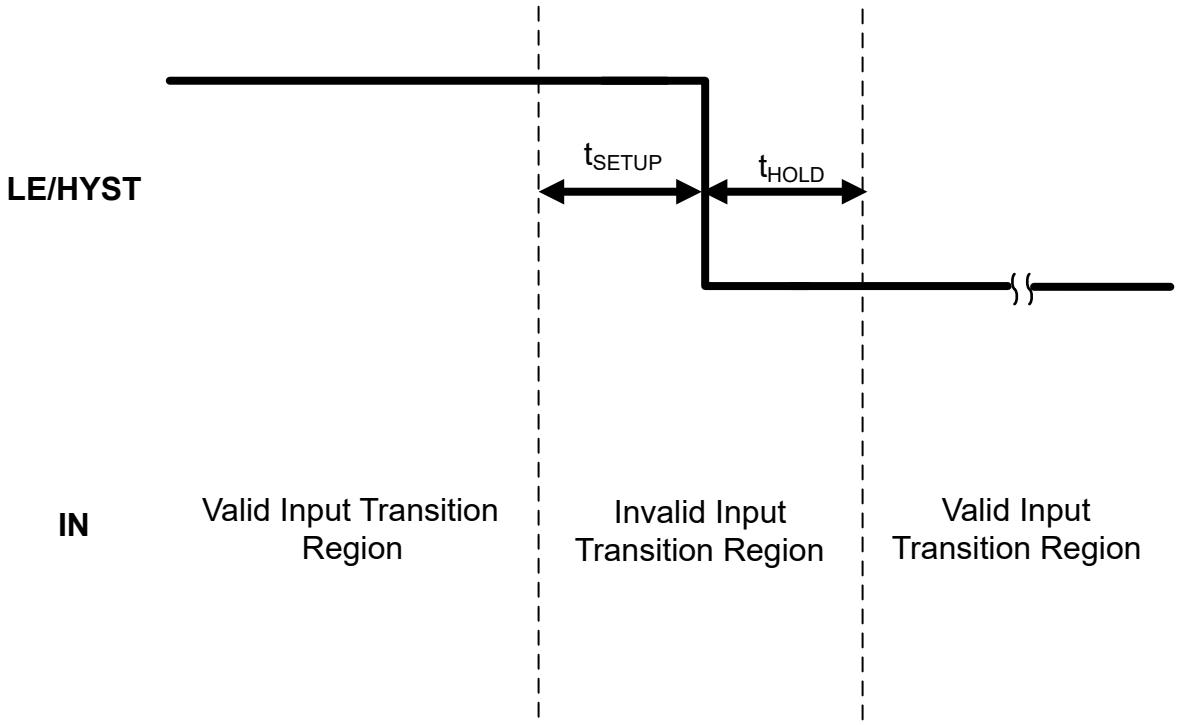

図 8-1. Valid Latch Diagram

Likewise, latch setup time is defined as the time that the input must be stable before the latch pin is asserted low. The figure above illustrates when the input can transition for a valid latch. Note that the typical setup time in the EC table is negative; this is due to the internal trace delays of the LEB/HYST pin relative to the input pin trace delays.

A small delay in the output response is shown below when the TLV3605 and TLV3607 exits a latched output stage.

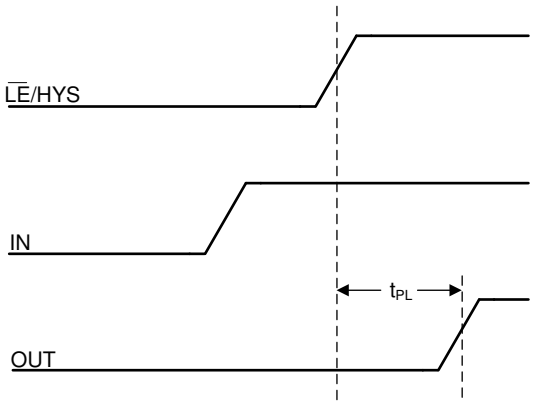

図 8-2. Latch Disable with Input Change

8.1.4 Adjustable Hysteresis

As a result of a comparator's high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between "logic high" and "logic low" states. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise.

These challenges can be overcome by adding hysteresis to the comparator. Since the TLV3604 does not have internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the Typical Application section for more details.

The TLV3605 and TLV3607 on the other hand has a LEB/HYST pin that can be used to increase the internal hysteresis of the comparator. In order to change the internal hysteresis of the TLV3605 and TLV3607, connect a single resistor as shown in the adjusting hysteresis figure between the LEB/HYST pin and VEE. A curve of hysteresis versus resistance is provided below to provide guidance in setting the desired amount of hysteresis.

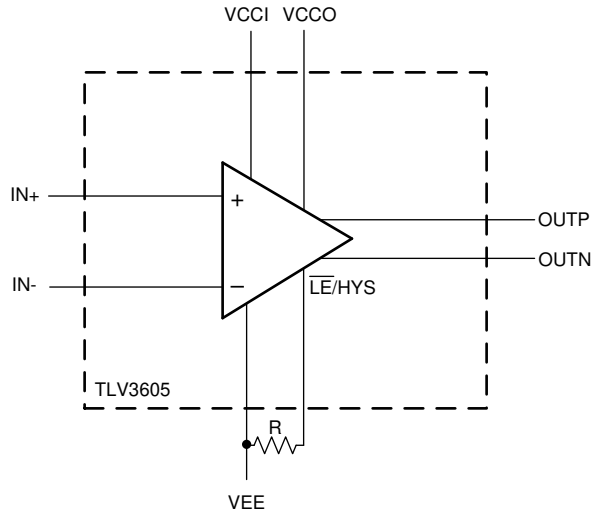

図 8-3. Adjusting Hysteresis with an External Resistor (R)

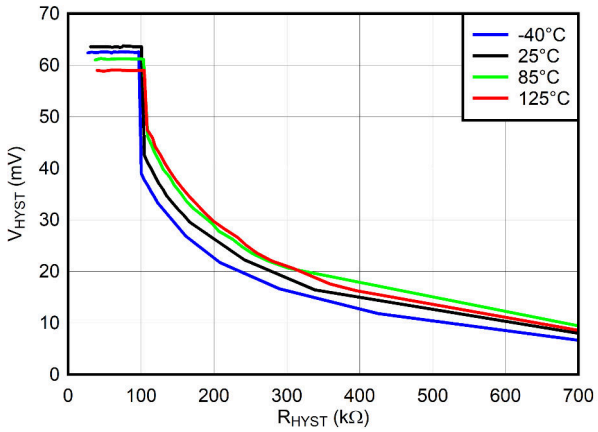

図 8-4. V_{HYST} (mV) vs R_{HYST} (kΩ), V_{CC} = 3.3V

8.2 Typical Application

8.2.1 Non-Inverting Comparator With Hysteresis

A way to implement external hysteresis to the TLV3604 is to add two resistors to the circuit: one in series between the reference voltage and the inverting pin, and another from the inverting pin to one of the differential output pins.

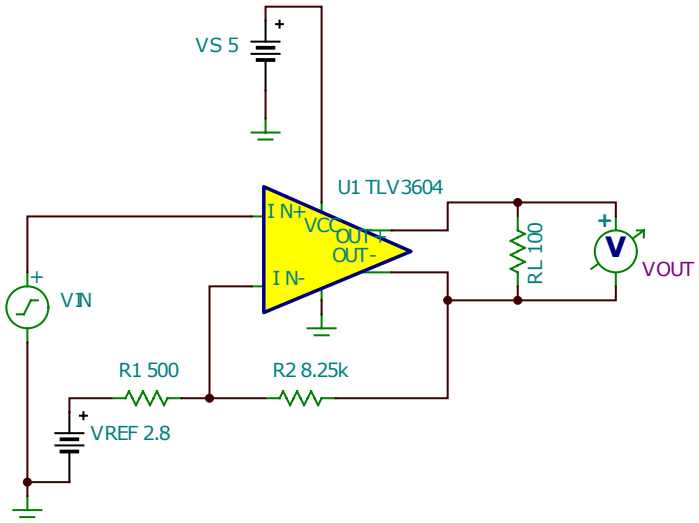

図 8-5. Non-Inverting Comparator with Hysteresis Circuit

8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
V_{HYS}	20mV
V_{REF}	5V
V_{T1}	3.6V
V_{T2}	3.4V
Q	1.375V
$\overline{Q}$	1.025V

8.2.1.2 Detailed Design Procedure

First, create an equation for V_T that covers both output voltages when the output is high or low.

$$V_{INN\_LOW} = V_{REF} - (V_{REF} - V_{OL}) \times R_1 / (R_1 + R_2) \quad (1)$$

$$V_{INN\_HI} = V_{REF} - (V_{REF} - V_{OH}) \times R_1 / (R_1 + R_2) \quad (2)$$

The hysteresis voltage in this network is equal to the difference in the two threshold voltage equations.

$$V_{HYS} = V_{INN\_HI} - V_{INN\_LOW} \quad (3)$$

$$\text{After simplifying: } V_{HYS} = (V_{OH} - V_{OL}) \times R_1 / (R_1 + R_2) \quad (4)$$

Since input bias is typically 1 µA, it is best to choose a value for R_1 and then solve for the required R_2 to provided the needed amount of hysteresis. In this example, a value of 500 Ω was selected to minimize the impact of input bias current on circuit offset voltage. Solving for R_2 provides the equation below. Note that VOD is 350 mV from the EC Table.

$$R_2 = R_1 \times (V_{OD} - V_{HYS}) / V_{HYS} \quad (5)$$

VREF can now be solved for using the equation for VINN_LOW or VINN_HI. IN this example, VINN_HI was chosen.

$$V_{REF} = (V_{INN\_HI} - k \times V_{OH}) / (1 - k) \text{ where } k = R_1 / (R_1 + R_2) \quad (6)$$

The external hysteresis design is now complete with R_1 = 500 Ω, R_2 = 8.25 kΩ, V_{REF} = 2.8 V.

8.2.1.3 Application Performance Plots

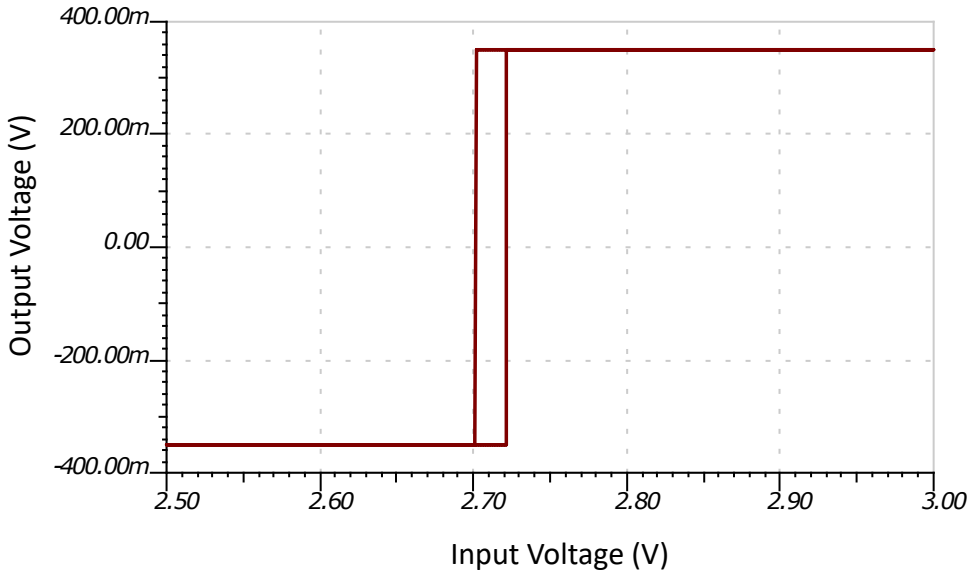

図 8-6. Hysteresis Curve for LVDS Comparator

8.2.2 Optical Receiver

The TLV3604, TLV3605, and TLV3607 can be used in conjunction with a high performance amplifier such as the OPA855 to create an optical receiver as shown in the 図 8-7. The photo diode is connected to a bias voltage and is being driven with a pulsed laser. The OPA855 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The TLV3604, TLV3605, and TLV3607 will then output the proper LVDS signal according to the threshold set (V_{REF2}).

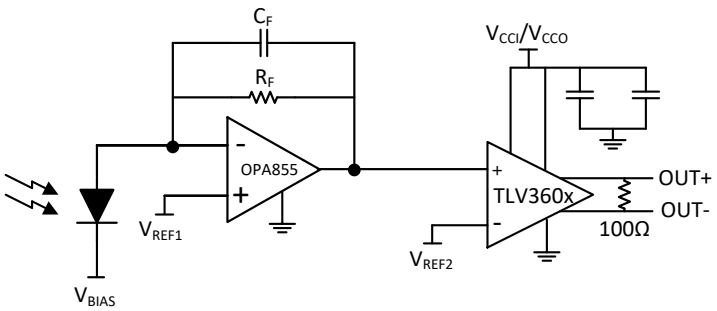

図 8-7. Optical Receiver

8.2.3 Logic Clock Source to LVDS Transceiver

The 図 8-8 shows a logic clock source being terminated and driven with the TLV3604, TLV3605, and TLV3607 across a CAT6 Cable to receive an equivalent LVDS clock signal at the receiver end.

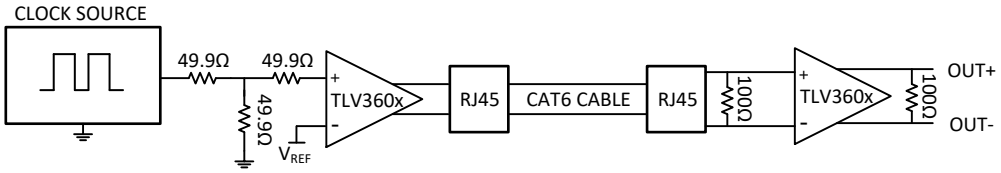

図 8-8. LVDS Clock Transceiver

8.2.4 External Trigger Function for Oscilloscopes

図 8-9 is a typical configuration for creating an external trigger on oscilliscopes. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV360x can use as a reference. The input voltage from an oscilloscope channel is then compared to the trigger reference voltage, and the TLV3604, TLV3605, and TLV3607 sends an LVDS signal to a downstream FPGA to begin a capture.

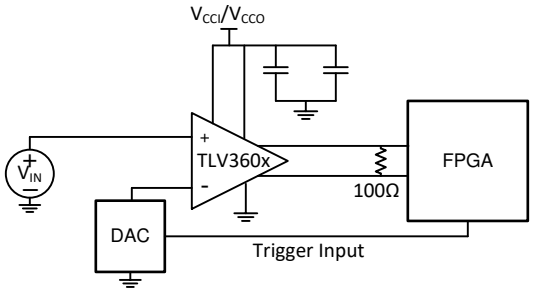

図 8-9. External Trigger Function

9 Power Supply Recommendations

The TLV3604, TLV3605, and TLV3607 are recommended for operation from 2.4 V to 5.5 V. One benefit of the TLV3605 and TLV3607 is that the comparator has separate input and output supply pins (VCCI and VCCO). This provides a system designer the flexibility of powering the input stage with a higher supply voltage such as 5V to maximize the dynamic range of the input while powering the output stage with a 2.5V supply to save power. Regardless of the VCCO supply voltage, the control pins such as LEB and SHDNB are 1.8V logic compliant.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance and input/output trace impedances.
2. To minimize supply noise, place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) directly between VCCI/VCCO and VEE.
3. On the inputs and outputs, utilize matched trace lengths to minimize timing skew. Also, minimize trace lengths and maximize ground pour spacings around the input and output traces to limit parasitic capacitance.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes minimal degradation to propagation delay when source impedance is low.
6. Use a 100 Ω termination resistor across the device's LVDS outputs.
7. Use higher performance substrate materials such as Rogers or High-Speed FR4.
8. PCB signal layers from the TLV3604EVM are shown for reference.

10.2 Layout Example

Figure 10-1 shows the 4 layer PCB signal routing for the TLV3604EVM as an example for how layout on this device can be done.

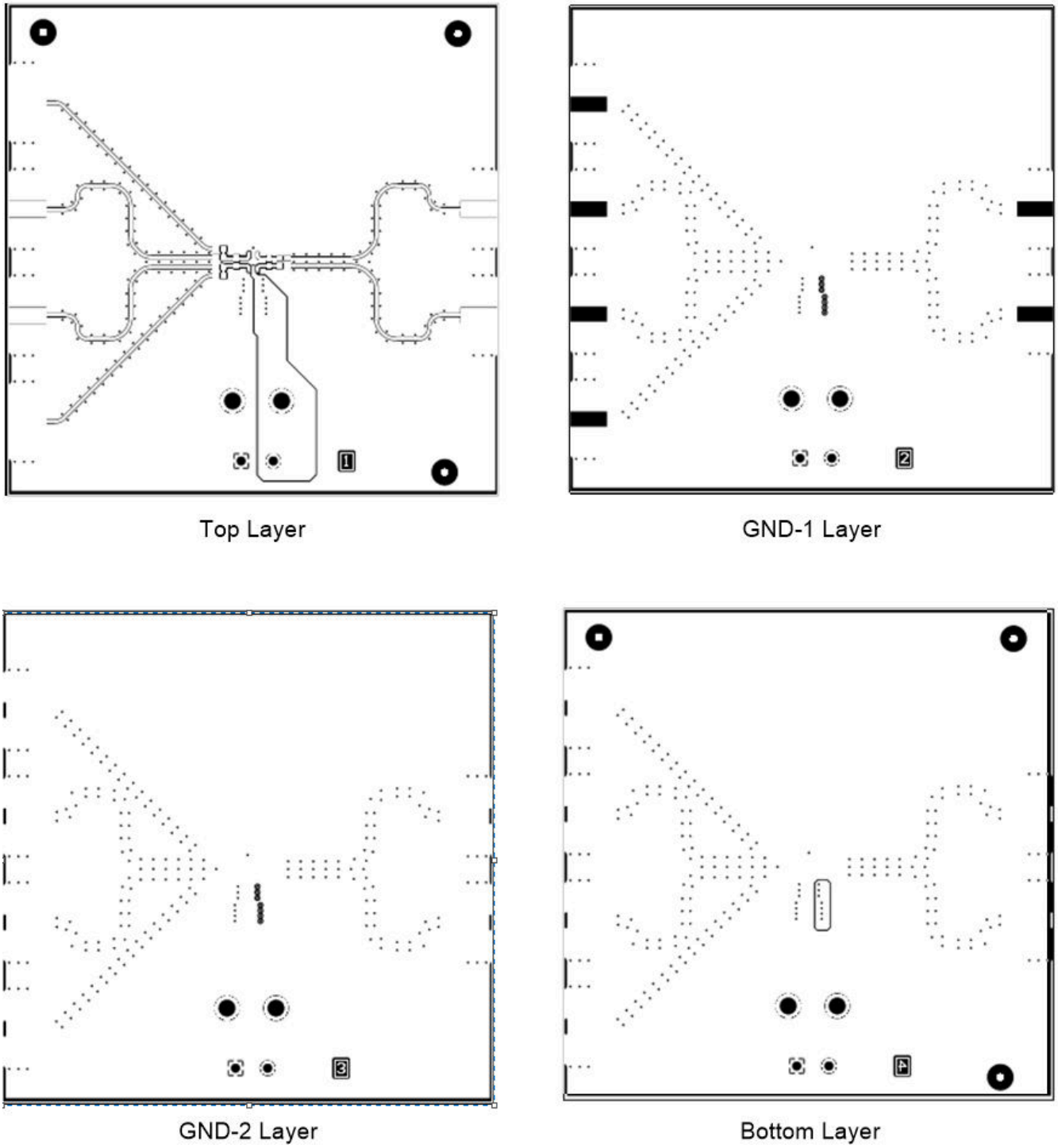

図 10-1. TLV3604EVM Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

11.2 ドキュメントの更新通知を受け取る方法

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11.3 サポート・リソース

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3604DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HF	Samples
TLV3604DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HF	Samples
TLV3605RVKR	ACTIVE	WQFN	RVK	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3605	Samples
TLV3605RVKT	ACTIVE	WQFN	RVK	12	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3605	Samples
TLV3607RTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL3607	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

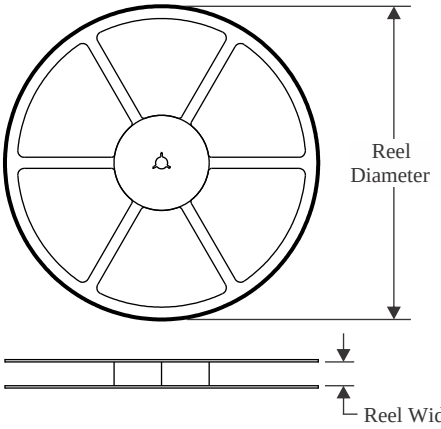
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

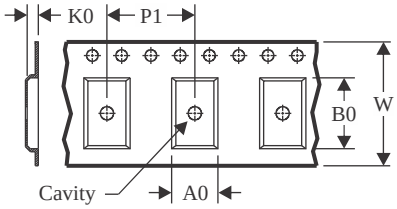
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

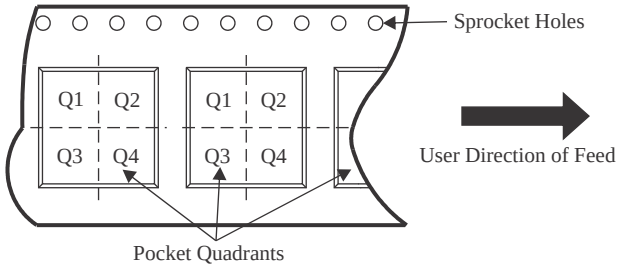


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

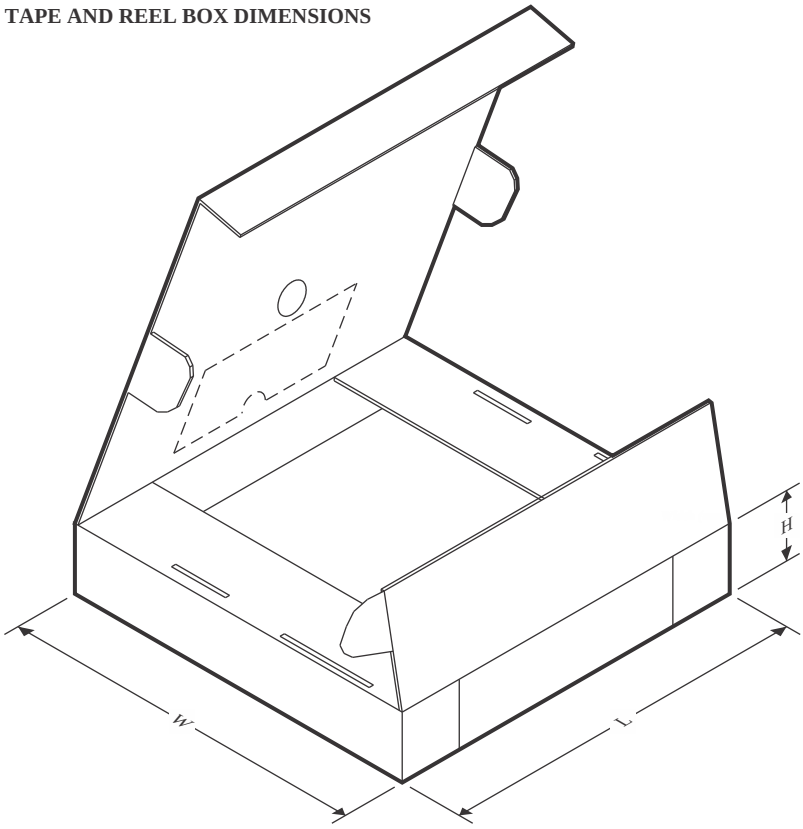
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3604DCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TLV3604DCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TLV3605RVKR	WQFN	RVK	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV3605RVKT	WQFN	RVK	12	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV3607RTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

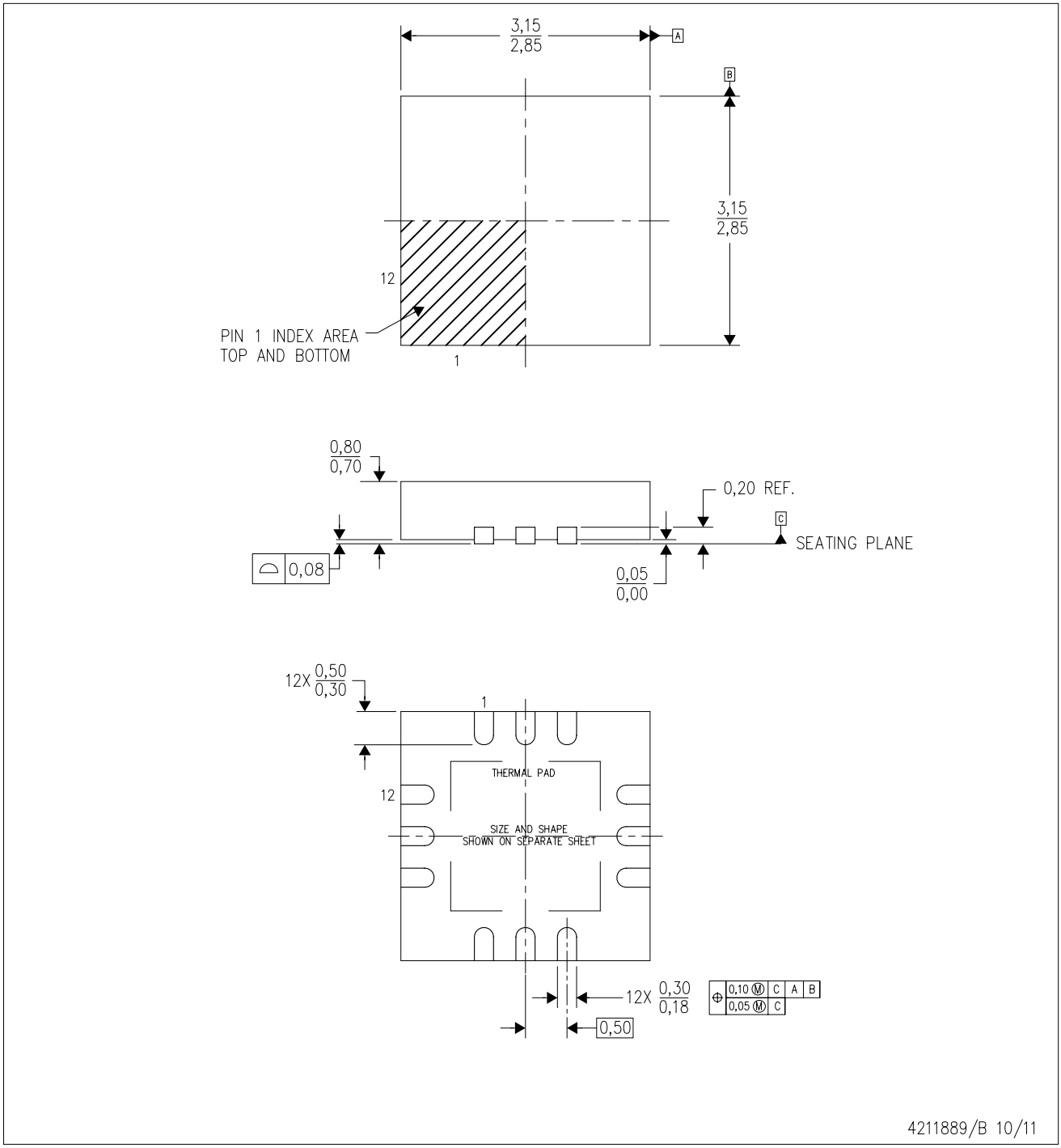
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3604DCKR	SC70	DCK	6	3000	183.0	183.0	20.0
TLV3604DCKT	SC70	DCK	6	250	183.0	183.0	20.0
TLV3605RVKR	WQFN	RVK	12	3000	367.0	367.0	35.0
TLV3605RVKT	WQFN	RVK	12	250	210.0	185.0	35.0
TLV3607RTER	WQFN	RTE	16	5000	367.0	367.0	35.0

RVK (S–PWQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



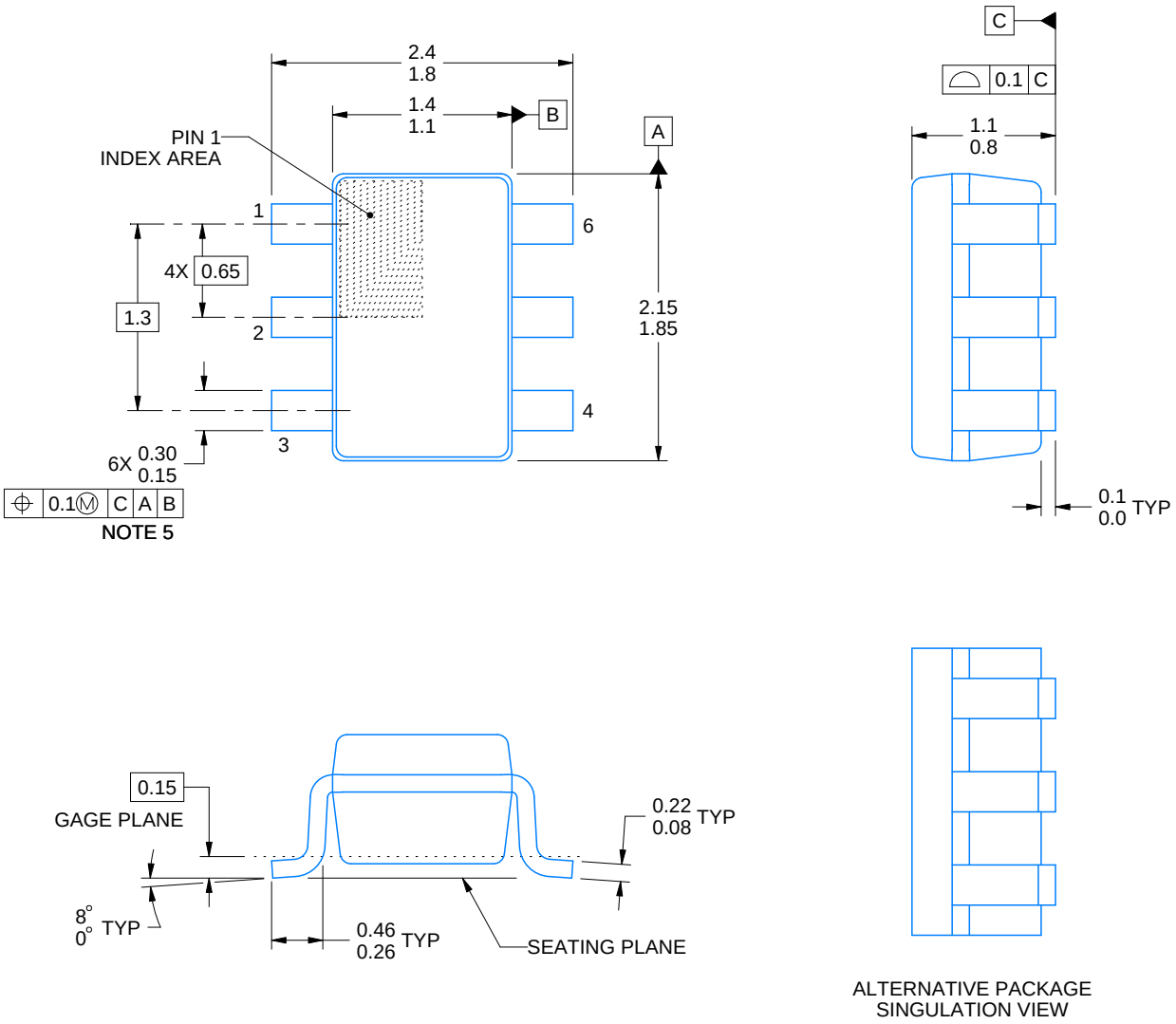
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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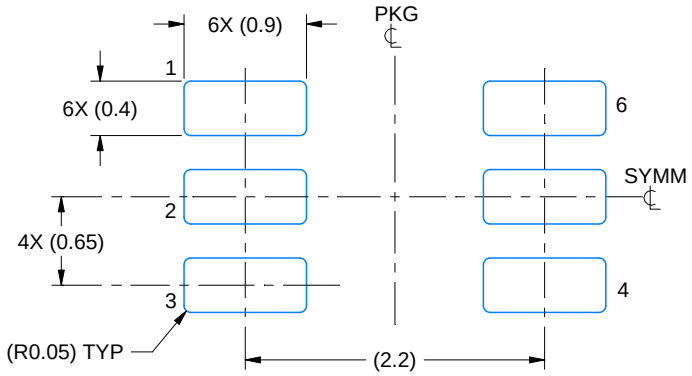
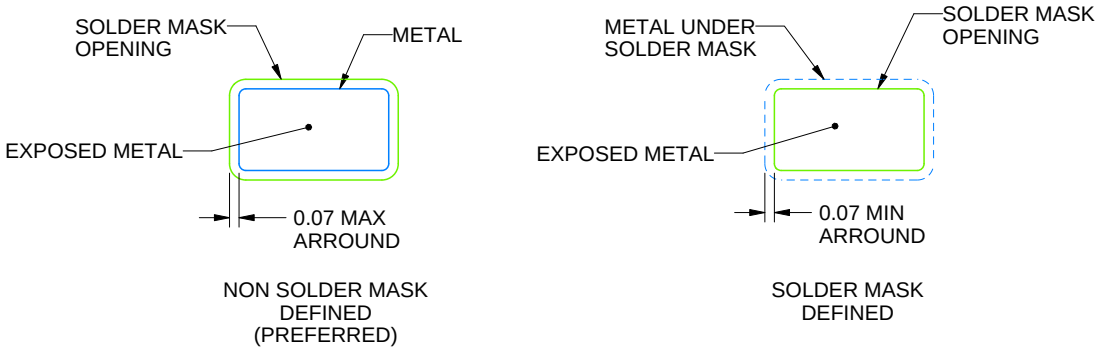
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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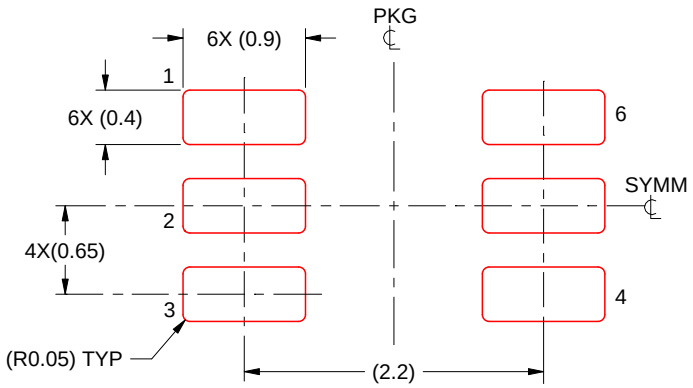
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

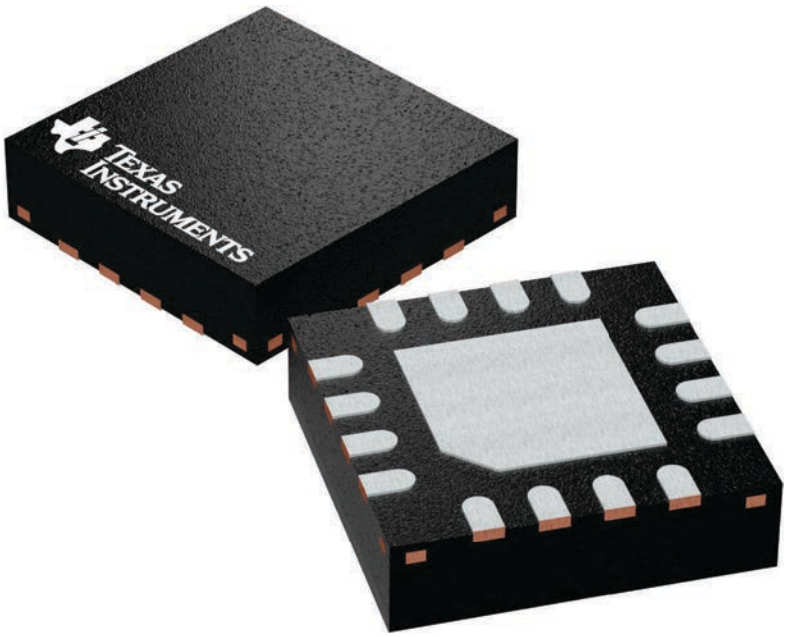
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

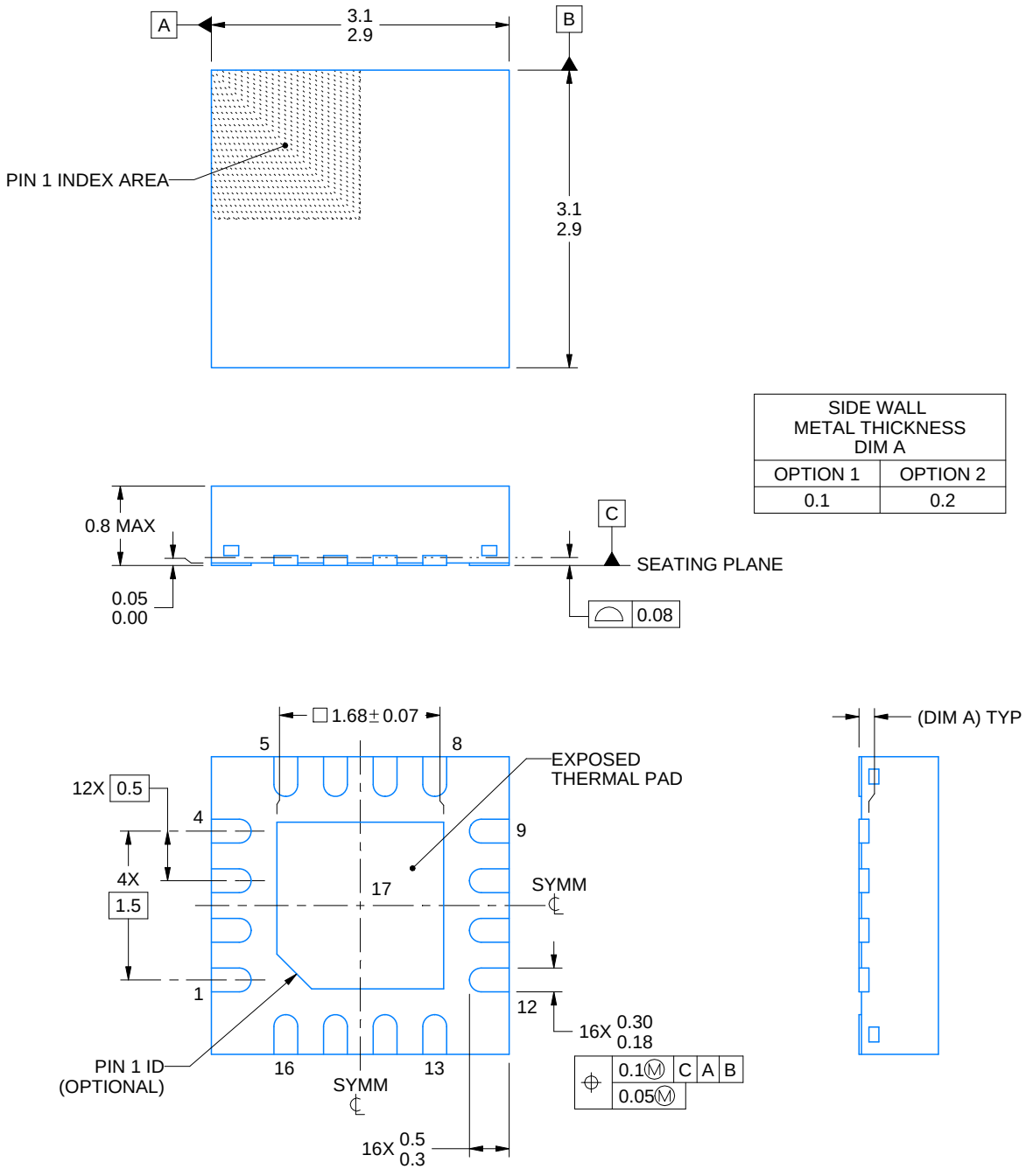


RTE0016C

PACKAGE OUTLINE

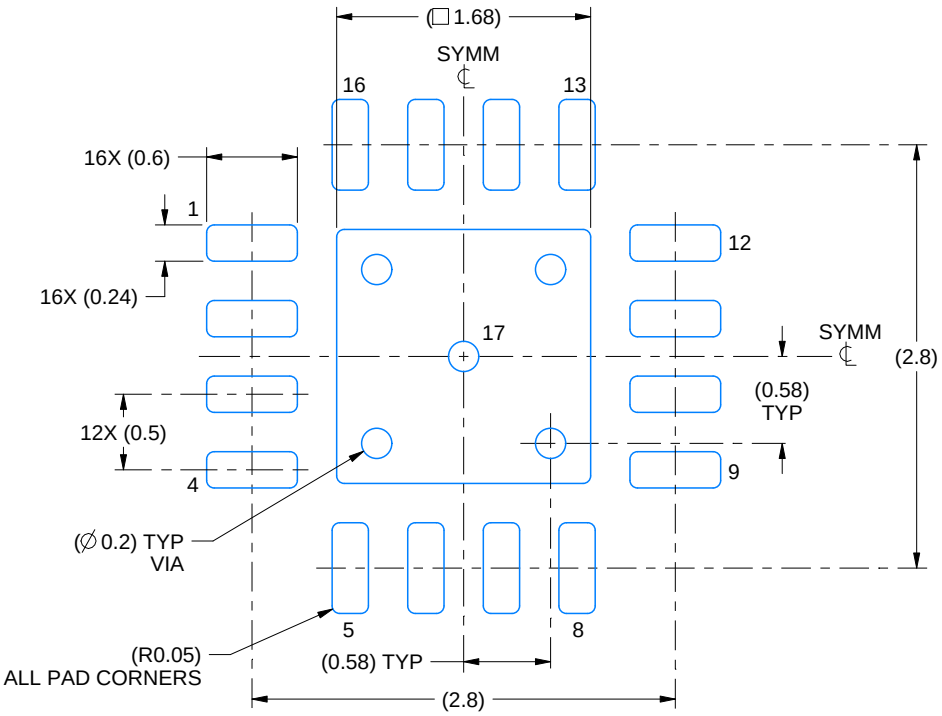
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

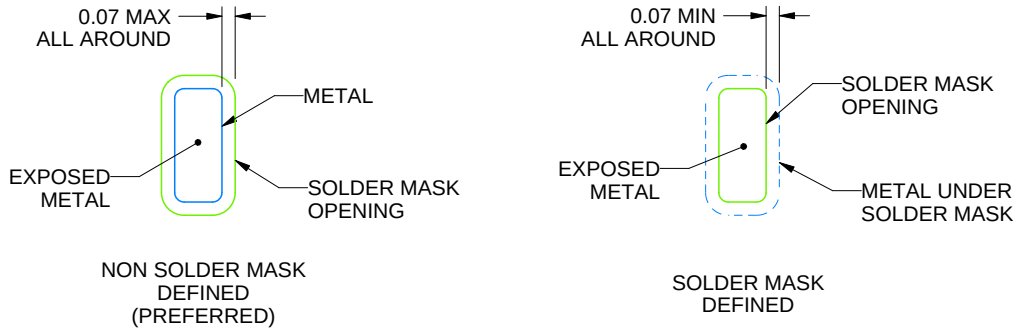


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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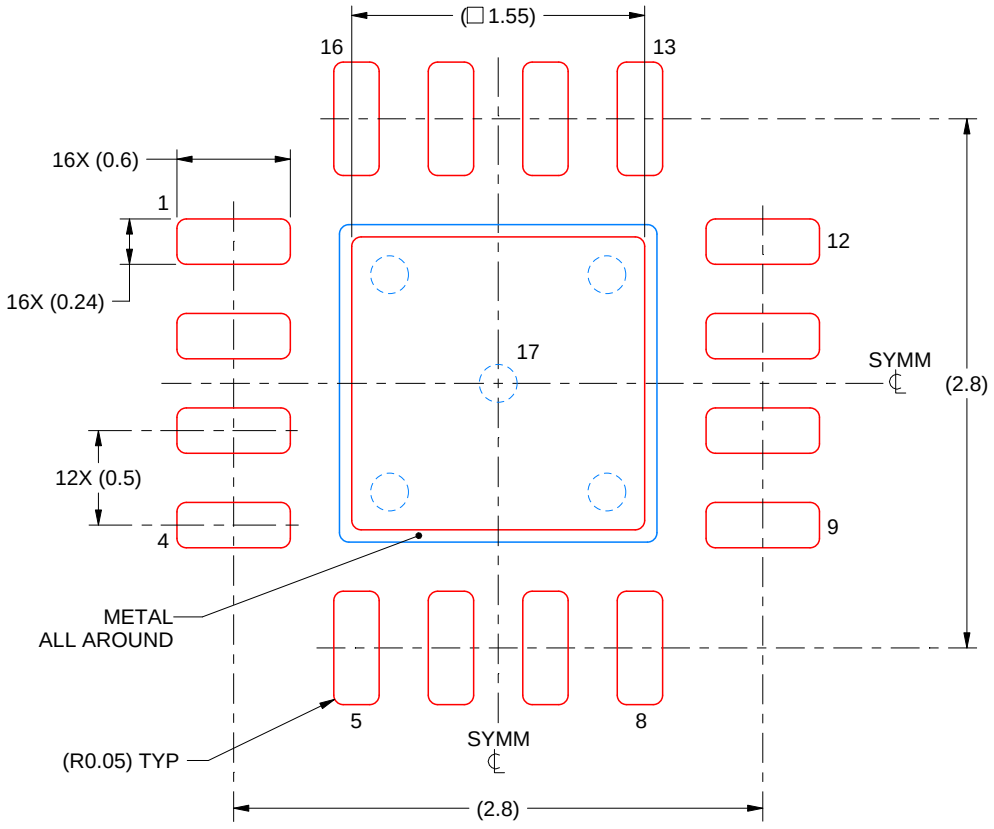
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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