TLV4021, TLV4031, TLV4041, TLV4051
JAJSGC6C – MARCH 2019 – REVISED DECEMBER 2021

TLV40x1 高精度リファレンス搭載、小型低消費電力コンパレータ

1 特長

- 広い電源電圧範囲:1.6V～5.5V
- 高精度リファレンス:0.2V、0.5V、1.2V
- 3.2V の固定スレッショルド
- リファレンス精度
  - 25℃ で 0.5%
  - 温度範囲全体で 1%
- 低い静止電流:2μA
- 伝搬遅延:360ns
- プッシュプルおよびオープン・ドレインの出力オプション
- 既知のスタートアップ条件
- 非反転入力品と反転入力品を選択可能
- 高精度ヒステリシス
- 温度範囲:-40℃～+125℃
- パッケージ:
  - 0.73mm × 0.73mm DSBGA (4 バンプ)
  - SOT-23 (5 ピン)

2 アプリケーション

- 自己診断
- リチウムイオン・バッテリの監視
- バッテリの管理および保護
- 電流および電圧センシング
- アナログ・フロント・エンド
- パワー・マネージメント
- ポイント・オブ・ロード・レギュレータ
- DC/DC、AC/DC 電源
- システム制御および監視

3 概要

TLV40x1 デバイスは、高精度リファレンスと高速応答を備えた低消費電力、高精度コンパレータです。TLV40x1 コンパレータは、超小型の DSBGA パッケージ (0.73mm × 0.73mm) で供給されており、低消費電力と動作条件の変化に対する高速応答とが必要な携帯型またはバッテリ駆動型電子機器など、スペースの制約が厳しい設計に適用できます。

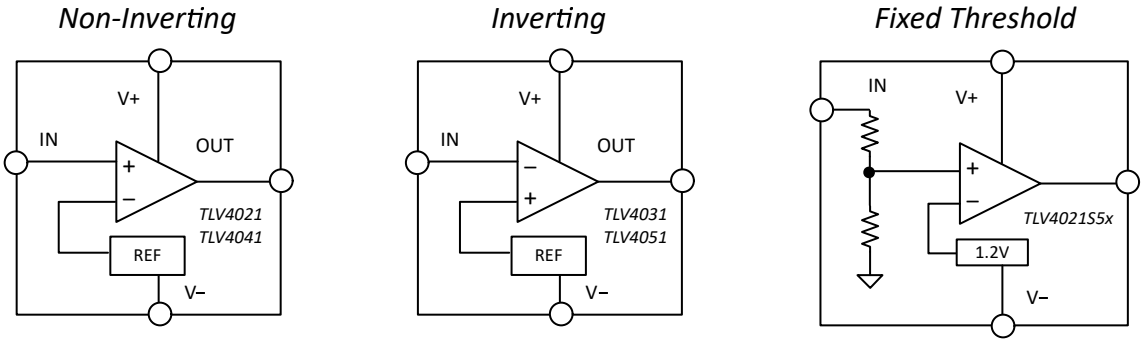
TLV40x1 は、リファレンスおよび高精度ヒステリシスを出荷時に調整済みであるため、低速で変化する入力信号をクリーンなデジタル出力に変換する必要がある、ノイズの多い過酷環境での電圧および電流監視に適しています。同様に、入力の短時間のグリッチは除去されるため、誤トリガのない安定した出力動作が確保されます。

TLV40x1 は各種構成で提供しているため、システム設計者は目的の出力応答を得られます。さらに、TLV4021 と TLV4041 は非反転入力、TLV4031 と TLV4051 は反転入力に対応しています。たとえば、TLV4021 と TLV4031 はオープン・ドレイン出力段を、TLV4041 と TLV4051 はプッシュプル出力段を備えています。また、TLV40x1 ファミリの各コンパレータには、0.2V、0.5V、1.2V の高精度リファレンスが用意されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TLV4021、TLV4031、TLV4041、TLV4051	DSBGA (4)	0.73mm × 0.73mm
TLV4041、TLV4051	SOT-23 (5)	2.9mm × 1.6mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

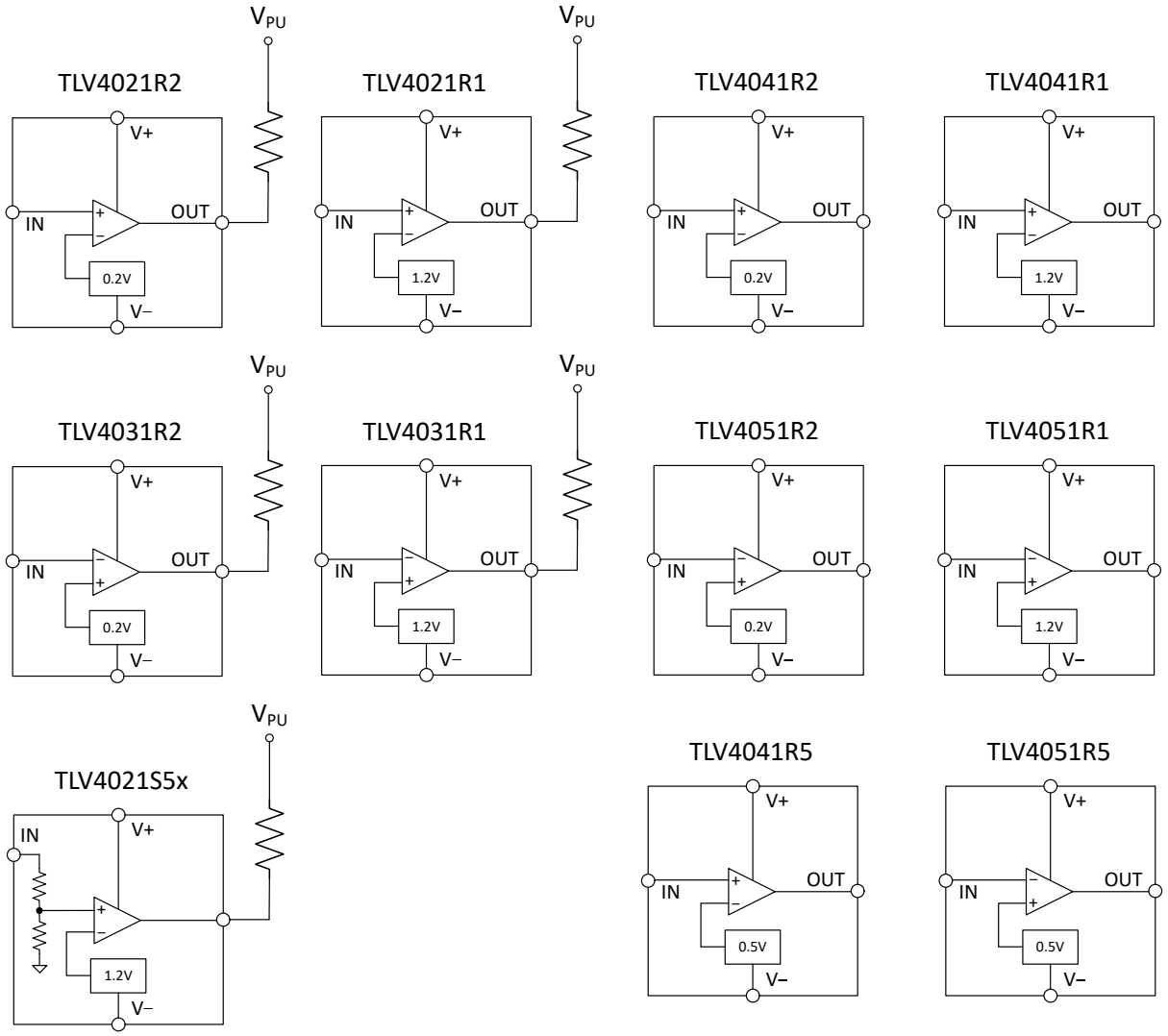


TLV40x1 の構成

表 3-1. TLV40x1 真理値表

デバイス	入力構成	リファレンス	出力方式
TLV4021R1	非反転	1.2V	オープン・ドレイン
TLV4041R1			プッシュプル
TLV4041R5		0.5V	プッシュプル
TLV4021R2		0.2V	オープン・ドレイン
TLV4041R2			プッシュプル
TLV4031R1	反転	1.2V	オープン・ドレイン
TLV4051R1			プッシュプル
TLV4051R5		0.5 V	プッシュプル
TLV4031R2		0.2V	オープン・ドレイン
TLV4051R2			プッシュプル

デバイス	入力構成	固定スレッショルド	出力方式
TLV4021S5x	非反転	3.2V	オープン・ドレイン



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2020) to Revision C (December 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- ドキュメント全体にわたって TLV4021S5x を追加 ... 1

Changes from Revision A (May 2019) to Revision B (March 2020) — **Page**

- リファレンス電圧 0.5V の SOT-23 パッケージ・オプションを追加。 ... 1
- 構成図と TLV40x1 の真理値表を変更。 ... 1
- TLV40x1 ファミリ全体の構成図を追加。 ... 1

Changes from Revision * (October 2018) to Revision A (May 2019) — **Page**

- 「製品プレビュー」から「量産データ」に変更 ... 1

5 Pin Configuration and Functions

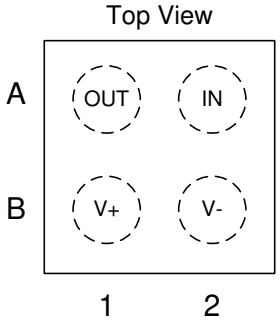


図 5-1. YKA Package
4-Bump DSBGA
Top View

表 5-1. DSBGA Package Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
OUT	A1	O	Comparator output: OUT is push-pull on TLV4041/4051 and open-drain on TLV4021/4031
V+	B1	P	Positive (highest) power supply
V–	B2	P	Negative (lowest) power supply
IN	A2	I	Comparator input: IN is non-Inverting on TLV4021/4041 and inverting on TLV4031/4051

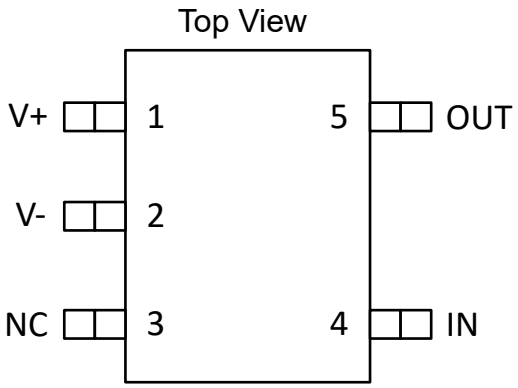


図 5-2. SOT-23 Package
5-pin
Top View

表 5-2. SOT-23 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V+	1	P	Positive (highest) power supply
V-	2	P	Negative (lowest) power supply
NC	3	x	No connect; this pin is not internally connected to the die. It can be grounded if that is preferred in the system.
IN	4	I	Comparator input: IN is inverting on TLV4031/4051
OUT	5	O	Comparator output: OUT is push-pull on TLV4041/4051

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		–0.3	6	V
Input voltage (IN) from (V–) (2)		–0.3	6	V
Input Current (IN)(2)			±10	mA
Output voltage (OUT) from (V-)	TLV4021, TLV4031	–0.3	6	V
	TLV4041, TLV4051	–0.3	(V+) + 0.3	V
Output short-circuit duration(3)			10	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3 V below (V–) must be current-limited to 10 mA or less.
In addition, IN can be greater than (V+) and OUT as long as it is within the –0.3 V to 6 V range. Input signals that can swing beyond this range must be current-limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	1.6	5.5	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV40x1		UNIT
		YKA (DSBGA)	SOT-23 (DBV)	
		4 BUMPS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.5	181.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.8	101.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	52.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	28.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.7	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_S = 1.8 V to 5 V, typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1R1	1.194	1.2	1.206	V
	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		1.188		1.212	
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C		1.174	1.18	1.186	
	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C		1.168		1.192	
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1R2	0.197	0.2	0.203	V
	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		0.196		0.204	
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C		0.177	0.18	0.183	
	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C		0.176		0.184	
V_{IT+}	Postive-going input threshold voltage (TLV40x1R5 only)	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1R5	0.495	0.5	0.505	V
	Postive-going input threshold voltage (TLV40x1R5 only)	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		0.49		0.51	V
V_{IT-}	Negative-going input threshold voltage (TLV40x1R5 only)	V_S = 1.8 V and 5 V, T_A = 25°C		0.4752	0.48	0.4848	V
	Negative-going input threshold voltage (TLV40x1R5 only)	V_S = 1.8 V and 5 V, T_A = -40°C to +125°C		0.4704		0.4896	V
V_{IT+}	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV4021S5x	3.238	3.254	3.270	V
	Postive-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		3.221		3.287	V
V_{IT-}	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = 25°C		3.184	3.2	3.216	V
	Negative-going input threshold voltage	V_S = 1.8 V and 5 V, T_A = -40℃ to +125℃		3.168		3.232	V
V_{HYS} (2)	Input hysteresis voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1Ry		20		mV
V_{HYS}	Input hysteresis voltage (TLV40x1R5 only)	V_S = 1.8 V and 5 V, T_A = 25℃	TLV40x1R5		20		mV
V_{HYS} (2)	Input hysteresis voltage	V_S = 1.8 V and 5 V, T_A = 25°C	TLV40x1S5x		54		mV
V_{IN}	Input voltage range	T_A = -40℃ to +125℃		V–		5.5	V
I_{BIAS}	Input bias current	Over V_{IN} range			10		pA
I_{BIAS}	Input bias current (TLV4021S5x only)	IN = 3.3 V			1.65		µA
V_{OL}	Voltage output swing from (V–)	I_{SINK} = 200 µA, OUT asserted low, V_S = 5 V, T_A = –40°C to +125°C				100	mV
		I_{SINK} = 3 mA, OUT asserted low, V_S = 5 V, T_A = –40°C to +125°C				400	mV
V_{OH}	Voltage output swing from (V+) (TLV4041/4051 only)	I_{SOURCE} = 200 µA, OUT asserted high, V_S = 5 V, T_A = –40°C to +125°C				100	mV
		I_{SOURCE} = 3 mA, OUT asserted high, V_S = 5 V, T_A = –40°C to +125°C				400	mV
I_{O-LKG}	Open-drain output leakage current (TLV4021/4031 only)	V_S = 5 V, OUT asserted high V_{PULLUP} = (V+), T_A = 25°C			20		pA
I_{SC}	Short-circuit current	V_S = 5 V, sinking, T_A = 25°C			55		mA
I_{SC}	Short-circuit current	V_S = 5 V, sourcing, T_A = 25°C (TLV4041/4051 only)			50		mA

6.5 Electrical Characteristics (continued)

V_S = 1.8 V to 5 V, typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	No load, T_A = 25°C, Output Low, V_S = 1.8 V		2	3.5	µA
		No load, T_A = –40°C to +125°C, Output Low, V_S = 1.8 V			5	µA
V_{POR} (1)	Power-on reset voltage			1.45		V

(1) See Section 7.4.1 (Power ON Reset) for more details.
(2) See Section 7.4.3 (Switching Thresholds and Hysteresis) for more details.

6.6 Switching Characteristics

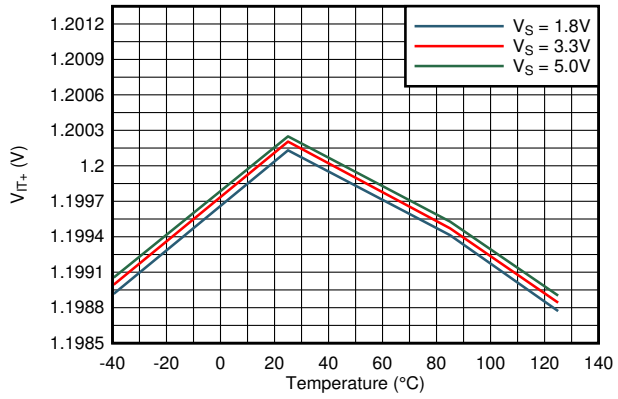
Typical values are at T_A = 25°C, V_S = 3.3 V, C_L = 15 pF; Input overdrive = 100 mV for TLV40x1Ry & 5% for TLV4021S5x, R_P=4.99 kΩ for open-drain options (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay, high-to-low (1)	Midpoint of input to midpoint of output		360		ns
t_{PLH}	Propagation delay, low-to-high (1)	Midpoint of input to midpoint of output		360		ns
t_{PHL}	Propagation delay, high-to-low ((1)) (TLV4021S5x only)	Midpoint of input to midpoint of output		2		µs
t_{PLH}	Propagation delay, low-to-high ((1)) (TLV4021S5x only)	Midpoint of input to midpoint of output		2		µs
t_R	Rise time (TLV4041/4051 only)	20% to 80%		10		ns
t_F	Fall time	20% to 80%		10		ns
t_{ON}	Power-up time (2)			500		µs

(1) High-to-low and low-to-high refers to the transition at the input.
(2) During power on cycle, V_S must exceed 1.6 V for t_{ON} before the output will reflect the condition on the input. Prior to t_{ON} elapsing, the output is controlled by the POR circuit.

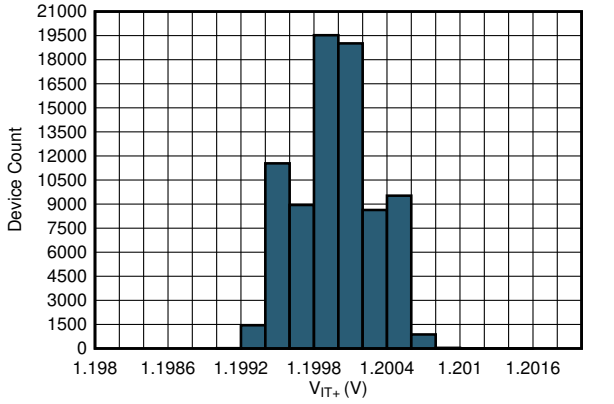
7 Typical Characteristics

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



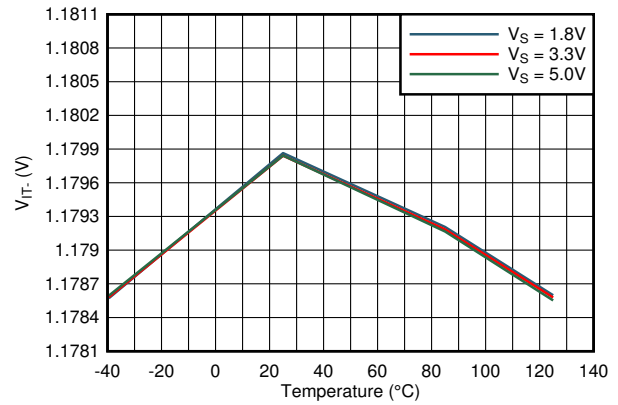
TLV40x1R1

図 7-1. Positive Threshold vs Temperature



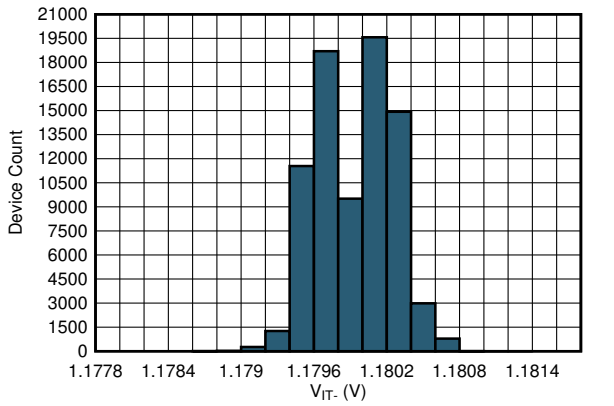
TLV40x1R1 V_S = 5 V

図 7-2. Positive Threshold Histogram



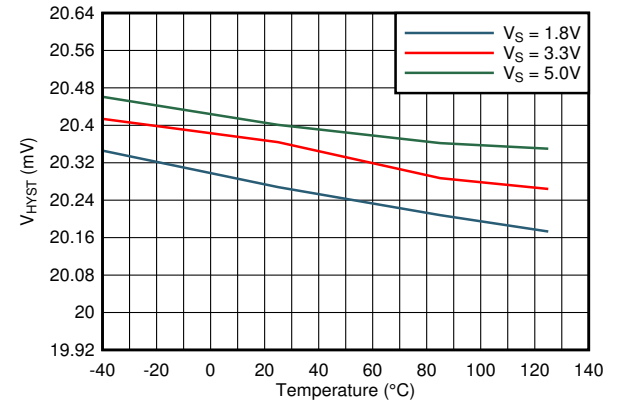
TLV40x1R1

図 7-3. Negative Threshold vs Temperature



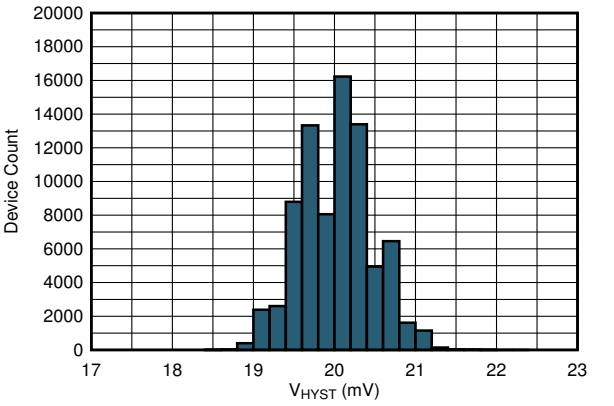
TLV40x1R1 V_S = 5 V

図 7-4. Negative Threshold Histogram



TLV40x1R1

図 7-5. Hysteresis vs Temperature

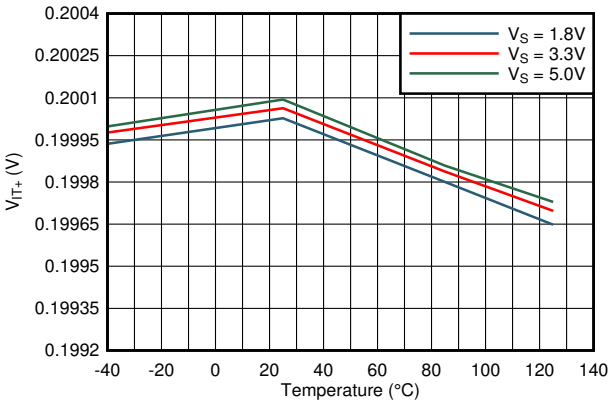


TLV40x1R1 V_S = 5 V

図 7-6. Hysteresis Histogram

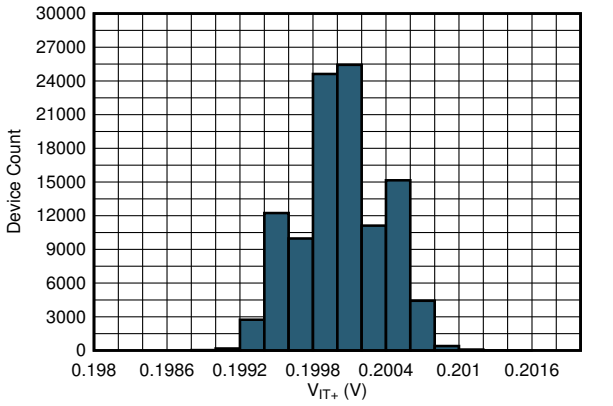
7 Typical Characteristics (continued)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



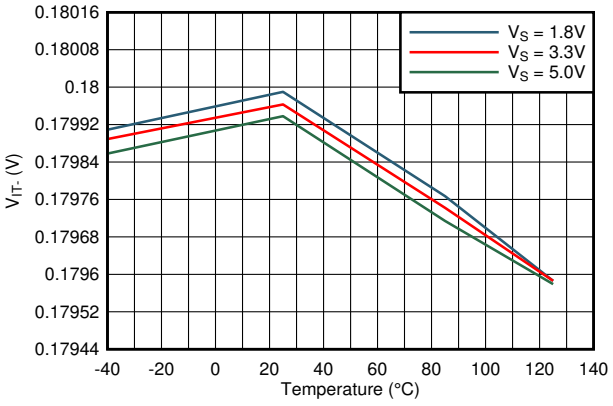
TLV40x1R2

図 7-7. Positive Threshold vs Temperature



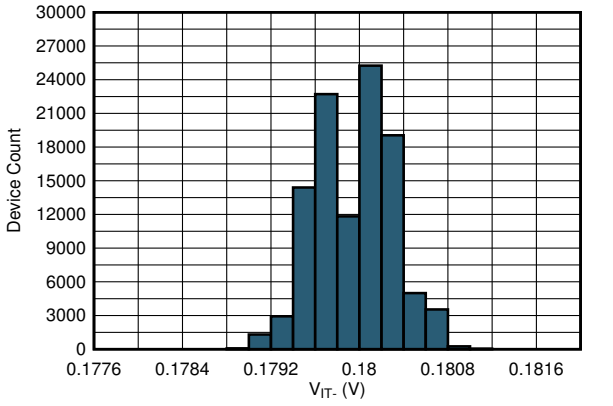
TLV40x1R2 V_S = 5 V

図 7-8. Positive Threshold Histogram



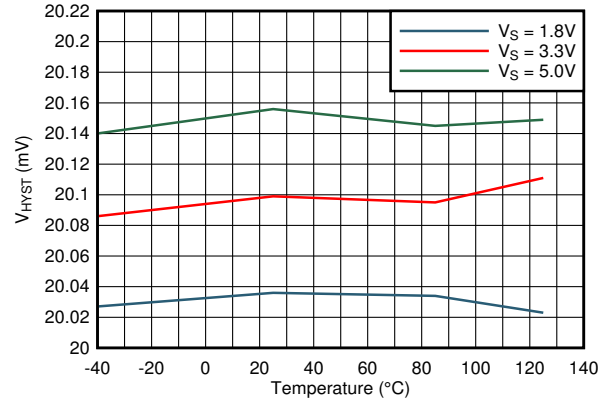
TLV40x1R2

図 7-9. Negative Threshold vs Temperature



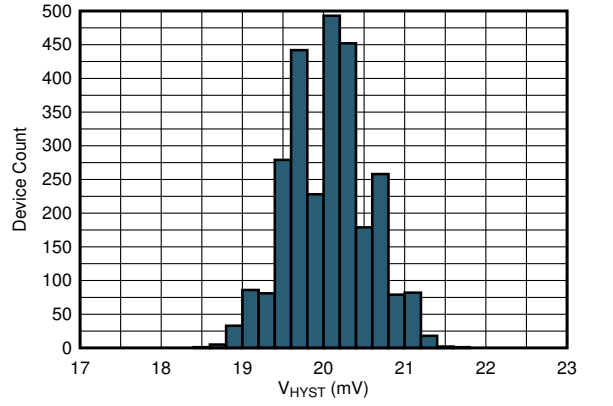
TLV40x1R2 V_S = 5 V

図 7-10. Negative Threshold Histogram



TLV40x1R2

図 7-11. Hysteresis vs Temperature

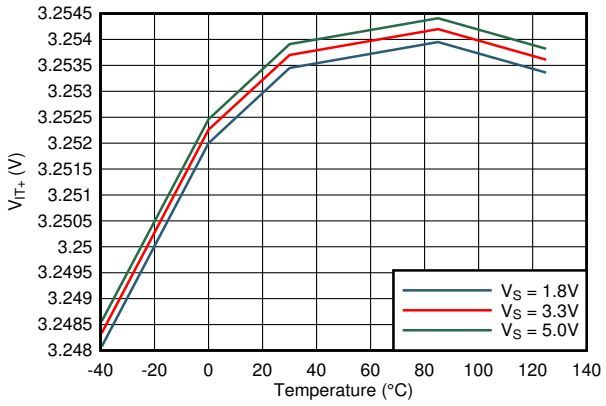


TLV40x1R2 V_S = 5 V

図 7-12. Hysteresis Histogram

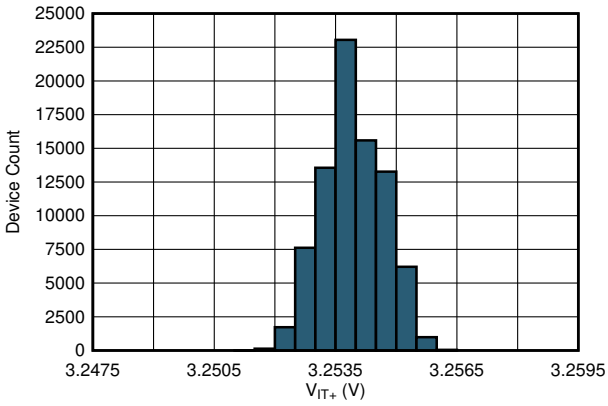
7 Typical Characteristics (continued)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



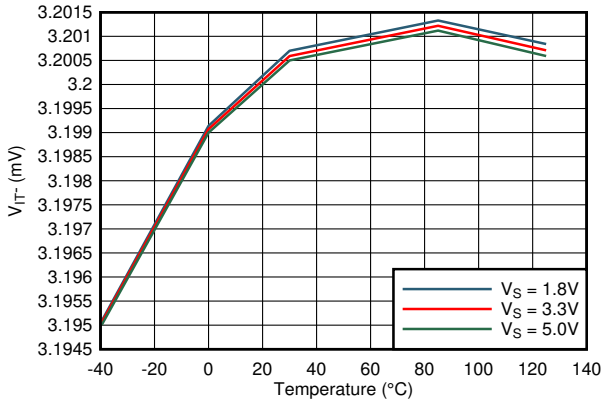
TLV4021S5x

図 7-13. Positive Threshold vs Temperature



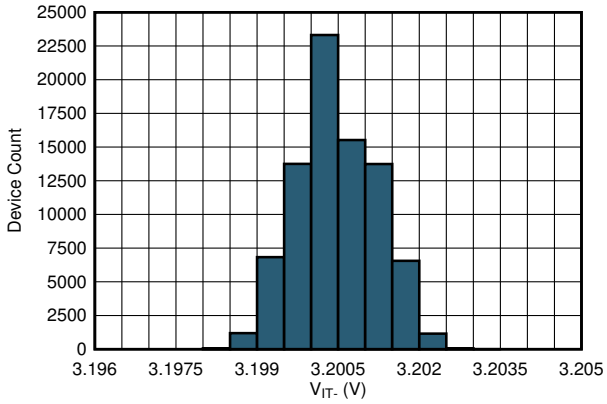
TLV4021S5x

図 7-14. Positive Threshold Histogram



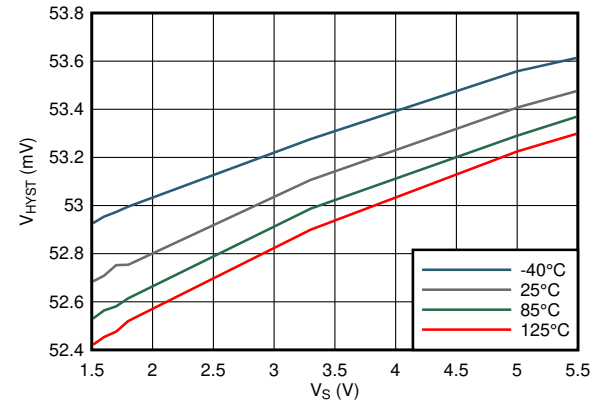
TLV4021S5x

図 7-15. Negative Threshold vs Temperature



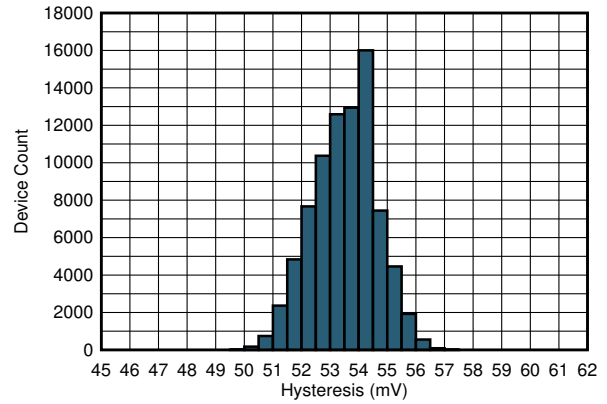
TLV4021S5x

図 7-16. Negative Threshold Histogram



TLV4021S5x

図 7-17. Hysteresis vs Supply Voltage

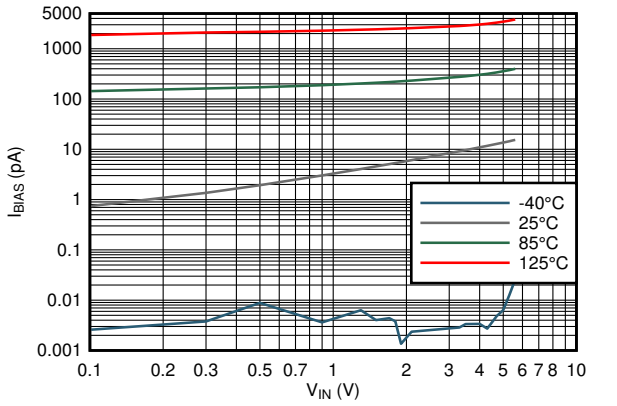


TLV4021S5x

図 7-18. Hysteresis Histogram

7 Typical Characteristics (continued)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



V_S = 1.8V to 5V TLV40x1Ry

図 7-19. Bias Current vs Common Mode Voltage

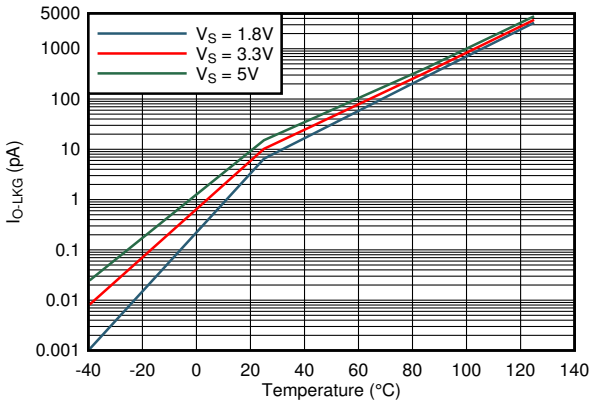
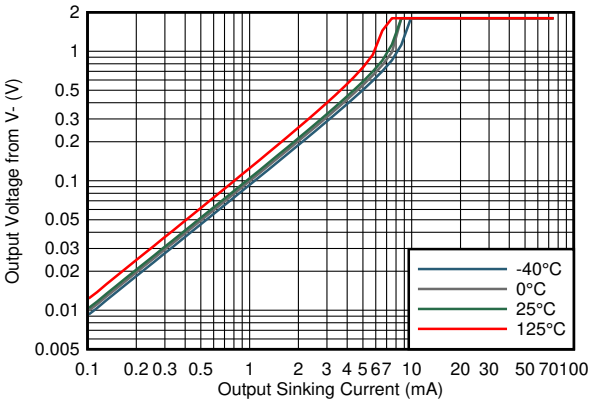
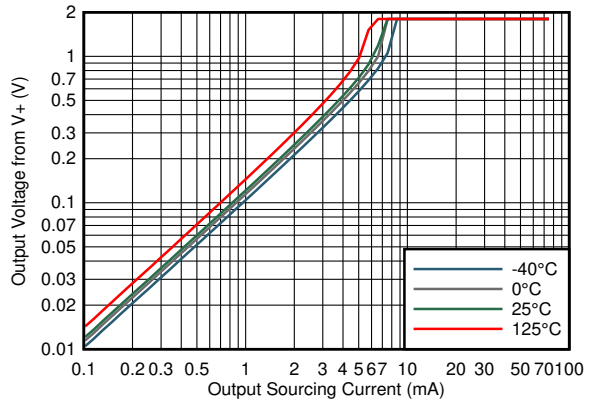


図 7-20. Output Current Leakage vs Temperature



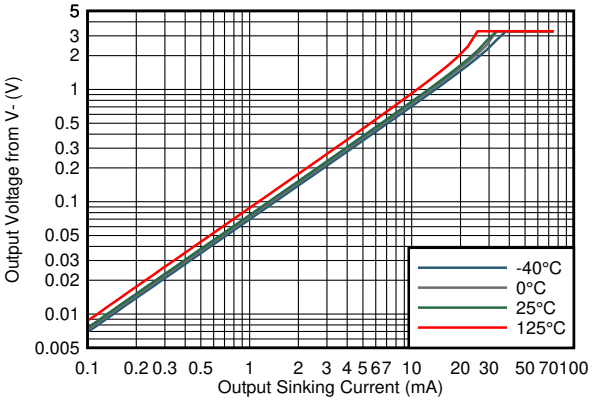
V_S = 1.8V

図 7-21. Output Voltage vs Output Sinking Current



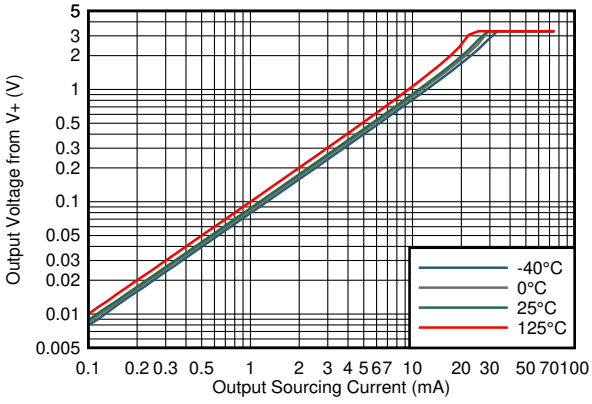
V_S = 1.8V

図 7-22. Output Voltage vs Output Sourcing Current



V_S = 3.3V

図 7-23. Output Voltage vs Output Sinking Current

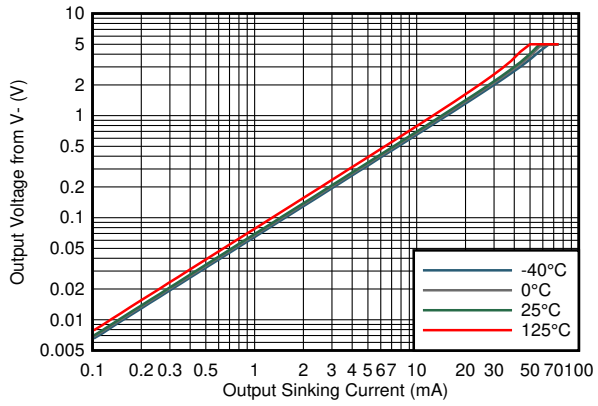


V_S = 3.3V

図 7-24. Output Voltage vs Output Sourcing Current

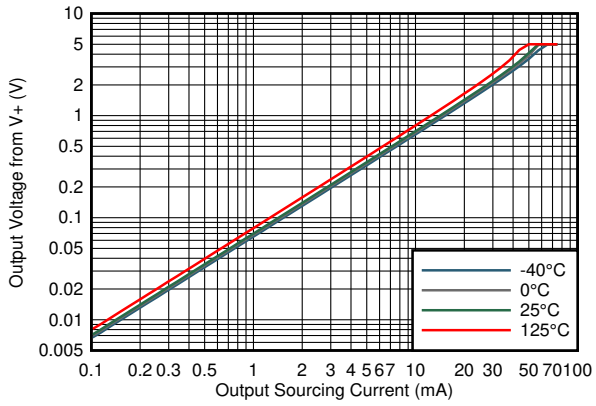
7 Typical Characteristics (continued)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



V_S = 5V

図 7-25. Output Voltage vs Output Sinking Current



V_S = 5V

図 7-26. Output Voltage vs Output Sourcing Current

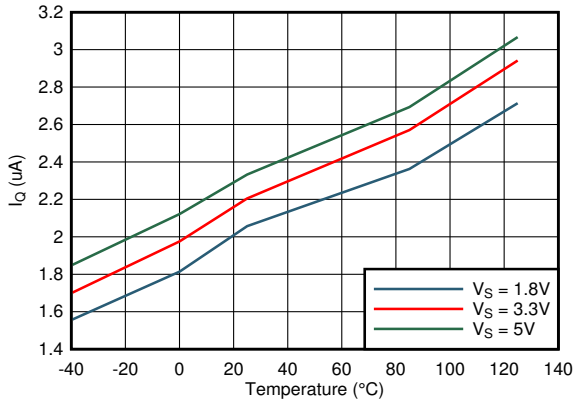
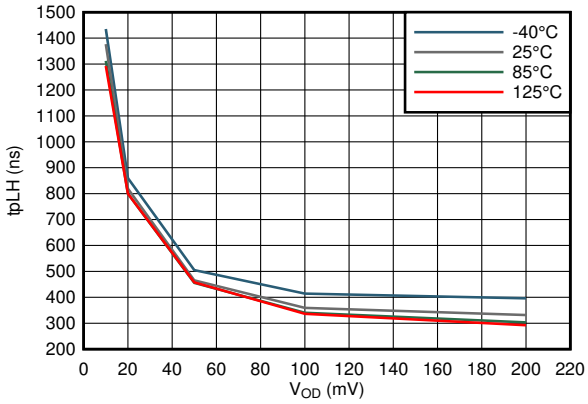
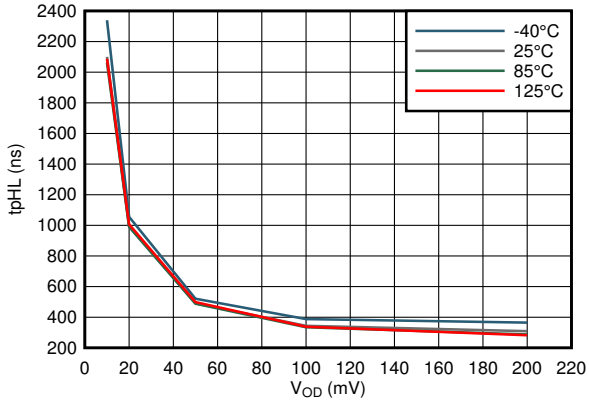


図 7-27. Supply Current vs Temperature



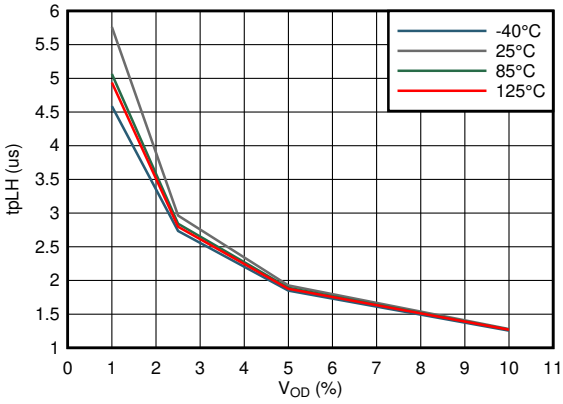
V_S = 1.8V to 5V TLV40x1R2

図 7-28. Propagation Delay Low-High vs Input Overdrive



V_S = 1.8V to 5V TLV40x1R2

図 7-29. Propagation Delay High-Low vs Input Overdrive

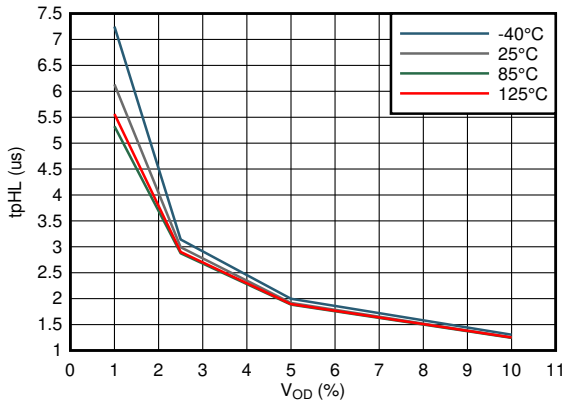


V_S = 1.8V to 5V TLV4021Sx5

図 7-30. Propagation Delay Low-High vs Input Overdrive

7 Typical Characteristics (continued)

at T_J = 25°C and V_S = 3.3 V (unless otherwise noted)



V_S = 1.8V to 5V TLV4021Sx5

7-31. Propagation Delay High-Low vs Input Overdrive

8 Detailed Description

8.1 Overview

The TLV40x1 devices are low-power comparators that are well suited for compact, low-current, precision voltage detection applications. With high-accuracy, switching thresholds options of 0.2V, 0.5 V, 1.2V, and 3.2V, 2uA of quiescent current, and propagation delay of 450ns and 2us, the TLV40x1 comparator family enables power conscious systems to monitor and respond quickly to fault conditions.

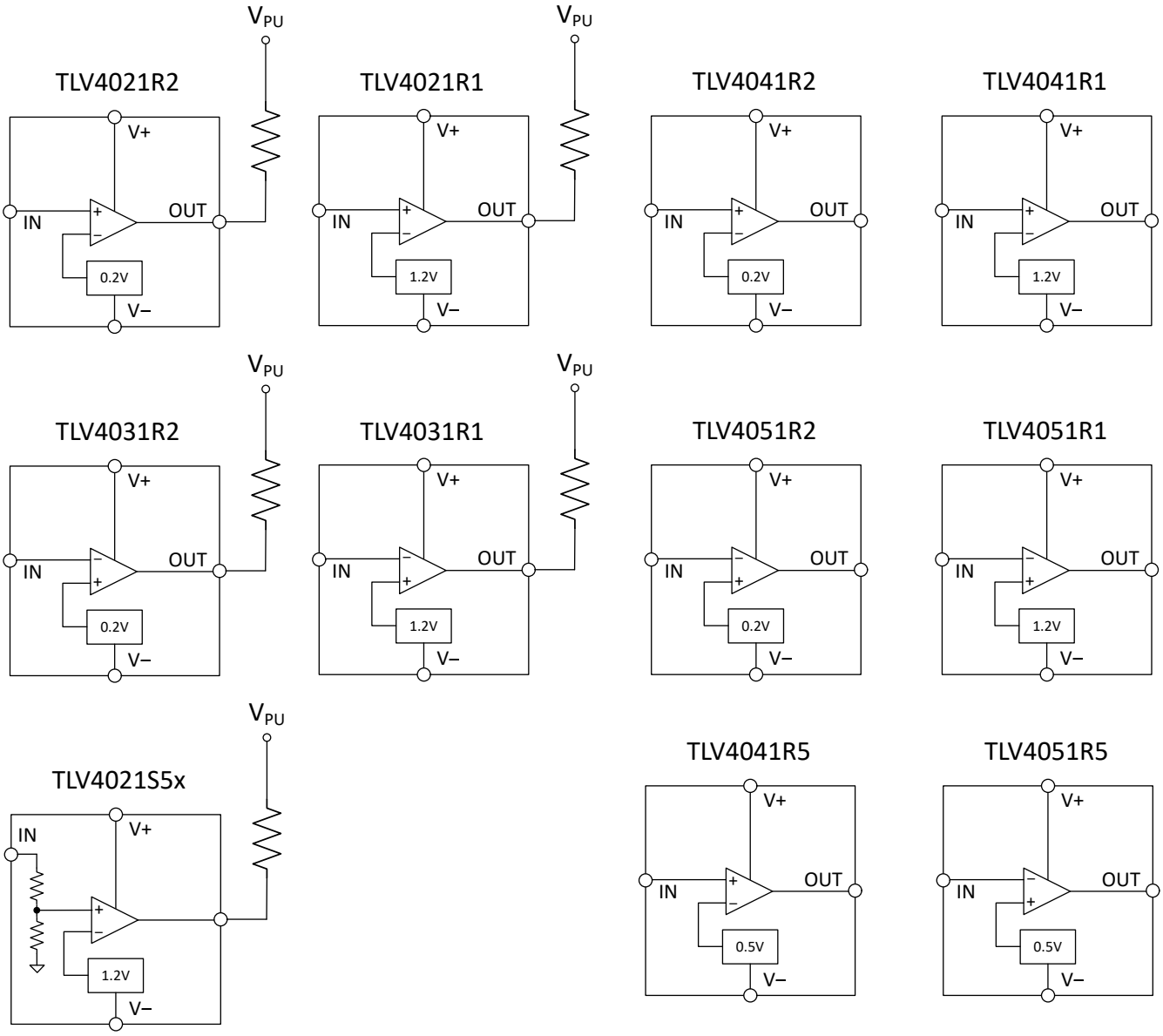
The TLV40x1Ry comparators assert the output signal as shown in 表 8-1. V_{IT+} represents the positive-going input threshold that causes the comparator output to change state, while V_{IT-} represents the negative-going input threshold that causes the output to change state. Since V_{IT+} and V_{IT-} are factory trimmed and warranted over temperature, the TLV40x1 is equally suited for undervoltage and overvoltage applications. In order to monitor any voltage above the internal reference voltage, an external resistor divider network is required.

The TLV4021S5x functions similar to the TLV40x1Ry comparators except the resistor divider is internal to the device. Having the resistor divider internal to the device allows the TLV4021S5x to have switching thresholds higher than the internal reference voltage of 1.2V without any external components.

表 8-1. TLV40x1 Truth Table

DEVICE	(V_{IT+}, V_{IT-})	OUTPUT TOPOLOGY	INPUT VOLTAGE	OUTPUT LOGIC LEVEL
TLV4021R2 TLV4021R1	0.2V, 0.18V 1.2V, 1.18V	Open-Drain	IN > V_{IT+}	Output high impedance
			IN < V_{IT-}	Output asserted low
TLV4041R2 TLV4041R5 TLV4041R1	0.2V, 0.18V 0.5V, 0.48V 1.2V, 1.18V	Push-Pull	IN > V_{IT+}	Output asserted high
			IN < V_{IT-}	Output asserted low
TLV4031R2 TLV4031R1	0.2V, 0.18V 1.2V, 1.18V	Open-Drain	IN > V_{IT+}	Output asserted low
			IN < V_{IT-}	Output high impedance
TLV4051R2 TLV4051R5 TLV4051R1	0.2V, 0.18V 0.5V, 0.48V 1.2V, 1.18V	Push-Pull	IN > V_{IT+}	Output asserted low
			IN < V_{IT-}	Output asserted high
TLV4021S5x	3.254V, 3.2V	Open-Drain	IN > V_{IT+}	Output high impedance
			IN < V_{IT-}	Output asserted low

8.2 Functional Block Diagram



8.3 Feature Description

The TLV40x1 is a family of 4-pin, precision, low-power comparators with precision switching thresholds. The TLV40x1 comparators feature a rail-to-rail input stage with factory programmed switching thresholds for both rising and falling input waveforms. The comparator family also supports open-drain and push-pull output configurations as well as non-inverting and inverting inputs.

8.4 Device Functional Modes

8.4.1 Power ON Reset (POR)

The TLV40x1 comparators have a Power-on-Reset (POR) circuit which provides system designers a known start-up condition for the output of the comparators. When the power supply (V_S) is ramping up or ramping down, the POR circuit will be active when V_S is below V_{POR}. For the TLV4021 and TLV4031, the POR circuit will force the output to High-Z, and for the TLV4041 and TLV4051, the POR circuit will hold the output low at (V-). When V_S is greater than, or equal to, the minimum recommended operating voltage, the comparator output reflects the state of the input (IN).

The following pictures represent how the TLV40x1 outputs respond for V_S rising and falling. For the comparators with open-drain outputs (TLV4021/4031), IN is connected to (V-) to highlight the transition from POR circuit control to standard comparator operation where the output reflects the input condition. Note how the output goes low when V_S reaches 1.45V. Likewise, for the comparators with push-pull outputs (TLV4041/4051), the input is connected to (V+). Note how the output goes high when V_S reaches 1.45V.

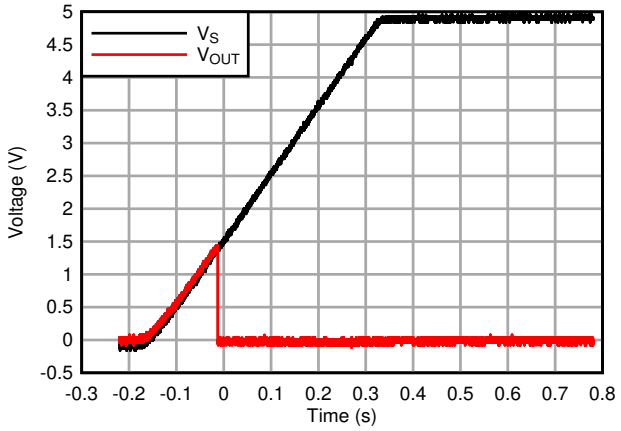


図 8-1. TLV4021/4031 Output for V_S Rising

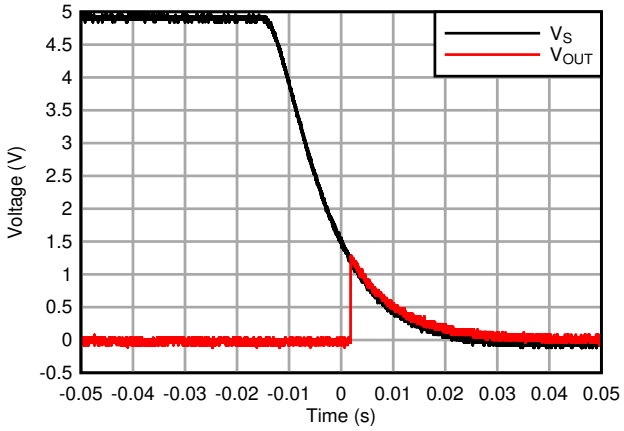


図 8-2. TLV4021/4031 Output for V_S Falling

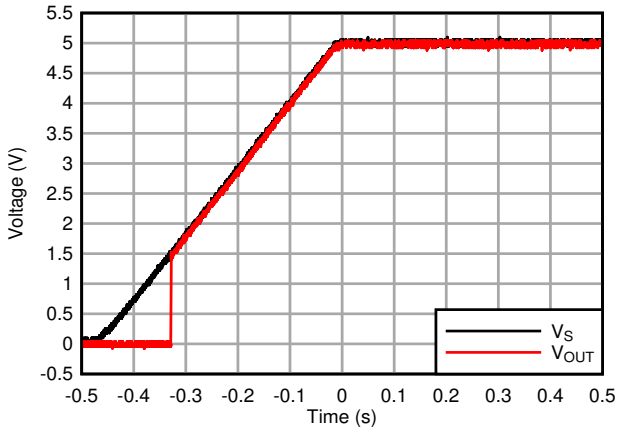


図 8-3. TLV4041/4051 Output for V_S Rising

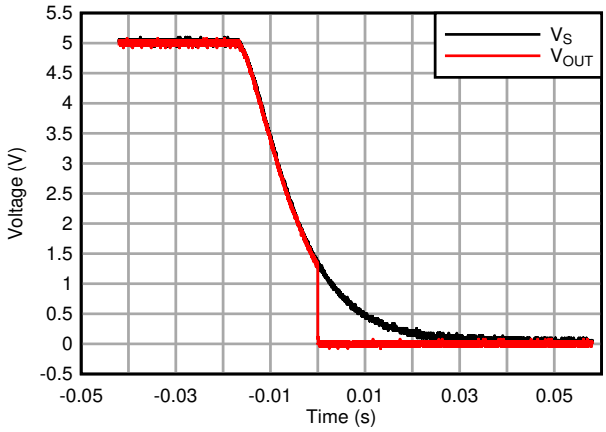


図 8-4. TLV4041/4051 Output for V_S Falling

8.4.2 Input (IN)

The TLV40x1 comparators have two inputs: one external input (IN) and one internal input that is connected to the integrated voltage reference. The comparator rising threshold is trimmed to the reference voltage (V_{IT+}) while the falling threshold is trimmed to (V_{IT-}). Since the rising and falling thresholds are both trimmed and warranted in the Electrical Characteristics Table, the TLV40x1 is equally suited for undervoltage and overvoltage detection. The difference between (V_{IT+}) and (V_{IT-}) is referred to as the comparator hysteresis and is 20 mV for TLV40x1Ry and 54 mV for TLV4021S5x. The integrated hysteresis makes the TLV40x1 less sensitive to supply-rail noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis.

The comparator input (IN) is able to swing 5.5 V above (V-) regardless of the device supply voltage. This includes the instance when no supply voltage is applied to the comparator (V_S = 0 V). As a result, the TLV40x1 is referred to as fault tolerant, meaning it maintains the same high input impedance when V_S is unpowered or ramping up. While not required in most cases, in order to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor at the comparator input.

For the TLV40x1Ry comparators, the input bias current is typically 10 pA for input voltages between (V-) and (V+) and the value typically doubles for every 10°C temperature increase. The comparator input is protected from voltages below (V-) by an internal diode connected to (V-). As the input voltage goes below (V-), the protection diode becomes forward biased and begins to conduct causing the input bias current to increase exponentially. A series resistor is recommended to limit the input current when sources have signal content that is less than (V-).

For the TLV4021S5x, the input bias current is limited by the internal resistor divider with typical impedance of 2M ohms.

8.4.3 Switching Thresholds and Hysteresis (V_{HYS})

The TLV40x1 transfer curve is shown in 図 8-5.

- V_{IT+} represents the positive-going input threshold that causes the comparator output to change from a logic low state to a logic high state.
- V_{IT-} represents the negative-going input threshold that causes the comparator output to change from a logic high state to a logic low state.
- V_{HYS} represents the difference between V_{IT+} and V_{IT-} and is 20 mV for TLV40x1Ry and 54 mV for TLV4021S5x.

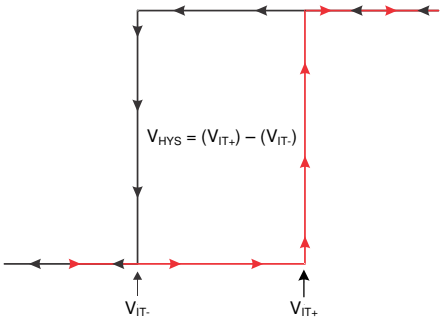


図 8-5. Transfer Curve

V_{IT+} and V_{IT-} have mV's of variation over temperature. The significant portion of the variation of these parameters is a result of the internal bandgap voltage from which V_{IT+} and V_{IT-} are derived. The following hysteresis histograms demonstrate the performance of the TLV40x1 hysteresis circuitry. Since the bandgap reference is used to set V_{IT+} and V_{IT-}, each of these parameters have a tendency to error (track) in the same direction. For example, if V_{IT+} has a positive 0.5% error, V_{IT-} would have a tendency to have a similar positive percentage error. As a result, the variation of hysteresis will never be equal to the difference of the highest V_{IT+} value of its range and the lowest V_{IT-} value of its range.

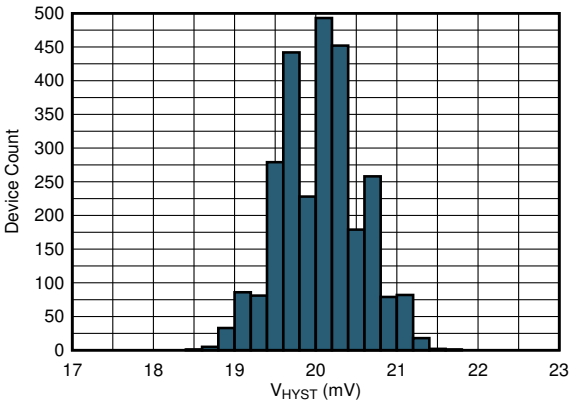


図 8-6. V_{HYST} Histogram (TLV40x1R2, V_S=5V)

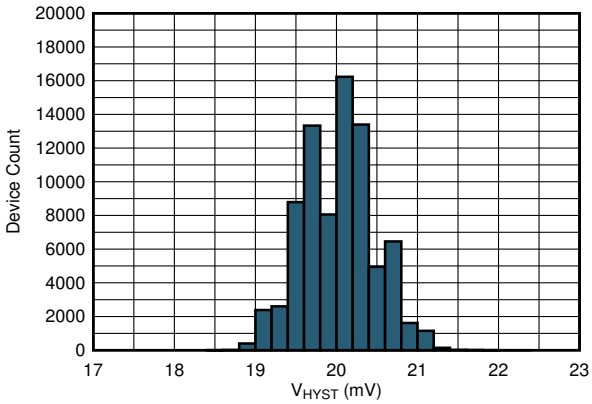


図 8-7. V_{HYST} Histogram (TLV40x1R1, V_S=5V)

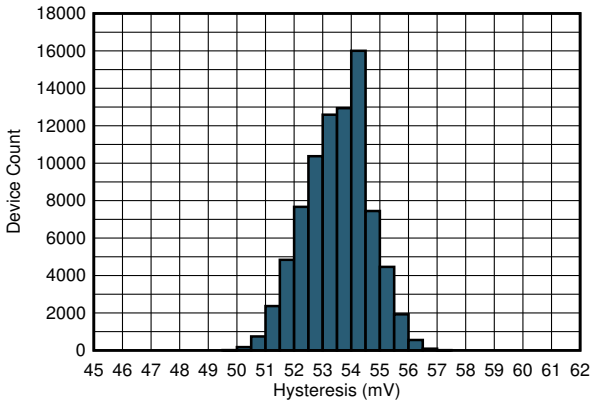


図 8-8. V_{HYST} Histogram (TLV40x1S5, V_S=5V)

8.4.4 Output (OUT)

The TLV4041 and TLV4051 feature a push-pull output stage which eliminates the need for an external pull-up resistor while providing a low impedance output driver. Likewise, the TLV4021 and TLV4031 feature an open-drain output stage which enables the output logic levels to be pulled-up to an external source as high as 5.5 V independent of the supply voltage.

In a typical TLV40x1 application, OUT is connected to an enable input of a processor or a voltage regulator such as a dc-dc converter or low-dropout regulator (LDO). The open-drain output versions (TLV4021/4031) are used if the power supply of the comparator is different than the supply voltage of the device being controlled. In this usage case, a pull-up resistor holds OUT high when the comparator output goes high impedance. The correct interface-voltage level is provided (also known as level-shifting) by connecting the pull-up resistor on OUT to the appropriate voltage rail. The TLV4021/4031 output can be pulled up to 5.5 V, independent of the device supply voltage (V_S). However, if level-shifting is not required, the push-pull output versions (TLV4041/4051) should be utilized in order to eliminate the need for the pull-up resistor.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TLV40x1 is a 4-pin, low-power comparator with a precision, integrated reference. The comparators in this family are well suited for monitoring voltages and currents in portable, battery powered devices.

9.1.1 Monitoring (V+)

Many applications monitor the same rail that is powering the comparator. In these applications the resistor divider is simply connected to the (V+) rail.

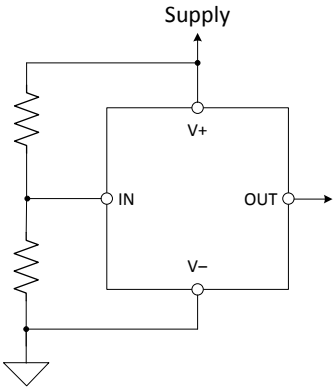


図 9-1. Supply Monitoring

9.1.2 Monitoring a Voltage Other than (V+)

Some applications monitor rails other than the one that is powering the comparator. In these applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.

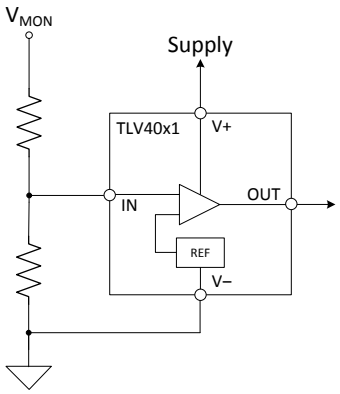


図 9-2. Monitoring a Voltage Other than the Supply

The TLV40x1Ry can monitor a voltage greater than the maximum (V+) with the use of an external resistor divider network. Likewise, the TLV40x1 can monitor voltages as low as the internal reference voltage (0.2 V, 0.5 V, or 1.2 V). The TLV40x1Ry also has the advantage of being able to monitor high impedance sources since the input bias current of the input (IN) is low. This provides an advantage over voltage supervisors that can only monitor the voltage rail that is powering them. Supervisors configured in this fashion have limitations in source impedance and minimum sensing voltage.

9.1.3 V_{PULLUP} to a Voltage Other than (V+)

For applications where the output of the comparator needs to interface with a reset/enable pin that operates from a different supply voltage, the open-drain comparators (TLV4021/4031) should be selected. In these usage cases, the output can be pulled up to any voltage that is lower than 5.5V (independent of (V+)). This technique is commonly referred to as "level-shifting."

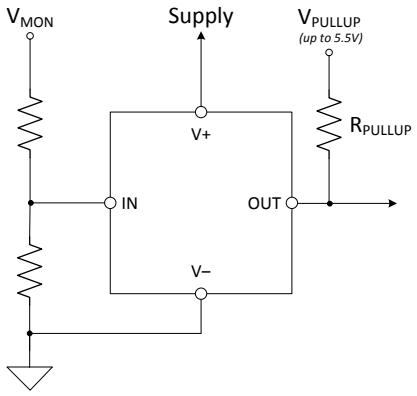


図 9-3. Level-Shifting

9.2 Typical Application

9.2.1 Under-Voltage Detection

Under-voltage detection is frequently required in battery-powered, portable electronics to alert the system that a battery voltage has dropped below the usable voltage level. 図 9-4 shows a simple under-voltage detection circuit using the TLV4041R1 which is a non-inverting comparator with an integrated 1.2 V reference and a push-pull output stage. The non-inverting TLV4041 option was selected in this example since the micro-controller required an active low signal when an undervoltage level occurs. However, if an active high signal was required, the TLV4051 option with an inverting input stage would be utilized.

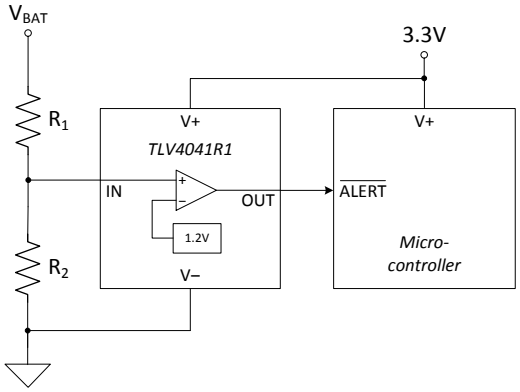


図 9-4. Under-Voltage Detection

9.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from 3.3 V power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

9.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 9-4. Connect (V+) to 3.3 V which also powers the micro-controller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0 V. When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses the (V_{IT-}) threshold of the TLV4041R1. This causes the comparator output to transition from a logic high to a logic low. The push-pull option of the TLV40x1 family is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal. The TLV4041 option with the 1.2 V internal reference is selected because it is the closest internal reference option that is less than the critical under-voltage level of 2.0 V. Choosing the internal reference option that is closest to the critical under-voltage level minimizes the resistor divider ratio which optimizes the accuracy of the circuit. Error at the falling edge threshold of (V_{IT-}) is amplified by the inverse of the resistor divider ratio. So minimizing the resistor divider ratio is a way of optimizing voltage monitoring accuracy.

式 1 is derived from the analysis of 図 9-4.

$$V_{IT-} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \quad (1)$$

where

- R_1 and R_2 are the resistor values for the resistor divider connected to IN
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{IT-} is the falling edge threshold where the comparator output changes state from high to low

Rearranging 式 1 and solving for R_1 yields 式 2.

$$R_1 = \frac{(V_{BAT} - V_{IT-})}{V_{IT-}} \times R_2 \quad (2)$$

For the specific undervoltage detection of 2.0 V using the TLV4041R1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.18)}{1.18} \times 1M = 695\ k\Omega \quad (3)$$

where

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{IT-} is set to1.18 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

9.2.1.3 Application Curve

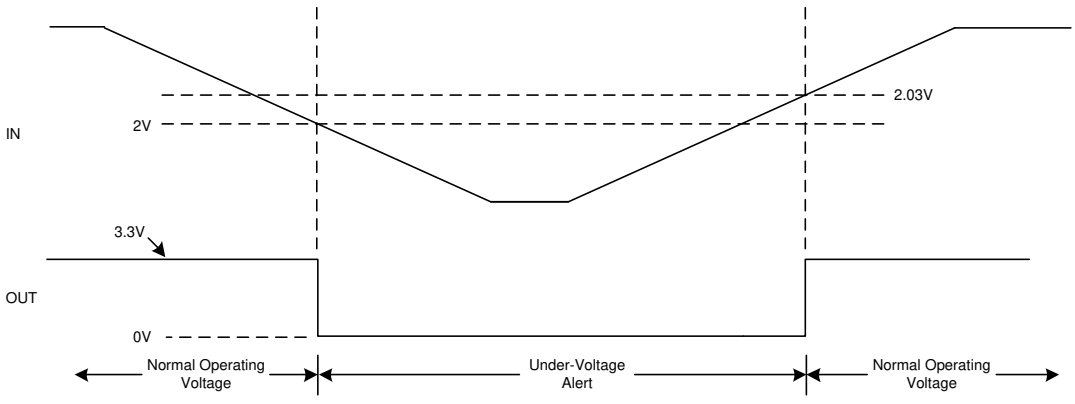


図 9-5. Under-Voltage Detection

9.2.2 Additional Application Information

9.2.2.1 Pull-up Resistor Selection

For the TLV4021 (open-drain output versions of the TLV40x1 family), care should be taken in selecting the pull-up resistor (R_{PU}) value to ensure proper output voltage levels. First, consider the required output high logic level requirement of the logic device that is being driven by the comparator when calculating the maximum R_{PU} value. When in a logic high output state, the output impedance of the comparator is very high but there is a finite amount of leakage current that needs to be accounted for. Use $I_{O\text{-}LKG}$ from the EC Table and the V_{IH} minimum from the logic device being driven to determine R_{PU} maximum using 式 4.

$$R_{PU}(max) = \frac{(V_{PU} - V_{IH(min)})}{I_{O-LKG}} \tag{4}$$

Next, determine the minimum value for R_{PU} by using the V_{IL} maximum from the logic device being driven. In order for the comparator output to be recognized as a logic low, V_{IL} maximum is used to determine the upper boundary of the comparator's V_{OL}. V_{OL} maximum for the comparator is available in the EC Table for specific sink current levels and can also be found from the V_{OUT} versus I_{SINK} curve in the Typical Application curves. A good design practice is to choose a value for V_{OL} maximum that is 1/2 the value of V_{IL} maximum for the input logic device. The corresponding sink current and V_{OL} maximum value will be needed to calculate the minimum R_{PU}. This method will ensure enough noise margin for the logic low level. With V_{OL} maximum determined and the corresponding I_{SINK} obtained, the minimum R_{PU} value is calculated with 式 5.

$$R_{PU}(min) = \frac{(V_{PU} - V_{OL(max)})}{I_{SINK}} \tag{5}$$

Since the range of possible R_{PU} values is large, a value between 5 kΩ and 100 kΩ is generally recommended. A smaller R_{PU} value provides faster output transition time and better noise immunity, while a larger R_{PU} value consumes less power when in a logic low output state.

9.2.2.2 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 100 nF low equivalent series resistance (ESR) capacitor from (V+) to (V-).

9.2.2.3 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor from the comparator input (IN) to the (V-) for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.3 What to Do and What Not to Do

Do connect a 100 nF decoupling capacitor from (V+) to (V-) for best system performance.

If the monitored voltage is noisy, do connect a decoupling capacitor from the comparator input (IN) to (V-).

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the impact on accuracy.

Don't use a pull-up resistor that is too small because the larger current sunk by the output may exceed the desired low-level output voltage (V_{OL}).

10 Power Supply Recommendations

These devices operate from an input voltage supply range between 1.7 V and 5.5 V.

11 Layout

11.1 Layout Guidelines

A power supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV40x1 output stage, higher than normal quiescent current can be drawn from the power supply when the output transitions. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

11.2 Layout Example

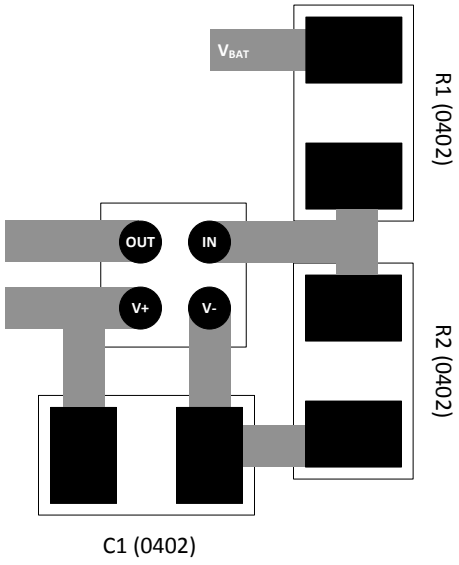


図 11-1. Layout Example

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.3 Trademarks

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12.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4021R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
TLV4021R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	6	Samples
TLV4021S5MYKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Q	Samples
TLV4021S5YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
TLV4031R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1	Samples
TLV4031R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
TLV4041R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	2	Samples
TLV4041R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
TLV4041R5DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23XT	Samples
TLV4041R5YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A	Samples
TLV4051R1YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
TLV4051R2DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3HQT	Samples
TLV4051R2YKAR	ACTIVE	DSBGA	YKA	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples
TLV4051R5DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23ZT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

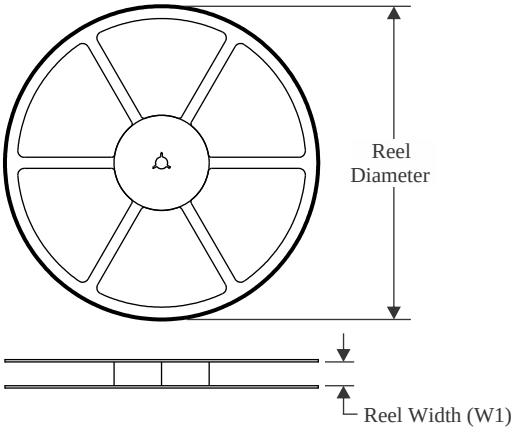
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

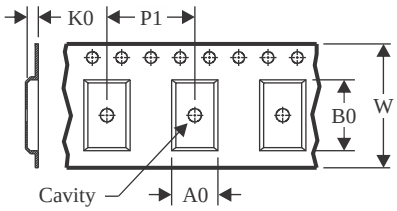
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

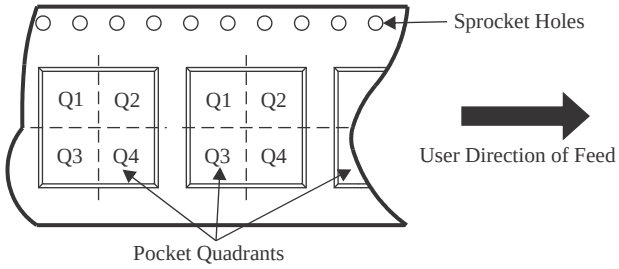


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

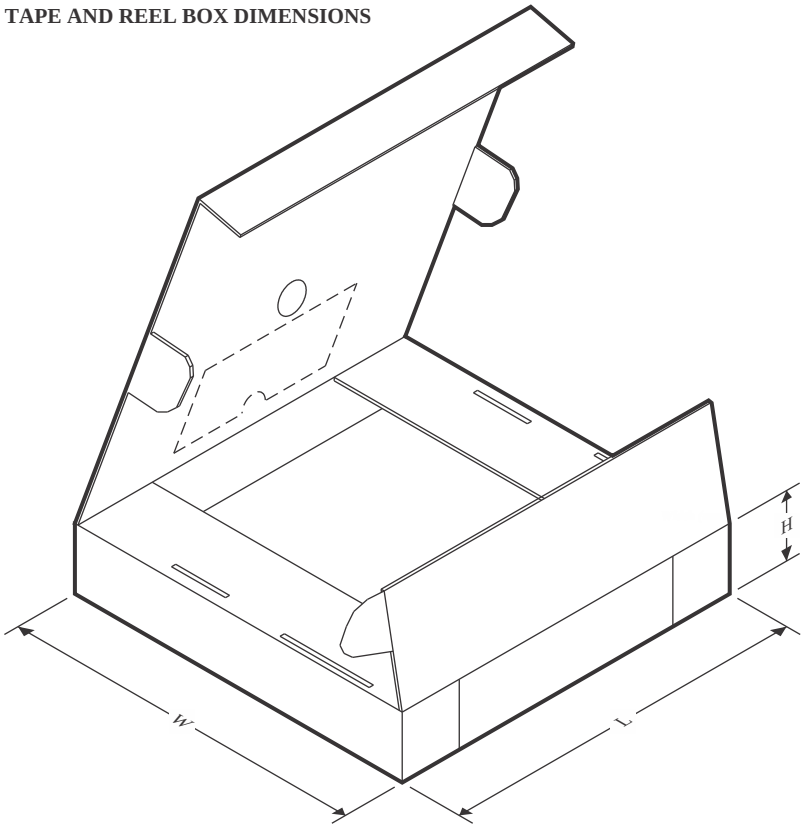
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4021R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021S5MYKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021S5YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4021S5YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4031R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4031R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4041R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4041R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4041R5DBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV4041R5YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4051R1YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4051R2DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV4051R2YKAR	DSBGA	YKA	4	3000	180.0	8.4	0.84	0.84	0.48	4.0	8.0	Q1
TLV4051R5DBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

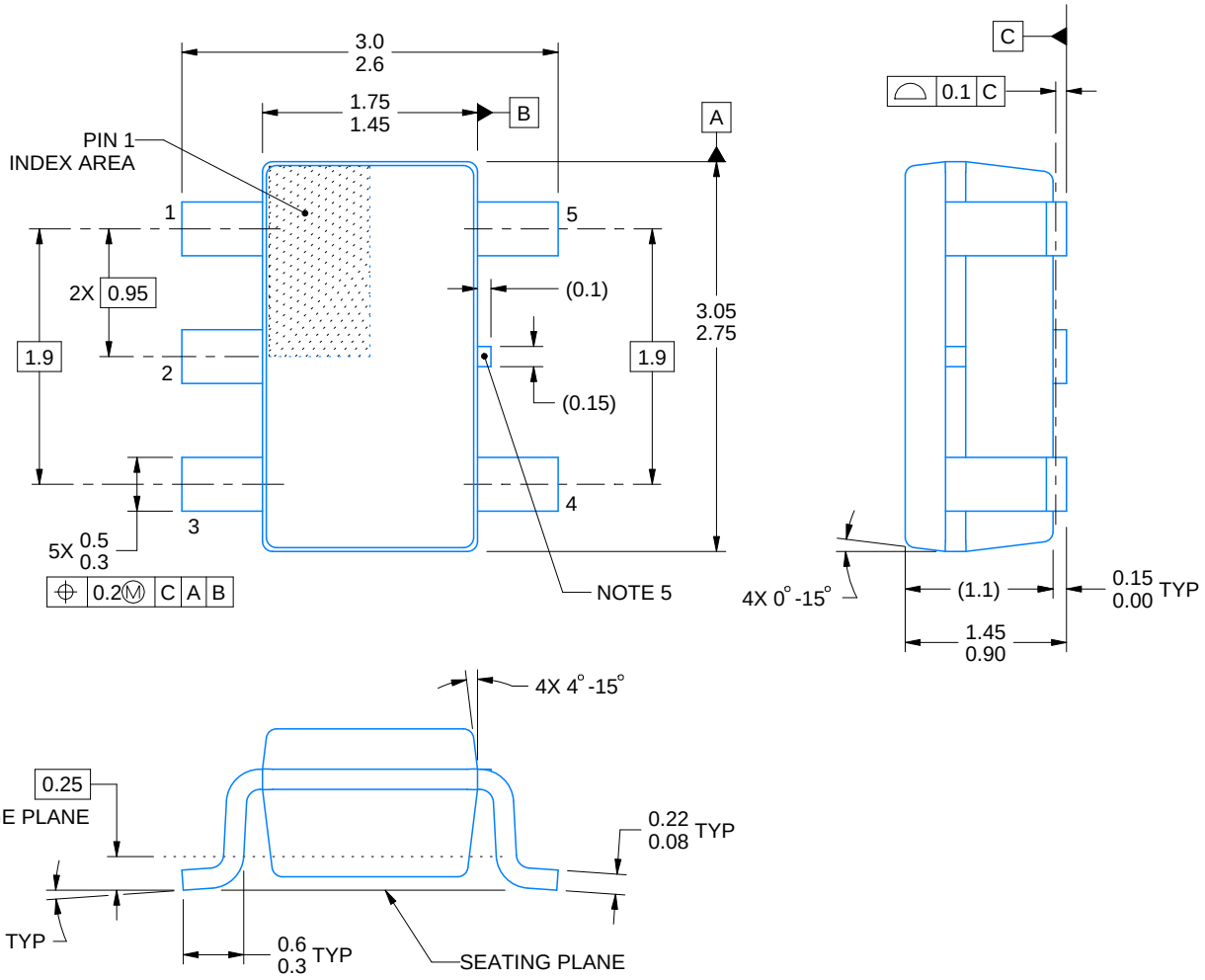
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4021R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021S5MYKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021S5YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4021S5YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4031R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4031R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4041R5DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV4041R5YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4051R1YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4051R2DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV4051R2YKAR	DSBGA	YKA	4	3000	182.0	182.0	20.0
TLV4051R5DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

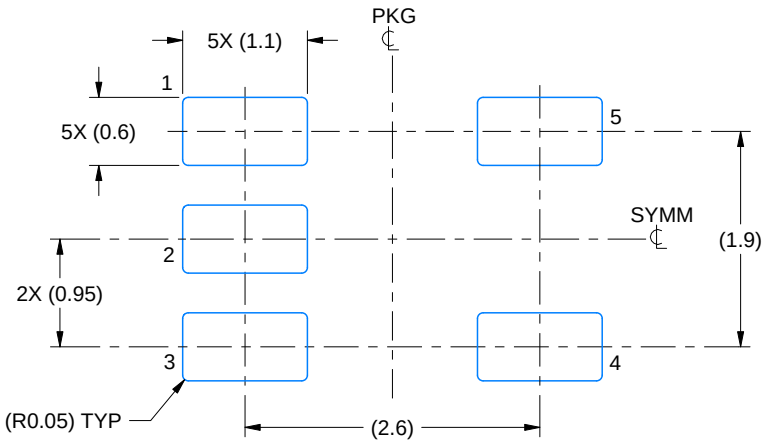
SMALL OUTLINE TRANSISTOR



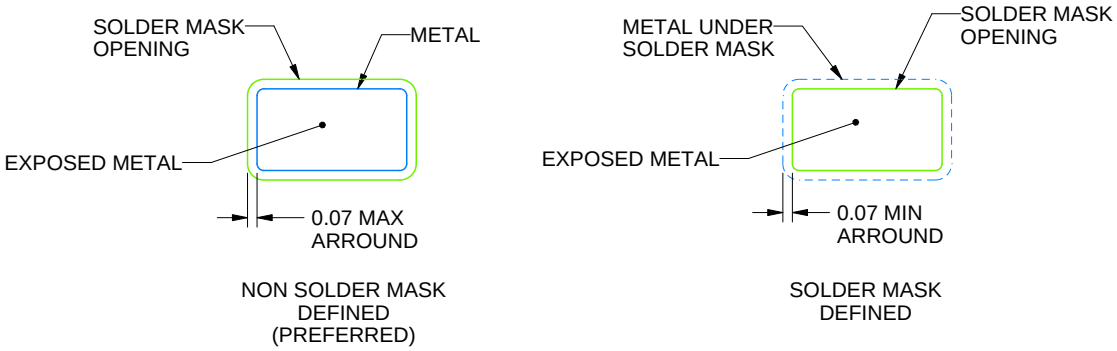
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

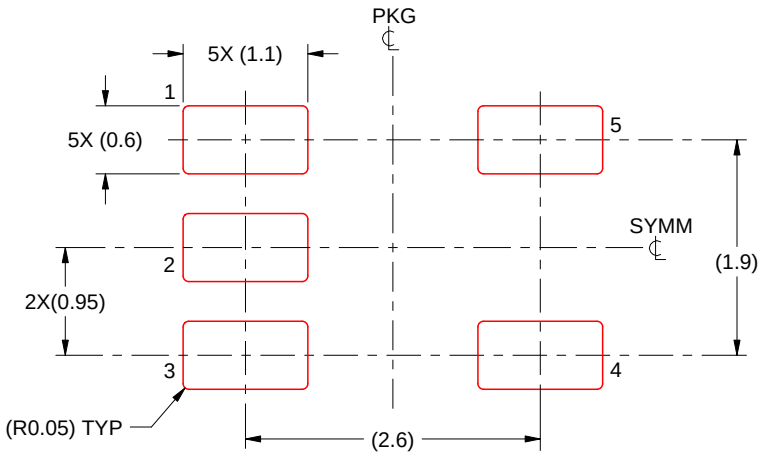


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

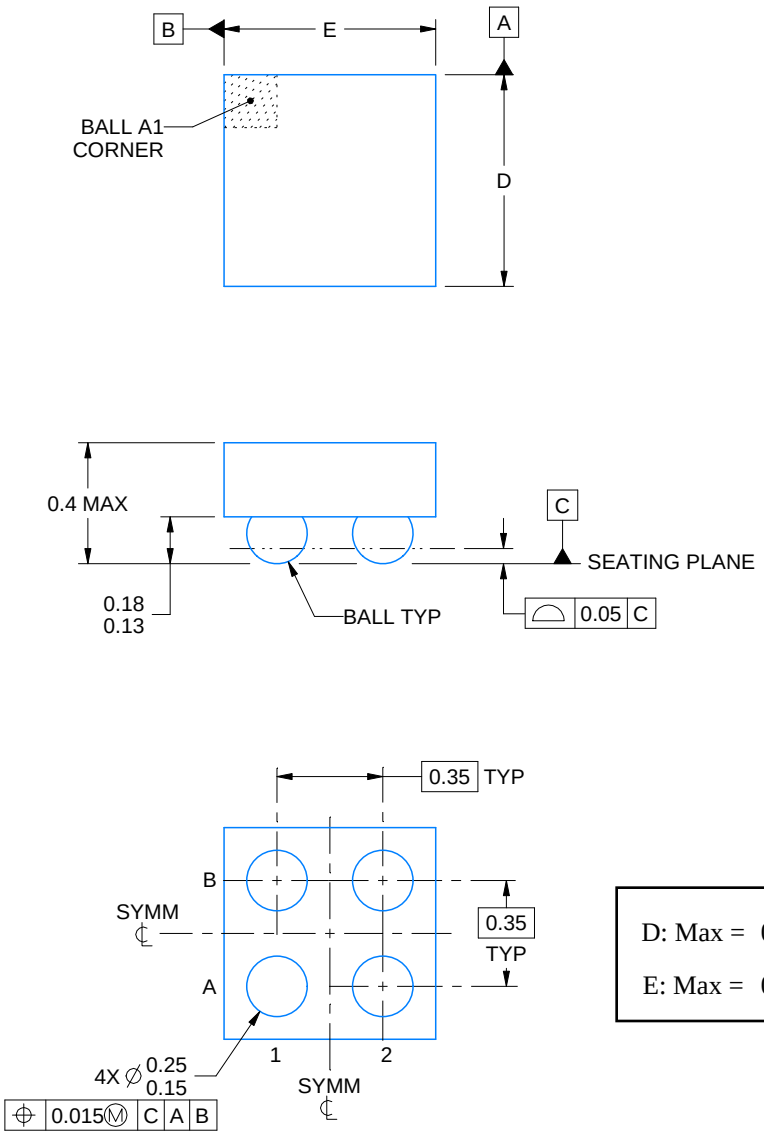
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YKA0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



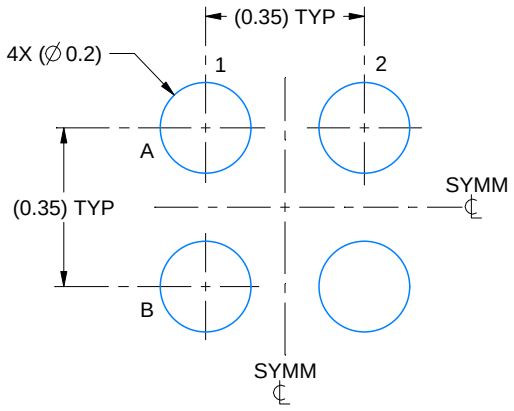
D: Max = 0.76 mm, Min = 0.7 mm

E: Max = 0.76 mm, Min = 0.7 mm

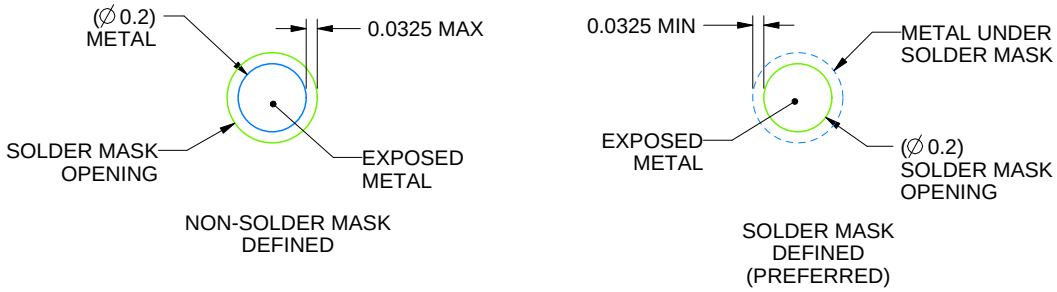
4221909/B 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

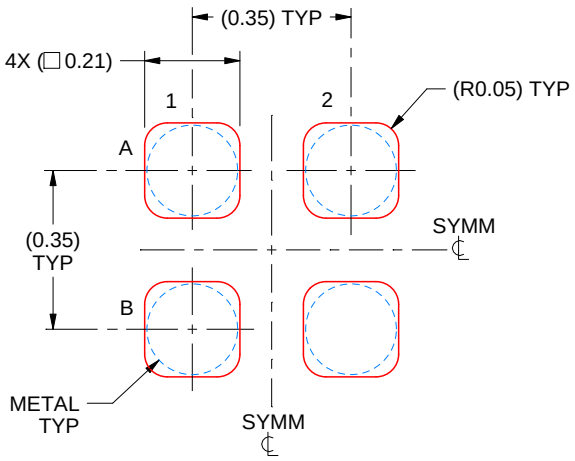


SOLDER MASK DETAILS
NOT TO SCALE

4221909/B 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

4221909/B 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

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