

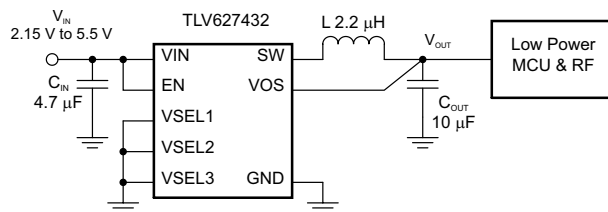
## TLV627432 超低静止電流、高効率降圧コンバータ

### 1 特長

- 入力電圧範囲  $V_{IN}$ : 2.15V~5.5V
- 出力電流最大 400mA
- 非常に小さい動作時静止電流
- 10 $\mu$ A 出力電流時に最高 90% の効率
- パワーセーブ・モード動作
- 出力電圧を選択可能
  - 1.2V~3.3V の 8 つの電圧オプション
- 出力電圧放電
- 低出力電圧リップル
- リップルなし 100% モードへの自動遷移
- RF 対応 DCS-Control™™
- 基板占有面積 < 10mm<sup>2</sup>
- 小型の 1.57mm × 0.88mm 8 ボール WCSP パッケージ

### 2 アプリケーション

- ウェアラブル
- フィットネス・トラッカー
- スマートウォッチ
- 健康状態モニタ
- ©Bluetooth Low Energy、RF4CE、Zigbee
- 高効率、超低消費電力のアプリケーション
- エネルギー・ハーベスト



代表的なアプリケーション

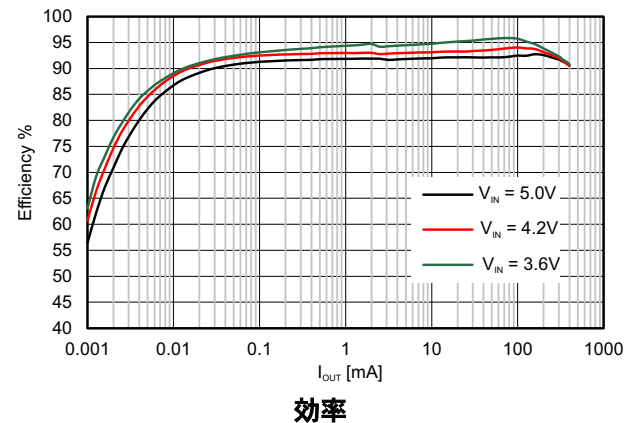
### 3 概要

TLV627432 は、静止電流が 360nA (標準値) ときわめて小さい、高効率の降圧コンバータです。このデバイスは、2.2 $\mu$ H のインダクタと 10 $\mu$ F の出力コンデンサで動作するよう最適化されています。このデバイスは、DCS-Control™™ を使用しており、1.2MHz (標準値) のスイッチング周波数で動作します。パワーセーブ・モードでは、10 $\mu$ A 以下の負荷電流範囲まで軽負荷時効率を維持できます。TLV627432 は、300mA の出力電流を供給できます。TLV627432 には 1.2 V~3.3 V の 8 つのプログラム可能な出力電圧があり、3 本のピンで選択できます。TLV627432 は小さな出力コンデンサだけで、低い出力電圧リップルと低ノイズを実現するよう最適化されています。入力電圧が出力電圧に近づく、デバイスはリップルなしの 100% モードに移行し、出力リップル電圧の増加を防止します。この動作モードでは、デバイスはスイッチングを停止し、ハイサイドの MOSFET スイッチがオンになります。

#### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
TLV627432	DSBGA (8)	1.57mm × 0.88mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision A (December 2019) to Revision B (March 2021)</b>	<b>Page</b>
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1

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<b>Changes from Revision * (June 2016) to Revision A (December 2019)</b>	<b>Page</b>
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## 5 Device Comparison Table

T <sub>A</sub>	PART NUMBER	OUTPUT VOLTAGE SETTINGS (VSEL 1 - 3)	OUTPUT CURRENT	PACKAGE MARKING
-40°C to 85°C	TLV627432	1.2 V, 1.5 V, 1.8 V, 2.1 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V	400 mA	160322

## 6 Pin Configuration and Functions

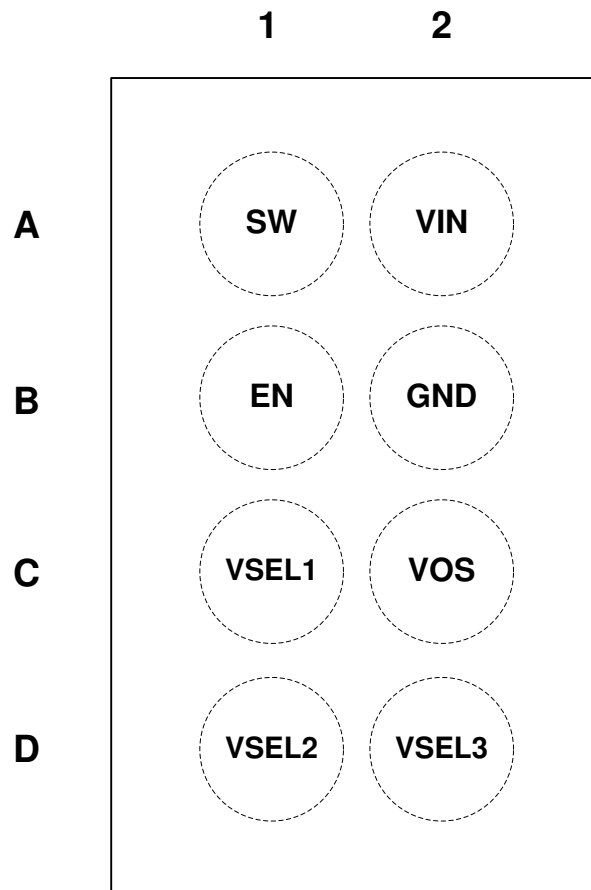


图 6-1. 8-Pin DSBGA YFP Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	A2	PWR	$V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor of 4.7 $\mu$ F is required.
SW	A1	OUT	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	B2	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VOS	C2	IN	Feedback pin for the internal feedback divider network and regulation loop. Discharges $V_{OUT}$ when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
VSEL3	D2	IN	Output voltage selection pins. See 表 6-2 for $V_{OUT}$ selection. These pin must be terminated. The pins can be dynamically changed during operation.
VSEL2	D1		
VSEL1	C1		
EN	B1	IN	High level enables the devices, low level turns the device off. The pin must be terminated.

**表 6-2. Output Voltage Setting**

Output Voltage Setting $V_{OUT}$ [V]	VSEL Setting		
TLV627432	VSEL3	VSEL2	VSEL1
1.2	0	0	0
1.5	0	0	1
1.8	0	1	0
2.1	0	1	1
2.5	1	0	0
2.8	1	0	1
3.0	1	1	0
3.3	1	1	1

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage <sup>(2)</sup>	V <sub>IN</sub>	-0.3	6	V
	SW	-0.3	V <sub>IN</sub> + 0.3V	V
	EN, VSEL1-3	-0.3	V <sub>IN</sub> + 0.3V	V
	VOS	-0.3	3.7	V
Operating junction temperature, T <sub>J</sub>		-40	125	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal GND.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Supply voltage V <sub>IN</sub>		2.15		5.5	V
I <sub>OUT</sub>	Device output current	5.5V ≥ V <sub>IN</sub> ≥ (V <sub>OUTnom</sub> + 0.7V) ≥ 2.15V			300	mA
		5.5V ≥ V <sub>IN</sub> ≥ (V <sub>OUTnom</sub> + 0.7V) ≥ 3V			400	
T <sub>J</sub>	Operating junction temperature range		-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV627432	UNIT
		YFP Package (DSBGA)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	103	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	1.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	20	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	20	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$V_{IN} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  typical values are at  $T_A = 25^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY</b>							
$I_Q$	Operating quiescent current	$EN = V_{IN}$ , $I_{OUT} = 0\mu A$ , $V_{OUT} = 1.8V$ , device not switching		360	1800	nA	
		$EN = V_{IN}$ , $I_{OUT} = 0mA$ , $V_{OUT} = 1.8V$ , device switching		460			
$I_{SD}$	Shutdown current	$EN = GND$ , shutdown current into $V_{IN}$		70	1000	nA	
$V_{TH\_UVLO+}$	Undervoltage lockout threshold	Rising $V_{IN}$		2.075	2.15	V	
$V_{TH\_UVLO-}$		Falling $V_{IN}$		1.925	2		
<b>INPUTS (EN, VSEL1-3)</b>							
$V_{IH\ TH}$	High level input threshold	$2.2V \leq V_{IN} \leq 5.5V$			1.1	V	
$V_{IL\ TH}$	Low level input threshold	$2.2V \leq V_{IN} \leq 5.5V$	0.4			V	
$I_{IN}$	Input bias Current			10	25	nA	
<b>POWER SWITCHES</b>							
$R_{DS(ON)}$	High side MOSFET on-resistance	$I_{OUT} = 50mA$		0.45	1.12	$\Omega$	
	Low Side MOSFET on-resistance			0.22	0.65		
$I_{LIMF}$	High side MOSFET switch current limit	$3.0V \leq V_{IN} \leq 5.5V$	590	650	800	mA	
	Low side MOSFET switch current limit			650			
<b>OUTPUT VOLTAGE DISCHARGE</b>							
$R_{DSCH\_VOS}$	MOSFET on-resistance	$EN = GND$ , $I_{VOS} = -10mA$ into VOS pin		30	65	$\Omega$	
$I_{IN\_VOS}$	Bias current into VOS pin	$EN = V_{IN}$ , $V_{OUT} = 2V$		40	1010	nA	
<b>AUTO 100% MODE TRANSITION</b>							
$V_{TH\_100+}$	Auto 100% Mode leave detection threshold (1)	Rising $V_{IN}$ , 100% Mode is left with $V_{IN} = V_{OUT} + V_{TH\_100+}$	150	250	350	mV	
$V_{TH\_100-}$	Auto 100% Mode enter detection threshold (1)	Falling $V_{IN}$ , 100% Mode is entered with $V_{IN} = V_{OUT} + V_{TH\_100-}$	85	200	290		
<b>OUTPUT</b>							
$I_{LIM\_softstart}$	High side softstart switch current limit	$EN = \text{low to high}$		80	150	200	mA
	Low side softstart switch current limit				150		
$V_{OUT}$	Output voltage range	Output voltages are selected with pins VSEL 1 - 3		1.2		3.3	V
	Output voltage accuracy	$I_{OUT} = 10mA$ , $V_{OUT} = 1.8V$		-2.5	0%	2.5	
		$I_{OUT} = 100mA$ , $V_{OUT} = 1.8V$		-2	0%	2	
	DC output voltage load regulation	$V_{OUT} = 1.8V$			0.001		%/mA
DC output voltage line regulation	$V_{OUT} = 1.8V$ , $I_{OUT} = 100mA$ , $2.5V \leq V_{IN} \leq 5.0V$			0		%/V	

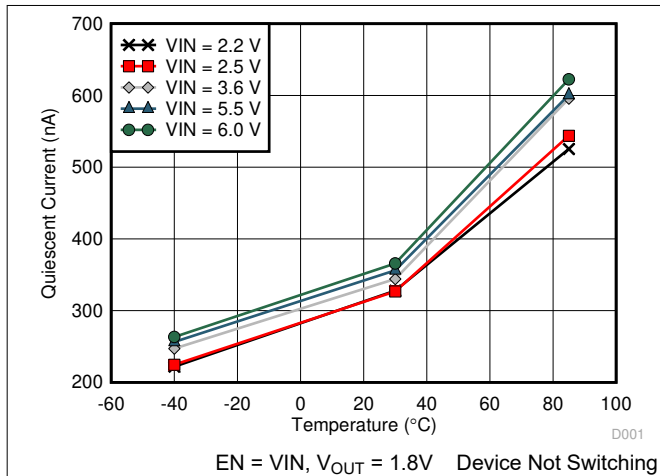
- (1)  $V_{IN}$  is compared to the programmed output voltage ( $V_{OUT}$ ). When  $V_{IN} - V_{OUT}$  falls below  $V_{TH\_100-}$ , the device enters 100% Mode by turning the high side MOSFET on. The 100% Mode is exited when  $V_{IN} - V_{OUT}$  exceeds  $V_{TH\_100+}$  and the device starts switching. The hysteresis for the 100% Mode detection threshold  $V_{TH\_100+} - V_{TH\_100-}$  will always be positive and will be approximately 50 mV(typ)

## 7.6 Timing Requirements

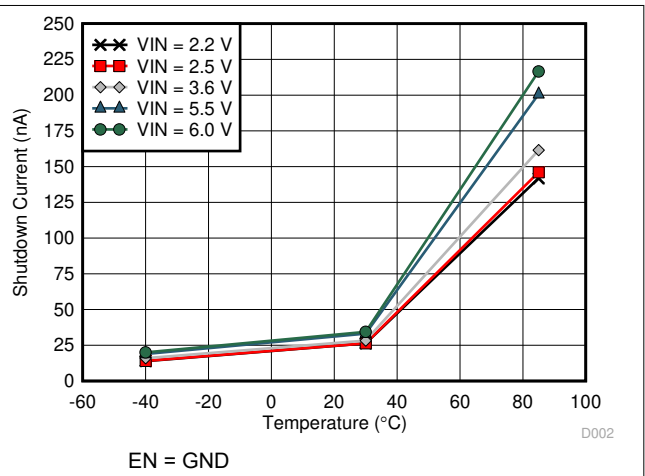
$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $85^{\circ}C$  typical values are at  $T_A = 25^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ONmin}$	Minimum ON time	$V_{OUT} = 2.0V$ , $I_{OUT} = 0\text{ mA}$		225		ns
$t_{OFFmin}$	Minimum OFF time			50		ns
$t_{Startup\_delay}$	Regulator start up delay time	From transition EN = low to high until device starts switching		10	25	ms
$t_{Softstart}$	Softstart time	$2.5V \leq V_{IN} \leq 5.5V$ , EN = $V_{IN}$		700	1200	$\mu s$

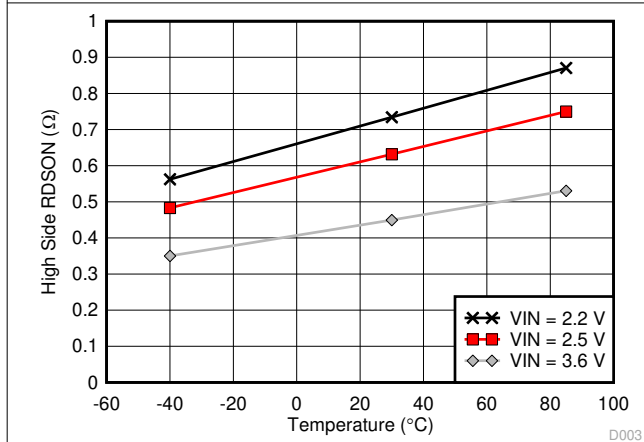
## 7.7 Typical Characteristics



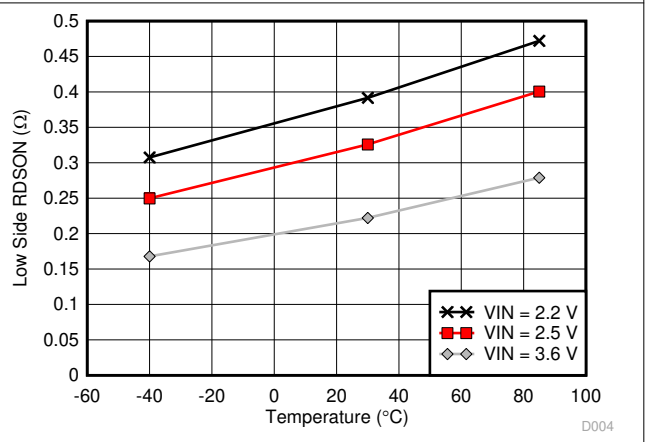
**7-1. Quiescent Current vs Temperature**



**7-2. Shutdown Current  $I_{SD}$  vs Temperature**



**7-3. High Side  $R_{DS(on)}$  vs Temperature**



**7-4. Low-side  $R_{DS(on)}$  vs Temperature**

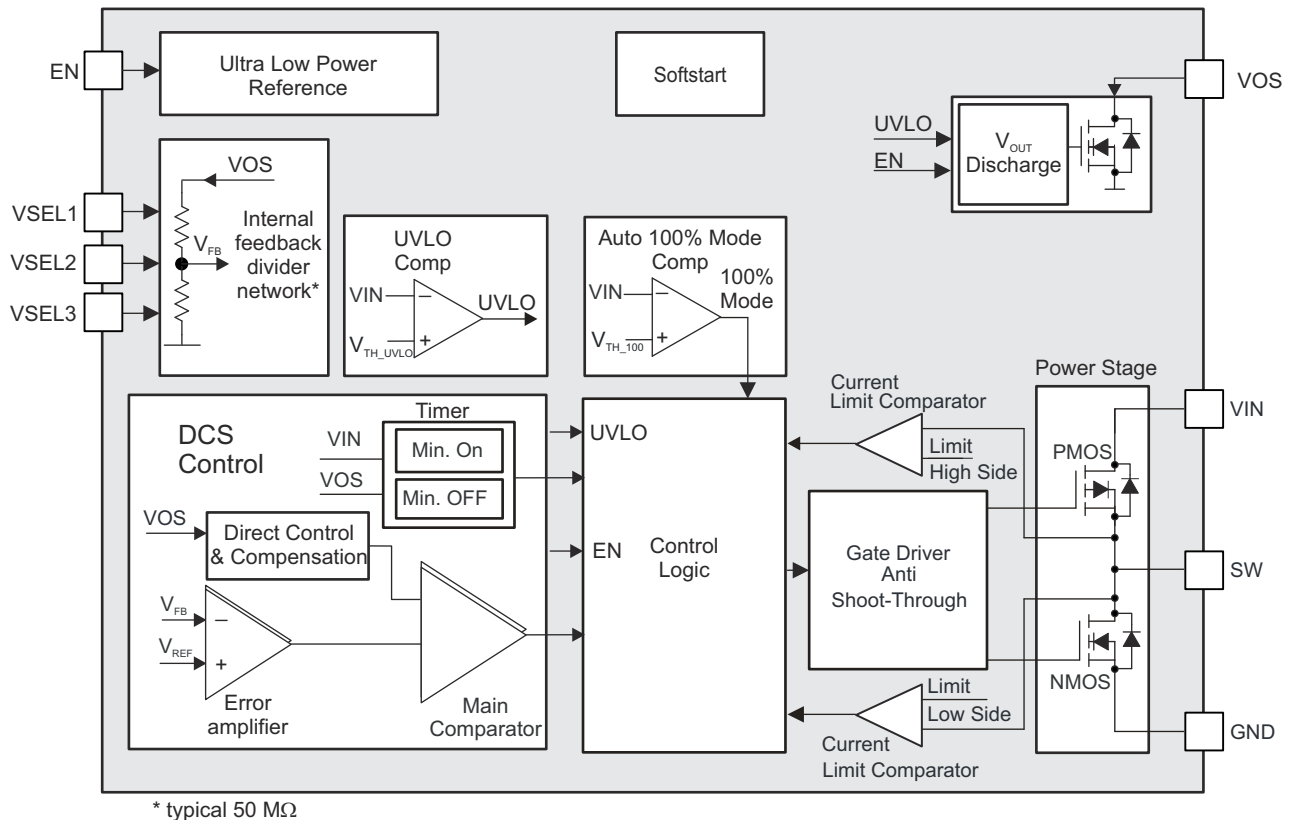


## 8 Detailed Description

### 8.1 Overview

The TLV627432 is a high frequency step down converter with ultra low quiescent current. The device operates with a quasi fixed switching frequency typically at 1.2 MHz. Using TI's DCS-Control™ topology the device extends the high efficiency operation area down to a few microamperes of load current during Power Save Mode Operation.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 DCS-Control™

TI's™ DCS-Control (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction mode. The switching frequency is typically 1.2 MHz with a controlled frequency variation depending on the input voltage and load current. If the load current decreases, the converter seamlessly enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the

transition from PWM to Power Save Mode is seamless with minimum output voltage ripple. The TLV627432 offers both excellent DC voltage and superior load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

### 8.3.2 Power Save Mode Operation

In Power Save Mode the device operates in PFM (Pulse Frequency Modulation) that generates a single switching pulse to ramp up the inductor current and recharges the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption of TLV627432 is reduced to 360 nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance feedback divider network and an optimized Power Save Mode operation.

### 8.3.3 Output Voltage Selection

The TLV627432 doesn't require an external resistor divider network to program the output voltage. The device integrates a high impedance feedback resistor divider network that is programmed by the pins VSEL1-3. TLV627432 supports an output voltage range from 1.2 V to 3.3 V. The output voltage is programmed according to [表 6-2](#). The output voltage can be changed during operation. This can be used for simple dynamic output voltage scaling.

### 8.3.4 Output Voltage Discharge of the Buck Converter

The device provides automatic output voltage discharge when EN is pulled low or the UVLO is triggered. The output of the buck converter is discharged over VOS. Because of this the output voltage will ramp up from zero once the device is enabled again. This is very helpful for accurate start-up sequencing.

### 8.3.5 Undervoltage Lockout UVLO

To avoid misoperation of the device at low input voltages, an undervoltage lockout is used. The UVLO shuts down the device at a maximum voltage level of 2.0 V. The device will start at a UVLO level of 2.15 V.

### 8.3.6 Short circuit protection

The TLV627432 integrates a current limit on the high side, as well on the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the switch current decreases below the low side MOSFET current limit. Once the low side MOSFET current limit trips, the low side MOSFET is turned off and the high side MOSFET turns on again.

## 8.4 Device Functional Modes

### 8.4.1 Enable and Shutdown

The device is turned on with EN=high. With EN=low the device enters shutdown. This pin must be terminated.

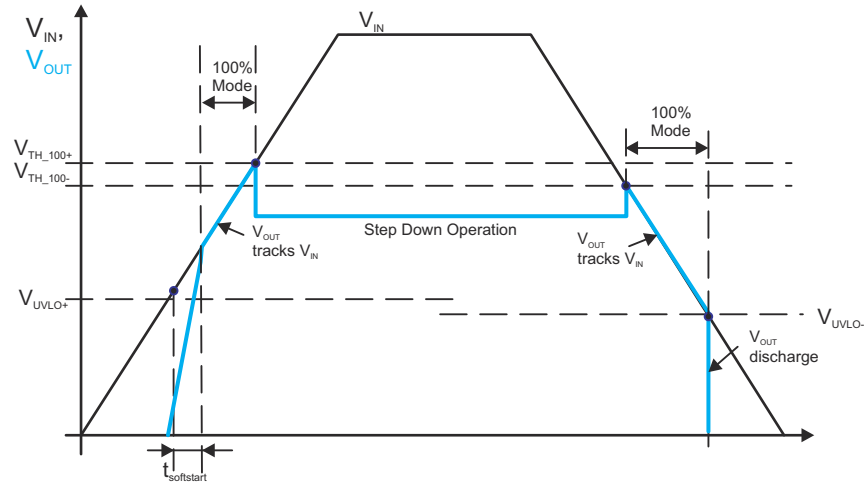
### 8.4.2 Device Start-up and Softstart

The device has an internal softstart to minimize input voltage drop during start-up. This allows the operation from high impedance battery cells. Once the device is enabled the device starts switching after a typical delay time of 10ms. Then the softstart time of typical 700  $\mu$ s begins with a reduced current limit of typical 150 mA. When this time passed by the device enters full current limit operation. This allows a smooth start-up and the device can start into full load current. Furthermore, larger output capacitors impact the start-up behaviour of the DC/DC converter. Especially when the output voltage does not reach its nominal value after the typical soft-start time of 700  $\mu$ s, has passed.

### 8.4.3 Automatic Transition Into No Ripple 100% Mode

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. It connects the output  $V_{OUT}$  via the inductor and the internal high side MOSFET switch to the input  $V_{IN}$ , once the input voltage  $V_{IN}$  falls below the 100% mode enter threshold,  $V_{TH\_100}$ . The DC/DC regulator is turned off, switching stops and therefore no output voltage ripple is generated. Since the

output is connected to the input, the output voltage follows the input voltage minus the voltage drop across the internal high side switch and the inductor. Once the input voltage increases and trips the 100% mode exit threshold,  $V_{TH\_100+}$ , the DC/DC regulator turns on and starts switching again. See [8-1](#) and [9-14](#).



**8-1. Automatic Transition into 100% Mode**

## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The TLV627432 is a high efficiency step down converter with ultra low quiescent current of typically 360 nA. The device operates with a tiny 2.2- $\mu$ H inductor and 10- $\mu$ F output capacitor over the entire recommended operation range. A dedicated measurement set-up is required for the light load efficiency measurement and device quiescent current due to the operation in the sub microampere range. In this range any leakage current in the measurement set-up will impact the measurement results.

### 9.2 Typical Application

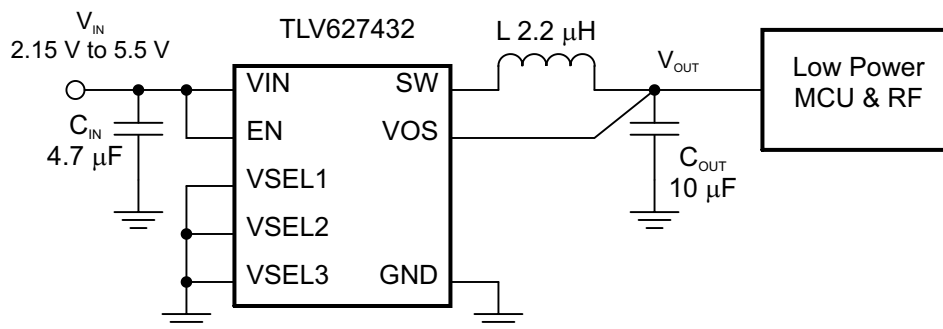


図 9-1. TLV627432 Typical Application Circuit

#### 9.2.1 Design Requirements

The TLV627432 is a highly integrated DC/DC converter. The output voltage is set via a VSEL pin interface. The design guideline provides a component selection to operate the device within the recommended operating conditions.

表 9-1 shows the list of components for the Application Characteristic Curves

表 9-1. Components for Application Characteristic Curves

Reference	Description	Value	Manufacturer <sup>(1)</sup>
TLV627432	360nA I <sub>q</sub> step down converter		Texas Instruments
C <sub>IN</sub>	Ceramic capacitor, GRM155R61C475ME15	4.7 $\mu$ F	Murata
C <sub>OUT</sub>	Ceramic capacitor, GRM155R60J106ME11	10 $\mu$ F	Murata
L	Inductor DFE201610C	2.2 $\mu$ H	Toko

(1) See [Third-Party Products Disclaimer](#)

#### 9.2.2 Detailed Design Procedure

The first step in the design procedure is the selection of the output filter components. To simplify this process, 表 9-2 outlines possible inductor and capacitor value combinations.

**表 9-2. Recommended LC Output Filter Combinations**

Inductor Value [μH] <sup>(2)</sup>	Output Capacitor Value [μF] <sup>(1)</sup>				
	4.7μF	10μF	22μF	47μF	100μF
2.2	√	√ <sup>(3)</sup>	√	√	

- (1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.  
(2) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.  
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

### 9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current ( $\Delta I_L$ ) decreases with higher inductance and increases with higher  $V_{IN}$  or  $V_{OUT}$  and can be estimated according to 式 1.

式 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with 式 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit,  $I_{LIMF}$ .

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- $f$  = switching frequency
- $L$  = inductor value
- $\Delta I_L$  = Peak to Peak inductor ripple current
- $I_{Lmax}$  = Maximum Inductor current

The table below shows a list of possible inductors.

**表 9-3. List of Possible Inductors**

INDUCTANCE [μH]	DIMENSIONS [mm <sup>3</sup> ]	INDUCTOR TYPE	ISAT/DCR	SUPPLIER	COMMENT
2.2	2.0 x 1.6 x 1.0	DPE201610C	1.4 A/170 mΩ	TOKO	Efficiency plot
2.2	2.0 x 1.25 x 1.0	MIPSZ2012D 2R2	0.7 A/230 mΩ	FDK	
2.2	2.0 x 1.2 x 1.0	744 797 752 22	0.7 A/200 mΩ	Würth Elektronik	
2.2	1.6 x 0.8 x 0.8	MDT1608-CH2R2M	0.7 A/300 mΩ	TOKO	

### 9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TLV627432 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

### 9.2.2.3 Input Capacitor Selection

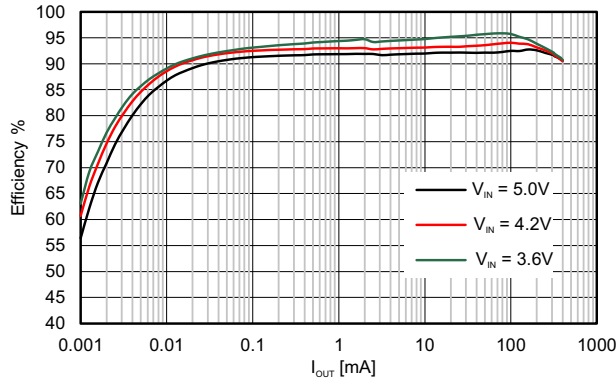
Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications a 4.7-μF input capacitor is sufficient. The

input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. [表 9-4](#) shows a selection of input and output capacitors.

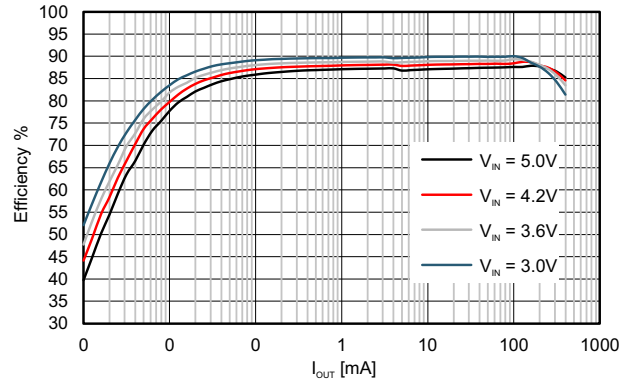
**表 9-4. List of Possible Capacitors**

CAPACITANCE [ $\mu$ F]	SIZE	CAPACITOR TYPE	SUPPLIER
4.7	0402	GRM155R61C475ME15	Murata
10	0402	GRM155R60J106ME11	Murata

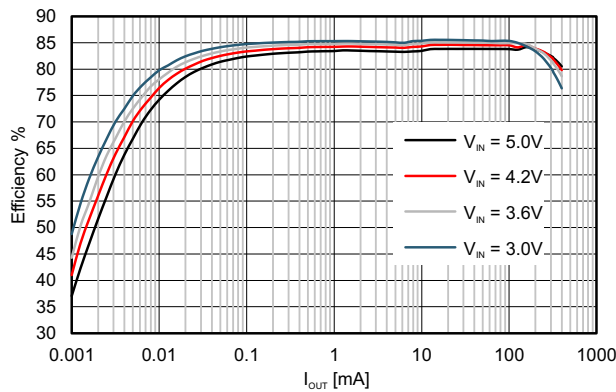
### 9.2.3 Application Curves



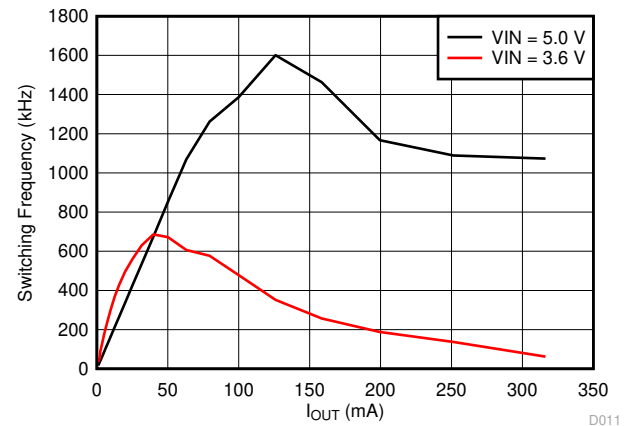
9-2. Efficiency vs Load Current,  $V_{OUT} = 3.3\text{ V}$



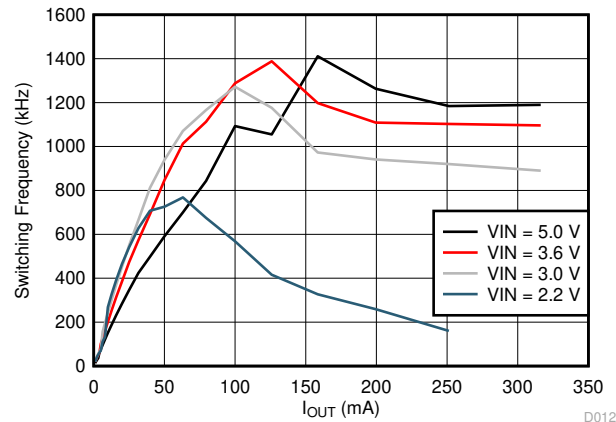
9-3. Efficiency vs Load Current;  $V_{OUT} = 1.8\text{ V}$



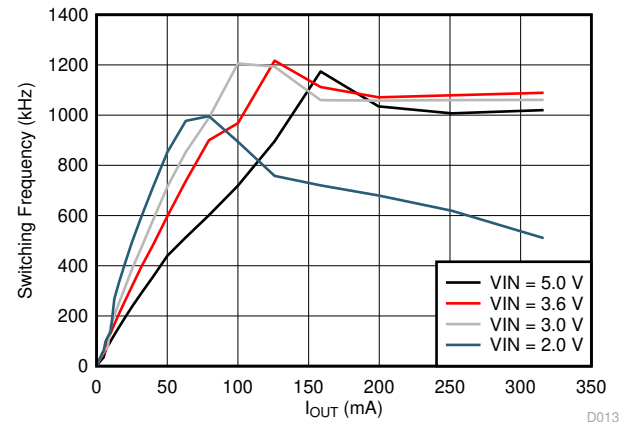
9-4. Efficiency vs Load Current;  $V_{OUT} = 1.2\text{ V}$



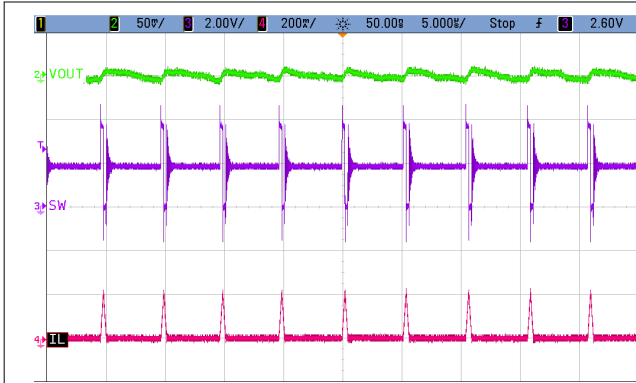
9-5. Switching Frequency vs Load Current  
 $V_{OUT} = 3.3\text{ V}$



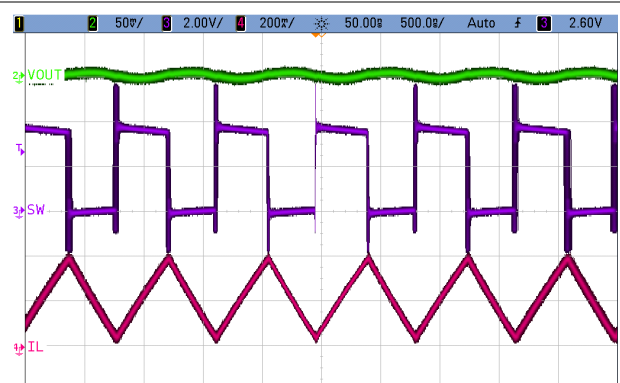
9-6. Switching Frequency vs Load Current  
 $V_{OUT} = 1.8\text{ V}$



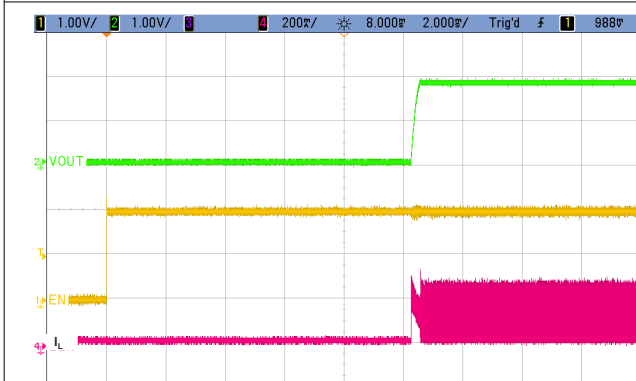
9-7. Switching Frequency vs Load Current  
 $V_{OUT} = 1.2\text{ V}$



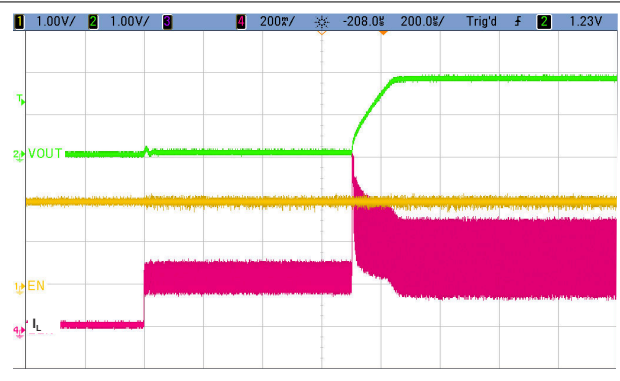
**9-8. PFM (Power Save Mode) Mode Operation**



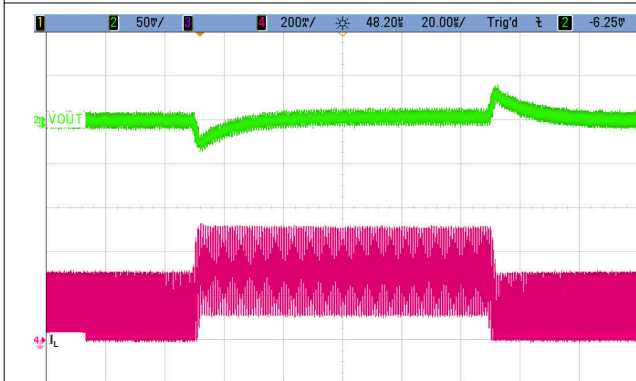
**9-9. PWM Mode Operation**



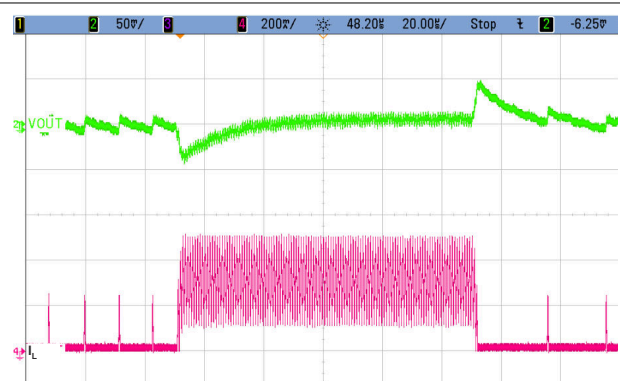
**9-10. Startup Into 100 mA Electronic Load EN Delay + Soft-Start Delay**



**9-11. Startup Into 300 mA Electronic Load Soft-Start Delay**

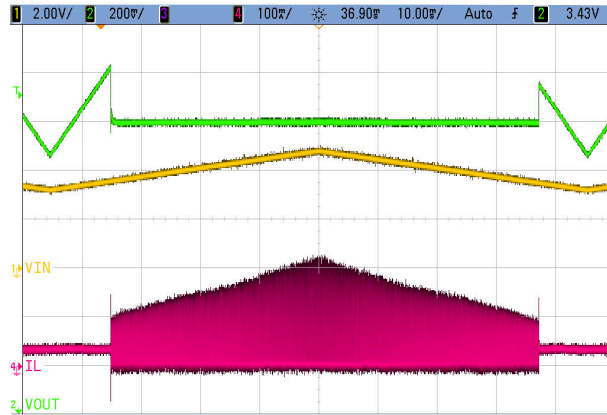


**9-12. Load Transient Response; 100 mA to 290 mA**



**9-13. Load Transient Response; 5 mA to 290 mA**





**9-14. 100% Mode Entry and Leave Operation**  
**I<sub>OUT</sub> = 30 mA**

## 10 Power Supply Recommendations

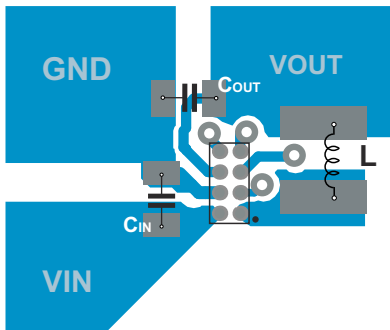
The power supply must provide a current rating according to the supply voltage, output voltage and output current of the TLV627432.

## 11 Layout

### 11.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the IC pins VIN and GND. This is the most critical component placement.
- The  $V_{OS}$  line is a sensitive high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources.

### 11.2 Layout Example



11-1. Recommended PCB Layout

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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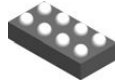
ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.6 用語集

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## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

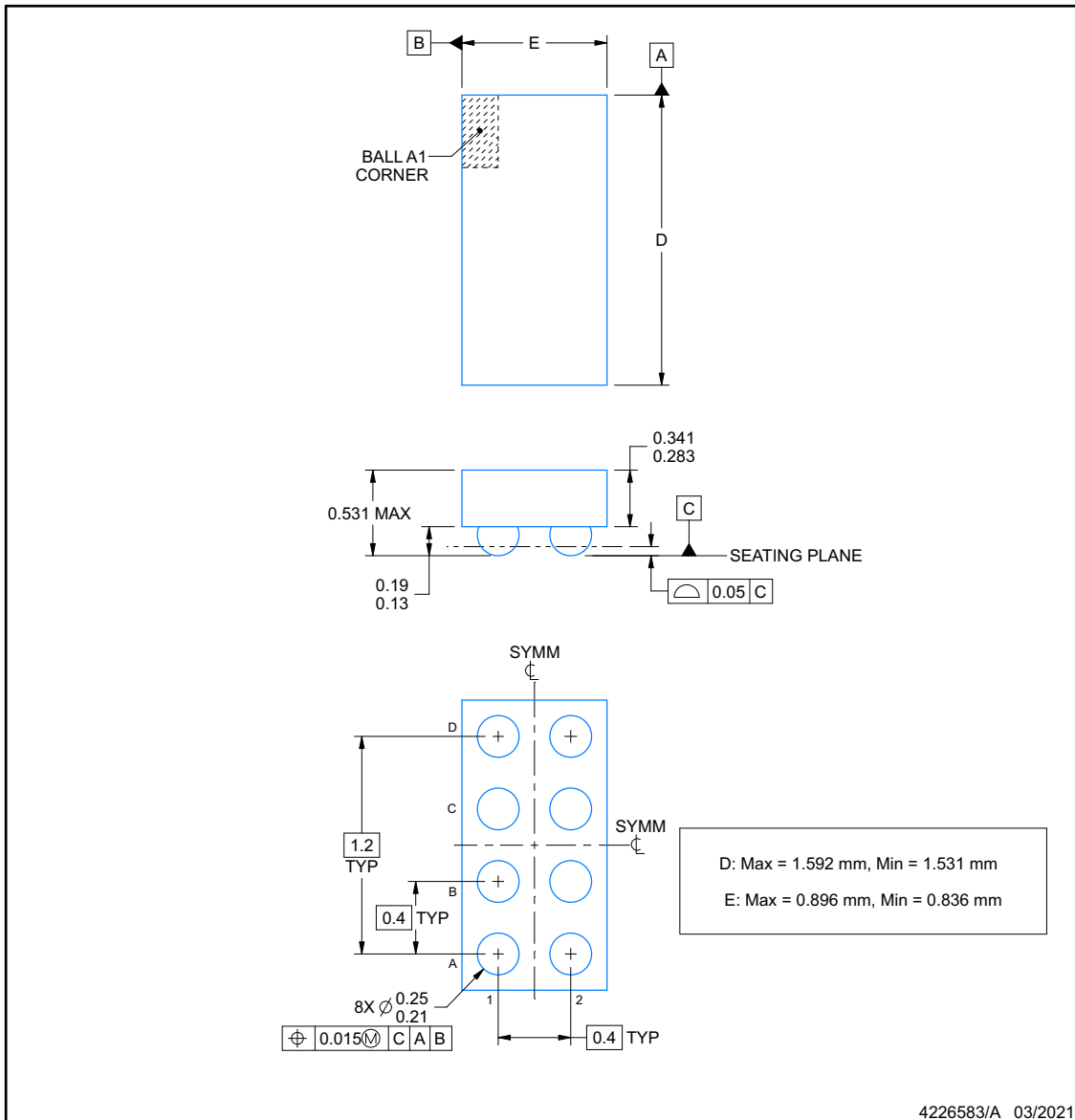


**YFP0008-C01**

**PACKAGE OUTLINE**

**DSBGA - 0.531 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES:

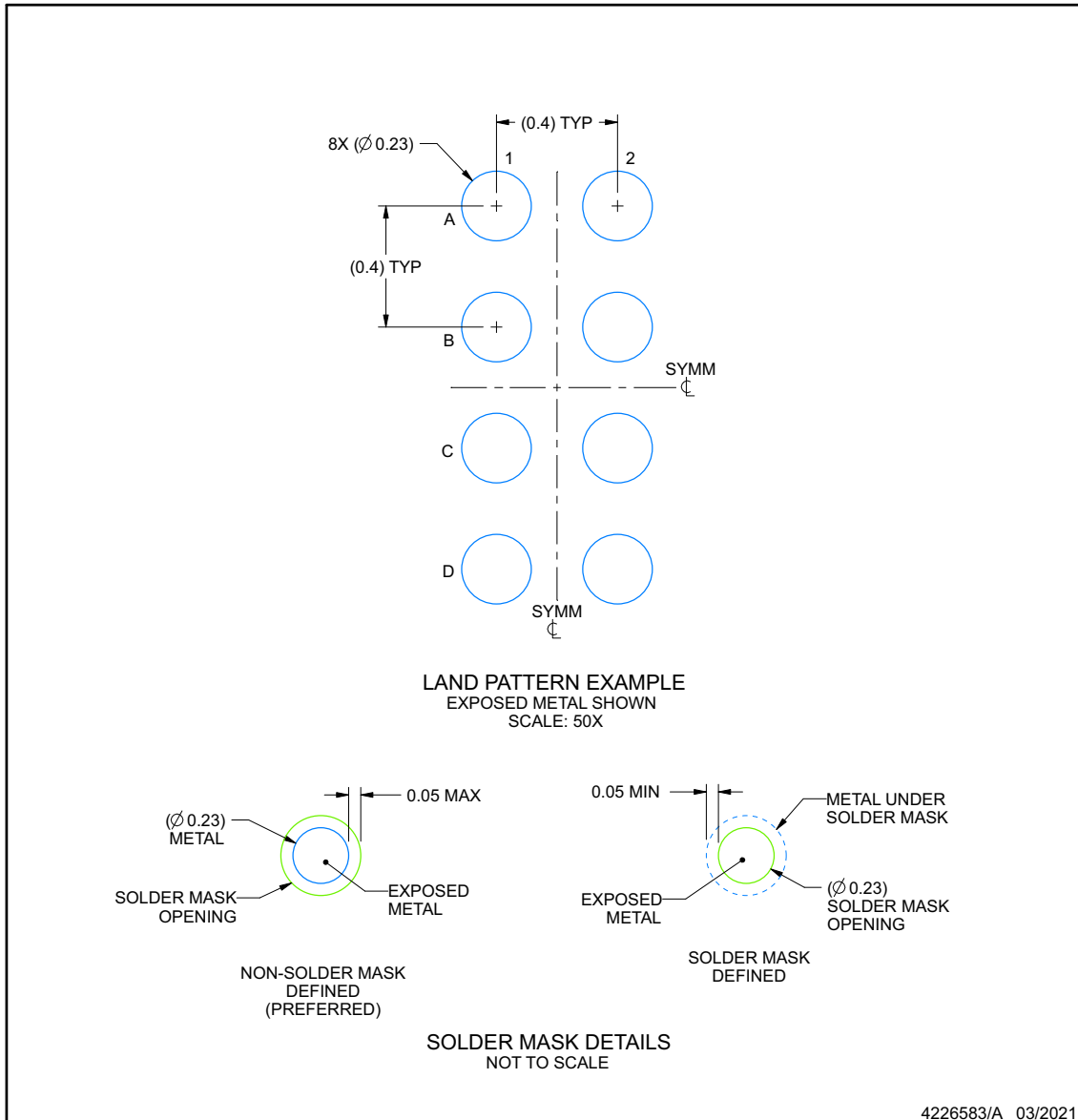
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

**YFP0008-C01**

**DSBGA - 0.531 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

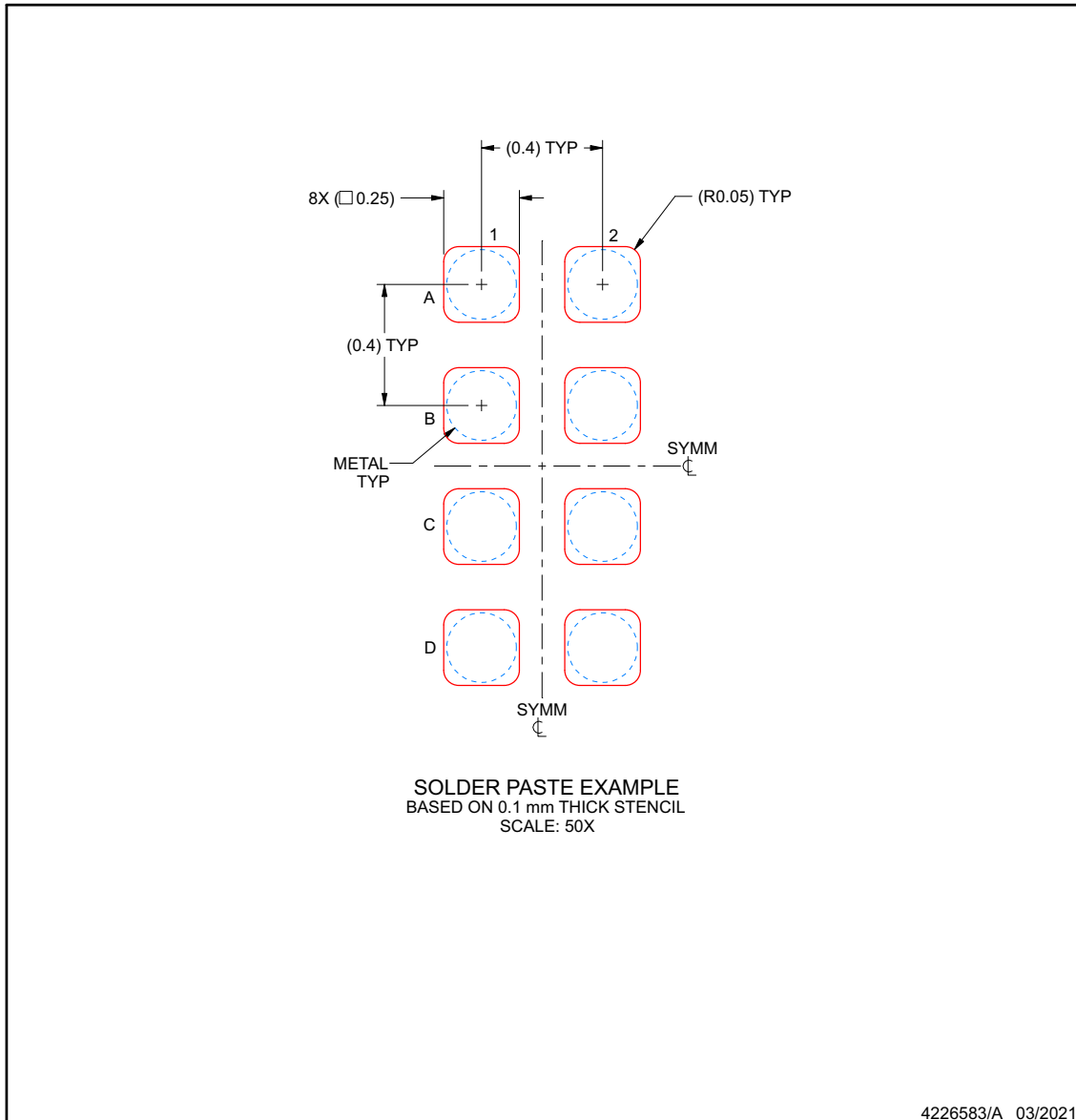
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

**EXAMPLE STENCIL DESIGN**

**YFP0008-C01**

**DSBGA - 0.531 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV627432YFPR	ACTIVE	DSBGA	YFP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	160322	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

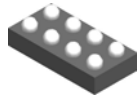
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV627432YFPR	DSBGA	YFP	8	3000	180.0	8.4	0.98	1.68	0.59	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV627432YFPR	DSBGA	YFP	8	3000	182.0	182.0	20.0

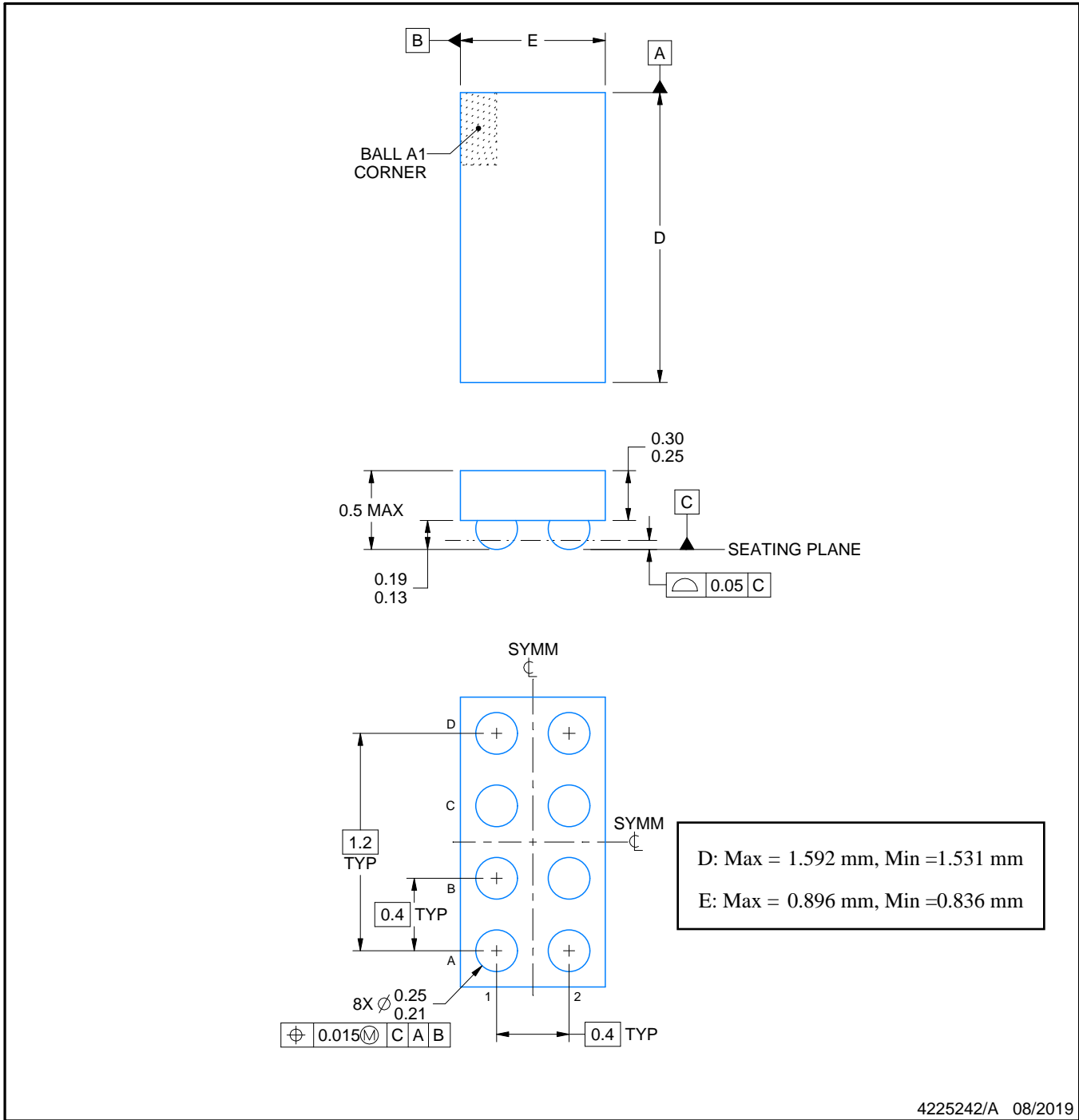
YFP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

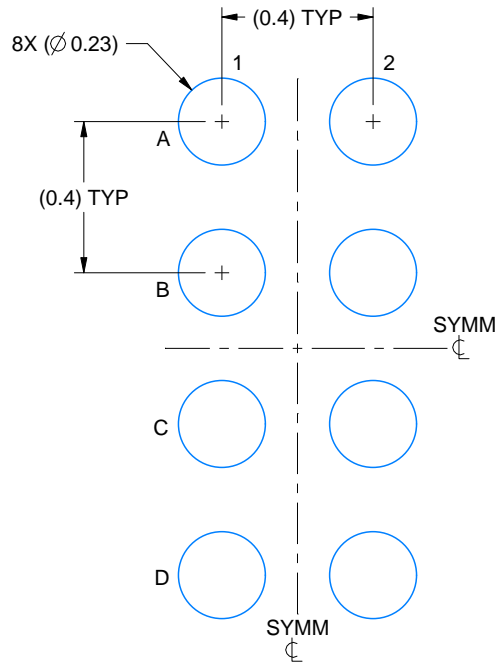
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

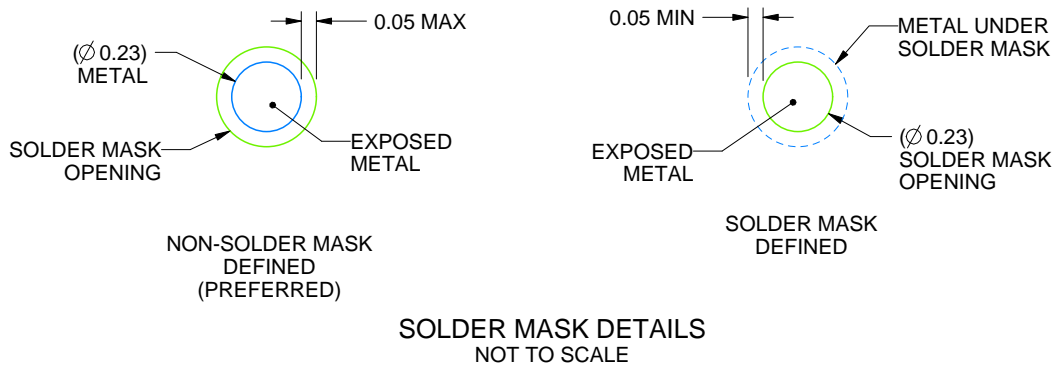
YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 50X



SOLDER MASK DETAILS  
NOT TO SCALE

4225242/A 08/2019

NOTES: (continued)

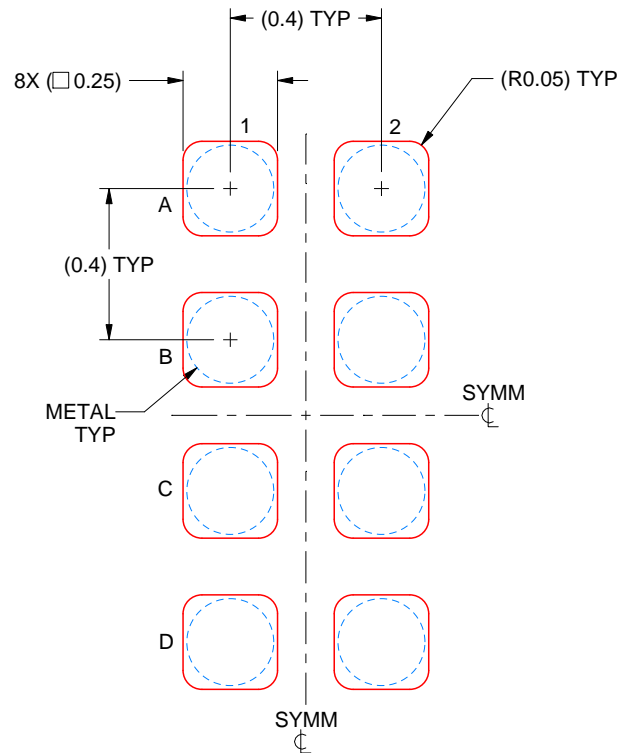
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 50X

4225242/A 08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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