

TLV703x および TLV704x 小型、nanoPower、低電圧コンパレータ

1 特長

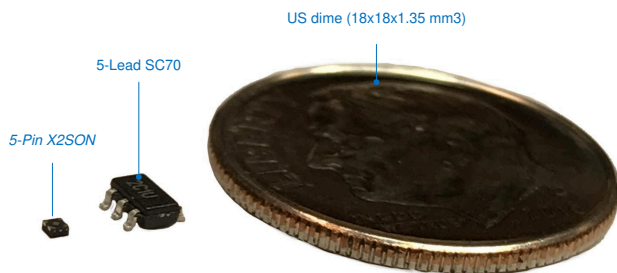
- 超小型の X2SON、WSON、WQFN パッケージ
- 小型の SOT-23、SC70、VSSOP、TSSOP パッケージ
- 広い電源電圧範囲: 1.6V~6.5V
- 静止消費電流: 315nA
- 短い伝搬遅延: 3μs
- レール・ツー・レールの同相入力電圧
- 内部ヒステリシス
- プッシュ・プル出力 (TLV703x)
- オープン・ドレイン出力 (TLV704x)
- オーバードライブ入力についても位相反転なし
- 40°C~125°Cの動作温度

2 アプリケーション

- 携帯電話およびタブレット
- ヘッドセット / ヘッドホン、小型イヤホン
- PC / ノート PC
- ガス検出器
- 煙感知器と熱感知器
- モーション・センサ
- ガス・メーター
- サーボ・ドライブ位置センサ

3 概要

TLV7031/TLV7041 (シングル・チャンネル)、TLV7032/42 (デュアル・チャンネル)、TLV7034/44 (クワッド・チャンネル) は、低電圧の nanoPower コンパレータです。これらのデバイスは、超小型リードレス・パッケージと、標準の 5 ピン SC70、SOT-23、VSSOP および TSSOP パッケージで供給されるため、スマートフォン、スマートメーター、その他の携帯用またはバッテリー駆動のアプリケーションなど、スペースに制約のある設計に適用可能です。



X2SON パッケージと、SC70 および米 10 セント硬貨との比較

TLV703x および TLV704x は、速度と消費電力との両立をうまく実現しており、伝搬遅延は 3μs、静止消費電流は 315nA です。この高速な応答時間と nanoPower との組み合わせを生かして、電力に制約のあるシステムでも、フォルト状況を監視して迅速に応答できます。これらのコンパレータの動作電圧範囲は 1.6V~6.5V で、3V および 5V のシステムと互換性があります。

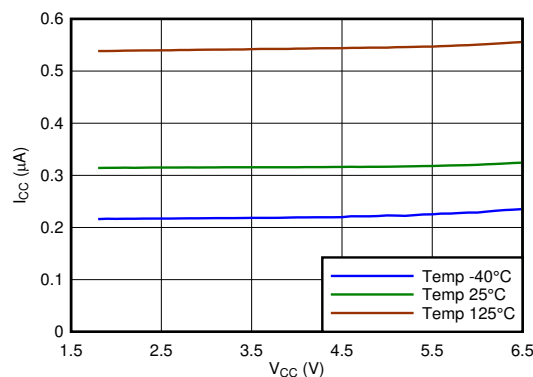
また、TLV703x と TLV704x は、オーバードライブ入力に対しても出力位相が反転しないことが保証されており、内部ヒステリシスが存在するため、ノイズが多い過酷な環境で、緩やかに変動する入力信号をクリーンなデジタル出力に変換する必要がある場合でも、高精度の電圧監視に使用できます。

TLV703x は、LED の制御または容量性負荷の駆動を行う際に数ミリアンペアの電流をシンクおよびソースできるプッシュプル出力段を備えています。TLV704x にはオープン・ドレインの出力段があり、V_{CC} を超える出力レベルが可能であるため、レベル変換器やバイポーラからシングルエンドへのコンバータに適しています。

製品情報

部品番号	パッケージ (ピン数) (1)	本体サイズ (公称)
TLV7031, TLV7041	X2SON (5)	0.80mm × 0.80mm
	SC70 (5)	2.00mm × 1.25mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV7032, TLV7042	VSSOP (8)	3.00mm × 3.00mm
	SOT-23 (8)	2.90mm × 1.60mm
	WSON (8)	2.00mm × 2.00mm
TLV7034, TLV7044	WQFN (16)	3.00mm × 3.00mm
	TSSOP (14)	4.40mm × 5.00mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



I_{CC} と電源電圧との関係



Table of Contents

1 特長	1	7 Detailed Description	18
2 アプリケーション	1	7.1 Overview.....	18
3 概要	1	7.2 Functional Block Diagram.....	18
4 Revision History	2	7.3 Feature Description.....	18
5 Pin Configuration and Functions	4	7.4 Device Functional Modes.....	18
Pin Functions.....	4	8 Application and Implementation	20
Pin Functions: TLV7032/42.....	5	8.1 Application Information.....	20
Pin Functions: TLV7034/44.....	6	8.2 Typical Applications.....	23
6 Specifications	7	9 Power Supply Recommendations	30
6.1 Absolute Maximum Ratings.....	7	10 Layout	31
6.2 ESD Ratings.....	7	10.1 Layout Guidelines.....	31
6.3 Recommended Operating Conditions.....	7	10.2 Layout Example.....	31
6.4 Thermal Information (Single).....	7	11 Device and Documentation Support	32
6.5 Thermal Information (Dual).....	8	11.1 Device Support.....	32
6.6 Thermal Information (Quad).....	8	11.2 Documentation Support.....	32
6.7 Electrical Characteristics (Single).....	9	11.3 Receiving Notification of Documentation Updates..	32
6.8 Switching Characteristics (Single).....	9	11.4 サポート・リソース.....	32
6.9 Electrical Characteristics (Dual).....	10	11.5 Trademarks.....	32
6.10 Switching Characteristics (Dual).....	10	11.6 Electrostatic Discharge Caution.....	32
6.11 Electrical Characteristics (Quad).....	11	11.7 Glossary.....	32
6.12 Switching Characteristics (Quad).....	11	12 Mechanical, Packaging, and Orderable Information	32
6.13 Timing Diagrams.....	12		
6.14 Typical Characteristics.....	13		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (Nov 2020) to Revision H (July 2021)	Page
• TSSOP パッケージ・オプションのリリース.....	1
Changes from Revision F (November 2019) to Revision G (December 2020)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• デュアル・チャンネル・オプションに SOT-23 (8) と WSON (8) を追加.....	1
Changes from Revision E (June 2019) to Revision F (November 2019)	Page
• クワッド・チャンネル・バージョンを追加.....	1
• デュアル・チャンネル・オプションに SOT-23 (8) と WSON (8) を追加.....	1
• クワッド・パッケージ・オプションを追加.....	1
• Added TSSOP and RTE pinout information to <i>Pin Configuration and Functions</i> section	5
Changes from Revision D (April 2019) to Revision E (June 2019)	Page
• Changed VOH min from 4.7V to 4.65V for all package options in EC Table (Single)	9
• Changed VOL max from 300mV to 350mV for all package options in EC Table (Single)	9
• Deleted separate rows for VOH & VOL for DBV package options only in EC Table (Single)	9
Changes from Revision C (March 2019) to Revision D (April 2019)	Page
• Added separate rows for VOH & VOL for DBV package options in EC Table (Single)	9
Changes from Revision B (May 2018) to Revision C (March 2019)	Page
• VSSOP パッケージにデュアル・チャンネル・バージョンを追加.....	1
• ドキュメント全体を通して TLV7031 を TLV703x に、TLV7041 を TLV704x に変更.....	1

• デュアル・チャンネル・バージョンを追加.....	1
• 製品情報に VSSOP パッケージのデュアル・チャンネル・バージョンを追加.....	1
• 「SOT-23 パッケージはプレビューのみです」を削除.....	1

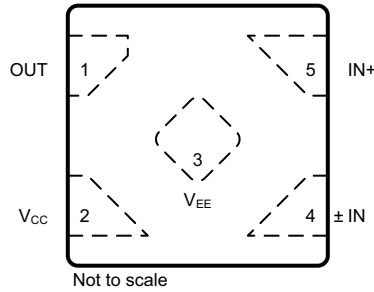
Changes from Revision A (January 2018) to Revision B (May 2018)	Page
--	-------------

• プレビューの SC70 パッケージを量産データに変更.....	1
-----------------------------------	---

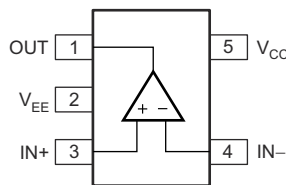
Changes from Revision * (September 2017) to Revision A (January 2018)	Page
--	-------------

• データシートのタイトルを「TLV7031/TLV7041 小型、nanoPower、低電圧コンパレータ」から「TLV7031 および TLV7041 小型、nanoPower、低電圧コンパレータ」に変更.....	1
• 「 <i>特長</i> 」に内部ヒステリシスの箇条書き項目を追加.....	1
• 「 <i>特長</i> 」に、プッシュプル出力およびオープン・ドレイン出力のオプションがどのデバイスに存在するかを記載.....	1
• 特性グラフが TLV7031 と TLV7041 の両方のデバイスを対象としているため、グラフのタイトルから (TLV7031) を削除.....	1
• Added X2SON tablenote to <i>Pin Functions</i> table	4
• Changed 図 6-2	12
• Added note to the <i>Timing Diagrams</i> section.....	12
• Smoothed Propagation Delay plots in 図 6-31 through	13
• Changed vertical labels on 図 6-20 , 図 6-21 , 図 6-17 , and 図 6-30	13
• Changed <i>Functional Block Diagram</i>	18
• Changed text 'the TLV7041 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 7 V' to 'the TLV7041 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V'.....	19
• Changed 図 8-3	23
• Added note to the <i>Layout Example</i> section.....	31
• Added <i>Documentation Support</i> section	32

5 Pin Configuration and Functions



**5-1. DPW Package
5-Pin X2SON
Top View**

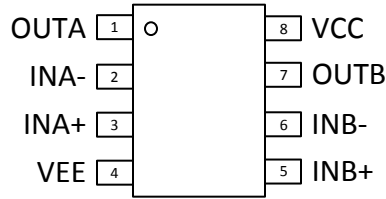


**5-2. DBV and DCK Package
5-Pin SOT-23 and SC70
Top View**

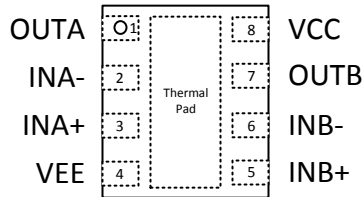
Pin Functions

PIN			I/O ⁽²⁾	DESCRIPTION
X2SON ⁽¹⁾	SOT-23, SC70	NAME		
1	1	OUT	O	Output
2	5	V _{CC}	P	Positive (highest) power supply
3	2	V _{EE}	P	Negative (lowest) power supply
4	4	IN ⁻	I	Inverting input
5	3	IN ⁺	I	Noninverting input

- (1) The application report [Designing and Manufacturing With TI's X2SON Packages](#) (SCEA055) provides more details on the optimal PCB designs.
- (2) I = Input, O = Output, P = Power



5-3. TLV7032/42 DGK, DDF Packages
8-Pin VSSOP, SOT-23
Top View

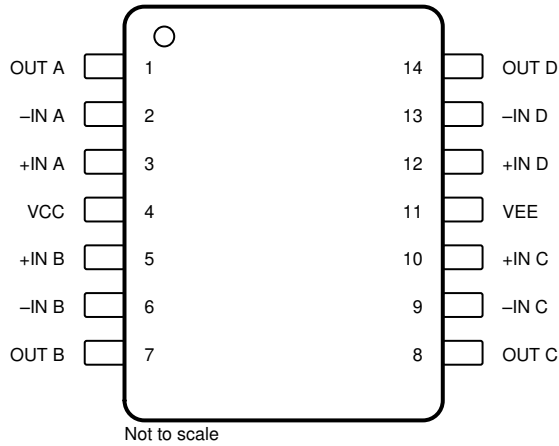


A. Connect thermal pad to V-.

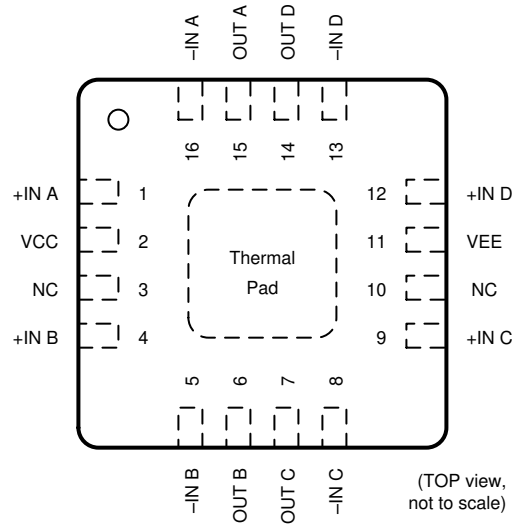
5-4. TLV7032/42 DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View

Pin Functions: TLV7032/42

PIN		I/O	DESCRIPTION
NAME	NO.		
INA-	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB-	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply



**5-5. TLV7034/44 PW Packages
14-Pin TSSOP
Top View**



A. Connect thermal pad to V-.

**5-6. TLV7034/44 RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View**

Pin Functions: TLV7034/44

NAME	PIN		I/O	DESCRIPTION
	TSSOP	WQFN		
-IN1 A	2	16	I	Inverting input, channel A
+IN A	3	1	I	Noninverting input, channel A
-IN B	6	5	I	Inverting input, channel B
+IN B	5	4	I	Noninverting input, channel B
-IN C	9	8	I	Inverting input, channel C
+IN C	10	9	I	Noninverting input, channel C
-IN D	13	13	I	Inverting input, channel D
+IN D	12	12	I	Noninverting input, channel D
NC	—	3, 10	—	No internal connection
OUT A	1	15	O	Output, channel A
OUT B	7	6	O	Output, channel B
OUT C	8	7	O	Output, channel C
OUT D	14	14	O	Output, channel D
VEE	11	11	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	4	2	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	-0.3	7	V
Input pins (IN+, IN-) ⁽²⁾	$V_{EE} - 0.3$	7	V
Current into Input pins (IN+, IN-)		±10	mA
Output (OUT) (TLV703x) ⁽³⁾	$V_{EE} - 0.3$	$V_{CC} + 0.3$	V
Output (OUT) (TLV704x)	$V_{EE} - 0.3$	7	V
Output short-circuit duration ⁽⁴⁾		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to V_{EE} . Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less
- (3) Output maximum is ($V_{CC} + 0.3$ V) or 7 V, whichever is less.
- (4) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	1.6	6.5	V
Input voltage range	$V_{EE} - 0.1$	$V_{CC} + 0.1$	V
Ambient temperature, T_A	-40	125	°C

6.4 Thermal Information (Single)

THERMAL METRIC ⁽¹⁾		TLV7031/TLV7041			UNIT
		DPW (X2SON)	DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	533.2	297.2	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	302.7	224.7	186.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	408.3	200.1	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.5	141.2	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	405.9	198.9	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	188.3	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information (Dual)

THERMAL METRIC ⁽¹⁾		TLV7032/TLV7042			UNIT
		DGK (VSSOP)	DDF (SOT-23)	DSG (WSON)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	211.7	212.5	106.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	96.1	127.3	127.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	133.5	129.2	72.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	28.3	25.8	16.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	131.7	129.0	72.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	47.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information (Quad)

THERMAL METRIC ⁽¹⁾		TLV7034/44		UNIT
		RTE (QFN)	PW (TSSOP)	
		16 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	65.4	131.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	70.2	60.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	40.5	74.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	5.6	12.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	40.5	73.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	24.1	n/a	°C/W

6.7 Electrical Characteristics (Single)

$V_S = 1.8\text{ V to }5\text{ V}$, $V_{CM} = V_S / 2$; minimum and maximum values are at $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	$V_S = 1.8\text{ V and }5\text{ V}$, $V_{CM} = V_S / 2$		± 0.1	± 8	mV
V_{HYS}	Hysteresis	$V_S = 1.8\text{ V and }5\text{ V}$, $V_{CM} = V_S / 2$, $T_A = 25^\circ\text{C}$	2	7	17	mV
V_{CM}	Common-mode voltage range		V_{EE}		$V_{CC} + 0.1$	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7031 only)	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$	4.65	4.8		V
V_{OL}	Output voltage low	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7041 only)	$V_S = 5\text{ V}$, $V_{ID} = +0.1\text{ V}$ (output high), $V_{PULLUP} = V_{CC}$		100		pA
CMRR	Common-mode rejection ratio	$V_{EE} < V_{CM} < V_{CC}$, $V_S = 5\text{ V}$		73		dB
PSRR	Power supply rejection ratio	$V_S = 1.8\text{ V to }5\text{ V}$, $V_{CM} = V_S / 2$		77		dB
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$, sourcing		29		mA
		$V_S = 5\text{ V}$, sinking		33		
I_{CC}	Supply current	$V_S = 1.8\text{ V}$, no load, $V_{ID} = -0.1\text{ V}$ (Output Low)		335	900	nA

6.8 Switching Characteristics (Single)

Typical values are at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = V_S / 2$; $CL = 15\text{ pF}$, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 2.5 k Ω TLV7041 only)	Midpoint of input to midpoint of output, $V_{OD} = 100\text{ mV}$		3		μs
t_{PLH}	Propagation delay time, low-to high (RP = 2.5 k Ω TLV7041 only)	Midpoint of input to midpoint of output, $V_{OD} = 100\text{ mV}$		3		μs
t_R	Rise time (TLV7031 only)	Measured from 10% to 90%		4.5		ns
t_F	Fall time	Measured from 10% to 90%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 μs before the output will reflect the input.		200		μs

6.9 Electrical Characteristics (Dual)

$V_S = 1.8\text{ V to }5\text{ V}$, $V_{CM} = V_S / 2$; minimum and maximum values are at $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	$V_S = 1.8\text{ V and }5\text{ V}$, $V_{CM} = V_S / 2$		± 0.1	± 8	mV
V_{HYS}	Hysteresis	$V_S = 1.8\text{ V and }5\text{ V}$, $V_{CM} = V_S / 2$	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		$V_{CC} + 0.1$	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7032 only)	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$	4.65	4.8		V
V_{OL}	Output voltage low	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7042 only)	$V_S = 5\text{ V}$, $V_{ID} = +0.1\text{ V}$ (output high), $V_{PULLUP} = V_{CC}$		100		pA
CMRR	Common-mode rejection ratio	$V_{EE} < V_{CM} < V_{CC}$, $V_S = 5\text{ V}$		73		dB
PSRR	Power supply rejection ratio	$V_S = 1.8\text{ V to }5\text{ V}$, $V_{CM} = V_S / 2$		77		dB
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$, sourcing (for TLV7032 only)		29		mA
		$V_S = 5\text{ V}$, sinking		33		
I_{CC}	Supply current / Channel	$V_S = 1.8\text{ V}$, no load, $V_{ID} = -0.1\text{ V}$ (Output Low)		315	750	nA

6.10 Switching Characteristics (Dual)

Typical values are at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = V_S / 2$; $CL = 15\text{ pF}$, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 k Ω TLV7042 only) (1)	Midpoint of input to midpoint of output, $V_{OD} = 100\text{ mV}$		3		μs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 k Ω TLV7042 only) (1)	Midpoint of input to midpoint of output, $V_{OD} = 100\text{ mV}$		3		μs
t_R	Rise time (TLV7032 only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for t_{ON} before the output will reflect the input.		200		μs

(1) The lower limit for RP is 650 Ω

6.11 Electrical Characteristics (Quad)

$V_S = 1.8\text{ V to }5\text{ V}$, $V_{CM} = V_S / 2$; minimum and maximum values are at $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	$V_S = 1.8\text{ V and }5\text{ V}$, $V_{CM} = V_S / 2$		± 0.1	± 8	mV
V_{HYS}	Hysteresis	$V_S = 1.8\text{ V and }5\text{ V}$, $V_{CM} = V_S / 2$	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		$V_{CC} + 0.1$	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7034 only)	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$	4.65	4.8		V
V_{OL}	Output voltage low	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $I_O = 3\text{ mA}$		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7044 only)	$V_S = 5\text{ V}$, $V_{ID} = +0.1\text{ V}$ (output high), $V_{PULLUP} = V_{CC}$		100		pA
CMRR	Common-mode rejection ratio	$V_{EE} < V_{CM} < V_{CC}$, $V_S = 5\text{ V}$		73		dB
PSRR	Power supply rejection ratio	$V_S = 1.8\text{ V to }5\text{ V}$, $V_{CM} = V_S / 2$		77		dB
I_{SC}	Short-circuit current	$V_S = 5\text{ V}$, sourcing (for TLV7034 only)		29		mA
		$V_S = 5\text{ V}$, sinking		33		
I_{CC}	Supply current / Channel	$V_S = 1.8\text{ V}$, no load, $V_{ID} = -0.1\text{ V}$ (Output Low)		315	750	nA

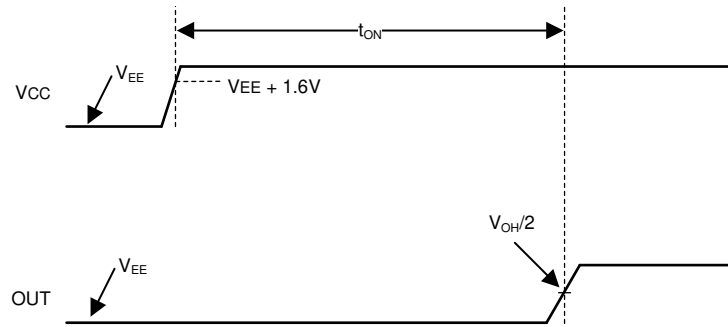
6.12 Switching Characteristics (Quad)

Typical values are at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{CM} = V_S / 2$; $CL = 15\text{ pF}$, input overdrive = 100 mV (unless otherwise noted).

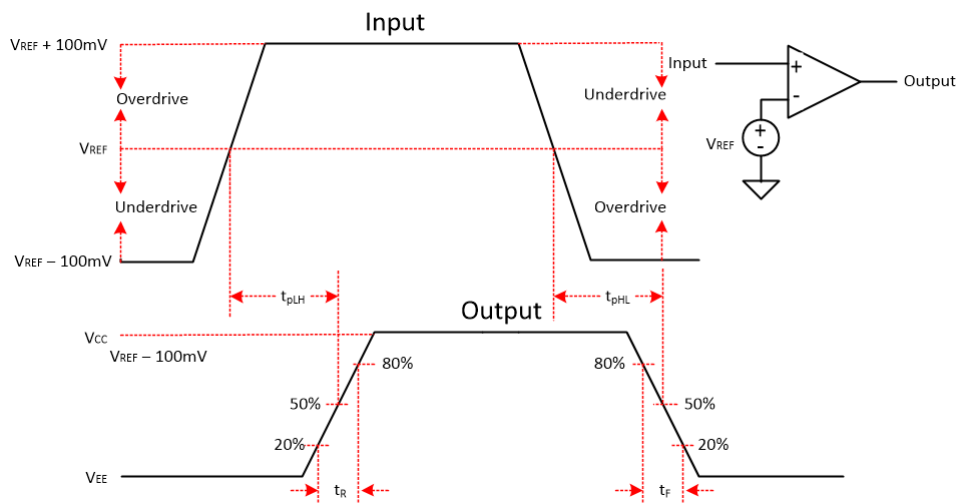
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 k Ω TLV7044 only) (1)	Midpoint of input to midpoint of output, $V_{OD} = 100\text{ mV}$		3		μs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 k Ω TLV7044 only) (1)	Midpoint of input to midpoint of output, $V_{OD} = 100\text{ mV}$		3		μs
t_R	Rise time (TLV7034 only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for t_{ON} before the output will reflect the input..		400		μs

(1) The lower limit for RP is 650 Ω

6.13 Timing Diagrams



6-1. Start-Up Time Timing Diagram ($IN+ > IN-$)



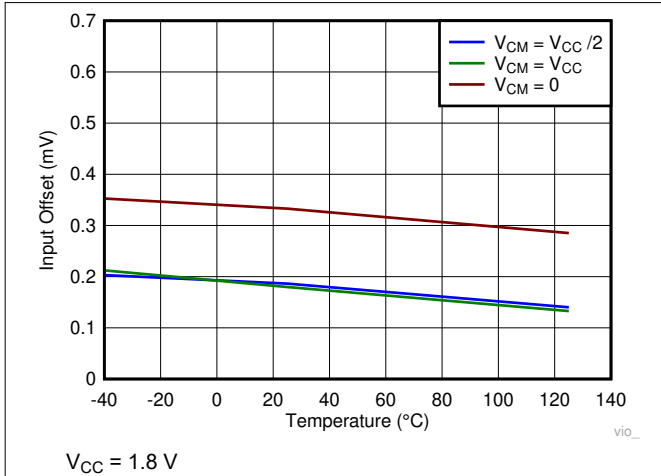
6-2. Propagation Delay Timing Diagram

Note

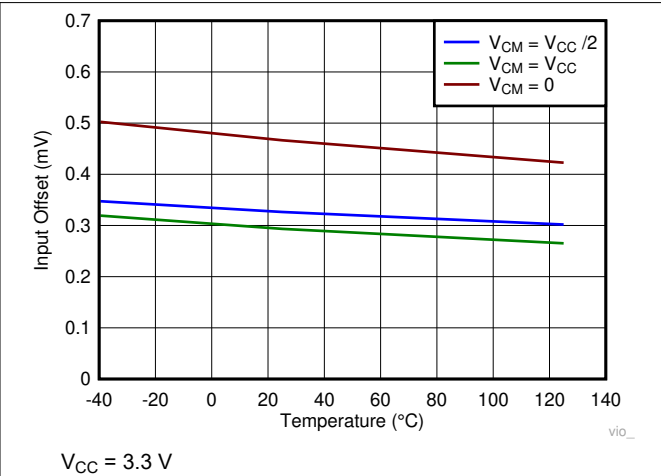
The propagation delays t_{pLH} and t_{pHL} include the contribution of input offset and hysteresis.

6.14 Typical Characteristics

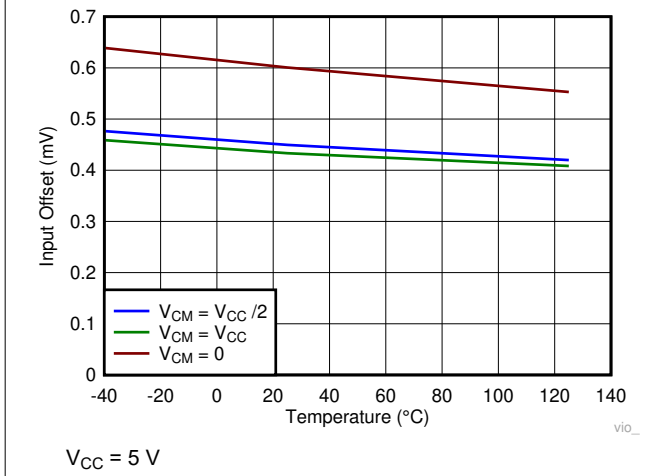
$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



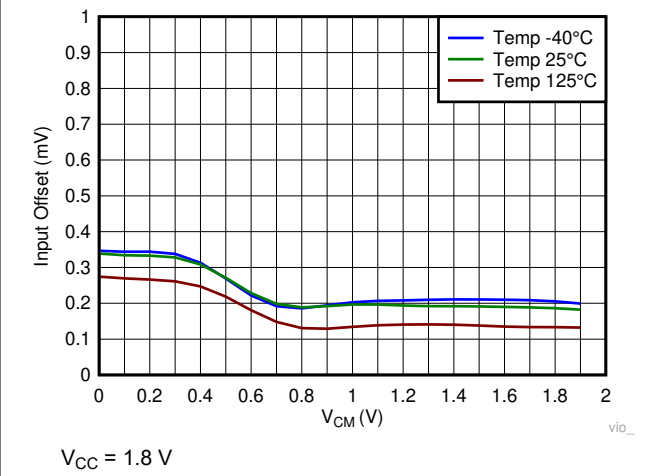
6-3. Input Offset vs Temperature



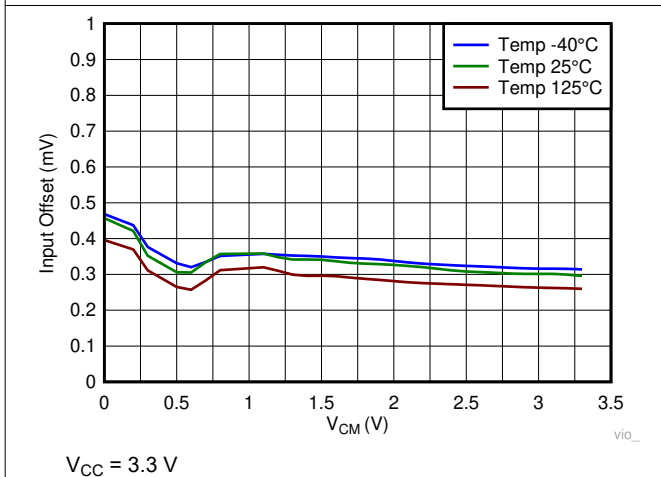
6-4. Input Offset vs Temperature



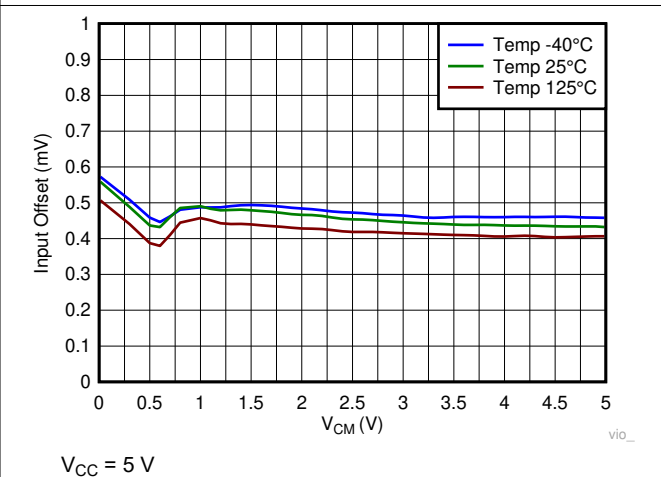
6-5. Input Offset vs Temperature



6-6. Input Offset Voltage vs V_{CM}



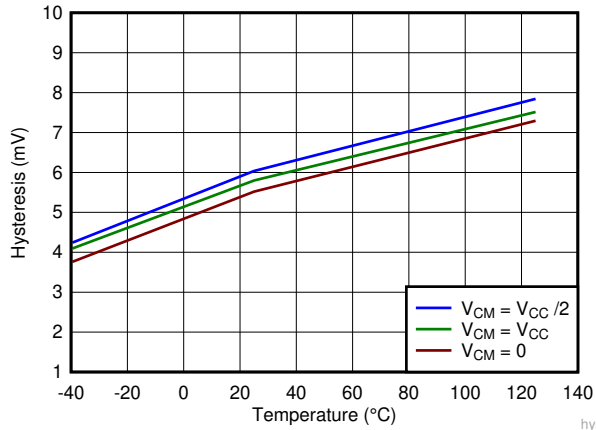
6-7. Input Offset Voltage vs V_{CM}



6-8. Input Offset Voltage vs V_{CM}

6.14 Typical Characteristics (continued)

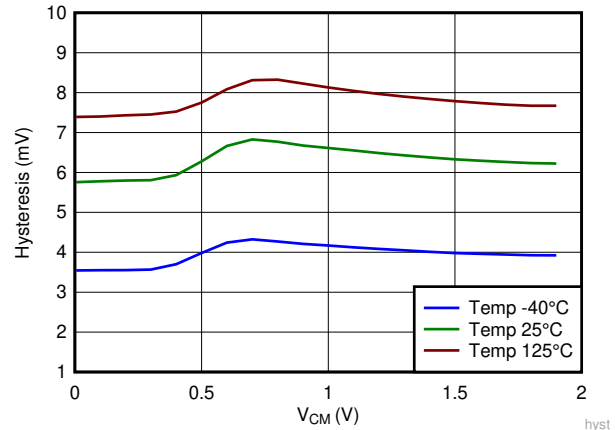
$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



$V_{CC} = 1.8\text{ V to } 5\text{ V}$

TLV70x1

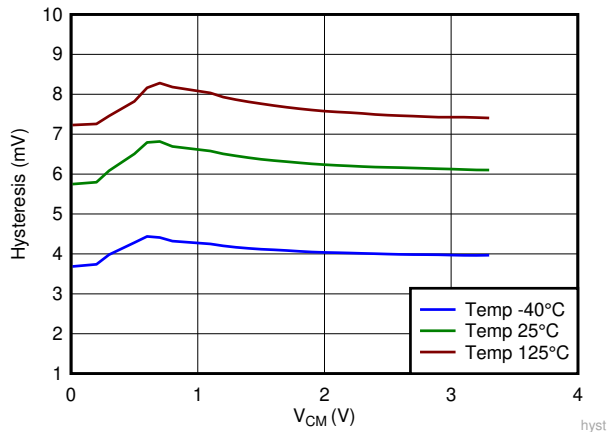
6-9. Hysteresis vs Temperature



$V_{CC} = 1.8\text{ V}$

TLV70x1

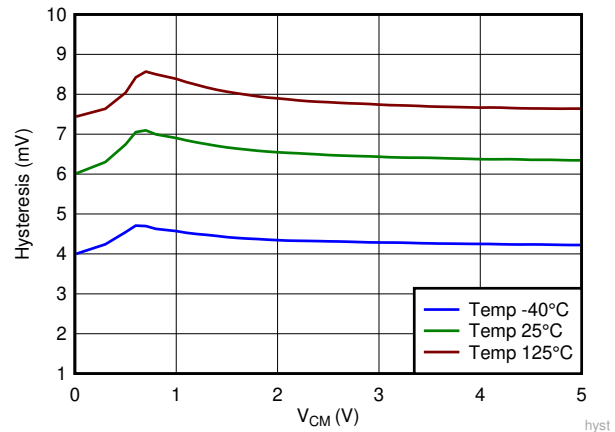
6-10. Hysteresis vs V_{CM}



$V_{CC} = 3.3\text{ V}$

TLV70x1

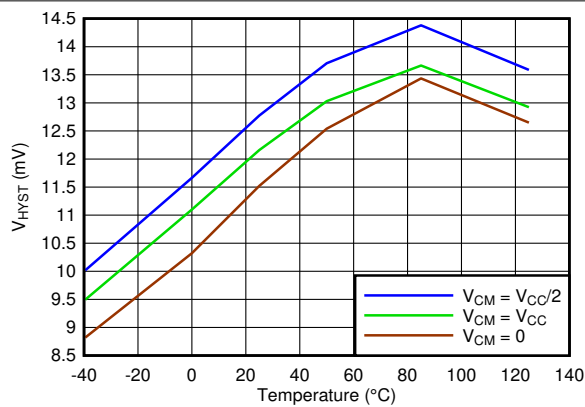
6-11. Hysteresis vs V_{CM}



$V_{CC} = 5\text{ V}$

TLV70x1

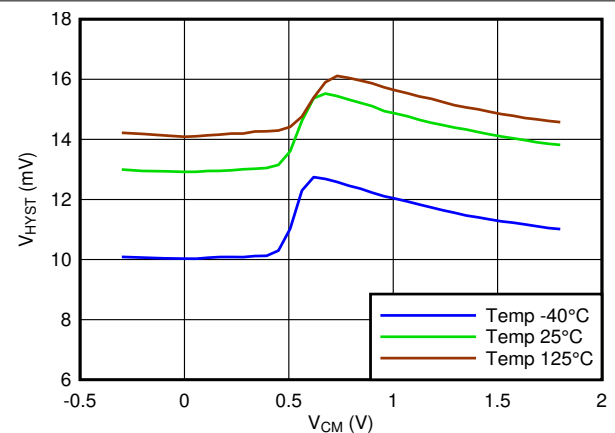
6-12. Hysteresis vs V_{CM}



$V_{CC} = 1.8\text{ V to } 5\text{ V}$

TLV70x2

6-13. Hysteresis vs Temperature



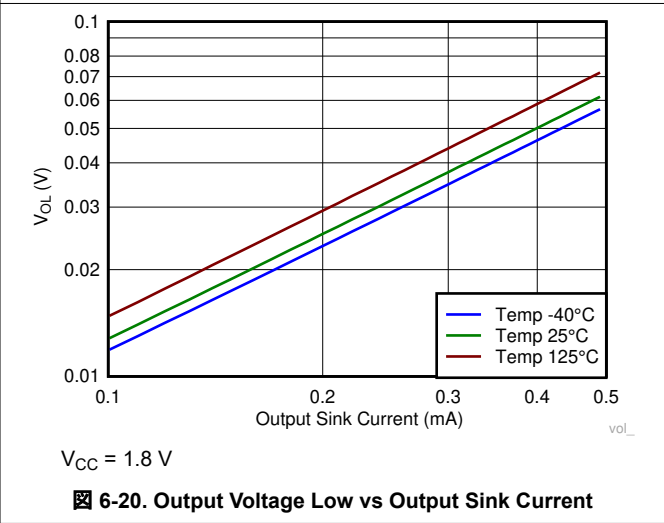
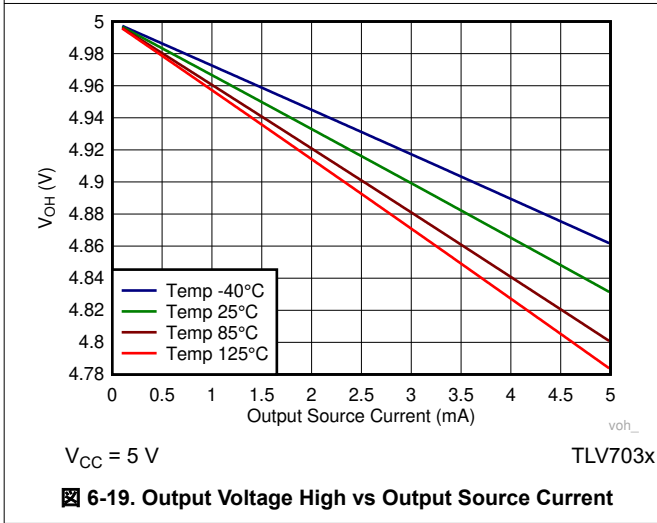
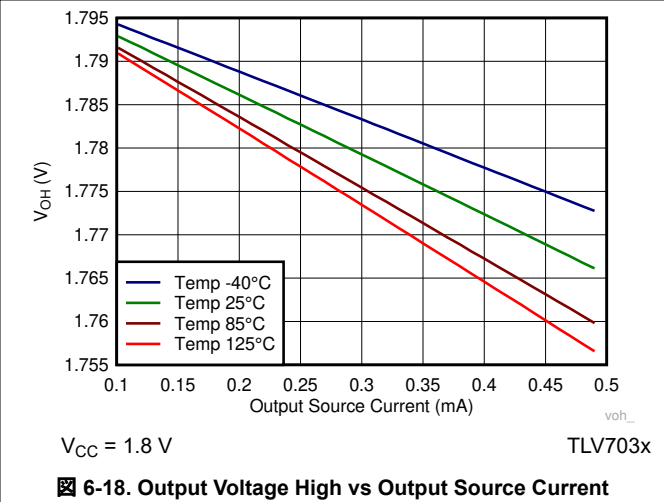
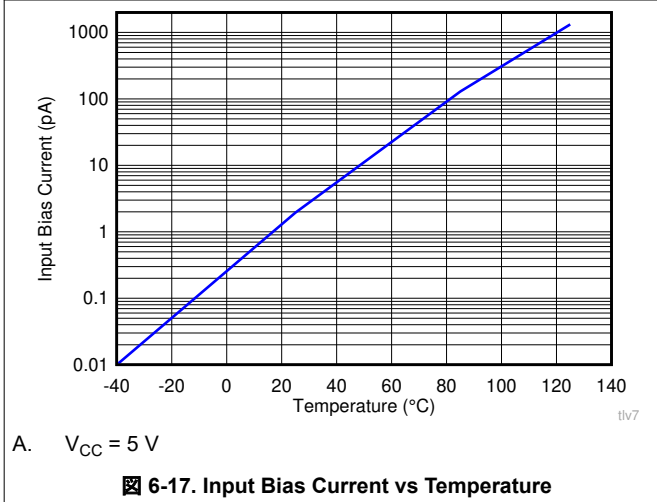
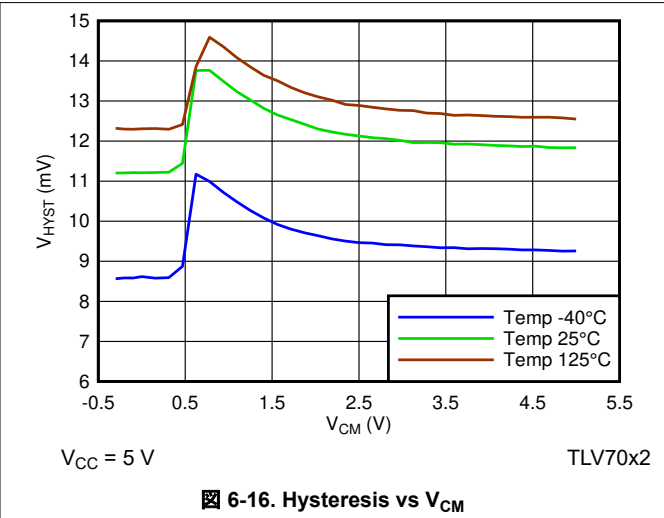
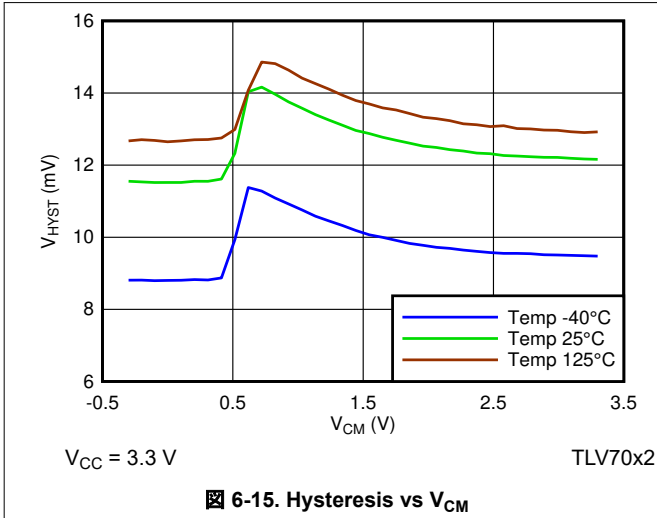
$V_{CC} = 1.8\text{ V}$

TLV70x2

6-14. Hysteresis vs V_{CM}

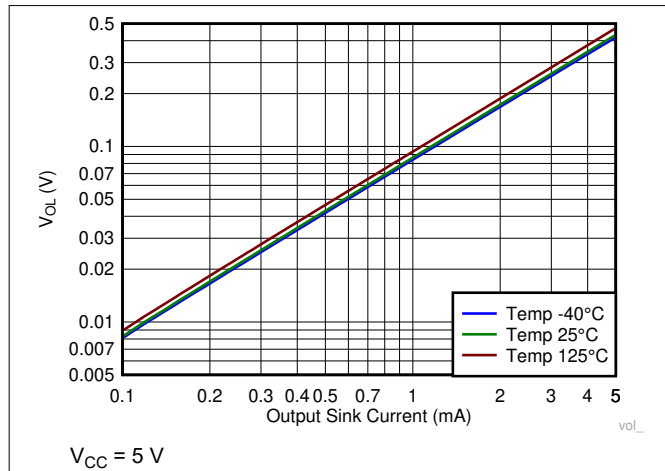
6.14 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$

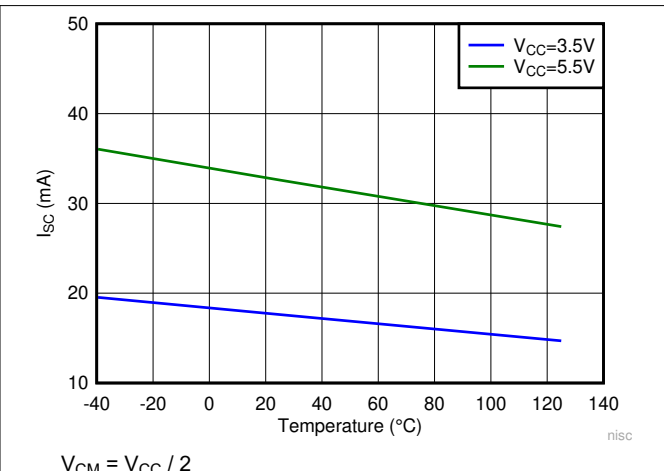


6.14 Typical Characteristics (continued)

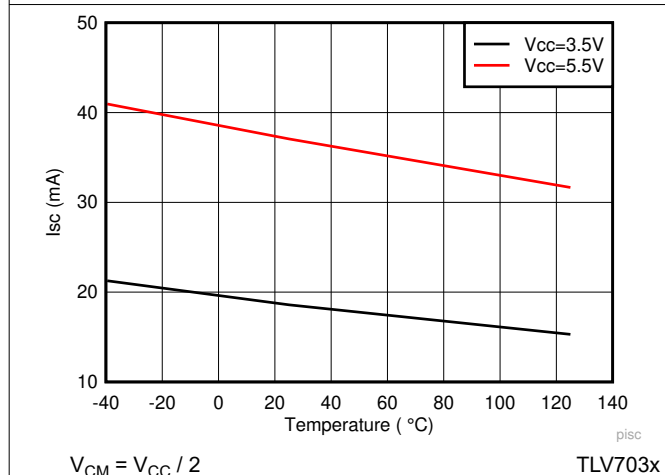
$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$



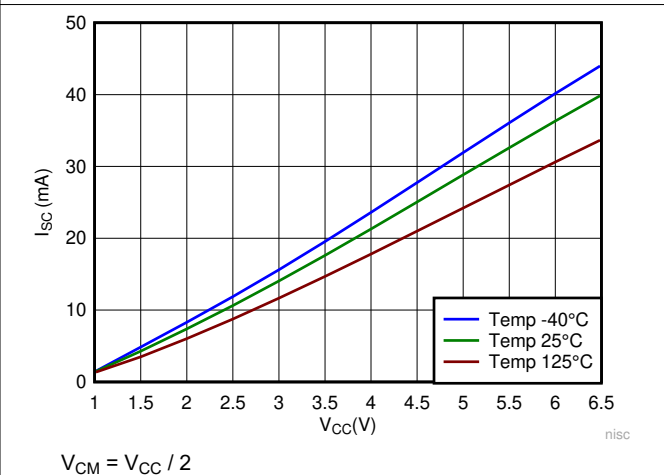
6-21. Output Voltage Low vs Output Sink Current



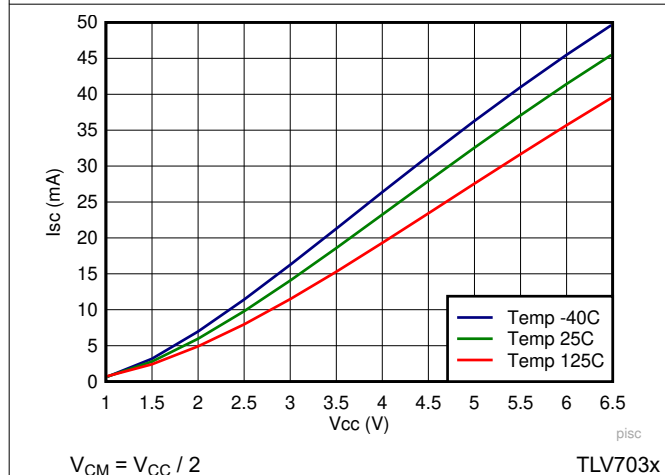
6-22. Output Short-Circuit (Sink) Current vs Temperature



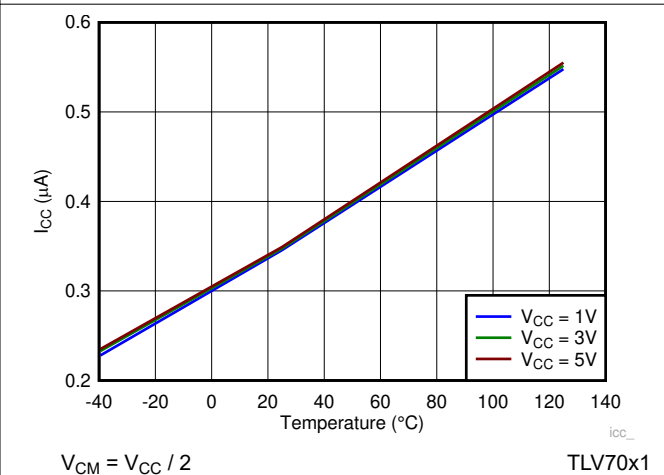
6-23. Output Short-Circuit (Source) Current vs Temperature



6-24. Output Short Circuit (Sink) vs V_{CC}



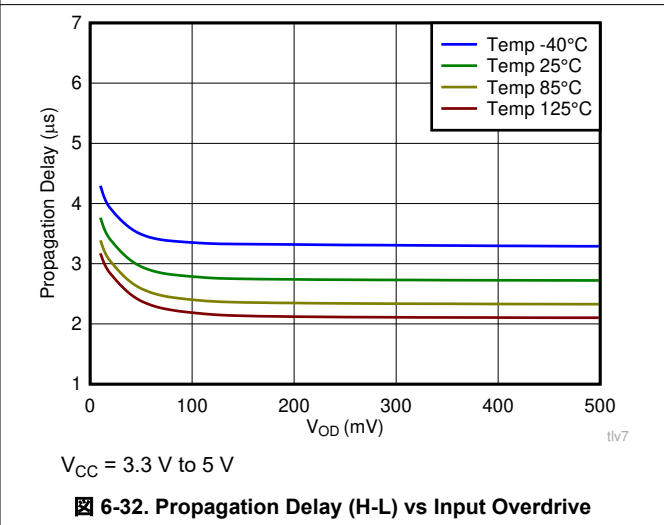
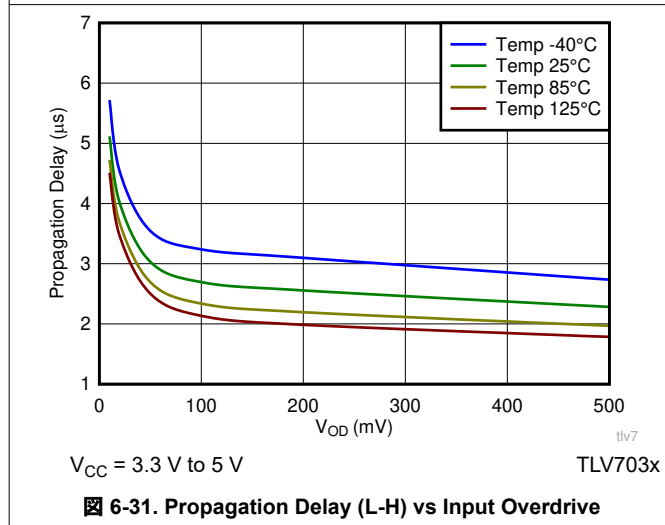
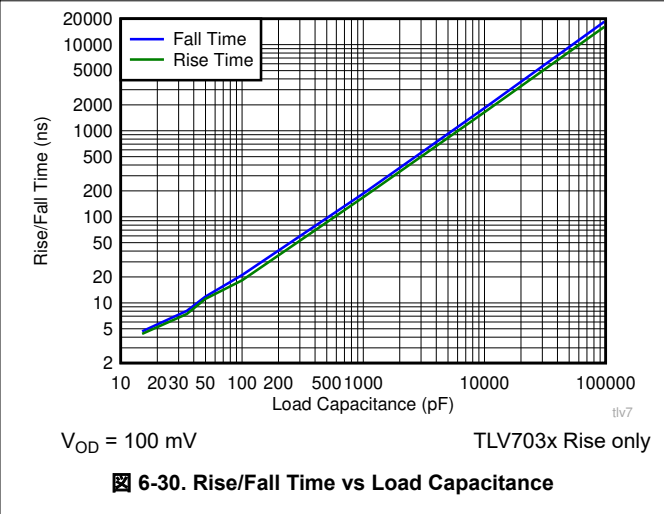
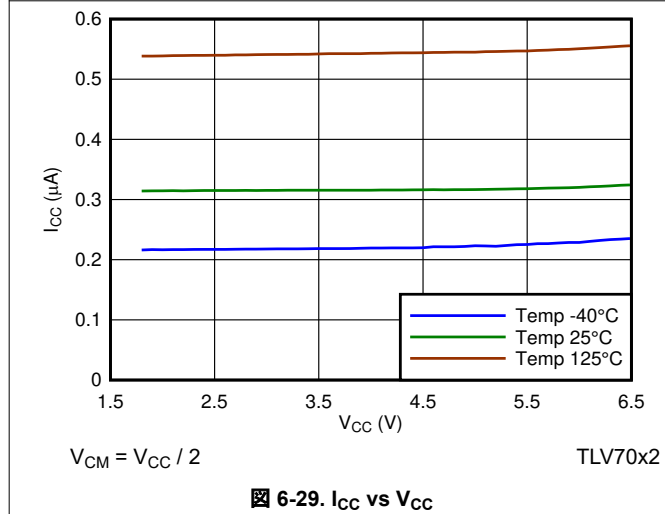
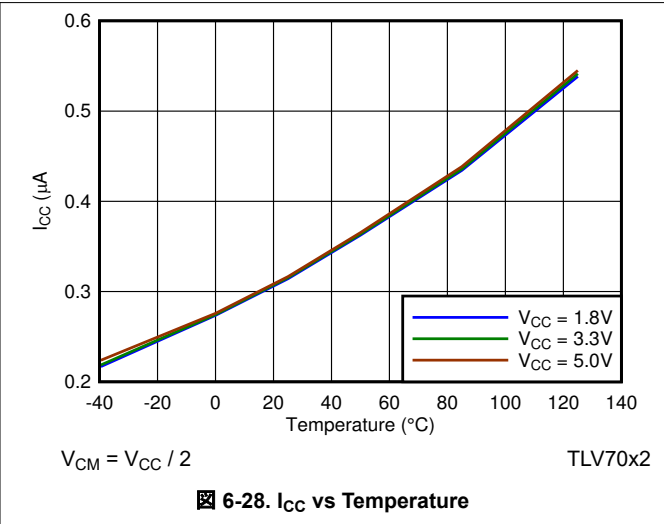
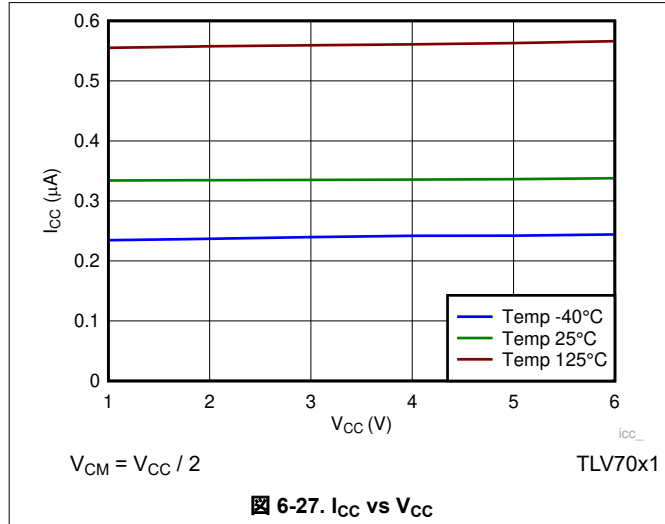
6-25. Output Short Circuit (Source) vs V_{CC}



6-26. I_{CC} vs Temperature

6.14 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{CM} = V_{CC}/2$, $C_L = 15\text{ pF}$

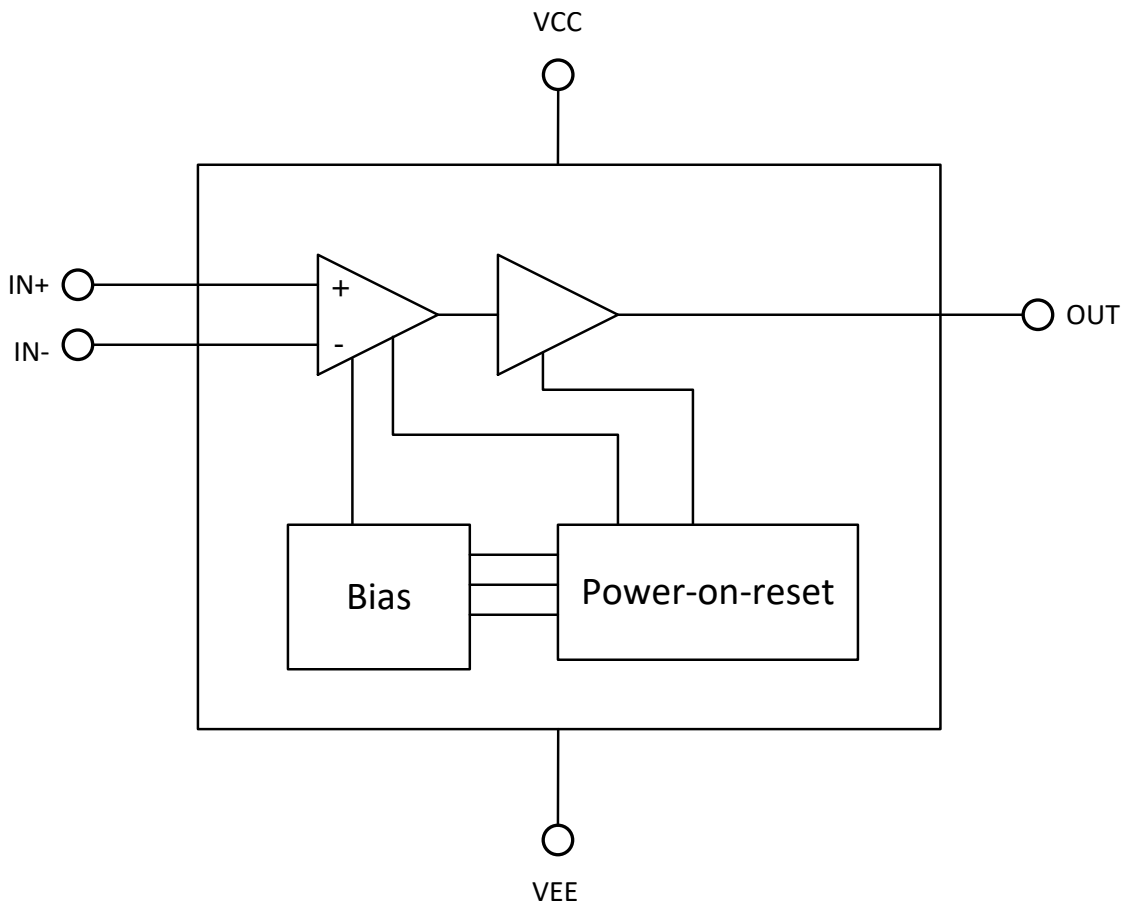


7 Detailed Description

7.1 Overview

The TLV703x and TLV704x are nano-power comparators with push-pull and open-drain outputs. Operating from 1.6 V to 6.5 V and consuming only 315 nA, the TLV703x and TLV704x are designed for portable and industrial applications. The TLV703x and TLV704x are available in a variety of leadless and leaded packages to offer significant board space saving in space-challenged designs.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV703x and TLV704x devices are nanoPower comparators that are capable of operating at low voltages. The TLV703x and TLV704x feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The TLV703x (push-pull) and TLV704x (open-drain) also feature internal hysteresis.

7.4 Device Functional Modes

The TLV703x and TLV704x have a power-on-reset (POR) circuit. While the power supply (V_S) is less than the minimum supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

For the TLV703x, the POR circuit holds the output low (at V_{EE}) while activated.

For the TLV704x, the POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

7.4.1 Inputs

The TLV703x and TLV704x input common-mode extends from V_{EE} to 100 mV above V_{CC} . The differential input voltage (V_{ID}) can be any voltage within these limits. No phase inversion of the comparator output occurs when the input pins exceed V_{CC} and V_{EE} .

The input of TLV703x and TLV704x is fault tolerant. It maintains the same high input impedance when V_{CC} is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (7 V) with $V_{CC} = 0$ V or any value up to the maximum specified. The V_{CC} is isolated from the input such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE} . The comparator inputs are protected from voltages below V_{EE} by internal diodes connected to V_{EE} . As the input voltage goes under V_{EE} , the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in [Figure 7-1](#). This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-} . This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (7 mV for both TLV703x and TLV704x).

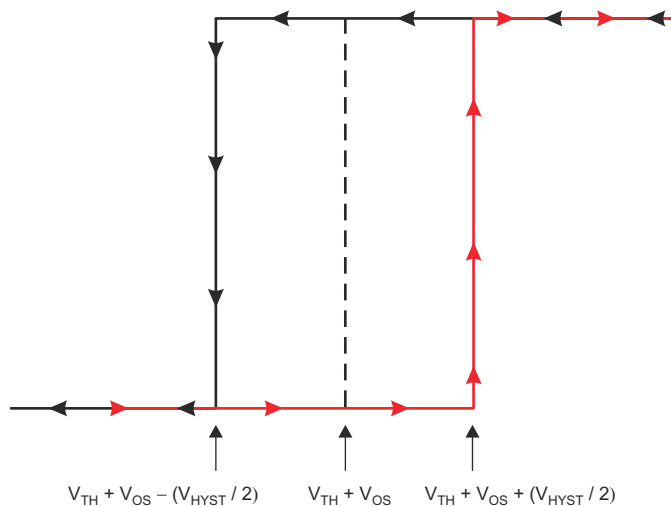


Figure 7-1. Hysteresis Transfer Curve

7.4.3 Output

The TLV703x features a push-pull output stage eliminating the need for an external pullup resistor. On the other hand, the TLV704x features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V independent of the supply voltage.

8 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV703x and TLV704x are nano-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV703x is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV704x with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and small size of the TLV703x and TLV704x make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV703x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in [Figure 8-1](#). When V_{IN} at the inverting input is less than V_A , the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R1 \parallel R3$ in series with $R2$. [Equation 1](#) defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When V_{IN} is greater than V_A , the output voltage is low, very close to ground. In this case, the three network resistors can be presented as $R2 \parallel R3$ in series with $R1$. Use [Equation 2](#) to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

[Equation 3](#) defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

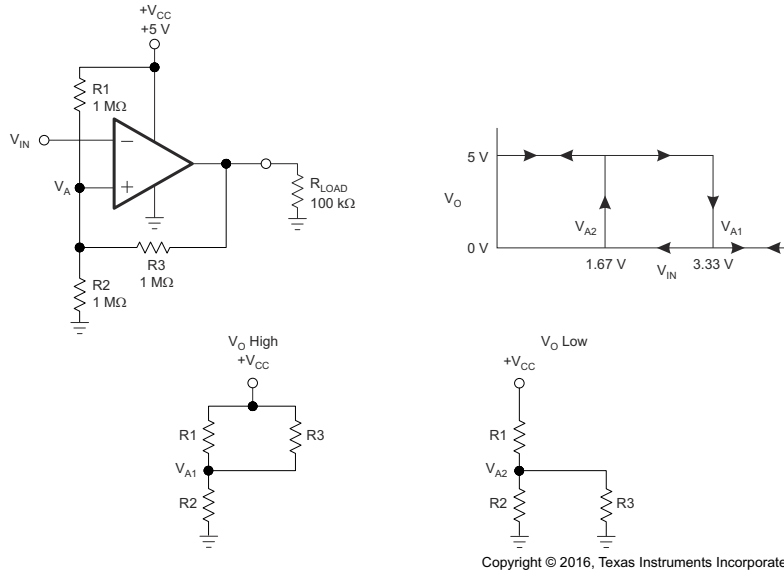


FIG 8-1. TLV703x in an Inverting Configuration With Hysteresis

8.1.2 Noninverting Comparator With Hysteresis for TLV703x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in [FIG 8-2](#), and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1} . Use [Equation 4](#) to calculate V_{IN1} .

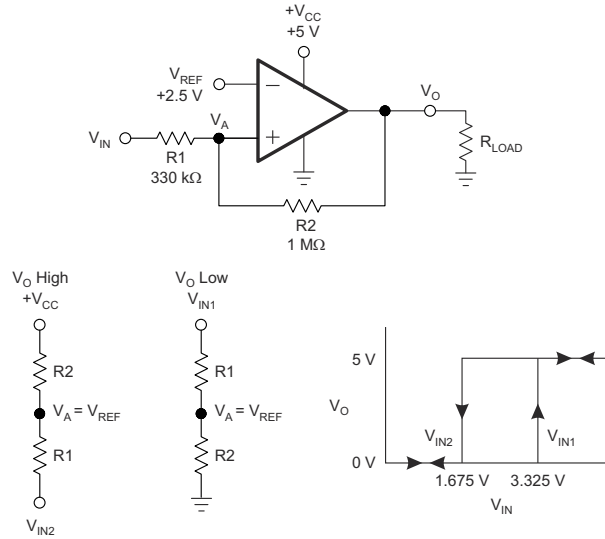
$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF} . Use [Equation 5](#) to calculate V_{IN2} .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2} , as shown in [Equation 6](#).

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$



Copyright © 2016, Texas Instruments Incorporated

8-2. TLV703x in a Noninverting Configuration With Hysteresis

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. [Figure 8-3](#) shows a simple window comparator circuit.

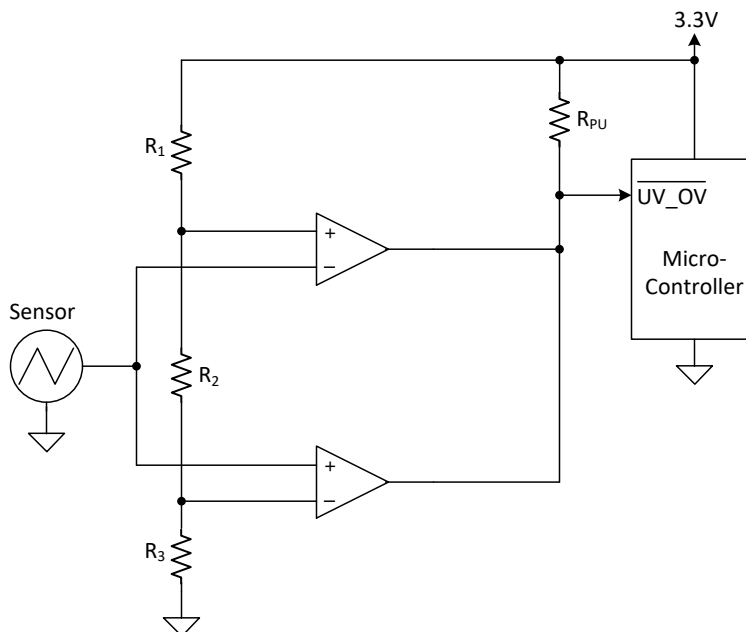


Figure 8-3. TLV704x-Based Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in [Figure 8-3](#). Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R_1 , R_2 , and R_3 each 10-M Ω resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10 M Ω are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV704x devices. The TLV704x is used for its open-drain output configuration. Using the TLV704x allows the two comparator outputs to be wire-ored together. The respective comparator outputs are low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} is high when the sensor is in the range of 1.1 V to 2.2 V.

8.2.1.3 Application Curve

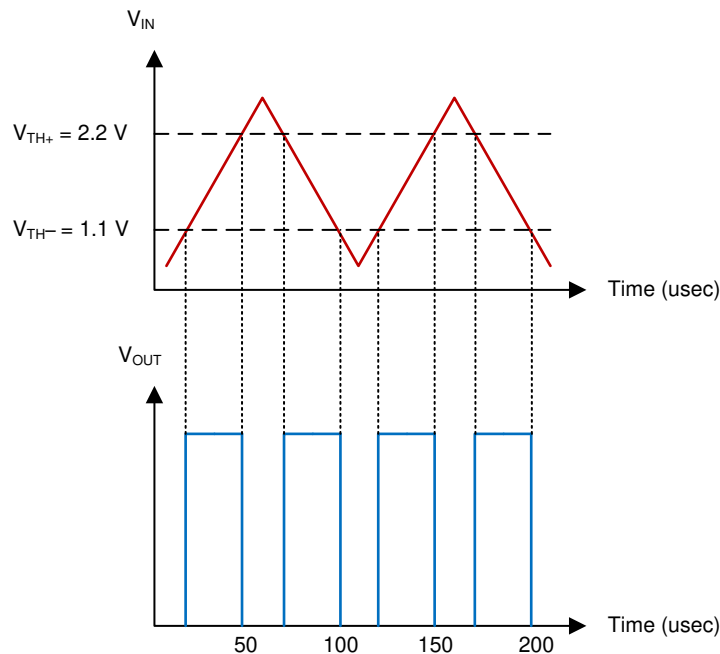
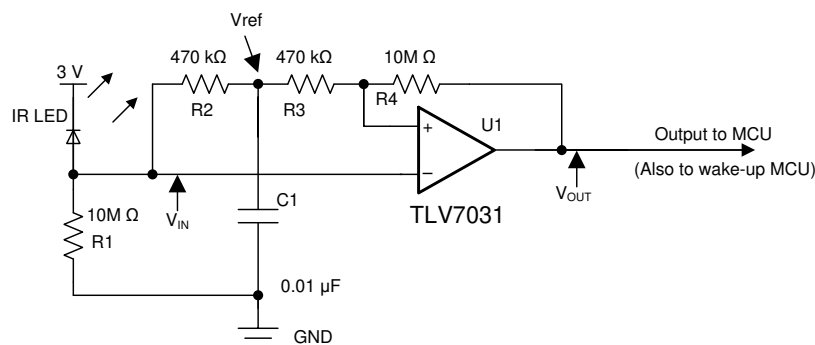


Figure 8-4. Window Comparator Results

8.2.2 IR Receiver Analog Front End

A single TLV703x device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.



Copyright © 2017, Texas Instruments Incorporated

Figure 8-5. IR Receiver Analog Front End Using TLV703x

8.2.2.1 Design Requirements

For this design, follow these design requirements:

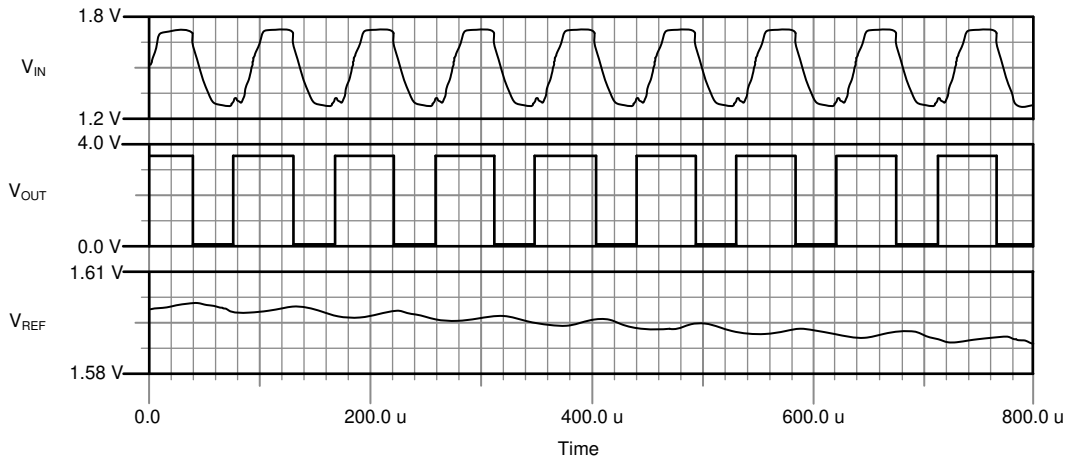
- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R_1 to be used.
- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R_2 and C_1 establishes a reference voltage V_{ref} , which tracks the mean amplitude of the IR signal. The noninverting input is directly connected to V_{ref} through R_3 . R_3 and R_4 are used to produce a hysteresis to keep transitions free of spurious toggles. To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

More technical details are provided in the TI TechNote [Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters](#) (SNVA808).

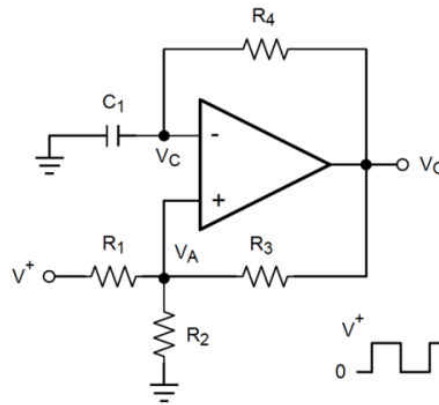
8.2.2.3 Application Curve



8-6. IR Receiver AFE Waveforms

8.2.3 Square-Wave Oscillator

A square-wave oscillator can be used as low-cost timing reference or system supervisory clock source.



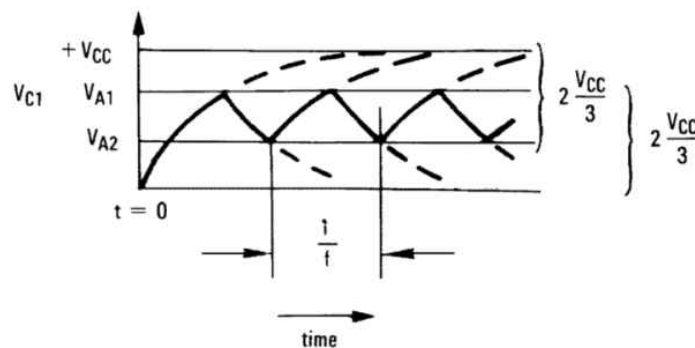
8-7. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by the propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following section provides details to calculate these component values.



8-8. Square-Wave Oscillator Timing Thresholds

First consider the output of figure 8-7 is high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4 , and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by 式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \parallel R_3} \tag{7}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2 V_{CC} / 3$

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by 式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \parallel R_3)}{R_1 + R_2 \parallel R_3} \quad (8)$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges through the R_4 , and the voltage V_{CC} decreases until it reaches V_{A2} . At this point, the output switches back to the starting state. The oscillation period equals the time duration from $2 V_{CC} / 3$ to $V_{CC} / 3$ then back to $2 V_{CC} / 3$, which is given by $R_4 C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2 R_4 C_1 \times \ln 2$. The oscillation frequency can be obtained by 式 9:

$$f = 1 / (2 R_4 \times C_1 \times \ln 2) \quad (9)$$

8.2.3.3 Application Curve

Figure 8-9 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100 \text{ k}\Omega$
- $C_1 = 100 \text{ pF}$, $C_L = 20 \text{ pF}$
- $V_+ = 5 \text{ V}$, $V_- = \text{GND}$
- C_{stray} (not shown) from V_A to GND = 10 pF

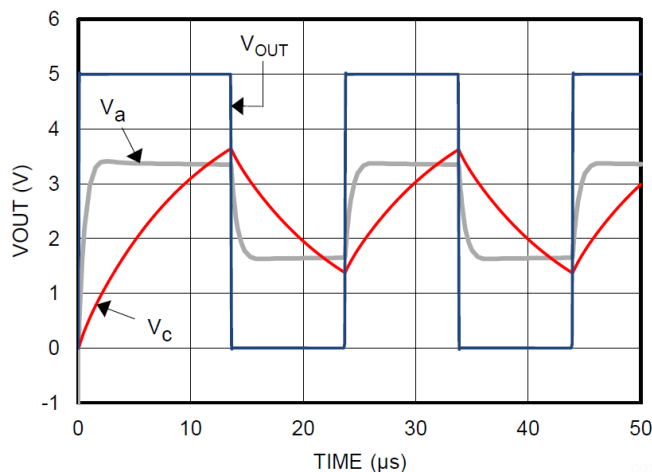
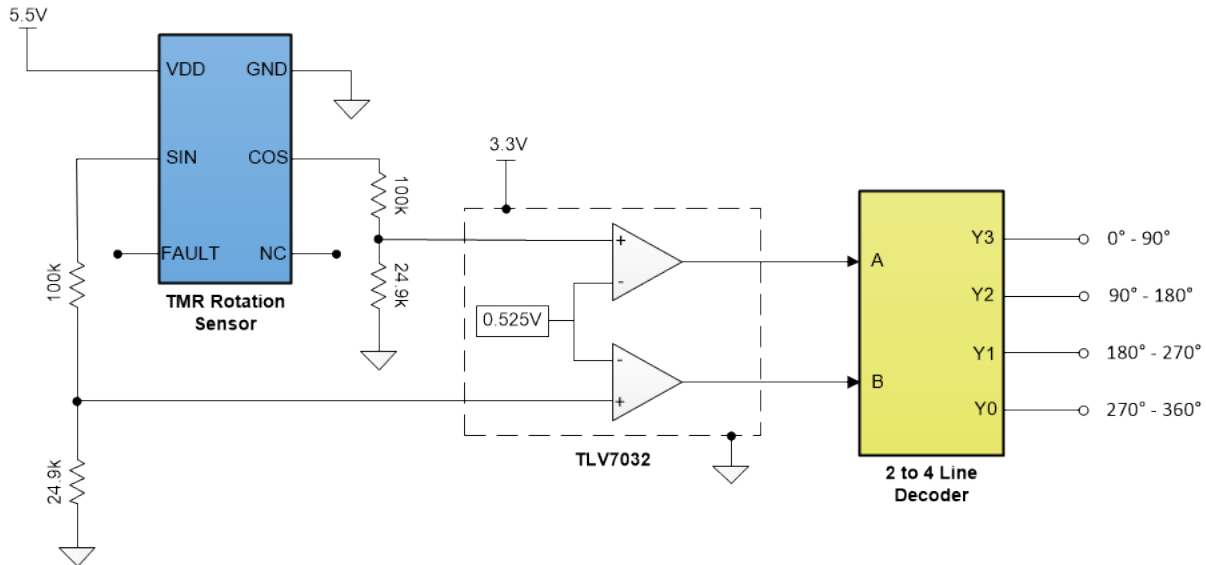


Figure 8-9. Square-Wave Oscillator Output Waveform

8.2.4 Quadrature Rotary Encoder

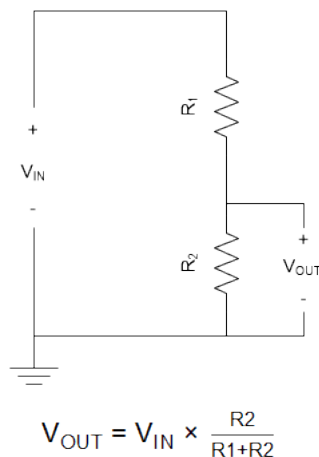
A quadrature encoder for rotary motors/shafts utilizing a Tunneling Magnetoresistance (TMR) Rotation Sensor can track the position of the motor shaft even when power is turned off, while the TLV7032 provides additional hysteresis to prevent unwanted output toggling between quadrants. The TLV7032 can be used with other sensing techniques as well, such as optical, capacitive, or inductive.



8-10. Quadrant Encoder Detector

8.2.4.1 Design Requirements

TMR Rotation Sensors general have two digital, binary outputs that are 90 degrees out of phase. The TLV7032 can be used to provide additional hysteresis to ensure there isn't any unwanted toggling of the output when the sensors are between the transition points of two quadrants. The TLV7032 already provides 10mV of typical internal hysteresis. By dividing down the output voltage from the rotation sensor using a voltage divider, the internal hysteresis will be scaled up by the same voltage divider ratio.



8-11. Voltage Divider Equation

8.2.4.2 Detailed Design Procedure

First, choose a target range of hysteresis to achieve. For this design example, 50mV of hysteresis will be the target. Since the TLV7032 already has 10mV (typ) of internal hysteresis, the voltage output from the TMR Rotation Sensor should be scaled down by a factor of 5. This way, the 10mV of internal hysteresis gets scaled up by a factor of 5, resulting in 50mV of hysteresis. The minimum output HIGH level for the TMR Rotation Sensor used in Figure 47 is 5.25 V. Since 5.25V will be the minimum output high value, it can be used to substitute V_{IN} from the Voltage Divider Equation in Figure 48. Since the voltage from the TMR rotation sensor needs to be scaled down by a factor of 5, the equation in Figure 48 can be rewritten as:

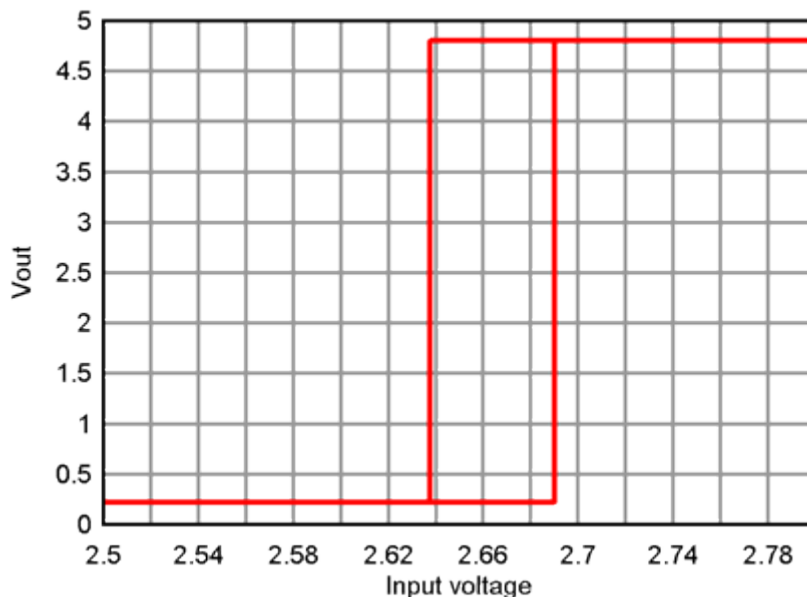
$$\frac{1}{5} = \frac{R_2}{R_1 + R_2}$$

The above equation can be solved for using standard resistor values, where $R_1 = 100k\Omega$, and $R_2 = 24.9k\Omega$. The minimum voltage seen at the noninverting pins of the comparator when the output is HIGH will be 1.05V. To make the device transition at 50% output high level, the inverting pins of the TLV7032 should be tied to a 0.525V reference.

8.2.4.3 Application Curve

Figure 49 shows the TLV7032 achieving approximately 50mV of hysteresis using the following component values:

- $R_1 = 100k\Omega$
- $R_2 = 24.9k\Omega$
- $V_{REF} (IN-) = 0.525V$



8-12. DC Input Voltage Sweep

9 Power Supply Recommendations

The TLV703x and TLV704x have a recommended operating voltage range (V_S) of 1.6 V to 6.5 V. V_S is defined as $V_{CC} - V_{EE}$. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and -2.5 V create comparable operating voltages for V_S . However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE} .

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

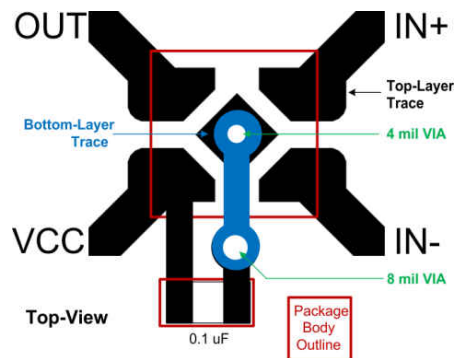
10 Layout

10.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

TI recommends a power-supply bypass capacitor of 100 nF when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV703x and TLV704x output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example



10-1. Layout Example

The application report [Designing and Manufacturing With TI's X2SON Packages](#) (SCEA055) helps PCB designers to achieve optimal designs.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV70x1 device family. The [TLV7011 Micro-Power Comparator Dip Adaptor Evaluation Module](#) can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- [Designing and Manufacturing With TI's X2SON Packages](#) (SCEA055)
- [Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters](#) (SNVA808)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7031DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	11E2	Samples
TLV7031DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	19P	Samples
TLV7031DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	19P	Samples
TLV7031DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7K	Samples
TLV7032DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22KF	Samples
TLV7032DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7032	Samples
TLV7032DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZXH	Samples
TLV7034PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV7034	Samples
TLV7034RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL7034	Samples
TLV7041DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	11F2	Samples
TLV7041DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	19Q	Samples
TLV7041DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	19Q	Samples
TLV7041DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7L	Samples
TLV7042DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22LF	Samples
TLV7042DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7042	Samples
TLV7042DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZZH	Samples
TLV7044PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV7044	Samples
TLV7044RTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL7044	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV7031, TLV7032, TLV7034, TLV7041, TLV7042, TLV7044 :

- Automotive : [TLV7031-Q1](#), [TLV7032-Q1](#), [TLV7034-Q1](#), [TLV7041-Q1](#), [TLV7042-Q1](#), [TLV7044-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7031DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7031DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7031DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7031DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7031DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7032DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7032DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7032DSGR	WSOP	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7034PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7034RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV7041DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7041DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7041DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7041DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7041DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7042DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7042DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7042DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7044PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7044RTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7031DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7031DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7031DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV7031DCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV7031DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7032DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7032DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7032DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV7034PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV7034RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV7041DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7041DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7041DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV7041DCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV7041DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7042DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7042DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7042DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7044PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV7044RTER	WQFN	RTE	16	5000	367.0	367.0	35.0

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

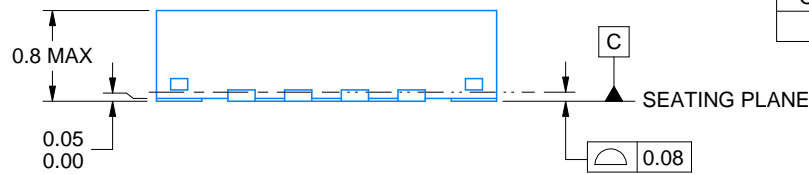
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4219117/B 04/2022

NOTES:

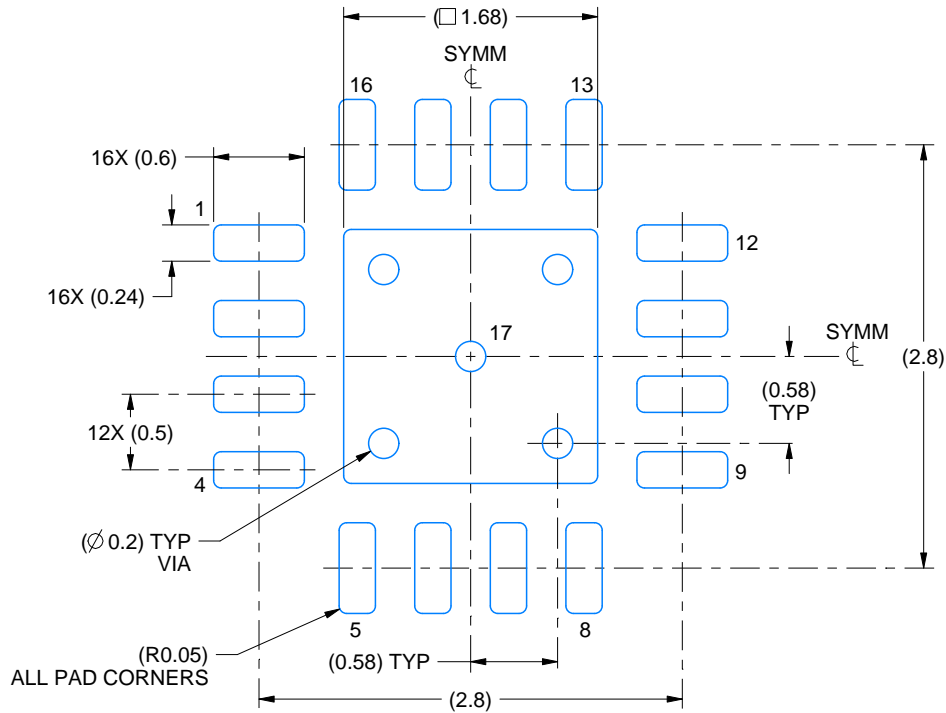
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

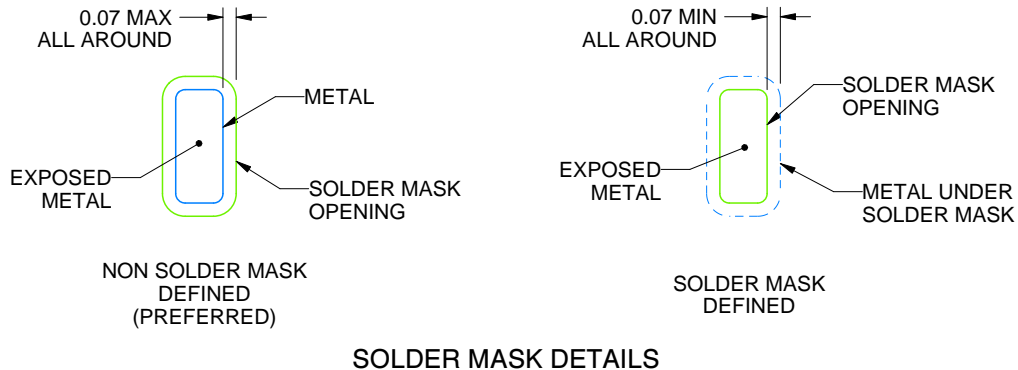
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DPW 5

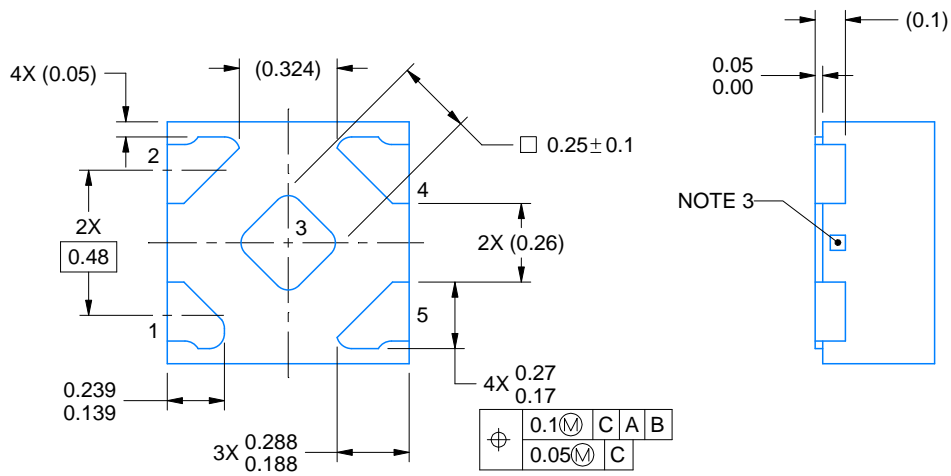
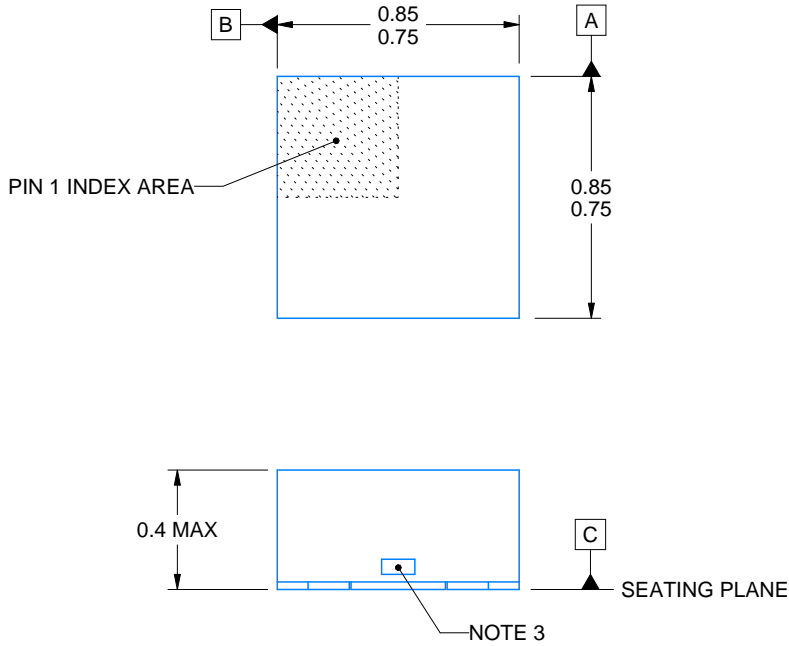
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

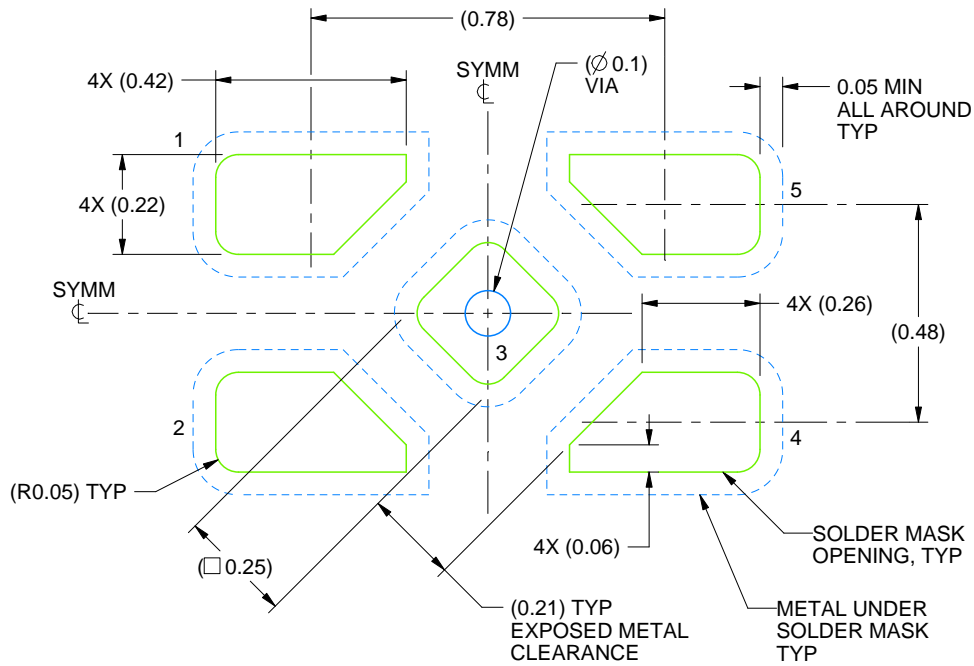
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sl原因271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

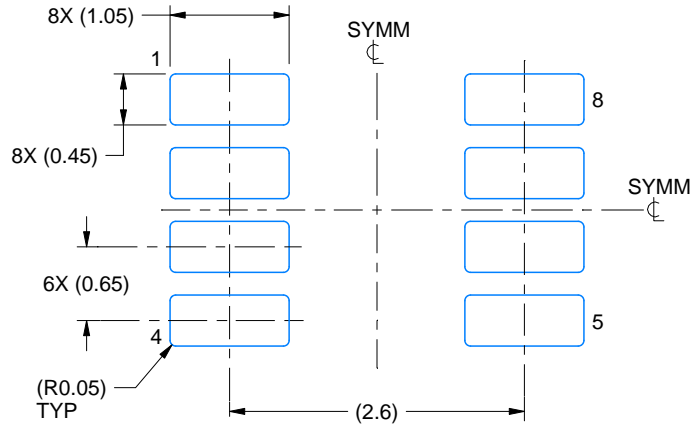
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

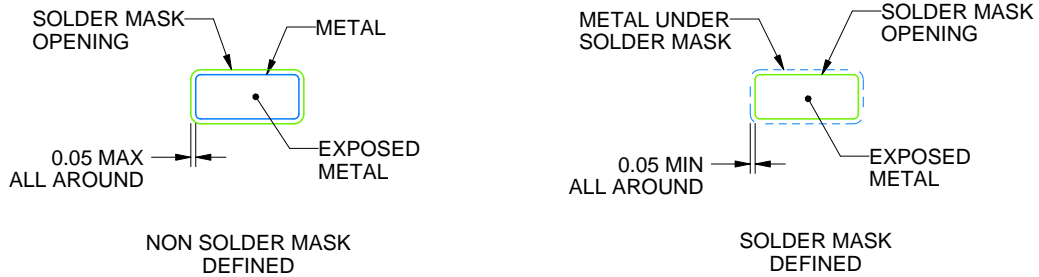
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

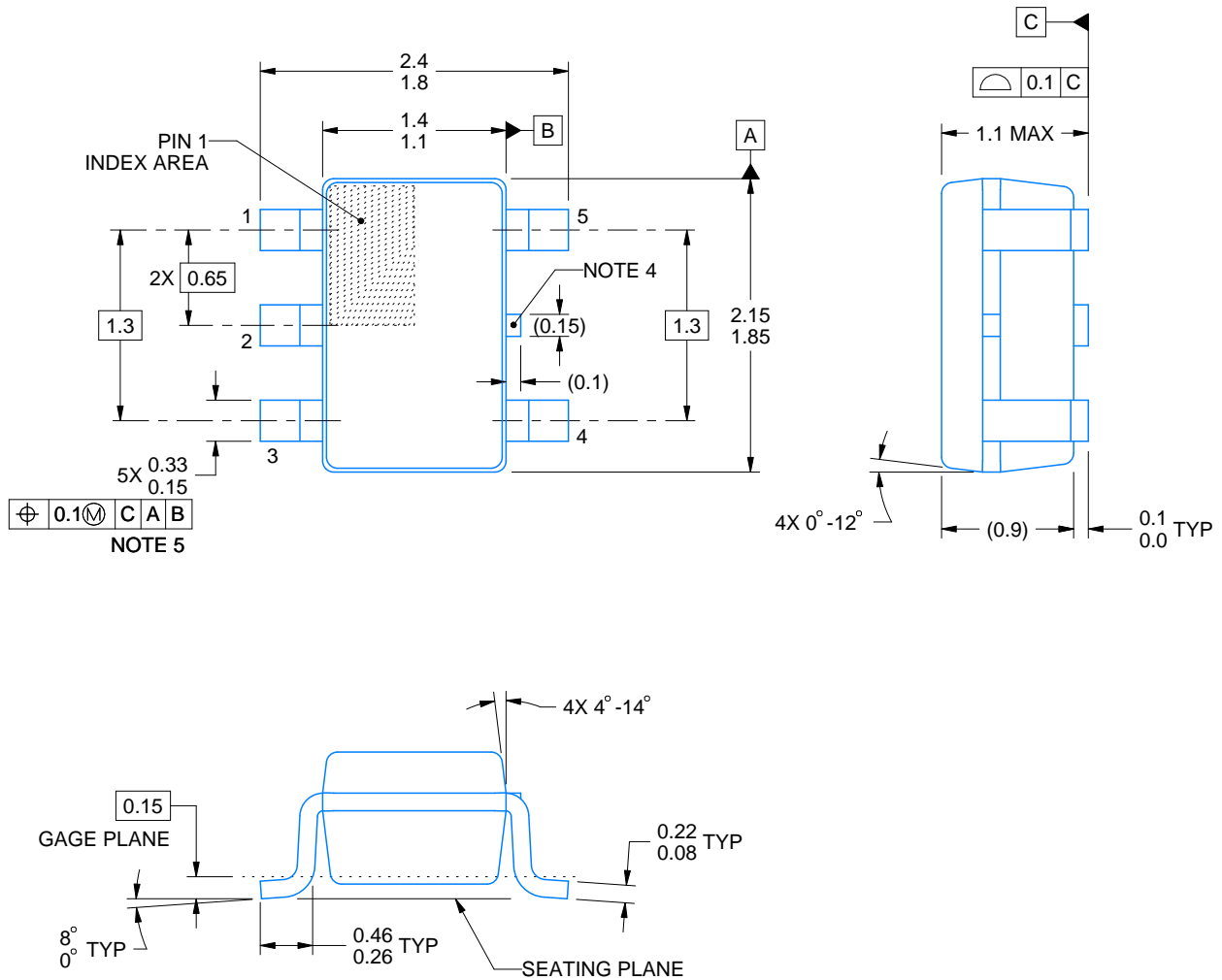
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

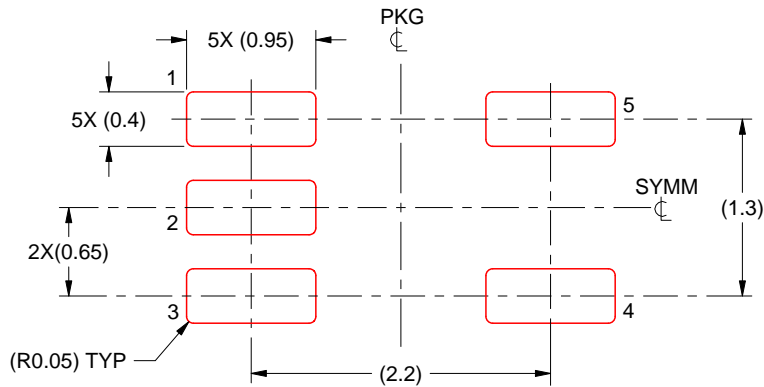
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

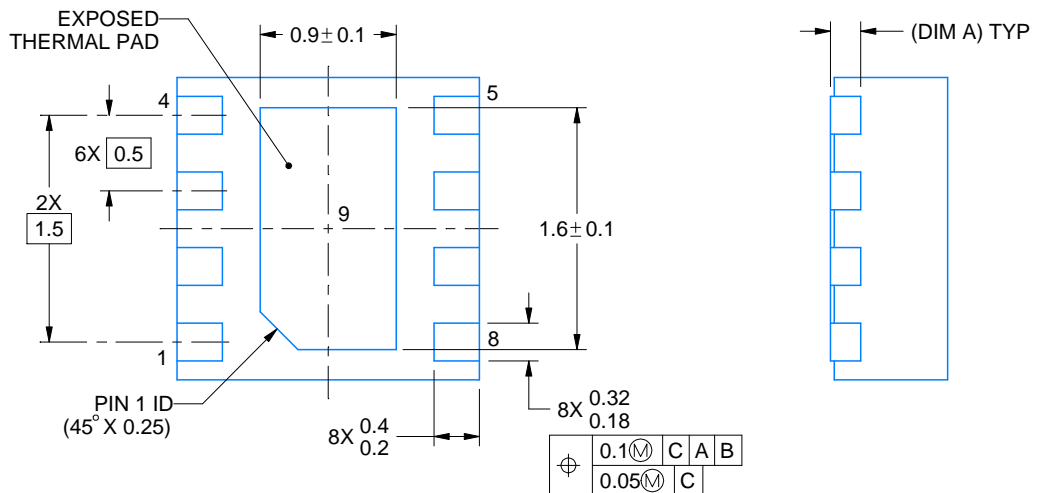
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



⌀	0.1	M	C	A	B
	0.05	M	C		

4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated