TLV707、TLV707P
200mA、低 I_Q、低ノイズ、低ドロップアウトの携帯型デバイス用レギュレータ

1 特長

- 標準精度:0.5%
- 200mA の出力をサポート
- 低 I_Q:25µA
- 0.85V～5.0V の固定出力電圧の組み合わせが可能(1)
- 高 PSRR:
  - 100Hz 時に 70dB
  - 1MHz 時に 50dB
- 実効容量 0.1µF で安定(2)
- サーマル・シャットダウン機能と過電流保護機能
- パッケージ:1mm × 1mm DQN (X2SON) [1] [2]

2 アプリケーション

- スマートフォンおよびワイヤレス・ハンドセット
- ゲームおよび玩具
- WLAN および他の PC アドオン・カード
- テレビおよびセットトップ・ボックス
- ウェアラブル電子機器

3 概要

TLV707 シリーズ (TLV707 および TLV707P) の低ドロップアウト・リニア・レギュレータ (LDO) は、静止電流が低く、ラインおよび負荷過渡特性が優れた、低消費電力が重要なアプリケーション向けのデバイスです。これらのデバイスの一般的な精度は 0.5% です。すべてのバージョンには安全性のため、サーマル・シャットダウンおよび過電流保護機能が搭載されています。

さらに、これらのデバイスはわずか 0.1µF の実効出力容量で安定します。この特長により、バイアス電圧が高く温度ディレーティングが大きい、コスト効率の高いコンデンサを使用できます。これらのデバイスは、出力負荷なしでも指定の精度へのレギュレーションを行います。

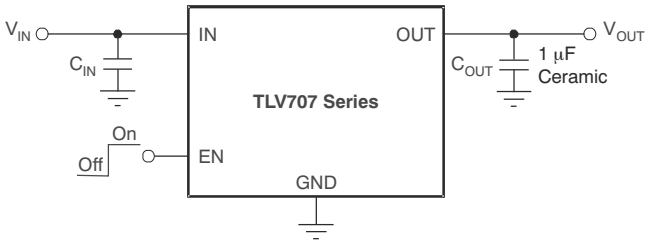
また、TLV707P にはアクティブ・プルダウン回路もあり、出力を迅速に放電します。

TLV707 シリーズの LDO は 1mm × 1mm の DQN (X2SON) パッケージで供給されるため、携帯型アプリケーションに好適です。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (2)
TLV707	DQN (X2SON、4)	1.00mm × 1.00mm
TLV707P		

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路

[1] 利用可能なすべての電圧オプションについては、データシートの末尾にあるパッケージ・オプションの付録を参照してください。
[2] 詳細については、「メカニカル、パッケージ、および注文情報」セクションを参照してください。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (May 2018) to Revision G (June 2023)	Page
• ドキュメントに TLV707xxA の情報を追加	1
• Added TLV707xxA information to $V_{(DO)}$ and I_{CL} parameters in *Electrical Characteristics* table	5
• Added TLV707xxA information to *Device Nomenclature* section	25

Changes from Revision E (February 2016) to Revision F (May 2018)	Page
• Changed $V_{(ESD)}$ HBM value from ±2000 V to ±4000 V in *ESD Ratings* table	4

5 Pin Configuration and Functions

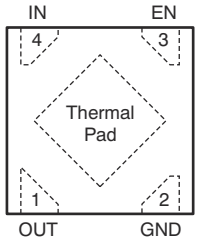


図 5-1. DQN Package, 4-Pin X2SON (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. For TLV707P, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
GND	2	—	Ground pin
IN	4	I	Input pin. For good transient performance, place a small 1-µF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Requirements* for more details.
OUT	1	O	Regulated output voltage pin. A small 1-µF ceramic capacitor is required from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6.0	V
	EN	–0.3	6.0	V
	OUT	–0.3	6.0	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)(1)	±4000	V
		Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.0		5.5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV707, TLV707P DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	108.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	159.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	159.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	110.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

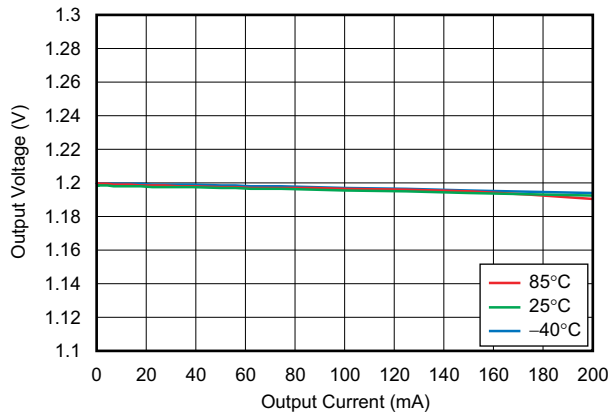
at V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 0.47 µF, and T_J = –40°C to +85°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage range				0.85		5	V
	DC output accuracy					0.5%		
		V_{OUT} ≥ 0.85 V			–1.5%		1.5%	
$\Delta V_{O\ (\Delta VI)}$	Line regulation					1	5	mV
$\Delta V_{O\ (\Delta IO)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA				10	20	mV
$V_{(DO)}$	Dropout voltage	V_{IN} = 0.98 x $V_{OUT(nom)}$	2.0 V < V_{OUT} ≤ 2.4 V	I_{OUT} = 30 mA		65		mV
				I_{OUT} = 150 mA		325	360	
			2.4 V < V_{OUT} ≤ 2.8 V	I_{OUT} = 30 mA		50		
				I_{OUT} = 150 mA		250	300	
			2.8 V < V_{OUT} ≤ 3.3 V	I_{OUT} = 30 mA		45		
				I_{OUT} = 150 mA		220	270	
			3.3 V < V_{OUT} ≤ 5.0 V	I_{OUT} = 30 mA		40		
				I_{OUT} = 150 mA		200	250	
$V_{(DO)}$	Dropout voltage, TLV707xxA	V_{IN} = 0.98 × $V_{OUT(nom)}$	2.0 V < VOUT ≤ 2.5 V	I_{OUT} = 30 mA		65		mV
				I_{OUT} = 150 mA		325	360	
			2.5 V < VOUT ≤ 3.1 V	I_{OUT} = 30 mA		50		
				I_{OUT} = 150 mA		250	300	
			3.1 V < VOUT ≤ 3.5 V	I_{OUT} = 30 mA		45		
				I_{OUT} = 150 mA		220	280	
			3.5 V < VOUT ≤ 5.0 V	I_{OUT} = 30 mA		40		
				I_{OUT} = 150 mA		200	260	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$			240	300	450	mA
I_{CL}	Output current limit, TLV707xxA	V_{OUT} = 0.9 × $V_{OUT(nom)}$, $V_{OUT(nom)}$ ≤ 1.5 V			220	300	450	mA
		V_{OUT} = 0.9 × $V_{OUT(nom)}$, $V_{OUT(nom)}$ > 1.5 V			240	300	450	
$I_{(GND)}$	Ground pin current	I_{OUT} = 0 mA				25	50	µA
$I_{(EN)}$	EN pin current	V_{EN} = 5.5 V				0.01		µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V				1		µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)				0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)				0.9		V_{IN}	V
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA		f = 100 Hz		70		dB
				f = 10 kHz		55		
				f = 1 MHz		50		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA				45		μV_{RMS}
t_{STR}	Start-up time(1)	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA				100		µs
$R_{PULLDOWN}$	Pulldown resistance (TLV707P only)					120		Ω

(1) Start-up time = time from EN assertion to 0.98 × V_{OUT}.

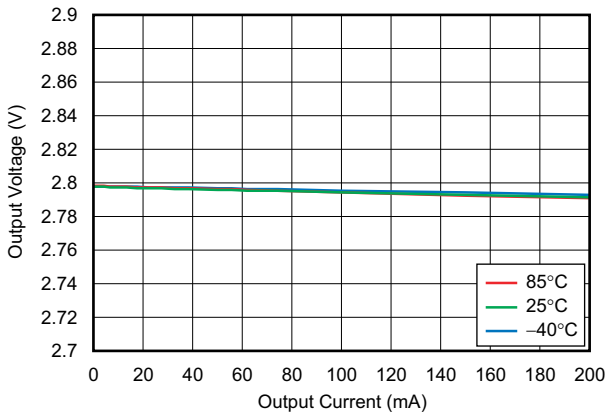
6.6 Typical Characteristics

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



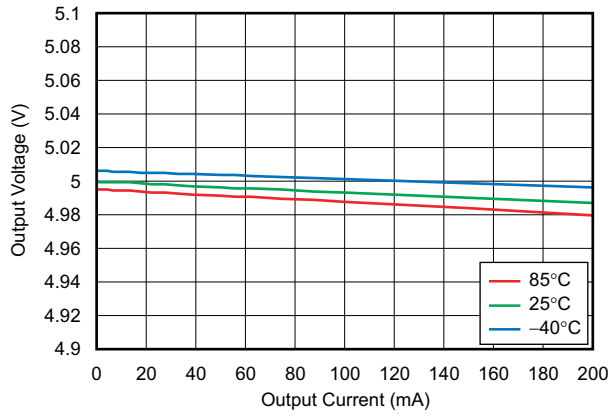
V_{OUT} = 1.2 V

図 6-1. Load Regulation



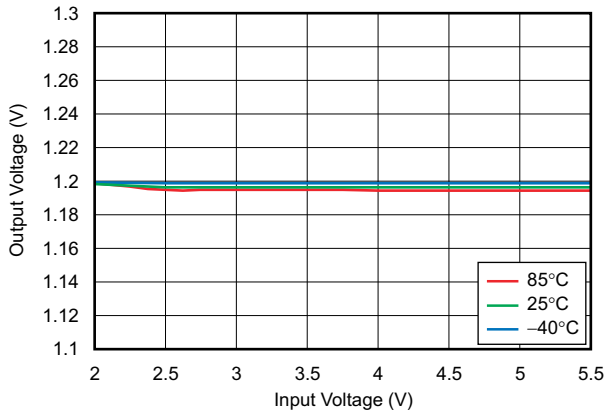
V_{OUT} = 2.8 V

図 6-2. Load Regulation



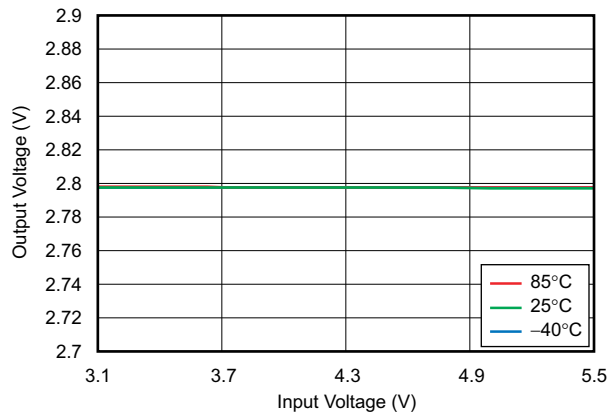
V_{OUT} = 5.0 V

図 6-3. Load Regulation



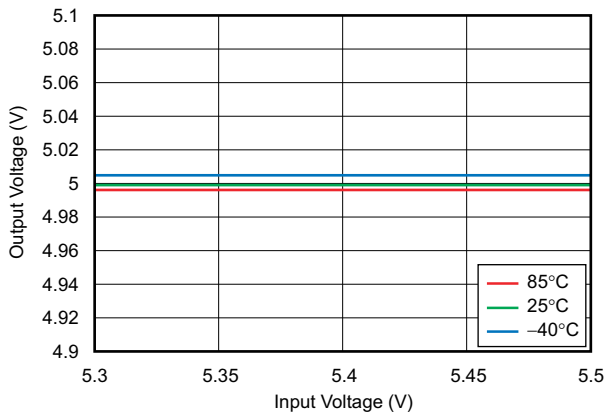
V_{OUT} = 1.2 V, I_{OUT} = 10 mA

図 6-4. Line Regulation



V_{OUT} = 2.8 V, I_{OUT} = 10 mA

図 6-5. Line Regulation

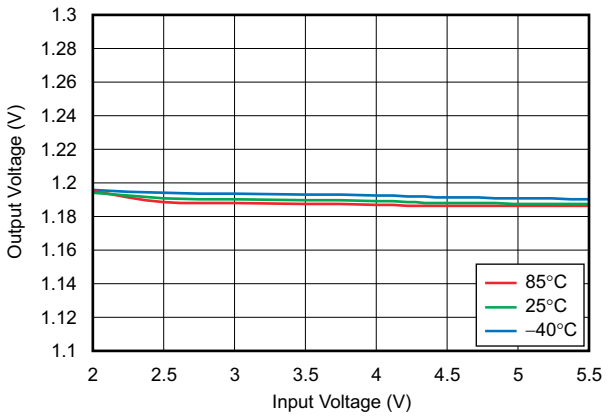


V_{OUT} = 5.0 V, I_{OUT} = 10 mA

図 6-6. Line Regulation

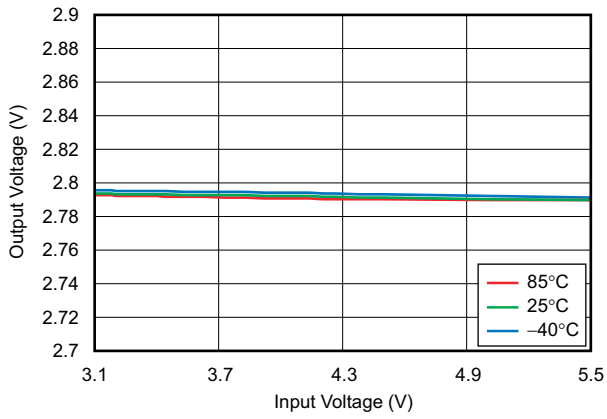
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



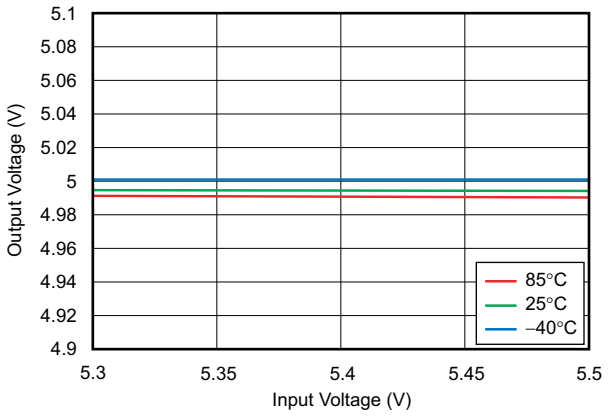
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

図 6-7. Line Regulation



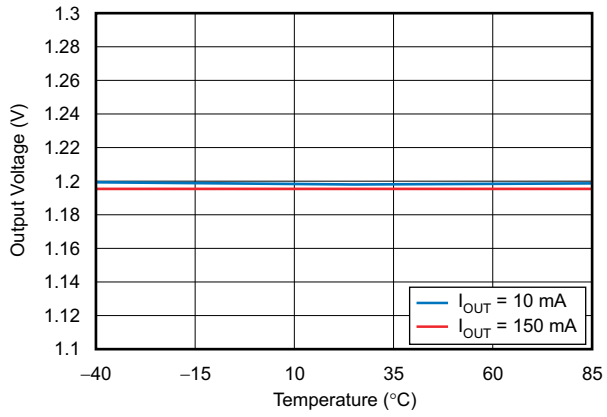
V_{OUT} = 2.8 V, I_{OUT} = 150 mA

図 6-8. Line Regulation



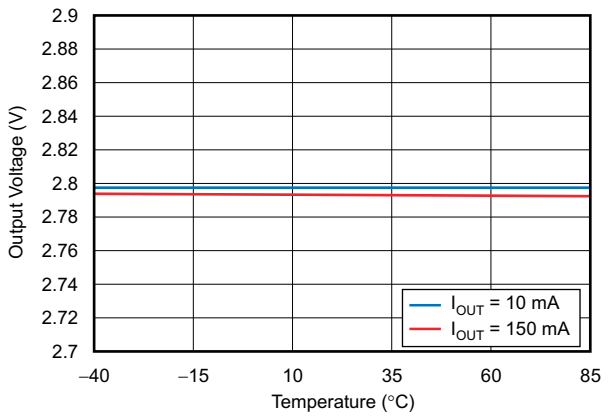
V_{OUT} = 5.0 V, I_{OUT} = 150 mA

図 6-9. Line Regulation



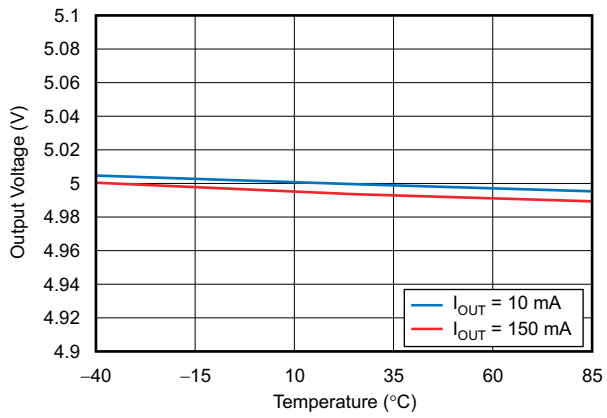
V_{OUT} = 1.2 V

図 6-10. Output Voltage vs Temperature



V_{OUT} = 2.8 V

図 6-11. Output Voltage vs Temperature

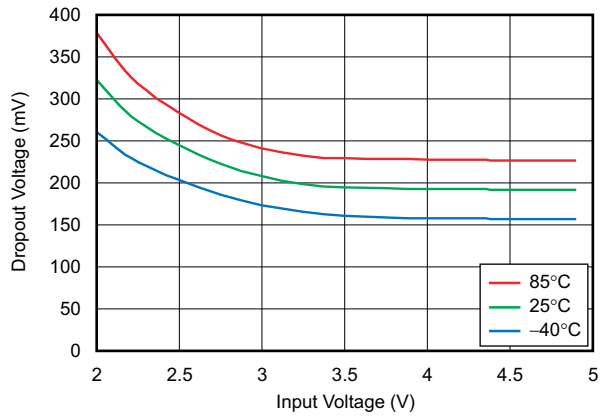


V_{OUT} = 5.0 V

図 6-12. Output Voltage vs Temperature

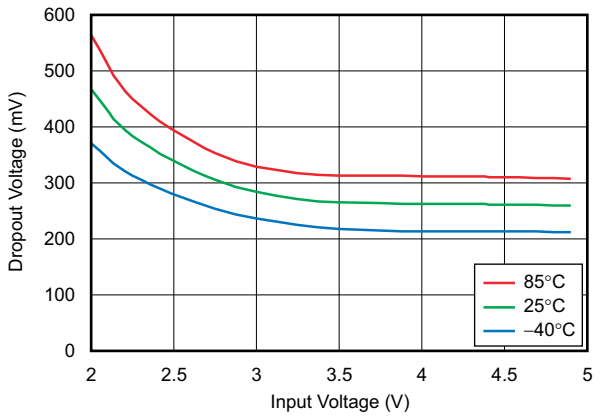
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



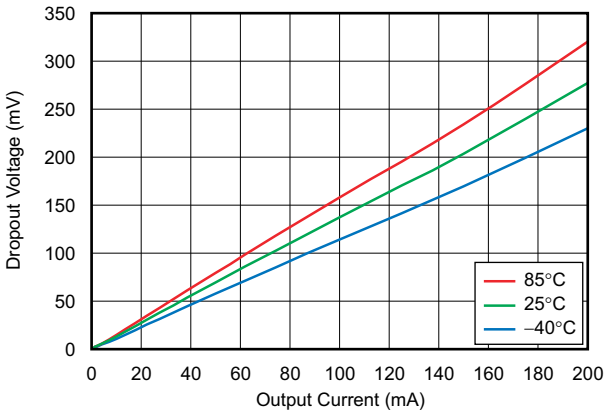
I_{OUT} = 150 mA

図 6-13. Dropout Voltage vs Input Voltage



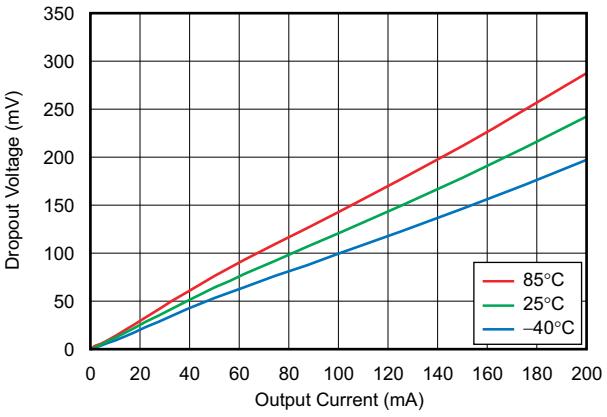
I_{OUT} = 200 mA

図 6-14. Dropout Voltage vs Input Voltage



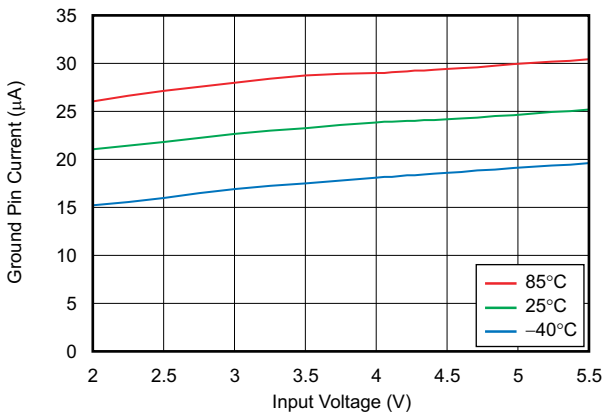
V_{OUT} = 2.8 V

図 6-15. Dropout Voltage vs Output Current



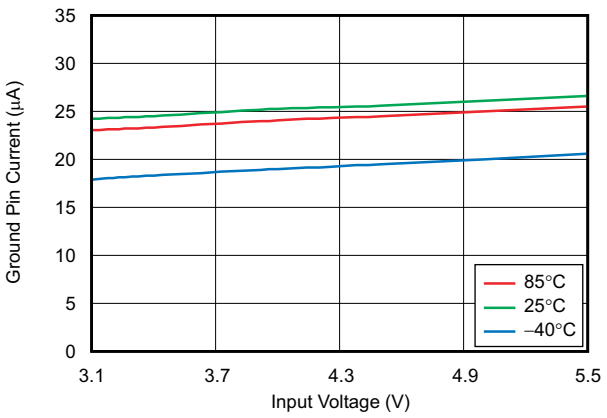
V_{OUT} = 5.0 V

図 6-16. Dropout Voltage vs Output Current



V_{OUT} = 1.2 V, I_{OUT} = 0 mA

図 6-17. Ground Pin Current vs Input Voltage

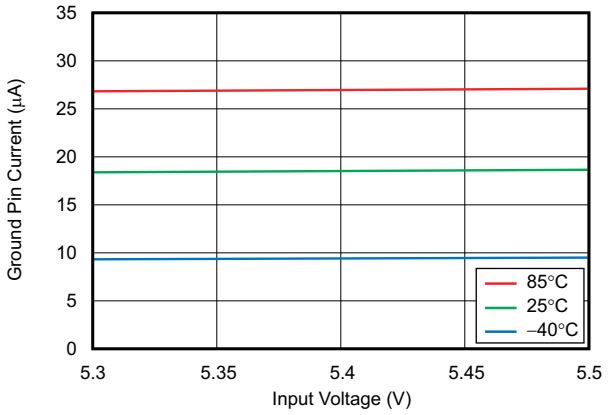


V_{OUT} = 2.8 V, I_{OUT} = 0 mA

図 6-18. Ground Pin Current vs Input Voltage

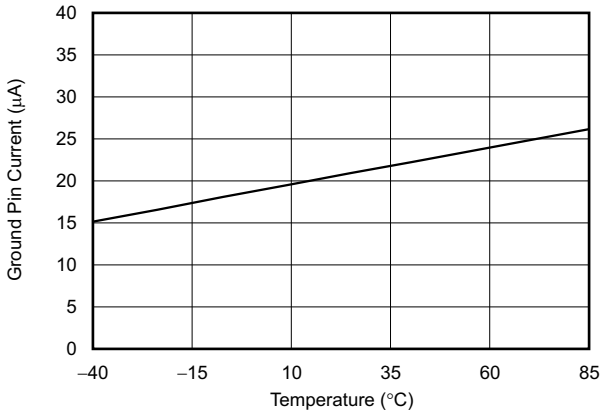
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



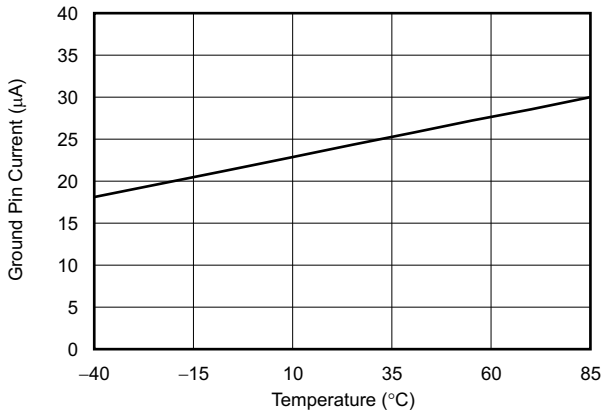
V_{OUT} = 5.0 V, I_{OUT} = 0 mA

図 6-19. Ground Pin Current vs Input Voltage



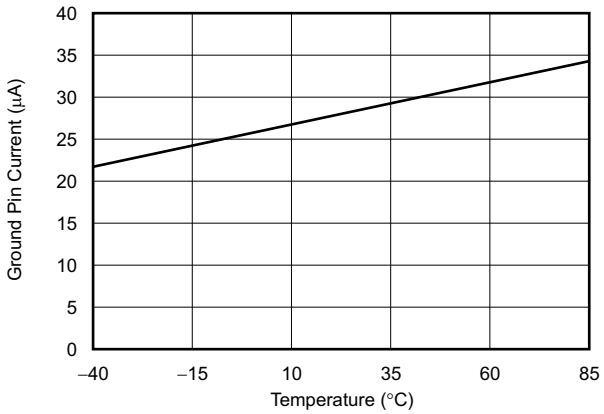
V_{OUT} = 1.2 V, I_{OUT} = 0 mA

図 6-20. Ground Pin Current vs Temperature



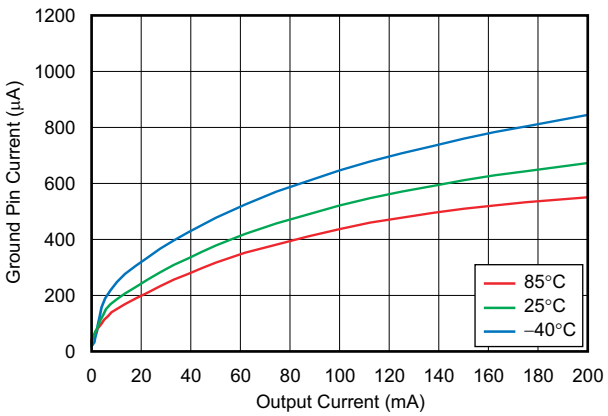
V_{OUT} = 2.8 V, I_{OUT} = 0 mA

図 6-21. Ground Pin Current vs Temperature



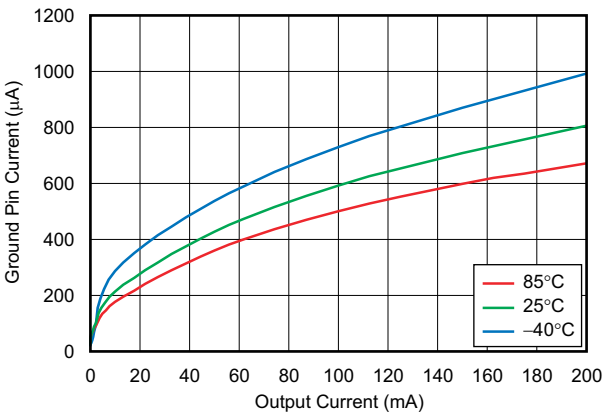
V_{OUT} = 5.0 V, I_{OUT} = 0 mA

図 6-22. Ground Pin Current vs Temperature



V_{OUT} = 1.2 V

図 6-23. Ground Pin Current vs Output Current

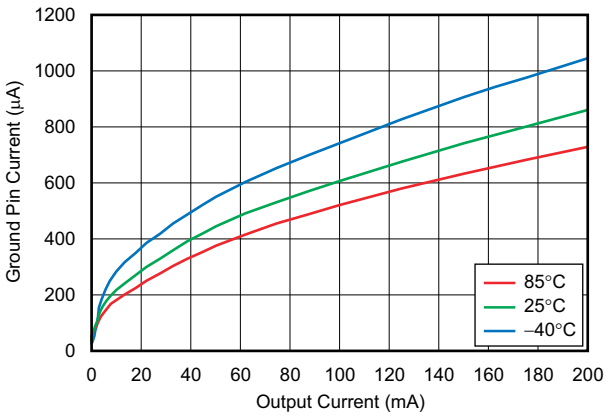


V_{OUT} = 2.8 V

図 6-24. Ground Pin Current vs Output Current

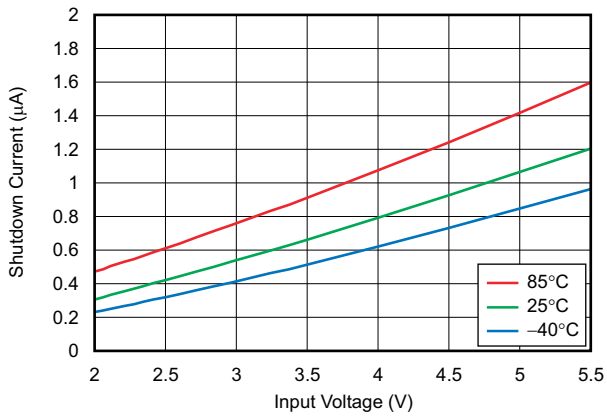
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



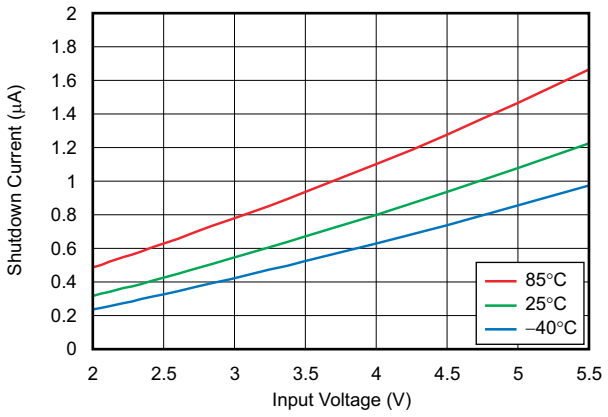
V_{OUT} = 5.0 V

図 6-25. Ground Pin Current vs Output Current



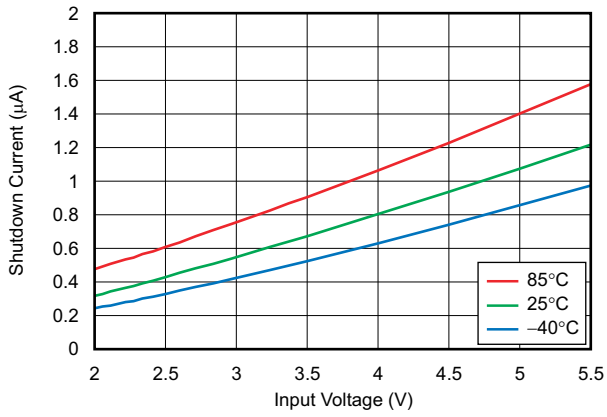
V_{OUT} = 1.2 V

図 6-26. Shutdown Current vs Input Voltage



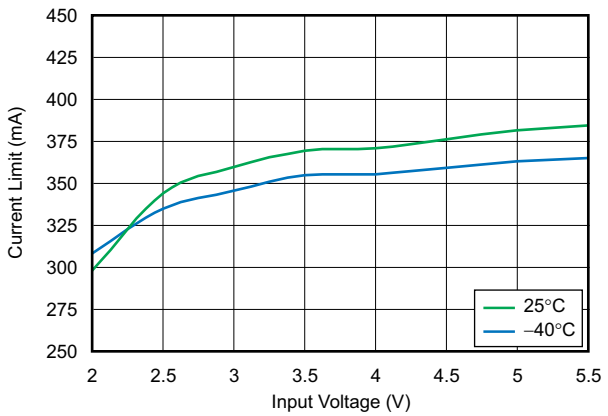
V_{OUT} = 2.8 V

図 6-27. Shutdown Current vs Input Voltage



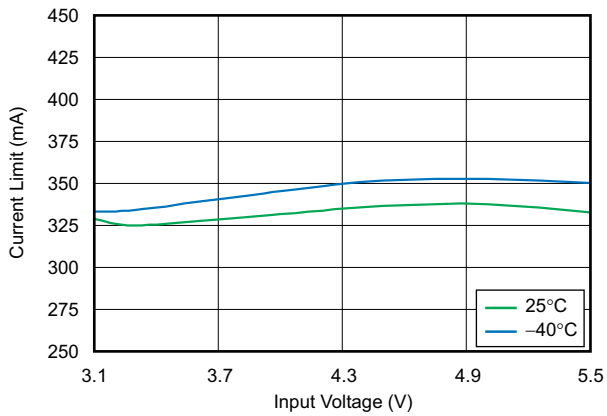
V_{OUT} = 5.0 V

図 6-28. Shutdown Current vs Input Voltage



V_{OUT} = 1.2 V

図 6-29. Current Limit vs Input Voltage

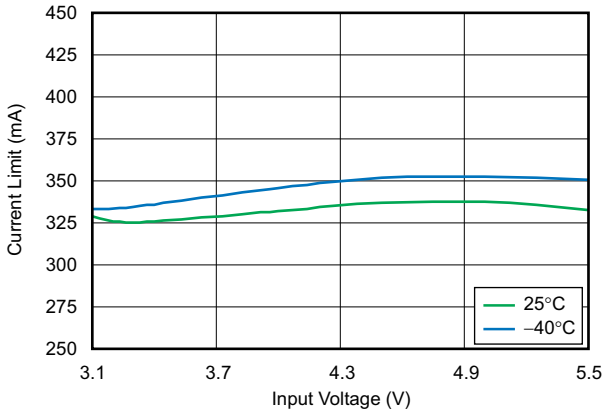


V_{OUT} = 2.8 V

図 6-30. Current Limit vs Input Voltage

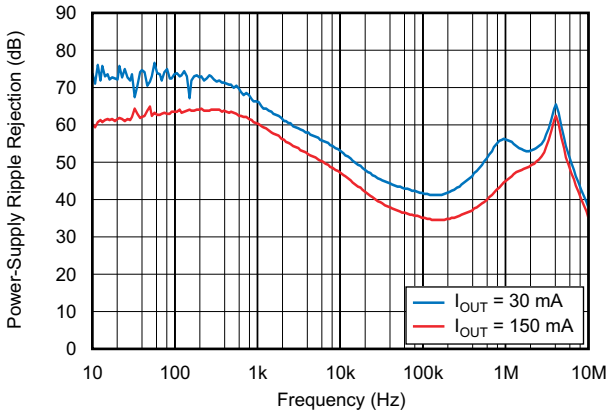
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



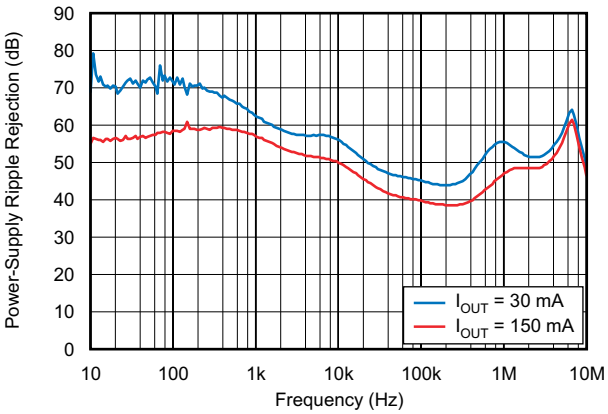
V_{OUT} = 5.0 V

図 6-31. Current Limit vs Input Voltage



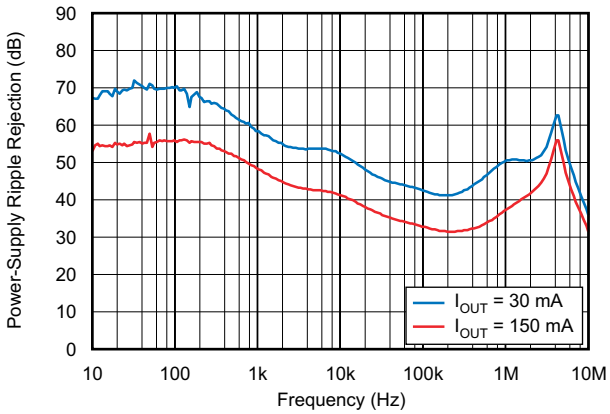
V_{OUT} = 1.2 V

図 6-32. Power-Supply Ripple Rejection vs Frequency



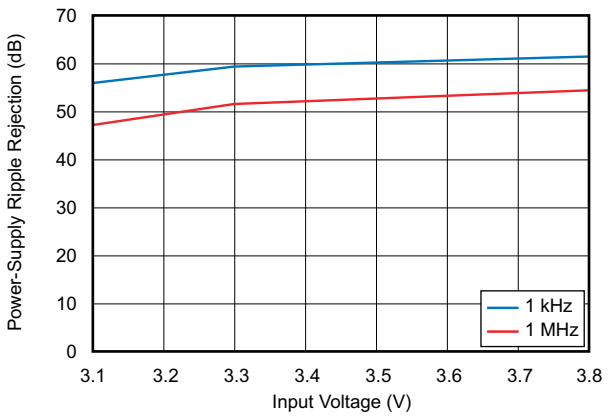
V_{OUT} = 2.8 V

図 6-33. Power-Supply Ripple Rejection vs Frequency



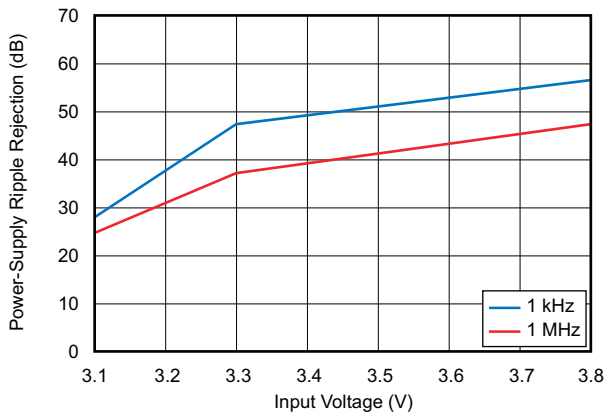
V_{OUT} = 5.0 V

図 6-34. Power-Supply Ripple Rejection vs Frequency



V_{OUT} = 2.8 V, I_{OUT} = 30 mA

図 6-35. Power-Supply Ripple Rejection vs Input Voltage

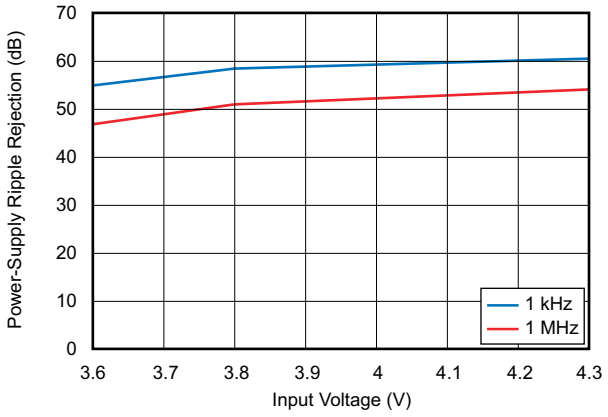


V_{OUT} = 2.8 V, I_{OUT} = 150 mA

図 6-36. Power-Supply Ripple Rejection vs Input Voltage

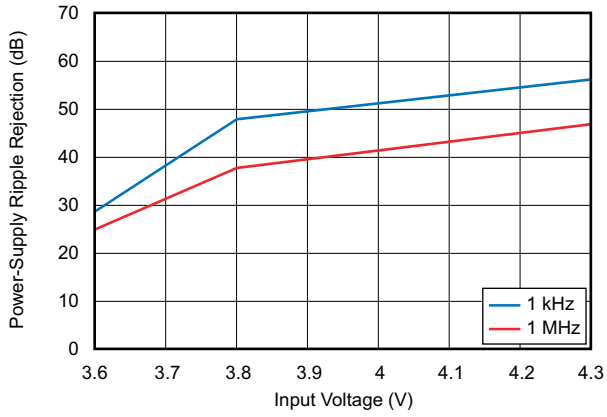
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



V_{OUT} = 3.3 V, I_{OUT} = 30 mA

図 6-37. Power-Supply Ripple Rejection vs Input Voltage



V_{OUT} = 3.3 V, I_{OUT} = 150 mA

図 6-38. Power-Supply Ripple Rejection vs Input Voltage

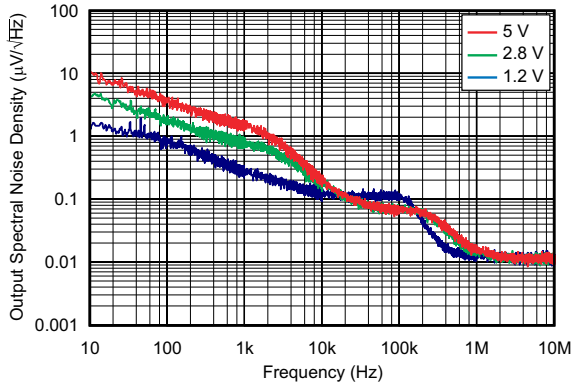
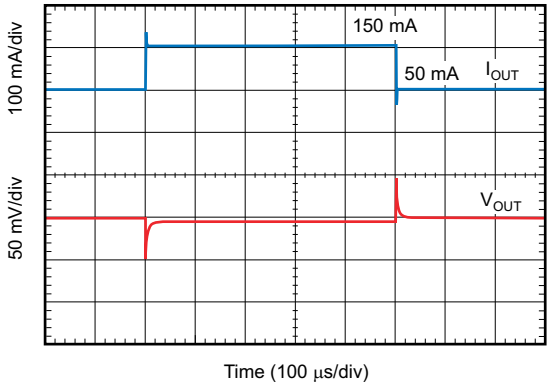
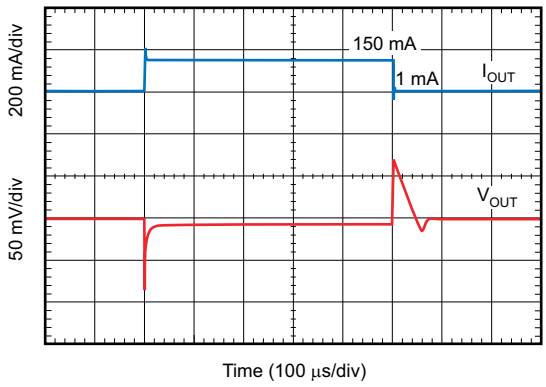


図 6-39. Output Spectral Noise Density vs Frequency



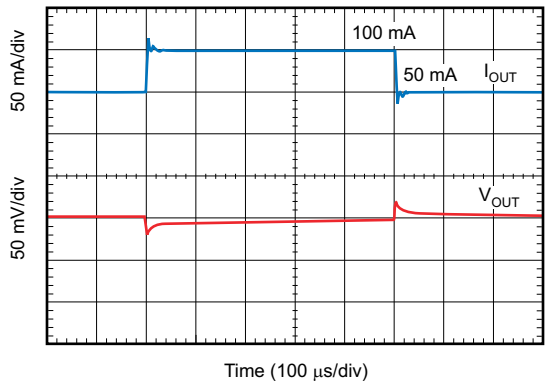
V_{OUT} = 1.2 V

図 6-40. Load Transient Response



V_{OUT} = 1.2 V

図 6-41. Load Transient Response

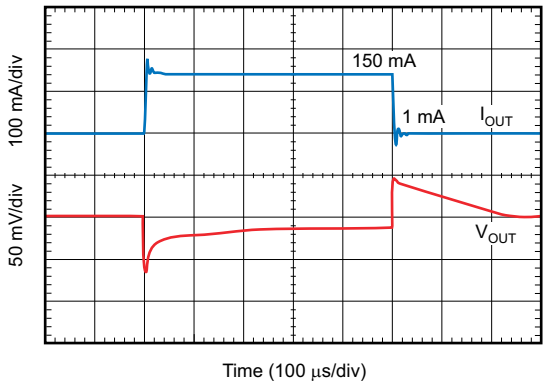


V_{OUT} = 2.8 V

図 6-42. Load Transient Response

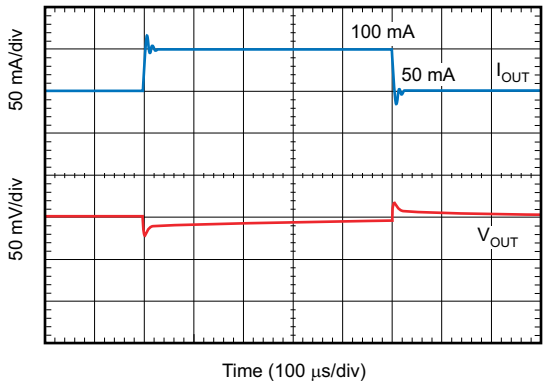
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



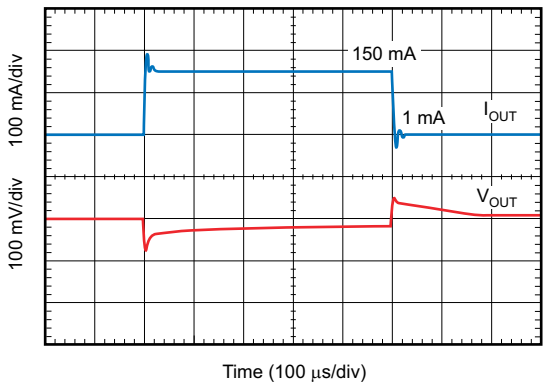
V_{OUT} = 2.8 V

図 6-43. Load Transient Response



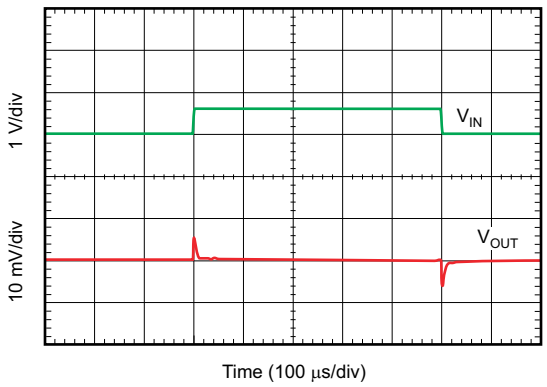
V_{OUT} = 5.0 V

図 6-44. Load Transient Response



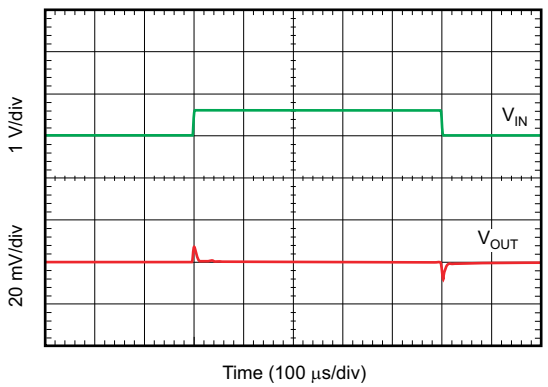
V_{OUT} = 5.0 V

図 6-45. Load Transient Response



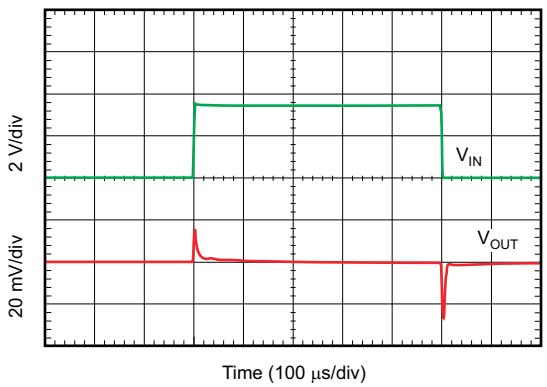
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

図 6-46. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 200 mA

図 6-47. Line Transient Response

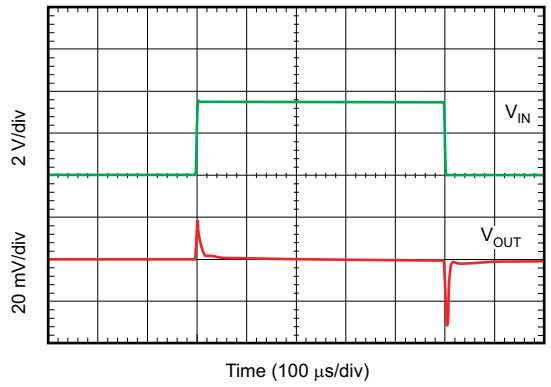


V_{OUT} = 1.2 V, I_{OUT} = 150 mA

図 6-48. Line Transient Response

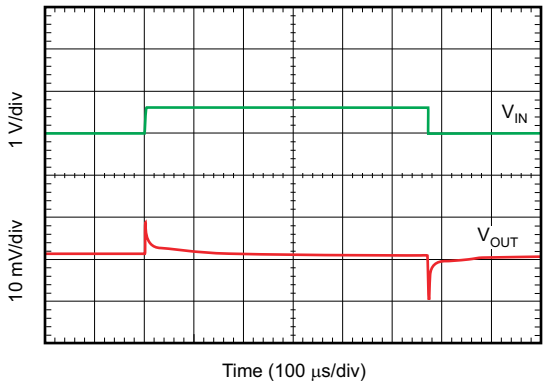
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



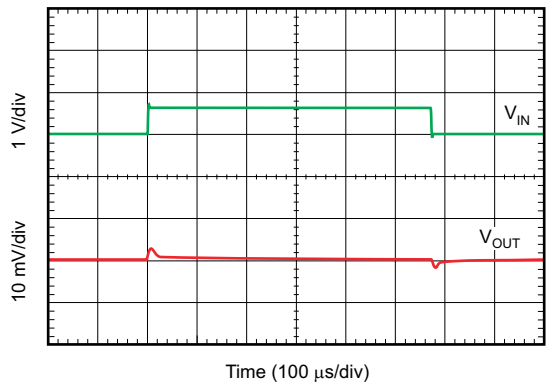
V_{OUT} = 1.2 V, I_{OUT} = 200 mA

図 6-49. Line Transient Response



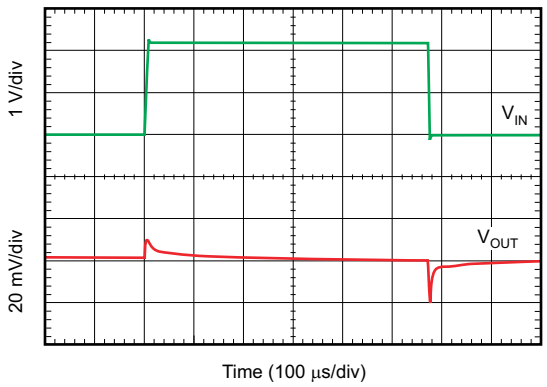
V_{OUT} = 2.8 V, I_{OUT} = 150 mA

図 6-50. Line Transient Response



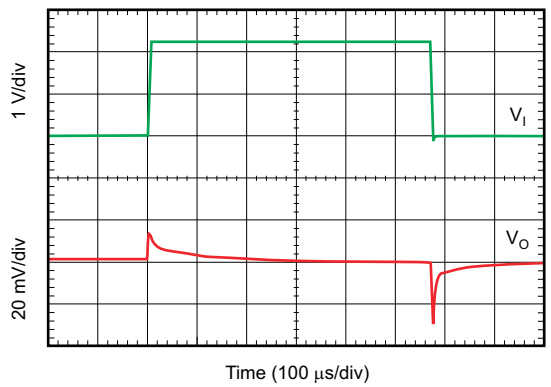
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

図 6-51. Line Transient Response



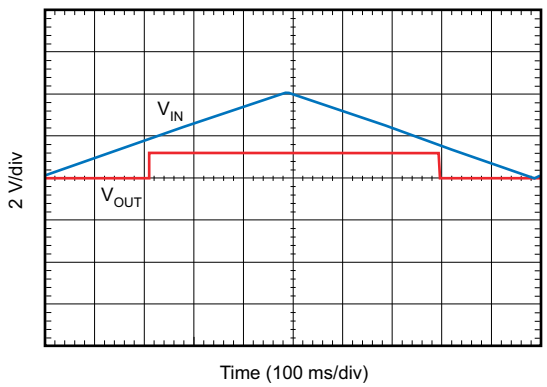
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

図 6-52. Line Transient Response



V_{OUT} = 2.8 V, I_{OUT} = 200 mA

図 6-53. Line Transient Response

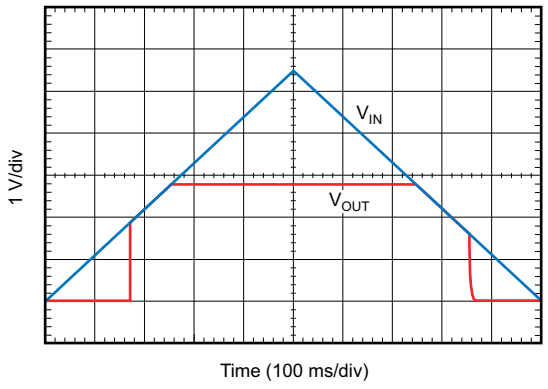


V_{OUT} = 1.2 V, I_{OUT} = 30 mA

図 6-54. V_{IN} Ramp Up, Ramp Down Response

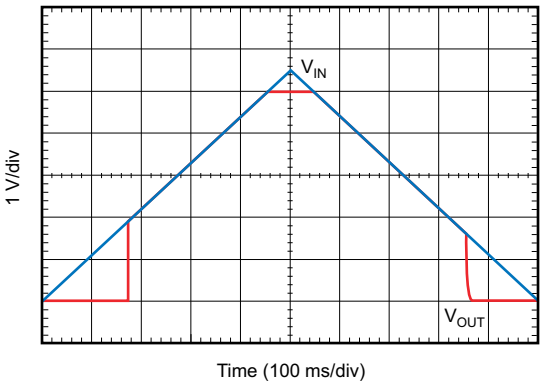
6.6 Typical Characteristics (continued)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



V_{OUT} = 2.8 V, I_{OUT} = 30 mA

図 6-55. V_{IN} Ramp Up, Ramp Down Response



V_{OUT} = 5 V, I_{OUT} = 30 mA

図 6-56. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV707 series (TLV707 and TLV707P) belongs to a family of low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this device designed for portable RF applications.

7.2 Functional Block Diagrams

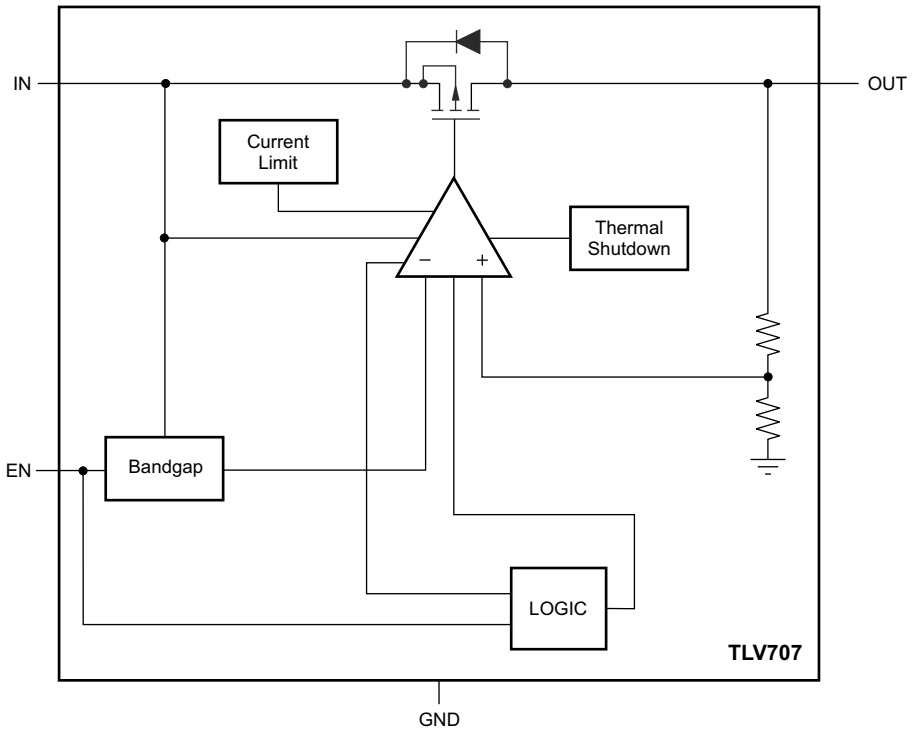


図 7-1. TLV707 Block Diagram

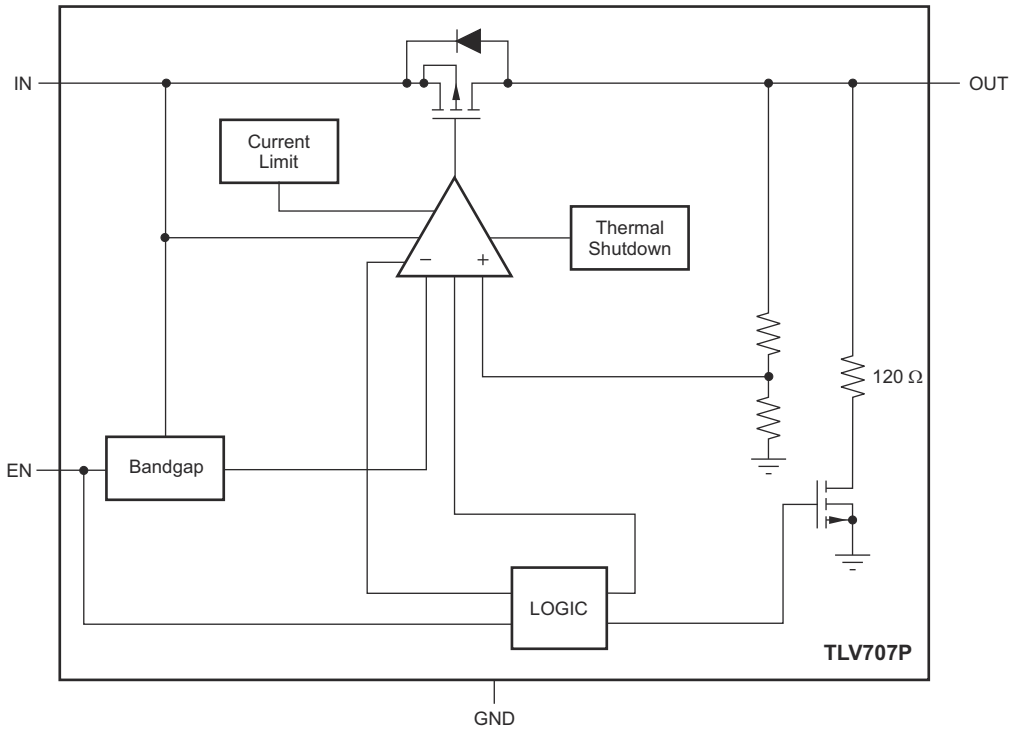


図 7-2. TLV707P Block Diagram

7.3 Feature Description

This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device is –40°C to +125°C.

7.3.1 Internal Current Limit

The internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* table for more details.

The PMOS pass transistor has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn on the LDO can also be used to power the device when connected to a GPIO of a newer processor, where the GPIO logic 1 voltage level is lower than that of traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV707P version has internal active pulldown circuitry that discharges the output with a time constant as given by 式 1:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

7.4 Device Functional Modes

The TLV707 series is specified over the recommended operating conditions (see the *Recommended Operating Conditions* table). The specifications can possibly not be met when exposed to conditions outside of the recommended operating range.

In order to turn on the regulator, the EN pin must be driven over 0.9 V. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device is reduced to 1 µA, typically.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV707 series is a low-dropout regulator (LDO) with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device series is –40°C to +125°C.

8.2 Typical Application

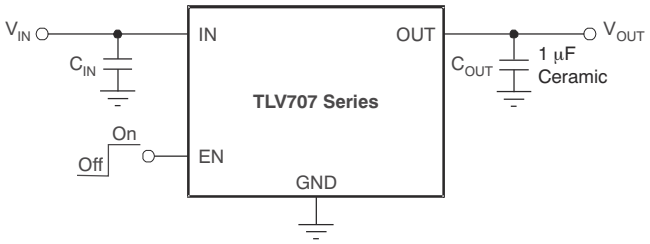


図 8-1. Typical Application Circuit

8.2.1 Design Requirements

Provide an input supply with adequate headroom to meet minimum VIN requirements (as shown in 表 8-1), compensate for the GND pin current, and to power the load.

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V–3.6 V
Output voltage	1.2 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Generally, 1.0-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV707 is designed to be stable with an effective capacitance of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of less expensive dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions is less than 0.1 µF. Maximum ESR must be less than 200 mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1.0-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2-Ω, a 0.1-µF input capacitor can be necessary to provide stability.

8.2.2.2 Dropout Voltage

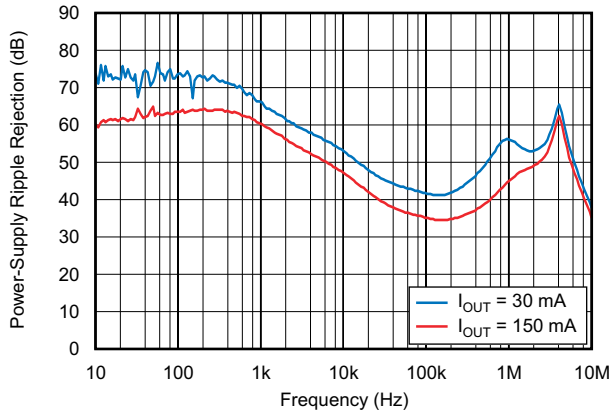
The TLV707 series of LDOs use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass transistor. V_{DO} scales approximately with output current because the PMOS transistor functions similar to a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout.

8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves



V_{OUT} = 1.2 V

図 8-2. Power-Supply Ripple Rejection vs Frequency

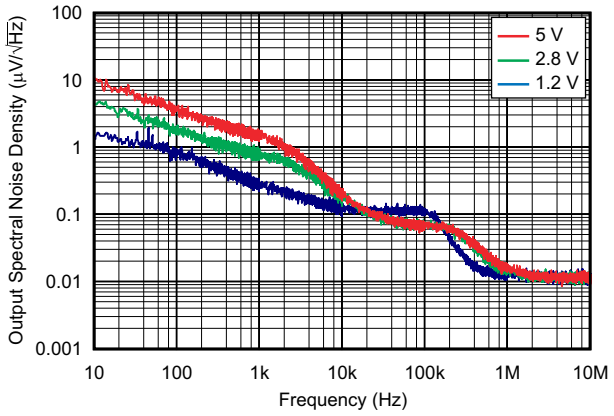
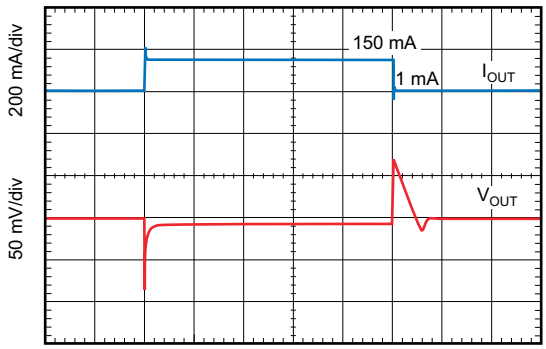
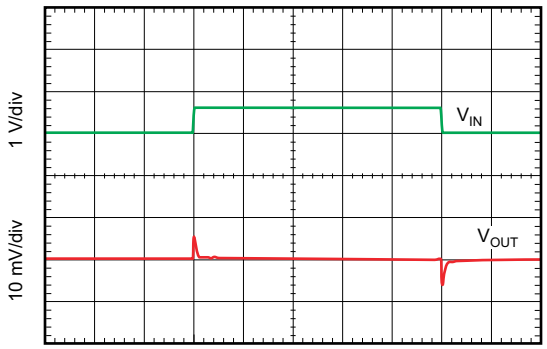


図 8-3. Output Spectral Noise Density vs Frequency



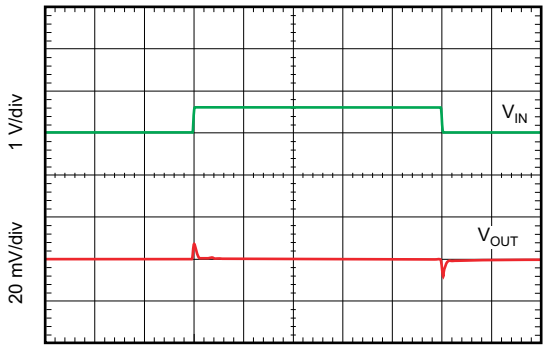
V_{OUT} = 1.2 V

図 8-4. Load Transient Response



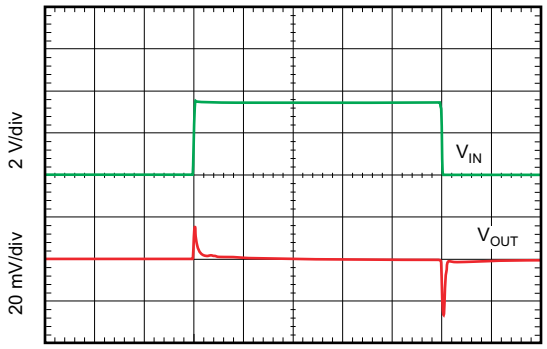
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

図 8-5. Line Transient Response



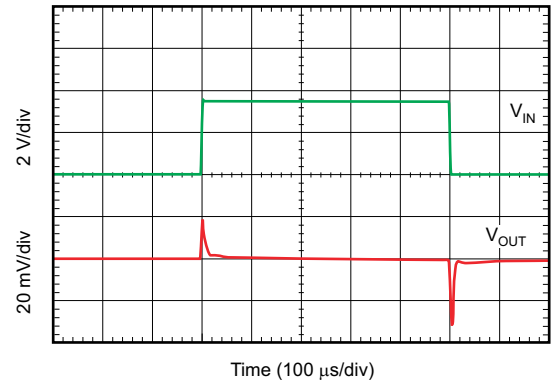
V_{OUT} = 1.2 V, I_{OUT} = 200 mA

図 8-6. Line Transient Response



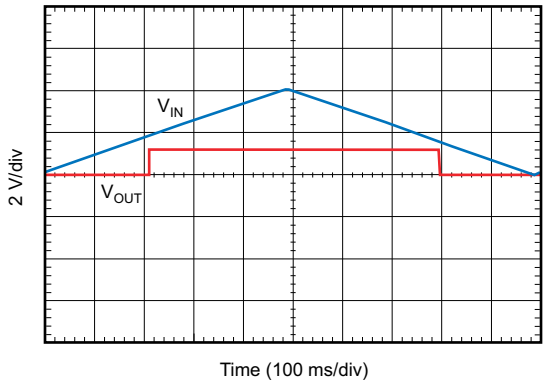
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

図 8-7. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 200 mA

図 8-8. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 30 mA

図 8-9. V_{IN} Ramp Up, Ramp Down Response

8.3 Best Design Practices

Place at least one 1.0-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 1.0-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

8.4 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.0 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated (see 図 6-46 through 図 6-53). If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

8.5 Layout

8.5.1 Layout Guidelines

8.5.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device, as shown in 図 8-10. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors can degrade PSRR performance.

8.5.1.2 Package Mounting

Solder pad footprint recommendations are available from TI's website at www.ti.com. The recommended land pattern for the DQN (X2SON-4) package is provided in the *Mechanical, Packaging, and Orderable Information* section.

8.5.1.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the LDO is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the LDO into thermal shutdown degrades device reliability.

8.5.1.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in 式 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

8.5.2 Layout Example

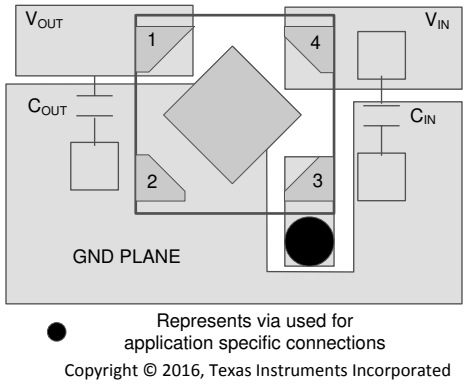


図 8-10. Recommended Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV707 and TLV707P. SLVU416 details the design kits and evaluation modules for TLV70728EVM-612.

The EVM can be requested at the Texas Instruments web site through the TLV707 and TLV707P product folders, or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV707 and TLV707P is available through the respective device product folders under *Simulation Models*.

9.1.2 Device Nomenclature

表 9-1. Ordering Information(1)

PRODUCT	V_{OUT} (2)
TLV707**xx(x)(A)(*P*)yyyz**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V, 285 = 2.85 V). **A** indicates a more recent design revision. **P** is optional; devices with P have an LDO regulator with an active output discharge. **yyy** is the package designator. **z** is the package quantity. Use ***R*** for reel (3000 pieces), and ***T*** for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.85 V to 5.0 V in 50-mV increments are available. Contact factory for details and availability.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV70728EVM-612 Evaluation Module* user guide

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated family of devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV707085DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BY	Samples
TLV707085DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BY	Samples
TLV70710DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BB	Samples
TLV70710DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BB	Samples
TLV70710PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BC	Samples
TLV70710PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BC	Samples
TLV707115DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B3	Samples
TLV707115DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B3	Samples
TLV70711PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3	Samples
TLV70711PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C3	Samples
TLV70712APDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N6	Samples
TLV70712PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WJ	Samples
TLV70712PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WJ	Samples
TLV707135DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD	Samples
TLV707135DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BD	Samples
TLV70715PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WI	Samples
TLV70715PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WI	Samples
TLV70717DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GD	Samples
TLV70717DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GD	Samples
TLV707185ADQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MZ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV707185DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZN	Samples
TLV707185DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZN	Samples
TLV707185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B1	Samples
TLV707185PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B1	Samples
TLV70718ADQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MX	Samples
TLV70718APDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N7	Samples
TLV70718DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZC	Samples
TLV70718DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZC	Samples
TLV70718PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SB	Samples
TLV70718PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SB	Samples
TLV70719PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZM	Samples
TLV70719PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ZM	Samples
TLV70725DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM	Samples
TLV70725DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM	Samples
TLV70725PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AT	Samples
TLV70725PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AT	Samples
TLV70726DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RF	Samples
TLV70726DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RF	Samples
TLV70726PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SC	Samples
TLV70726PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SC	Samples
TLV70727PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70727PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C6	Samples
TLV707285DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RZ	Samples
TLV707285DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RZ	Samples
TLV707285PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	XE	Samples
TLV707285PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	XE	Samples
TLV70728APDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N8	Samples
TLV70728PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SD	Samples
TLV70728PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SD	Samples
TLV70729DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BF	Samples
TLV70729DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BF	Samples
TLV70729PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BG	Samples
TLV70729PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BG	Samples
TLV70730ADQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N1	Samples
TLV70730APDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N2	Samples
TLV70730DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TLV70730DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HJ	Samples
TLV70730PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SE	Samples
TLV70730PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SE	Samples
TLV70731DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DI	Samples
TLV70731DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DI	Samples
TLV70732DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70732DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C8	Samples
TLV707335ADQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N5	Samples
TLV707335DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TLV707335DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F6	Samples
TLV70733ADQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N3	Samples
TLV70733APDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N4	Samples
TLV70733DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YH	Samples
TLV70733DQNR1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BN	Samples
TLV70733DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YH	Samples
TLV70733PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TI	Samples
TLV70733PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TI	Samples
TLV70734DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQ	Samples
TLV70734DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AQ	Samples
TLV70734PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AP	Samples
TLV70734PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AP	Samples
TLV70736DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC	Samples
TLV70736DQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CC	Samples
TLV70736PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZO	Samples
TLV70736PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

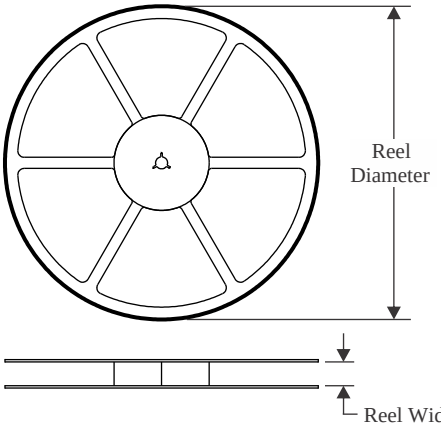
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

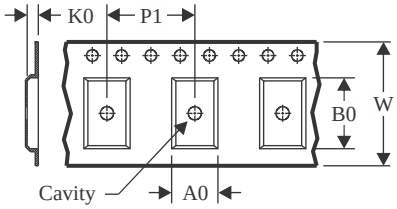
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

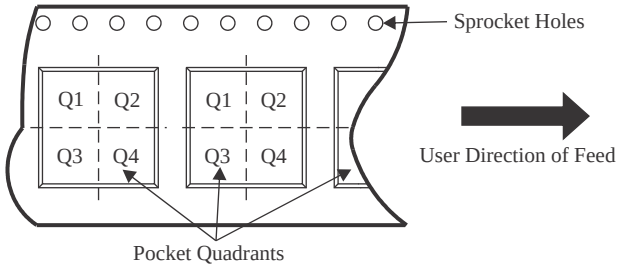


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

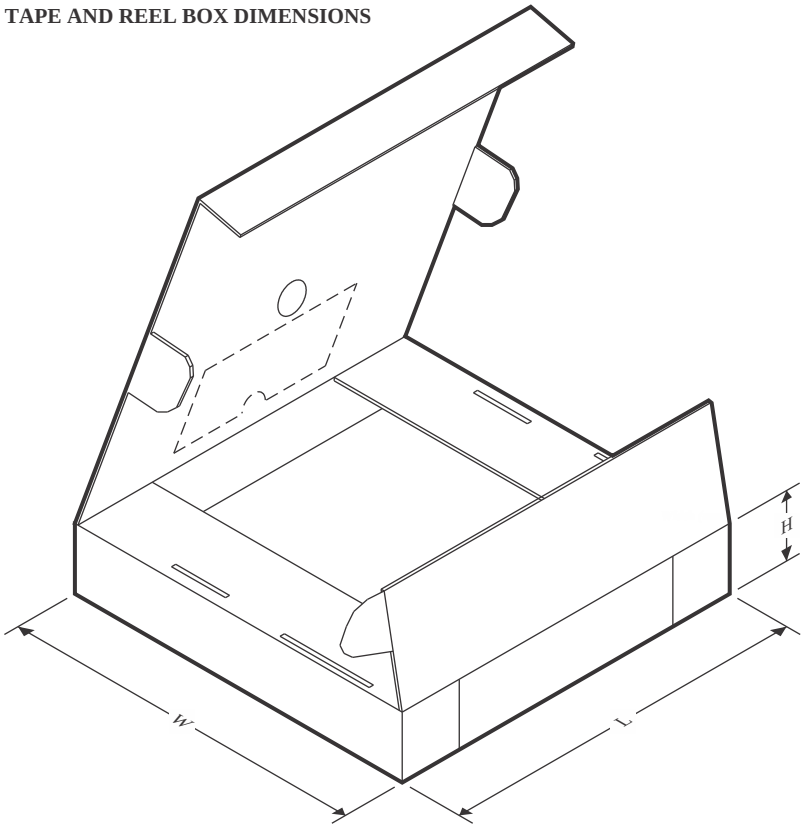
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV707085DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707085DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70710PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707115DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707115DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70711PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70711PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70712APDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70712PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70712PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707135DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707135DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70717DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70717DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185ADQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718ADQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718APDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70718PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70719PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70719PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70725PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70726PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70727PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70727PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV707285DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70728APDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70729PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730ADQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730APDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70731DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70731DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70732DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70732DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707335ADQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV707335DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV707335DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733ADQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733APDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733DQNR1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q1
TLV70733DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70733PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70734PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70736DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70736DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV70736DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV70736PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV707085DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707085DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70710DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70710DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70710DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70710PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70710PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70710PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707115DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707115DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV707115DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV707115DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70711PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70711PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70712APDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70712PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70712PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707135DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707135DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70715PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70715PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70715PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70715PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70717DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70717DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707185ADQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707185DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV707185DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707185DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707185PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707185PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70718ADQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70718APDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70718DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70718DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70718DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70718PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70718PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70719PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70719PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70725DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70725DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70725PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70725PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70726DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70726DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70726DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70726DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70726PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70726PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70726PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70726PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70727PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70727PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707285DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707285DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707285PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707285PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70728APDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70728PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70728PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70728PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70729DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70729DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70729PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70729PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70729PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70729PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70730ADQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70730APDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70730DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70730DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70730PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70730PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70730PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70731DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70731DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70732DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70732DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV707335ADQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV707335DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707335DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70733ADQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70733APDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70733DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70733DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733DQNR1	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70733DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70733PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70733PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70734DQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70734DQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70734PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70734PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV70736DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70736DQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV70736DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70736DQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV70736PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV70736PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

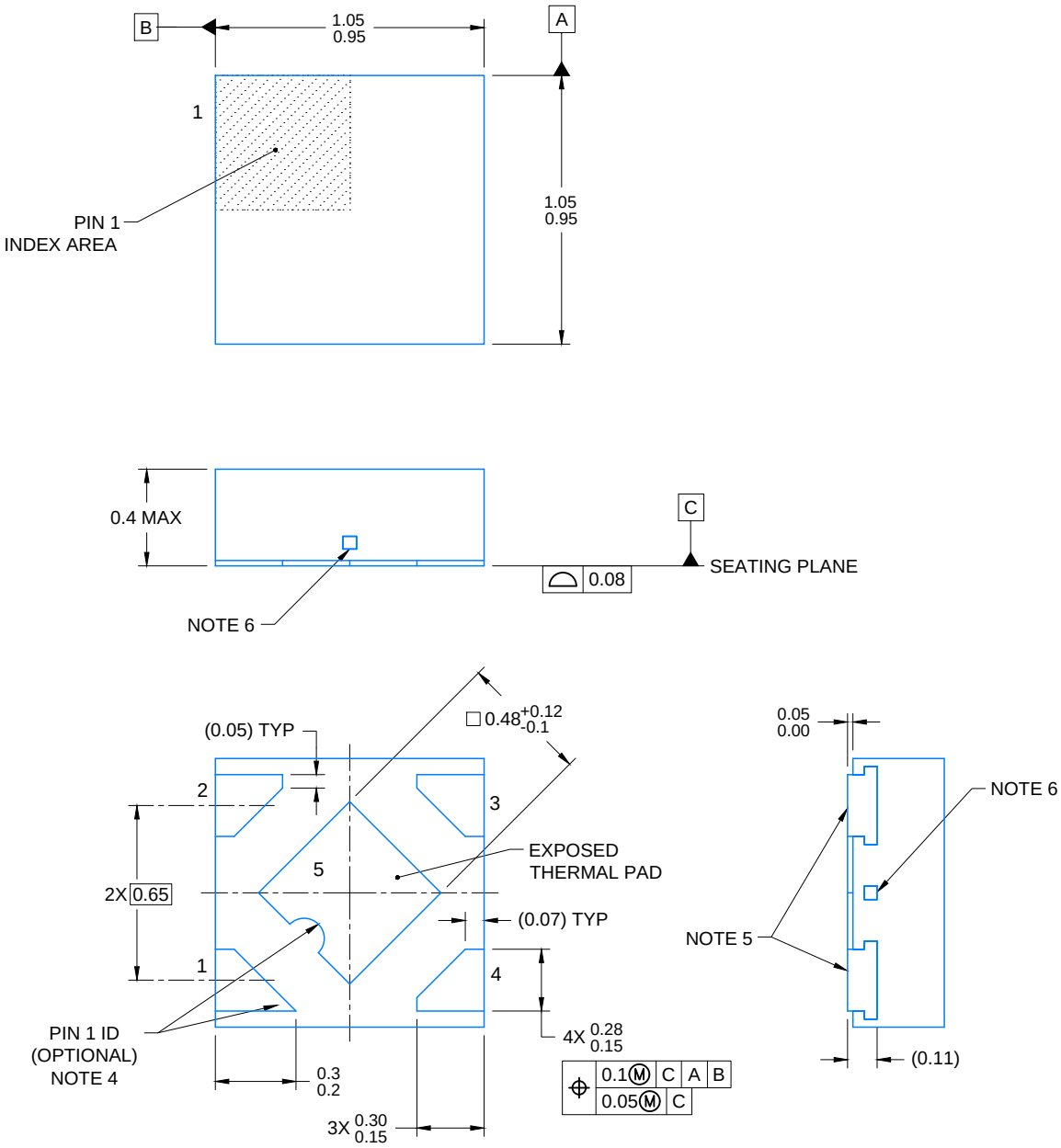
4210367/F

PACKAGE OUTLINE

DQN0004A

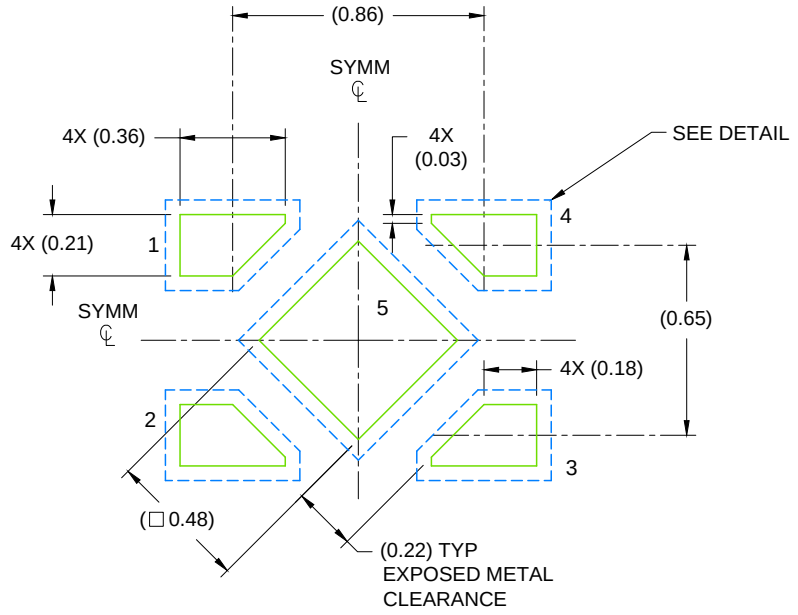
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



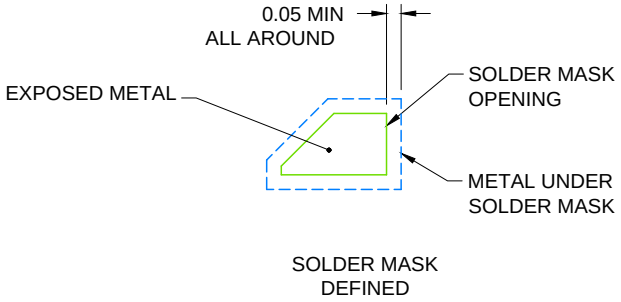
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X



SOLDER MASK DETAIL

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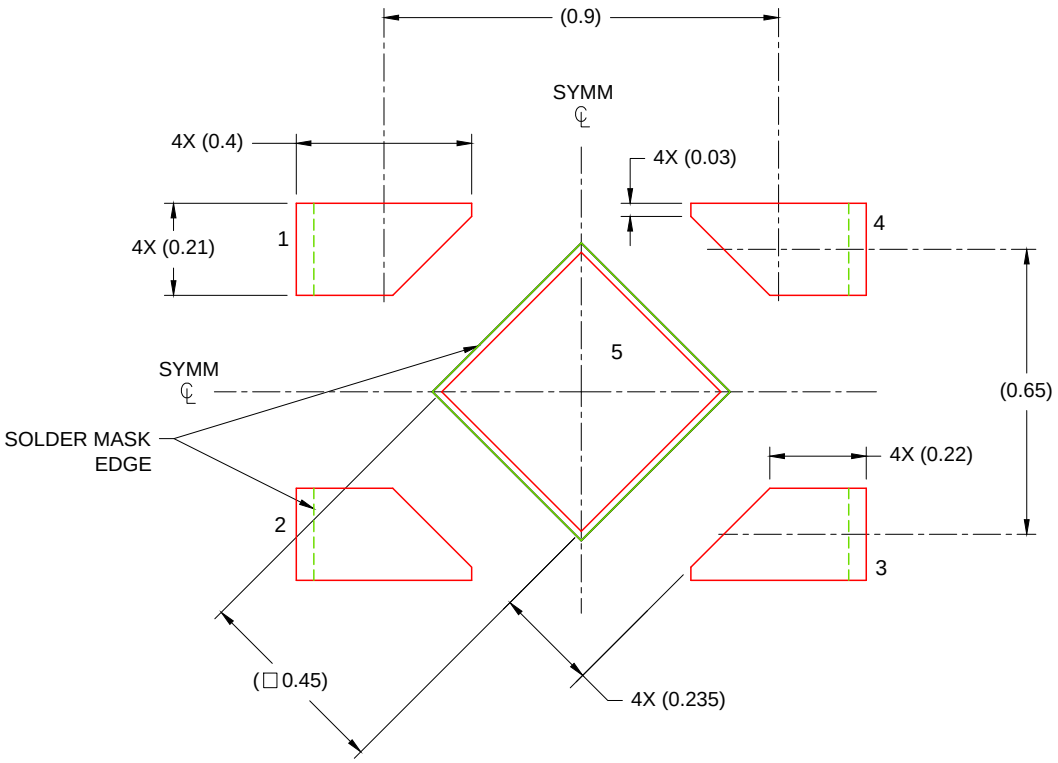
NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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