

TLV906xS コスト重視システム向け 10MHz、RRIO、CMOS オペアンプ

1 特長

- レール ツー レール入出力
- 低い入力オフセット電圧: $\pm 0.3\text{mV}$
- ユニティゲイン帯域幅: 10MHz
- 低い広帯域ノイズ: $10\text{nV}/\sqrt{\text{Hz}}$
- 低い入力バイアス電流: 0.5pA
- 低い静止電流: $538\mu\text{A}$
- ユニティゲイン安定
- 内部 RFI および EMI フィルタ
- 最低 1.8V の電源電圧で動作
- 抵抗性の開ループ出力インピーダンスにより、大きな容量性負荷でも簡単に安定
- シャットダウンバージョン: TLV906xS
- 拡張温度範囲: $-40^\circ\text{C} \sim 125^\circ\text{C}$

2 アプリケーション

- 電動アシスト自転車
- 煙感知器
- HVAC: 暖房、換気、空調
- モーター制御: AC 誘導モーター
- 冷蔵庫
- ウェアラブル機器
- ノート PC
- 洗濯機
- センサ シグナル コンディショニング
- パワー モジュール
- バーコード スキャナ
- アクティブ フィルタ
- ローサイド電流センシング

3 概要

TLV9061 (シングル)、TLV9062 (デュアル)、TLV9064 (クワッド) は、レール ツー レールの入力および出力スイング機能を備えたシングル / デュアル / クワッド低電圧 (1.8V ~ 5.5V) オペアンプです。

これらのデバイスは、低電圧での動作、小さな占有面積、大きな容量性負荷の駆動が必要なアプリケーション向けの、コスト効率の優れた選択肢です。

TLV906x の容量性負荷駆動能力は 100pF ですが、開ループ出力インピーダンスは抵抗性なので、大きい容量性の負荷でも簡単に安定できます。これらのオペアンプは低電圧 (1.8V ~ 5.5V) で動作し、OPAx316 および TLVx316 デバイスと同様の性能仕様を満たすよう、特別に設計されています。

TLV906xS デバイスにはシャットダウン モードが備わっており、標準消費電流 $1\mu\text{A}$ 未満で、アンプをスタンバイモードに切り替えることができます。

TLV906xS ファミリーはユニティゲイン安定で、RFI および EMI 除去フィルタが内蔵され、オーバードライブ状態で位相反転が発生しないため、システムの設計を簡素化するため役立ちます。

すべてのチャネル バリエーション (シングル、デュアル、クワッド) で、X2SON、X2QFN などのマイクロサイズ パッケージと、SOIC、MSOP、SOT-23、TSSOP などの業界標準パッケージが利用可能です。

製品情報

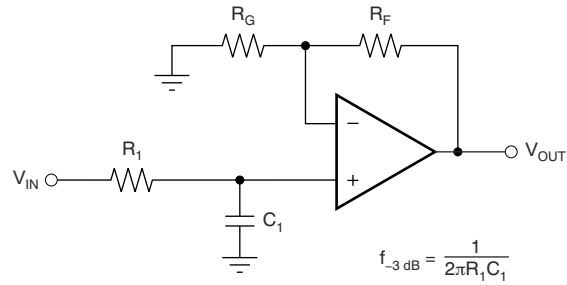
部品番号 ⁽³⁾	パッケージ ⁽¹⁾	本体サイズ (公称) ⁽⁴⁾
TLV9061	DBV (SOT-23, 5)	2.90mm × 1.60mm
	DCK (SC70, 5)	2.00mm × 1.25mm
	DRL (SOT-553, 5) ⁽²⁾	1.60mm × 1.20mm
	DPW (X2SON, 5)	0.80mm × 0.80mm
TLV9061S	DBV (SOT-23, 6)	2.90mm × 1.60mm
	DRY (USON, 6)	1.45mm × 1.00mm
TLV9062	D (SOIC, 8)	4.90mm × 3.90mm
	PW (TSSOP, 8)	3.00mm × 4.40mm
	DGK (VSSOP, 8)	3.00mm × 3.00mm
	DDF (SOT-23, 8)	2.90mm × 1.60mm
TLV9062S	DSG (WSO, 8)	2.00mm × 2.00mm
	DGS (VSSOP, 10)	3.00mm × 3.00mm
	RUG (X2QFN, 10)	2.00mm × 1.50mm
TLV9064	YCK (DSBGA, 9)	1.00 mm × 1.00mm
	D (SOIC, 14)	8.65mm × 3.90mm
TLV9064S	PW (TSSOP, 14)	5.00mm × 4.40mm
	RTE (WQFN, 16)	3.00mm × 3.00mm
	RUC (X2QFN, 14)	2.00mm × 2.00mm
TLV9064S	RTE (WQFN, 16)	3.00mm × 3.00mm

- (1) 供給されているすべてのパッケージについては、[セクション 10](#) を参照してください。
- (2) このパッケージはプレビューのみです。
- (3) [製品比較表](#)を参照してください。
- (4) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



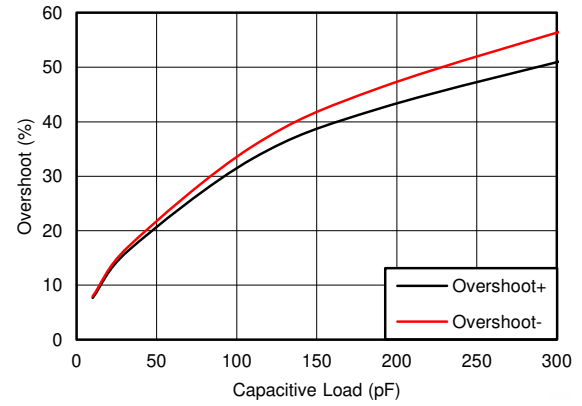
TLV9061, TLV9062, TLV9064

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$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

シングルポールのローパスフィルタ



小信号のオーバーシュートと負荷容量との関係

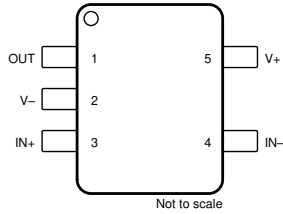
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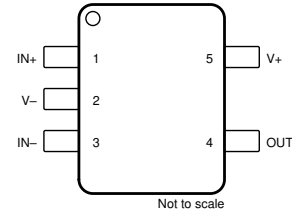
Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS														
		SOIC D	USON DRY	SOT-23 DBV	SC-70 DCK	VSSOP D GK	VSSOP D GS	DSBGA YCK	X2SON DPW	SOT-55 3 DRL	WSON DSG	TSSOP PW	SOT-23 DDF	WQFN RTE	X2QFN RUC	X2QFN RUG
TLV9061	1	8	—	5	5	—	—	—	5	5	—	—	—	—	—	—
TLV9061S		—	6	6	—	—	—	—	—	—	—	—	—	—	—	—
TLV9062	2	8	—	—	—	8	10	—	—	—	8	8	8	—	—	—
TLV9062S		—	—	—	—	—	10	9	—	—	—	—	—	—	—	10
TLV9064	4	14	—	—	—	—	—	—	—	—	—	14	—	16	14	—
TLV9064S		—	—	—	—	—	—	—	—	—	—	—	—	16	—	—

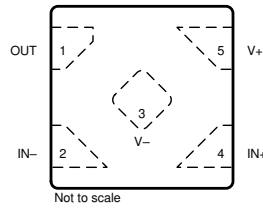
4 Pin Configuration and Functions



☒ 4-1. TLV9061 DBV or DRL Package, 5-Pin SOT-23 or SOT-553 (Top View)



☒ 4-2. TLV9061 DCK Package, 5-Pin SC70 (Top View)



☒ 4-3. TLV9061 DPW Package, 5-Pin X2SON (Top View)

表 4-1. Pin Functions: TLV9061

NAME	PIN			TYPE ⁽¹⁾	DESCRIPTION
	SOT-23, SOT-553	SC70	X2SON		
IN-	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V-	2	2	3	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply

(1) I = input, O = output

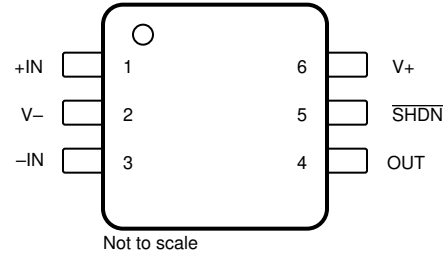
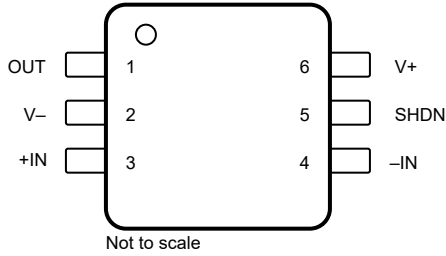


図 4-4. TLV9061S DBV Package, 6-Pin SOT-23 (Top View)

図 4-5. TLV9061S DRY Package, 6-Pin USON (Top View)

表 4-2. Pin Functions: TLV9061S

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	SOT-23	USON		
IN-	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
SHDN	5	5	I	Shutdown: low = amp disabled, high = amp enabled. See Shutdown Function section for more information.
V-	2	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	6	6	I	Positive (high) supply

(1) I = input, O = output

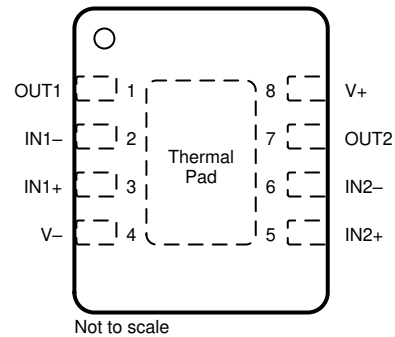
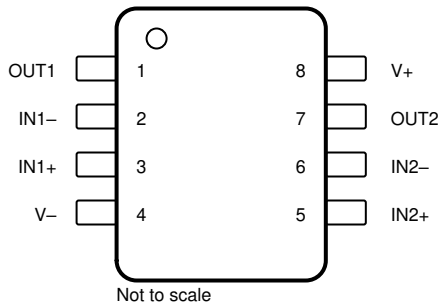


図 4-6. TLV9062 D, DGK, PW, or DDF Package, 8-Pin SOIC, VSSOP, TSSOP, or SOT-23 (Top View)

A. Connect thermal pad to V-

図 4-7. TLV9062 DSG Package, 8-Pin WSON With Exposed Thermal Pad (Top View)

表 4-3. Pin Functions: TLV9062

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	NO.			
IN1-	2		I	Inverting input, channel 1
IN1+	3		I	Noninverting input, channel 1
IN2-	6		I	Inverting input, channel 2
IN2+	5		I	Noninverting input, channel 2
OUT1	1		O	Output, channel 1
OUT2	7		O	Output, channel 2
V-	4		—	Negative (lowest) supply or ground (for single-supply operation)

表 4-3. Pin Functions: TLV9062 (続き)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V+	8	—	Positive (highest) supply

(1) I = input, O = output

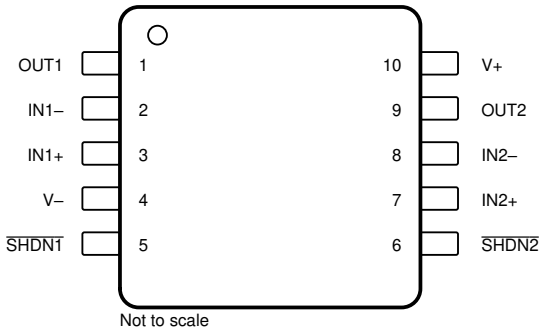


図 4-8. TLV9062S DGS Package, 10-Pin VSSOP (Top View)

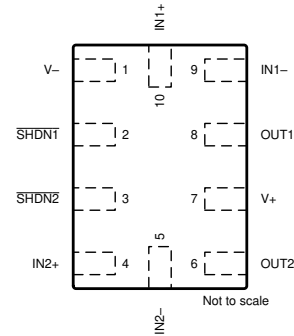


図 4-9. TLV9062S RUG Package, 10-Pin X2QFN (Top View)

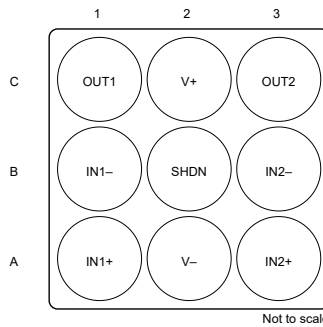


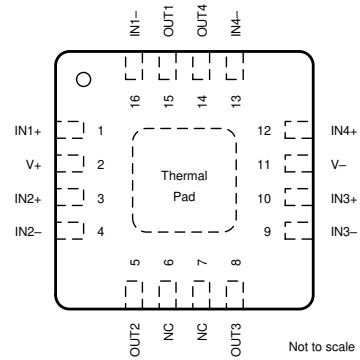
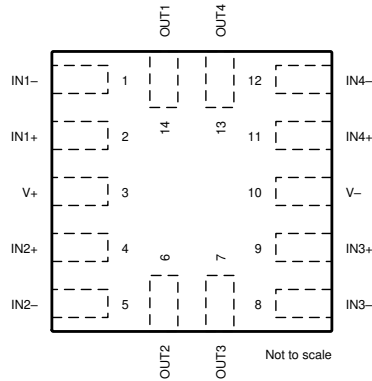
図 4-10. TLV9062S YCK Package 9-Pin DSBGA (WCSP) Bottom View

表 4-4. Pin Functions: TLV9062S

NAME	PIN			I/O	DESCRIPTION
	VSSOP	X2QFN	DSBGA (WCSP)		
IN1-	2	9	B1	I	Inverting input, channel 1
IN1+	3	10	A1	I	Noninverting input, channel 1
IN2-	8	5	B3	I	Inverting input, channel 2
IN2+	7	4	A3	I	Noninverting input, channel 2
OUT1	1	8	C1	O	Output, channel 1
OUT2	9	6	C3	O	Output, channel 2
SHDN1	5	2	—	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See Shutdown Function for more information.
SHDN2	6	3	—	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See Shutdown Function for more information.
SHDN	—	—	B2		Shutdown: low = both amplifiers disabled, high = both amplifiers enabled

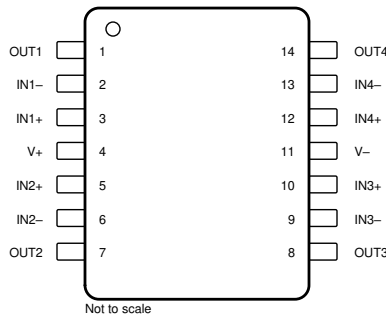
表 4-4. Pin Functions: TLV9062S (続き)

PIN				I/O	DESCRIPTION
NAME	VSSOP	X2QFN	DSBGA (WCSP)		
V-	4	1	A2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	10	7	C2	I	Positive (high) supply



4-11. TLV9064 RUC Package, 14-Pin X2QFN (Top View)

A. Connect thermal pad to V-
4-12. TLV9064 RTE Package, 16-Pin WQFN With Exposed Thermal Pad (Top View)

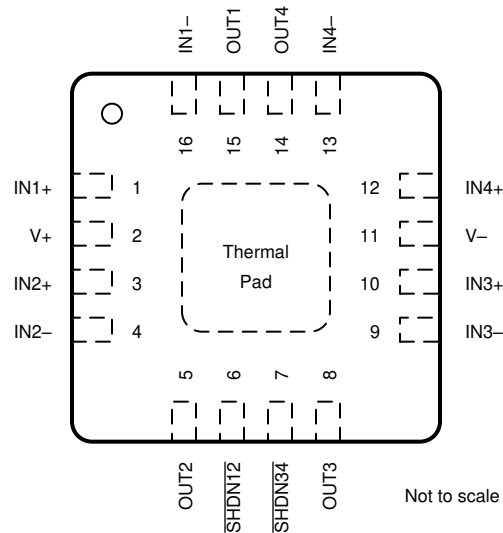


4-13. TLV9064 D or PW Package, 14-Pin SOIC or TSSOP (Top View)

表 4-5. Pin Functions: TLV9064

NAME	PIN			TYPE ⁽¹⁾	DESCRIPTION
	SOIC, TSSOP	WQFN	X2QFN		
IN1-	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2-	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2
IN3-	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4-	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V-	11	11	10	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	I	Positive (high) supply

(1) I = input, O = output



A. Connect thermal pad to V-

図 4-14. TLV9064S RTE Package, 16-Pin WQFN With Exposed Thermal Pad (Top View)

表 4-6. Pin Functions: TLV9064S

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IN1-	16	I	Inverting input, channel 1
IN1+	1	I	Noninverting input, channel 1
IN2-	4	I	Inverting input, channel 2
IN2+	3	I	Noninverting input, channel 2
IN3-	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4-	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
SHDN12	6	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information.
SHDN34	7	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information.
V-	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	2	I	Positive (high) supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Supply voltage [(V+) – (V–)]		0	6	V	
Signal input pins	Voltage ⁽²⁾	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential	(V+) – (V–) + 0.2		V
	Current ⁽²⁾	–10	10	mA	
Output short-circuit ⁽³⁾		Continuous		mA	
Temperature	Specified, T _A	–40	125	°C	
	Junction, T _J		150		
	Storage, T _{stg}	–65	150		

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

		VALUE	UNIT
TLV9061 PACKAGES			
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	
ALL OTHER PACKAGES			
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage (V _S = [V+] – [V–])	1.8	5.5	V
V _I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
V _O	Output voltage range	V–	V+	V
V _{SHDN_IH}	High level input voltage at shutdown pin (amplifier enabled)	1.1	V+	V
V _{SHDN_IL}	Low level input voltage at shutdown pin (amplifier disabled)	V–	0.2	V
T _A	Specified temperature	–40	125	°C

5.4 Thermal Information: TLV9061

THERMAL METRIC ⁽¹⁾		TLV9061			UNIT
		DBV (SOT-23)	DCK (SC70)	DPW (X2SON)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.7	263.3	467	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	144.7	75.5	211.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	51	332.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.1	1	29.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49	50.3	330.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	125	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.5 Thermal Information: TLV9061S

THERMAL METRIC ⁽¹⁾		TLV9061S		UNIT
		DBV (SOT-23)	DRY (USON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.5	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	155.1	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	96.2	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	80.3	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	95.9	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#).

5.6 Thermal Information: TLV9062

THERMAL METRIC ⁽¹⁾		TLV9062					UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	201.2	94.4	205.1	184.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	85.7	116.5	93.7	112.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	122.9	61.3	135.7	99.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	55.6	21.2	13	25.0	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.2	121.4	61.7	134.0	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	34.4	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.7 Thermal Information: TLV9062S

THERMAL METRIC ⁽¹⁾		TLV9002S			UNIT
		YCK (DSBGA)	RUG (X2QFN)	DGS (VSSOP)	
		9 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.8	197.2	170.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	93.3	84.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.5	123.8	113.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	3.7	16.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.1	120.2	112.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.8 Thermal Information: TLV9064

THERMAL METRIC ⁽¹⁾		TLV9064				UNIT
		PW (TSSOP)	D (SOIC)	RTE (WQFN)	RUC (X2QFN)	
		14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.8	106.9	65.1	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64	64	67.9	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79	63	40.4	150.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.7	25.9	5.5	3.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.4	62.7	40.2	149.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	23.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.9 Thermal Information: TLV9064S

THERMAL METRIC ⁽¹⁾		TLV9064S	UNIT
		RTE (WQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	23.8	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.10 Electrical Characteristics

For V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8V$ to $5.5V$ at $T_A = 25^\circ C$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$V_S = 5V$		± 0.3	± 1.6	mV
		$V_S = 5V, T_A = -40^\circ C$ to $125^\circ C$			± 2	
dV_{OS}/dT	Drift	$V_S = 5V, T_A = -40^\circ C$ to $125^\circ C$		± 0.53		$\mu V/^\circ C$
PSRR	Power-supply rejection ratio	$V_S = 1.8V - 5.5V, V_{CM} = (V-)$		± 7	± 80	$\mu V/V$
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	$V_S = 1.8V$ to $5.5V$	$(V-) - 0.1$		$(V+) + 0.1$	V
CMRR	Common-mode rejection ratio	$V_S = 5.5V, (V-) - 0.1V < V_{CM} < (V+) - 1.4V,$ $T_A = -40^\circ C$ to $125^\circ C$	80	103		dB
		$V_S = 5.5V, V_{CM} = -0.1V$ to $5.6V,$ $T_A = -40^\circ C$ to $125^\circ C$	57	87		
		$V_S = 1.8V, (V-) - 0.1V < V_{CM} < (V+) - 1.4V,$ $T_A = -40^\circ C$ to $125^\circ C$		88		
		$V_S = 1.8V, V_{CM} = -0.1V$ to $1.9V,$ $T_A = -40^\circ C$ to $125^\circ C$		81		
INPUT BIAS CURRENT						
I_B	Input bias current			± 0.5		pA
I_{OS}	Input offset current			± 0.05		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	$V_S = 5V, f = 0.1\text{ Hz}$ to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	$V_S = 5V, f = 10\text{ kHz}$		10		$nV/\sqrt{\text{Hz}}$
		$V_S = 5V, f = 1\text{ kHz}$		16		
i_n	Input current noise density	$f = 1\text{ kHz}$		23		$fA/\sqrt{\text{Hz}}$
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 1.8V, (V-) + 0.04V < V_O < (V+) - 0.04V,$ $R_L = 10\text{ k}\Omega$		100		dB
		$V_S = 5.5V, (V-) + 0.05V < V_O < (V+) - 0.05V,$ $R_L = 10\text{ k}\Omega$	104	130		
		$V_S = 1.8V, (V-) + 0.06V < V_O < (V+) - 0.06V,$ $R_L = 2\text{ k}\Omega$		100		
		$V_S = 5.5V, (V-) + 0.15V < V_O < (V+) - 0.15V,$ $R_L = 2\text{ k}\Omega$		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	$V_S = 5V, G = +1$		10		MHz
ϕ_m	Phase margin	$V_S = 5V, G = +1$		55		°
SR	Slew rate	$V_S = 5V, G = +1$		6.5		V/ μs
t_s	Settling time	To 0.1%, $V_S = 5V, 2V$ step, $G = +1, C_L = 100\text{ pF}$		0.5		μs
		To 0.01%, $V_S = 5V, 2V$ step, $G = +1, C_L = 100\text{ pF}$		1		
t_{OR}	Overload recovery time	$V_S = 5V, V_{IN} \times \text{gain} > V_S$		0.2		μs
THD + N	Total harmonic distortion + noise ⁽¹⁾	$V_S = 5.5V, V_{CM} = 2.5V, V_O = 1V_{RMS}, G = +1,$ $f = 1\text{ kHz}$		0.0008%		
OUTPUT						
V_O	Voltage output swing from supply rails	$V_S = 5.5V, R_L = 10\text{ k}\Omega$			20	mV
		$V_S = 5.5V, R_L = 2\text{ k}\Omega$			60	

5.10 Electrical Characteristics (続き)

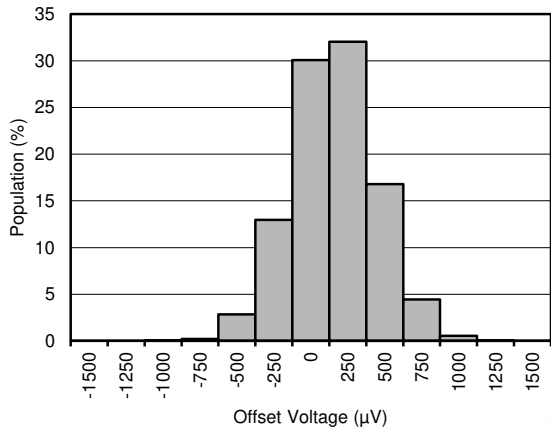
For V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8V$ to $5.5V$ at $T_A = 25^\circ C$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	$V_S = 5V$		± 50		mA
Z_O	Open-loop output impedance	$V_S = 5V$, $f = 10\text{MHz}$		100		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$V_S = 5.5V$, $I_O = 0\text{mA}$		538	750	μA
		$V_S = 5.5V$, $I_O = 0\text{mA}$, $T_A = -40^\circ C$ to $125^\circ C$			800	
SHUTDOWN						
I_{QSD}	Quiescent current per amplifier	$V_S = 1.8V$ to $5.5V$, all amplifiers disabled, $\overline{SHDN} = \text{Low}$		0.5	1.5	μA
Z_{SHDN}	Output impedance during shutdown	$V_S = 1.8V$ to $5.5V$, amplifier disabled		$10 \parallel 8$		$G\Omega \parallel pF$
$V_{SHDN_THR_HI}$	High level voltage shutdown threshold (amplifier enabled)	$V_S = 1.8V$ to $5.5V$		$(V-) + 0.9V$	$(V-) + 1.1V$	V
$V_{SHDN_THR_LO}$	Low level voltage shutdown threshold (amplifier disabled)	$V_S = 1.8V$ to $5.5V$		$(V-) + 0.2V$	$(V-) + 0.7V$	V
t_{ON}	Amplifier enable time (shutdown) (2)	$V_S = 1.8V$ to $5.5V$, full shutdown; $G = 1$, $V_{OUT} = 0.9 \times V_S / 2$, R_L connected to $V-$		10		μs
t_{OFF}	Amplifier disable time ⁽²⁾	$V_S = 1.8V$ to $5.5V$, $G = 1$, $V_{OUT} = 0.1 \times V_S / 2$, R_L connected to $V-$		0.6		μs
	\overline{SHDN} pin input bias current (per pin)	$V_S = 1.8V$ to $5.5V$, $V+ \geq \overline{SHDN} \geq (V+) - 0.8V$		130		pA
		$V_S = 1.8V$ to $5.5V$, $V- \leq \overline{SHDN} \leq V- + 0.8V$		40		

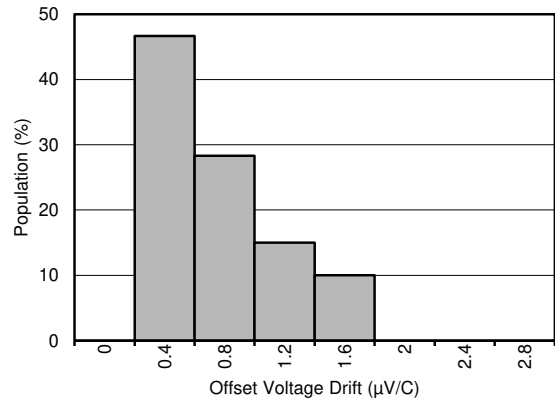
- Third-order filter; bandwidth = 80kHz at -3dB .
- Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the \overline{SHDN} pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

5.11 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

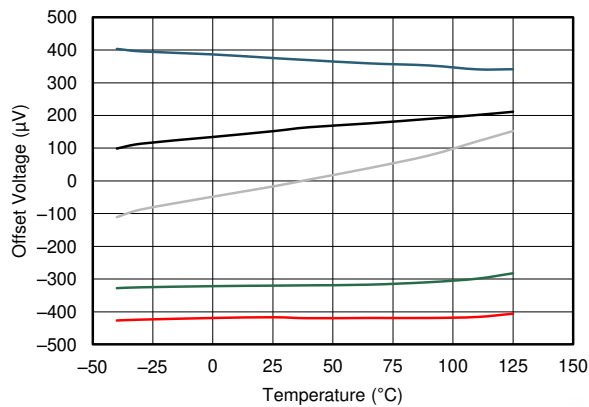


5-1. Offset Voltage Production Distribution

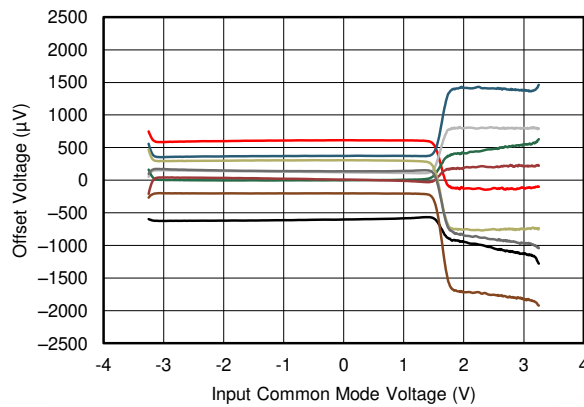


$T_A = -40^\circ\text{C}$ to 125°C

5-2. Offset Voltage Drift Distribution

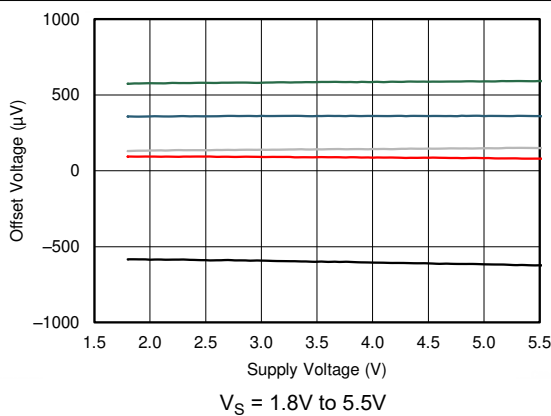


5-3. Offset Voltage vs Temperature



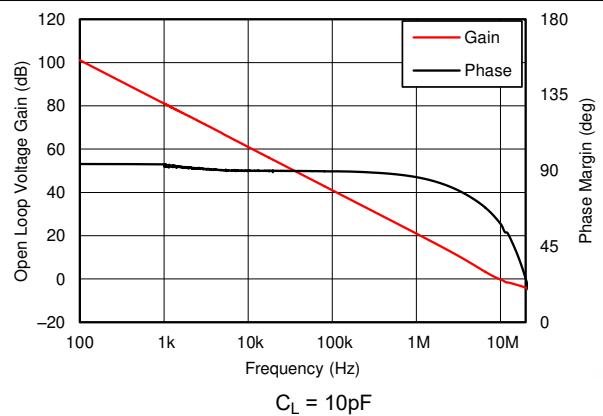
$V_+ = 2.75\text{V}$ $V_- = -2.75\text{V}$

5-4. Offset Voltage vs Common-Mode Voltage



$V_S = 1.8\text{V}$ to 5.5V

5-5. Offset Voltage vs Power Supply



$C_L = 10\text{pF}$

5-6. Open-Loop Gain and Phase vs Frequency

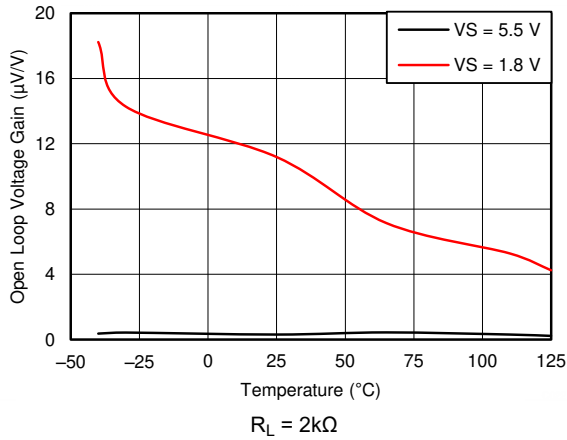


Figure 5-7. Open-Loop Gain vs Temperature

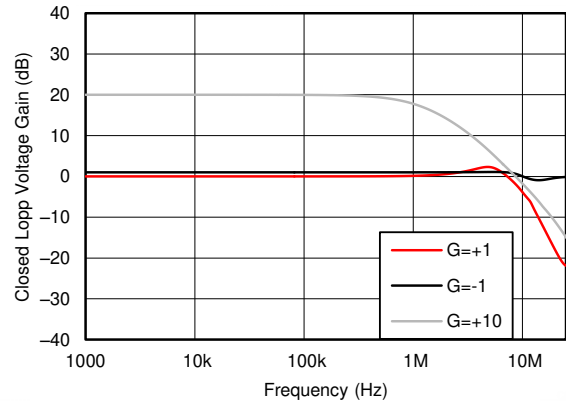


Figure 5-8. Closed-Loop Gain vs Frequency

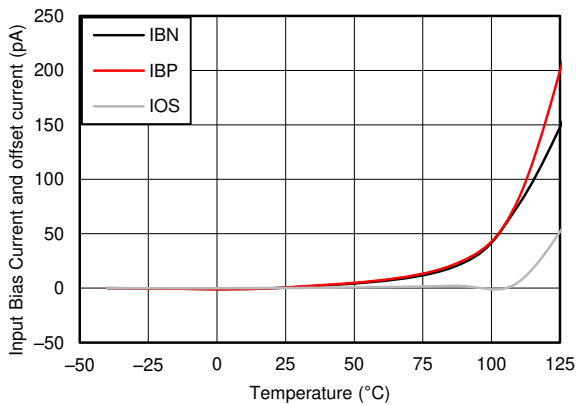


Figure 5-9. Input Bias Current vs Temperature

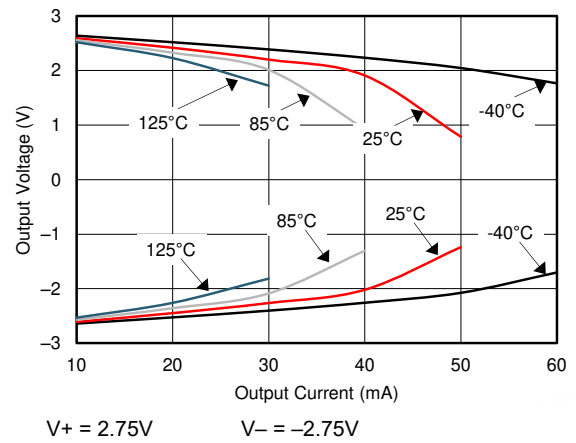


Figure 5-10. Output Voltage Swing vs Output Current

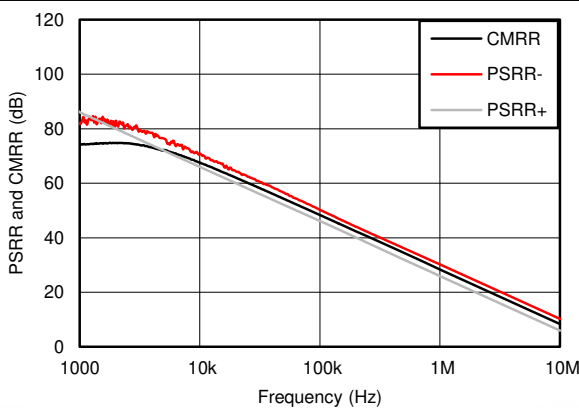


Figure 5-11. CMRR and PSRR vs Frequency (Referred to Input)

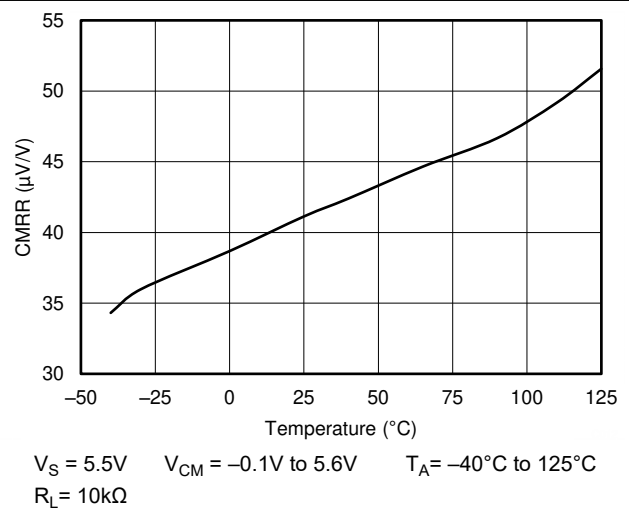
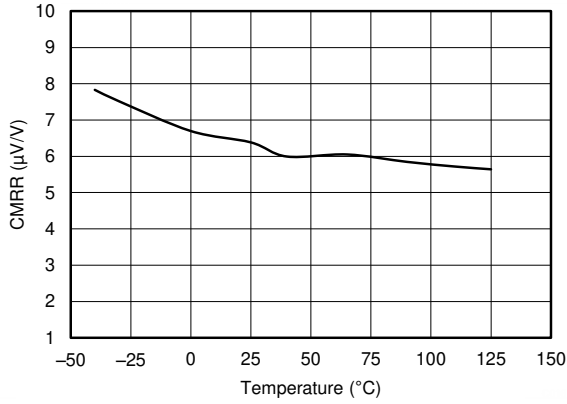
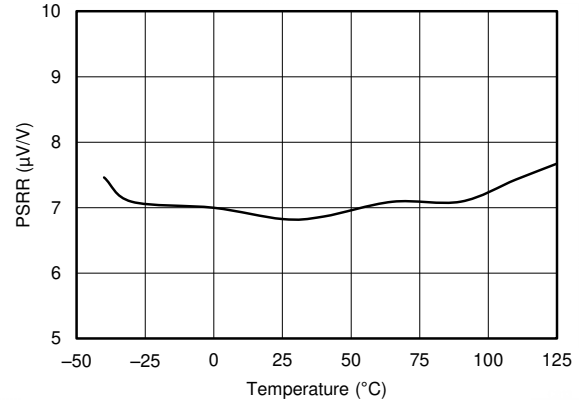


Figure 5-12. CMRR vs Temperature



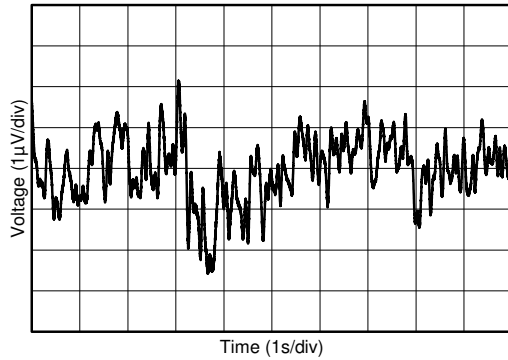
$V_{CM} = (V-) - 0.1V \text{ to } (V+) - 1.4V$
 $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ $R_L = 10k\Omega$ $V_S = 5.5V$

☒ 5-13. CMRR vs Temperature



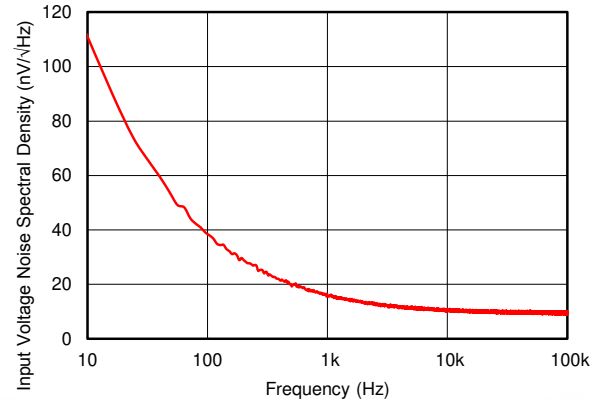
$V_S = 1.8V \text{ to } 5.5V$

☒ 5-14. PSRR vs Temperature

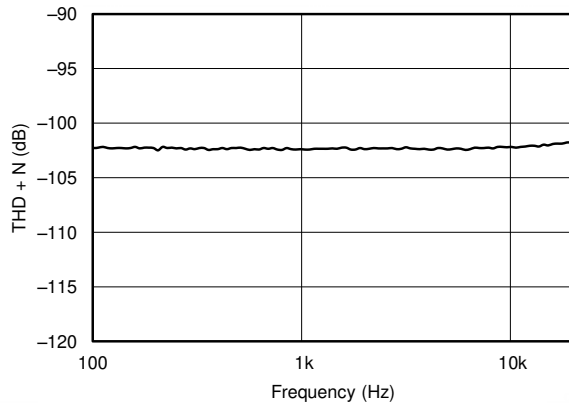


$V_S = 1.8V \text{ to } 5.5V$

☒ 5-15. 0.1Hz to 10Hz Input Voltage Noise

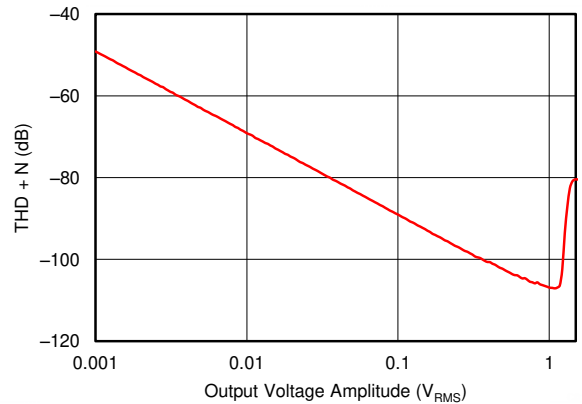


☒ 5-16. Input Voltage Noise Spectral Density vs Frequency



$V_S = 5.5V$ $V_{CM} = 2.5V$ $R_L = 2k\Omega$
 $V_{OUT} = 0.5V_{RMS}$ $BW = 80kHz$ $G = +1$

☒ 5-17. THD + N vs Frequency



$V_S = 5.5V$ $R_L = 2k\Omega$ $G = +1$
 $V_{CM} = 2.5V$ $BW = 80kHz$ $f = 1kHz$

☒ 5-18. THD + N vs Amplitude

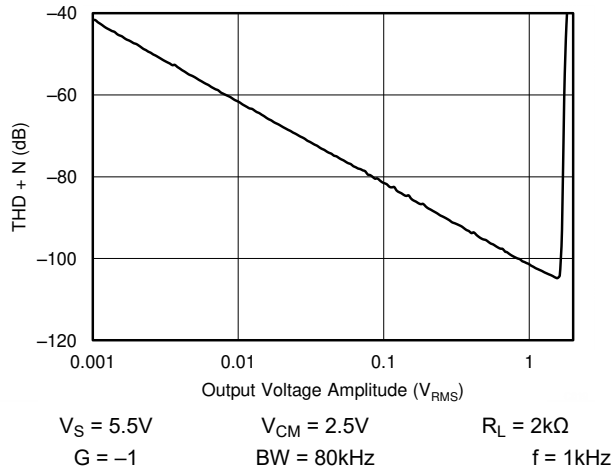


图 5-19. THD + N vs Amplitude

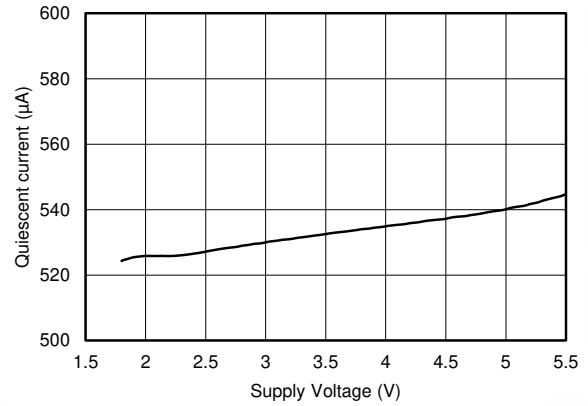


图 5-20. Quiescent Current vs Supply Voltage

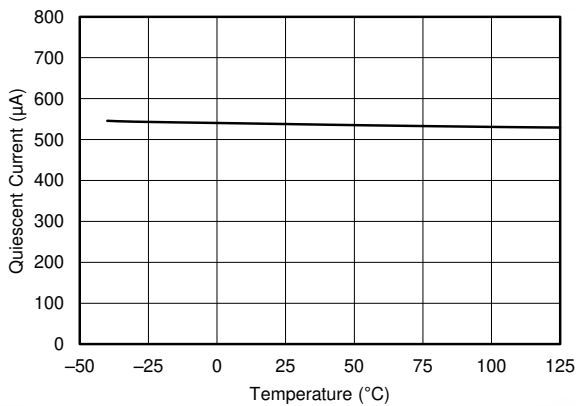


图 5-21. Quiescent Current vs Temperature

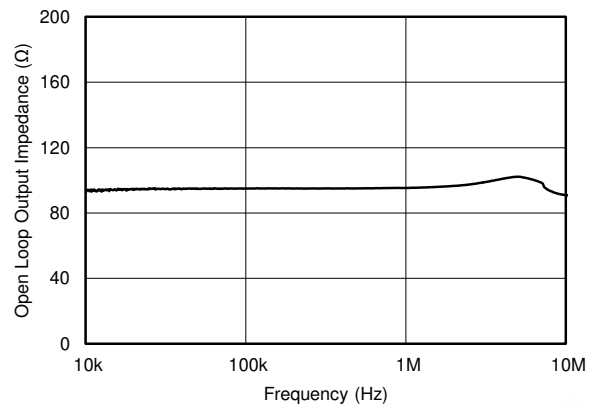


图 5-22. Open-Loop Output Impedance vs Frequency

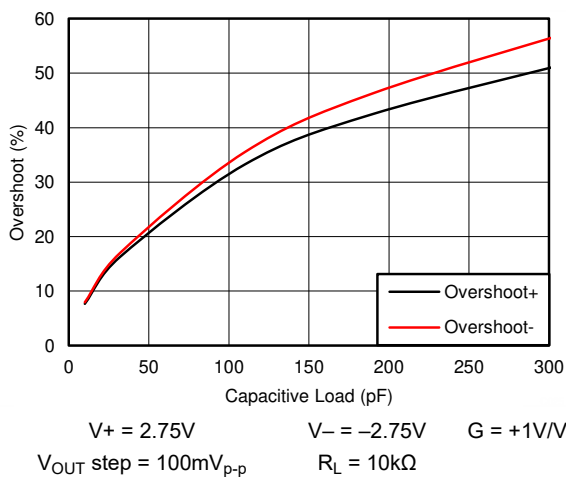


图 5-23. Small-Signal Overshoot vs Load Capacitance

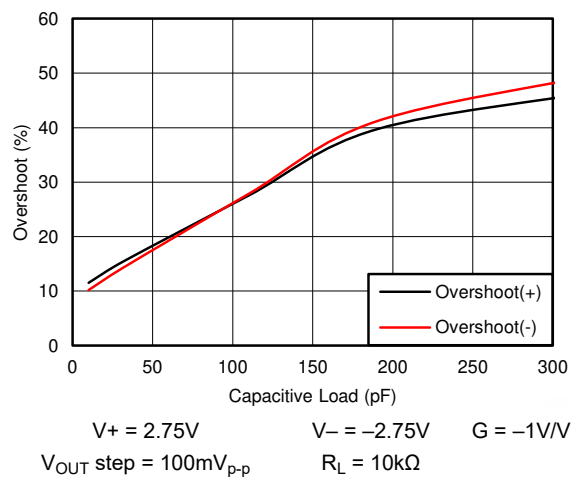
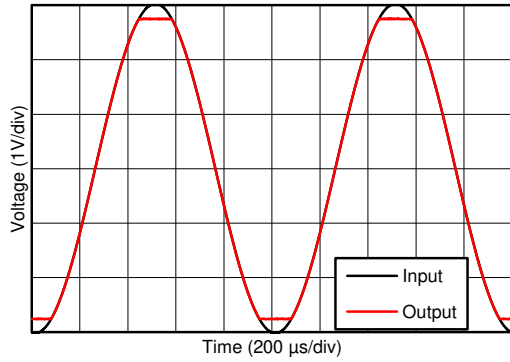
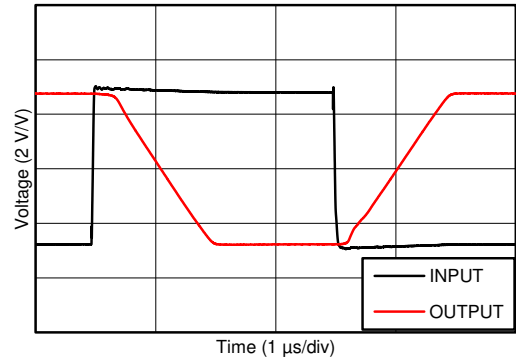


图 5-24. Small-Signal Overshoot vs Load Capacitance



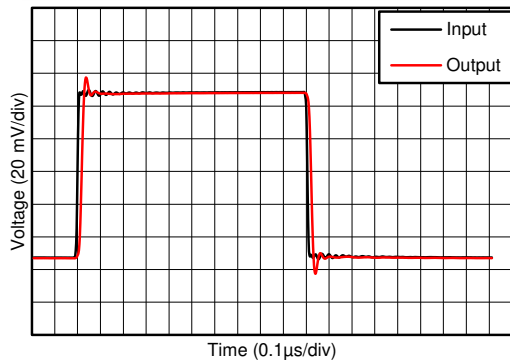
V+ = 2.75V V- = -2.75V

5-25. No Phase Reversal



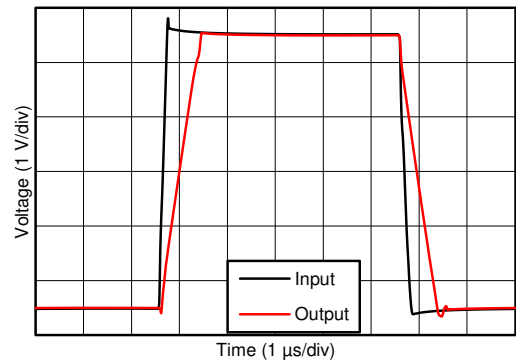
V+ = 2.75V V- = -2.75V G = -10V/V

5-26. Overload Recovery



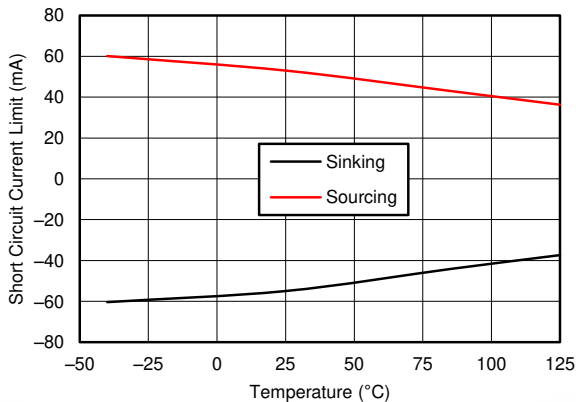
V+ = 2.75V V- = -2.75V G = 1V/V

5-27. Small-Signal Step Response

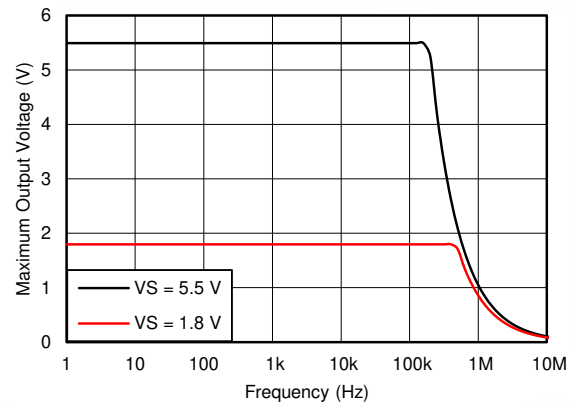


V+ = 2.75V V- = -2.75V C_L = 100pF
G = 1V/V

5-28. Large-Signal Step Response

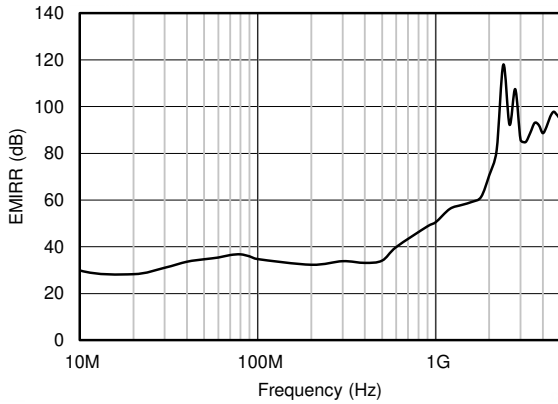


5-29. Short-Circuit Current vs Temperature



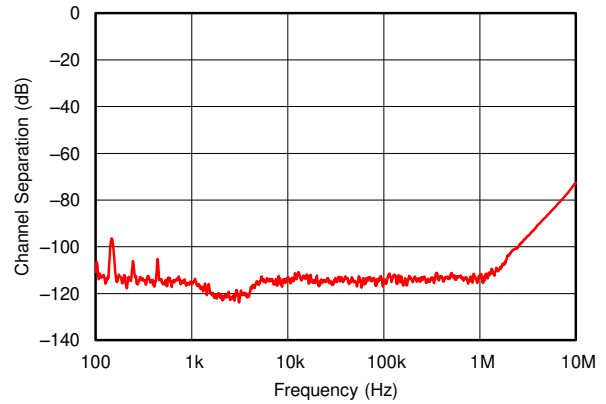
R_L = 10 kΩ C_L = 10pF

5-30. Maximum Output Voltage vs Frequency and Supply Voltage



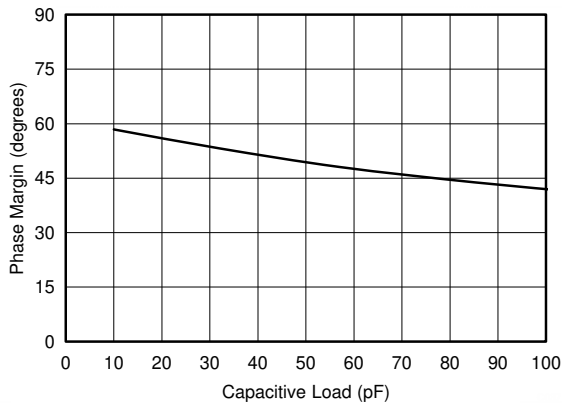
$P_{RF} = -10\text{dBm}$

5-31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



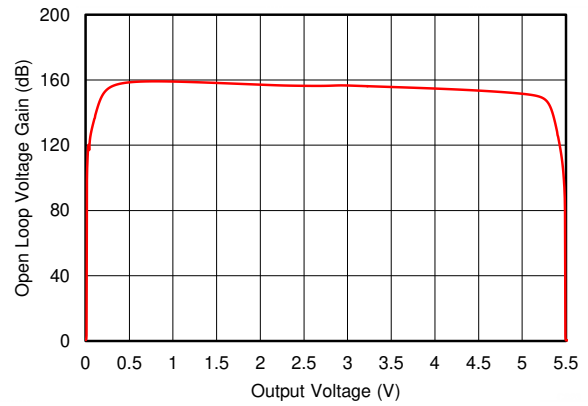
$V_+ = 2.75\text{V}$ $V_- = -2.75\text{V}$

5-32. Channel Separation vs Frequency



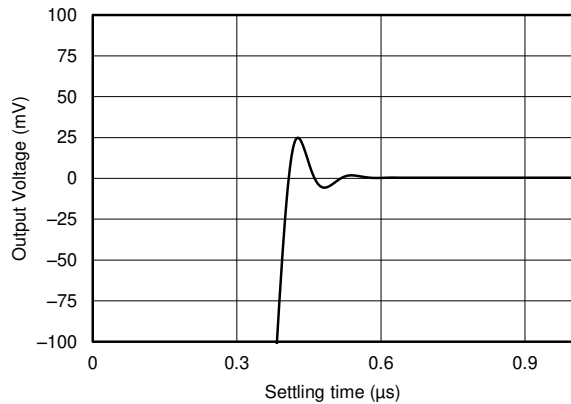
$V_S = 5.5\text{V}$

5-33. Phase Margin vs Capacitive Load

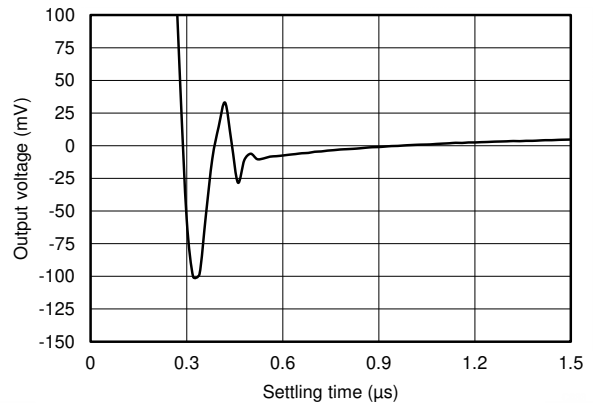


$V_S = 5.5\text{V}$

5-34. Open Loop Voltage Gain vs Output Voltage



5-35. Large Signal Settling Time (Positive)



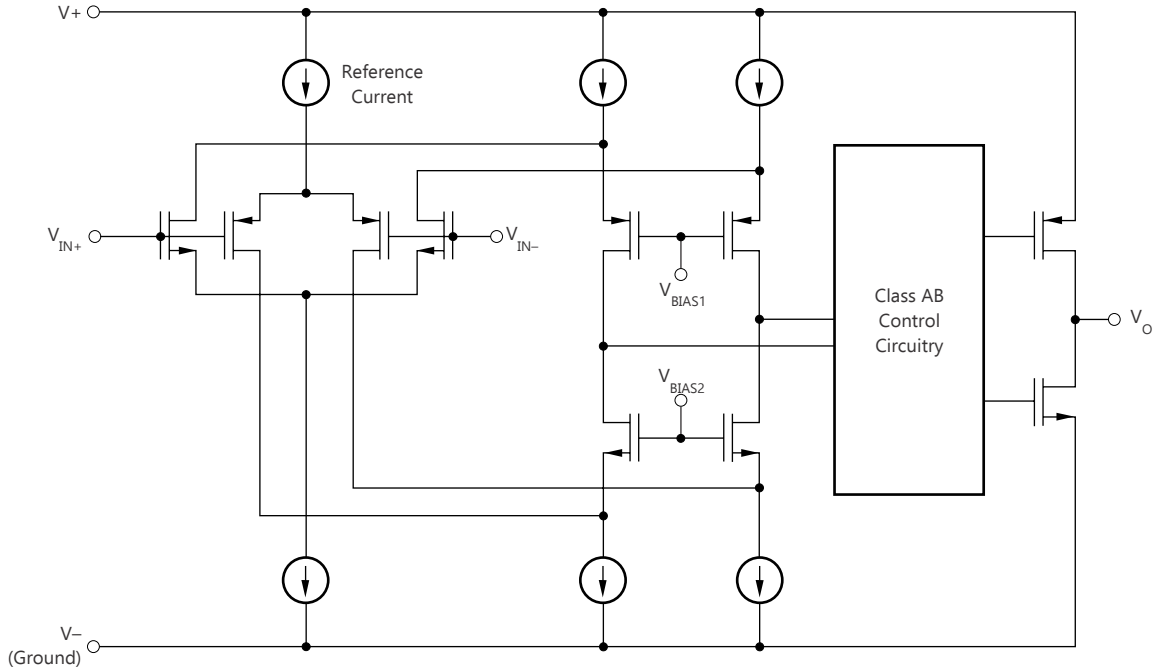
5-36. Large Signal Settling Time (Negative)

6 Detailed Description

6.1 Overview

The TLV906x devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-and-hold circuitry of analog-to-digital converters (ADCs).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x family extends 100mV beyond the supply rails for the full supply voltage range of 1.8V to 5.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4V$ to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately $(V+) - 1.4V$. There is a small transition region, typically $(V+) - 1.2V$ to $(V+) - 1V$, in which both pairs are on. This 200-mV transition region can vary up to 200mV with process variation. Thus, the transition region (with both stages on) can range from $(V+) - 1.4V$ to $(V+) - 1.2V$ on the low end, and up to $(V+) - 1V$ to $(V+) - 0.8V$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

6.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 15mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

6.3.3 EMI Rejection

The TLV906x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV906x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. [Figure 6-1](#) shows the results of this testing on the TLV906x. [Table 6-1](#) lists the EMIRR IN+ values for the TLV906x at particular frequencies commonly encountered in real-world applications. See [EMI Rejection Ratio of Operational Amplifiers application note](#) for more information.

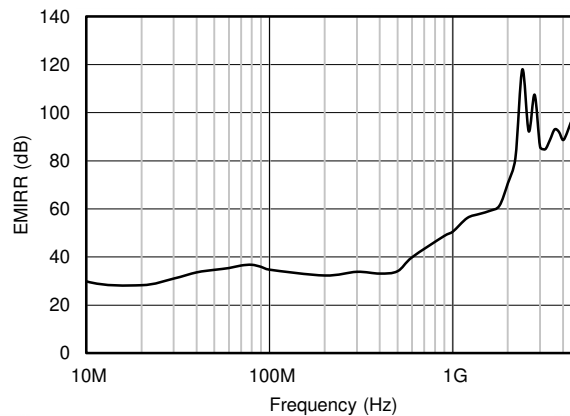


图 6-1. EMIRR Testing

表 6-1. TLV906x EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION or ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	68.9dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	77.8dB

表 6-1. TLV906x EMIRR IN+ For Frequencies of Interest (続き)

FREQUENCY	APPLICATION or ALLOCATION	EMIRR IN+
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	78.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	87.6dB

6.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x family is approximately 200ns.

6.3.5 Shutdown Function

The TLV906xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 1 μA . The $\overline{\text{SHDN}}$ pins are active-low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V_- and $V_- + 0.2\text{V}$. A valid logic high is defined as a voltage between $V_- + 1.2\text{V}$ and V_+ . The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit. There is **no** internal pull-up to enable the amplifier.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 μs for full shutdown of all channels; disable time is 6 μs . When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS to operate as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10k Ω load to midsupply ($V_S / 2$) is required. If using the TLV906xS without a load, the resulting turnoff time is significantly increased.

6.4 Device Functional Modes

The TLV906x family are operational when the power-supply voltage is between 1.8V ($\pm 0.9\text{V}$) and 5.5V ($\pm 2.75\text{V}$). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TLV906x family features 10MHz bandwidth and 6.5V/ μ s slew rate with only 538 μ A of supply current per channel, providing good AC-performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10nV/ $\sqrt{\text{Hz}}$ at 10kHz, low input bias current, and a typical input offset voltage of 0.3mV.

7.2 Typical Applications

7.2.1 Typical Low-Side Current Sense Application

図 7-1 shows the TLV906x configured in a low-side current-sensing application.

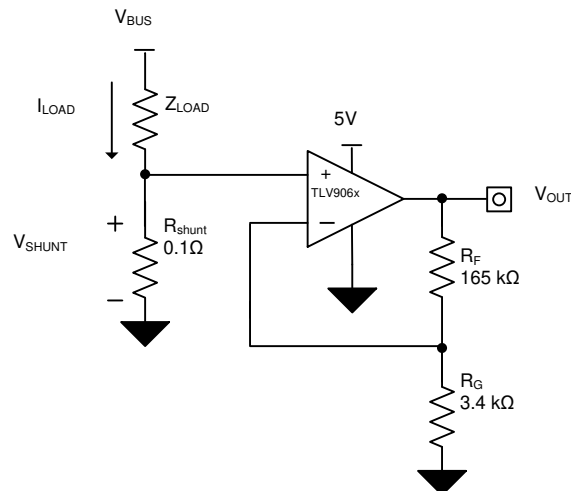


図 7-1. TLV906x in a Low-Side, Current-Sensing Application

7.2.2 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.95V
- Maximum shunt voltage: 100mV

7.2.3 Detailed Design Procedure

The transfer function of the circuit in [図 7-1](#) is given in [式 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times GAIN \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using [式 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using [式 2](#), R_{SHUNT} equals 100m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV906x to produce an output voltage of approximately 0V to 4.95V. [式 3](#) calculates the gain required for the TLV906x to produce the required output voltage.

$$Gain = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using [式 3](#), the required gain equals 49.5V/V, which is set with the R_F and R_G resistors. [式 4](#) sizes the R_F and R_G resistors to set the gain of the TLV906x to 49.5V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F to equal 165k Ω and R_G to equal 3.4k Ω provides a combination that equals approximately 49.5V/V. [図 7-2](#) shows the measured transfer function of the circuit shown in [図 7-1](#). Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

7.2.4 Application Curve

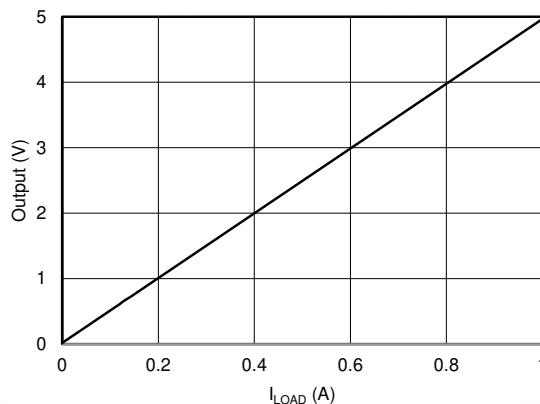


図 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV906x series is specified for operation from 1.8V to 5.5V ($\pm 0.9\text{V}$ to $\pm 2.75\text{V}$); many specifications apply from -40°C to 125°C . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages larger than 6V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1 μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

7.3.1 Input and ESD Protection

The TLV906x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA, as shown in the [Absolute Maximum Ratings](#) table. [Figure 7-3](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

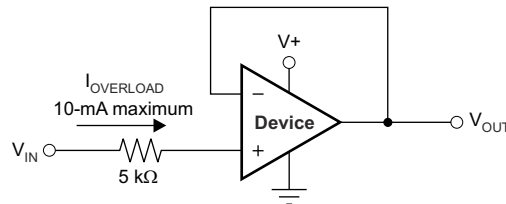


図 7-3. Input Current Protection

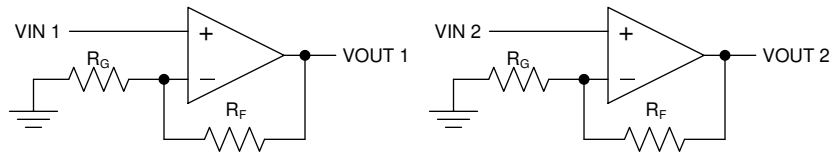
7.4 Layout

7.4.1 Layout Guidelines

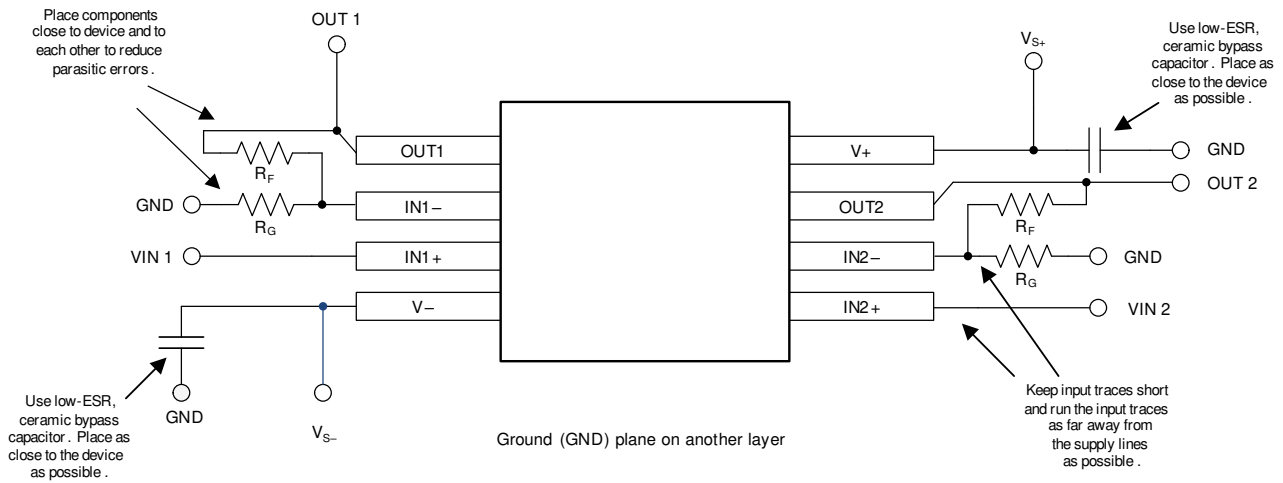
For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 7-5](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example



7-4. Schematic Representation for the Layout Example



7-5. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Circuit Board Layout Techniques](#)
- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers application note](#)
- Texas Instruments, [QFN/SON PCB Attachment application note](#)
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages application note](#)
- Texas Instruments, [Single-Ended Input to Differential Output Conversion Circuit design guide](#)
- Texas Instruments, [TLVx313 Low-Power, Rail-to-Rail In/Out, 500- \$\mu\$ V Typical Offset, 1MHz Operational Amplifier for Cost-Sensitive Systems data sheet](#)
- Texas Instruments, [TLVx314 3MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier data sheet](#)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision L (September 2024) to Revision M (December 2024)	Page
• Changed TLV9061S DBV (SOT-23) pinout drawing to match the <i>Pin Functions</i> table.....	4

Changes from Revision K (July 2024) to Revision L (September 2024) **Page**

- 「製品情報」表で TLV9062S (YCK、DSBGA) パッケージのプレビュー版の注を削除 1
-

Changes from Revision J (September 2019) to Revision K (July 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... 1
 - 「製品情報」の表を更新..... 1
 - 「製品情報」表で TLV9062S (YCK、DSBGA) パッケージのプレビュー版の注を追加..... 1
 - Added YCK packages to the *Device Comparison* table..... 3
 - Added TLV9062S YCK (DSBGA) pinout drawing to *Pin Configuration and Functions* section..... 4
-

Changes from Revision I (May 2019) to Revision J (September 2019) **Page**

- データシート全体にわたって TLV9062IDDFR (SOT-23, 8) パッケージのプレビュー版の注を削除..... 1
 - Added industry standard package names to *Device Comparison Table* 3
 - Added note to packages with thermal pads, specifying that the thermal pads need to be connected to V-..... 4
 - Added link to *Shutdown Function* section in $\overline{\text{SHDN}}$ pin function rows..... 4
 - Added *EMI Rejection* section to the *Feature Description* section..... 22
 - Changed *Shutdown Function* section to add more clarification 23
-

Changes from Revision H (April 2019) to Revision I (May 2019) **Page**

- Added DDF (SOT-23) thermal information to replace TBDs..... 11
-

Changes from Revision G (December 2018) to Revision H (April 2019) **Page**

- 「製品情報」に (SOT-23, 8) の情報を追加..... 1
 - Added DDF package column to *Device Comparison Table* 3
 - Added DDF (SOT-23) package, to *Pin Functions* 4
 - Added DDF (SOT-23) package to *Thermal Information* 11
-

Changes from Revision F (September 2018) to Revision G (December 2018) **Page**

- 「製品情報」表で TLV9064 RUC パッケージの名前を(WQFN、14) から(X2QFN、14) に変更..... 1
 - Added RUC (X2QFN) package, pinout information to *Pin Functions: TLV9064 table*..... 4
 - Added TLV9064 RUC (X2QFN) pinout drawing to *Pin Configuration and Functions* section..... 4
 - Added RUC (X2QFN) to *Thermal Information: TLV9064 table*..... 12
-

Changes from Revision E (July 2018) to Revision F (September 2018) **Page**

- データシートのヘッダーからシャットダウン型番を削除..... 1
 - 「製品情報」表から TLV9062 の (X2QFN、10) パッケージを削除..... 1
 - 「概要」セクションにシャットダウン型番の参照を追加..... 1
 - データシート全体にわたって TLV906xS シリーズを TLV906xS ファミリーに変更..... 1
 - Added Shutdown devices to *Device Comparison Table* 3
 - Changed pin namings for all pinout drawings to reflect updated nomenclature 4
 - Added TLV9061S *Thermal Information Table*..... 11
 - Added TLV9064S *Thermal Information Table*..... 12
-

• Deleted Partial Shutdown Amplifier Enable Time.....	13
• Added clarification on selecting resistors for a current sensing application in the Typical Applications Section	25
• Changed wording of third bullet in Layout Guidelines.....	27

Changes from Revision D (June 2018) to Revision E (July 2018)	Page
• 「製品情報」表に TLV9061S デバイスを追加.....	1
• 「製品情報」表に TLV9064S デバイスを追加.....	1
• Added RUC and RUG packages to the <i>Device Comparison</i> table.....	3
• Added TLV9061S DBV (SOT-23) pinout drawing to <i>Pin Configuration and Functions</i> section.....	4
• Added TLV9061S DBV (SOT-23) package, pinout information to <i>Pin Functions: TLV9061S</i> table.....	4
• Added TLV9062S RUG (VSSOP) package, pinout drawing to <i>Pin Configuration and Functions</i> section.....	4
• Added TLV9064 RTE pinout information to <i>Pin Functions: TLV9064</i> table.....	4
• Added TLV9064S RTE (WQFN) pinout drawing to <i>Pin Configuration and Functions</i> section	4
• Added TLV9062S RUG (VSSOP) package, pinout information to <i>Pin Functions: TLV9062S</i> table.....	4
• Added TLV9064 RTE (WQFN) pinout drawing to <i>Pin Configuration and Functions</i> section	4

Changes from Revision C (March 2018) to Revision D (June 2018)	Page
• ドキュメントのタイトルの「TLV906x」にシャットダウン接尾辞を追加.....	1
• 「特長」の箇条書き一覧に「シャットダウン バージョン」項目を追加	1
• 「製品情報」表に TLV9062S デバイスを追加.....	1
• 「概要 (続き)」セクションにシャットダウンのテキストを追加.....	1
• Added " $V_S = [V+] - [V-]$ " supply voltage parameter in <i>Absolute Maximum Ratings</i> table.....	10
• Added "input voltage range" and "output voltage range" parameters and values to <i>Recommended Operating Conditions</i> table.....	10
• Added shutdown pin recommended operating conditions in <i>Recommended Operating Conditions</i> table.....	10
• Added " T_A " symbol to "specified temperature" parameter to <i>Recommended Operating Conditions</i> table	10
• Added <i>Thermal Information: TLV9062S</i> thermal table data.....	12
• Added shutdown section to <i>Electrical Characteristics: V_S (Total Supply Voltage) = (V+) - (V-) = 1.8V to 5.5V</i> table.....	13
• Added <i>Shutdown Function</i> section	23

Changes from Revision B (October 2017) to Revision C (March 2018)	Page
• デバイスのステータスを「量産データ / 混在ステータス」から「量産データ」に変更.....	1
• 「製品情報」表で TLV9061 (DPW, X2SON) パッケージのプレビュー版の注を削除.....	1
• Deleted package, preview note from TLV9061 DPW (X2SON) package, pinout drawing	4
• Changed formatting of <i>ESD Ratings</i> table to show different results for all packages	10
• Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table	11
• Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table	11

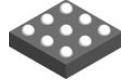
Changes from Revision A (June 2017) to Revision B (October 2017)	Page
• Added 8-pin PW package, to <i>Pin Configuration and Functions</i> section	4
• Added DSG (WSON) package to <i>Thermal Information</i> table.....	11
• Added PW (TSSOP) to TLV9062 <i>Thermal Information</i> table	11
• Changed maximum input offset voltage value from $\pm 1.6\text{mV}$ to 2mV	13
• Changed maximum input offset voltage value from ± 1.5 to $\pm 1.6\text{mV}$	13

• Changed minimum common-mode rejection ratio input voltage range from 86dB to 80dB	13
• Changed typical input current noise density value from 10 to $23\text{fA}/\sqrt{\text{Hz}}$	13
• Changed THD + N test conditions from $V_S = 5\text{V}$ to $V_S = 5.5\text{V}$	13
• Added $V_{\text{CM}} = 2.5\text{V}$ test condition to THD + N parameter in <i>Electrical Characteristics</i> table	13
• Added maximum output voltage swing value from 25mV to 60mV.....	13
• Changed maximum output voltage swing value from 15mV to 20mV	13

Changes from Revision * (March 2017) to Revision A (June 2017)	Page
• デバイス ステータスを「事前情報」から「量産データ」に変更.....	1

10 Mechanical, Packaging, and Orderable Information

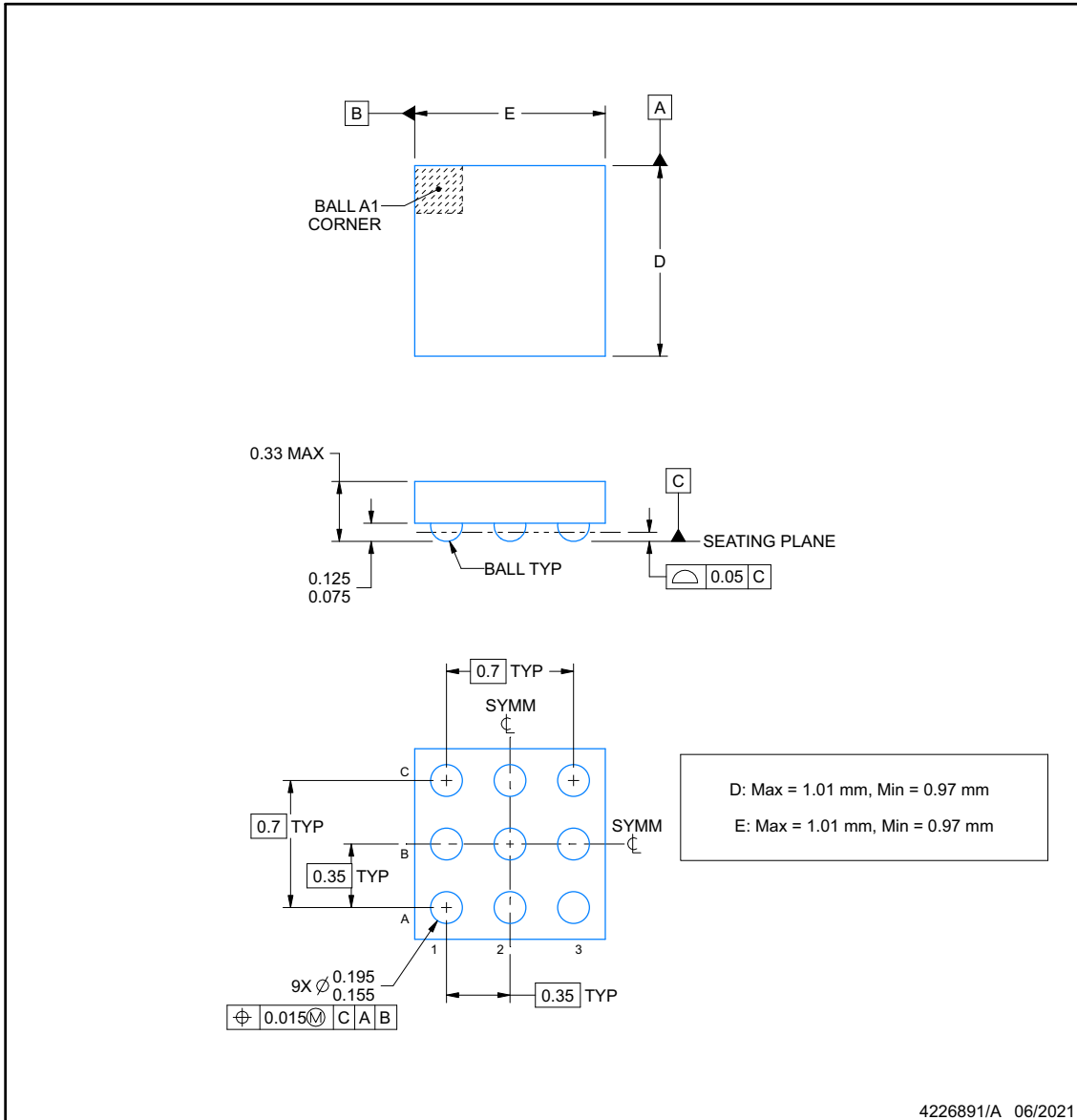
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.



YCK0009-C01

PACKAGE OUTLINE
DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

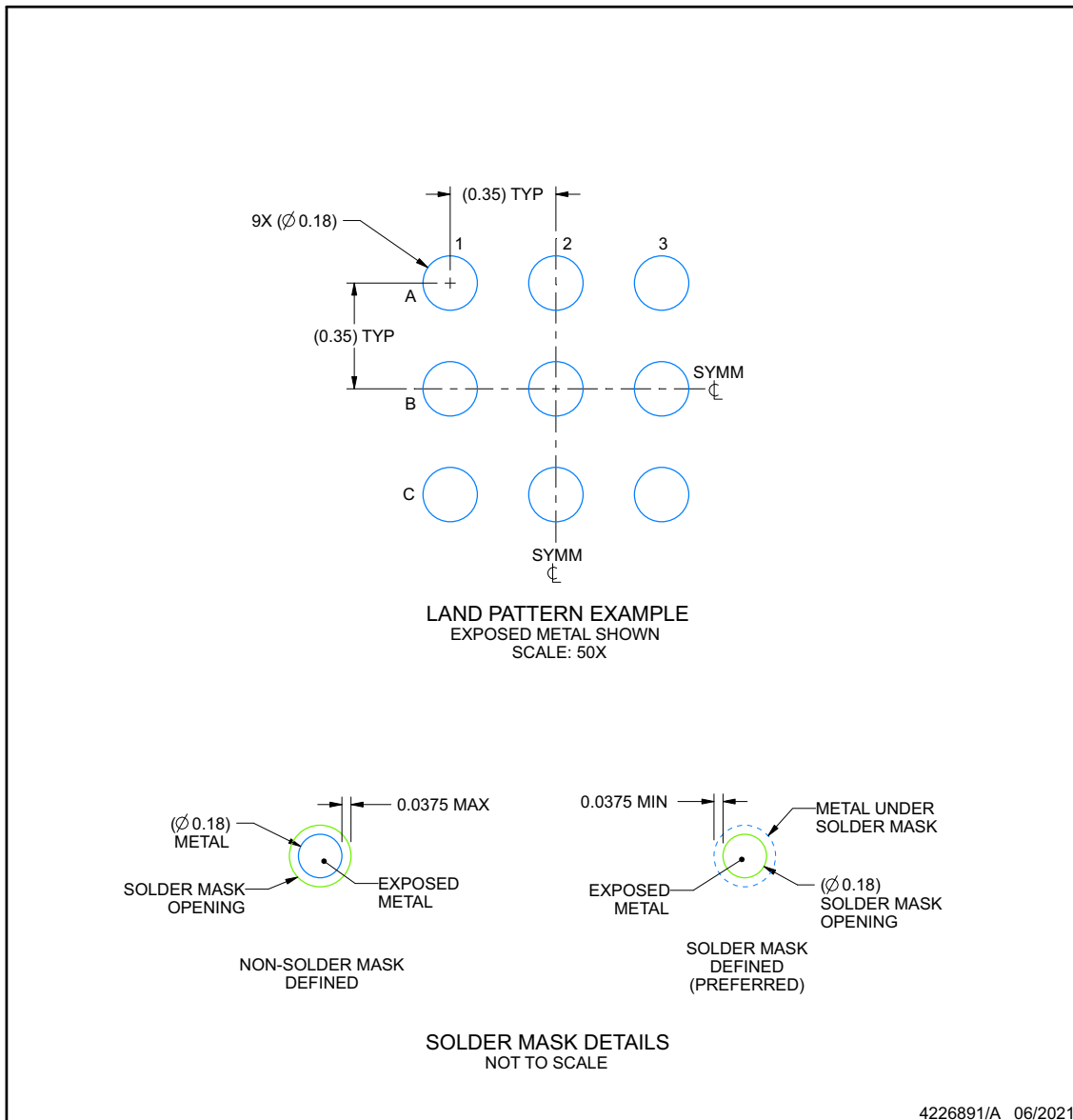
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

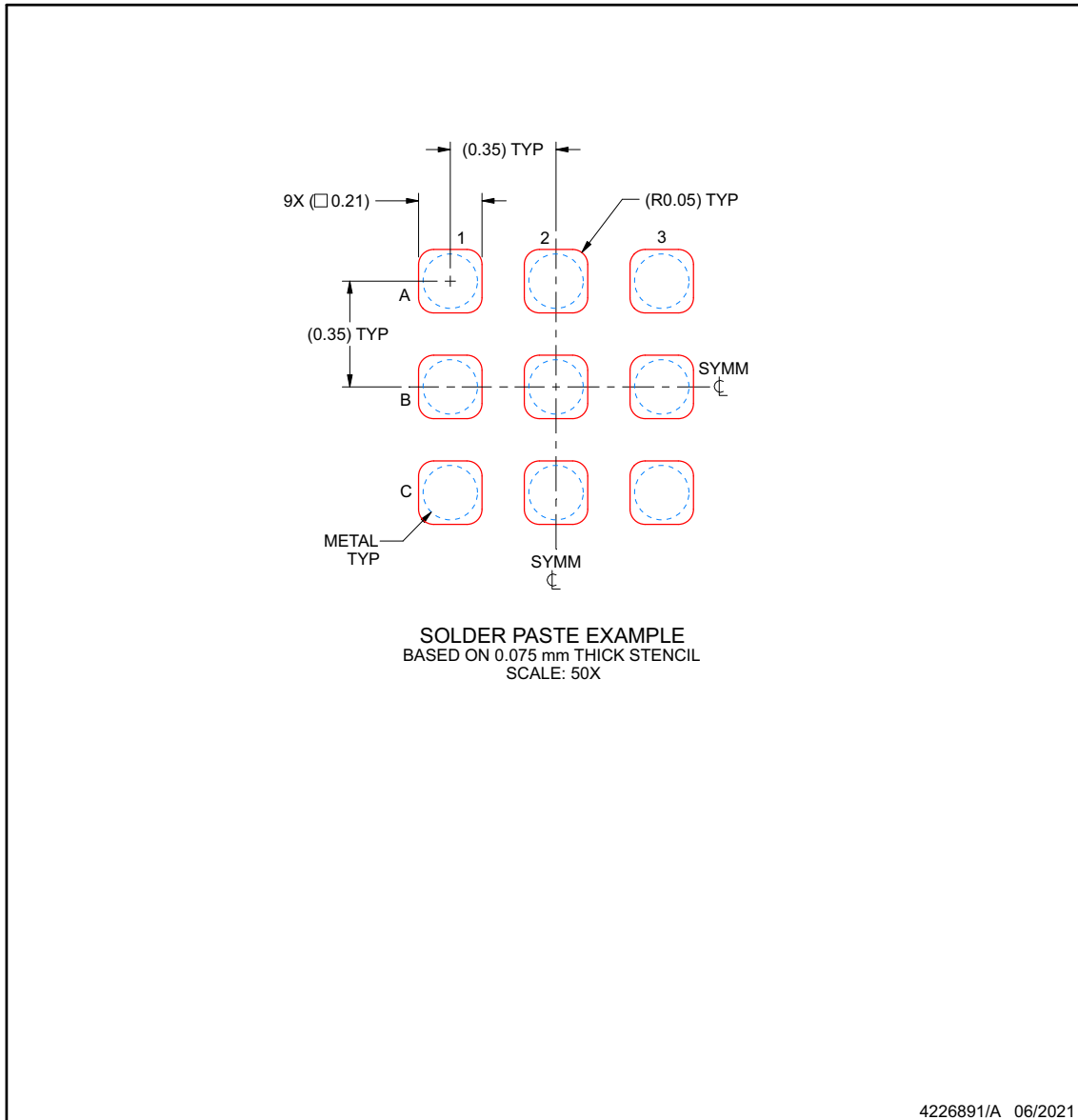
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9061IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1OAF	Samples
TLV9061IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1CA	Samples
TLV9061IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	CG	Samples
TLV9061SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OEF	Samples
TLV9062IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9062	Samples
TLV9062IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IDSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	Samples
TLV9062SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1TDX	Samples
TLV9062SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EOF	Samples
TLV9062SIYCKR	ACTIVE	DSBGA	YCK	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EH	Samples
TLV9064IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064D	Samples
TLV9064IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	Samples
TLV9064IPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	Samples
TLV9064IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064	Samples
TLV9064IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9064SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064S	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV9061, TLV9062, TLV9064 :

- Automotive : [TLV9061-Q1](#), [TLV9062-Q1](#), [TLV9064-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV9061IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9061SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDGKT	VSSOP	DGK	8	250	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9062SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9062SIYCKR	DSBGA	YCK	9	3000	180.0	8.4	1.1	1.1	0.4	2.0	8.0	Q1
TLV9064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9064IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9064SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV9061IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9061SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9062IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
TLV9062IDGKT	VSSOP	DGK	8	250	356.0	356.0	35.0
TLV9062IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV9062IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9062IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TLV9062IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV9062SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9062SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9062SIYCKR	DSBGA	YCK	9	3000	182.0	182.0	20.0
TLV9064IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV9064IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9064IPWT	TSSOP	PW	14	250	353.0	353.0	32.0
TLV9064IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9064IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9064SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

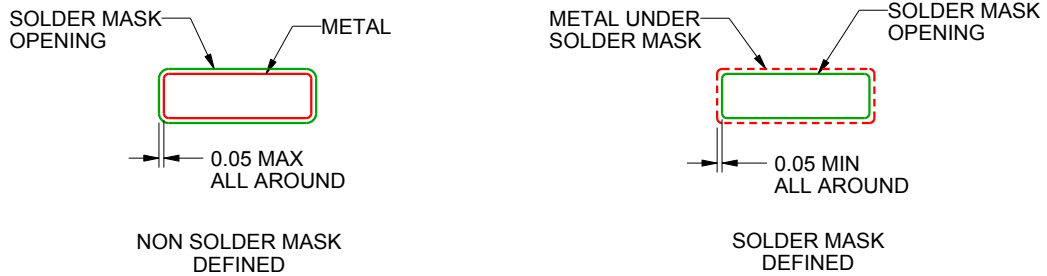
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

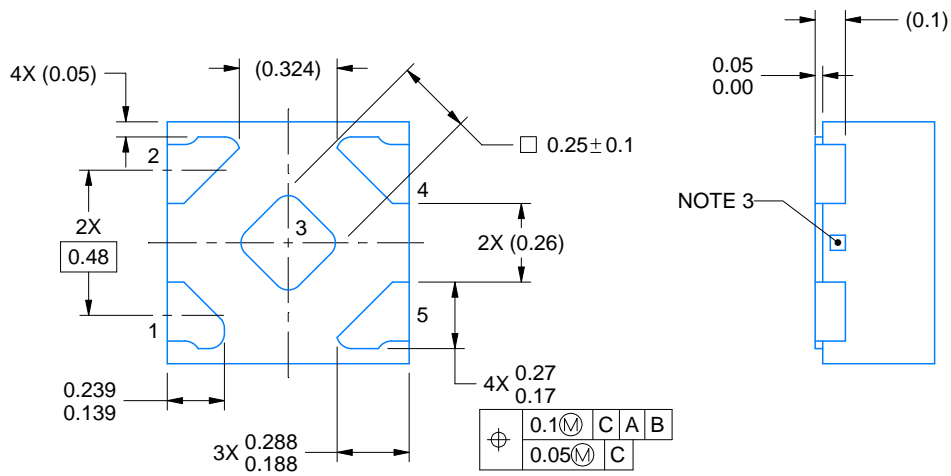
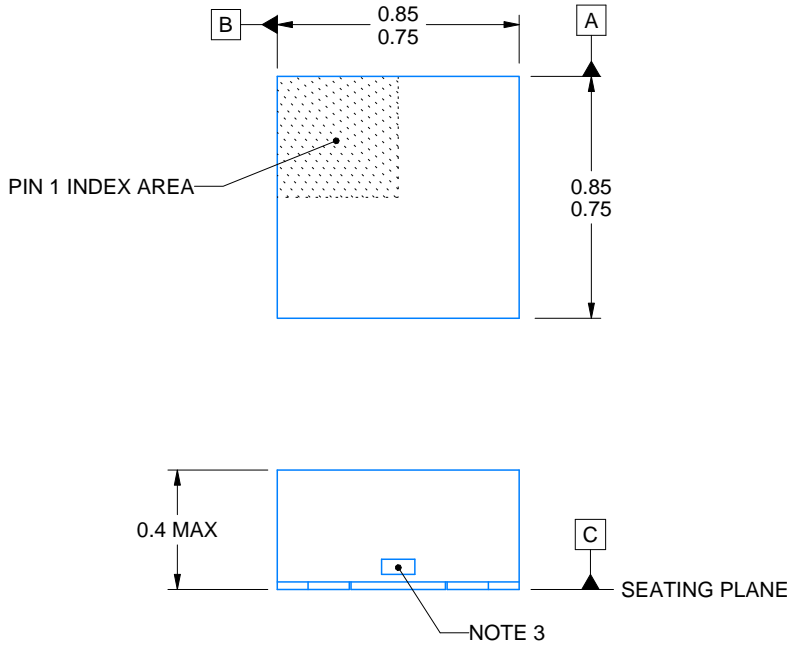
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

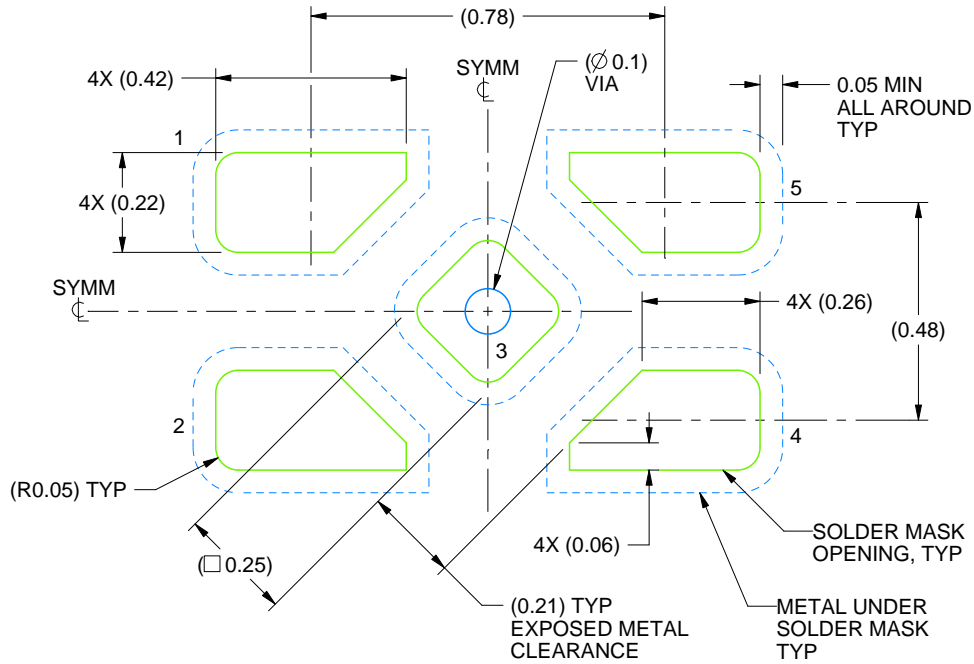
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

RUG (R-PQFP-N10)

PLASTIC QUAD FLATPACK



4208528-3/B 04/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R-PQFP-N10)



4210299-3/A 06/09

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



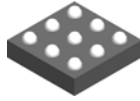
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

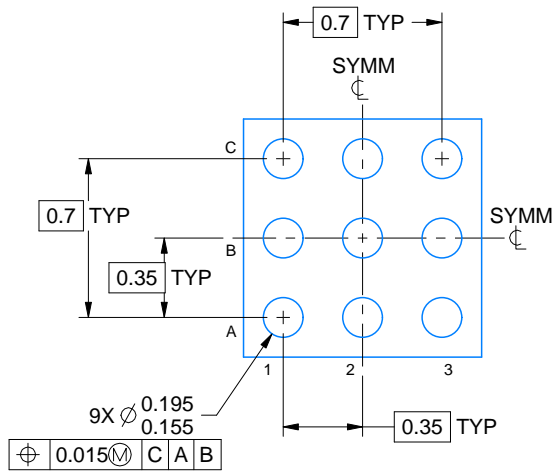
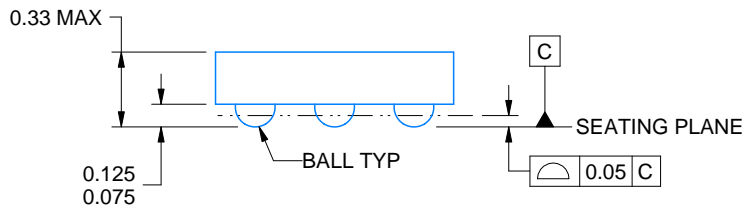
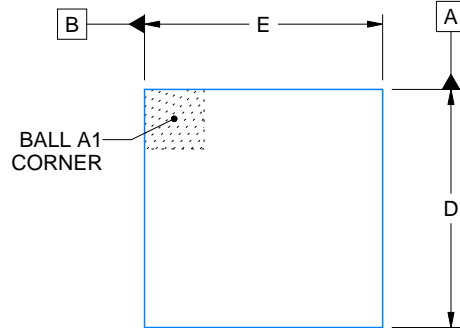
YCK0009



PACKAGE OUTLINE

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.98 mm, Min = 0.92 mm
E: Max = 0.98 mm, Min = 0.92 mm

4225837/A 04/2020

NOTES:

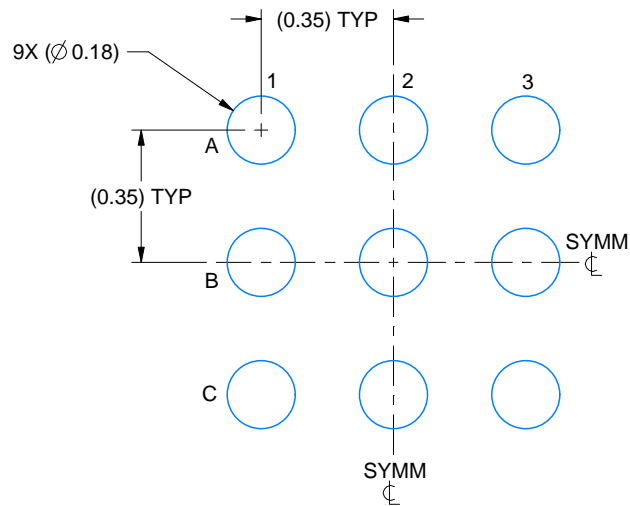
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

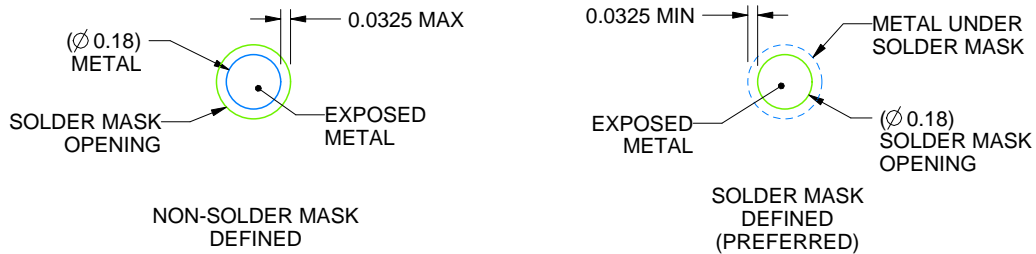
YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4225837/A 04/2020

NOTES: (continued)

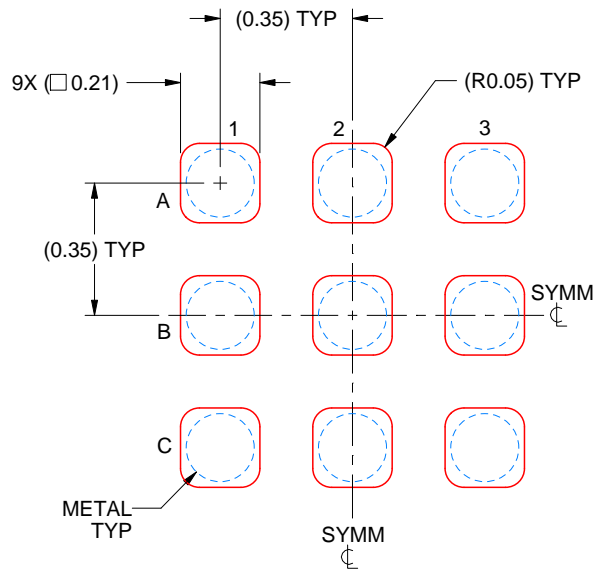
- 3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4225837/A 04/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

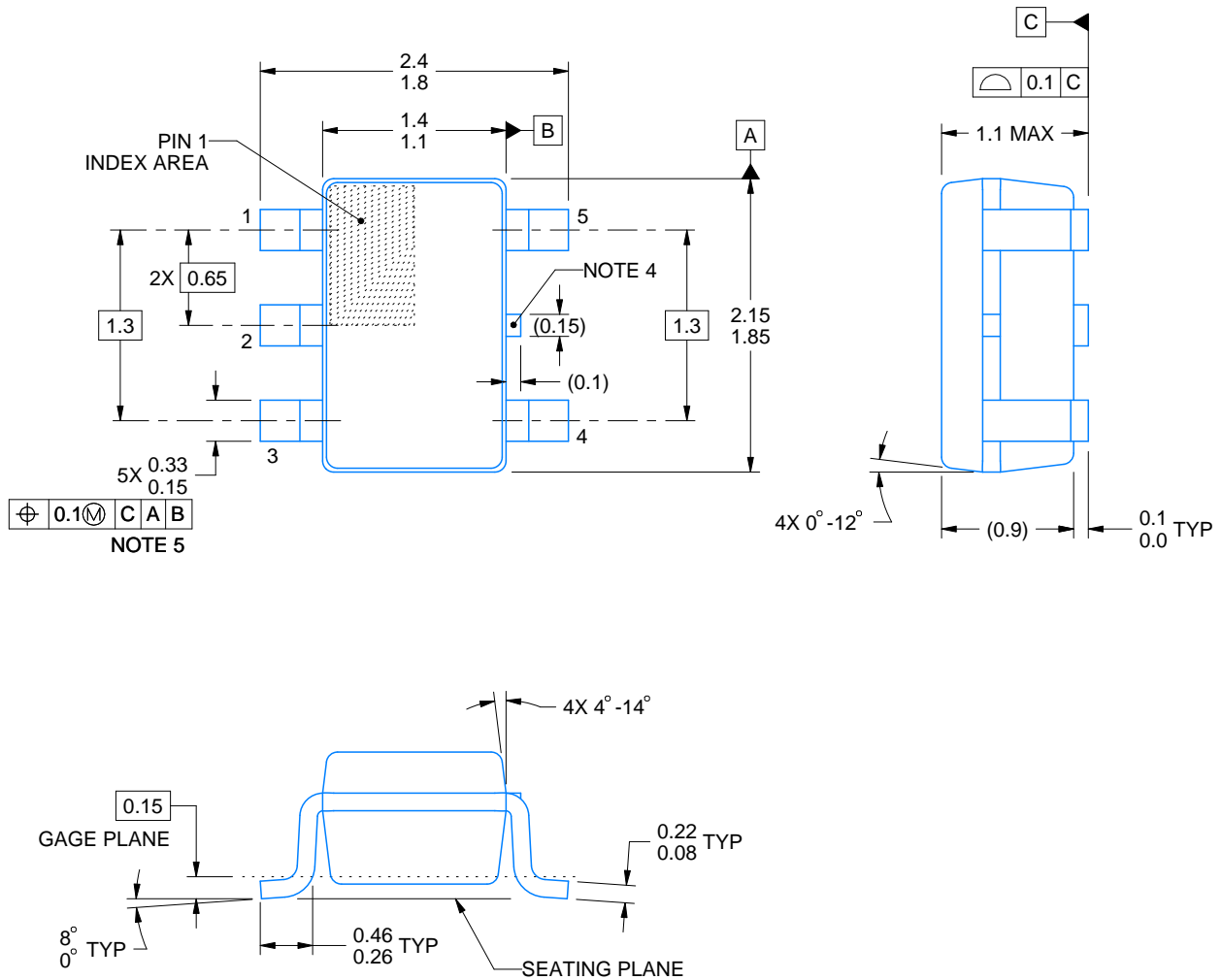
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/F 08/2024

NOTES:

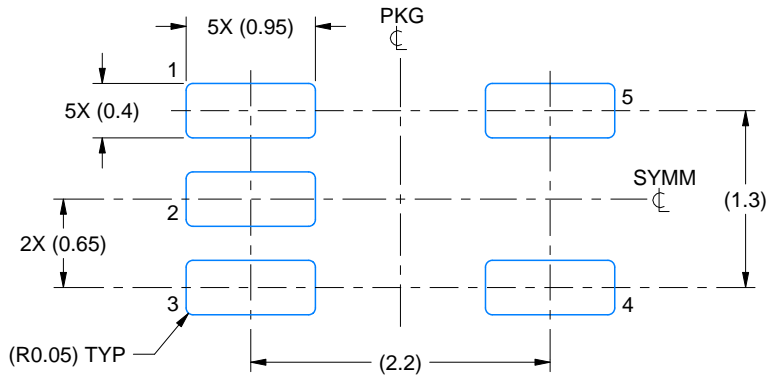
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

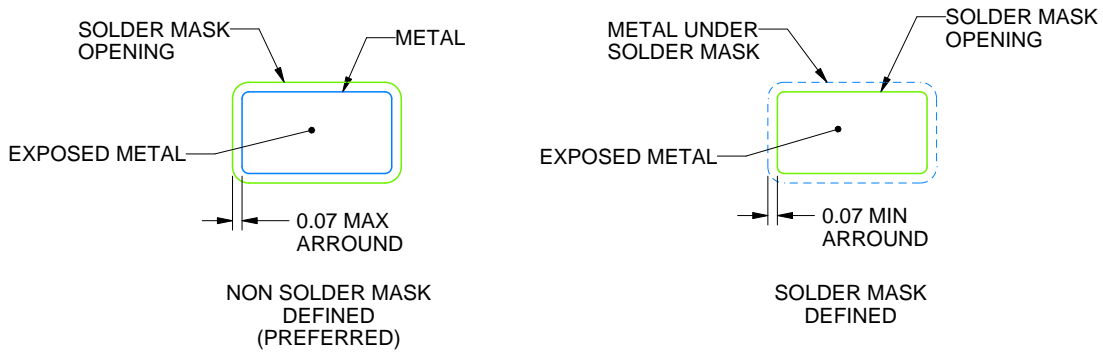
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

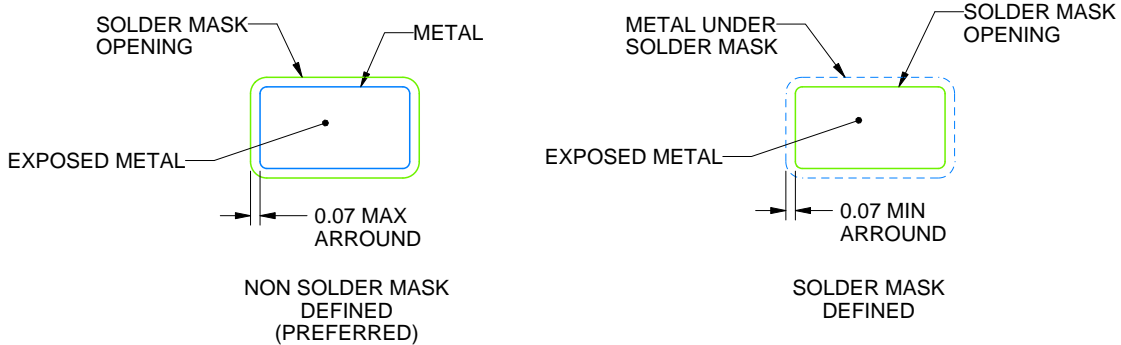
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

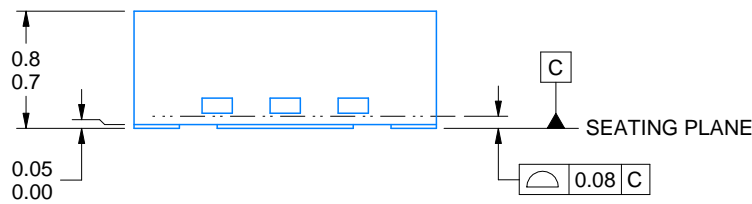
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

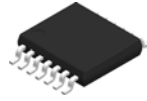
EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

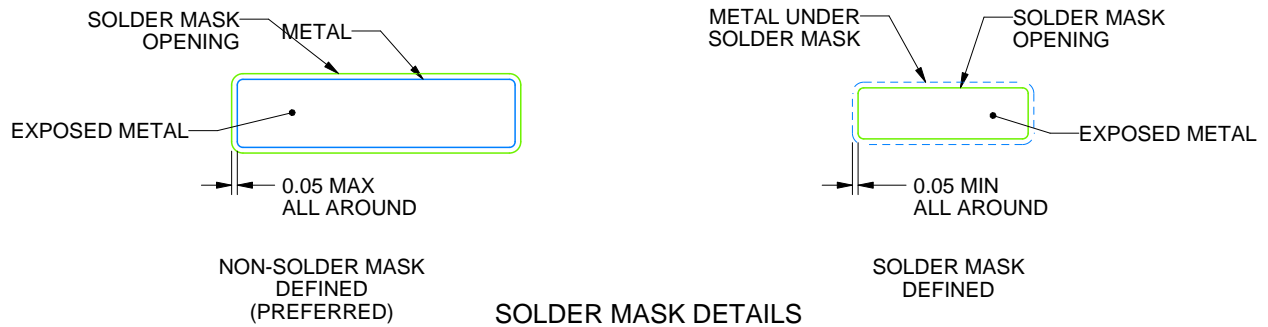
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

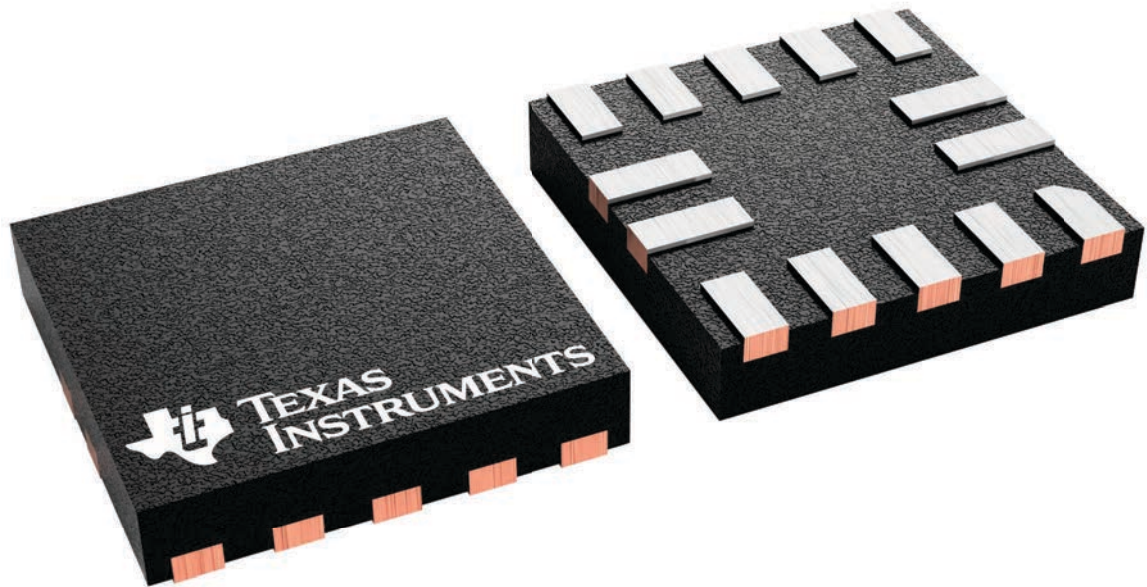
RUC 14

X2QFN - 0.4 mm max height

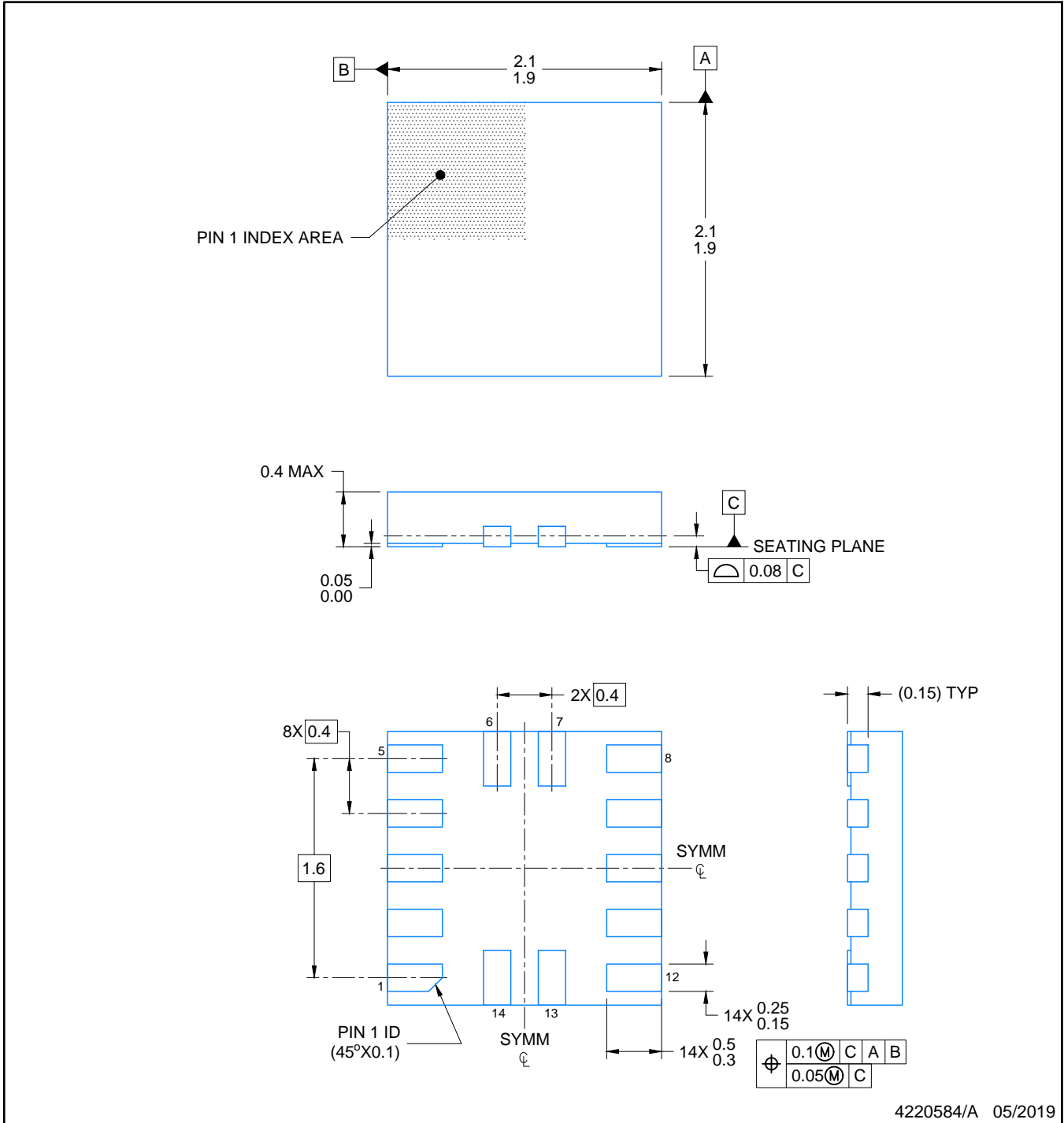
2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



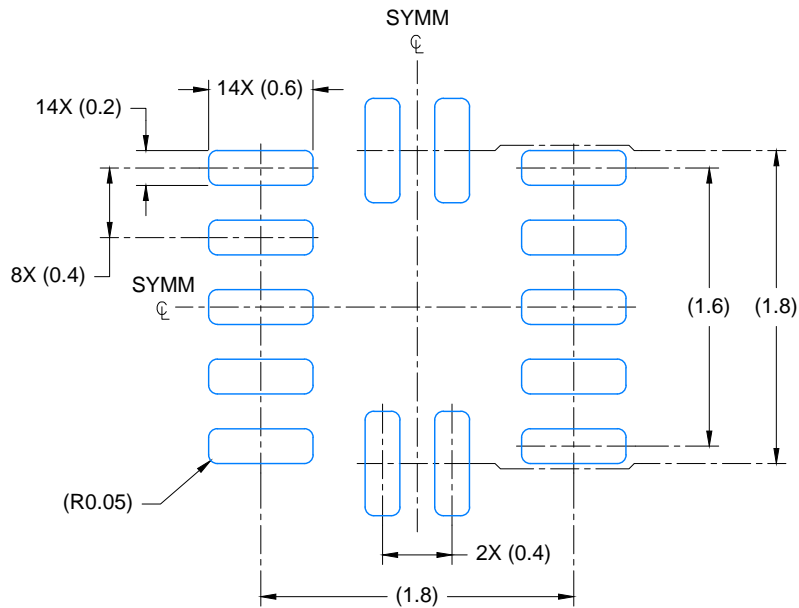
4229871/A



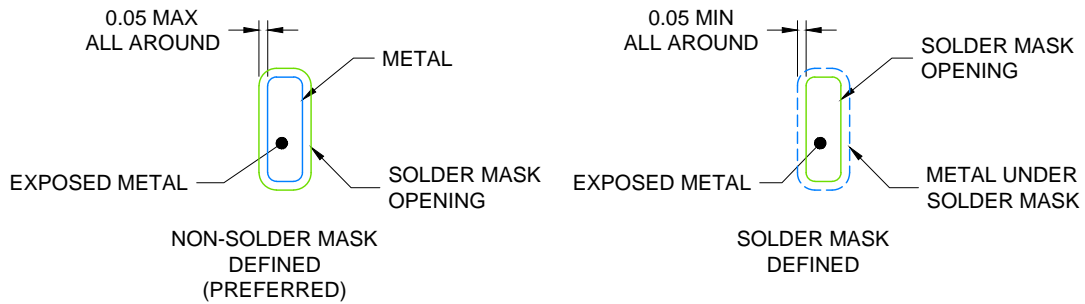
4220584/A 05/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

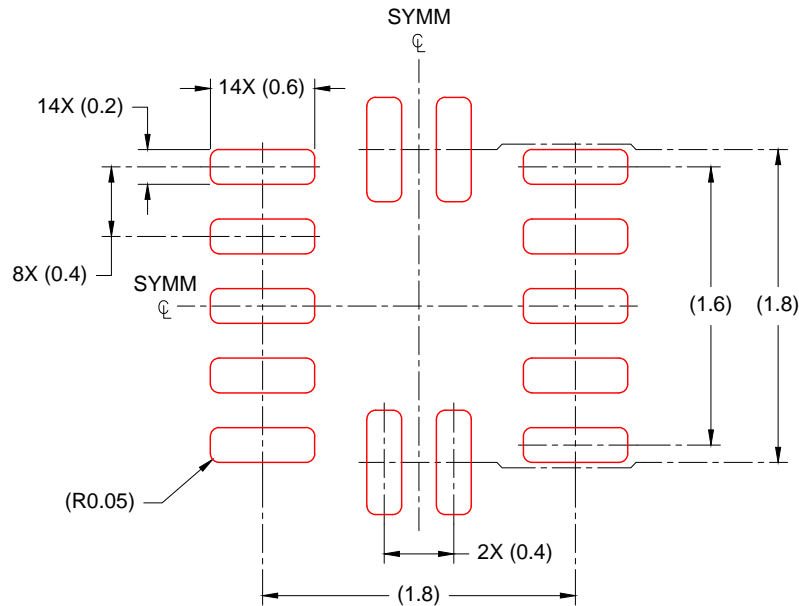
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUC0014A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

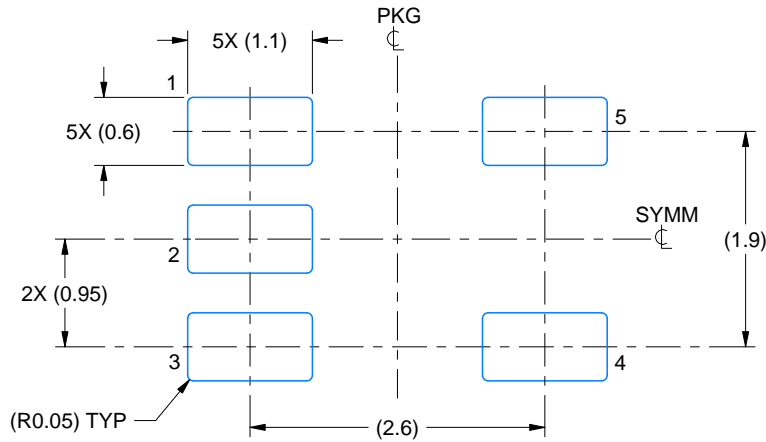
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

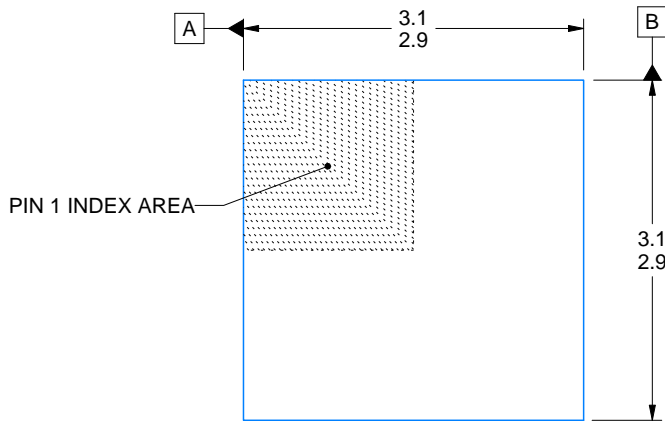
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

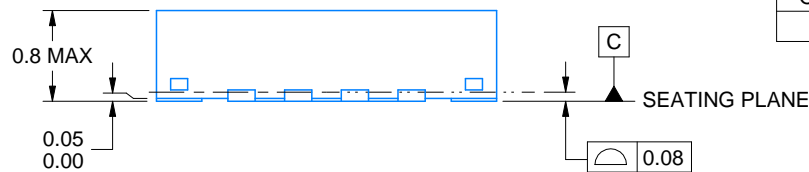
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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