TMP20 ±2.5℃、低消費電力、アナログ出力温度センサ

1 特長

- -55℃～+130℃にわたって±2.5℃の精度
- 電源電圧範囲: 1.8V～5.5V
- 低消費電力: 4µA (最大値)
- *Micro*Sizeパッケージ: SOT-563、SC70-5
- SC70はLM20とピン互換

2 アプリケーション

- 携帯電話
- デスクトップPCおよびノートPC
- ポータブル・デバイス
- 消費者向け電子機器
- バッテリ管理
- 電源
- HVAC
- 熱監視
- ディスク・ドライブ
- 家庭用電気製品および白物家電
- 車載

3 概要

TMP20デバイスはCMOSの高精度アナログ出力温度センサで、小さなSOT-563パッケージで利用できます。TMP20は–55℃～+130℃、電源電圧2.7V～5.5Vで動作し、消費電流は4µAです。15℃～130℃の温度範囲では、最低1.8Vでの動作が可能です。線形伝達関数の傾きは –11.77mV/℃ (標準値)、0℃での出力電圧は1.8639V (標準値)です。TMP20は、–55℃～+130℃の定格温度範囲にわたって±2.5℃の精度を維持します。

TMP20の消費電流は4µA (最大値)なので、デバイスの自己発熱は0.01℃未満に抑えられます。V+が0.5V未満のとき、デバイスはシャットダウン・モードとなり、消費電流は20nA未満(標準値)です。

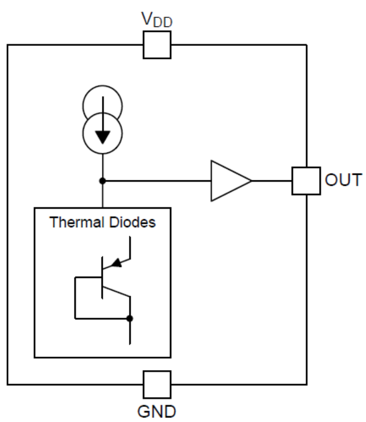
TMP20は5リードのSC70または6リードのSOT-563パッケージで供給され、必要な全体の基板面積を減らすことができます。

製品情報(1)

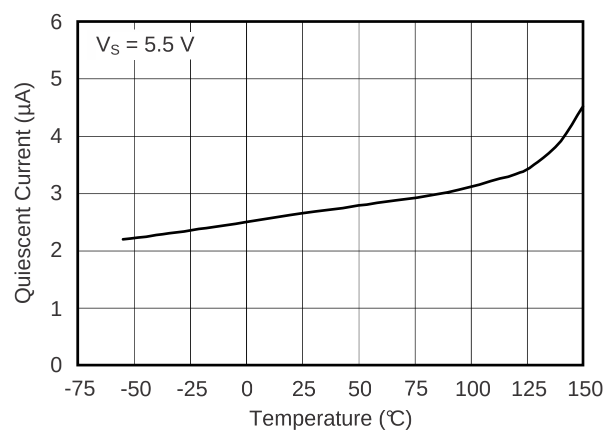
型番	パッケージ	本体サイズ(公称)
TMP20	SOT-563 (6)	1.60mm×1.20mm
	SC70 (5)	2.00mm×1.25mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

デバイスのブロック図



デバイスの温度と静止電流との関係



目次

4 改訂履歴

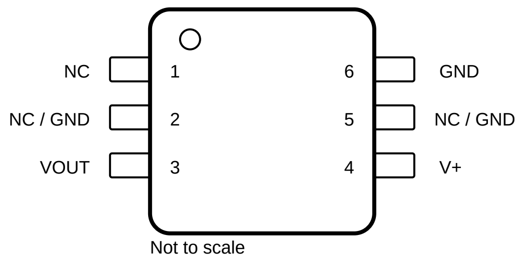
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (October 2017) から Revision B に変更	**Page**
• 「*デバイスの温度と静止電流との関係*」グラフのy軸の単位をmAからµAに変更	1
• Changed the y-axis unit of *Device Quiescent Current vs Temperature* graph from: mA to: µA	6
• Changed the y-axis unit of *Device Quiescent Current vs Temperature* graph from: mA to: µA	12
• 「*ドキュメントの更新通知を受け取る方法*」セクションを追加	16

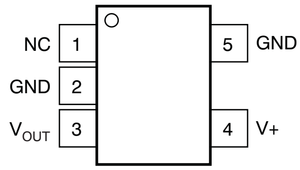
2009年12月発行のものから更新	**Page**
• 最新のTIドキュメントおよび翻訳基準に合わせてデータシートのフォーマットと内容を更新	1
• 「*製品情報*」セクションに本体サイズの情報を追加	1
• 「デバイスのブロック図」を更新	1
• 「デバイスの温度と静止電流との関係」を更新	1
• Reformatted *Absolute Maximum Ratings* table	4
• Changed *Thermal Information* table and added thermal information	4
• Changed minimum temperature sensitivity value from –11.4 mV/°C to –12.2 mV/°C in *Electrical Characteristics* table	5
• Changed maximum temperature sensitivity value from –12.2 mV/°C to –11.4 mV/°C in *Electrical Characteristics* table	5
• Updated 図 1	6
• Updated 図 3	6
• Updated 図 7	6
• 追加 *Functional Block* diagram, key graphics on front page, typical application schematic, application curves, and updated layout images	8
• Reformatted equations in *Transfer Function* section	9
• Corrected 式 2 in *Transfer Function* section	9
• 追加 図 15および図 16に著作権表記を	14

5 Pin Configuration and Functions

DRL Package
6-Pin SOT-563
Top View



DCK Package
5-Pin SC70
Top View



NC- no internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRL (SOT-563)	DCK (SC70)		
GND	6	5	—	Ground pin
NC	1	1	—	This pin must be grounded or left floating. See *Layout Example* for more information.
NC / GND	2, 5	2	—	This pin must be grounded or left floating. For best thermal response, connect to GND plane. See *Layout Example* for more information.
V_{OUT}	3	3	O	Analog output
V+	4	4	I	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V+		7	V
Operating temperature	–55	150	°C
Junction temperature, $T_{J(max)}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	1.8	5.5	V
T_A	Specified temperature range	–55	130	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP20		UNIT
		DRL (SOT563)	DCK (SC70)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	238	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	253	263.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	126.4	76.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	126	51.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	1.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	125.9	50.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT [(1)]						
	Accuracy [(2)]	T_A = –55°C to 130°C	–2.5		2.5	°C
	vs supply	V+ = 1.8 V to 5.5 V T_A = 15°C to 130°C	–0.05		0.05	°C/V
		V+ = 2.7 V to 5.5 V T_A = –50°C to 130°C	–0.05		0.05	°C/V
	Temperature sensitivity [(3)]	T_A = –30°C to 100°C	–12.2	–11.77	–11.4	mV/°C
	Output voltage [(4)]	T_A = 0°C		1863.9		mV
		T_A = 25°C		1574		
	Nonlinearity [(5)]	–20°C ≤ T_A ≤ 80°C		±0.4%		
ANALOG OUTPUT						
	Output resistance	–600 µA ≤ I_{LOAD} ≤ 600 µA		10		Ω
	Load regulation	–600 µA ≤ I_{LOAD} ≤ 600 µA		6		mV
	Maximum capacitive load		1			nF
POWER SUPPLY						
V_S	Specified voltage	T_A = –55°C to 130°C	2.7		5.5	V
		T_A = 15°C to 130°C [(6)]	1.8		5.5	
I_Q	Quiescent current	V+ = 5.5 V T_A = 25°C		2.6	4	µA
	Over temperature	V+ = 5.5 V T_A = –55°C to 130°C			6	µA
I_{SD}	Shutdown current	V+ < 0.5 V		20		nA
TEMPERATURE RANGE						
	Specified operating	T_A = –55°C to 130°C	–55		130	°C
		T_A = 15°C to 130°C [(6)]	15		130	°C
	Operating range	V+ = 2.7 V to 5.5 V	–55		150	°C
θ_{JA}	Thermal resistance	SC70		185		°C/W
		SOT-563		238		°C/W
	Self-heating	SC70			0.01	°C
		SOT-563			0.01	°C

(1) 100% production tested at T_A = 25°C. Specifications over temperature range are assured by design.
(2) Power-supply rejection is encompassed in the accuracy specification.
(3) Temperature sensitivity is the average slope to the equation $V_O = (-11.77 \times T) + 1.860$ V.
(4) V_{OUT} is calculated from temperature with the following equation:
$V_O = (-3.88 \times 10^{-6} \times T^2) + (-1.15 \times 10^{-2} \times T) + 1.8639$ V,
where T is in °C.
(5) Nonlinearity is the deviation of the calculated output voltage from the best fit straight line.
(6) The TMP20 transfer function requires the output voltage to rise above the 1.8-V supply as the temperature decreases below 15°C. When operating at a 1.8-V supply, it is normal for the TMP20 output to approach 1.8 V and remain at that voltage as the temperature continues to decrease below 15°C. This condition does not damage the device. Once the temperature rises above 15°C, the output voltage resumes changing as the temperature changes, according to the transfer function specified in this document. For more information about the transfer function, see *Transfer Function* .

6.6 Typical Characteristics

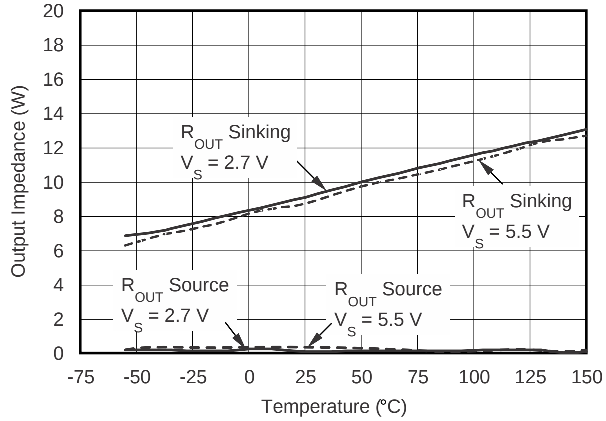


図 1. Output Impedance vs Temperature

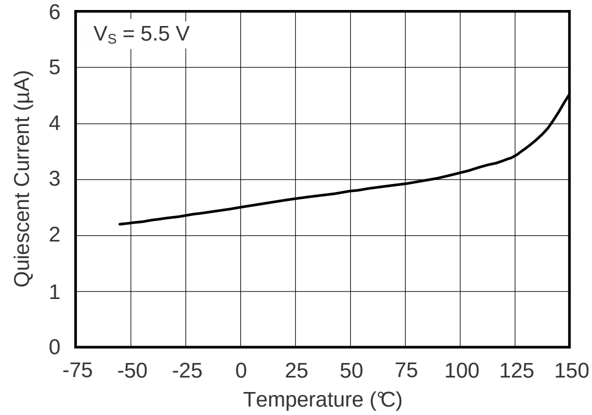


図 2. Quiescent Current vs Temperature

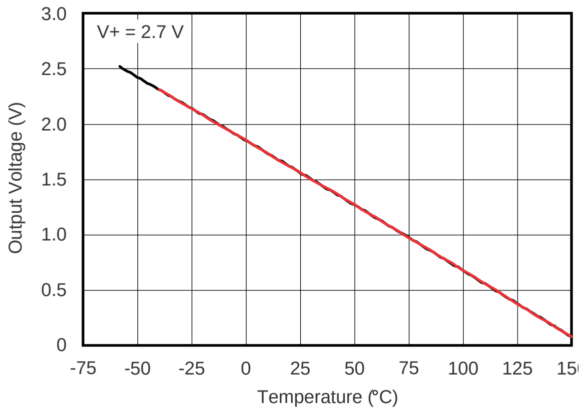


図 3. Output Voltage vs Temperature

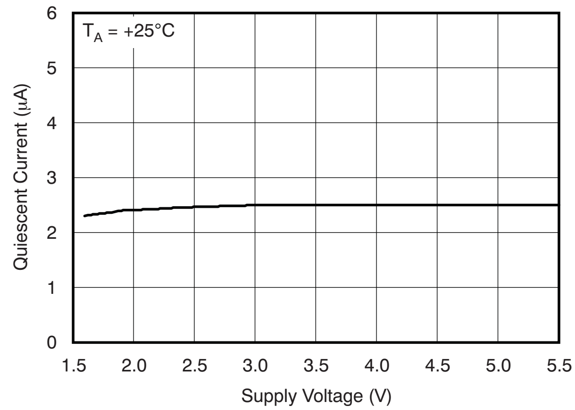


図 4. Quiescent Current vs Supply Voltage

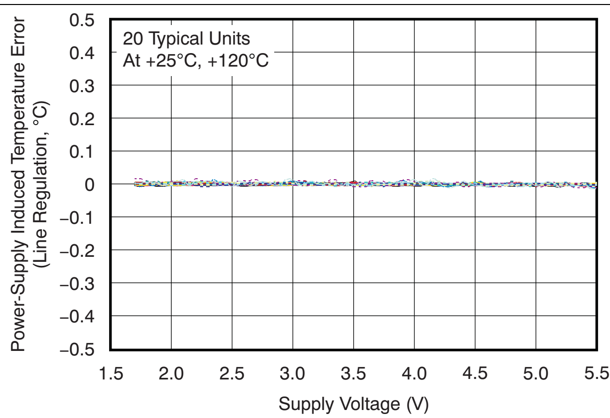


図 5. Power-Supply Rejection vs Temperature

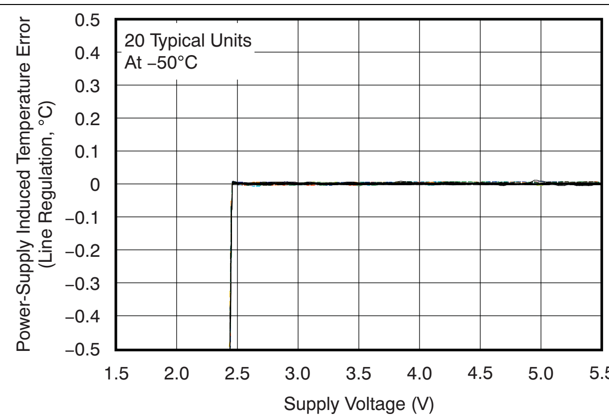


図 6. Power-Supply Rejection vs Temperature

Typical Characteristics (continued)

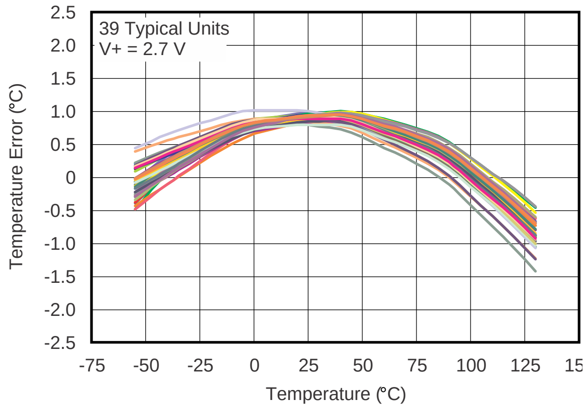


図 7. Temperature Error vs Temperature

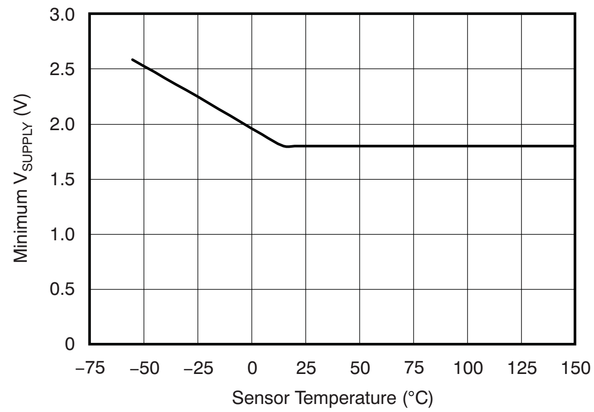


図 8. Minimum Supply Voltage vs Temperature

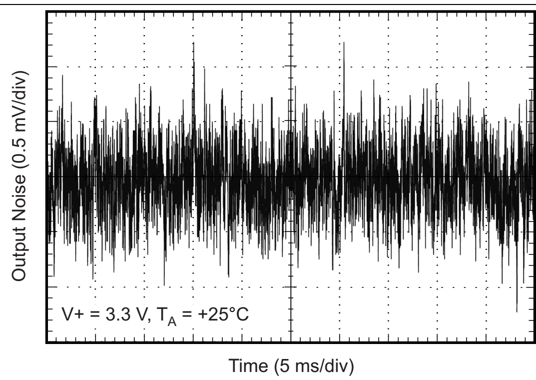


図 9. Wideband Output Noise Voltage

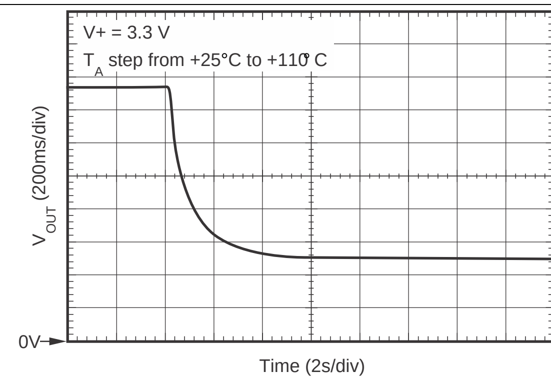


図 10. Thermal Settling (Fluid-Filled Temperature Bath)

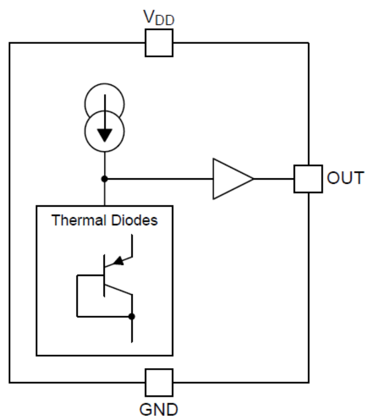
7 Detailed Description

7.1 Overview

The TMP20 device is a precision analog output temperature sensor. The temperature range of operation is –55°C to +130°C with supply voltages of 2.7 V to 5.5 V. The TMP20 operates from power-supply voltages as low as 1.8 V over a temperature range of 15°C to 130°C.

TI recommends power supply bypassing; use a 100-nF capacitor placed as closely as possible to the supply pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Transfer Function

The analog output of the TMP20 over the –55°C to +130°C temperature range corresponds to the parabolic transfer function shown in
「ドキュメントの更新通知を受け取る方法」セクションを追加:

$$V_{OUT} = \left(-3.88 \times 10^{-6} \times T^2\right) + \left(-1.15 \times 10^{-2} \times T\right) + 1.8639\ V \quad (1)$$

Where:

- the temperature (T) is in °C.

When solving for temperature, the equation is shown as 式 2:

$$T = -1481.96 + \sqrt{2.1962 \times 10^6 + \frac{(1.8639 - V_O)}{3.88 \times 10^{-6}}} \quad (2)$$

These equations apply over the entire operating range of –55°C to +130°C.

A simplified linear transfer function referenced at 25°C is shown in 式 3:

$$V_{OUT} = -11.69\ mV/°C \times T + 1.8863\ V \quad (3)$$

Linear transfer functions are calculated for limited temperature ranges by calculating the slope and offset for that limited range, where slope is calculated by 式 4:

$$m = -7.76 \times 10^{-6} \times T - 0.0115 \quad (4)$$

Where:

- T equals the temperature at the middle of the temperature range of interest

The offset in the linear transfer function is calculated with 式 5:

$$b = \left(V_{OUT}(T_{MAX}) + V_{OUT}(T) - m \times (T_{MAX} + T)\right) / 2 \quad (5)$$

where

- $V_{OUT}(T_{MAX})$ is the calculated output voltage at T_{MAX} as determined from 「ドキュメントの更新通知を受け取る方法」セクションを追加.

$V_{OUT}(T)$ is the calculated output voltage at T as calculated by
「ドキュメントの更新通知を受け取る方法」セクションを追加.

7.3.1.1 Example 1

Determine the linear transfer function for –40°C to +110°C.

T_{MIN} = –40°C; T_{MAX} = 110°C; therefore, T = 35°C

m = –11.77mV/°C
V_{OUT} (110°C) = 0.5520 V
V_{OUT} (35°C) = 1.4566 V
b = 1.8576 V

The linear transfer function for –40°C to +110°C is shown in 式 6:

$$V_{OUT} = -11.77\ mV/°C \times T + 1.8576\ V \quad (6)$$

Feature Description (continued)

表 1 lists common temperature ranges of interest and the corresponding linear transfer functions for these ranges. Note that the error (maximum deviation) of the linear equation from the parabolic equation increases as the temperature ranges widen.

表 1. Common Temperature Ranges and Corresponding Linear Transfer Functions

TEMPERATURE RANGE		LINEAR EQUATION (V)	MAXIMUM DEVIATION OF LINEAR EQUATION FROM PARABOLIC EQUATION (°C)
T_{MIN} (°C)	T_{MAX} (°C)		
–55	130	V_{OUT} = –11.79 mV/°C × T + 1.8528	±1.41
–40	110	V_{OUT} = –11.77 mV/°C × T + 1.8577	±0.93
–30	100	V_{OUT} = –11.77 mV/°C × T + 1.8605	±0.70
–40	85	V_{OUT} = –11.67 mV/°C × T + 1.8583	±0.65
–10	65	V_{OUT} = –11.71 mV/°C × T + 1.8641	±0.23
35	45	V_{OUT} = –11.81 mV/°C × T + 1.8701	±0.004
20	30	V_{OUT} = –11.69 mV/°C × T + 1.8663	±0.004

7.4 Device Functional Modes

The singular functional mode of the TMP20 is an analog output inversely proportional to temperature.

8 Application and Implementation

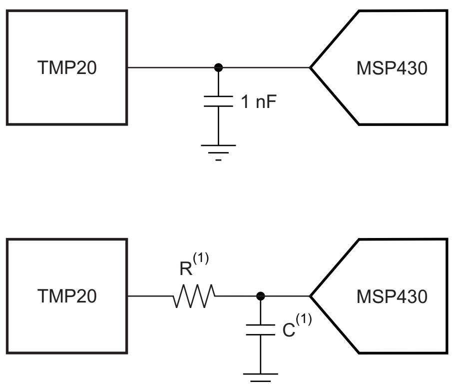
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Drive and Capacitive Loads

When used in noisy environments, adding a capacitor from the output to ground with a series resistor filters the TMP20 output; this configuration is shown in 図 11. The TMP20 can drive up to 1 nF of load capacitance while sourcing and sinking 600 μA. Under this condition, capacitive loads in the range of 1 nF to 10 μF require a 150-Ω series output resistor to achieve a stable temperature measurement. The output impedance of the TMP20 is typically 10 Ω when sinking currents and less than 1 Ω when sourcing current, as shown in 図 1.



(1) A series resistor (R) may be required depending upon the amount of capacitance (C) and the amount of source and sink current drawn from the output of the TMP20.

図 11. TMP20 Output Filtering

8.2 Typical Application

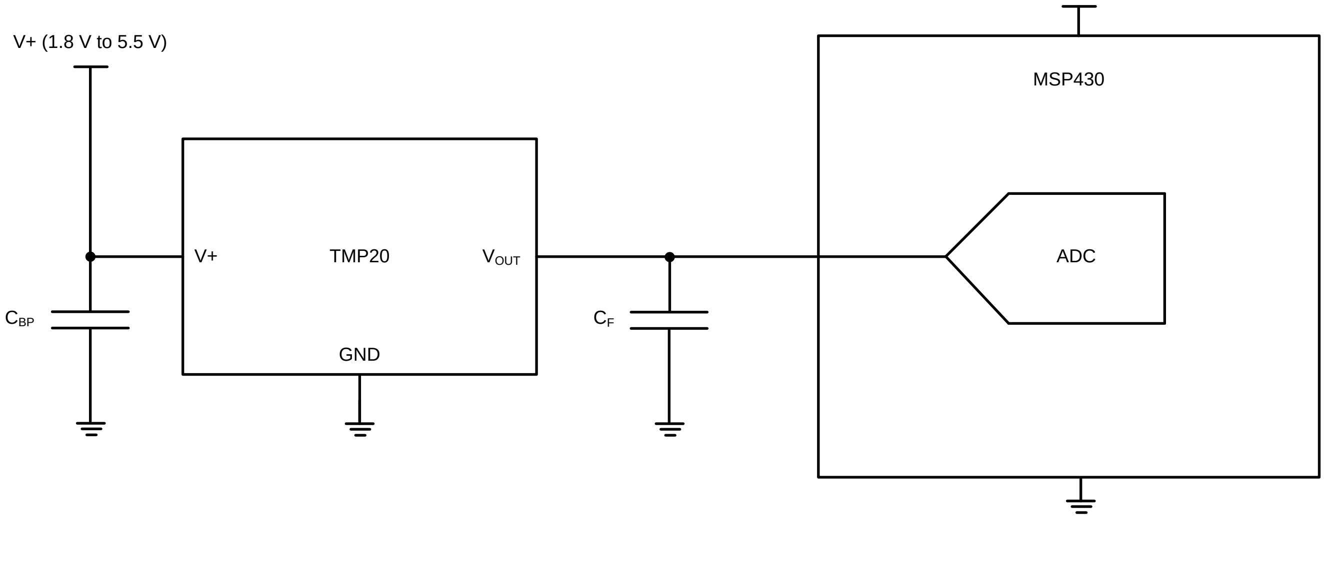


図 12. Suggested Connections to a MCU ADC

8.2.1 Design Requirements

ADCs that are found in microcontrollers (such as the MSP430 line of microcontrollers) take charge during the sampling phase. A high sampling frequency results in too much charge pulled into the ADC and sags the output voltage of the TMP20, which results in a reading that is hotter than normal. To mitigate this, place a capacitor (C_F) between the TMP20 and the ADC. The capacitor functions as a charge reservoir.

8.2.2 Detailed Design Procedure

The size of C_F depends on the size of the internal sampling capacitor and the sampling frequency. The charge requirements may vary because not all ADCs have identical input stages. This general ADC application is shown as an example only.

8.2.3 Application Curves

図 13 shows the quiescent current versus temperature.

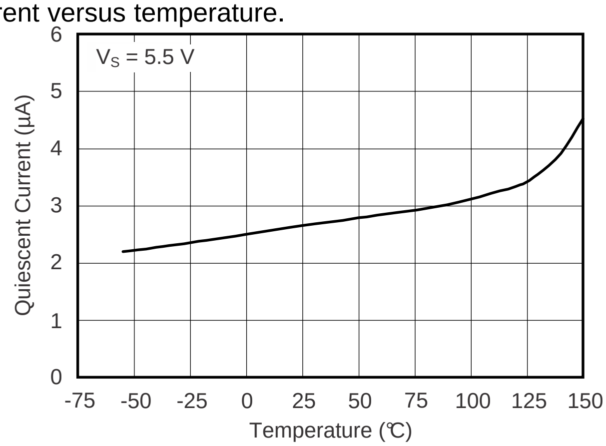


図 13. Quiescent Current vs Temperature

9 Power Supply Recommendations

The low supply current and supply range of 1.8 V to 5.5 V enable the TMP20 to be powered from multiple supply sources.

Power supply bypassing is optional and is typically dependent on the noise of the power supply. In noisy systems, adding bypass capacitors may be necessary to decrease the noise that couples to the output of the TMP20.

10 Layout

10.1 Layout Guidelines

The substrate on the TMP20AIDCK package is directly connected through conductive epoxy to the flag that connects pin 2 on the lead frame. Consequently, pin 2 is the best lead for a conductive thermal connection to the TMP20 die. The optimal electrical connection for this pin is ground (GND).

注意

Do not attempt to connect pin 2 (DCK package) to any electrical potential other than ground.

If it is not possible to connect pin 2 to ground, it is possible to electrically isolate this pin (that is, leave it floating). Take care when electrically isolating this pin because any noise or electromagnetic interference or radio frequency interference (EMI or RFI) spikes that couple in through this pin can cause erroneous temperature results.

shows a proper layout of the TMP20 with correct electrical and thermal connections to pin 2.

10.2 Layout Example

図 14 shows a layout of the TMP20 with proper electrical and thermal connections to pin 2.

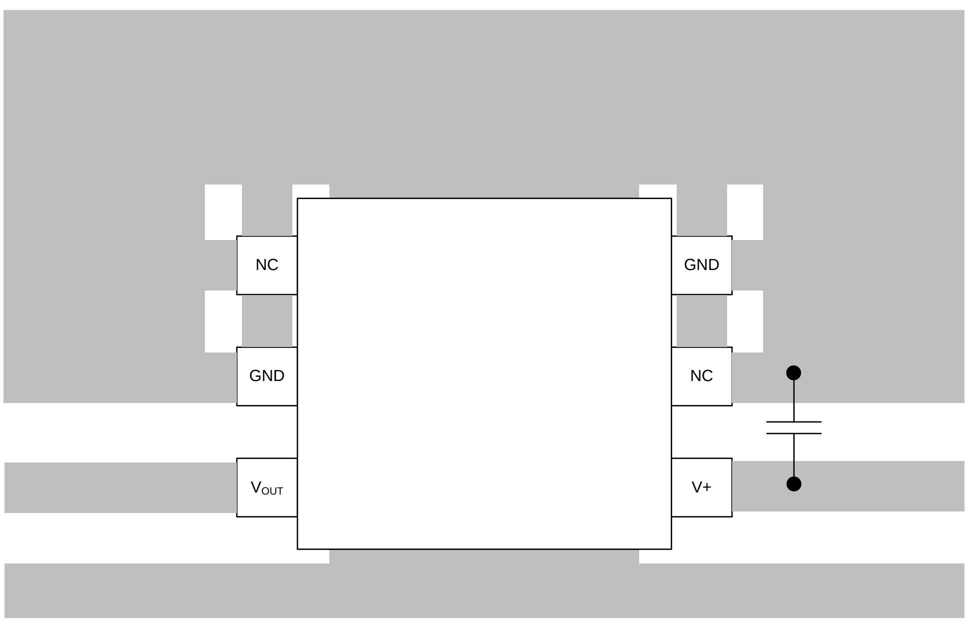


図 14. TMP20 Layout With Proper Electrical and Thermal Connections

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 TINA-TI (無料のダウンロード・ソフトウェア)

TINAは、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TIはTINAソフトウェアの無料バージョンで、完全な機能を持ち、パッシブとアクティブ両方のモデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはWEBENCH® Design Centerから無償でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。

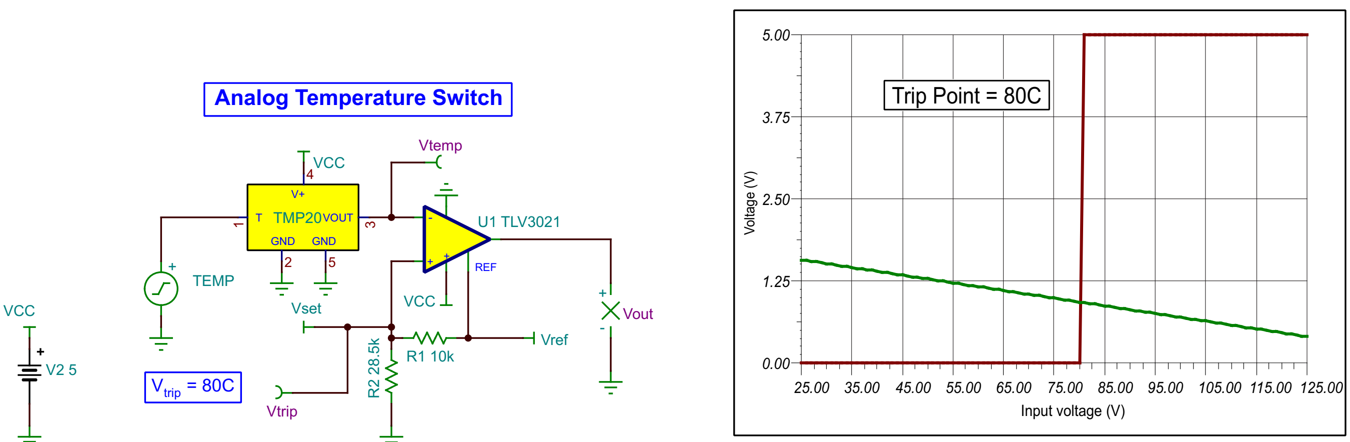
仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

TMP20用のTINA-TI回路の例を、図 15および図 16に示します。これによって、特定のアプリケーション用の回路設計を開発、変更、および評価できます。これらのシミュレーション・ファイルのダウンロード用リンクを以下に示します。

11.1.1.1 TINA-TI SPICEベースのアナログ・シミュレーション・プログラムをTMP20で使用する

注

これらのファイルを使用するには、TINAソフトウェア(DesignSoftから入手できます)またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

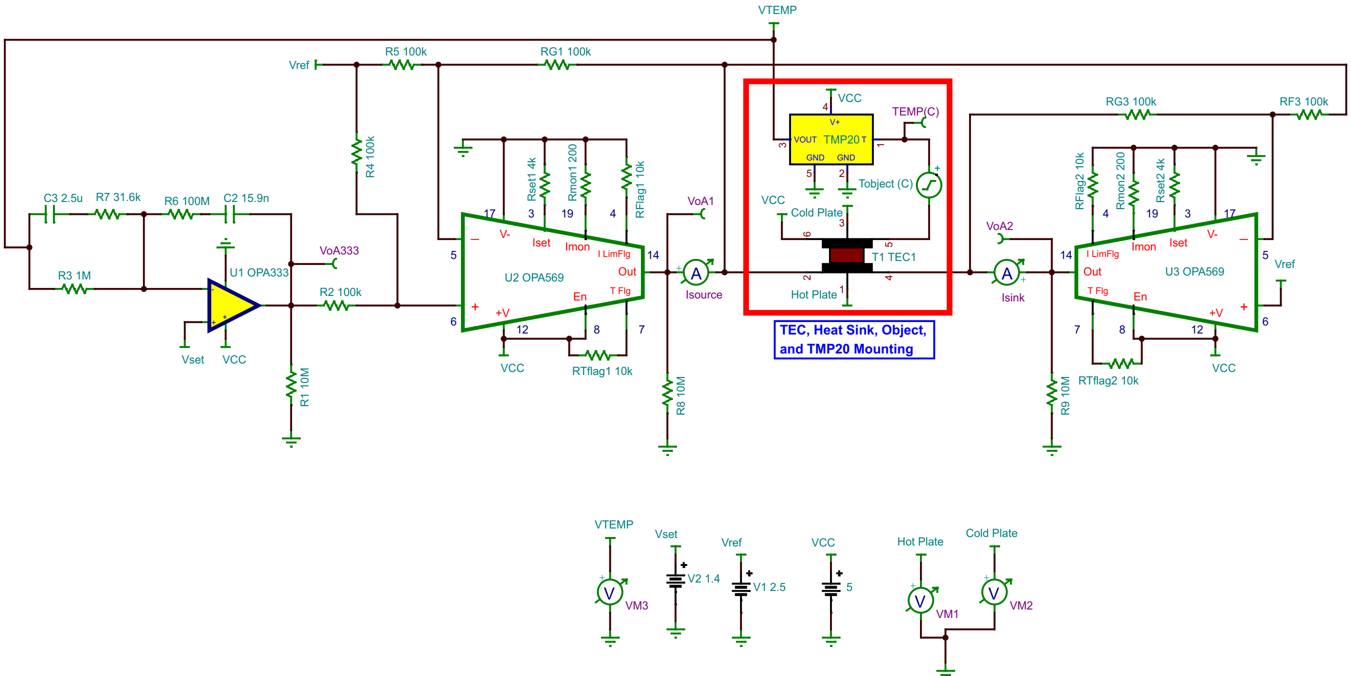


Note: このTMP20 TINAモデルは暫定的なものです。

図 15. アナログ温度スイッチ

この回路用のTINA-TIシミュレーション・ファイルを含む圧縮ファイルを、WEBENCH® Design Centerでダウンロードできます。

デバイス・サポート (continued)



(1) このTMP20 TINAモデルは暫定的なものです。

(2) パラメータと定義

a. T_{object} = 冷却対象物の温度(℃)

b. V_{set} = TMP20から期待される出力温度に対応する電圧

c. VTEMP = TMP20の出力電圧

d. Hotplate = 対象物の反対側にあるTECプレート

e. Coldplate = 対象物と接触しているTECプレート

(3) この構成では、TECドライバは-T℃まで冷却を、41℃まで加熱を行えます。V_{set}の範囲は1.38V～1.95Vです。OPA569デバイスの出力は±1.65A、±0.5V～±4.5Vです。10MΩの抵抗はTINAの収束用です。

(4) TINAソフトウェアの収束には、**Analysis/Set Analysis Parameters**メニューで、シャントのコンダクタンス = 1pに設定します。

図 16. 熱電冷却器

この回路用のTINA-TIシミュレーション・ファイルを含む圧縮ファイルは、「熱電冷却器」でダウンロードできます。

デバイス・サポート (continued)

11.1.2 開発サポート

WEBENCH® Design Center

TINA-TIフォルダ

アナログ温度スイッチ

熱電冷却器

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP20AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODB	Samples
TMP20AIDCKT	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-55 to 125	ODB	
TMP20AIDRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODA	Samples
TMP20AIDRLT	OBSOLETE	SOT-5X3	DRL	6		TBD	Call TI	Call TI	-55 to 125	ODA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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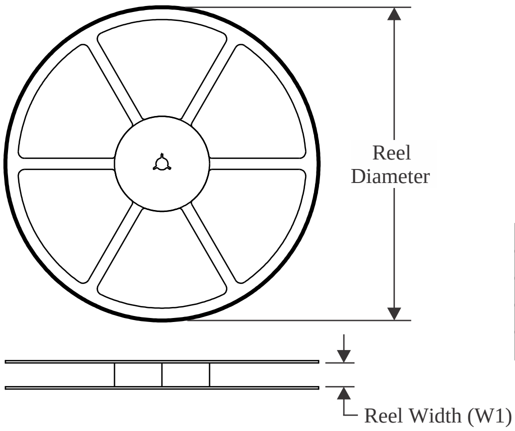
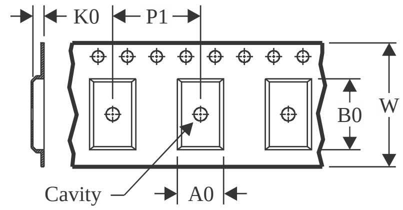
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

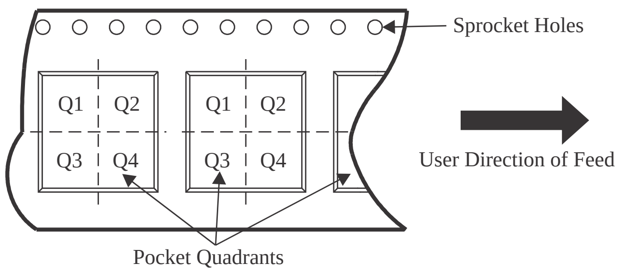


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

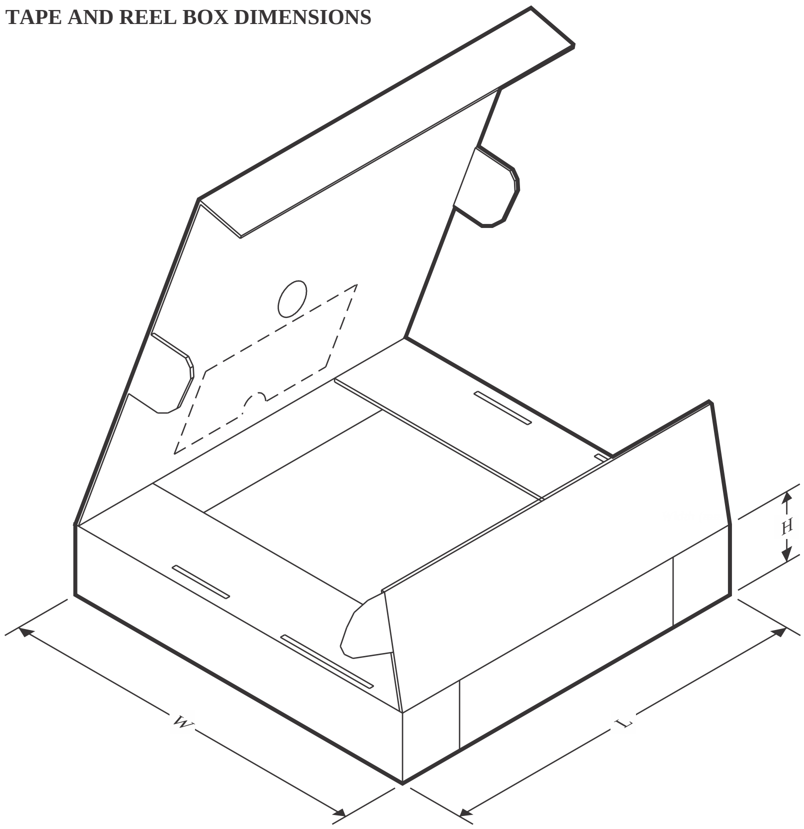
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

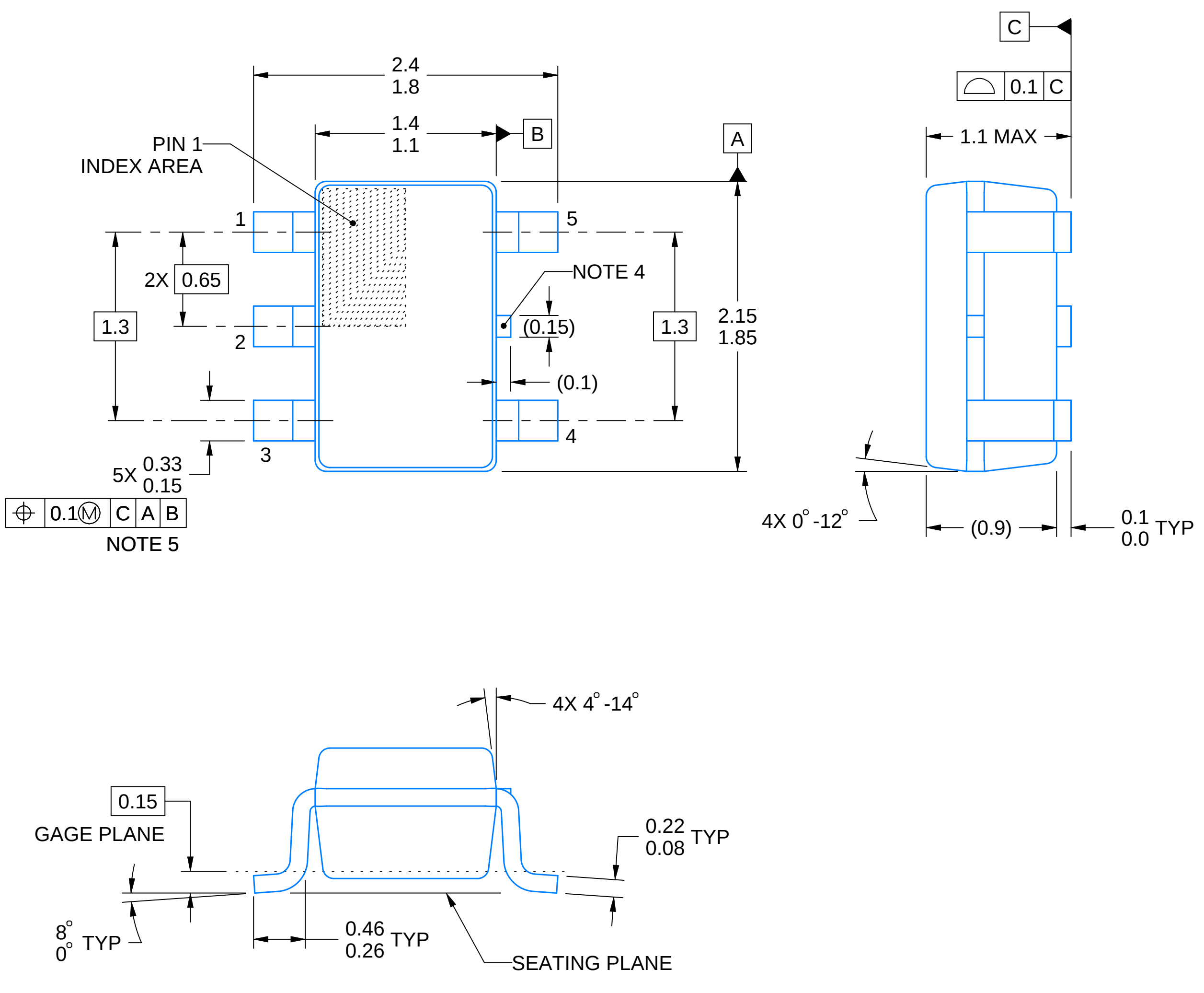
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP20AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMP20AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMP20AIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



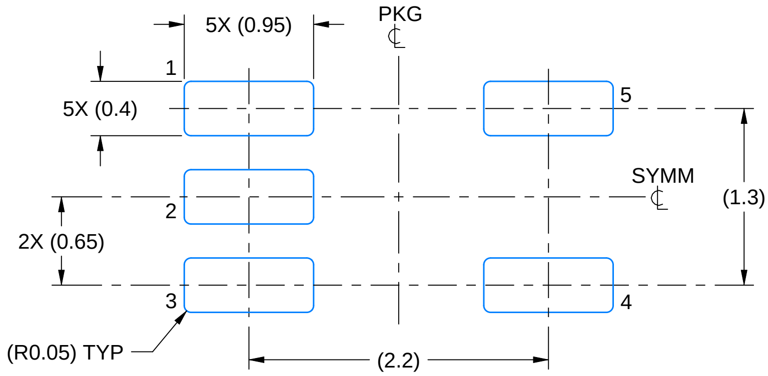
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP20AIDCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TMP20AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TMP20AIDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

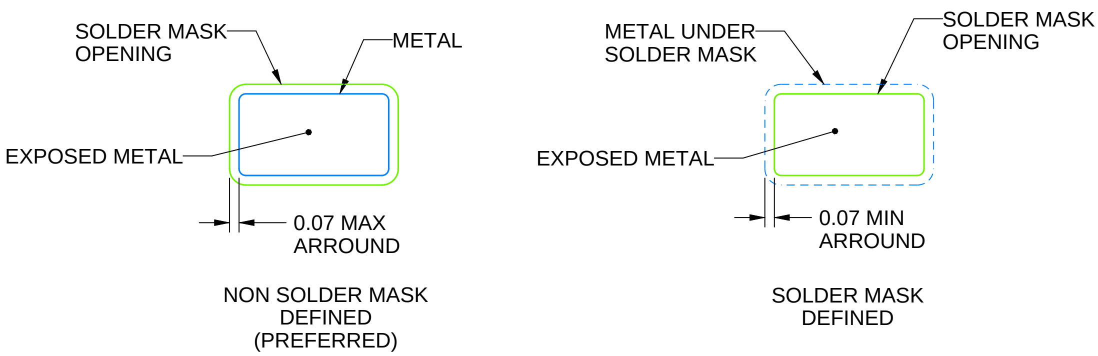


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

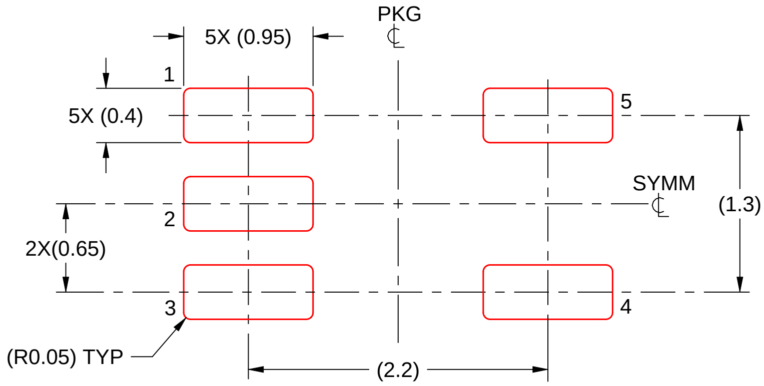


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

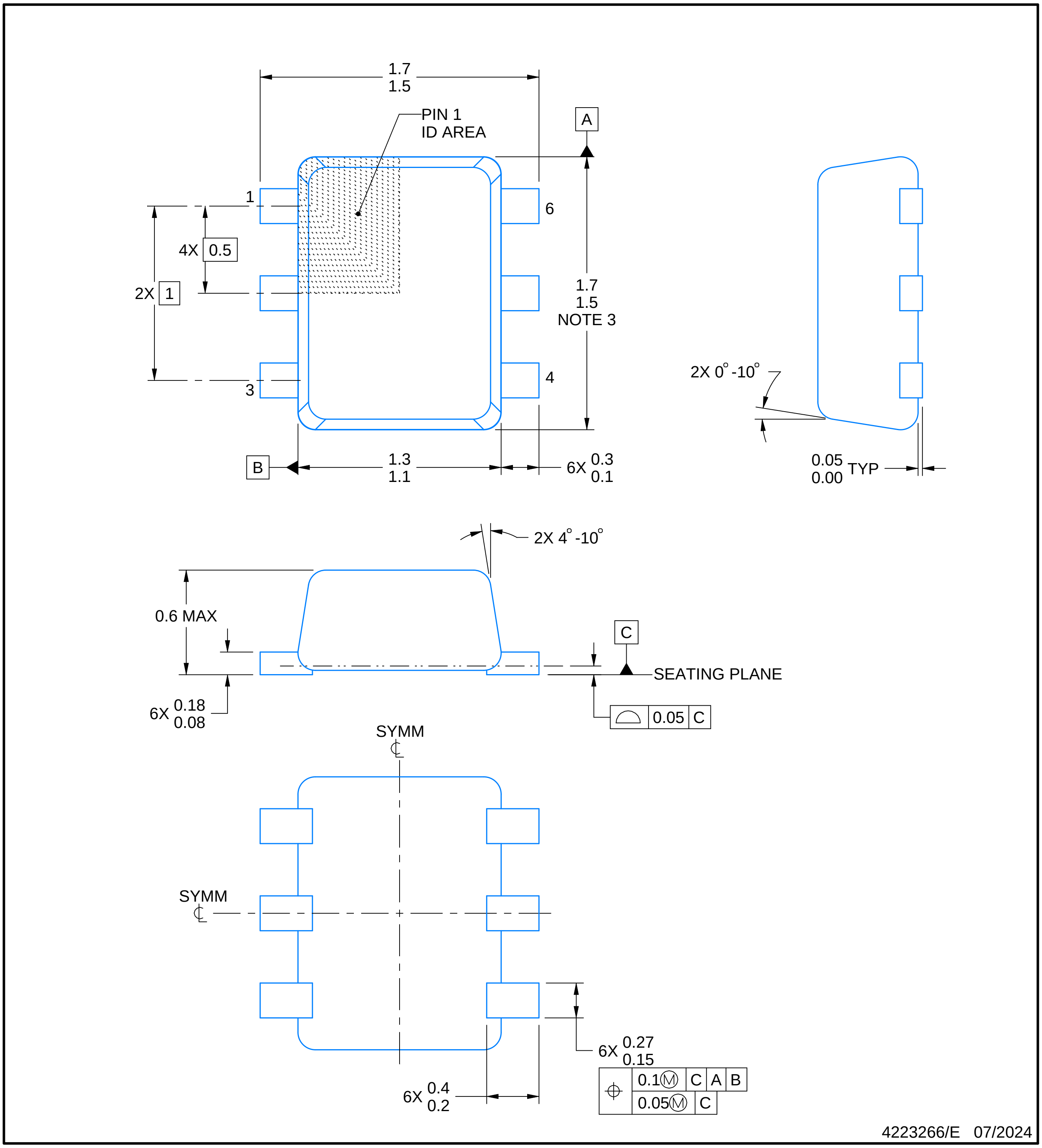


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

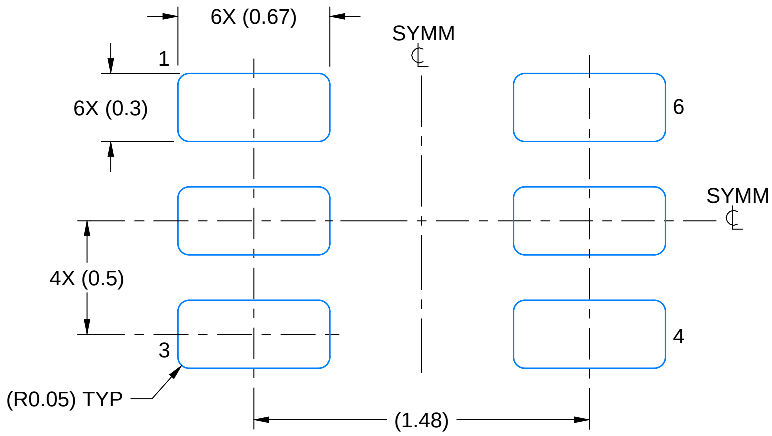
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



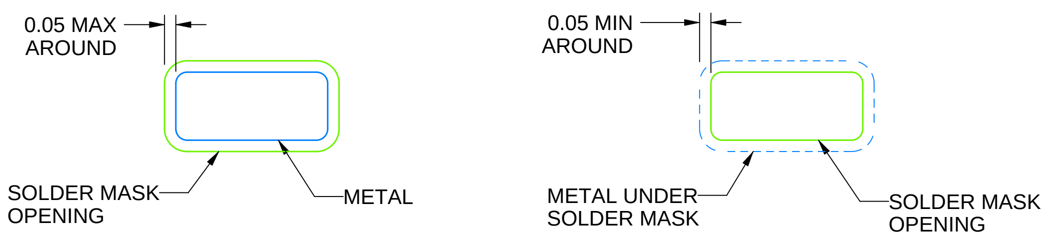
4223266/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

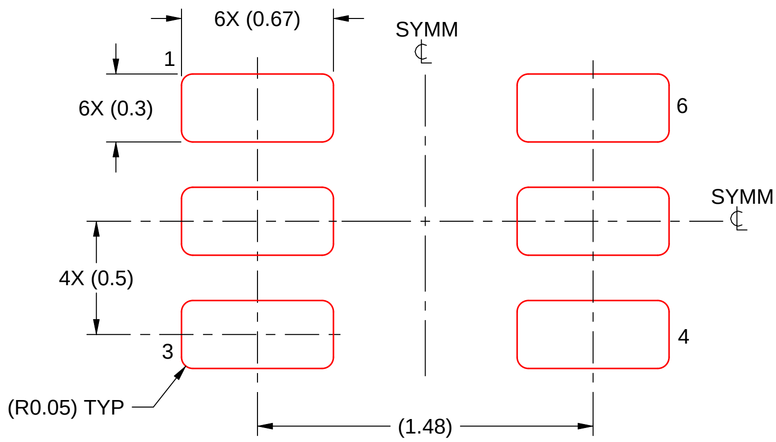
SOLDER MASK
DEFINED

SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.