

# TMUX582F-SEP 宇宙用強化プラスチックに封止した可変フォルト スレッシュホルド付き、 $\pm 60V$ 保護、ラッチアップ耐性、8 : 1 マルチプレクサ

## 1 特長

- 放射線耐性を強化
- シングル イベント ラッチアップ (SEL) 耐性:  $125^{\circ}\text{C}$  で  $43\text{MeV}\cdot\text{cm}^2/\text{mg}$  まで
- $30\text{krad}(\text{Si})$  まで ELDRS フリー
- すべてのウェハー ロットについて、 $20\text{krad}(\text{Si})$  までの吸収線量 (TID) RLAT
- $30\text{krad}(\text{Si})$  まで吸収線量 (TID) 特性を評価済み
- 宇宙向け強化プラスチック
- 電源電圧範囲:  $8V\sim 22V$  または  $\pm 5V\sim \pm 16.5V$
- 電源オフおよび過電圧保護を内蔵<sup>1</sup>
  - ソースと電源間、またはドレイン間で最大  $85V$  の過電圧耐性
  - 最大  $\pm 60V$  の過電圧および電源オフ
  - 最大  $\pm 60V$  のコールド スペアに対応
  - 障害スレッシュホルド ( $V_{fp}$  および  $V_{fn}$ ) を  $5V$  から電源に調整可能
  - 障害が発生したチャンネルを示す割り込みフラグ フィードバック
  - 障害が発生していないチャンネルは低リーク電流で動作を維持
- ラッチアップ耐性構造
- $100\text{pA}$  の標準的なリーク電流、 $3.5\text{pF}$  の静電容量、 $1\%$  の  $R_{on}$  平坦度で高精度を実現
- 動作温度範囲:  $-55^{\circ}\text{C}\sim +125^{\circ}\text{C}$
- 管理されたベースライン
- 金ワイヤ、NiPdAu リード仕上げ
- 単一のアセンブリ/テスト施設
- 単一の製造施設
- 長期にわたる製品ライフ サイクル
- 製品のトレーサビリティ
- モールド コンパウンドの改良による低いガス放出
- 小型で業界標準の TSSOP-20 パッケージ

## 2 アプリケーション

- 低軌道 (LEO) 衛星用途
- リモート インターフェイス ユニット (RIU)
- リモート テレメトリ ユニット (RTU)
- 宇宙のシステム監視
- ラッチアップおよび過電圧検出
- パワーアップ シーケンシング保護
- オンボード データ処理用の衛星テレメトリおよびテレコマンド

<sup>1</sup> このマルチプレクサのアプリケーション シナリオは、通常の動作条件において最大電源電圧でバイアスが印加されることを想定しており、そのように照射されます。デバイスは、障害保護が正常であるかどうかを判定するために事後テストされます。詳細については、バイアス方式の放射線レポートを参照してください。

- センサ データ アクイジション

## 3 概要

TMUX582F-SEP は、最新の 8 : 1 マルチプレクサで、シングルエンドと差動の両方の動作に適しています。このラッチアップ耐性デバイスは、最大  $\pm 60V$  の堅牢な過電圧保護を実現し、過酷な宇宙環境に最適です。さらに、この保護機能は電源オン、電源オフ、フローティングの各電源条件でも動作します。

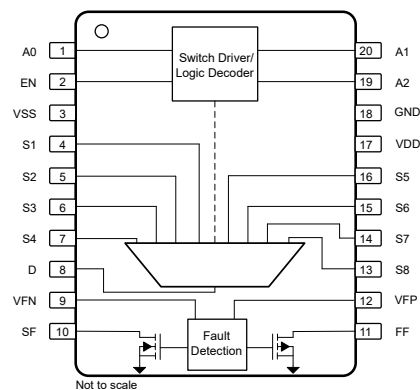
過電圧または低電圧イベントなどの障害が発生すると、問題のチャンネルがオフになり、 $S_x$  ピンは高インピーダンスになります。この障害が発生しているチャンネルを選択すると、ドレイン (D) が超過したフォルト レール ( $V_{fp}$  または  $V_{fn}$ ) にプルされます。障害が発生していない他のすべての  $S_x$  ピンは、引き続き正常に動作します。通常動作時、ソース ( $S_x$ ) が  $V_{fp}$  または  $V_{fn}$  を超えない場合、スイッチは低リーク、低静電容量、超フラットなオン抵抗で動作します。これにより、最小限の歪みで高性能のシグナル インテグリティを実現できます。

TMUX582F-SEP は、システム監視から電源オン シーケンス保護、高精度のフロント エンド データ アクイジションに至るまで、ほぼすべてのアプリケーションに対応できる柔軟性を備えた、障害保護機能搭載の CMOS マルチプレクサです。

### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TMUX582F-SEP	PW (TSSOP, 20)	6.5mm × 6.4mm

- 詳細については、[セクション 12](#) を参照してください。
- パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



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## 4 Pin Configuration and Functions

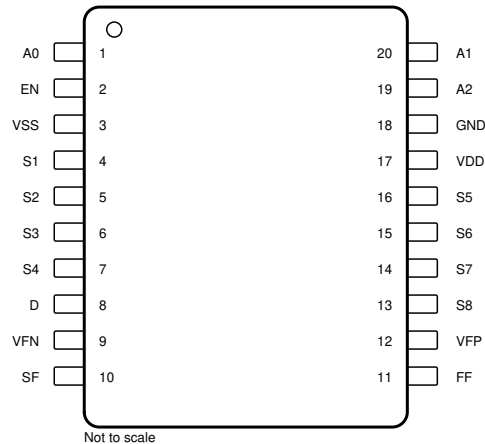


図 4-1. PW Package, 20-Pin TSSOP (Top View)

表 4-1. Pin Functions: TMUX582F-SEP

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A0	1	I	Logic control input address 0 (A0). The pin has a weak internal pull-down. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault.
EN	2	I	Active high digital enable (EN) pin. The pin has a weak internal pull-down. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V <sub>SS</sub>	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V <sub>SS</sub> and GND.
S1	4	I/O	Overvoltage protected source pin 1. Can be an input or output.
S2	5	I/O	Overvoltage protected source pin 2. Can be an input or output.
S3	6	I/O	Overvoltage protected source pin 3. Can be an input or output.
S4	7	I/O	Overvoltage protected source pin 4. Can be an input or output.
D	8	I/O	Drain pin. Can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
V <sub>FN</sub>	9	P	Negative fault voltage supply that determines the overvoltage protection triggering threshold on the negative side. Connect to V <sub>SS</sub> if the triggering threshold is to be the same as the device's negative supply. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V <sub>FN</sub> and GND.
SF	10	O	Specific fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on a specific pin, depending on the state of A0, A1, and A2, as shown in 表 7-1. Connect this pin to an external supply (1.8V to 5.5V) through a 1kΩ pull-up resistor.
FF	11	O	General fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on any of the source (Sx) input pins. Connect this pin to an external supply (1.8V to 5.5V) through a 1kΩ pull-up resistor.
V <sub>FP</sub>	12	P	Positive fault voltage supply that determines the overvoltage protection triggering threshold on the positive side. Connect to V <sub>DD</sub> if the triggering threshold is to be the same as the device's positive supply. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V <sub>FP</sub> and GND.
S8	13	I/O	Overvoltage protected source pin 8. Can be an input or output.
S7	14	I/O	Overvoltage protected source pin 7. Can be an input or output.
S6	15	I/O	Overvoltage protected source pin 6. Can be an input or output.
S5	16	I/O	Overvoltage protected source pin 5. Can be an input or output.
V <sub>DD</sub>	17	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V <sub>DD</sub> and GND.
GND	18	P	Ground (0V) reference
A2	19	I	Logic control input address 2 (A2). The pin has a weak internal pull-down. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault.

表 4-1. Pin Functions: TMUX582F-SEP (続き)

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A1	20	I	Logic control input address 1 (A1). The pin has a weak internal pull-down. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault.

(1) I = input, O = output, I/O = input and output, P = power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub> to V <sub>SS</sub>			38	V
V <sub>DD</sub> to GND	Supply voltage	-0.3	28	V
V <sub>SS</sub> to GND		-18	0.3	V
V <sub>FP</sub> to GND	Positive fault clamping voltage	-0.3	V <sub>DD</sub> + 0.3	V
V <sub>FN</sub> to GND	Negative fault clamping voltage	V <sub>SS</sub> - 0.3	0.3	V
V <sub>S</sub> to GND	Source input pin (Sx) voltage to GND	-65	65	V
V <sub>S</sub> to V <sub>DD</sub>	Source input pin (Sx) voltage to V <sub>DD</sub>	-90		V
V <sub>S</sub> to V <sub>SS</sub>	Source input pin (Sx) voltage to V <sub>SS</sub>		90	V
V <sub>D</sub>	Drain pin (D or Dx) voltage	V <sub>FN</sub> -0.7	V <sub>FP</sub> +0.7	V
V <sub>SEL</sub> or V <sub>EN</sub>	Logic control input pin voltage (EN, A0, A1, A2) <sup>(2)</sup>	GND - 0.7	48	V
V <sub>DIG_OUT</sub>	Digital output pin (SF, FF) voltage <sup>(2)</sup>	GND - 0.7	6	V
I <sub>SEL</sub> or I <sub>EN</sub>	Logic control input pin current (EN, A0, A1, A2) <sup>(2)</sup>	-30	30	mA
I <sub>DIG_OUT</sub>	Digital output pin (SF, FF) current <sup>(2)</sup>	-10	10	mA
I <sub>S</sub> or I <sub>D</sub> (CONT)	Source or drain continuous current (Sx or D)	I <sub>DC</sub> ± 10 % <sup>(3)</sup>	I <sub>DC</sub> ± 10 % <sup>(3)</sup>	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C
T <sub>A</sub>	Ambient temperature	-55	150	°C
T <sub>J</sub>	Junction temperature		150	°C
P <sub>tot</sub> <sup>(4)</sup>	Total power dissipation		800	mW

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Stresses have to be kept at or below both voltage and current ratings at all time.
- (3) Refer to Recommended Operating Conditions for I<sub>DC</sub> ratings.
- (4) P<sub>tot</sub> derates linearly above T<sub>A</sub> = 70°C by 12.0 mW/°C

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub> - V <sub>SS</sub> <sup>(1)</sup>	Power supply voltage differential	8		33	V
V <sub>DD</sub>	Positive power supply voltage	5		22	V
V <sub>FP</sub>	Positive fault clamping voltage	3		V <sub>DD</sub>	V
V <sub>FN</sub>	Negative fault clamping voltage	V <sub>SS</sub>		0	V
V <sub>S</sub>	Source pin (Sx) voltage (non-fault condition)	V <sub>FN</sub>		V <sub>FP</sub>	V
V <sub>S_FAULT</sub> <sup>(3)</sup>	Source pin (Sx) voltage (fault condition)	-60		60	V

### 5.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_S$ to $V_{DD}$ <sup>(2)</sup>	Source pin (Sx) voltage to $V_{DD}$ or $V_D$ (fault condition)	Source pin (Sx) voltage to $V_{DD}$ or $V_D$ (fault condition)	-85			V
$V_S$ to $V_{SS}$ <sup>(2)</sup>	Source pin (Sx) voltage to $V_{SS}$ or $V_D$ (fault condition)	Source pin (Sx) voltage to $V_{SS}$ or $V_D$ (fault condition)			85	V
$V_D$	Drain pin (D, Dx) voltage		$V_{FN}$		$V_{FP}$	V
$V_{SEL}$ of $V_{EN}$	Logic control input pin voltage (EN, A0, A1, A2)		0		22	V
$V_{DIG\_OUT}$	Digital output pin (SF, FF) voltage		0		5.5	V
$T_A$	Ambient temperature		-55		125	°C
IDC <sup>(3)</sup>	Continuous current through switch, TSSOP package	$T_A = 25^\circ\text{C}$			9	mA
		$T_A = 85^\circ\text{C}$			6.5	mA
		$T_A = 150^\circ\text{C}$			5	mA

(1)  $V_{DD}$  and  $V_{SS}$  can be any value as long as  $8\text{V} \leq (V_{DD} - V_{SS}) \leq 33\text{V}$ .

(2) Under a fault condition, the potential difference between source pin (Sx) and supply pins ( $V_{DD}$  and  $V_{SS}$ .) or source pin (Sx) and drain pins (D, Dx) may not exceed 85V.

(3) Fault supplies are tied to the primary supplies ( $V_{FP} = V_{DD}$ ,  $V_{FN} = V_{SS}$ )

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMUX582F-SEP	UNIT
		PW (TSSOP)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	36.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Electrical Characteristics (Global)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$V_T$	Threshold voltage for fault detector		-55°C to +125°C		0.7		V
<b>DIGITAL INPUT/ OUTPUT</b>							
$V_{IH}$	High-level input voltage	EN, Ax pins	-55°C to +125°C	1.3		22	V
$V_{IL}$	Low-level input voltage	EN, Ax pins	-55°C to +125°C	0		0.8	V
$V_{OL(FLAG)}$	Low-level output voltage	FF and SF pins, $I_O = 5\text{mA}$	-55°C to +125°C		0.1		V
<b>POWER SUPPLY</b>							
$V_{UVLO}$	Undervoltage lockout (UVLO) threshold voltage ( $V_{DD} - V_{SS}$ )	single supply configuration only	-55°C to +125°C		6		V
$R_{D(OVP)}$	Drain resistance to fault rail during overvoltage event on selected source pin		25°C		40		kΩ

## 5.6 Dual Supply: Electrical Characteristics

$V_{DD} = +15V \pm 10\%$ ,  $V_{SS} = -15V \pm 10\%$ , GND = 0V (unless otherwise noted)  
Typical at  $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = -10V$ to $+10V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	180			$\Omega$
			$-55^\circ C$ to $+125^\circ C$	400			
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = -10V$ to $+10V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	2.5			$\Omega$
			$-55^\circ C$ to $+125^\circ C$	13			
$R_{FLAT}$	On-resistance flatness	$V_S = -10V$ to $+10V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	1.5			$\Omega$
			$-55^\circ C$ to $+125^\circ C$	4			
$R_{ON\_DRIFT}$	On-resistance drift	$V_S = 0V$ , $I_S = -1mA$	$-55^\circ C$ to $+125^\circ C$	1.2			$\Omega/^\circ C$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	Switch state is off, $V_S = +10V/-10V$ , $V_D = -10V/+10V$ , $V_{DD} = 16.5V$ , $V_{SS} = -16.5V$	$-55^\circ C$ to $+25^\circ C$	-1	0.1	1	nA
			$-55^\circ C$ to $+125^\circ C$	-4.5		4.5	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	Switch state is off, $V_S = +10V/-10V$ , $V_D = -10V/+10V$ , $V_{DD} = 16.5V$ , $V_{SS} = -16.5V$	$-55^\circ C$ to $+25^\circ C$	-1	0.1	1	nA
			$-55^\circ C$ to $+125^\circ C$	-15		15	
$I_{S(ON)}, I_{D(ON)}$	Channel on leakage current	Switch state is on, $V_S =$ floating, $V_D = -10V/+10V$ , or $V_S = -10V/+10V$ , $V_D =$ floating, $V_{DD} = 16.5V$ , $V_{SS} = -16.5V$	$-55^\circ C$ to $+25^\circ C$	-1.5	0.3	1.5	nA
			$-55^\circ C$ to $+125^\circ C$	-23		23	
<b>FAULT CONDITION</b>							
$I_{S(FA)}$	Input leakage current during overvoltage	$V_S = \pm 60V$ , GND = 0V, $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$	$-55^\circ C$ to $+125^\circ C$	$\pm 110$			$\mu A$
	Input leakage current during overvoltage with grounded supplies	$V_S = \pm 60V$ , GND = 0V, $V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0V$ , $V_{EN} = V_{AX} = 0V$ or floating		$\pm 135$			
	Input leakage current during overvoltage with floating supplies	$V_S = \pm 60V$ , GND = 0V, $V_{DD} = V_{SS} = V_{FP} = V_{FN} =$ floating, $V_{EN} = V_{AX} = 0V$ or floating		$\pm 135$			
$I_{D(FA)}$	Output leakage current during overvoltage	$V_S = \pm 60V$ , GND = 0V, $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$	$-55^\circ C$ to $+25^\circ C$	$\pm 10$			nA
			$-55^\circ C$ to $+125^\circ C$	-150		150	
	Output leakage current during overvoltage with grounded supplies	$V_S = \pm 60V$ , GND = 0V, $V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0V$ , $V_{EN} = V_{AX} = 0V$ or floating	$-55^\circ C$ to $+25^\circ C$	-50	$\pm 1$	50	
			$-55^\circ C$ to $+125^\circ C$	-550		550	
Output leakage current during overvoltage with floating supplies	$V_S = \pm 60V$ , GND = 0V, $V_{DD} = V_{SS} = V_{FP} = V_{FN} =$ floating, $V_{EN} = V_{AX} = 0V$ or floating	$-55^\circ C$ to $+25^\circ C$	$\pm 3$			$\mu A$	
		$-55^\circ C$ to $+125^\circ C$	$\pm 8$				
<b>DIGITAL INPUT/ OUTPUT</b>							
$I_{IH}$	High-level input current	$V_{EN} = V_{AX} = V_{DD}$	$-55^\circ C$ to $+125^\circ C$	-2.5	$\pm 0.6$	2.5	$\mu A$
$I_{IL}$	Low-level input current	$V_{EN} = V_{AX} = 0V$	$-55^\circ C$ to $+125^\circ C$	-1.5	$\pm 0.6$	1.5	$\mu A$
<b>SWITCHING CHARACTERISTICS</b>							
$t_{ON(EN)}$	Enable turn-on time	$V_S = 10V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+25^\circ C$	175			ns
			$-55^\circ C$ to $+125^\circ C$	290			
$t_{OFF(EN)}$	Enable turn-off time	$V_S = 10V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+25^\circ C$	350			ns
			$-55^\circ C$ to $+125^\circ C$	400			
$t_{TRAN}$	Transition time	$V_S = 10V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+25^\circ C$	180			ns
			$-55^\circ C$ to $+125^\circ C$	250			
$t_{BBM}$	Break-before-make time delay	$V_S = 10V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+125^\circ C$	120			ns
$t_{RESPONSE}$	Fault response time	$V_{FP} = 10V$ , $V_{FN} = -10V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+125^\circ C$	300			ns
$t_{RECOVERY}$	Fault recovery time	$V_{FP} = 10V$ , $V_{FN} = -10V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+125^\circ C$	1.5			$\mu s$
$t_{RESPONSE(FLAG)}$	Fault flag response time	$V_{FP} = 10V$ , $V_{FN} = -10V$ , $V_{PU} = 5V$ , $R_{PU} = 1k\Omega$ , $C_L = 12pF$	$25^\circ C$	120			ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	$V_{FP} = 10V$ , $V_{FN} = -10V$ , $V_{PU} = 5V$ , $R_{PU} = 1k\Omega$ , $C_L = 12pF$	$25^\circ C$	1			$\mu s$

### 5.6 Dual Supply: Electrical Characteristics (続き)

$V_{DD} = +15V \pm 10\%$ ,  $V_{SS} = -15V \pm 10\%$ , GND = 0V (unless otherwise noted)

Typical at  $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$Q_{INJ}$	Charge injection	$V_S = 0V$ , $C_L = 1nF$ , $R_S = 0\Omega$	$25^\circ C$		-15		pC
$O_{ISO}$	Off-isolation	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 0V$ , $f = 1MHz$	$25^\circ C$		-80		dB
$X_{TALK}$	Intra-channel crosstalk	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 0V$ , $f = 1MHz$	$25^\circ C$		-95		dB
BW	-3 dB bandwidth	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 0V$	$25^\circ C$		150		MHz
$I_{LOSS}$	Insertion loss	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 0V$ , $f = 1MHz$	$25^\circ C$		-9		dB
THD+N	Total harmonic distortion plus noise	$R_S = 40\Omega$ , $R_L = 10k\Omega$ , $V_S = 15V_{PP}$ , $V_{BIAS} = 0V$ , $f = 20Hz$ to $20kHz$	$25^\circ C$		0.0015		%
$C_{S(OFF)}$	Input off-capacitance	$f = 1MHz$ , $V_S = 0V$	$25^\circ C$		3.5		pF
$C_{D(OFF)}$	Output off-capacitance	$f = 1MHz$ , $V_S = 0V$	$25^\circ C$		28		pF
$C_{S(ON)}$ , $C_{D(ON)}$	Input/Output on-capacitance	$f = 1MHz$ , $V_S = 0V$	$25^\circ C$		30		pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$ , $V_S = 0V$	$25^\circ C$		0.25		mA
			$-55^\circ C$ to $+125^\circ C$			0.6	
$I_{SS}$	$V_{SS}$ supply current	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$ , $V_S = 0V$	$25^\circ C$		0.15		mA
			$-55^\circ C$ to $+125^\circ C$			0.5	
$I_{GND}$	GND current	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$ , $V_S = 0V$	$25^\circ C$		0.075		mA
$I_{FP}$	$V_{FP}$ supply current	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$ , $V_S = 0V$	$25^\circ C$		10		$\mu A$
$I_{FN}$	$V_{FN}$ supply current	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$ , $V_S = 0V$	$25^\circ C$		10		$\mu A$
$I_{DD(FA)}$	$V_{DD}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$	$25^\circ C$		0.25		mA
			$-55^\circ C$ to $+125^\circ C$			1.25	
$I_{SS(FA)}$	$V_{SS}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$	$25^\circ C$		0.15		mA
			$-55^\circ C$ to $+125^\circ C$			0.75	
$I_{GND(FA)}$	GND current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$	$25^\circ C$		0.2		mA
$I_{FP(FA)}$	$V_{FP}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$	$25^\circ C$		20		$\mu A$
$I_{FN(FA)}$	$V_{FN}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 5V$ or $V_{DD}$	$25^\circ C$		20		$\mu A$
$I_{DD(DISABLE)}$	$V_{DD}$ supply current (disable mode)	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 0V$ , $V_S = 0V$	$25^\circ C$		0.15		mA
			$-55^\circ C$ to $+125^\circ C$			0.6	
$I_{SS(DISABLE)}$	$V_{SS}$ supply current (disable mode)	$V_{DD} = V_{FP} = 16.5V$ , $V_{SS} = V_{FN} = -16.5V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 0V$ , $V_S = 0V$	$25^\circ C$		0.1		mA
			$-55^\circ C$ to $+125^\circ C$			0.5	

(1) When  $V_S$  is positive,  $V_D$  is negative, and vice versa.



## 5.7 Single Supply: Electrical Characteristics

$V_{DD} = +12V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $GND = 0V$  (unless otherwise noted)  
Typical at  $V_{DD} = +12V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0V$ to $7.8V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	180			$\Omega$
			$-55^\circ C$ to $+125^\circ C$	400			
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = 0V$ to $7.8V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	2.5			$\Omega$
			$-55^\circ C$ to $+125^\circ C$	13			
$R_{FLAT}$	On-resistance flatness	$V_S = 0V$ to $7.8V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	7			$\Omega$
$R_{FLAT}$	On-resistance flatness	$V_S = 0V$ to $7.8V$ , $I_S = -1mA$	$-55^\circ C$ to $+125^\circ C$	80			$\Omega$
$R_{FLAT}$	On-resistance flatness	$V_S = 1V$ to $7.8V$ , $I_S = -1mA$	$-55^\circ C$ to $+25^\circ C$	1.5			$\Omega$
			$-55^\circ C$ to $+125^\circ C$	8			
$R_{ON\_DRIFT}$	On-resistance drift	$V_S = 6V$ , $I_S = -1mA$	$-55^\circ C$ to $+125^\circ C$	1.2			$\Omega/^\circ C$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	Switch state is off, $V_S = 1V/10V$ , $V_D = 10V/1V$ , $V_{DD} = 13.2V$	$-55^\circ C$ to $+25^\circ C$	-1	0.1	1	nA
			$-55^\circ C$ to $+125^\circ C$	-4.5		4.5	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	Switch state is off, $V_S = 1V/10V$ , $V_D = 10V/1V$ , $V_{DD} = 13.2V$	$-55^\circ C$ to $+25^\circ C$	-1	0.1	1	nA
			$-55^\circ C$ to $+125^\circ C$	-15		15	
$I_{S(ON)}, I_{D(ON)}$	Channel on leakage current	Switch state is on, $V_S =$ floating, $V_D = 1V/10V$ , $V_{DD} = 13.2$	$-55^\circ C$ to $+25^\circ C$	-1.5	0.3	1.5	nA
			$-55^\circ C$ to $+125^\circ C$	-23		23	
<b>FAULT CONDITION</b>							
$I_{S(FA)}$	Input leakage current during overvoltage	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$	$-55^\circ C$ to $+125^\circ C$	$\pm 145$			$\mu A$
	Input leakage current during overvoltage with grounded supplies	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0V$ , $V_{EN} = V_{Ax} = 0V$ or floating		$\pm 135$			
	Input leakage current during overvoltage with floating supplies	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} =$ floating, $V_{EN} = V_{Ax} = 0V$ or floating		$\pm 135$			
$I_{D(FA)}$	Output leakage current during overvoltage	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$	$-55^\circ C$ to $+25^\circ C$	$\pm 10$			nA
	Output leakage current during overvoltage with grounded supplies	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0V$ , $V_{EN} = V_{Ax} = 0V$ or floating	$-55^\circ C$ to $+125^\circ C$	-100		100	
	Output leakage current during overvoltage with floating supplies	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} =$ floating, $V_{EN} = V_{Ax} = 0V$ or floating	$-55^\circ C$ to $+125^\circ C$	-50	$\pm 1$	50	
	Output leakage current during overvoltage with floating supplies	$V_S = \pm 60V$ , $GND = 0V$ , $V_{DD} = V_{SS} = V_{FP} = V_{FN} =$ floating, $V_{EN} = V_{Ax} = 0V$ or floating	$-55^\circ C$ to $+125^\circ C$	$\pm 3$			$\mu A$
			$-55^\circ C$ to $+125^\circ C$	$\pm 8$			
<b>DIGITAL INPUT/ OUTPUT</b>							
$I_{IH}$	High-level input current	$V_{EN} = V_{Ax} = V_{DD}$	$-55^\circ C$ to $+125^\circ C$	-2.5	$\pm 0.6$	2.5	$\mu A$
$I_{IL}$	Low-level input current	$V_{EN} = V_{Ax} = 0V$	$-55^\circ C$ to $+125^\circ C$	-1.5	$\pm 0.6$	1.5	$\mu A$
<b>SWITCHING CHARACTERISTICS</b>							
$t_{ON(EN)}$	Enable turn-on time	$V_S = 8V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+25^\circ C$	160			ns
			$-55^\circ C$ to $+125^\circ C$	300			
$t_{OFF(EN)}$	Enable turn-off time	$V_S = 8V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+25^\circ C$	420			ns
			$-55^\circ C$ to $+125^\circ C$	500			
$t_{TRAN}$	Transition time	$V_S = 8V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+25^\circ C$	160			ns
			$-55^\circ C$ to $+125^\circ C$	240			
$t_{BBM}$	Break-before-make time delay	$V_S = 8V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+125^\circ C$	90			ns
$t_{RESPONSE}$	Fault response time	$V_{FP} = 8V$ , $V_{FN} = 0V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+125^\circ C$	225			ns
$t_{RECOVERY}$	Fault recovery time	$V_{FP} = 8V$ , $V_{FN} = 0V$ , $R_L = 4k\Omega$ , $C_L = 12pF$	$-55^\circ C$ to $+125^\circ C$	0.75			$\mu s$
$t_{RESPONSE(FLAG)}$	Fault flag response time	$V_{FP} = 8V$ , $V_{FN} = 0V$ , $V_{PU} = 5V$ , $R_{PU} = 1k\Omega$ , $C_L = 12pF$	$25^\circ C$	120			ns

### 5.7 Single Supply: Electrical Characteristics (続き)

$V_{DD} = +12V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $GND = 0V$  (unless otherwise noted)

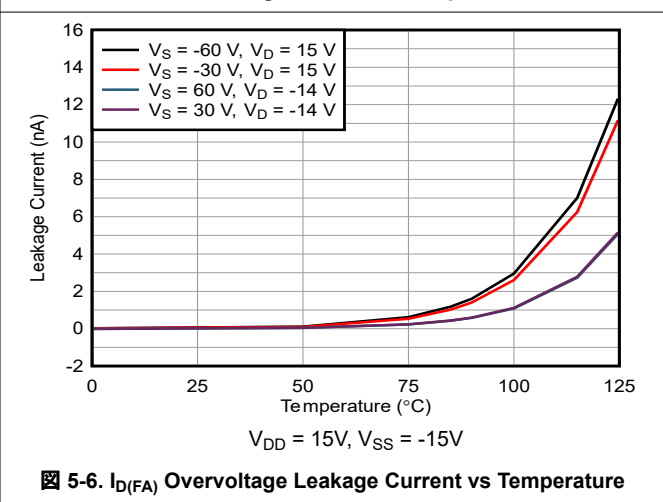
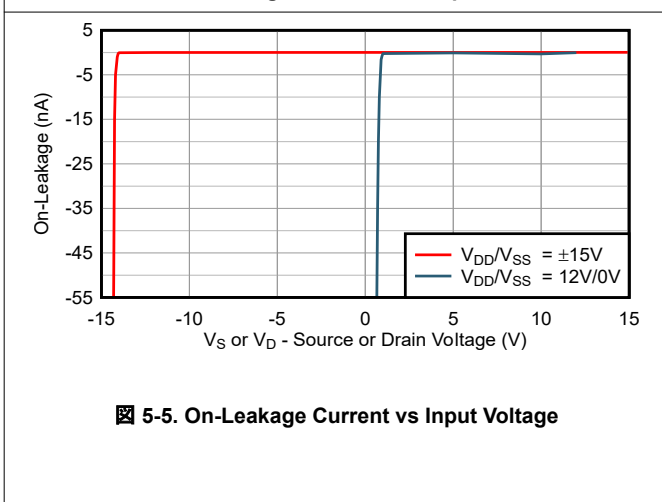
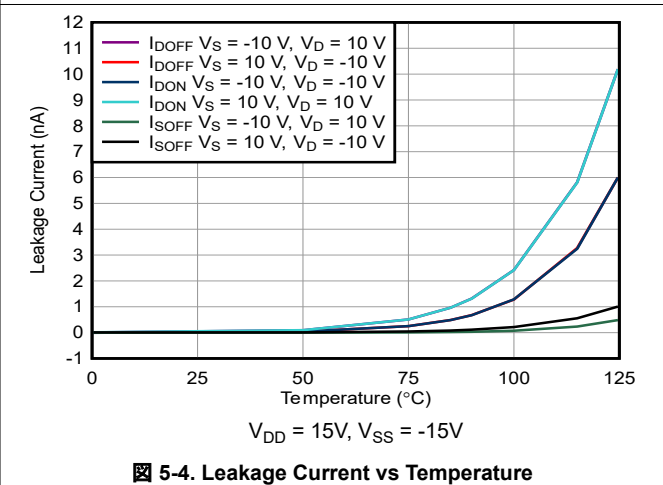
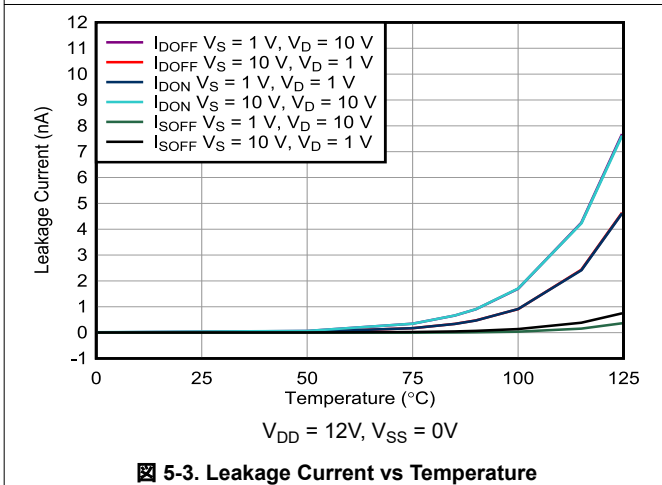
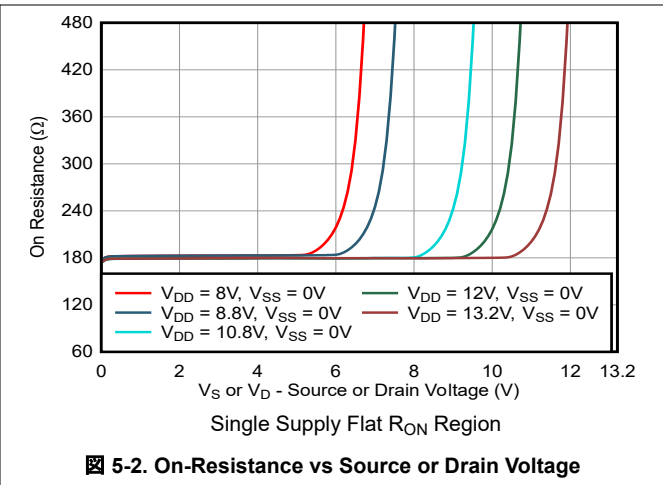
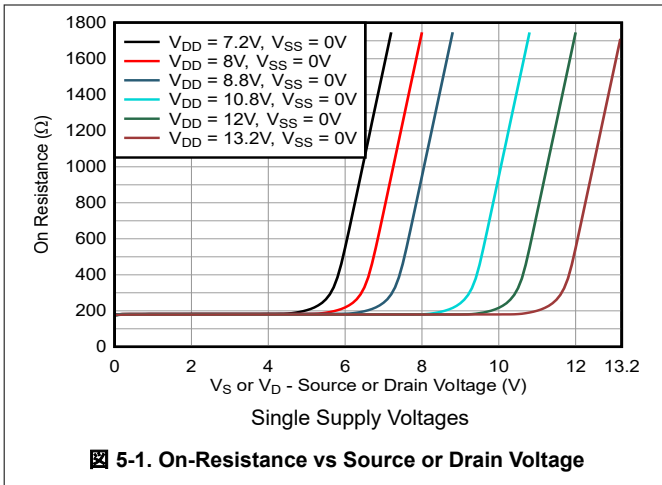
Typical at  $V_{DD} = +12V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	$V_{FP} = 8V$ , $V_{FN} = 0V$ , $V_{PU} = 5V$ , $R_{PU} = 1k\Omega$ , $C_L = 12pF$	$25^\circ C$		0.75		$\mu s$
$Q_{INJ}$	Charge injection	$V_S = 6V$ , $C_L = 1nF$ , $R_S = 0\Omega$	$25^\circ C$		-11		pC
$O_{ISO}$	Off-isolation	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 2V$ , $f = 1MHz$	$25^\circ C$		-75		dB
$X_{TALK}$	Intra-channel crosstalk	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 2V$ , $f = 1MHz$	$25^\circ C$		-90		dB
BW	-3 dB bandwidth	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 2V$ , $f = 1MHz$	$25^\circ C$		130		MHz
$I_{LOSS}$	Insertion loss	$R_S = 50\Omega$ , $R_L = 50\Omega$ , $C_L = 5pF$ , $V_S = 200 mV_{RMS}$ , $V_{BIAS} = 2V$ , $f = 1MHz$	$25^\circ C$		-9		dB
THD+N	Total harmonic distortion plus noise	$R_S = 40\Omega$ , $R_L = 10k\Omega$ , $V_S = 6V_{PP}$ , $V_{BIAS} = 6V$ , $f = 20Hz$ to $20kHz$	$25^\circ C$		0.0025		%
$C_{S(OFF)}$	Input off-capacitance	$f = 1MHz$ , $V_S = 6V$	$25^\circ C$		4		pF
$C_{D(OFF)}$	Output off-capacitance	$f = 1MHz$ , $V_S = 6V$	$25^\circ C$		31		pF
$C_{S(ON)}$ , $C_{D(ON)}$	Input/Output on-capacitance	$f = 1MHz$ , $V_S = 6V$	$25^\circ C$		34		pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/$ $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_S = 6V$	$25^\circ C$		0.25		mA
			$-55^\circ C$ to $+125^\circ C$			0.6	
$I_{SS}$	$V_{SS}$ supply current	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/$ $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_S = 6V$	$25^\circ C$		0.15		mA
			$-55^\circ C$ to $+125^\circ C$			0.5	
$I_{GND}$	GND current	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/$ $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_S = 6V$	$25^\circ C$		0.075		mA
$I_{FP}$	$V_{FP}$ supply current	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/$ $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_S = 6V$	$25^\circ C$		10		$\mu A$
$I_{FN}$	$V_{FN}$ supply current	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/$ $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_S = 6V$	$25^\circ C$		10		$\mu A$
$I_{DD(FA)}$	$V_{DD}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/ V_{AX} = 0V$ , $5V$ , or $V_{DD}$	$25^\circ C$		0.25		mA
			$-55^\circ C$ to $+125^\circ C$			1.25	
$I_{SS(FA)}$	$V_{SS}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/ V_{AX} = 0V$ , $5V$ , or $V_{DD}$	$25^\circ C$		0.15		mA
			$-55^\circ C$ to $+125^\circ C$			0.75	
$I_{GND(FA)}$	GND current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/ V_{AX} = 0V$ , $5V$ , or $V_{DD}$	$25^\circ C$		0.2		mA
$I_{FP(FA)}$	$V_{FP}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/ V_{AX} = 0V$ , $5V$ , or $V_{DD}$	$25^\circ C$		20		$\mu A$
$I_{FN(FA)}$	$V_{FN}$ supply current under fault	$V_S = \pm 60V$ , $V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{EN}/ V_{AX} = 0V$ , $5V$ , or $V_{DD}$	$25^\circ C$		20		$\mu A$
$I_{DD(DISABLE)}$	$V_{DD}$ supply current (disable mode)	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 0V$ , $V_S = 0V$	$25^\circ C$		0.15		mA
			$-55^\circ C$ to $+125^\circ C$			0.6	
$I_{SS(DISABLE)}$	$V_{SS}$ supply current (disable mode)	$V_{DD} = V_{FP} = 13.2V$ , $V_{SS} = V_{FN} = 0V$ , $V_{AX} = 0V$ , $5V$ , or $V_{DD}$ , $V_{EN} = 0V$ , $V_S = 0V$	$25^\circ C$		0.1		mA
			$-55^\circ C$ to $+125^\circ C$			0.5	

(1) When  $V_S$  is positive,  $V_D$  is negative, and vice versa.

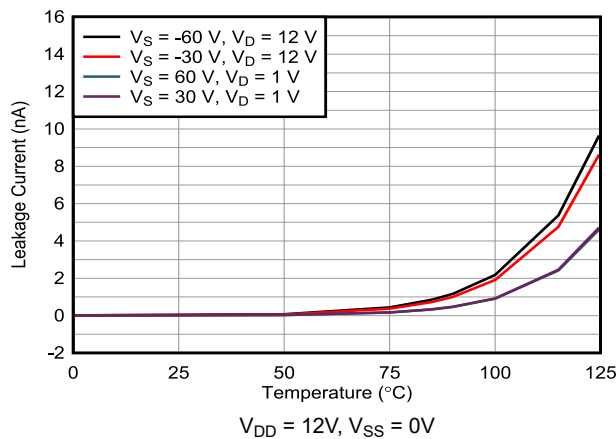
### 5.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 15\text{V}$ , and  $V_{SS} = -15\text{V}$  (unless otherwise noted)

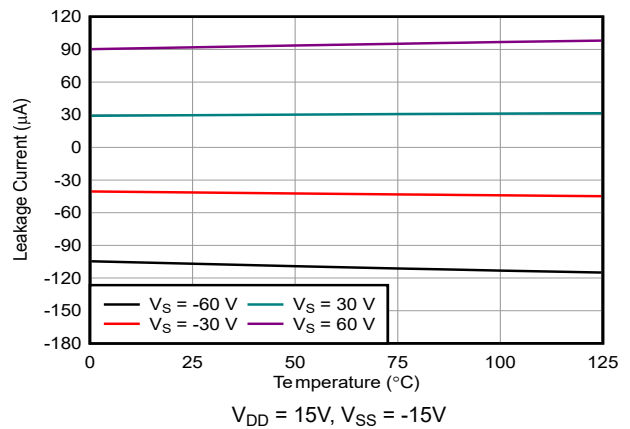


## 5.8 Typical Characteristics (continued)

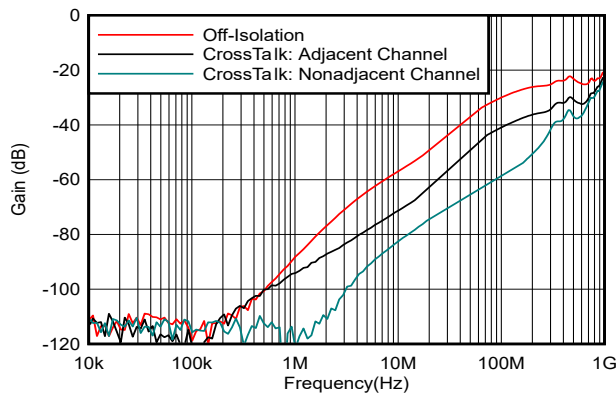
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 15\text{V}$ , and  $V_{SS} = -15\text{V}$  (unless otherwise noted)



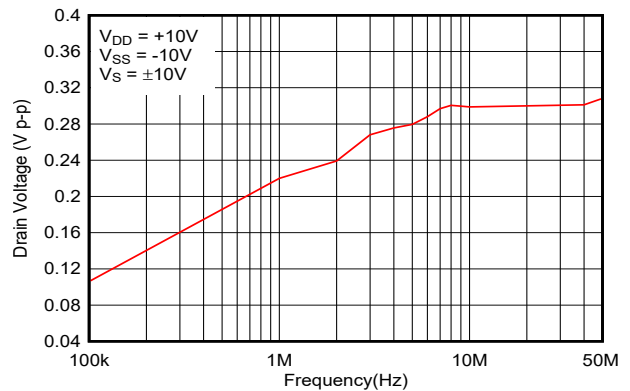
5-7.  $I_{D(FA)}$  Overvoltage Leakage Current vs Temperature



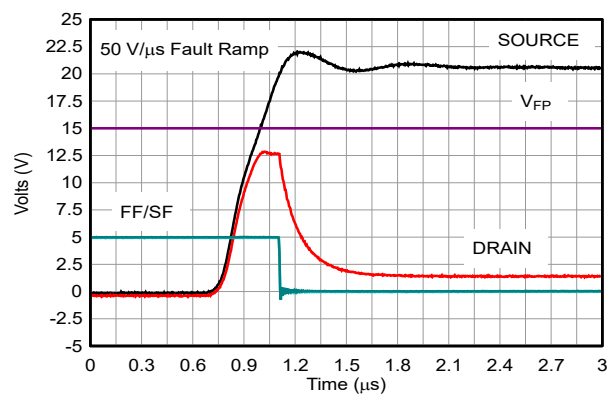
5-8.  $I_{S(FA)}$  Overvoltage Leakage Current vs Temperature



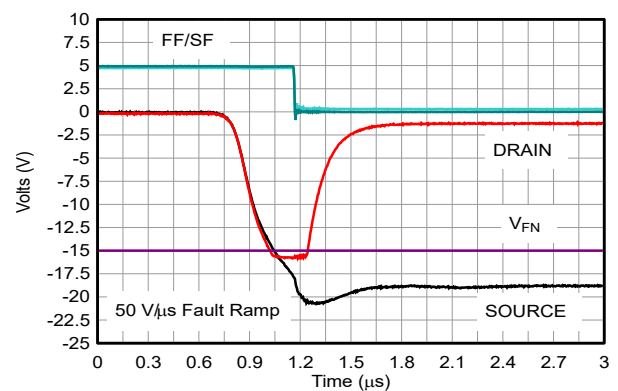
5-9. Off Isolation and Crosstalk vs Frequency



5-10. Large Signal Voltage Off Isolation vs Frequency



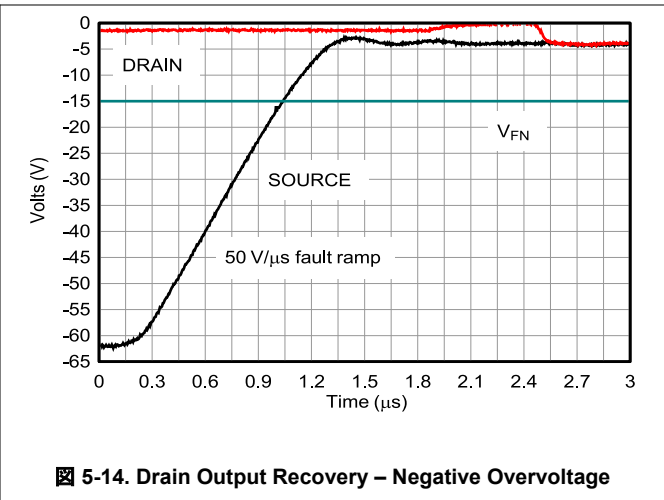
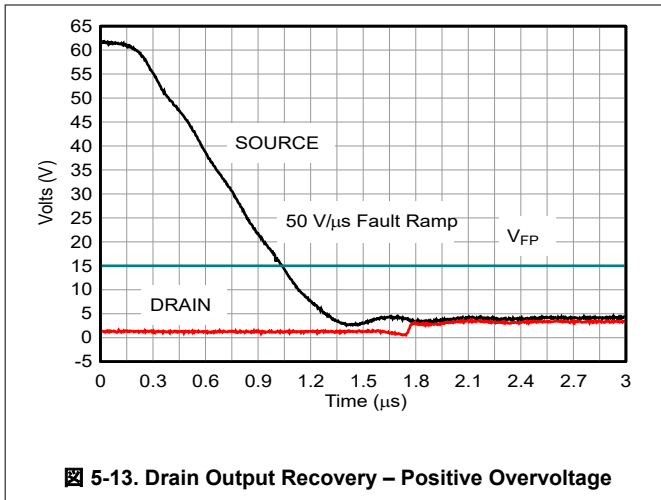
5-11. Drain Output Response – Positive Overvoltage



5-12. Drain Output Response – Negative Overvoltage

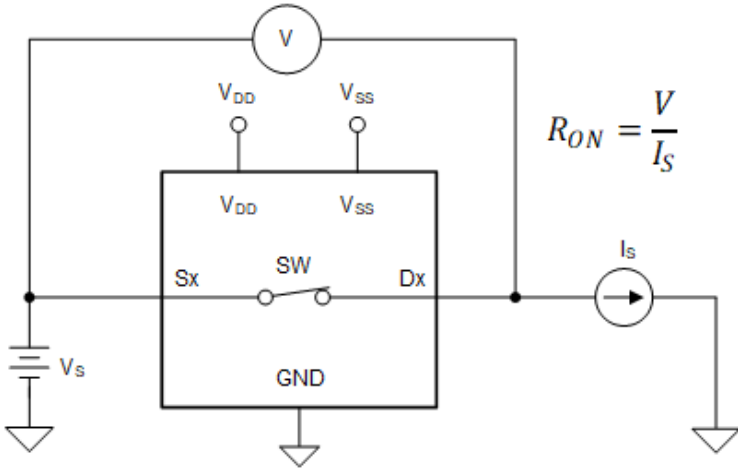
## 5.8 Typical Characteristics (continued)

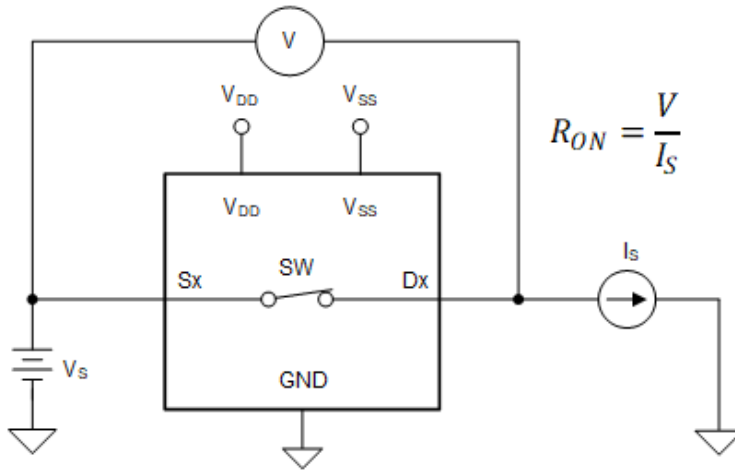
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 15\text{V}$ , and  $V_{SS} = -15\text{V}$  (unless otherwise noted)



## 6 Parameter Measurement Information

### 6.1 On-Resistance

The on-resistance of the TMUX582F-SEP is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol  $R_{ON}$  is used to denote on-resistance. The measurement setup used to measure  $R_{ON}$  is shown in  6-1.  $\Delta R_{ON}$  represents the difference between the  $R_{ON}$  of any two channels, while  $R_{ON\_FLAT}$  denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.




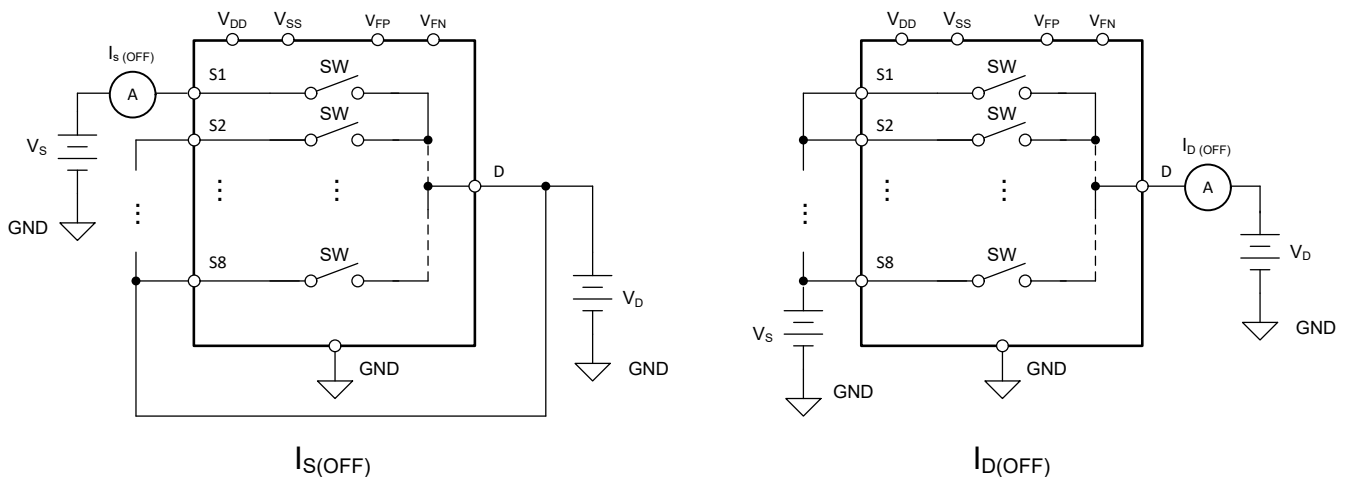
 6-1. On-Resistance Measurement Setup

### 6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

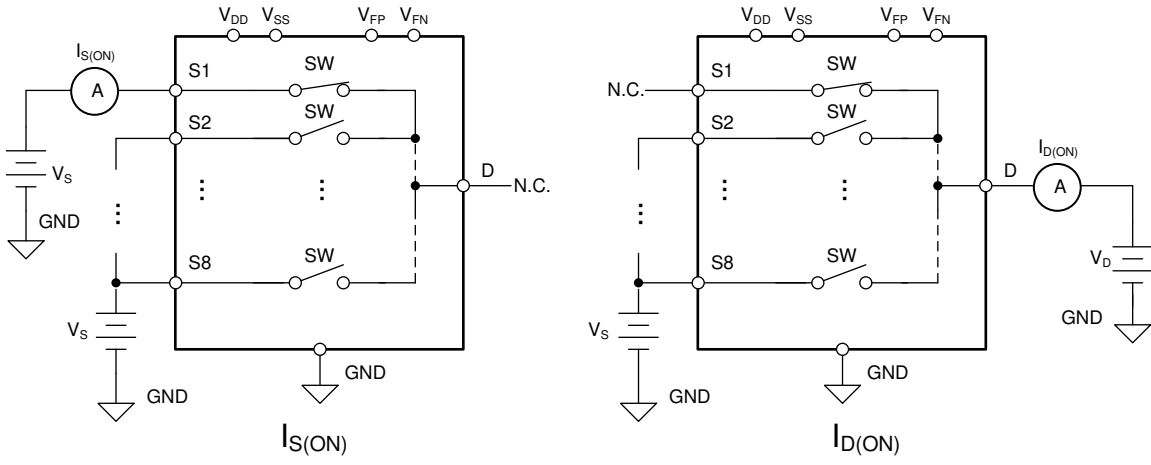
1. Source off-leakage current  $I_{S(OFF)}$ : the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current  $I_{D(OFF)}$ : the leakage current flowing into or out of the drain pin when the switch is off.

 6-2 shows the setup used to measure both off-leakage currents.



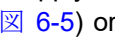
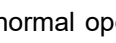
 6-2. Off-Leakage Measurement Setup

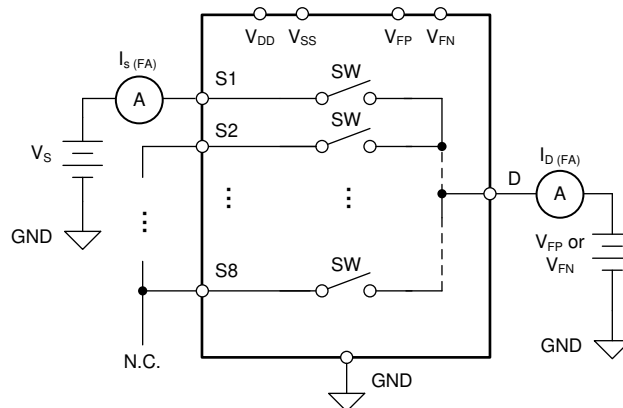
### 6.3 On-Leakage Current

Source on-leakage current ( $I_{S(ON)}$ ) and drain on-leakage current ( $I_{D(ON)}$ ) denote the channel leakage currents when the switch is in the on state.  $I_{S(ON)}$  is measured with the drain floating, while  $I_{D(ON)}$  is measured with the source floating. 

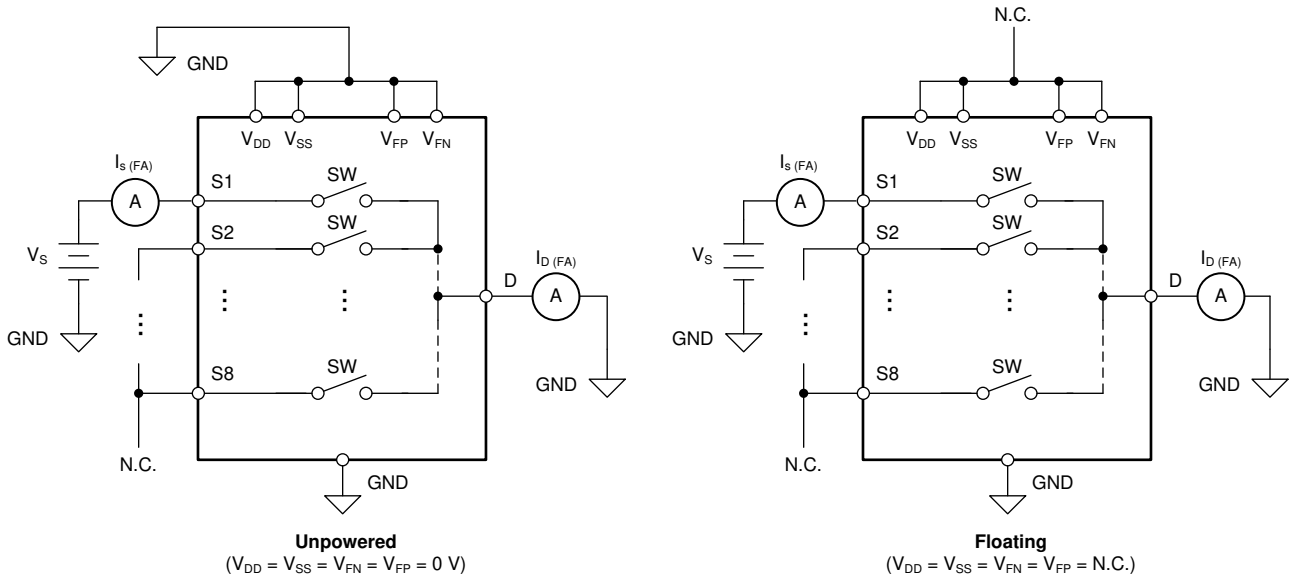


### 6.4 Input and Output Leakage Current Under Overvoltage Fault

If any of the source pin voltage goes above the fault supplies ( $V_{FP}$  or  $V_{FN}$ ), the overvoltage protection feature of the TMUX582F-SEP is triggered to turn off the switch under fault, keeping the fault channel in high-impedance state.  $I_{S(FA)}$  and  $I_{D(FA)}$  denotes the input and output leakage current under overvoltage fault conditions, respectively. For  $I_{D(FA)}$  the device is disabled to measure leakage current on the drain pin without being impacted by the 40k $\Omega$  impedance to the fault supply. When the overvoltage fault occurs, the supply (or supplies) can either be in normal operating condition () or abnormal operating condition (). During abnormal operating condition, the supply (or supplies) can either be unpowered ( $V_{DD} = V_{SS} = V_{FN} = V_{FP} = 0V$ ) or floating ( $V_{DD} = V_{SS} = V_{FN} = V_{FP} = \text{No Connection}$ ), and remains within the leakage performance specifications.



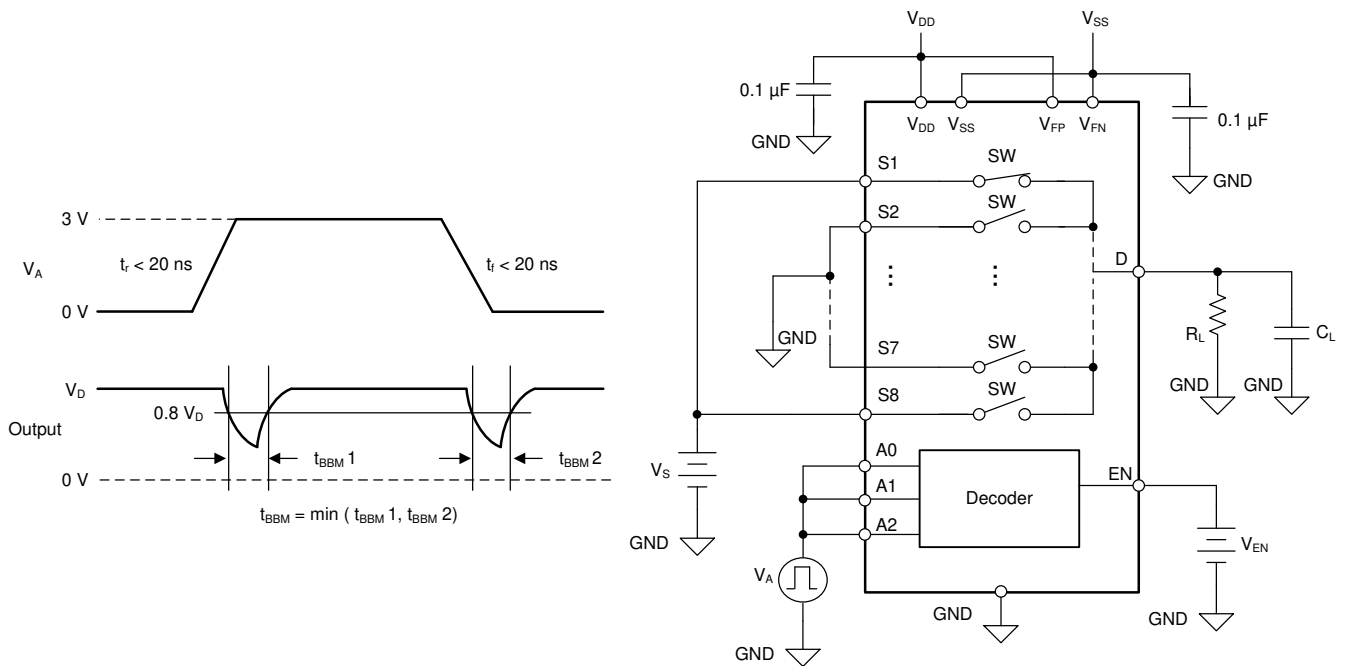




**Figure 6-5. Measurement Setup for Input and Output Leakage Current Under Overtolerance Fault with Unpowered or Floating Supplies**

### 6.5 Break-Before-Make Delay

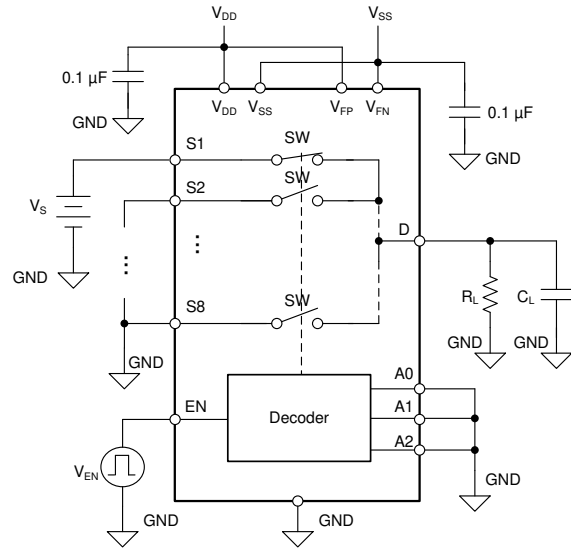
The break-before-make delay is a safety feature of the TMUX582F-SEP. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-6 shows the setup used to measure break-before-make delay, denoted by the symbol  $t_{BBM}$ .

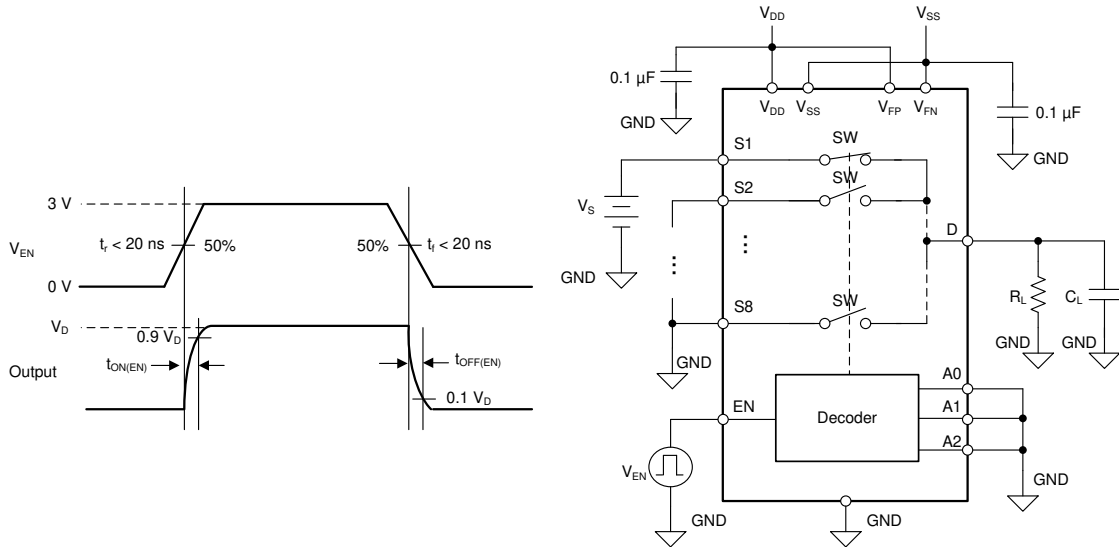


**Figure 6-6. Break-Before-Make Delay Measurement Setup**



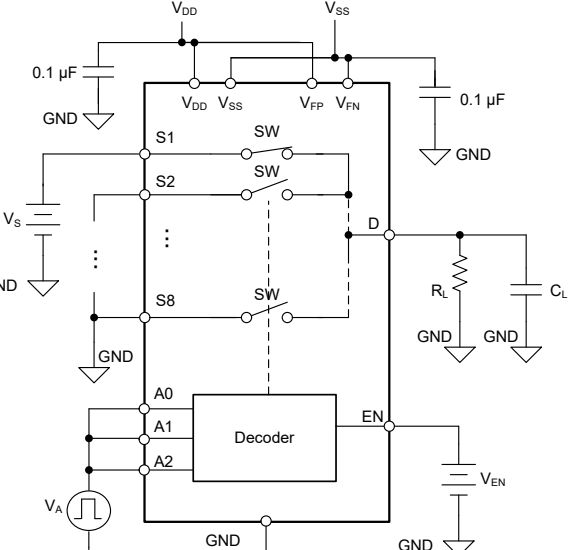
## 6.6 Enable Delay Time

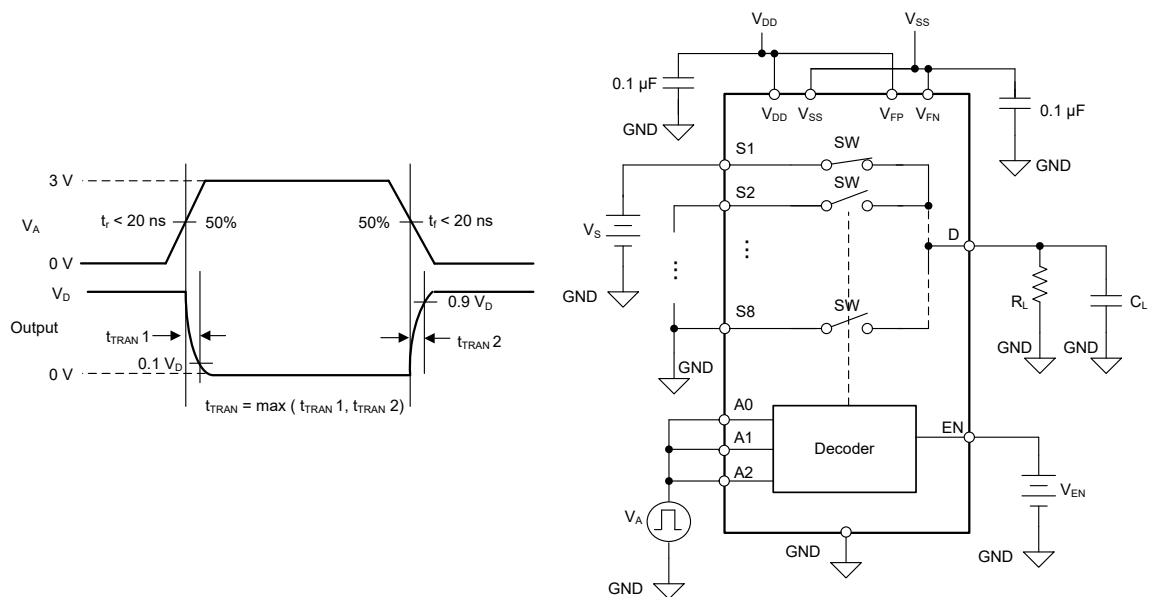
$t_{ON(EN)}$  time is defined as the time taken by the output of the TMUX582F-SEP to rise to a 90% final value after the EN signal has risen to a 50% final value.  $t_{OFF(EN)}$  is defined as the time taken by the output of the TMUX582F-SEP to fall to a 10% initial value after the EN signal has fallen to a 50% initial value.  6-7 shows the setup used to measure the enable delay time.



 6-7. Enable Delay Measurement Setup

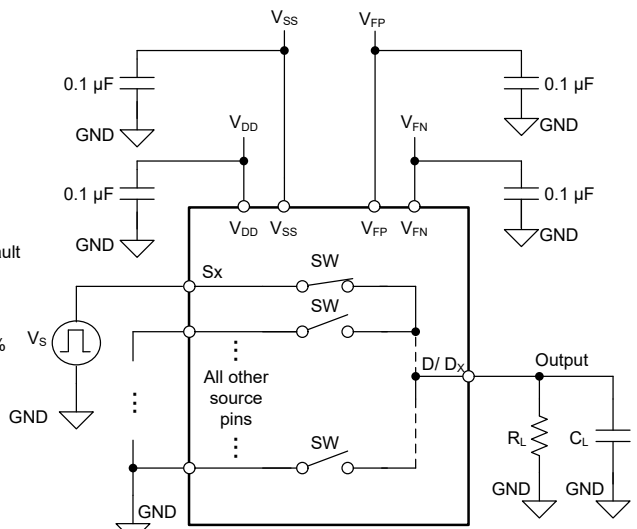
## 6.7 Transition Time

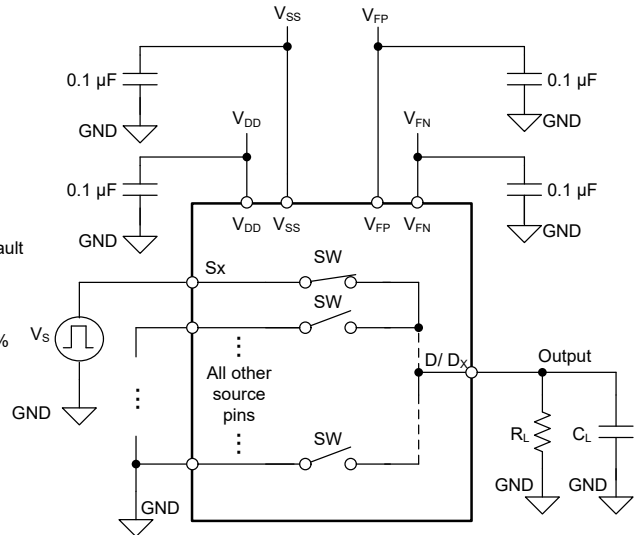
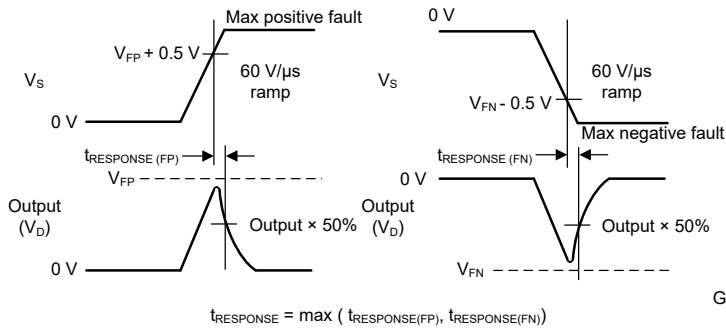
Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal ( $A_x$ ) has fallen or risen to 50% of the transition.  6-8 shows the setup used to measure transition time, denoted by the symbol  $t_{TRAN}$ .



 6-8. Transition Time Measurement Setup

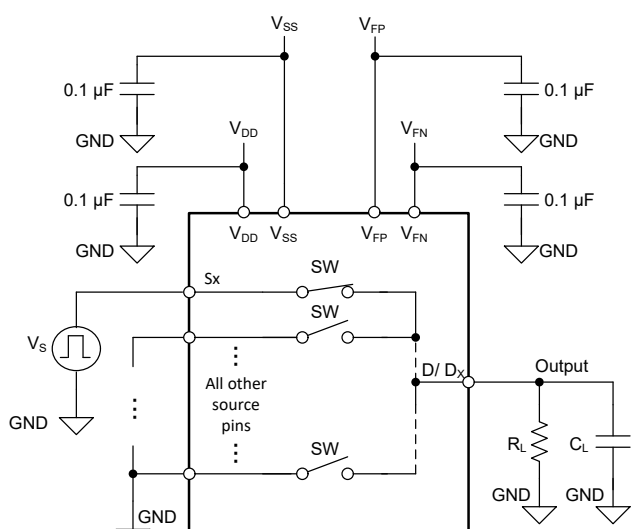
## 6.8 Fault Response Time

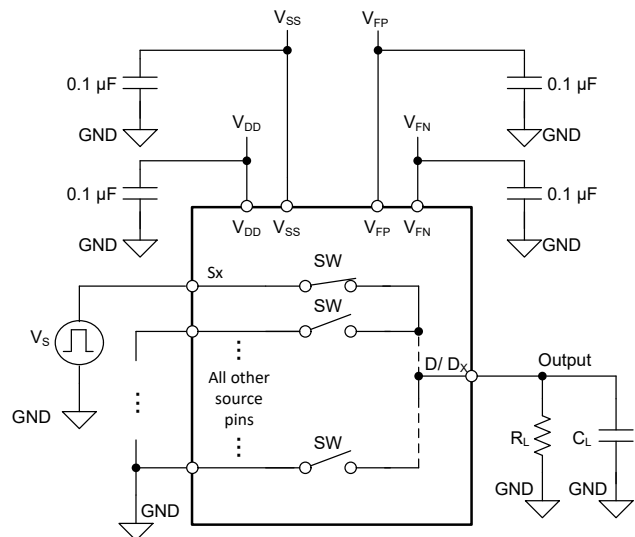
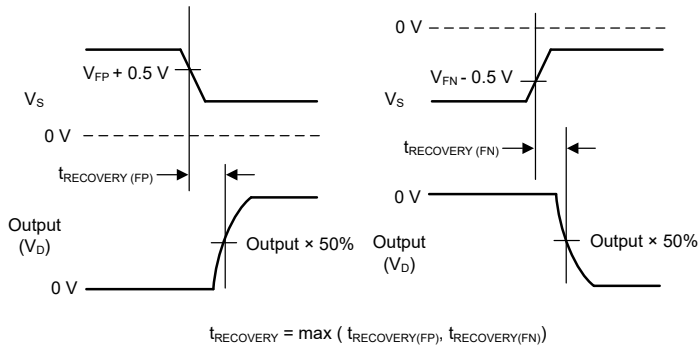
Fault response time ( $t_{\text{RESPONSE}}$ ) measures the delay between the source voltage exceeding the fault supply voltage ( $V_{\text{FP}}$  or  $V_{\text{FN}}$ ) by 0.5V and the drain voltage failing to 50% of the maximum output voltage.  shows the setup used to measure  $t_{\text{RESPONSE}}$ .



 **6-9. Fault Response Time Measurement Setup**

## 6.9 Fault Recovery Time

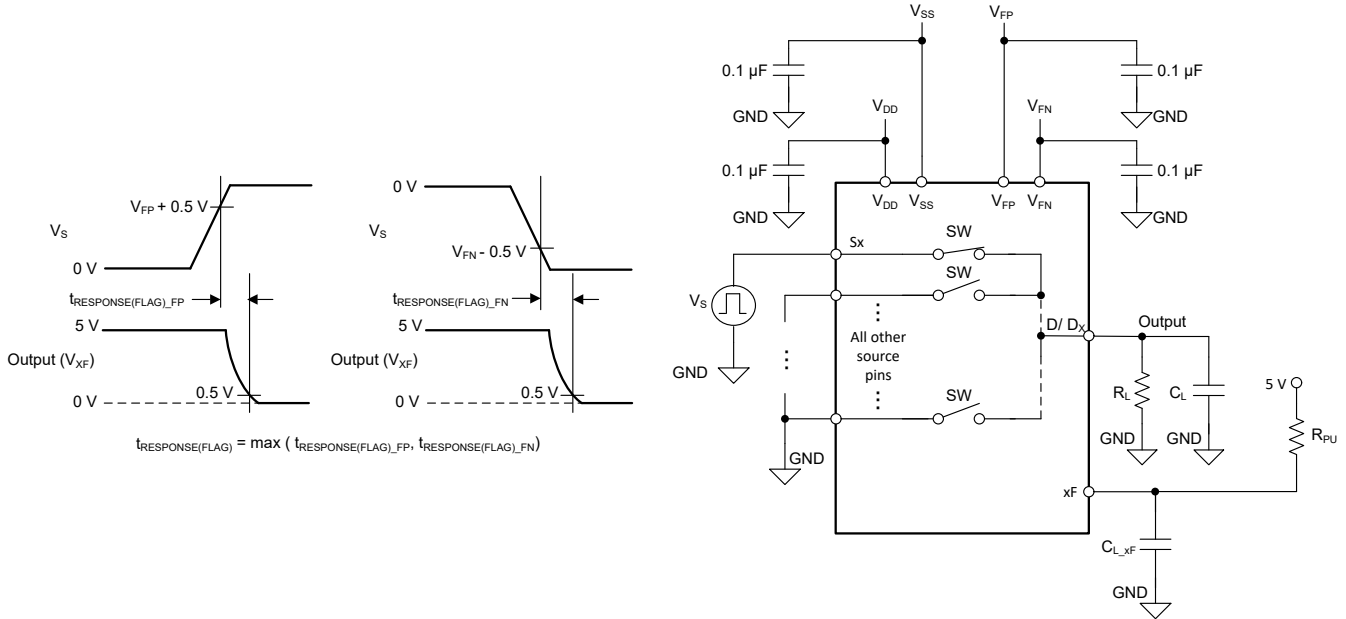
Fault recovery time ( $t_{\text{RECOVERY}}$ ) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage ( $V_{\text{FP}}$  or  $V_{\text{FN}}$ ) plus 0.5V and the drain voltage rising from 0V to 50% of the final output voltage.  shows the setup used to measure  $t_{\text{RECOVERY}}$ .



 **6-10. Fault Recovery Time Measurement Setup**

## 6.10 Fault Flag Response Time

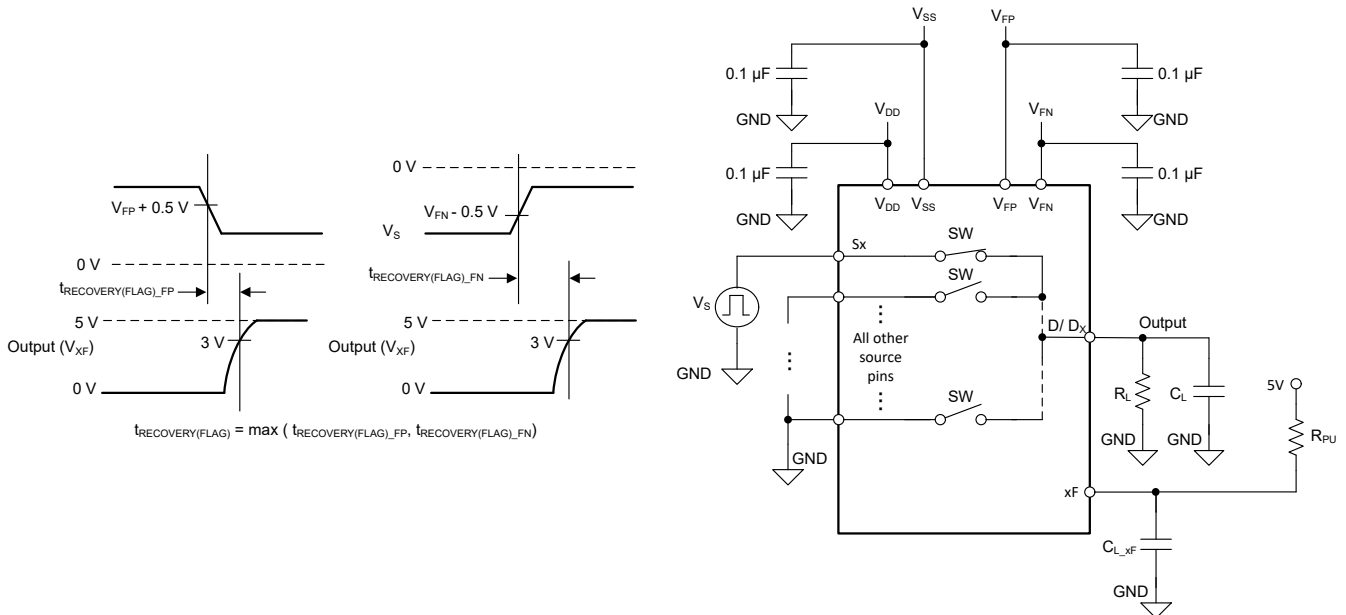
Fault flag response time ( $t_{\text{RESPONSE(FLAG)}}$ ) measures the delay between the source voltage exceeding the fault supply voltage ( $V_{\text{FP}}$  or  $V_{\text{FN}}$ ) by 0.5V and the general fault flag (FF) pin or specific fault flag (SF) pin to go below 10% of its original value. shows the setup used to measure  $t_{\text{RESPONSE(FLAG)}}$ .



6-11. Fault Flag Response Time Measurement Setup


## 6.11 Fault Flag Recovery Time

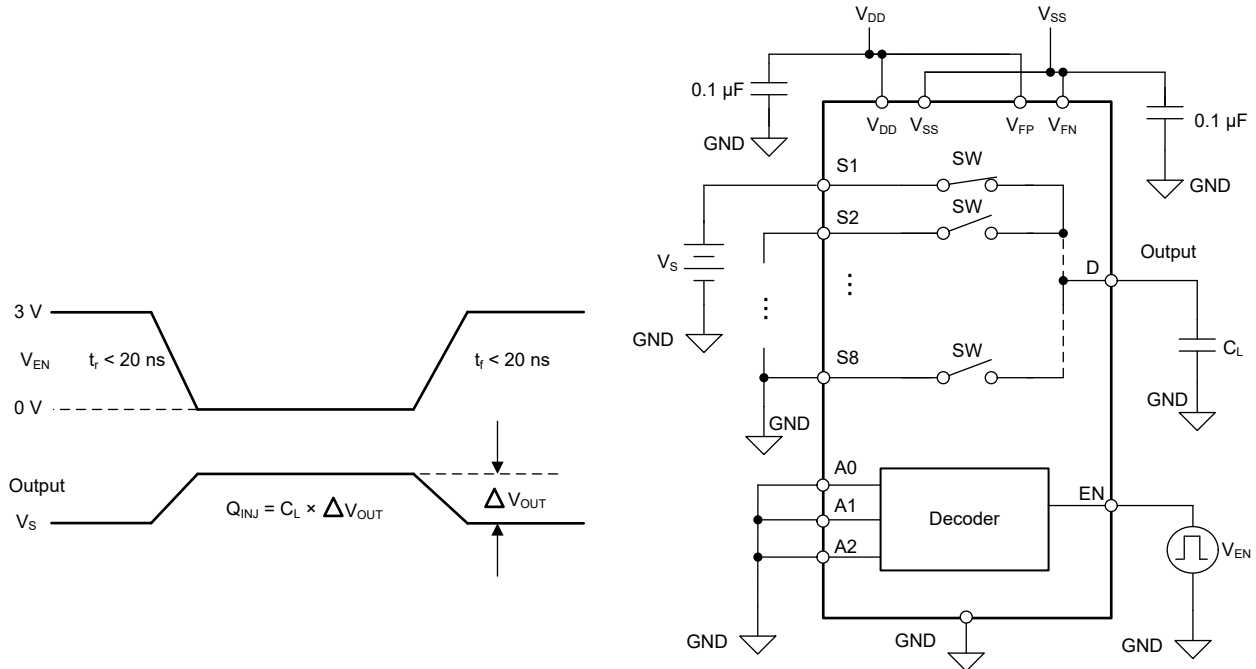
Fault flag recovery time ( $t_{\text{RECOVERY(FLAG)}}$ ) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage ( $V_{\text{FP}}$  or  $V_{\text{FN}}$ ) plus 0.5V and the general fault flag (FF) pin or the specific fault flag (SF) pin to rise above 3V with 5V external pull-up. shows the setup used to measure  $t_{\text{RECOVERY(FLAG)}}$ .



6-12. Fault Flag Recovery Time Measurement Setup

### 6.12 Charge Injection

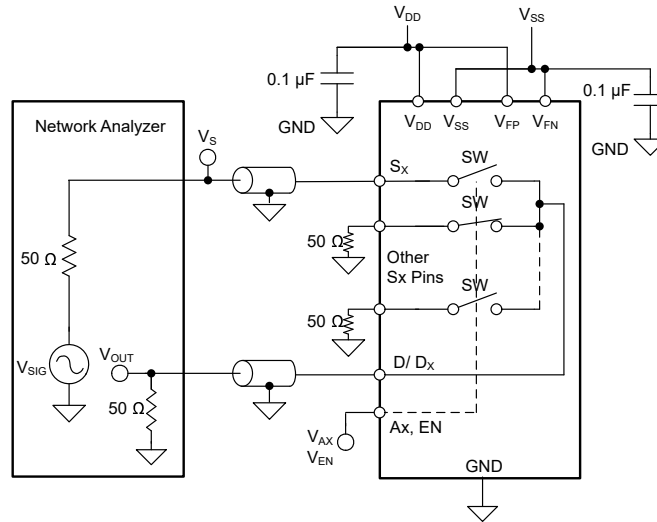
Charge injection is a measure of the glitch impulse transferred from the logic input to the analog output during switching, and is denoted by the symbol  $Q_{INJ}$ .  6-13 shows the setup used to measure charge injection from the source to drain.



 6-13. Charge-Injection Measurement Setup

### 6.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. [図 6-14](#) and [式 1](#) shows the setup used to measure, and the equation used to calculate off isolation.

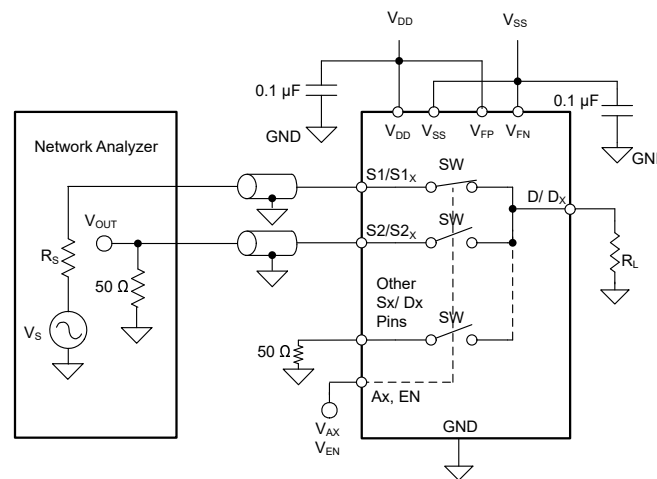


**図 6-14. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \times \text{Log} \frac{V_{OUT}}{V_S} \quad (1)$$

### 6.14 Crosstalk

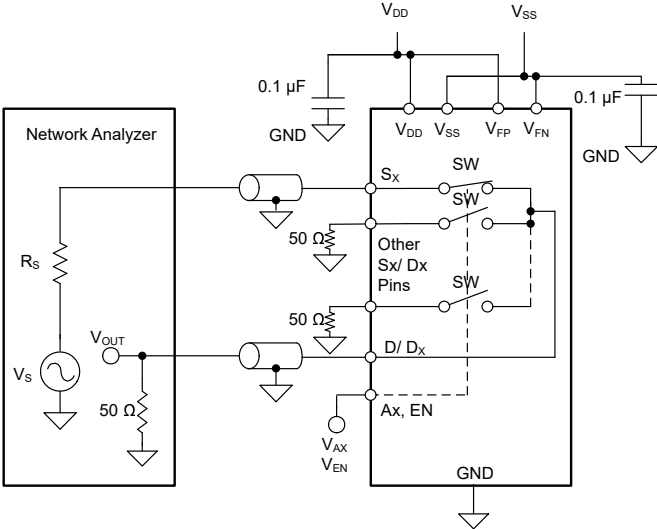
Crosstalk ( $X_{TALK}$ ) is defined as the voltage at the source pin (Sx) of an off-switch input, when a signal is applied at the source pin of an on-switch input in the same channel, as shown in [図 6-15](#) and [式 2](#).

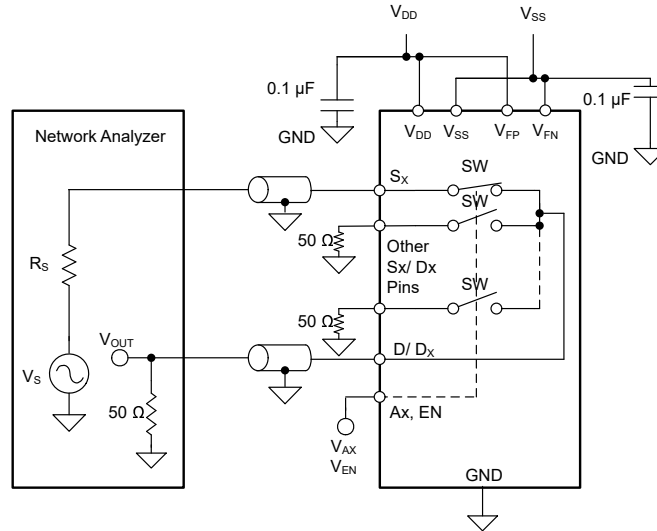


**図 6-15. Intra-Channel Crosstalk Measurement Setup**

$$\text{Intra-channel Crosstalk} = 20 \times \text{Log} \frac{V_{OUT}}{V_S} \quad (2)$$

## 6.15 Bandwidth

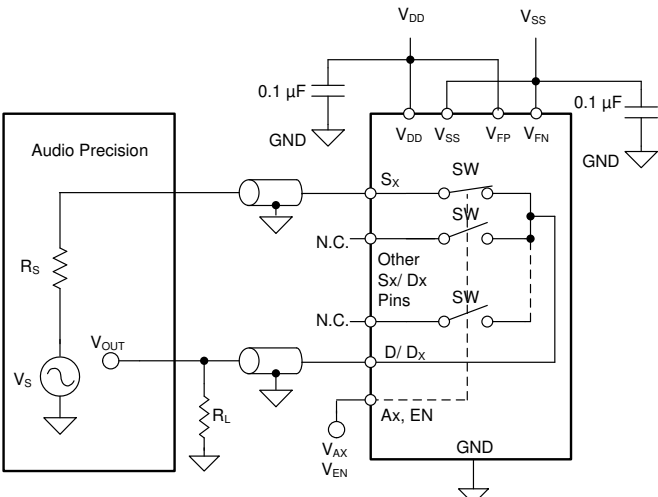
Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (S<sub>x</sub>) of an on-channel, and the output is measured at the drain pin (D) of the TMUX582F-SEP.  6-16 and 式 3 shows the setup used to measure bandwidth of the switch.

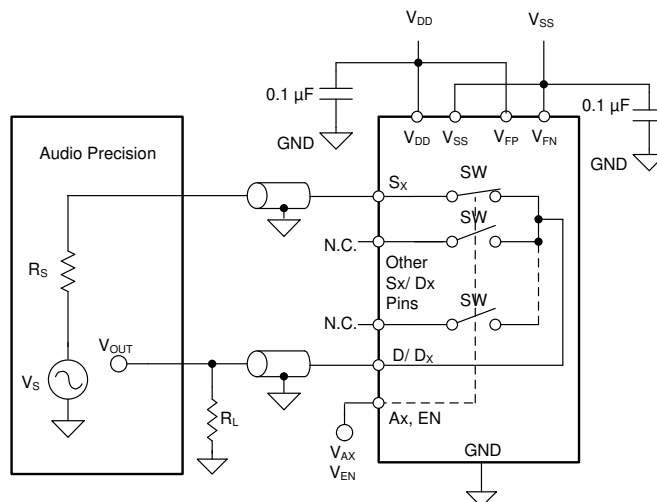


 6-16. Bandwidth Measurement Setup

$$\text{Bandwidth} = 20 \times \text{Log} \frac{V_{OUT}}{V_S} \quad (3)$$

## 6.16 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the TMUX582F-SEP varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.  6-17 shows the setup used to measure THD+N of the devices.



 6-17. THD+N Measurement Setup

## 7 Truth Table

表 7-1 provides the truth tables for the TMUX582F-SEP under normal and fault conditions.

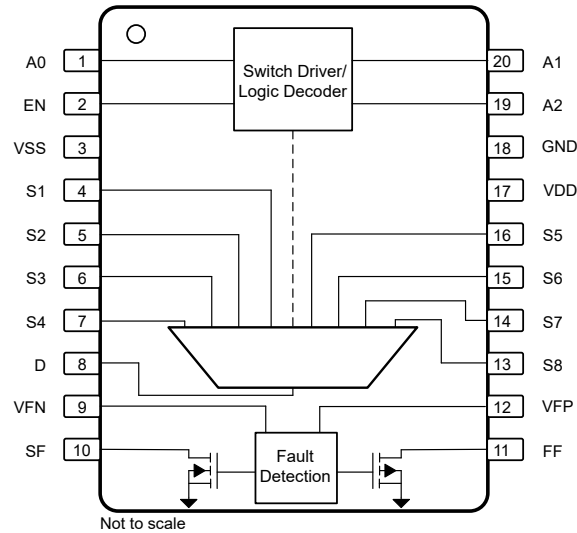
**表 7-1. TMUX582F-SEP Truth Table**

EN	A2	A1	A0	Normal Condition	Fault Condition								
					State of Specific Flag (SF) when fault occurs on								
				On Switch	S1	S2	S3	S4	S5	S6	S7	S8	
0	0	0	0	None	0	1	1	1	1	1	1	1	1
0	0	0	1	None	1	0	1	1	1	1	1	1	1
0	0	1	0	None	1	1	0	1	1	1	1	1	1
0	0	1	1	None	1	1	1	0	1	1	1	1	1
0	1	0	0	None	1	1	1	1	0	1	1	1	1
0	1	0	1	None	1	1	1	1	1	0	1	1	1
0	1	1	0	None	1	1	1	1	1	1	1	0	1
0	1	1	1	None	1	1	1	1	1	1	1	1	0
1	0	0	0	S1	0	1	1	1	1	1	1	1	1
1	0	0	1	S2	1	0	1	1	1	1	1	1	1
1	0	1	0	S3	1	1	0	1	1	1	1	1	1
1	0	1	1	S4	1	1	1	0	1	1	1	1	1
1	1	0	0	S5	1	1	1	1	0	1	1	1	1
1	1	0	1	S6	1	1	1	1	1	0	1	1	1
1	1	1	0	S7	1	1	1	1	1	1	1	0	1
1	1	1	1	S8	1	1	1	1	1	1	1	1	0

## 8 Detailed Description

The TMUX582F-SEP is a modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in a 8:1 configuration. The device works well with dual supplies ( $\pm 5V$  to  $\pm 16.5V$ ), a single supply (8V to 22V), or asymmetric supplies (such as  $V_{DD} = 12V$ ,  $V_{SS} = -5V$ ). The device features a number of protection features, allowing it to be used in harsh industrial environments.

### 8.1 Functional Block Diagram





## 8.2 Feature Description

### 8.2.1 Flat ON- Resistance

The TMUX582F-SEP is designed with a special switch architecture to produce ultra-flat on-resistance ( $R_{ON}$ ) across most of the switch input operation region. The flat  $R_{ON}$  response allows the device to be used in precision sensor applications since the  $R_{ON}$  is controlled regardless of the signals sampled. The architecture is implemented without a charge pump, so no unwanted noise is produced from the device to affect sampling accuracy.

### 8.2.2 Protection Features

The TMUX582F-SEP offer a number of protection features to enable robust system implementations.

#### 8.2.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60V or -60V, which allows the device to handle typical voltage fault condition in industrial applications. Take caution: the device is rated to handle a maximum stress of 85V across different pins:

1. **Between source pins and supply rails:**

For example, if the device is powered by  $V_{DD}$  supply of 20V, the maximum negative signal level on any source pin is -60V. If the device is powered by  $V_{DD}$  supply of 40V, the maximum negative signal level on any source pin is reduced to -45V to maintain the 85V maximum rating across the source pin and the supply.

2. **Between source pins and one or more of the drain pins:**

For example, if channel S1 is ON and the voltage on S1(A) pin is 40V. In this case, the drain voltage is also 40V. The maximum negative voltage on any of the other source pins is -45V to maintain the 85V maximum rating across the source pin and the drain pin.

#### 8.2.2.2 Powered-Off Protection

When the supplies of TMUX582F-SEP are removed ( $V_{DD}/V_{SS} = 0V$  or floating), the source (Sx) pins of the device remain in the high impedance (Hi-Z) state, and the source (Sx) and drain (Dx) pins of the device remain within the leakage performance mentioned in the Electrical Specifications. Powered-off protection minimizes system complexity by removing the need to control the power supply sequencing of the system. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, the signal on the input source pins can back-power the supply rails through the internal ESD diodes and potentially cause damage to the system. For more information on powered-off protection refer to [Eliminate Power Sequencing With Powered-Off Protection Signal Switches](#).

The switch remains OFF regardless of whether the  $V_{DD}$  and  $V_{SS}$  supplies are 0V or floating. A GND reference must always be present to allow for proper operation. Source and drain voltage levels of up to  $\pm 60V$  are blocked in the powered-off condition.

#### 8.2.2.3 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. The switch is specified to be in the OFF state, regardless of the state of the logic signals. The logic inputs are protected against positive faults of up to +24V in the powered-off condition, but do not offer protection against the negative overvoltage condition.

Fail-safe logic also allows the TMUX582F-SEP devices to interface with a voltage greater than  $V_{DD}$  during normal operation to add maximum flexibility in system design. For example, with a  $V_{DD}$  of 15V, the logic control pins could be connected to +24V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 24V.

### 8.2.2.4 Overvoltage Protection and Detection

The TMUX582F-SEP detects overvoltage inputs by comparing the voltage on a source pin (Sx) with the fault supplies ( $V_{FP}$  and  $V_{FN}$ ). A signal is considered overvoltage if it exceeds the fault supply voltages by the threshold voltage ( $V_T$ ).

When an overvoltage is detected, the switch automatically turns OFF regardless of the logic controls. The source pin becomes high impedance and allows only a small leakage current through the switch and the overvoltage does not appear on the drain. When the overvoltage channel is selected by the logic control, the drain pin (D) is pulled to the supply that was exceeded. For example, if the source voltage exceeds  $V_{FP}$ , the drain output is pulled to  $V_{FP}$ . If the source voltage exceeds  $V_{FN}$ , the drain output is pulled to  $V_{FN}$ . The pull-up impedance is approximately 40k $\Omega$ , and as a result, the drain current is limited to roughly 1mA during a shorted load (to GND) condition.

Figure 8-1 shows a detailed view of how the pullup/down controls the output state of the drain pin under a fault scenario.

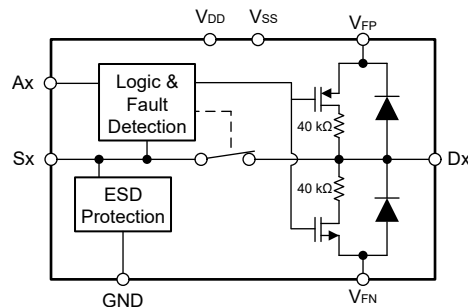


Figure 8-1. Detailed Functional Diagram

$V_{FP}$  and  $V_{FN}$  are required fault supplies that set the level at which the overvoltage protection is engaged.  $V_{FP}$  can be supplied from 3V to  $V_{DD}$ , while the  $V_{FN}$  can be supplied from  $V_{SS}$  to 0V. If the fault supplies are unavailable in the system, the  $V_{FP}$  pin must be connected to  $V_{DD}$ , while the  $V_{FN}$  pin must be connected to  $V_{SS}$ . In this case, overvoltage protection then engages at the primary supply voltages  $V_{DD}$  and  $V_{SS}$ .

### 8.2.2.5 Adjacent Channel Operation During Fault

When the logic pins are set to a channel under a fault, the overvoltage detection will trigger, the switch will open, and the drain pin will be pulled up or down as described in Section 8.2.2.4. During such an event, all other channels not under a fault can continue to operate as normal. For example, if S1 voltage exceeds  $V_{FP}$ , and the logic pins are set to S1, the drain output is pulled to  $V_{FP}$ . Then if the logic pins are changed to set S4, which is not in overvoltage or undervoltage, the drain will disconnect from the pullup to  $V_{FP}$  and the S4 switch will be enabled and connected to the drain, operating as normal. If the logic pins are switched back to S1, the S4 switch will be disabled, the drain pin will be pulled up to  $V_{FP}$  again, and the switch from S1 to drain will not be enabled until the overvoltage fault is removed.

### 8.2.2.6 ESD Protection

All pins on the TMUX582F-SEP support HBM ESD protection level up to  $\pm 3.5$ kV, which helps the device from getting ESD damages during the manufacturing process.

The drain pins (D) have internal ESD protection diodes to the fault supplies  $V_{FP}$  and  $V_{FN}$ . Therefore, the voltage at the drain pins must not exceed the fault supply voltages to prevent excessive diode current. The source pins have specialized ESD protection that allows the signal voltage to reach  $\pm 60$ V regardless of the supply voltage level. Exceeding  $\pm 60$ V on any source input may damage the ESD protection circuitry on the device and cause the device to malfunction if the damage is excessive.

### 8.2.2.7 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX582F-SEP devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX582F-SEP to be used in harsh environments. For more information on latch-up immunity, refer to [Using Latch Up Immune Multiplexers to Help Improve System Reliability](#).

### 8.2.2.8 EMC Protection

The TMUX582F-SEP are not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specification: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistors, are required to prevent source input voltages from going above the rated  $\pm 60\text{V}$  limits.

When selecting a TVS protection device, it is critical to confirm that the maximum working voltage is greater than both the normal operating range of the input source pins to be protected and any known system common-mode overvoltage that may be present due to incorrect wiring, loss of power, or short circuit. [Figure 8-2](#) shows an example of the proper design window when selecting a TVS device.

Region 1 denotes normal operation region of TMUX582F-SEP where the input source voltages stay below the fault supplies  $V_{FP}$  and  $V_{FN}$ . Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX582F-SEP. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX582F-SEP, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin system designers must impose when selecting the TVS protection device to prevent accidental triggering of ESD cells of the TMUX582F-SEP devices.

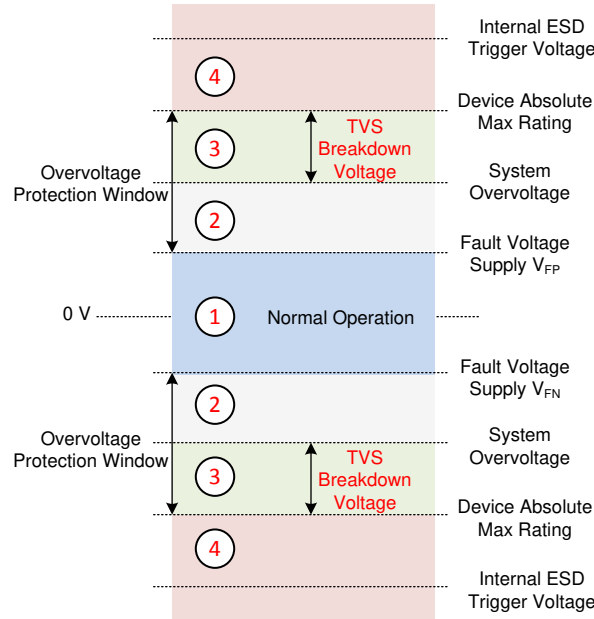


図 8-2. System Operation Regions and Proper Region of Selecting a TVS Protection Device

### 8.2.3 Overvoltage Fault Flags

The voltages on the source input pins of the TMUX582F-SEP is continuously monitored, and the status of whether an overvoltage condition occurs is indicated by an active low general fault flag (FF). The voltage on the FF pin indicates if any of the source input pins are experiencing an overvoltage condition. If any source pin voltage exceeds the fault supply voltages  $V_T$ , then the FF output is pulled-down to below  $V_{OL}$ .

The specific fault (SF) output pins, on the other hand, can be used to decode which inputs are experiencing an overvoltage condition. The SF pin is pulled-down to below  $V_{OL}$  when an overvoltage condition is detected on a specific source input pin, depending on the state of the A0, A1, A2, and EN logic pins (表 7-1 provides more details).

Both the FF pin and SF pin are open-drain output and external pull-up resistors of 1 kΩ are recommended. The pull-up voltage can be in the range of 1.8V to 5.5V, depending on the controller voltage the device interfaces with.

### 8.2.4 Bidirectional and Rail-to-Rail Operation

The TMUX582F-SEP conducts equally well from source ( $S_x$ ) to drain (D or  $D_x$ ) or from drain (D or  $D_x$ ) to source ( $S_x$ ). Each signal path has very similar characteristics in both directions. It is important to note, however, that the overvoltage protection is implemented only on the source ( $S_x$ ) side. The voltage on the drain is only allowed to swing between  $V_{FP}$  and  $V_{FN}$  and no overvoltage protection is available on the drain side.

The primary supplies ( $V_{DD}$  and  $V_{SS}$ ) define the on-resistance profile of the switch channel, whereas the fault voltage supplies ( $V_{FP}$  and  $V_{FN}$ ) define the signal range that can be passed through from source to drain of the device. It is good practice to use voltages on  $V_{FP}$  and  $V_{FN}$  that are lower than  $V_{DD}$  and  $V_{SS}$  to take advantage of the flat on-resistance region of the device for better input-to-output linearity. The flattest on-resistance region extends from  $V_{SS}$  to roughly 3V below  $V_{DD}$ . Once the signal is within 3V of  $V_{DD}$  the on-resistance will exponentially increase and may impact desired signal transmission.

### 8.2.5 1.8V Logic Compatible Inputs

The TMUX582F-SEP devices have 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX582F-SEP to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations, refer to [Simplifying Design with 1.8V logic Muxes and Switches](#).

### 8.2.6 Integrated Pull-Down Resistor on Logic Pins

The TMUX582F-SEP have internal weak pull-down resistors to GND to confirm the logic pins are not left floating. The value of this pull-down resistor is approximately 4M $\Omega$ , but is clamped to about 1 $\mu$ A at higher voltages. This feature integrates up to four external components and reduces system size and cost.

## 8.3 Device Functional Modes

The TMUX582F-SEP offer two modes, Normal mode and Fault mode, of operation depending on whether any of the input pins experience overvoltage condition.

### 8.3.1 Normal Mode

In Normal mode operation, signals of up to  $V_{FP}$  and  $V_{FN}$  can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). As provided in 表 7-1, the address (Ax) pins and the enable (EN) pin determine which switch path to turn on, The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies ( $V_{DD} - V_{SS}$ ) must be higher or equal to 8V. With a minimum  $V_{DD}$  of 5V.
- $V_{FP}$  must between 3V and  $V_{DD}$ , and  $V_{FN}$  must between  $V_{SS}$  and 0V.
- The input signals on the source (Sx) or the drain (D or Dx) must be between  $V_{FP} + V_T$  and  $V_{FN} - V_T$ .
- The logic control (Ax and EN) must have selected the switch.

### 8.3.2 Fault Mode

The TMUX582F-SEP enters into Fault mode when any of the input signals on the source (Sx) pins exceed  $V_{FP}$  or  $V_{FN}$  by a threshold voltage  $V_T$ . Under the overvoltage condition, the switch input experiencing the fault automatically turns OFF regardless of the digital logic status, and the source pin becomes high impedance with a negligible amount of leakage current flowing through the switch. When the fault channel is selected by the digital logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded through a 40k $\Omega$  internal resistor.

In the Fault Mode, the general fault flag (FF) is asserted low. The specific flag (SF) is asserted low when a specific input path is selected, as provided in 表 7-1.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (D or Dx) pin, if used as signal input, must stay in between  $V_{FP}$  and  $V_{FN}$  at all time since no overvoltage protection is implemented on the drain pin.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The TMUX582F-SEP is part of the fault protected switches and multiplexers family of devices. The ability to protect downstream components from overvoltage events up to  $\pm 60V$  makes these switches and multiplexers an excellent choice for harsh aerospace environments.

### 9.2 Typical Application

#### 9.2.1 System Diagnostics – Telemetry

In large remote systems, on-board diagnostics is essential to correct fault scenarios. Through measuring subsystem voltage, current consumption, or a fault pin directly, the system MCU can easily detect where a potential issue surfaces and automatically correct it; however, this requires many ADC channels to accomplish. TMUX582F-SEP allows a significant reduction in ADC channels. Low distortion, charge injection and off-isolation increases measurement accuracy and helps reduce the likelihood of false positives or negatives. In addition, overvoltage and power-off or cold sparing protection helps prevent faults from the subsystems propagating throughout the system.

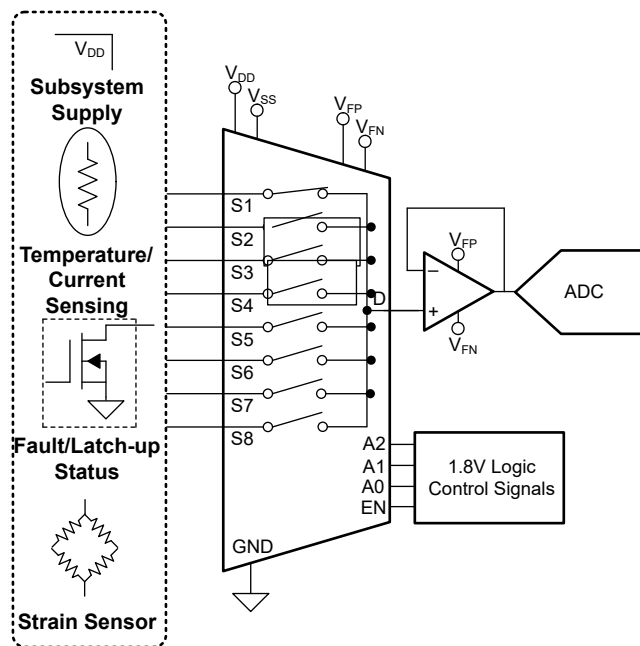


図 9-1. System Diagnostics - Telemetry

## 9.2.2 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Positive supply ( $V_{DD}$ ) mux	+12V
Negative supply ( $V_{SS}$ ) mux	-5V
Positive fault voltage supply ( $V_{FP}$ ) mux and ADC	+5V
Negative fault voltage supply ( $V_{FN}$ ) mux and ADC	0V
Max power supply voltage on board	+24V
Input / output signal range non-faulted	+5V to 0V
Overvoltage protection levels	-60V to 60V
Control logic thresholds	1.8V compatible
Temperature range	-55°C to +125°C

## 9.2.3 Detailed Design Procedure

The TMUX582F-SEP is built on a latch-up immune process that can support telemetry applications by decreasing the number of ADC channels used while also reducing distortions in sampled inputs by maintaining an ultra low Ron flatness response that helps prevent false positives and negatives. TMUX582F-SEP also utilizes overvoltage and power-off protection (cold sparing capable up to  $\pm 60V$ ), which can help prevent downstream devices from experiencing these events.

## 9.2.4 Application Curves

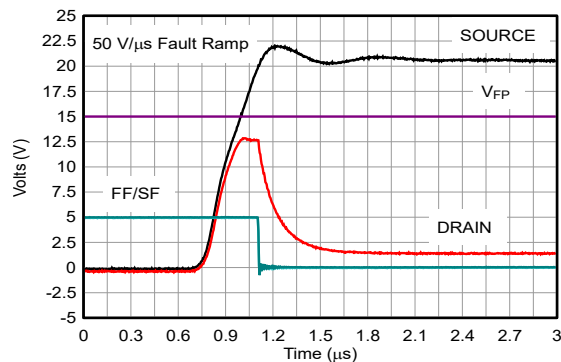


図 9-2. Positive Overvoltage Response

## 9.3 Power Supply Recommendations

The TMUX582F-SEP operates across a wide supply range of  $\pm 5V$  to  $\pm 16.5V$  (8V to 22V in single-supply mode). They also perform well with asymmetrical supplies such as  $V_{DD} = 12V$  and  $V_{SS} = -5V$ . For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 $\mu F$  to 10 $\mu F$  at both the  $V_{DD}$  and  $V_{SS}$  pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped. As a best practice, it is recommended to ramp  $V_{SS}$  first before  $V_{DD}$  in dual or asymmetrical supply applications.

The fault supplies ( $V_{FP}$  and  $V_{FN}$ ) provide the current required to operate the fault protection, and thus, must be low impedance supplies. They can be derived from the primary supplies by using a resistor divider and buffer. The fault supplies must not exceed the primary supplies as it might cause unexpected behavior of the switch.

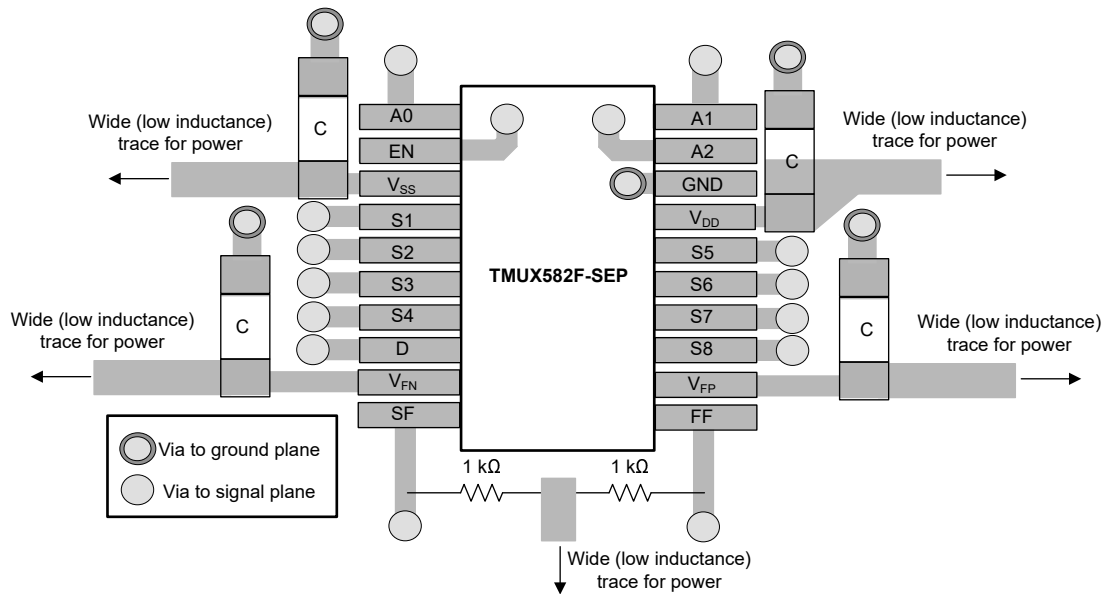
## 9.4 Layout

### 9.4.1 Layout Guidelines

The following figure illustrates an example of a PCB layout with the TMUX582F-SEP. Some key considerations are as follows:

- Decouple the  $V_{DD}$  and  $V_{SS}$  pins with a 0.1  $\mu\text{F}$  capacitor, placed as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the  $V_{DD}$  and  $V_{SS}$  supplies.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

### 9.4.2 Layout Example



☒ 9-3. TMUX582F-SEP PW Layout Example



## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ADS866x 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges](#)
- Texas Instruments, [OPAx140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz, JFET Op Amp](#)
- Texas Instruments, [OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™](#)

### 10.2 ドキュメントの更新通知を受け取る方法

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[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision \* (June 2022) to Revision A (July 2024)

Page

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|---|------|
| • ドキュメントのステータスを「事前情報」から「量産データ」に変更 .....                       | 1    |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX582FPWTSEP	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TM582FSEP	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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