TEXAS INSTRUMENTS
TMUXHS4412
JAJSKW6 – DECEMBER 2020

TMUXHS4412 4 チャネル、20Gbps、2:1/1:2、差動マルチプレクサ / デマルチプレクサ

1 特長

- 4 つの差動チャネルに対して、双方向パッシブ 2:1 マルチプレクサ / 1:2 デマルチプレクサを実現します
- 最大 20Gbps のデータ伝送能力
- 最大 16Gbps の PCI Express 4.0 をサポート
- USB 3.2、USB 4.0、TBT 3.0、DP 2.0、SATA、SAS、MIPI DSI/CSI、FPD-Link III、LVDS、SFI、イーサネットの各インターフェイスもサポート
- 13GHz の –3dB 差動帯域幅
- PCIe 4.0 信号処理に適した優れた動的特性
  - 挿入損失:-1.3dB (8GHz)
  - 反射損失:–22dB (8GHz)
  - クロストーク:-58dB (8GHz)
- 適応型同相電圧トラッキング
- 0～1.8V の同相電圧をサポート
- 3.3V または 1.8V の単一電源電圧 VCC
- 超低消費電力:320µA (アクティブ時)、0.1µA (スタンバイ時)
- 産業用温度範囲 (–40℃～105℃) のオプション
- DS160PR421 と DS160PR412 を搭載したピン互換 PCIe 4.0 リニア・リドライバ・オプション
- 3.5mm × 9mm の QFN パッケージで供給されます

2 アプリケーション

- PC とノート PC
- ゲーム、ホーム・シアター、エンターテインメント、TV
- データ・センターおよびエンタープライズ・コンピューティング
- 医療用アプリケーション
- 試験および測定機器
- ファクトリ・オートメーションおよび制御
- 航空宇宙および防衛
- 電子 POS (EPOS)
- ワイヤレス・インフラ

3 概要

TMUXHS4412 は高速双方向パッシブ・スイッチで、マルチプレクサ (mux) とデマルチプレクサ (demux) 両方の構成に使用できます。TMUXHS4412 は、PCI Express 4.0 など最高 20Gbps のデータ・レートの多数の高速差動インターフェイスに使用できるアナログ差動パッシブ・マルチプレクサ / デマルチプレクサです。電気的チャネルのシグナル・インテグリティに余裕がある場合には、さらに高いデータ・レートで使用できます。TMUXHS4412 は、同相電圧範囲 (CMV) が最大 0～1.8V、差動振幅が最大 1800mVpp の差動信号をサポートしています。適応型 CMV トラッキングにより、デバイスを通るチャネルが同相電圧範囲全体にわたって変化しないようにしています。

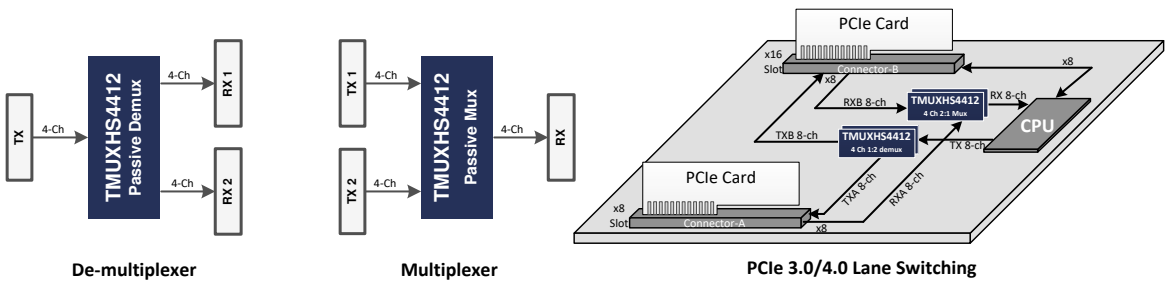
TMUXHS4412 の優れた動的特性は、信号アイ・ダイアグラムの減衰の最小化、超低ジッタを可能にしています。このデバイスのシリコン設計は、高い周波数の信号帯域でも優れた周波数応答が得られるように最適化されています。このデバイスのシリコン信号トレースとスイッチ・ネットワークは、最良のペア内スキュー性能が得られるように整合されています。

TMUXHS4412 は、産業用および高信頼性用途などの多数の堅牢なアプリケーションに適した拡張産業用温度範囲で動作します。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TMUXHS4412	WQFN (42)	3.5mm × 9.0mm × 0.5mm ピッチ
TMUXHS4412I		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション使用事例

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2020	*	Initial release

5 Pin Configuration and Functions

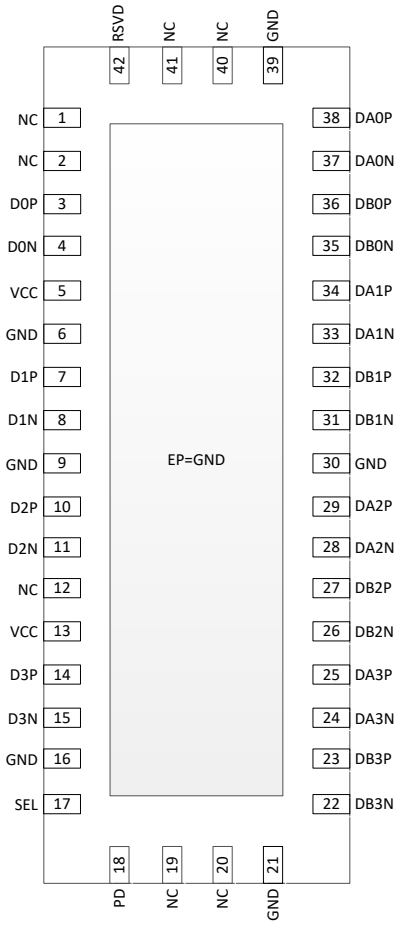


図 5-1. RUA package 42-Pin WQFN Top View (not to scale)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D0P	3	I/O	Common Port (D), channel 0, high-speed positive signal
D0N	4	I/O	Common Port, channel 0, high-speed negative signal
D1P	7	I/O	Common Port, channel 1, high-speed positive signal
D1N	8	I/O	Common Port, channel 1, high-speed negative signal
D2P	10	I/O	Common Port, channel 2, high-speed positive signal
D2N	11	I/O	Common Port, channel 2, high-speed negative signal
D3P	14	I/O	Common Port, channel 3, high-speed positive signal
D3N	15	I/O	Common Port, channel 3, high-speed negative signal
DA0P	38	I/O	Port A (DA), channel 0, high-speed positive signal
DA0N	37	I/O	Port A, channel 0, high-speed negative signal
DA1P	34	I/O	Port A, channel 1, high-speed positive signal
DA1N	33	I/O	Port A, channel 1, high-speed negative signal
DA2P	29	I/O	Port A, channel 2, high-speed positive signal
DA2N	28	I/O	Port A, channel 2, high-speed negative signal
DA3P	25	I/O	Port A, channel 3, high-speed positive signal

PIN		TYPE	DESCRIPTION
NAME	NO.		
DA3N	24	I/O	Port A, channel 3, high-speed negative signal
DB0P	36	I/O	Port B (DB), channel 0, high-speed positive signal
DB0N	35	I/O	Port B, channel 0, high-speed negative signal
DB1P	32	I/O	Port B, channel 1, high-speed positive signal
DB1N	31	I/O	Port B, channel 1, high-speed negative signal
DB2P	27	I/O	Port B, channel 2, high-speed positive signal
DB2N	26	I/O	Port B, channel 2, high-speed negative signal
DB3P	23	I/O	Port B, channel 3, high-speed positive signal
DB3N	22	I/O	Port B, channel 3, high-speed negative signal
GND	6, 9, 16, 21,30, 39	G	Ground
PD	18	I	Active-low chip enable. H: Shutdown
NC	1, 2, 12, 19, 20, 40, 41	NA	Leave unconnected
RSVD	42	NA	Reserved - TI test mode. Pull-down to GND using a resistor such as 4.7 kΩ
SEL	17	I	Port select pin. L: Common Port (D) to Port A (DA) H: Common Port (D) to Port B (DB)
V_{CC}	5, 13	P	3.3 or 1.8 V power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC-ABSMAX}$	Supply voltage		–0.5	4	V
$V_{HS-ABSMAX}$	Voltage	Differential I/O pins	–0.5	2.4	V
$V_{CTR-ABSMAX}$	Voltage	Control pins	–0.5	V_{CC}+0.4	V
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	1.8 V supply voltage mode	1.71	1.8	1.98	V
		3.3 V supply voltage mode	3.0	3.3	3.6	V
$V_{CC-RAMP}$	Supply voltage ramp time		0.1		100	ms
V_{IH}	Input high voltage	SEL, PD pins	0.75V_{CC}			V
V_{IL}	Input low voltage	SEL, PD pins			0.25V_{CC}	V
V_{DIFF}	High-speed signal pins differential voltage		0		1.8	V_{pp}
V_{CM}	High speed signal pins common mode voltage	1.8 V supply voltage mode, biased from common port (D)	0		0.9	V
		3.3 V supply voltage mode, biased from D or DA/DB ports.	0		1.8	V
T_A	Operating free-air/ambient temperature	TMUXHS4412	0		70	°C
		TMUXHS4412I	-40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUXHS4412 RUA (WQFN) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W

THERMAL METRIC(1)		TMUXHS4412 RUA (WQFN) 42 PINS	UNIT
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

6.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	PD = 0; 0 V ≤ V_{CM} ≤ 1.8; SEL = 0 or V_{CC}		320	480	µA
I_{STDN}	Device shutdown current	PD = V_{CC}		0.1	2	µA
C_{ON}	Output ON capacitance to GND	PD = 0; f = 8 Ghz		0.45		pF
R_{ON}	Output ON resistance	0 V ≤ V_{CM} ≤ 1.8 V; I_O = –8 mA		5	8	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, PD)	V_{IN} = 3.6 V			2	µA
$I_{IL,CTRL}$	Input low current, control pins (SEL, PD)	V_{IN} = 0 V			1	µA
$R_{CM,HS}$	Common mode resistance to ground on D pins (Dx[P/N])	Each pin to GND		1.0	1.4	MΩ
$I_{IH,HS,SEL}$	Input high current, high-speed pins [Dx/DAx/DBx][P/N]	V_{IN} = 1.8 V for selected port, D and DA pins with SEL = 0, and D and DB pins with SEL = V_{CC}			5	µA
$I_{IH,HS,NSEL}$	Input high current, high-speed pins [Dx/DAx/DBx][P/N]	V_{IN} = 1.8 V for non-selected port, DB with SEL = 0, and DA with SEL = V_{CC} (1)			150	µA
$I_{HIZ,HS}$	Leakage current through turned off switch between Dx[P/N] and [DA/DB]x[P/N]	PD = VCC; Dx[P/N] = 1.8 V, [DA/DB]x[P/N] = 0 V and Dx[P/N] = 0 V, [DA/DB]x[P/N] = 1.8 V			4	µA
$R_{A,p2n}$	DC Impedance between Dx[P] and Dx[N] pins	PD = 0 and VCC		20		KΩ

(1) There is a 20-kΩ pull-down in non-selected port.

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	f = 10 MHz		-0.4		dB
		f = 2.5 GHz		-0.7		
		f = 4 GHz		-0.8		
		f = 5 GHz		-0.9		
		f = 8 GHz		-1.3		
		f = 10 GHz		-1.8		
BW	–3-dB bandwidth			13		GHz
R_L	Differential return loss	f = 10 MHz		-30		dB
		f = 2.5 GHz		-23		
		f = 4 GHz		-23		
		f = 5 GHz		-22		
		f = 8 GHz		-22		
		f = 10 GHz		-15		

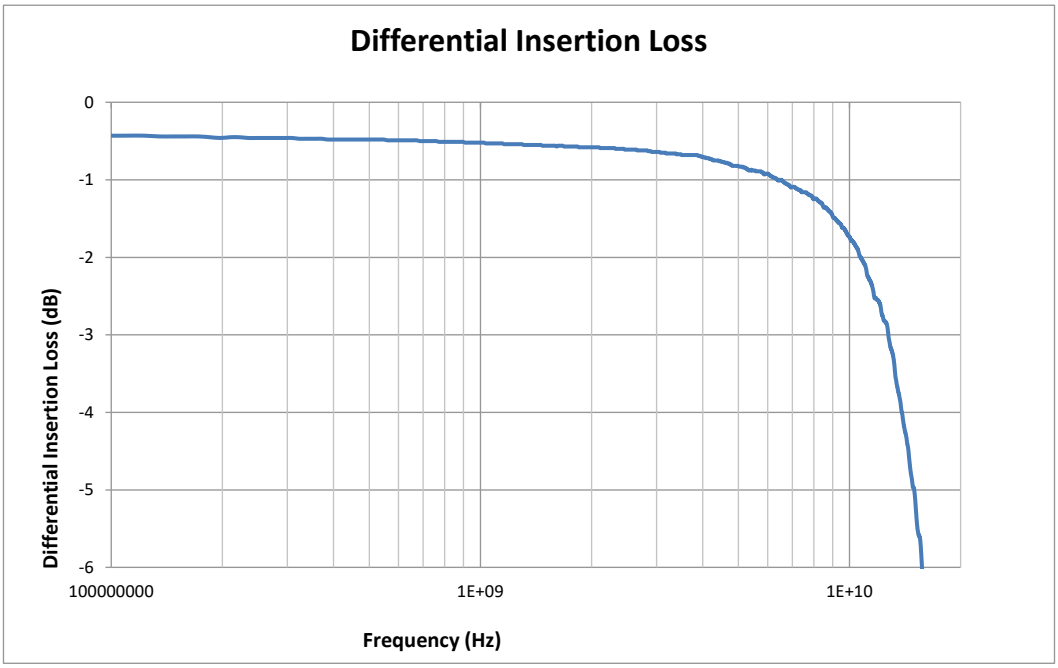
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
O_{IRR}	Differential OFF isolation	f = 10 MHz		-57		dB
		f = 2.5 GHz		-27		
		f = 4 GHz		-22		
		f = 5 GHz		-20		
		f = 8 GHz		-15		
		f = 10 GHz		-12		
X_{TALK}	Differential crosstalk	f = 10 MHz		-73		dB
		f = 2.5 GHz		-64		
		f = 4 GHz		-61		
		f = 5 GHz		-61		
		f = 8 GHz		-58		
		f = 10 GHz		-54		
SCD11,22	Mode conversion - differential to common mode	f = 8 GHz		-29		dB
SCD21,12	Mode conversion - differential to common mode	f = 8 GHz		-25		dB
SDC11,22	Mode conversion - common mode to differential	f = 8 GHz		-29		dB
SDC21,12	Mode conversion - common mode to differential	f = 8 GHz		-25		dB

6.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	f = 1 Ghz		50		ps
t_{SW_ON}	Switching time SEL-to-Switch ON	Biased from DA/DB side with CMV difference is <100mV, DA/DB pins at 90% of final value			130	ns
t_{SW_OFF}	Switching time SEL-to-Switch OFF	Biased from DA/DB side with CMV difference is <100mV, DA/DB pins at 90% of final value			100	ns
t_{SK_INTRA}	Intra-pair output skew between P and N pins for same channel	f = 1 Ghz		4.0		ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1 Ghz		4.0		ps

6.8 Typical Characteristics

図 6-1 shows differential insertion loss on the top plot and return loss on the bottom plot of a typical TMUXHS4412 channel. Note measurements are performed in TI evaluation board with board and equipment parasitics calibrated out.



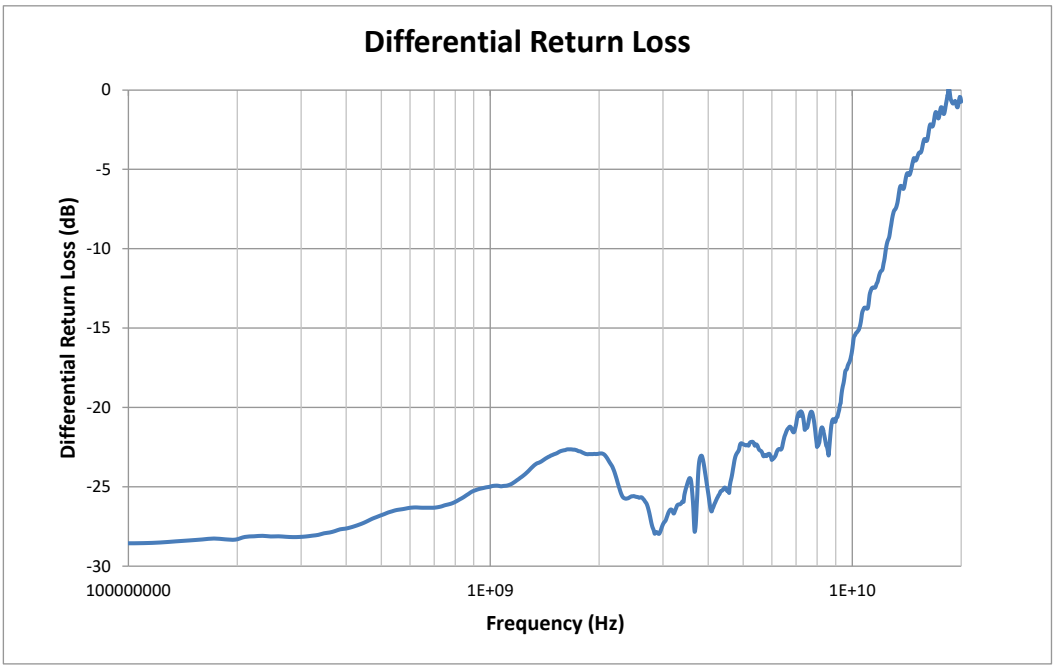


図 6-1. S-parameter plots for a TMUXHS4412 channel - top: differential insertion loss, and bottom: return loss vs frequency

図 6-2 shows side by side comparison of 10 Gbps signals through calibration traces and a typical TMUXHS4412 channels.

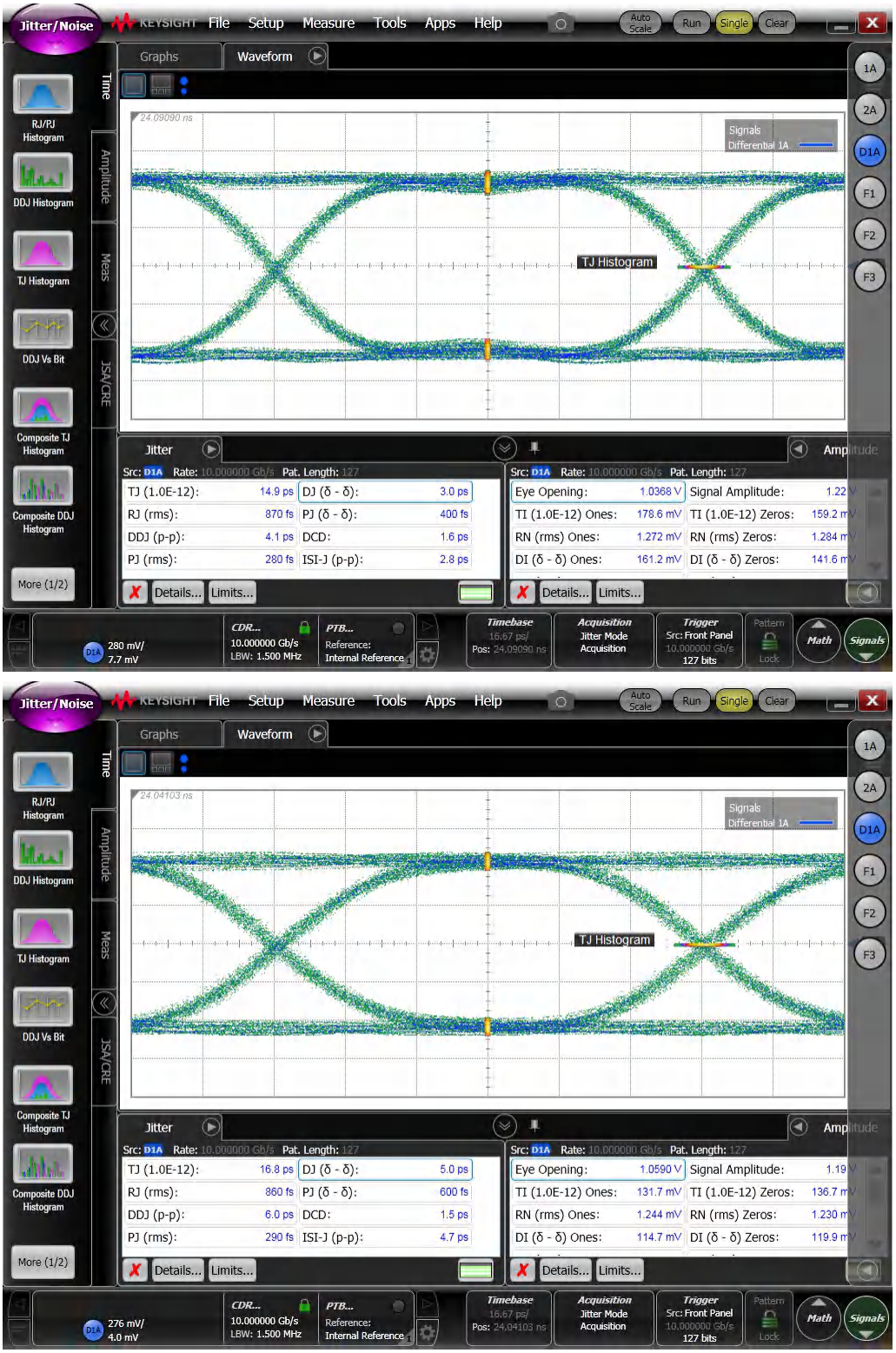


図 6-2. Jitter decomposition of 10 Gbps PRBS-7 signals in TI evaluation board - Top: through calibration traces, Bottom: through a typical TMUXHS4412 channels

図 6-3 shows side by side comparison of 20 Gbps signals through calibration traces and a typical TMUXHS4412 channels.

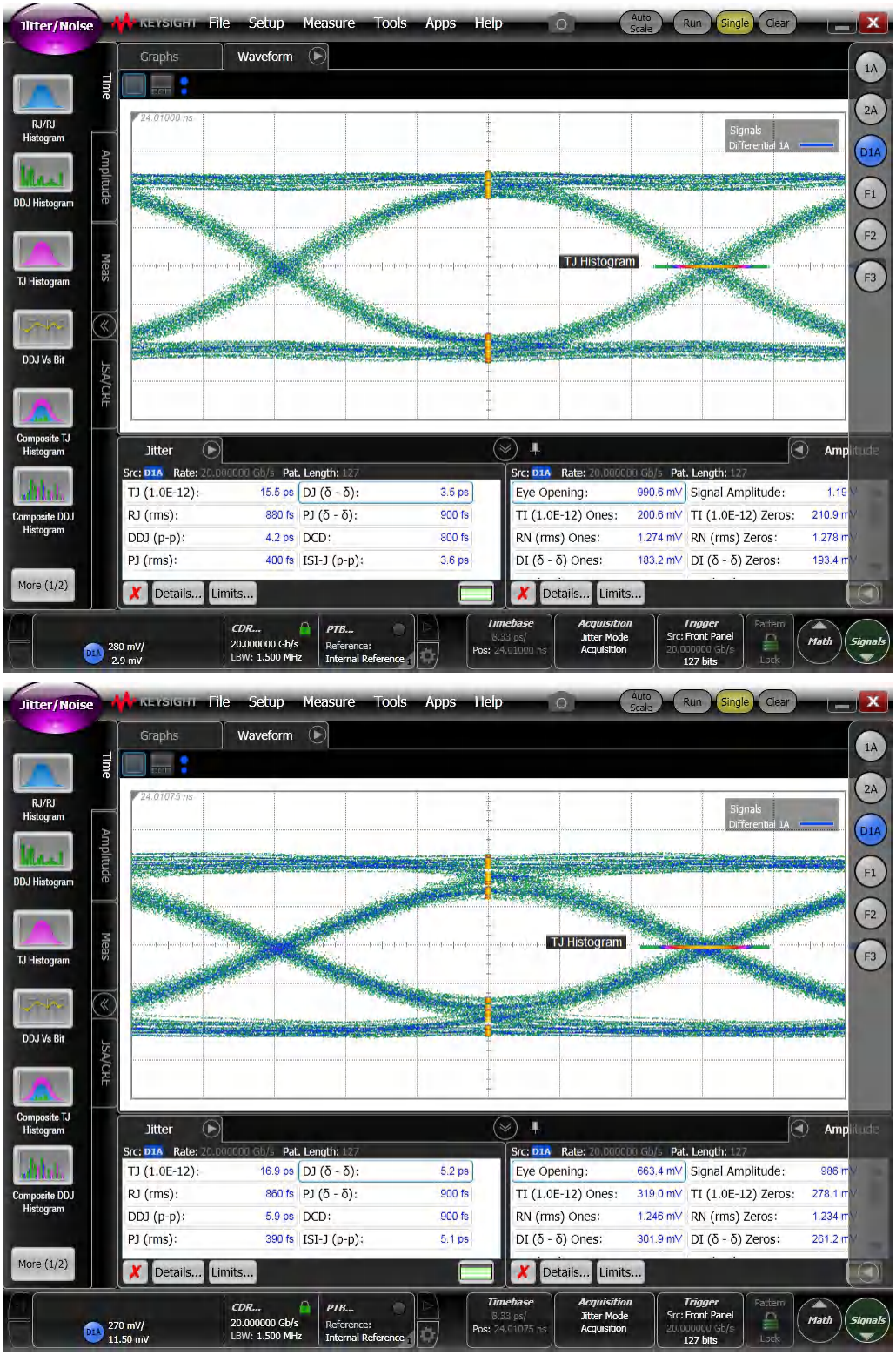


図 6-3. Jitter decomposition of 20 Gbps PRBS-7 signals in TI evaluation board - Top: through calibration traces, Bottom: through a typical TMUXHS4412 channels

7 Detailed Description

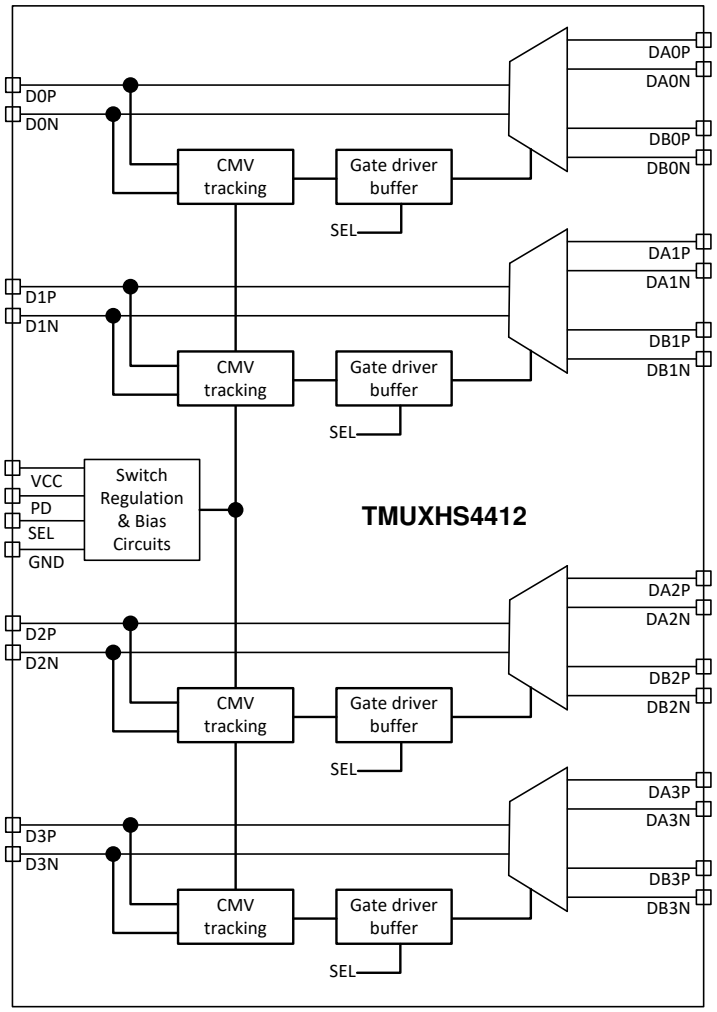
7.1 Overview

The TMUXHS4412 is a analog passive mux/demux that can work for any high-speed interface as long as its signaling is differential, has a common mode voltage (CMV) that is within valid range (0 to 1.8 V for 3.3 V supply voltage mode), and has amplitude up to 1800 mVpp-differential. It employs adaptive input voltage tracking that ensures the channel remains unchanged for the entire common mode voltage range. Two channels of the device can be used for electrical signals that have different CMV between them. Two channels can also be used such a way that the device switches two different interface signals with different data and electrical characteristics.

Excellent dynamic characteristics of the device allow high speed switching with minimum attenuation to the signal eye diagram with very little added jitter. While the device is recommended for the interfaces up to 20 Gbps, actual data rate where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained the device can potentially be used for higher data rates.

The TMUXHS4412 is only recommended for differential signaling. If the two signals on differential lines are completely un-correlated, then internal circuits can create certain artifacts. It is recommended to analyze the data line biasing of the device for such single ended use cases. The device parameters are characterized for differential signaling only.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Enable and Power Savings

The TMUXHS4412 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very-little current to achieve ultra low power in systems where power saving is critical. To enter standby mode, the PD control pin is pulled high through a resistor and must remain high. For active/normal operation, the PD control pin should be pulled low to GND or dynamically controlled to switch between H or L.

7.3.2 Data Line Biasing

The TMUXHS4412 has a weak pull-down of 1MΩ from D[0/1/2/3][P/N] pins to GND. While these resistors biases the device data channels to common mode voltage (CMV) of 0 V with very weak strength, it is recommended that the device is biased by a stronger impedance from either side of the device to a valid value. To avoid double biasing appropriate AC coupling capacitors should be ensured on either side of the device.

In certain use cases if both side of the TMUXHS4412 is ac coupled, it is recommended that appropriate CMV biasing is used for the device. 10 kΩ to GND or any other bias voltage in the CMV range for each D[0/1/2/3][P/N] pin will suffice for most use cases.

The high-speed data ports incorporate 20 kΩ pull-down resistors that are switched in when a port is not selected and switched out when the port is selected. For example when SEL = L, the DB[0/1/2/3][P/N] pins have 20 kΩ resistors to GND. The feature ensures that unselected port is always biased to a known voltage for long term reliability of the device and the electrical channel.

The positive and negative terminals of data pins D[0/1/2/3] have a weak (20 kΩ) differential resistor in between them for device switch regulation operation. This does not impact signal integrity or functionality of high speed differential signaling that typically has much stronger differential impedance (such as 100 Ω).

7.4 Device Functional Modes

表 7-1. Port Select Control Logic(1)

PORT D CHANNEL	PORT DA OR PORT DB CHANNEL CONNECTED TO PORT D CHANNEL	
	SEL = L	SEL = H
D0P	DA0P	DB0P
D0N	DA0N	DB0N
D1P	DA1P	DB1P
D1N	DA1N	DB1N
D2P	DA2P	DB2P
D2N	DA2N	DB2N
D3P	DA3P	DB3P
D3N	DA3N	DB3N

(1) The TMUXHS4412 can tolerate polarity inversions for all differential signals on Ports D, DA, and DB. In such flexible implementation one must ensure that the same polarity is maintained on Port D versus Ports DA/DB.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMUXHS4412 is an analog 4-channel high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The TMUXHS4412 can be used for many high speed interfaces including:

- Peripheral Component Interconnect Express (PCIe) Gen 1.0, 2.0, 3.0, 4.0
- USB 4.0
- Universal Serial Bus (USB) 3.2 Gen 1.0, 2.0
- Serial ATA (SATA/eSATA)
- Serial Attached SCSI (SAS)
- Display Port (DP) 1.4, 2.0
- Thunderbolt (TBT) 3.0
- Mipi Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- Low Voltage Differential Signalling (LVDS)
- Serdes Framer Interface (SFI)
- Ethenet Interfaces

The device's mux/demux selection pin SEL can easily be controlled by an available GPIO pin of a controller or hard tie to voltage level H or L as an application requires.

The TMUXHS4412 with adaptive voltage tracking technology can support applications where the common mode is different between the RX and TX pair. The switch paths of the TMUXHS4412 have internal weak pull-down resistors of 1 MΩ on the common port pins. While these resistors biases the device data channels to common mode voltage (CMV) of 0 V with a weak strength, it is recommended that the device is biased from either side of the device to a valid value (in the range of 0 - 1.8 V in 3.3 V supply voltage mode). It is expected that the system/ host controller and Device/End point common mode bias impedances are much stronger (smaller) than the TMUXHS4412 internal pull-down resistors; therefore, they are not impacted.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option to provide AC coupling. Avoid the 0603, 0805 size capacitors and C-packs. When placing AC coupling capacitors, symmetric placement is best. The capacitor value must be chosen according to the specific interface the device is being used. The value of the capacitor should match for the positive and negative signal pair. For many interfaces such as USB 3.2 and PCIe, the designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board. Depending upon the application and interface specifications, use the appropriate value for AC coupling capacitors.

The AC coupling capacitors have several placement options. Typical use cases warrant that the capacitors are placed on one side of the TMUXHS4412. In certain use cases, if both side of the TMUXHS4412 is ac coupled, it is recommended that appropriate CMV biasing is used for the device. 10 kΩ to GND or any other bias voltage in the valid CMV range for each D[0/1/2/3][P/N] pin of the common port suffice for most use cases. 図 8-1 shows a few placement options. Note for brevity not all channels are illustrated in the block diagrams. Some interfaces such as USB SS and PCIe recommends AC coupling capacitors on the TX signals before it goes to a connector. Option (a) features TX AC coupling capacitors on the connector side of the TMUXHS4412. Option (b) illustrates the capacitors on the host of the TMUXHS4412. Option (c) showcases where the TMUXHS4412 is ac coupled on both sides. VBIAS must be within the valid CMV of the device.

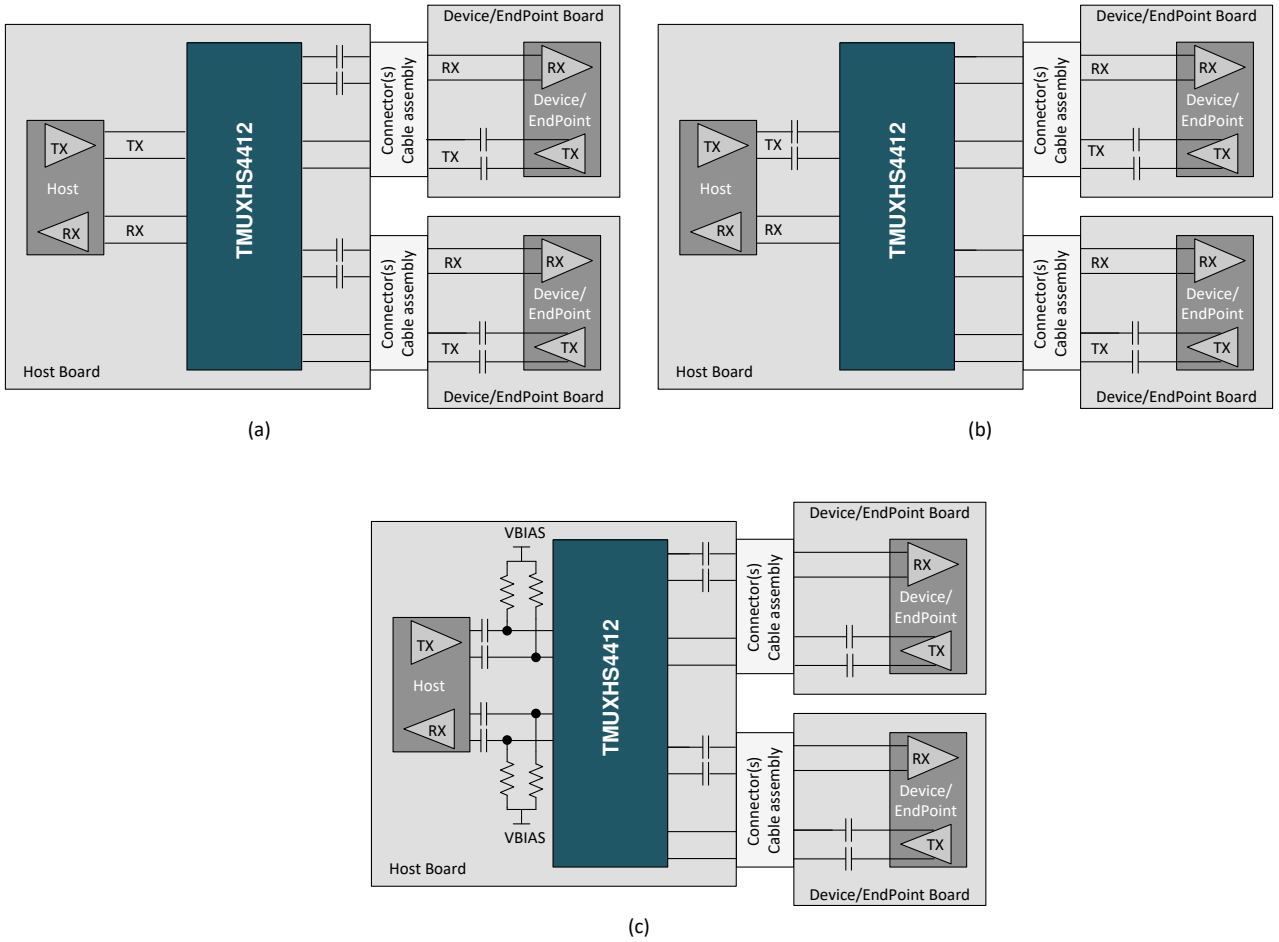


図 8-1. AC Coupling Capacitors Placement Options between Host and Device / Endpoint

8.2 Typical Applications

8.2.1 PCIe Lane Muxing

The TMUXHS4412 can be used to switch PCIe lanes between two slots. In many PC and server motherboards, the CPU does not have enough PCIe lanes to provide desired system flexibility for end customers. In such applications, the TMUXHS4412 can be used to switch PCIe TX and RX lanes between two slots. 図 8-2 provides a schematic where four TMUXHS4412 are used to switch eight PCIe lanes (8-TX and 8-RX channels). Note the common mode voltage (CMV) bias for the TMUXHS4412 must be within the valid range. In implementations where receiver CMV bias of a PCIe root complex or an end point can not be ensured within the CMV range, additional DC blocking capacitors and appropriate CMV biasing must be implemented. One side of the device has AC coupling capacitors. Additionally the PD pin must be low for device to work. This pin can be driven by a processor.

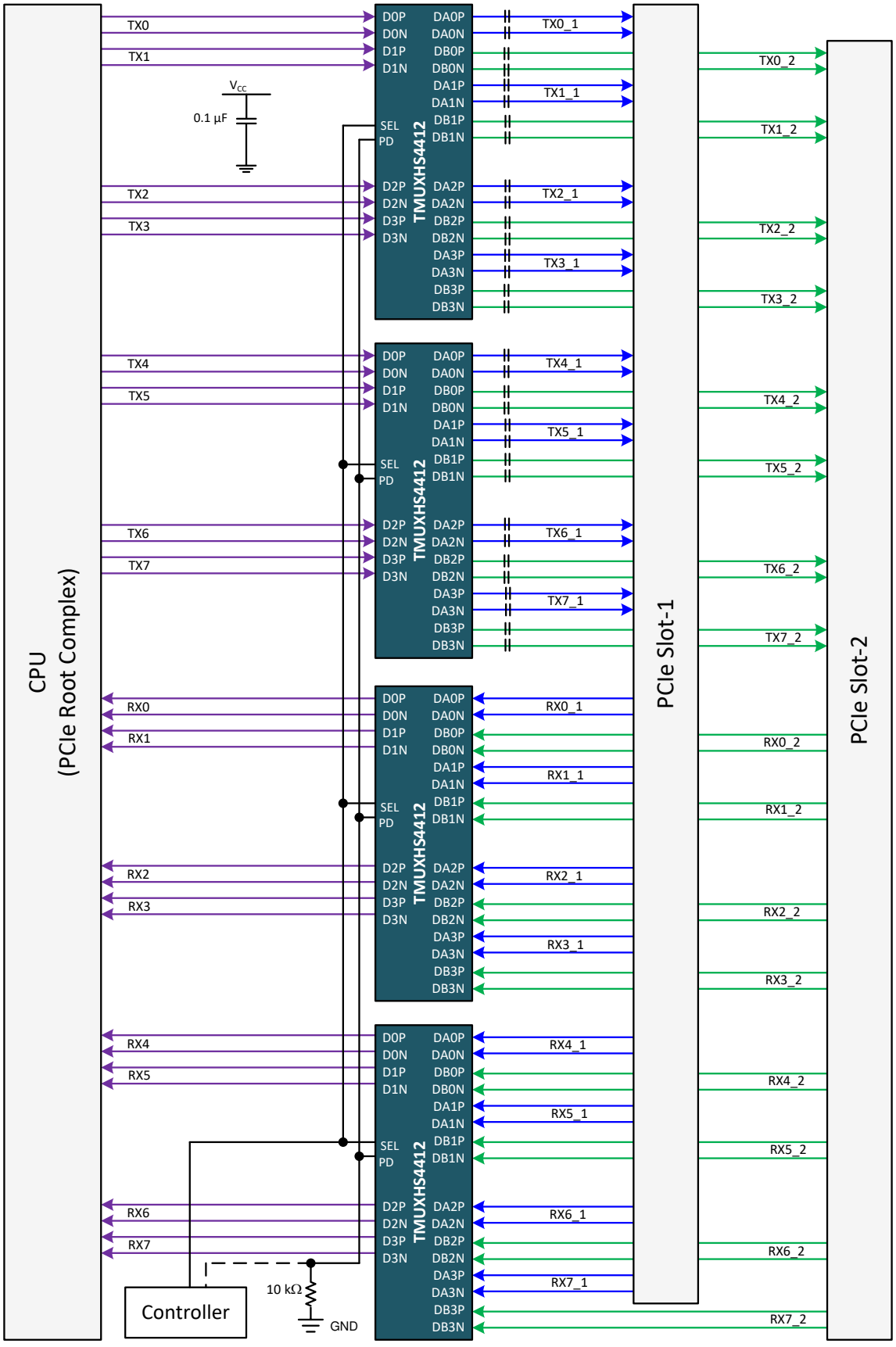


図 8-2. PCIe Lane Muxing

8.2.1.1 Design Requirements

表 8-1 provide various parameters and their expected values to implement the PCIe lane switching topology. Note the recommendation is for illustration purpose only.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE (V_{CC} = 3.3 V)	VALUE (V_{CC} = 1.8 V)
Dx[P/N], DAx[P/N], DBx[P/N] CM input voltage	0 V to 1.8 V	0 V to 0.9V Must be biased from Dx[P/N] side)
SEL/PD pin max voltage for low	<0.25*V_{CC}	
SEL/PD pin min voltage for high	>0.75*V_{CC}	
AC coupling capacitor for PCIe TX pins	75 nF to 265 nF	
Decoupling capacitor for V_{CC}	0.1 uF	

8.2.1.2 Detailed Design Procedure

The TMUXHS4412 is a high-speed passive switch device that can behave as a mux or demux. Because this is a passive switch, signal integrity is important because the device provides no signal conditioning capability. To implement PCIe lane swithing topology, the designer needs to understand the following.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and PD pins.
- The thermal pad must be connected to ground.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground.

8.2.1.3 Pin-to-pin Passive versus Redriver Option

For eight lane PCIe lane muxing application a topology with four TMUXHS4412 devices is illustrated. TMUXHS4412 is a passive mux/demux component that does not provide any signal conditioning. If a specific board implementation has too much loss from CPU to PCIe CEM connectors, a signal conditioning device such as linear redriver might be required for best fidelity of the PCIe link. *DS160PR421* is a PCIe 4.0 linear redriver with intergrated mux and *DS160PR412* is a PCIe 4.0 linear redriver with integrated demux. Both of these devices are pin-to-pin (p2p) compatible with TMUXHS4412 allowing easy transition if signal conditioing function is needed to extend the PCIe link reach. 図 8-3 illustrates p2p passive vs redriver option to implement PCIe lane switching.

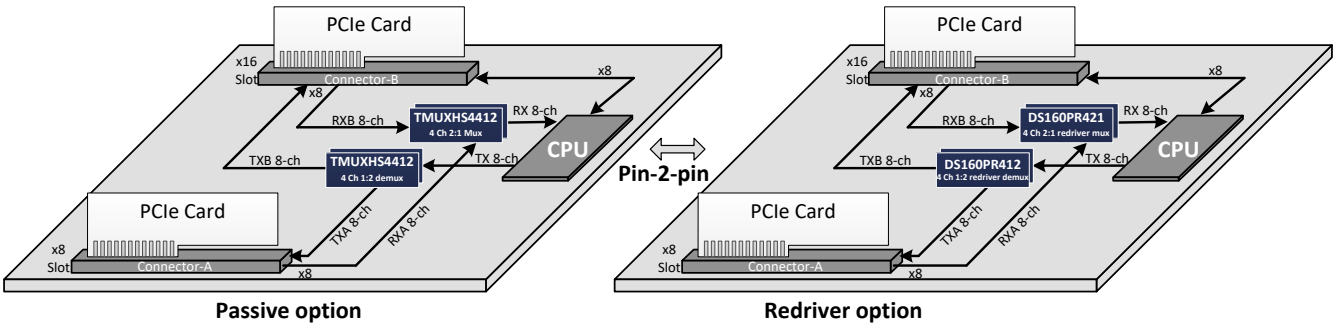


図 8-3. Pin-to-pin passive vs redriver option for PCIe lane switching

8.2.1.4 Application Curves

図 8-4 and 図 8-5 show eye diagrams for PRBS-7 signals though calibration trace and TMUXHS4412 for PCIe 3.0 (8 Gbps) and PCIe 4.0 (16 Gbps) respectively.

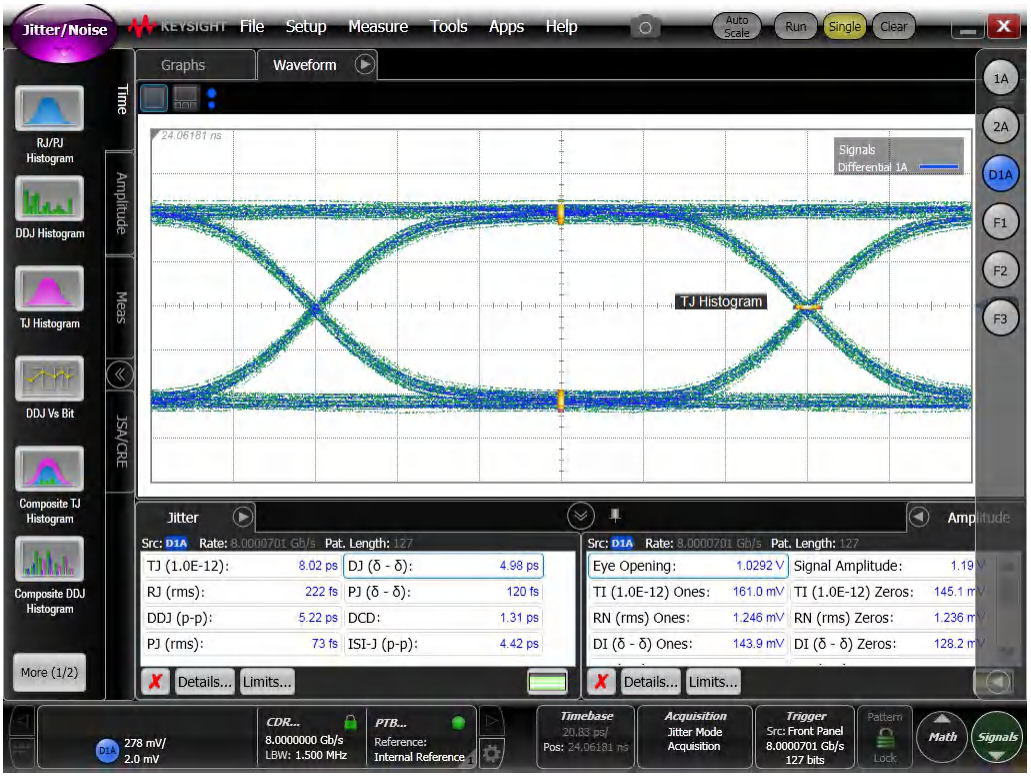
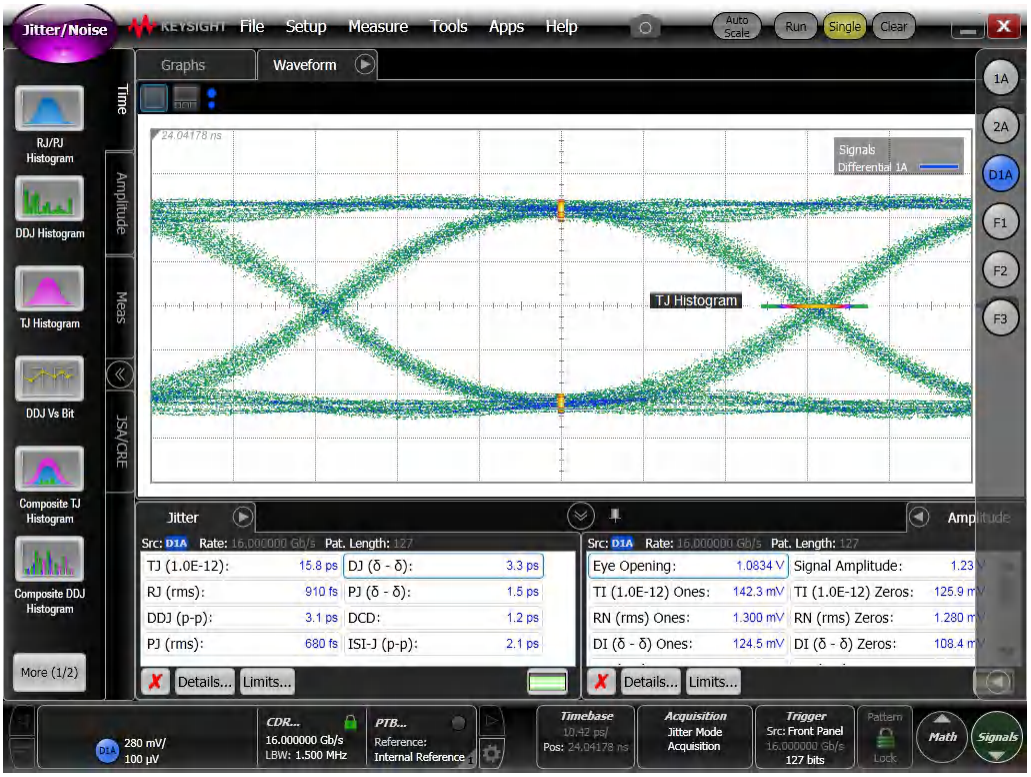


図 8-4. 8 Gbps PRBS-7 signals in TI evaluation board - Top: through calibration traces, Bottom: through a typical TMUXHS4412 channel



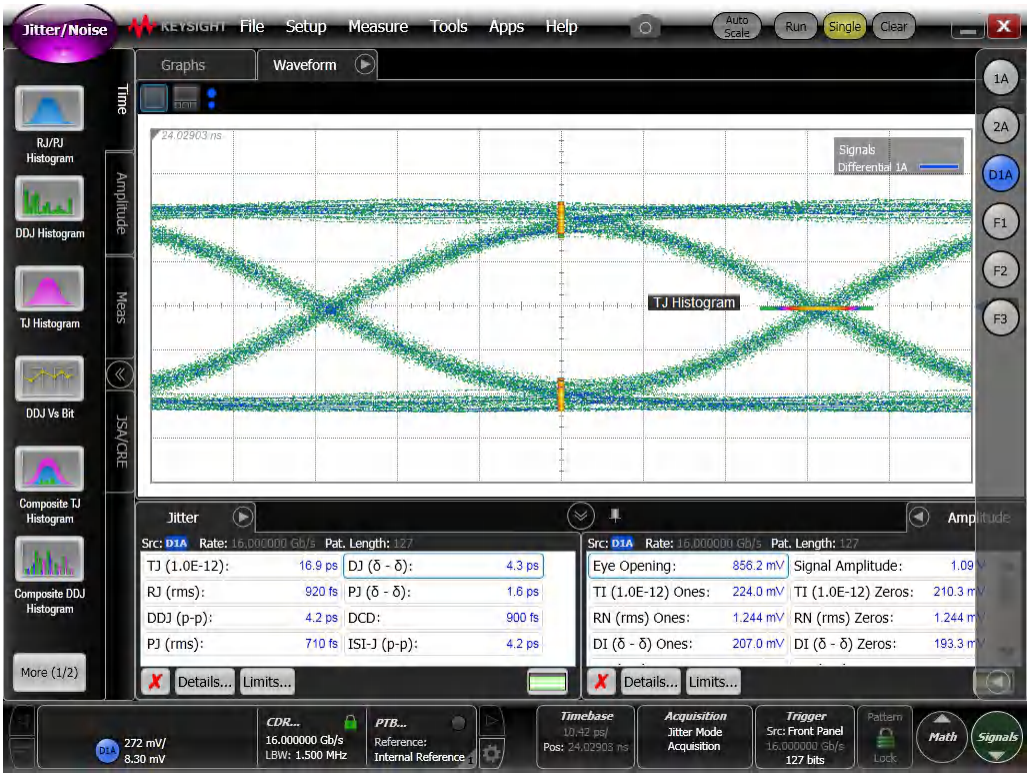


図 8-5. 16 Gbps PRBS-7 signals in TI evaluation board - Top: through calibration traces, Bottom: through a typical TMUXHS4412 channel

8.3 Systems Examples

8.3.1 PCIe Muxing for Hybrid SSD

図 8-6 illustrate a use case where a hybrid SSD is shared by CPU and an IO expander (PCH).

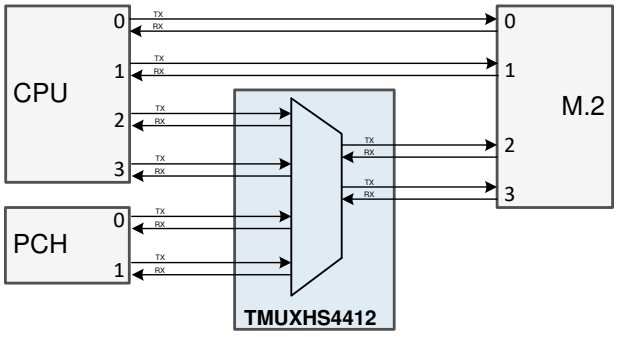


図 8-6. PCIe muxing to M.2 connectivity for hybrid SSD

8.3.2 DisplayPort Main Link

図 8-7 shows an application block diagram to implement DisplayPort (DP) main link switch either in mux or demux configuration. Note DP link also has sideband signals such as Auxiliary (AUX) and Hot Plug Detect (HPD) which must be switched outside of this device.

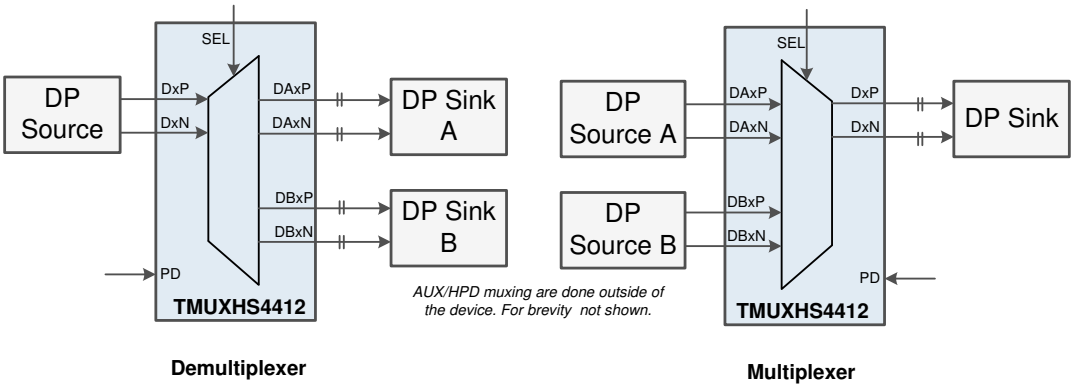


図 8-7. DisplayPort Main Link Demuxing/muxing

8.3.3 USB 4.0 / TBT 3.0 Demuxing

図 8-8 shows an application block diagram where TMUXHS4412 is used to demultiplex USB 4.0 / TBT 3.0 TX and TX signals. Note SBU signals within USB-C interface must be switched outside of this device.

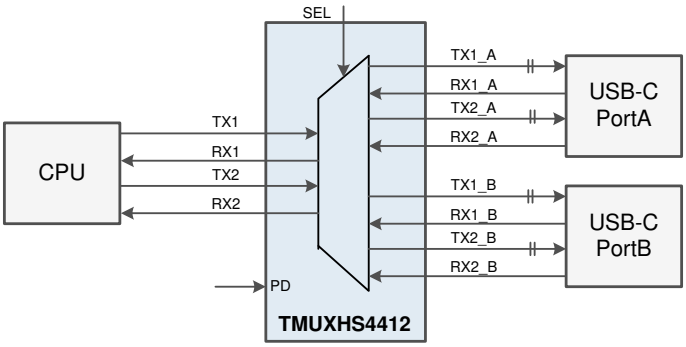


図 8-8. USB 4.0 / TBT 3.0 Demuxing

9 Power Supply Recommendations

The TMUXHS4412 does not require a power supply sequence. However, TI recommends that PD is asserted low after device supply VCC is stable and in specification. TI also recommends to place ample decoupling capacitors at the device VCC near the pin.

10 Layout

10.1 Layout Guidelines

On a high-K board, TI always recommends to solder the Power-pad™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the Power-pad package. On a high-K board, the TMUXHS4412 can operate over the full temperature range by soldering the Power-pad onto the thermal land without vias.

For high speed layout guidelines refer to *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*, SLLA414.

On a low-K board, for the device to operate across the temperature range, the designer must use a 1-oz Cu trace connecting the GND pins to the thermal land. A general PCB design guide for Power-pad packages is provided in *Power-pad Thermally-Enhanced Package*, SLMA002.

10.2 Layout Example

図 10-1 shows TMUXHS4412 layout example.

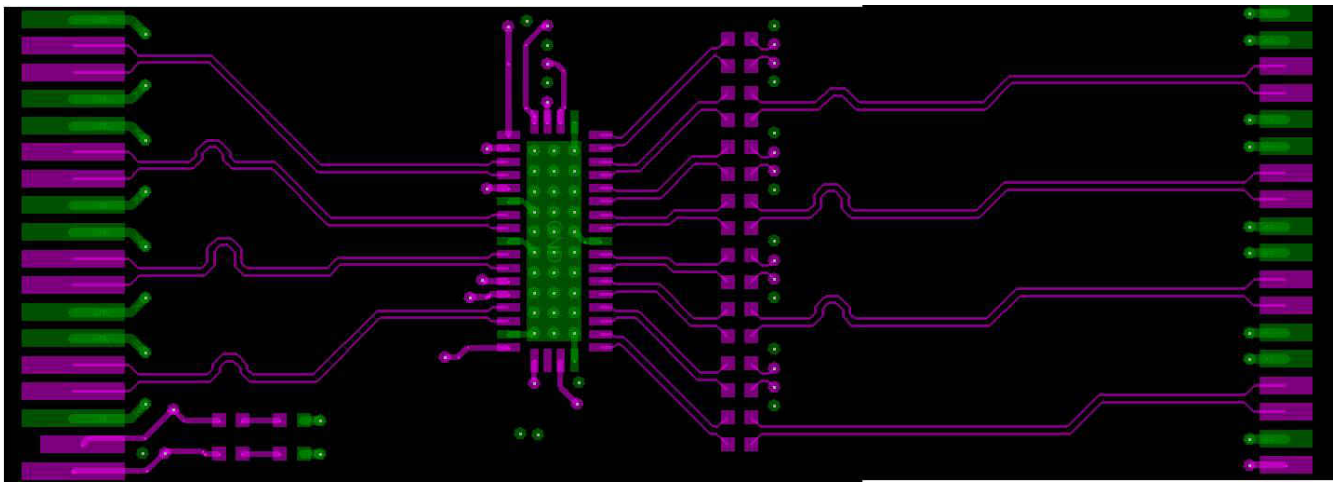


図 10-1. TMUXHS4412 layout example

図 10-2 shows a layout illustration here four TMUXHS4412 is used to switch eight PCIe lanes between two PCIe connectors.

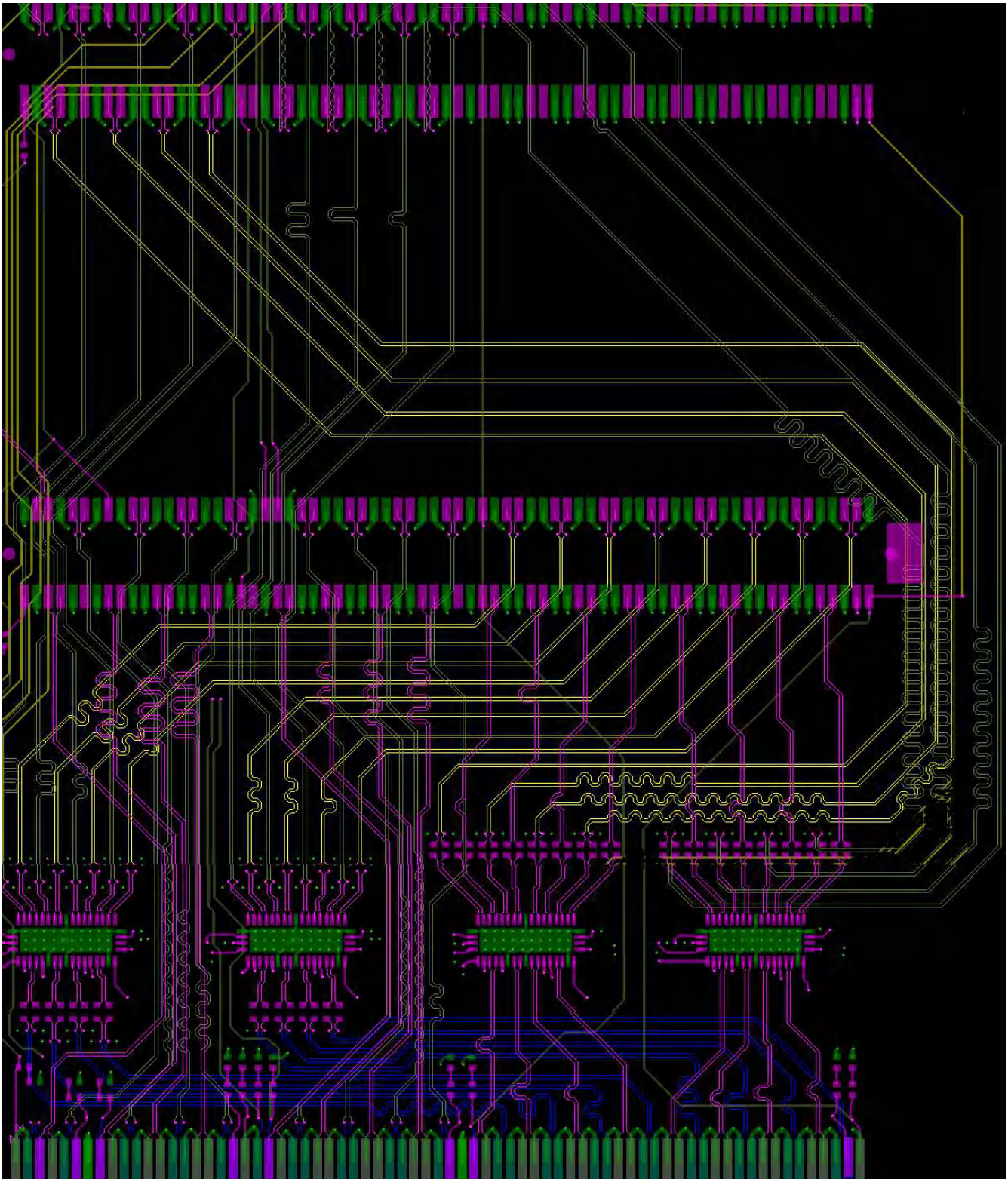


図 10-2. Layout example for PCIe lane muxing application

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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11.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUXHS4412IRUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HS4412	Samples
TMUXHS4412IRUAT	ACTIVE	WQFN	RUA	42	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HS4412	Samples
TMUXHS4412RUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS4412	Samples
TMUXHS4412RUAT	ACTIVE	WQFN	RUA	42	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS4412	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

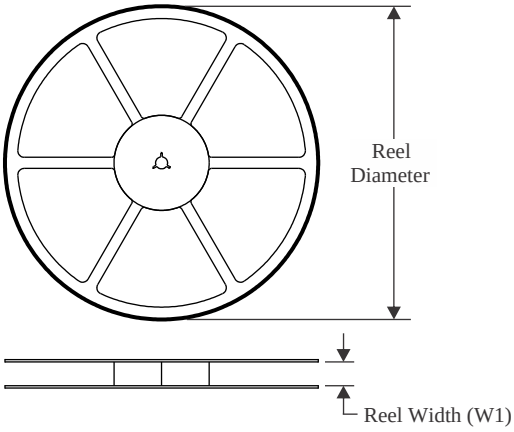
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

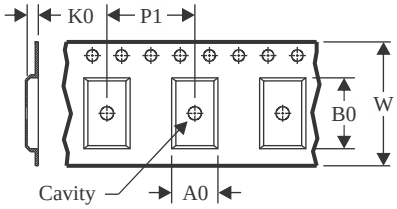
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

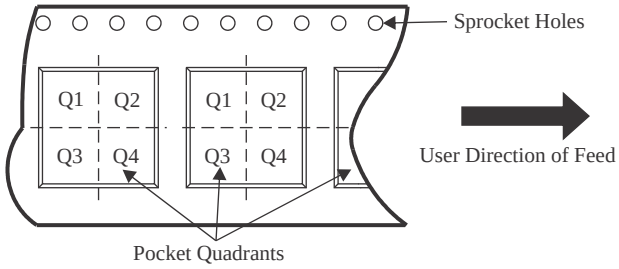


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

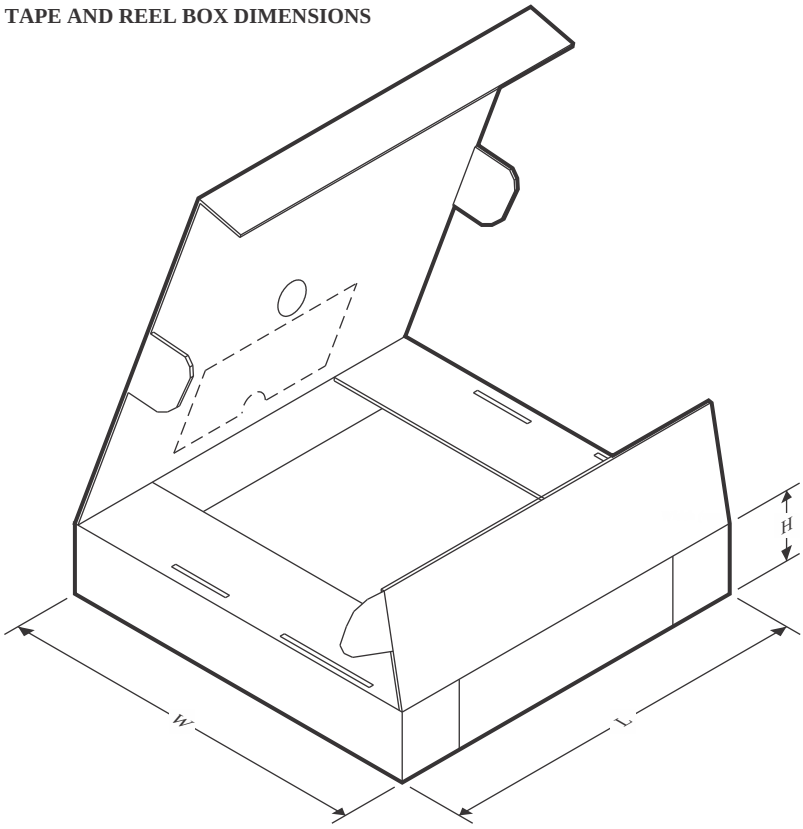
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS4412IRUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TMUXHS4412IRUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TMUXHS4412RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TMUXHS4412RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS4412IRUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
TMUXHS4412IRUAT	WQFN	RUA	42	250	210.0	185.0	35.0
TMUXHS4412RUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
TMUXHS4412RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

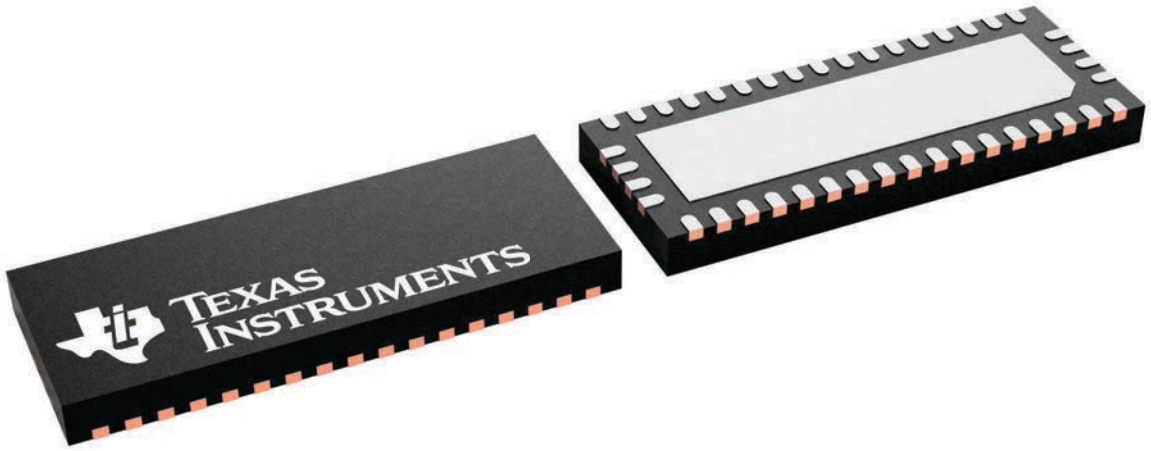
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

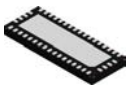
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



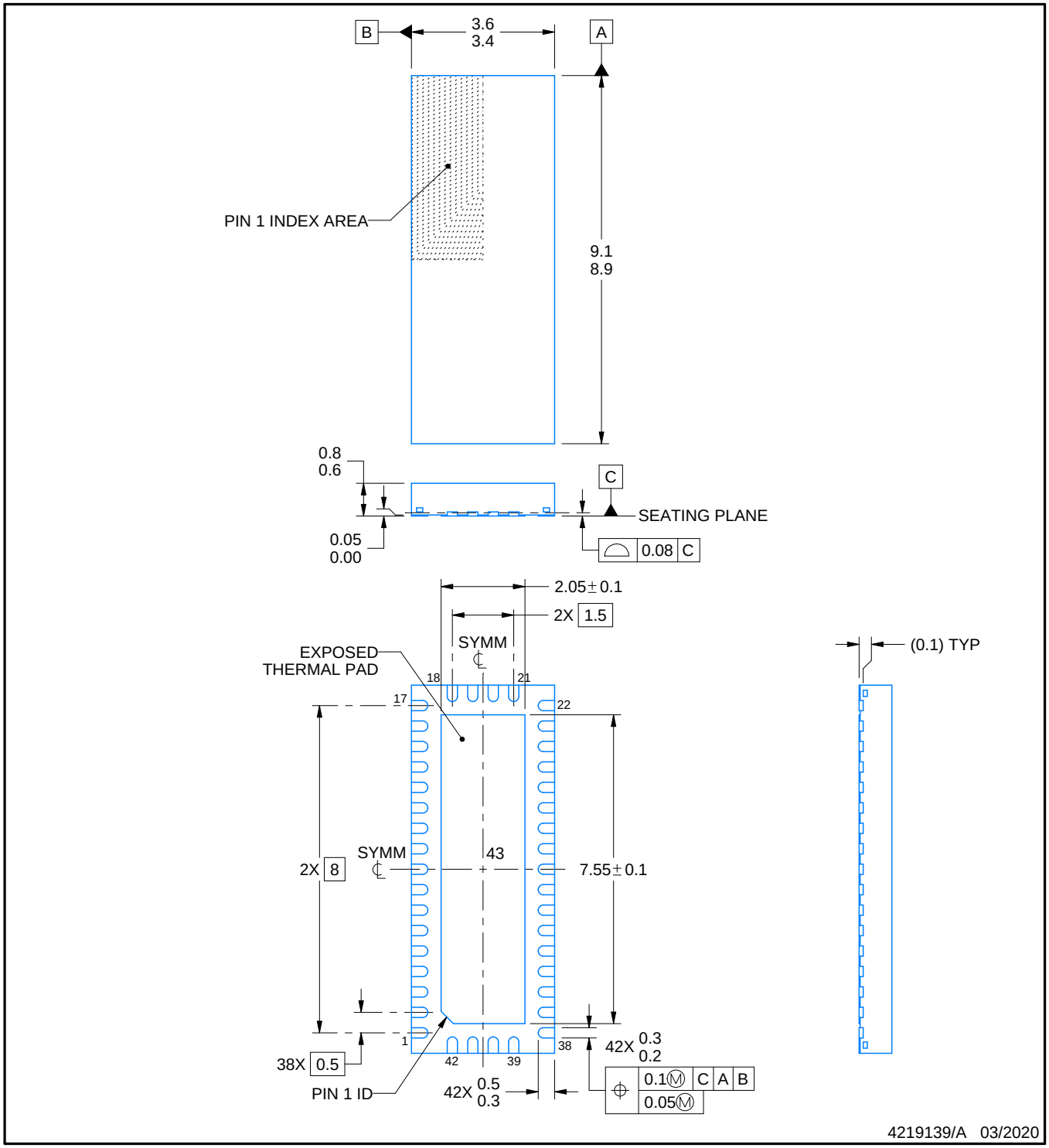
PACKAGE OUTLINE

RUA0042A



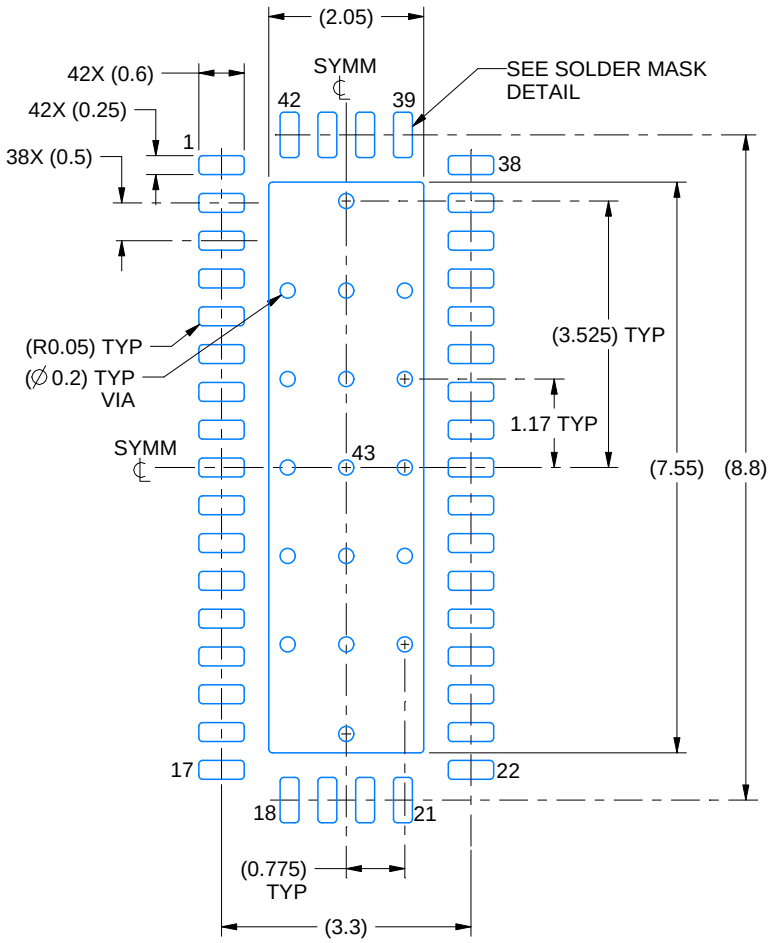
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

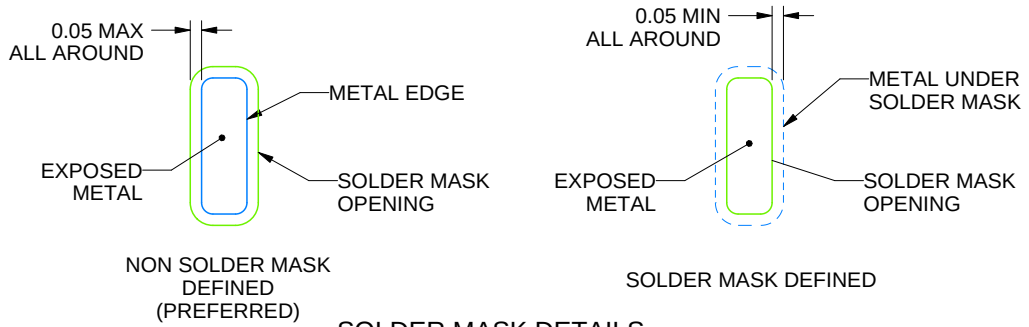


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4219139/A 03/2020

NOTES: (continued)

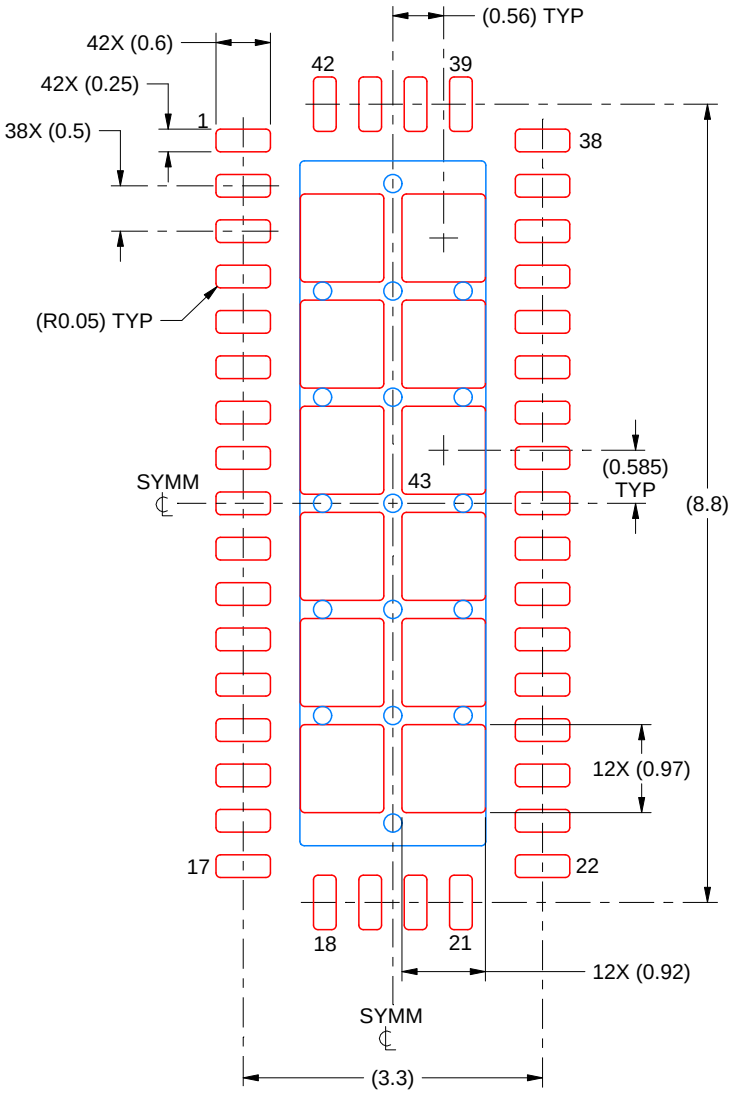
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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