TPD1E10B09 シングル・チャネル ESD 保護デバイス、0402 パッケージ

1 特長

- 最大 ±9V の I/O インターフェイスに対するシステムレベルの ESD 保護を実現
- IEC 61000-4-2 レベル 4:
  - ±20kV (空中放電)
  - ±20kV (接触放電)
- IEC 61000-4-5 サージ保護:
  - 4.5A (8/20µs)
- I/O 容量:10pF (標準値)
- R_{DYN}:0.5ω (標準値)
- DC ブレークダウン電圧:±9.5V (最小値)
- 超低リーク電流:100nA (最大値)
- 13V のクランプ電圧 (I_{PP} = 1A での最大値)
- 産業用温度範囲:-40℃～125℃
- 省スペースの 0402 フットプリント
  (1mm × 0.6mm × 0.5mm)

2 アプリケーション

- 最終製品:
  - タブレット
  - リモート・コントローラ
  - ウェアラブル
  - セットトップ・ボックス
  - 電子 POS (EPOS)
  - 電子書籍
- インターフェイス:
  - オーディオ・ライン
  - 押しボタン
  - 汎用入出力 (GPIO)

3 概要

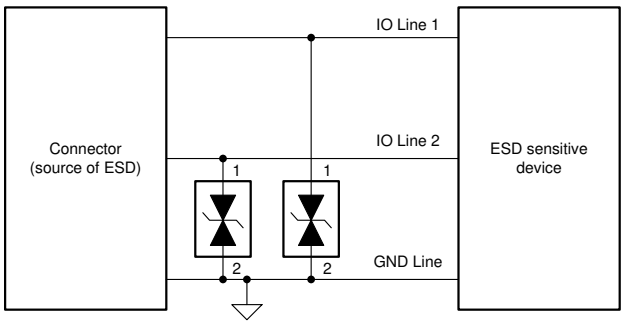
TPD1E10B09 デバイスは、小型の 0402 パッケージに搭載されたシングル・チャネルの静電放電 (ESD) 過渡電圧抑制 (TVS) ダイオードです。この ESD 保護ダイオードは、±20kV IEC 61000-4-2 (レベル 4) の接触および空中 ESD 保護を提供します。バック・ツー・バックの TVS ダイオード構成により、バイポーラまたは双方向の信号をサポートできます。10pF のライン容量は、最大 500Mbps のデータ・レートに対応する各種アプリケーションに適しています。0402 パッケージは業界標準であり、スペースに制約のあるアプリケーションでの部品配置に便利です。

この ESD 保護 TVS ダイオードの代表的なアプリケーションは、オーディオ・ライン (マイク、イヤホン、スピーカホン)、SD インターフェイス、キーパッドやその他のボタン、USB ポートの V_{BUS} ピンと ID ピン、汎用 I/O ポートの回路保護です。この ESD クランプは、電子書籍、タブレット、リモート・コントローラ、ウェアラブル、セットトップ・ボックス、デンス POS 機器などの最終製品の保護に適しています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(1)
TPD1E10B09	DPY (X1SON、2)	1mm × 0.6mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2015) to Revision E (September 2023) — **Page**

- 「パッケージ情報」表のフォーマットを更新し、パッケージ・リード・サイズを追加 ... 1
- ドキュメント全体にわたって表、図、相互参照の採番方法を変更 ... 1

Changes from Revision C (June 2015) to Revision D (August 2015) — **Page**

- Added capacitive measurement frequency ... 5

Changes from Revision B (October 2012) to Revision C (June 2015) — **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

Changes from Revision A (March 2012) to Revision B (October 2012) — **Page**

- Added *Thermal Information* table ... 4

Changes from Revision * (February 2012) to Revision A (March 2012) — **Page**

- 「特長」セクションを更新 ... 1
- Added graphs to *Typical Characteristics* section ... 6
- Added APPLICATION INFORMATION section ... 9

5 Pin Configuration and Functions

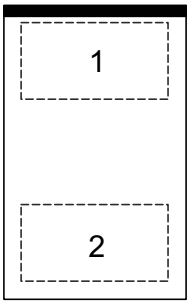


図 5-1. DPY Package, 2-Pin X1SON (Top View)

表 5-1. Pin Functions

PIN	TYPE(1)	DESCRIPTION
1	I/O	ESD protected I/O
2		

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
	Operating temperature	–40	125	°C
I_{PP}	Peak pulse current (tp = 8/20 µs)		4.5	A
P_{PP}	Peak pulse power (tp = 8/20 µs)		90	W
T_{stg}	Storage temperature	–65	155	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[1]	±1000	
		IEC 61000-4-2 Contact Discharge	20000	
		IEC 61000-4-2 Air-Gap Discharge	20000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		–40		125	°C
Operating voltage	Pin 1 to 2 or pin 2 to 1	–9		9	V

6.4 Thermal Information

THERMAL METRIC[1]		TPD1E10B09 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	615.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	404.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	493.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	127.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	493.3	°C/W
P	Power Dissipation[1]	162	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Max junction temperature: 125°C; power dissipation calculated at 25°C ambient temperature using JEDEC High K board Standard. Not to be used for steady state power dissipation in the breakdown region.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	Pin 1 to 2 or pin 2 to 1			9	V
I_{LEAK}	Leakage current	Pin 1 = 5 V, pin 2 = 0 V			100	nA
VClamp1,2	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	I_{PP} = 1 A, tp = 8/20 µSec(1)			13	V
		I_{PP} = 5 A, tp = 8/20 µSec(1)			17	
VClamp2,1	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	I_{PP} = 1 A, tp = 8/20 µSec(1)			13	V
		I_{PP} = 4.5 A, tp = 8/20 µSec(1)			20	
R_{DYN}	Dynamic resistance	Pin 1 to pin 2(1)		0.5		Ω
		Pin 2 to pin 1(1)		0.5		
C_{IO}	I/O capacitance	V_{IO} = 2.5 V; *f* = 1 MHz		10		pF
$V_{BR1,2}$	Break-down voltage, pin 1 to pin 2	I_{IO} = 1 mA	9.5			V
$V_{BR2,1}$	Break-down voltage, pin 2 to pin 1	I_{IO} = 1 mA	9.5			V

(1) Extraction of R_{DYN} using least squares fit of TLP characteristics from I_{PP} = 10 A to I_{PP} = 20 A.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

6.6 Typical Characteristics

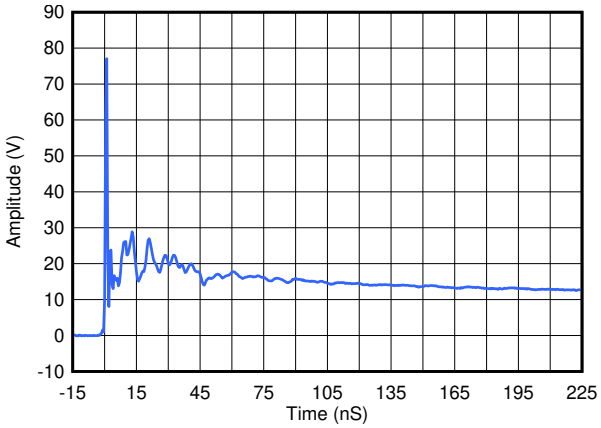


図 6-1. ESD Clamp Voltage +8 kV Contact ESD

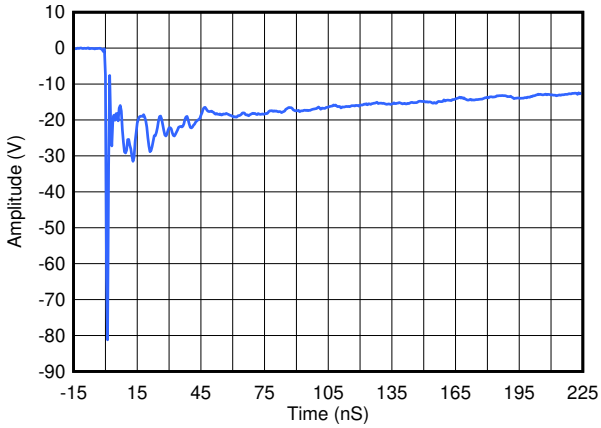


図 6-2. ESD Clamp Voltage –8 kV Contact ESD

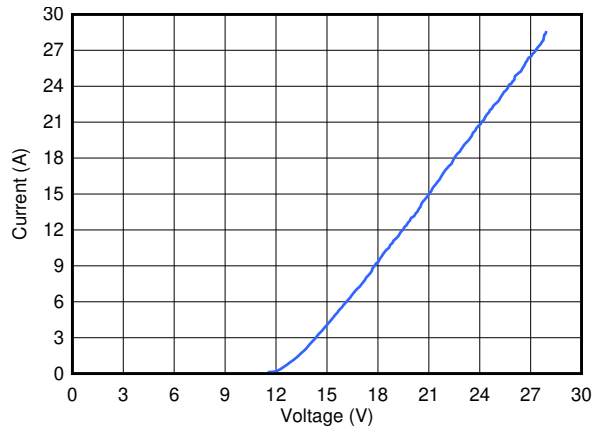


図 6-3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

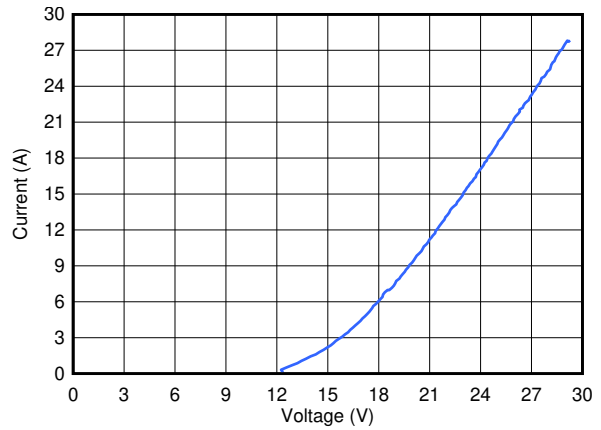


図 6-4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

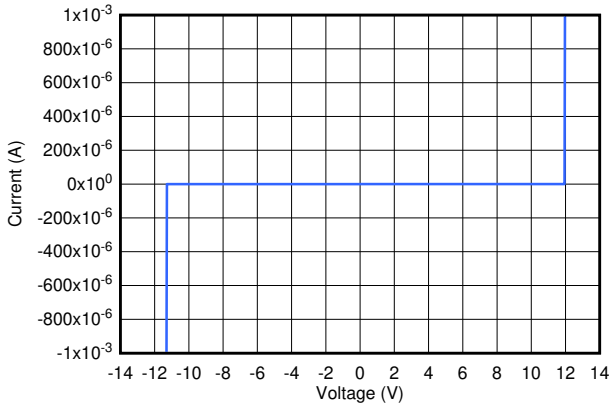


図 6-5. IV Curve

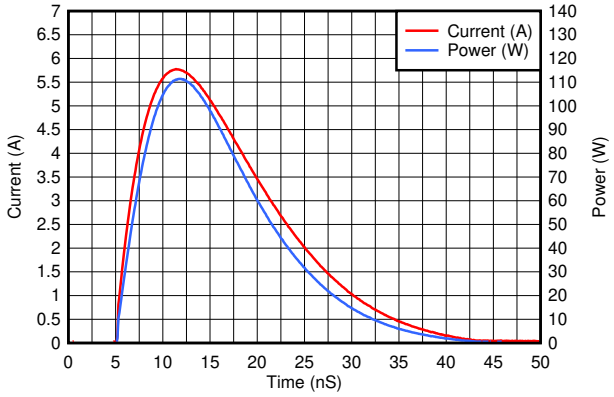


図 6-6. Positive Surge Waveform 8/20 µs

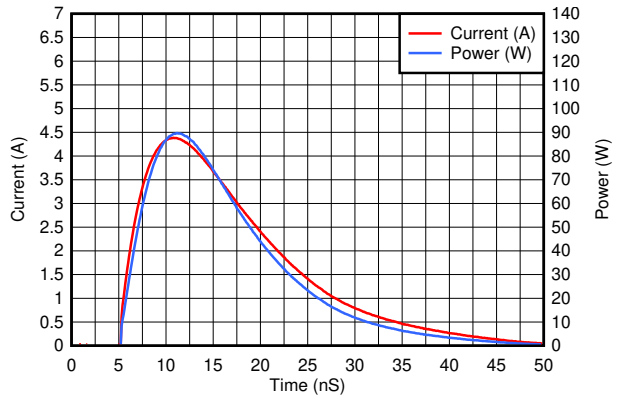


図 6-7. Negative Surge Waveform 8/20 µs

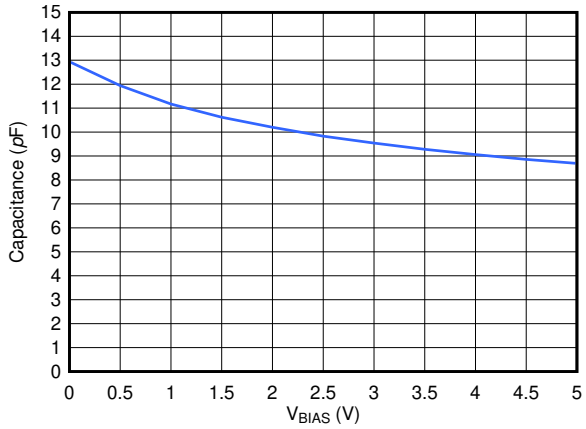


図 6-8. Pin Capacitance Across V_{BIAS}

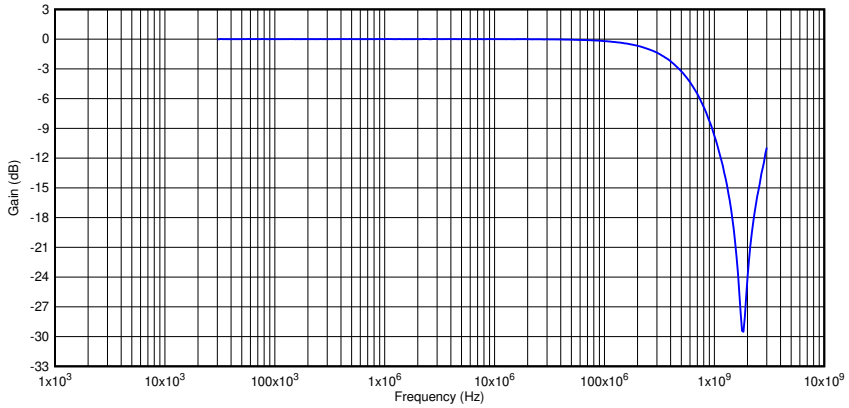


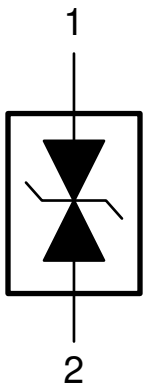
図 6-9. Insertion Loss

7 Detailed Description

7.1 Overview

TPD1E10B09 is a single-channel ESD TVS that provides ±20-kV IEC 61000-4-2 (Level 4) contact and air-gap ESD protection. The 10-pF back-to-back diode architecture is suitable for signals that range from –9 V to 9 V and supports data rates up to 500 Mbps. The industry-standard 0402 package is convenient for placement in applications with limited space.

7.2 Functional Block Diagram



7.3 Feature Description

TPD1E10B09 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ±20-kV contact and ±20-kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 4.5-A surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 10 pF supports a data rate up to 500 Mbps. This clamping device has a small dynamic resistance of 0.5 Ω typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 13 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO, especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the V_{RWM}. The industrial temperature range of –40°C to 125°C makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

7.4 Device Functional Modes

TPD1E10B09 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below V_{RWM} and activates when the voltage between pin 1 and pin 2 goes above V_{BR}. During IEC ESD events, transient voltages as high as ±20 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPD1E10B09 is a single-channel back-to-back diode that protects one bidirectional signal line from electrostatic discharge and surge pulses. Because the diode is bidirectional, TPD1E10B09 protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10-pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode should be placed very close to the external connector for optimal performance. It is best to place the diode on the line that it is protecting.

Layout: Pin 1 of the diode should be right over the protected signal line. There should a thick and short trace from pin 2 to ground. For an example, see the *Layout* section.

8.2 Typical Application

A system with a human interface is vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E10B09 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

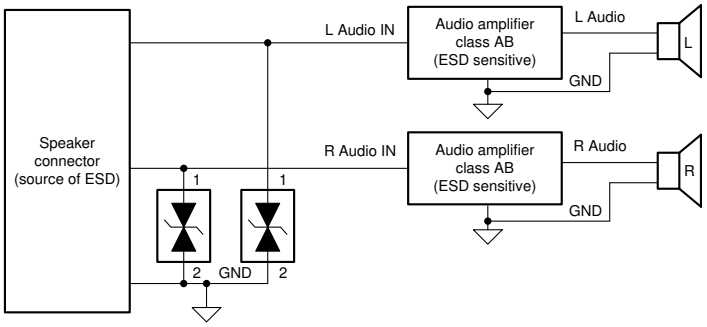


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, two TPD1E10B09s will be used to protect left and right audio channels. Table 1-1 lists the known system parameters for this audio application.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	–8 V to 8 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±15-kV Contact/ ±15-kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, consider the following parameters:

- Ensure the voltage range on the protected line does not exceed the reverse standoff voltage of the TVS diodes (V_{RWM}).
- Ensure the operating frequency is supported by the I/O capacitance (C_{IO}) of the TVS diode.
- Ensure the IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is –8 V to 8 V. The V_{RWM} for the TVS is –9.5 V to 9.5 V; therefore, the bidirectional TVS will not break down during normal operation, and normal operation of the audio signal will not be affected due to the signal voltage range. In this application, a bidirectional TVS like TPD1E10B09 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; filter the TVS I/O capacitance so that it does not distort this signal. With TPD1E10B09 typical capacitance of 10 pF, which leads to a typical cutoff frequency of just under 500 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires protection for ±15-kV Contact and ±15-kV Air-Gap ESD, which is above the standard Level 4 IEC 61000-4-2 system-level ESD protection. A standard TVS cannot survive this level of IEC ESD stress. However, TPD1E10B09 can survive at least ±20-kV Contact and ±20-kV Air-Gap ESD. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. For instructions on properly laying out TPD1E10B09, see *Layout*.

8.2.3 Application Curves

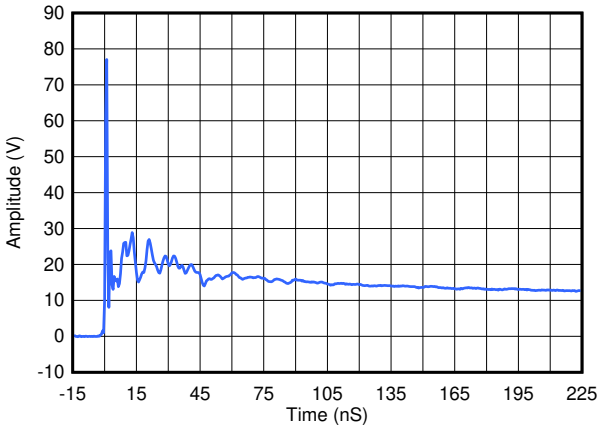


図 8-2. ESD Clamp Voltage +8-kV Contact ESD

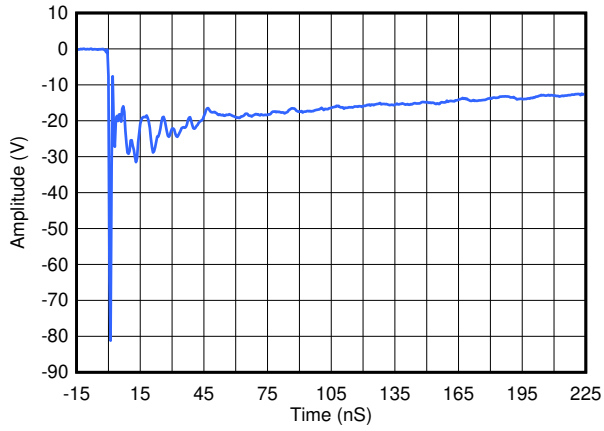


図 8-3. ESD Clamp Voltage –8-kV Contact ESD

8.3 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Do not violate the maximum specifications for each pin.

8.4 Layout

8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Use rounded corners with the largest radii possible on the protected traces between the TVS and the connector, thus eliminating any sharp corners.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path.

8.4.2 Layout Example

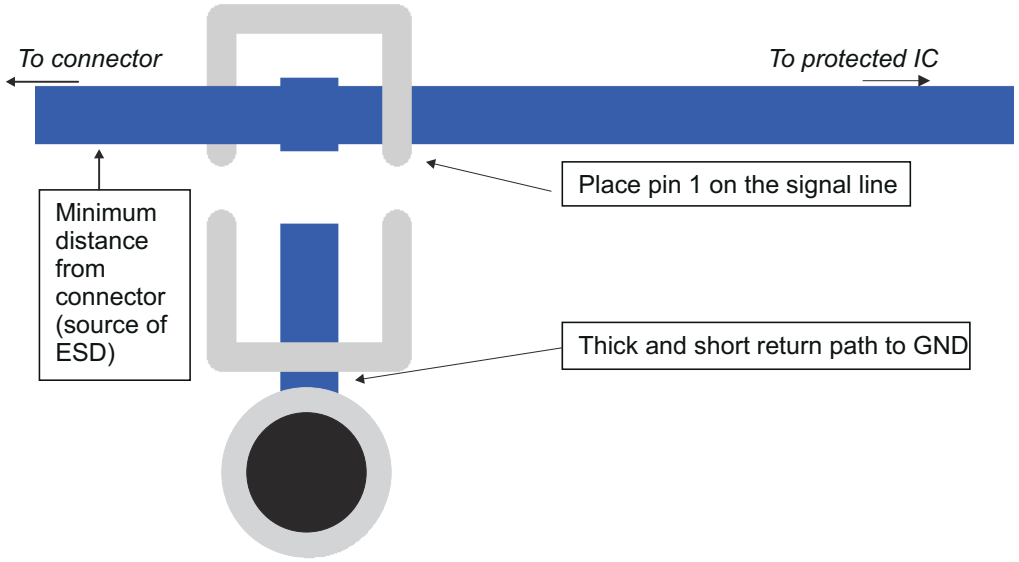


図 8-4. Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E10B09DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A1, A2, A5, A6, BJ)	Samples
TPD1E10B09DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		(A1, A2, A6, BJ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD1E10B09 :

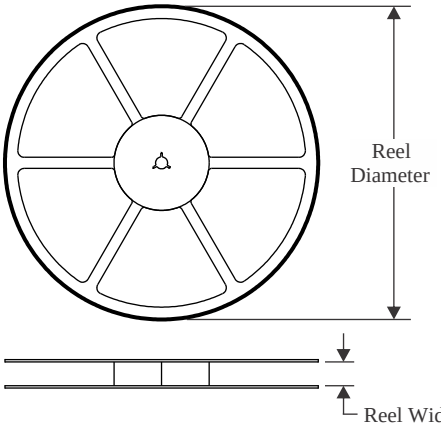
- Automotive : TPD1E10B09-Q1

NOTE: Qualified Version Definitions:

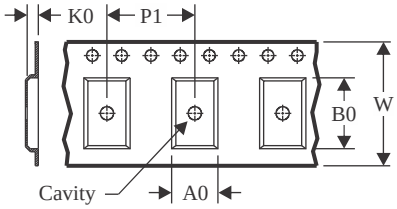
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

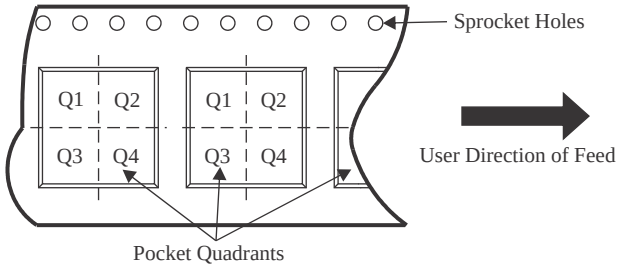


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

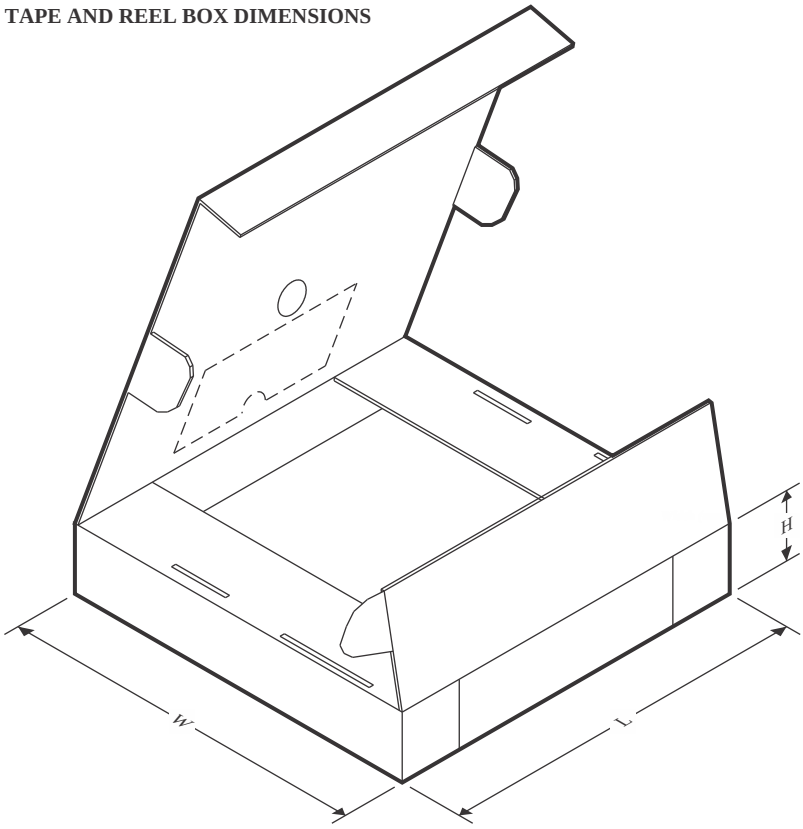
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

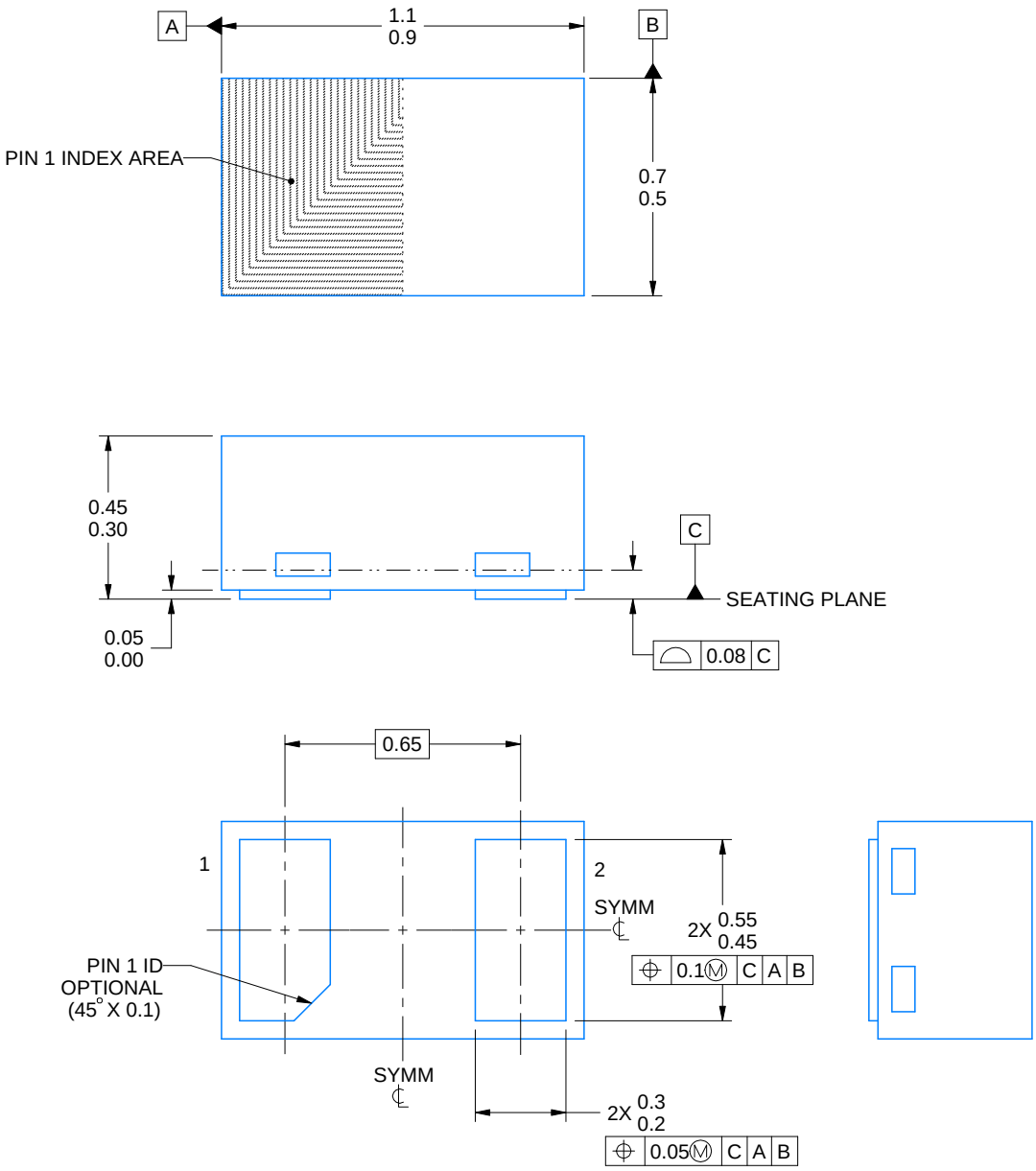
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B09DPYT	X1SON	DPY	2	250	189.0	185.0	36.0
TPD1E10B09DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E10B09DPYT	X1SON	DPY	2	250	205.0	200.0	33.0

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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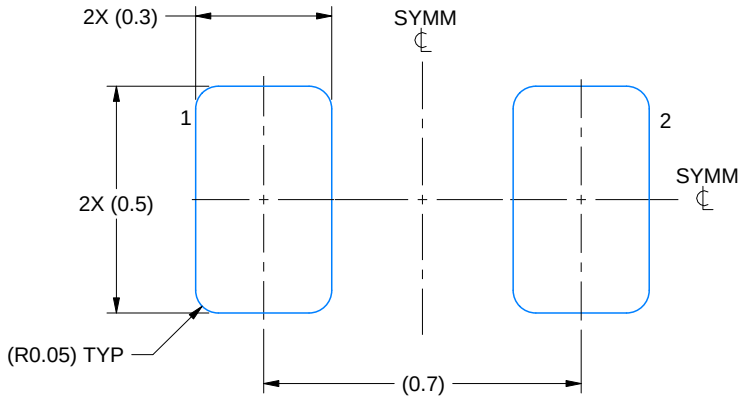
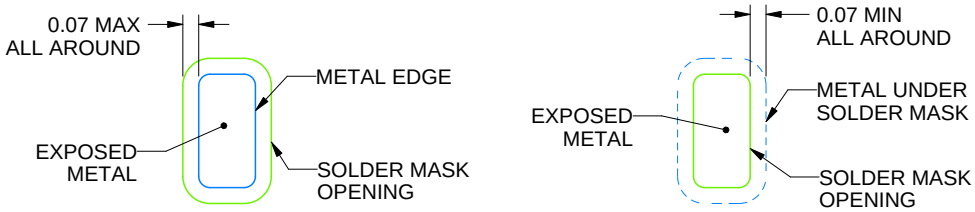
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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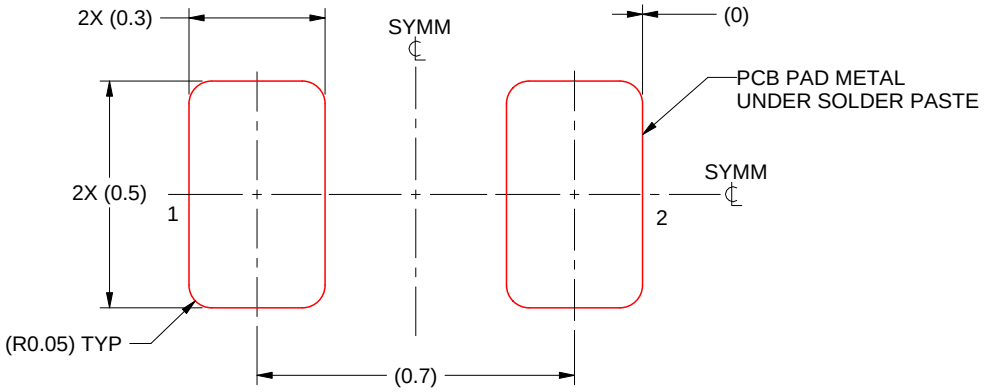
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265