

TPD2S017 2 チャンネル、超低クランプ電圧 ESD ソリューション、直列抵抗付き

1 特長

- クランプ電圧が非常に低いため、ESD イベント時に超低電圧コア・チップセットを確実に保護できます
- IEC 61000-4-2 ESD 保護
- 直列抵抗 ($R = 1\Omega$) のマッチング $\pm 8m\Omega$ (標準値)
- 差動チャンネル入力容量で $0.02pF$ (標準値) のマッチング
- 高周波数 ($-3dB$ 帯域幅、 $\approx 3GHz$) での高速データレートと EMI フィルタの動作
- 6 ピンの小型トランジスタ [SOT-23 (DBV)] パッケージで供給されます
- 使いやすいストレート・ルーティング・パッケージ

2 アプリケーション

- 高速 USB
- IEEE 1394 インターフェイス
- 低電圧差動信号伝送 (LVDS)
- モバイル・ディスプレイ・デジタル・インターフェイス (MDDI) およびモバイル産業用プロセッサ・インターフェイス (MIPI)
- HS 信号

3 概要

TPD2S017 は、2 チャンネルの静電気放電 (ESD) 保護デバイスです。この保護製品は、各ラインに 2 段の ESD 過渡電圧抑制 (TVS) ダイオードを提供し、通常 1Ω の直列抵抗絶縁を実現します。このアーキテクチャにより、デバイスはシステム・レベルの ESD 衝撃時に非常に低い電圧にクランプできます。

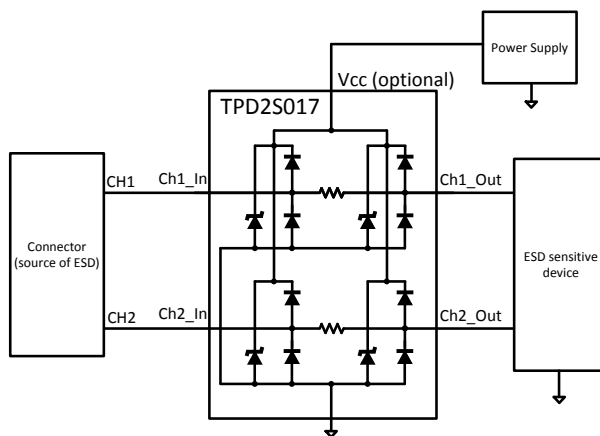
TPD2S017 は、IEC61000-4-2 ESD 保護規格に準拠しています。直列抵抗部品のために、TPD2S017 には制御されたフィルタのロールオフが含まれており、さらに強力なスプリアス EMI 抑制とシグナル・インテグリティが得られます。モノリシックなシリコン・テクノロジーにより、差動信号ペア間のクランプ容量や直列抵抗など、部品の値を適切にマッチングすることができます。ライン容量と直列抵抗の厳密なマッチングにより、追加された ESD クランプによる差動信号の歪みが最小限に抑えられ、本デバイスは高速差動データ速度 ($1.5Gbps$ 超過) で動作することができます。DBV パッケージはフロースルー・ピン・マッピングにより、基板レイアウトを容易にします。

この ESD 保護デバイスの代表的なアプリケーションは、USB データ・ライン、IEEE 1394 インターフェイス、LVDS、MDDI/MIPI、HS 信号に対する回路保護です。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPD2S017	DBV (SOT-23, 6)	2.90mm × 1.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション回路図



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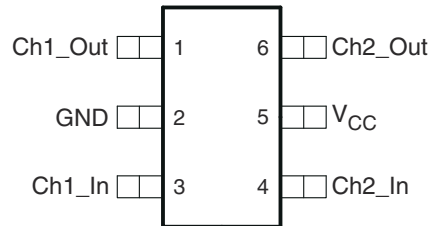
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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2015) to Revision C (January 2023)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated the maximum IO voltage for V_{IO} from 5 V to 6 V in the <i>Absolute Maximum Ratings</i> section.....	4
• Updated the maximum operating voltage for V_{CC} from 5 V to 5.5 V in the <i>Recommended Operating Conditions</i> section.....	4
Changes from Revision A (July 2015) to Revision B (December 2015)	Page
• Added $f = 10\text{ MHz}$ to the test condition of <i>IO capacitance</i> in the <i>Electrical Characteristics</i> table	4
Changes from Revision * (September 2009) to Revision A (July 2015)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1

5 Pin Configuration and Functions



**図 5-1. DBV Package
6-Pin SOT-23
Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Ch1_In	3	I	High-speed ESD clamp input
Ch2_In	4		
Ch1_Out	1	O	High-speed ESD clamp output
Ch2_Out	6		
GND	2	—	Ground
V _{CC}	5	—	Optional power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{IO}	IO voltage	0	6	V
T_A	Operating temperature	-40	85	°C
T_{stg}	Storage temperature	-85	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±15000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500
		IEC 61000-4-2 Contact Discharge	±11000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		-40		85	°C
Operating voltage	V_{CC}	0		5.5	V
	Ch1_In	0		V_{CC}	
	Ch2_In	0		V_{CC}	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD2S017	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	44.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Series resistor		1		Ω
I_{IO}	Current from I/O pins	$V_{IO} = 3\text{ V}$	0.01	0.1	μA

over operating free-air temperature range (unless otherwise noted)

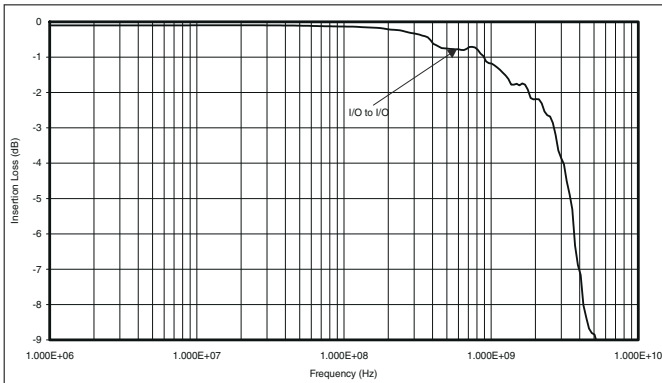
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔRS	Channel-to-channel resistance match	$V_{IO} = 3\text{ V}$		± 8	± 15	m Ω
V_D	Diode forward voltage for lower clamp	$I_D = 8\text{ mA}$	-0.6	-0.8	-0.95	V
R_{DYN}	Dynamic resistance (for I/O clamp)	$I = 9\text{ A}$		0.8		Ω
C_{IO}	IO capacitance	$V_{IO} = 2.5\text{ V}; f = 10\text{ MHz}$		1		pF
V_{BR}	Break-down voltage	$I_O = 1\text{ mA}$	11	12		V

6.6 Dissipation Ratings

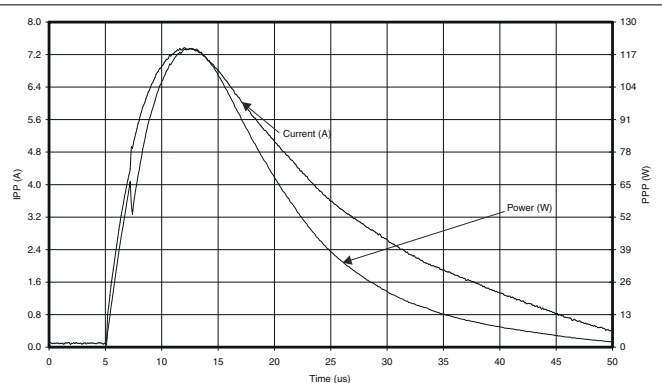
PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A \leq 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DBV	463.18 mW	-4.63 mW/C	254.75 mW

(1) Derating factor is defined as the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).

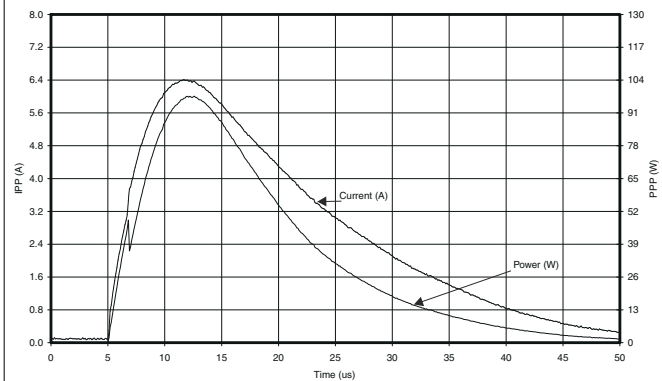
6.7 Typical Characteristics



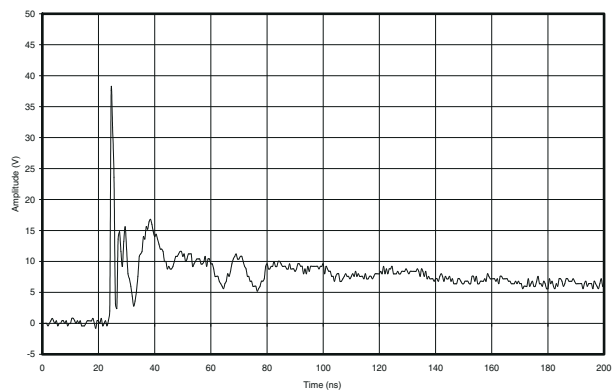
6-1. Insertion Loss Data (S21)



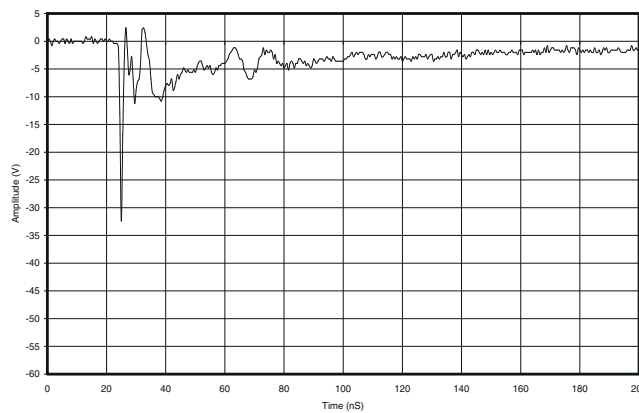
6-2. Peak Pulse Waveforms Ch1_Out, PUT with respect to GND, $V_{CC} = 5\text{ V}$



6-3. Peak Pulse Waveforms Ch2_In, PUT with respect to GND, $V_{CC} = 5\text{ V}$



6-4. IEC Clamping Waveforms 8 kV Contact, 1 GHz Bandwidth



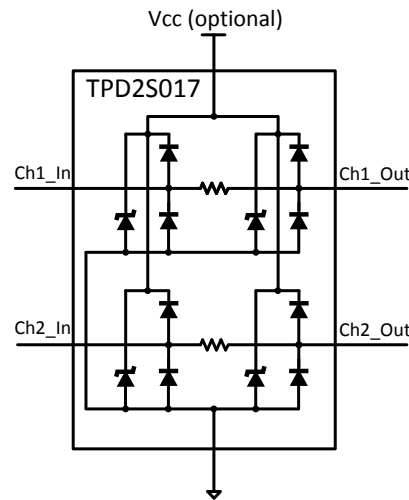
6-5. IEC Clamping Waveforms -8 kV Contact, 1 GHz Bandwidth

7 Detailed Description

7.1 Overview

The TPD2S017 is a two-channel ESD protection device. The two-stage ESD diodes and 1-Ω isolation resistor topology of the device gives the system very robust and good protection during ESD strikes. The TPD2S017 conforms to the IEC61000-4-2 ESD protection standard. The TPD2S017 provides a –3 dB frequency at almost 3 GHz which provides enough bandwidth for a vast majority of applications. Thanks to the monolithic silicon technology, the tight matching of the line capacitances and series resistances ensures a minimum distorted differential signal and a high operating differential data rate. The DBV package offers a flow-through pin mapping for ease of board layout.

7.2 Functional Block Diagram



7.3 Feature Description

Each channel of the TPD2S017 device has a topology of two-stage clamps with isolation resistor. This topology optimizes the clamping performance while supporting a high bandwidth. Due to the low clamping voltage, the down stream circuits that connect to the output of the channels are well-protected. The high IEC 61000-4-2 level ensures the system's robustness during the ESD events. The good matching of the resistor and capacitance values will yield minimal distortion of the signals. The low resistance and capacitance values make sure that this device supports a high differential data rate. The flow-through pinout ensures no additional layout burden on the printed circuit board (PCB).

7.4 Device Functional Modes

The TPD2S017 device stays passive and has low leakage during normal operation when the voltage at the input of each channel is from 0 V to V_{CC} and activates when that voltage exceeds one forward diode drop above V_{CC} or below ground. During IEC ESD events, contact transient voltages as high as ± 11 kV can be suppressed. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

When a system contains a human interface connector, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. Protection products are typically used to suppress ESD at these connectors. TPD2S017 is a two-channel ESD protection device. In each channel, it contains two-stage TVS diodes and a resistor between the two clamping stages as an isolation. This implementation provides good clamping performance, minimal signal distortion and the support of high data speed.

8.2 Typical Application

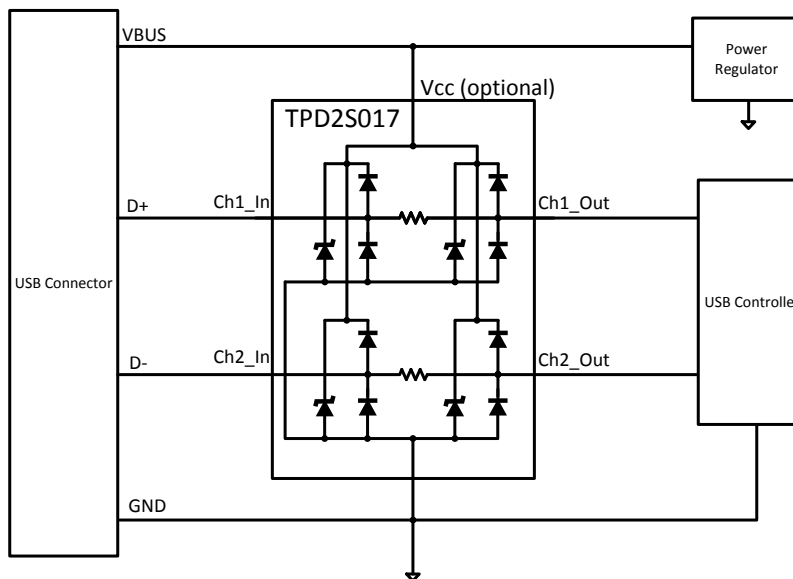


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, a TPD2S017 will be used to protect the USB 2.0 high-speed data lines. The following system parameters are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
High-speed mode high-level output voltage	400 mV ±10%
High-speed mode low-level output voltage	0 V ± 10 mV
USB 2.0 high-speed data rate	480 Mbps
Required IEC 61000-4-2 ESD Protection	±8 kV Contact

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected lines must not go beyond one forward diode drop above the V_{CC} and must not go below one forward diode drop below the ground.
- Operating frequency is supported by the IO capacitance C_{IO} .
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, a high speed USB 2.0 signal that ranges from -10 mV to 440 mV will be applied to each line. Connect a 5 V power supply to V_{CC} pin; therefore, the signal will not fall outside of the normal operation range and the TPD2S017 will stay passive and low leakage during normal operation.

Next, consider the data rate of this signal and ensure that the TVS I/O capacitance will not distort this signal by filtering it. The speed of a USB 2.0 high-speed signal is 480 Mbit/s. With TPD2S017's ultra low IO capacitance, this device can support 1.5 Gbit/s data rate and thus can pass USB 2.0 high-speed signal with minimal distortion.

Finally, TPD2S017 is rated for the IEC 61000-4-2 (Level 4) so it provides sufficient system-level ESD protection to the human interface in this application. See [セクション 10.2](#) for instructions on properly laying out TPD2S017.

8.2.3 Application Curves

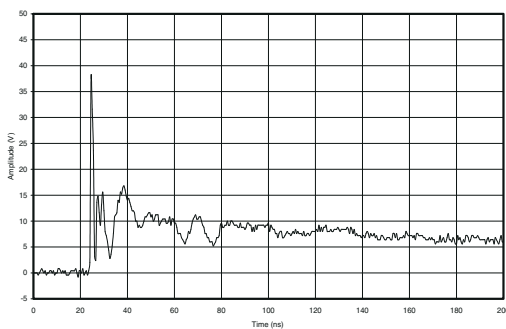


図 8-2. IEC Clamping Waveforms 8 kV Contact, 1 GHz Bandwidth

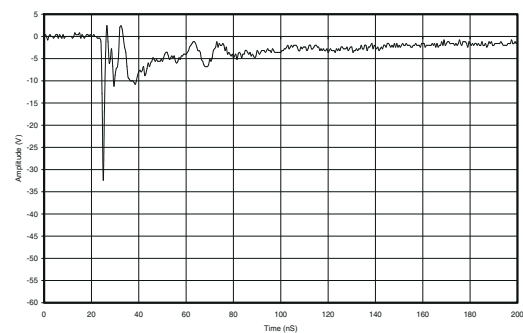


図 8-3. IEC Clamping Waveforms -8 kV Contact, 1 GHz Bandwidth

9 Power Supply Recommendations

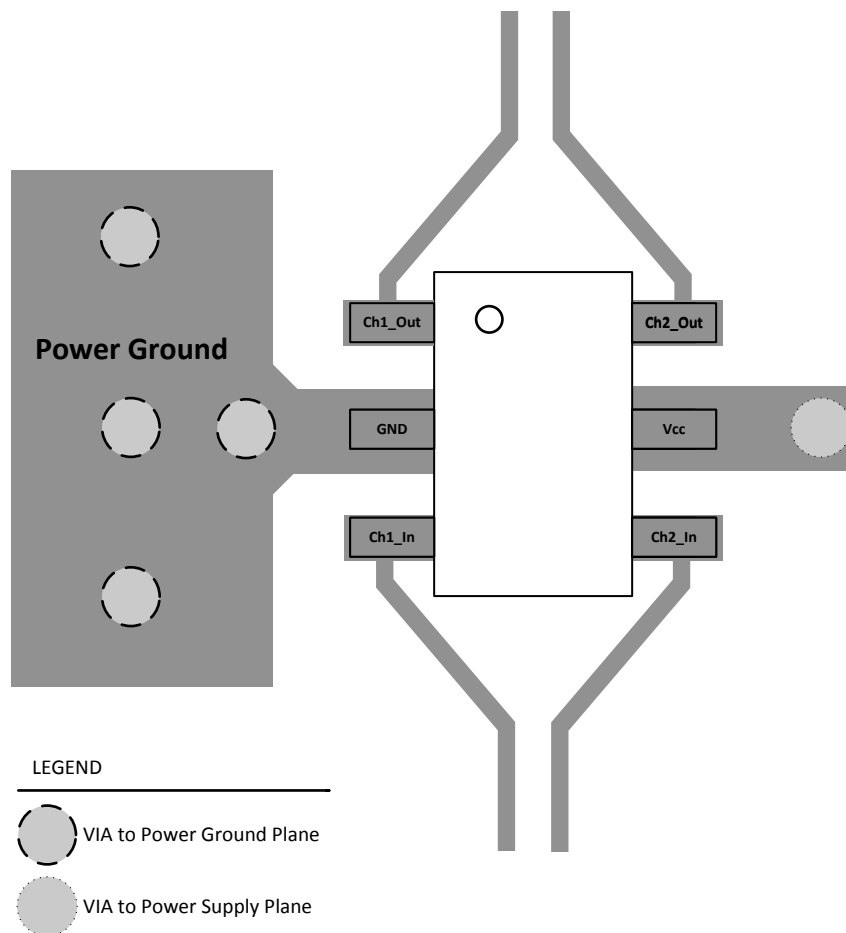
The optional V_{CC} power supply bias is recommended to lower the I/O capacitances. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- Use thick and short traces for the power and ground paths.
- Run differential signal lines in pair with small distance to optimize signal integrity.

10.2 Layout Example



☒ 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

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11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.4 静電気放電に関する注意事項



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11.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2S017DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	NFT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S017DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S017DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

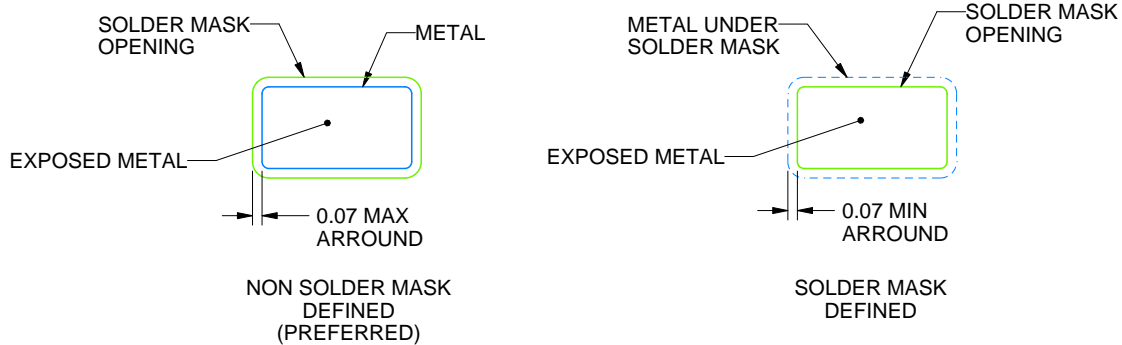
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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