

# TPD2S701-Q1 車載用USB 2チャンネル・データ・ラインのV<sub>BUS</sub>への短絡およびIEC ESD保護

## 1 特長

- AEC-Q100認定済み
  - 動作温度範囲: -40°C ~ 125°C
- VD+およびVD-でのVBUSへの短絡保護
- VD+, VD-のESD性能
  - 接触放電±8kV (IEC 61000-4-2およびISO 10605 330pF, 330Ω)
  - エアギャップ放電±15kV (IEC 61000-4-2およびISO 10605 330pF, 330Ω)
- 高速データ・スイッチ(1GHz帯域幅)
- 5V電源のみで動作
- OVPスレッシュホールドを変更可能
- 短い過電圧応答時間(標準値200ns)
- サーマル・シャットダウン機能
- 入力イネーブルおよびフォルト出力信号を内蔵
- フロースルー配線によるデータ整合性
  - 10ピンのVSSOPパッケージ(3mm×3mm)
  - 10ピンのQFNパッケージ(2.5mm×2.5mm)

## 2 アプリケーション

- 最終製品
  - ヘッド・ユニット
  - リアシート用エンターテインメント
  - テレマティクス
  - USBハブ
  - ナビゲーション・モジュール
  - メディア・インターフェイス
- インターフェイス
  - USB 2.0
  - USB 3.0

## 3 概要

TPD2S701-Q1は、USB 2.0などの車載用高速インターフェイス向けに開発された、2チャンネル・データ・ラインのV<sub>BUS</sub>への短絡保護、およびIEC61000-4-2 ESD保護デバイスです。TPD2S701-Q1には2つのデータ・ラインnFETスイッチが内蔵されており、クラス最高の帯域幅により信号の劣化を最小限に抑えて安全なデータ通信を保証しながら、同時にVD+およびVD-ピンの過電圧状況からも内部のシステム回路を保護します。

デバイスはこれらのピンで、最高7V DCまでの過電圧保護に対応できます。これによって、データ・ラインがUSBのV<sub>BUS</sub>レールへ短絡した場合に、十分な保護が得られます。過電圧保護回路は、業界で最も信頼性の高いV<sub>BUS</sub>への短絡の絶縁を行い、200nsでデータ・スイッチをシャットオフして、危険な電圧や電流スパイクから上流の回路を保護します。

さらに、TPD2S701-Q1は5Vの単一電源のみで動作するため、電源ツリーのサイズとコストを最適化できます。OVPスレッシュホールドおよびクランプ回路は抵抗分圧回路により設定できるため、あらゆるトランシーバについて、単純かつコスト効果の高い方法でシステム保護を最適化できます。また、TPD2S701-Q1にはFLTピンが搭載され、デバイスが過電圧状況を検出したことを通知します。過電圧状況が解消されると、このピンは自動的にリセットされます。

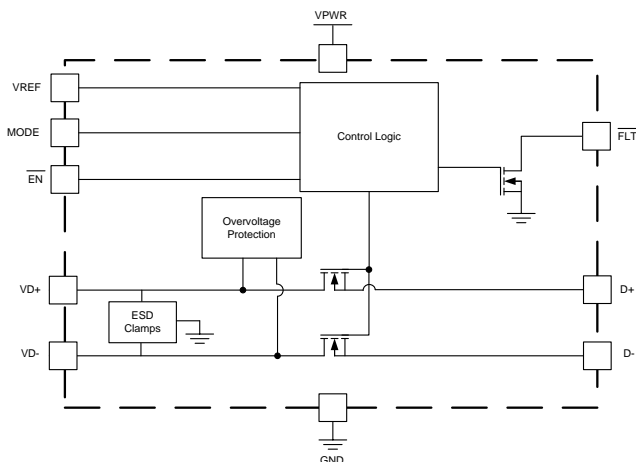
さらに、TPD2S701-Q1ではシステム・レベルのIEC 61000-4-2およびISO 10605 ESDクランプがVD+およびVD-ピンに統合されているため、アプリケーションで外付けの高電圧、低容量TVSクランプ回路を使用する必要がありません。

### 製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPD2S701-Q1	VSSOP (10)	3.00mm×3.00mm
	QFN (10)	2.50mm×2.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 機能ブロック図



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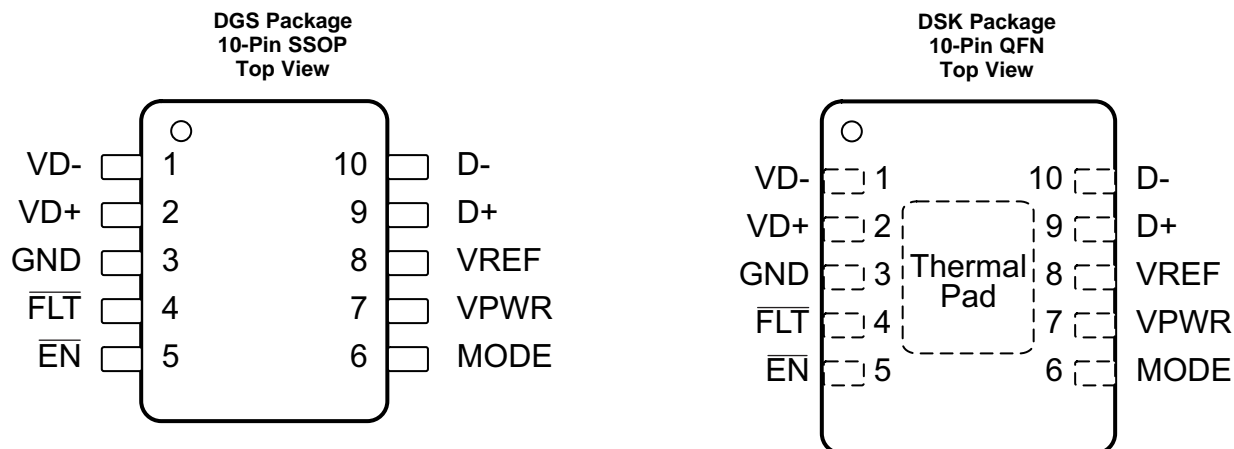
## 4 改訂履歴

2017年4月発行のものから更新

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## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VD-	I/O	High voltage D- USB data line, connect to USB connector D+, D- IEC61000-4-2 ESD protection
2	VD+	I/O	High voltage D+ USB data line, connect to USB connector D+, D- IEC61000-4-2 ESD protection
3	GND	Ground	Ground pin for internal circuits and IEC ESD clamps
4	$\overline{\text{FLT}}$	O	Open-drain fault pin. See <a href="#">表 1</a>
5	$\overline{\text{EN}}$	I	Enable active-low input. Drive $\overline{\text{EN}}$ low to enable the switches. Drive $\overline{\text{EN}}$ high to disable the switches. See <a href="#">表 1</a> for mode selection
6	MODE	I	Selects between device modes. See the <a href="#">Detailed Description</a> section. Acts as LDO reference voltage for mode 1
7	VPWR	I	5-V DC supply input for internal circuits. Connect to internal power rail on PCB
8	VREF	I/O	Pin to set OVP threshold. See the <a href="#">Detailed Description</a> section for instructions on how to set OVP threshold
9	D+	I/O	I/O protected low voltage D+ USB data line, connects to transceiver
10	D-	I/O	Protected low voltage D- USB data line, connects to transceiver

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>PWR</sub>	5-V DC supply voltage for internal circuitry	-0.3	7.7	V
V <sub>REF</sub>	Pin to set OVP threshold	-0.3	6	V
VD+, VD-	Voltage range from connector-side USB data lines	-0.3	7.7	V
D+, D-	Voltage range for internal USB data lines	-0.3	V <sub>REF</sub> + 0.3	V
V <sub>MODE</sub>	Voltage on MODE pin	-0.3	7.7	V
V <sub>FLT</sub>	Voltage on FLT pin	-0.3	7.7	V
V <sub>EN</sub>	Voltage on enable pin	-0.3	7.7	V
T <sub>A</sub>	Operating free air temperature <sup>(3)</sup>	-40	125	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(3) Thermal limits and power dissipation limits must be observed.

### 6.2 ESD Ratings—AEC Specification

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins besides corners		±500
			Corner pins		±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000	V
		IEC 61000-4-2 air-gap discharge	±15000	

(1) See [19](#) for details on system level ESD testing setup.

### 6.4 ESD Ratings—ISO Specification

			VALUE	UNIT
V <sub>ESD</sub> <sup>(1)</sup>	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω) contact discharge (10 strikes)	±8000	V
		ISO 10605 (330 pF, 330 Ω) air-gap discharge (10 strikes)	±15000	
		ISO 10605 (150 pF, 330 Ω) contact discharge (10 strikes)	±8000	
		ISO 10605 (150 pF, 330 Ω) air-gap discharge (10 strikes)	±15000	
		ISO 10605 (330 pF, 2 kΩ) contact discharge (10 strikes) <sup>(2)</sup>	±8000	
		ISO 10605 (330 pF, 2 kΩ) air-gap discharge (10 strikes)	±15000	
		ISO 10605 (150 pF, 2 kΩ) air-gap discharge (10 discharges)	±25000	

(1) See [19](#) for details on system level ESD testing setup.

(2) V<sub>REF</sub> > 3 V.

## 6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V <sub>PWR</sub>	5-V DC supply voltage for internal circuitry	4.5		7	V
V <sub>REF</sub>	Mode 0. Voltage range for V <sub>REF</sub> pin (for setting OVP threshold)	3		3.6	V
V <sub>REF</sub>	Mode 1. Voltage range for V <sub>REF</sub> pin (for setting OVP threshold)	0.63		3.8	V
VD+, VD–	Voltage range from connector-side USB data lines	0		3.6	V
D+, D–	Voltage range for internal USB data lines	0		3.6	V
V <sub>EN</sub>	Voltage range for enable	0		7	V
V <sub>FLT</sub>	Voltage range for $\overline{\text{FLT}}$	0		7	V
I <sub>FLT</sub>	Current into open drain $\overline{\text{FLT}}$ pin FET	0		3	mA
C <sub>VPWR</sub>	V <sub>PWR</sub> capacitance <sup>(1)</sup>   External Capacitor on V <sub>PWR</sub> pin	1	10		μF
C <sub>VREF</sub>	V <sub>REF</sub> capacitance   External Capacitor on V <sub>REF</sub> pin	0.3	1	3	μF
C <sub>MODE</sub>	Allowed parasitic capacitance on mode pin from PCB and mode 1 external resistors			20	pF
R <sub>MODE_0</sub>	Resistance to GND to set to mode 0		2	2.6	kΩ
R <sub>MODE_1</sub>	Resistance to GND to set to mode 1 (calculate parallel combination of R <sub>TOP</sub> and R <sub>BOT</sub> )	14	20		kΩ

- (1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented should be within the minimum and maximums listed in the table.

## 6.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD2S701-Q1		UNIT
		DGS (VSSOP)	DSK (WSON)	
		10 PINS	10 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	167.3	61.5	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	56.9	51.3	°C/W
θ <sub>JB</sub>	Junction-to-board thermal resistance	87.6	34	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.7	1.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	86.2	34.3	°C/W
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	N/A	7.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>MODE 1 ADJUSTABLE V<sub>REF</sub></b>							
V <sub>MODE_CMP</sub>	Mode 1 V <sub>REF</sub> feedback regulator voltage	V <sub>MODE</sub>	Standard mode 1 set-up. $\overline{EN} = 0$ V. Once V <sub>REF</sub> = 3.3 V, measure voltage on mode pin	0.47	0.5	0.53	V
I <sub>MODE_LEAK</sub>	Mode pin mode 1 leakage current	I <sub>MODE</sub>	Standard mode 1. Remove R <sub>TOP</sub> and R <sub>BOT</sub> . Power up device and wait until start-up time has passed. Then force 0.53 V on the MODE pin and measure current into pin		50	200	nA
V <sub>REF_ACCURACY</sub>	V <sub>REF</sub> accuracy	V <sub>REF</sub>	Informative, test parameters below; accuracy with R <sub>TOP</sub> and R <sub>BOT</sub> as ±1% resistors	–8%		8%	
V <sub>REF_3.3V</sub>	Mode 1 V <sub>REF</sub> set to 3.3 V	V <sub>REF</sub>	Standard mode 1 set-up. R <sub>TOP</sub> = 140 kΩ ± 1%, R <sub>BOT</sub> = 24.9 kΩ ± 1%. $\overline{EN} = 0$ . Measure value of V <sub>REF</sub> once it settles	3.04	3.31	3.58	V
V <sub>REF_0.66V</sub>	Mode 1 V <sub>REF</sub> set to 0.66 V	V <sub>REF</sub>	Standard mode 1 set-up. R <sub>TOP</sub> = 47.5 kΩ ± 1%, R <sub>BOT</sub> = 150 kΩ ± 1%. $\overline{EN} = 0$ . Measure value of V <sub>REF</sub> once it settles	0.6	0.66	0.72	V
V <sub>REF_3.8V</sub>	Mode 1 V <sub>REF</sub> set to 3.8 V	V <sub>REF</sub>	Standard mode 1 set-up. R <sub>TOP</sub> = 165 kΩ ± 1%, R <sub>BOT</sub> = 24.9 kΩ ± 1%. $\overline{EN} = 0$ . Measure value of V <sub>REF</sub> once it settles	3.5	3.81	4.12	V
<b>EN, FLT PINS</b>							
V <sub>IH</sub>	High-level input voltage	$\overline{EN}$	Mode 0. Connect VPWR = 5 V; V <sub>REF</sub> = 3.3 V; VD+ = 3.3 V; Set VIH( $\overline{EN}$ ) = 0 V; Sweep VIH from 0 V to 1.4 V; Measure when D+ drops low (less than or equal to 5% of 3.3 V) from 3.3 V	1.2			V
	Low-level input voltage		Mode 0. Connect VPWR = 5 V; V <sub>REF</sub> = 3.3 V; VD+ = 3.3 V. Set VIH( $\overline{EN}$ ) = 3.3 V; Sweep VIH from 3.3 V to 0.5 V; Measure when D+ rise to 95% of 3.3 V from 0 V	0.8			
I <sub>IL</sub>	Input leakage current	$\overline{EN}$	Mode 0. VPWR = 5 V; V <sub>REF</sub> = 3.3 V; VI (EN) = 3.3 V; Measure current into EN pin			1	μA
V <sub>OL</sub>	Low-level output voltage	$\overline{FLT}$	Mode 0. Drive the TPS2S701-Q1 in OVP to assert FLT pin. Source I <sub>OL</sub> = 1 mA into FLT pin and measure voltage on FLT pin when asserted			0.4	V
T <sub>SD_RISING</sub>	The rising over temperature protection shutdown threshold		VPWR = 5 V, ENZ = 0 V, T <sub>A</sub> stepped up until FLTZ is asserted	140	150	165	°C
T <sub>SD_FALLING</sub>	The falling over temperature protection shutdown threshold		VPWR = 5 V, ENZ = 0 V, T <sub>A</sub> stepped down from T <sub>SD_RISING</sub> until FLTZ is cleared	125	138	150	°C
T <sub>SD_HYST</sub>	The over temperature protection shutdown threshold hysteresis		T <sub>SD_RISING</sub> – T <sub>SD_FALLING</sub>	10	12	15	°C
<b>OVP CIRCUIT—VD±</b>							
V <sub>OVP_RISING</sub>	Input overvoltage protection threshold, V <sub>REF</sub> > 3.6 V	VD±	Mode 1. Set V <sub>PWR</sub> = 5 V; $\overline{EN} = 0$ V; R <sub>TOP</sub> = 165 kΩ, R <sub>BOT</sub> = 24.9 kΩ. Connect D± to 40-Ω load. Increase VD+ or VD– from 4.1 V to 4.9 V. Measure the value at which FLTZ is asserted	4.3	4.5	4.7	V
V <sub>OVP_RISING</sub>	Input overvoltage protection threshold	VD±	Mode 1. Set V <sub>PWR</sub> = 5 V; $\overline{EN} = 0$ V; R <sub>TOP</sub> = 140 kΩ, R <sub>BOT</sub> = 24.9 kΩ. Increase VD+ or VD– from 3.6 V to 4.6 V. Measure the value at which FLTZ is asserted. Repeat for R <sub>TOP</sub> = 39 kΩ, R <sub>BOT</sub> = 150 kΩ. Increase VD+ or VD– from 0.6 V to 0.9 V. Measure the value at which FLTZ is asserted. See the resultant values meet the equation, and make sure to observe data switches turnoff. Also check for mode 0 when V <sub>REF</sub> = 3.3 V	1.19 × V <sub>REF</sub>	1.25 × V <sub>REF</sub>	1.31 × V <sub>REF</sub>	V
V <sub>HYS_OVP</sub>	Hysteresis on OVP	VD±	Difference between rising and falling OVP thresholds on VD±		25		mV
V <sub>OVP_FALLING</sub>	Input overvoltage protection threshold	VD±	After collecting each rising OVP threshold, lower the VD± voltage until you see $\overline{FLT}$ deassert. This gives the falling OVP threshold. Use this value to calculate V <sub>HYS_OVP</sub>		VOV P_RI SING – VHYS _OVP		V
I <sub>VD_LEAK_0 V</sub>	Leakage current on VD± during normal operation	VD±	Standard mode 0 or mode 1. Set VD± = 0 V. D± = floating. Measure current flowing into VD±	–0.1		0.1	μA

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{VD\_LEAK\_3.6V}$	Leakage current on $VD_{\pm}$ during normal operation	$VD_{\pm}$	Standard mode 0 or mode 1. Set $VD_{\pm} = 3.6\text{ V}$ . $D_{\pm} =$ floating. Measure current flowing into $VD_{\pm}$		2.5	4	$\mu\text{A}$
$V_{OVP\_3.3V}$	Input overvoltage threshold for $V_{REF} = 3.3\text{ V}$	$VD_{\pm}$	Standard mode 1. $R_{TOP} = 140\text{ k}\Omega \pm 1\%$ , $R_{BOT} = 24.9\text{ k}\Omega \pm 1\%$ . Connect $D_{\pm}$ to $40\text{-}\Omega$ load. Measure the value at which FLTZ is asserted	3.61	4.14	4.67	V
$V_{OVP\_0.66V}$	Input overvoltage threshold for $V_{REF} = 0.66\text{ V}$	$VD_{\pm}$	Standard mode 1. $R_{TOP} = 47.5\text{ k}\Omega \pm 1\%$ , $R_{BOT} = 150\text{ k}\Omega \pm 1\%$ . Connect $D_{\pm}$ to $40\text{-}\Omega$ load. Measure the value at which FLTZ is asserted	0.72	0.83	0.94	V
<b>DATA LINE SWITCHES – <math>VD+</math> to <math>D+</math> or <math>VD-</math> to <math>D-</math></b>							
$R_{ON}$	On resistance		Mode 0 or 1. Set $V_{PWR} = 5\text{ V}$ ; $V_{REF} = 3.3\text{ V}$ ; $\overline{EN} = 0\text{ V}$ ; Measure resistance between $D+$ and $VD+$ or $D-$ and $VD-$ , voltage between 0 and 0.4 V		4	6.5	$\Omega$
$R_{ON(Flat)}$	On resistance flatness		Mode 0 or 1. Set $V_{PWR} = 5\text{ V}$ ; $V_{REF} = 3.3\text{ V}$ ; $\overline{EN} = 0\text{ V}$ ; Measure resistance between $D+$ and $VD+$ or $D-$ and $VD-$ , sweep voltage between 0 and 0.4 V. Take difference of resistance at 0.4-V and 0-V $VD_{\pm}$ bias			1	$\Omega$
$BW_{ON}$	On bandwidth (–3-dB)		Mode 0 or 1. Set $V_{PWR} = 5\text{ V}$ ; $V_{REF} = 3.3\text{ V}$ ; $\overline{EN} = 0\text{ V}$ ; Measure S21 bandwidth from $D+$ to $VD+$ or $D-$ to $VD-$ with voltage swing = 400 mVpp, $V_{cm} = 0.2\text{ V}$		960		MHz

## 6.8 Power Supply and Supply Current Consumption Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{UVLO\_RISING\_VPWR}$	$V_{PWR}$ rising UVLO threshold		Use standard mode 0 set-up. Set $\overline{EN} = 0\text{ V}$ , load $D+$ to $45\text{ }\Omega$ , $VD+ = 3.3\text{ V}$ . Set $V_{PWR} = 3.5\text{ V}$ , and step up $V_{PWR}$ until 90% of $VD+$ appears on $D+$	3.7	3.95	4.2	V
$V_{UVLO\_HYST\_VPWR}$	$VPWR$ UVLO hysteresis		Use standard mode 0 set up. Set $\overline{EN} = 0\text{ V}$ , load $D+$ to $45\text{ }\Omega$ , $VD+ = 3.3\text{ V}$ . Set $V_{PWR} = 4.3\text{ V}$ , and step down $V_{PWR}$ until $D+$ falls to 10% of $VD+$ . This gives $V_{UVLO\_FALLING\_VPWR} \cdot V_{UVLO\_RISING\_VPWR} - V_{UVLO\_FALLING\_VPWR} = V_{UVLO\_HYST\_VPWR}$ for this unit	250	300	400	mV
$V_{UVLO\_RISING\_VREF}$	$V_{REF}$ rising UVLO threshold in mode 0		Use standard mode 0 set up. Set $\overline{EN} = 0\text{ V}$ , load $D+$ to $45\text{ }\Omega$ , $VD+ = 3.3\text{ V}$ . Set $V_{REF} = 2.5\text{ V}$ , and step up $V_{REF}$ until 90% of $VD+$ appears on $D+$	2.6	2.7	2.9	V
$V_{UVLO\_HYST\_VREF}$	$V_{REF}$ UVLO hysteresis		Use standard mode 0 set up. Set $\overline{EN} = 0\text{ V}$ , load $D+$ to $45\text{ }\Omega$ , $VD+ = 3.3\text{ V}$ . Set $V_{REF} = 3\text{ V}$ , and step down $V_{REF}$ until $D+$ falls to 10% of $VD+$ . This gives $V_{UVLO\_FALLING\_VREF} \cdot V_{UVLO\_RISING\_VREF} - V_{UVLO\_FALLING\_VREF} = V_{UVLO\_HYST\_VREF}$ for this unit	75	125	200	mV
$I_{VPWR\_DISABLE\_D\_MODE0}$	$V_{PWR}$ disabled current consumption		Use standard mode 0. $\overline{EN} = 5\text{ V}$ . Measure current into $V_{PWR}$			110	$\mu\text{A}$
$I_{VPWR\_DISABLE\_D\_MODE1}$	$V_{PWR}$ disabled current consumption		Use standard mode 1. $\overline{EN} = 5\text{ V}$ . Measure current into $V_{PWR}$			110	$\mu\text{A}$
$I_{VREF\_DISABLE\_D}$	$V_{REF}$ disabled current consumption mode 0		Use standard mode 0. $\overline{EN} = 5\text{ V}$ . Measure current into $V_{REF}$			10	$\mu\text{A}$
$I_{VPWR\_MODE0}$	$V_{PWR}$ operating current consumption		Use standard mode 0. $\overline{EN} = 0\text{ V}$ . Measure current into $V_{PWR}$			250	$\mu\text{A}$
$I_{VPWR\_MODE1}$	$V_{PWR}$ operating current consumption		Use standard mode 1. $\overline{EN} = 0\text{ V}$ . Measure current into $V_{PWR}$			350	$\mu\text{A}$
$I_{VREF}$	$V_{REF}$ operating current consumption mode 0		Use standard mode 0. $\overline{EN} = 0\text{ V}$ . Measure current into $V_{REF}$		12	20	$\mu\text{A}$
$I_{CHG\_VREF}$	$V_{REF}$ fast charge current		Standard mode 1. $0.1\text{ }\mu\text{F} < C_{VREF} < 3\text{ }\mu\text{F}$ . Set-up for charging to $3.3\text{ V}$ . Use a high voltage capacitor that does not derate capacitance up the $3.3\text{ V}$ . Measure slope to calculate the current when $C_{VREF}$ cap is being charged. Test to check this OPEN LOOP method		22		mA

### Power Supply and Supply Current Consumption Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{D\_OFF\_LEAK\_S\_TB}$	Mode 0. Measured flowing into D+ or D– supply, $V_{PWR} = 0$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 0$ V, $D_{\pm} = 0$ V	-1		1	$\mu$ A
$I_{D\_ON\_LEAK\_STB}$	Mode 0. Measured flowing into D+ or D– supply, $V_{PWR} = 5$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 3.3$ V, $D_{\pm} = 0$ V	-1		1	$\mu$ A
$I_{VD\_OFF\_LEAK\_STB}$	Mode 0. Measured flowing out of $VD+$ or $VD-$ supply, $V_{PWR} = 0$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 0$ V, $D_{\pm} = 0$ V			120	
$I_{VD\_ON\_LEAK\_STB}$	Mode 0. Measured flowing out of $VD+$ or $VD-$ supply, $V_{PWR} = 5$ V, $VD+$ or $VD- = 18$ V, $\overline{EN} = 0$ V, $V_{REF} = 3.3$ V, $D_{\pm} = 0$ V			120	$\mu$ A
$I_{VPWR\_TO\_VREF\_LEAK}$	Leakage from VPWR to VREF Use standard mode 0. Set $V_{REF} = 0$ V. Measured current flowing out of VREF pin			1	$\mu$ A
$I_{VREF\_TO\_VPWR\_LEAK}$	Leakage from VREF to VPWR Use standard mode 0. Set $VPWR = 0$ V. Measured as current flowing out of VPWR pin			1	$\mu$ A

### 6.9 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
<b>ENABLE PIN AND VREF FAST CHARGE</b>						
$T_{VREF\_CHG}$	VREF fast charge time	Time between when 5 V is applied to $V_{PWR}$ , and $V_{REF}$ reaches $V_{VREF\_FAST\_CHG}$ . Needs to happen before or at same time $t_{ON\_STARTUP}$ completes		0.5	1	ms
$T_{ON\_STARTUP\_P\_MODE0}$	Device turnon time from UVLO mode 0	Mode 0. $\overline{EN} = 0$ V, measured from $V_{PWR}$ and $V_{REF} = UVLO+$ to data FET ON, $V_{PWR}$ comes to $UVLO+$ second. Place 3.3 V on $VD_{\pm}$ . Ramp $V_{REF}$ to 3.3 V, then $VPWR$ to 5 V and measure the time it takes for $D_{\pm}$ to reach 90% of $VD_{\pm}$		0.5	1	ms
$T_{ON\_STARTUP\_P\_MODE1}$	Device turnon time from UVLO mode 1	Informative. mode 1. $\overline{EN} = 0$ V, measured from $V_{PWR} = UVLO+$ to data FET ON		0.5 + $T_{CHG\_C\_VREF}$		ms
$T_{ON\_STARTUP\_P\_MODE1\_3.3V}$	Device turnon time from UVLO mode 1	Mode 1. $\overline{EN} = 0$ V, measured from $V_{PWR} = UVLO+$ to data FET ON, $C_{VREF} = 1 \mu$ F, $V_{REF\_FINAL} = 3.3$ V. Measure the time it takes for $D_{\pm}$ to reach 90% of $VD_{\pm}$		0.6	1	ms
$T_{ON\_EN\_MODE0}$	Device turnon time mode 0	Mode 0. $V_{PWR} = 5$ V, $V_{REF} = 3.3$ V, time from $\overline{EN}$ is asserted until data FET is ON. Place 3.3 V on $VD_{\pm}$ , measure the time it takes for $D_{\pm}$ to reach 90% of $VD_{\pm}$		150		$\mu$ s
$T_{ON\_EN\_MODE1}$	Device turnon time mode 1	Mode 1. $V_{PWR} = 5$ V, $V_{REF\_INITIAL} = 0$ V, time from $\overline{EN}$ is asserted until data FET is ON. Place 3.3 V on $VD_{\pm}$ , measure the time it takes for $D_{\pm}$ to reach 90% of $VD_{\pm}$		150 + $T_{CHG\_V\_REF}$		$\mu$ s
$T_{ON\_EN\_MODE1\_3.3V}$	Device turnon time mode 1 for $V_{REF} = 3.3$ V	Mode 1. $V_{PWR} = 5$ V, $V_{REF\_INITIAL} = 0$ V, time from $\overline{EN}$ is asserted until data FET is ON. Place 3.3 V on $VD_{\pm}$ , measure the time it takes for $D_{\pm}$ to reach 90% of $VD_{\pm}$ . $C_{VREF} = 1 \mu$ F, $V_{REF\_FINAL} = 3.3$ V		300		$\mu$ s
$T_{OFF\_EN}$	Device turnoff time	Mode 0 or 1. $V_{PWR} = 5$ V, $V_{REF} = 3.3$ V, time from $\overline{EN}$ is deasserted until data FET is off. Place 3.3 V on $VD_{\pm}$ , measure the time it takes for $D_{\pm}$ to fall to 10% of $VD_{\pm}$ , $R_{D_{\pm}} = 45 \Omega$		5		$\mu$ s
$T_{CHG\_CVREF}$	Time to charge $C_{VREF}$	Informative. Mode 1. Time from $V_{REF} = 0$ V to $80\% \times V_{REF\_FINAL}$ after $\overline{EN}$ transitions from high to low		$(C_{VREF} \times 0.8 (V_{REF\_FINAL} - V_{REF\_INITIAL}) / (I_{CHG\_VREF}))$		s
$T_{CHG\_CVREF\_3.3V}$	Time to charge $C_{VREF}$ to 3.3 V	Mode 1. Time from $V_{REF} = 0$ V to $90\% \times 3.3$ V after $\overline{EN}$ transitions from high to low, $C_{VREF} = 1 \mu$ F		132		$\mu$ s



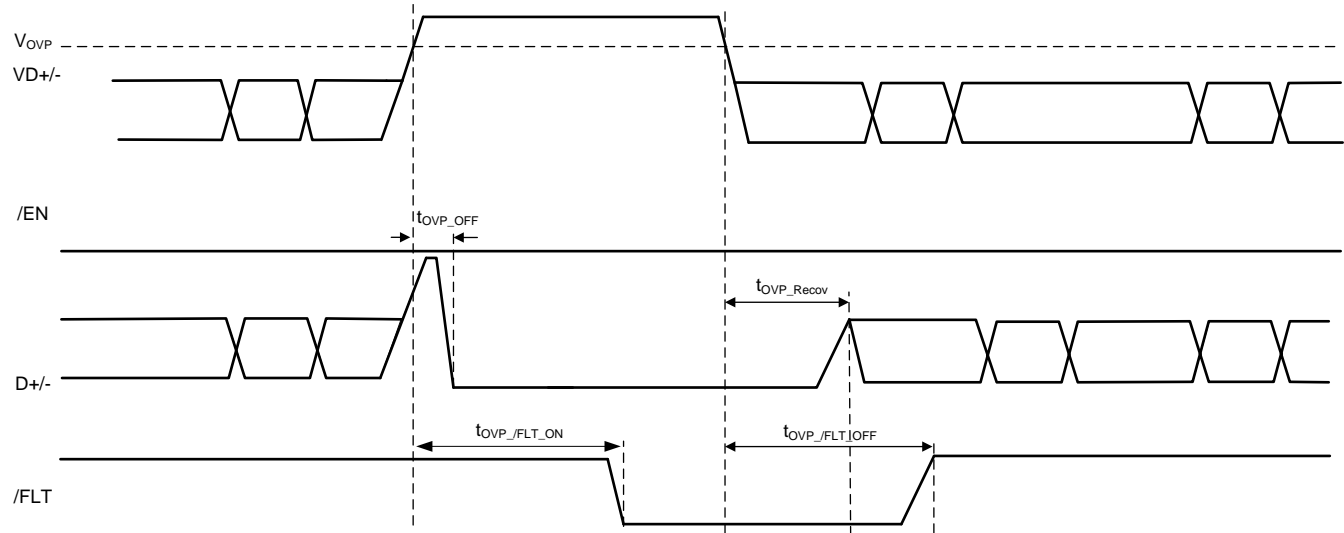
Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{CHG\_CVREF\_0.66V}$	Time to charge $C_{VREF}$ to 0.66 V	Mode 1. Time from $V_{REF} = 0 V$ to $90\% \times 0.63 V$ after $\overline{EN}$ transitions from high to low, $C_{VREF} = 1 \mu F$ . $R_{TOP} = 47.5 k\Omega \pm 1\%$ , $R_{BOT} = 150 k\Omega \pm 1\%$		26		$\mu s$
<b>OVERVOLTAGE PROTECTION</b>						
$t_{OVP\_response\_VBUS}$	OVP response time to VBUS	Mode 0 or 1. Measured from OVP condition to FET turn off . Short $VD_{\pm}$ to 5 V and measure the time it takes $D_{\pm}$ voltage to reach $0.1 \times V_{D_{\pm\_CLAMP\_MAX}}$ from the time the 5-V hot-plug is applied. $R_{LOAD\_D_{\pm}} = 45 \Omega$ . <sup>(1) (2)</sup>		2		$\mu s$
$t_{OVP\_response}$	OVP response time	Mode 0 or 1. Measured from OVP condition to FET turn off . Short $VD_{\pm}$ to 18 V and measure the time it takes $D_{\pm}$ voltage to reach $0.1 \times V_{D_{\pm\_CLAMP\_MAX}}$ from the time the 18-V hot-plug is applied. $R_{LOAD\_D_{\pm}} = 45 \Omega$ . <sup>(1) (2)</sup>		0.1	1	$\mu s$
$t_{OVP\_Recov\_FLT}$	Recovery time $\overline{FLT}$ pin	Measured from OVP clear to $\overline{FLT}$ deassertion <sup>(1)</sup>		32		ms
$t_{OVP\_Recov\_FET}$	Recovery time for data FET to turn back on	Measured from OVP clear until FET turns back on. Drop $VD+$ from 16 V to 3.3 V with $V_{REF} = 3.3 V$ , measure time it takes for $D+$ to reach 90% of 3.3 V		32		ms
$t_{OVP\_ASSERT}$	$\overline{FLT}$ assertion time	Measured from OVP on $VD+$ or $VD-$ to $\overline{FLT}$ assertion	12.6	18	23.4	ms

(1) Shown in [Figure 1](#).

(2) Specified by design, not production tested.



(1) OVP Operation –  $VD+$ ,  $VD-$

Figure 1. TPD2S701-Q1 Timing Diagram

**6.10 Typical Characteristics**

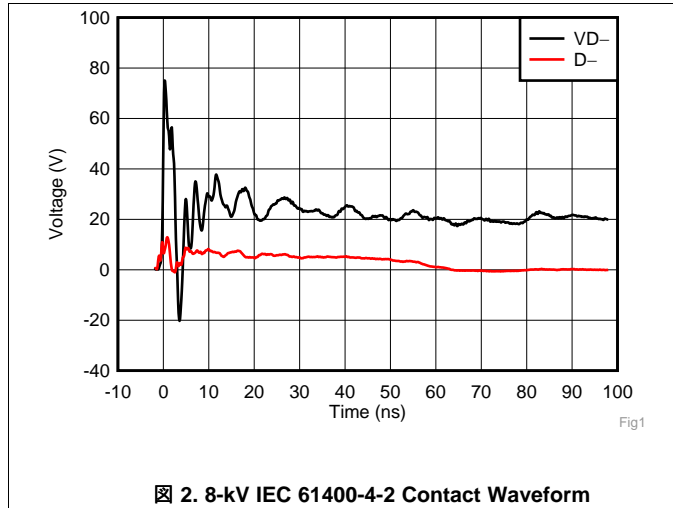


图 2. 8-kV IEC 61400-4-2 Contact Waveform

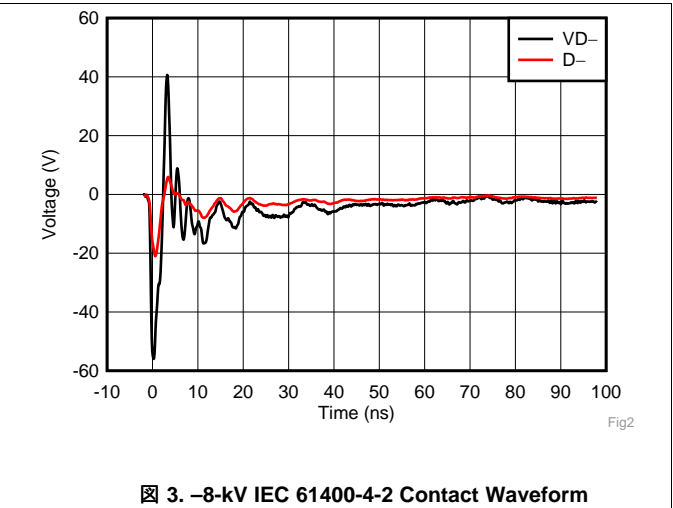


图 3. -8-kV IEC 61400-4-2 Contact Waveform

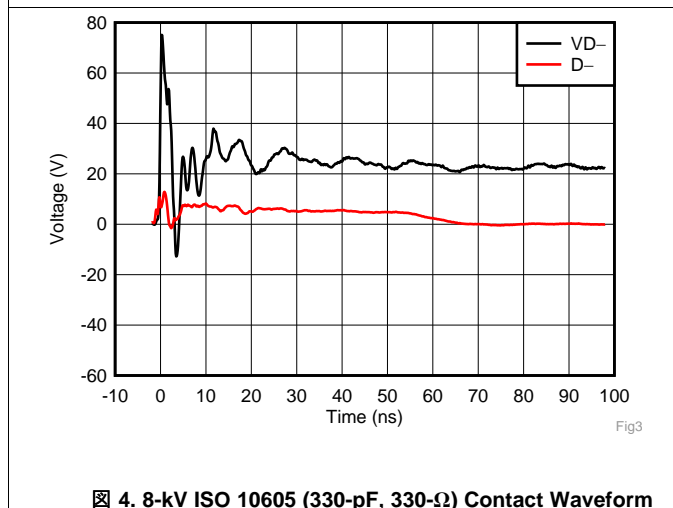


图 4. 8-kV ISO 10605 (330-pF, 330-Ω) Contact Waveform

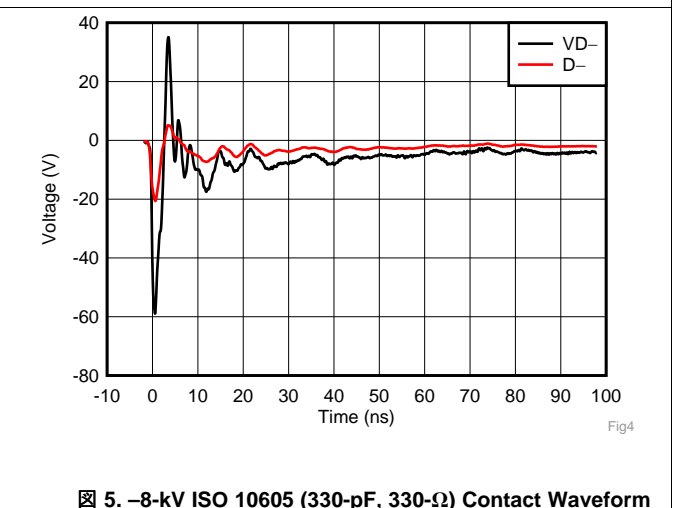


图 5. -8-kV ISO 10605 (330-pF, 330-Ω) Contact Waveform

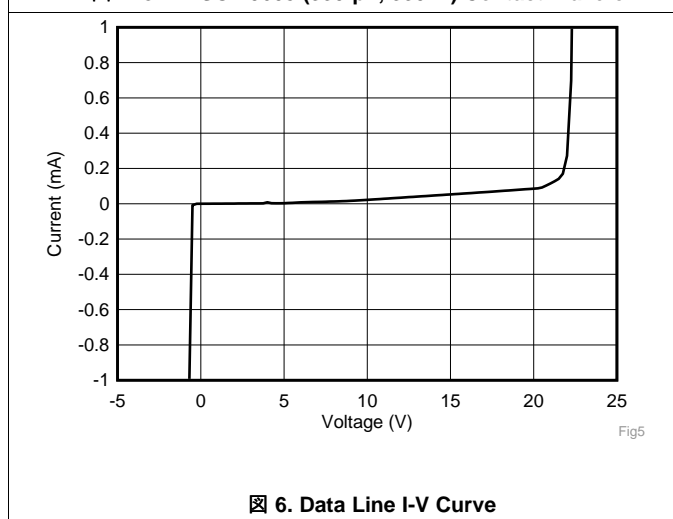


图 6. Data Line I-V Curve

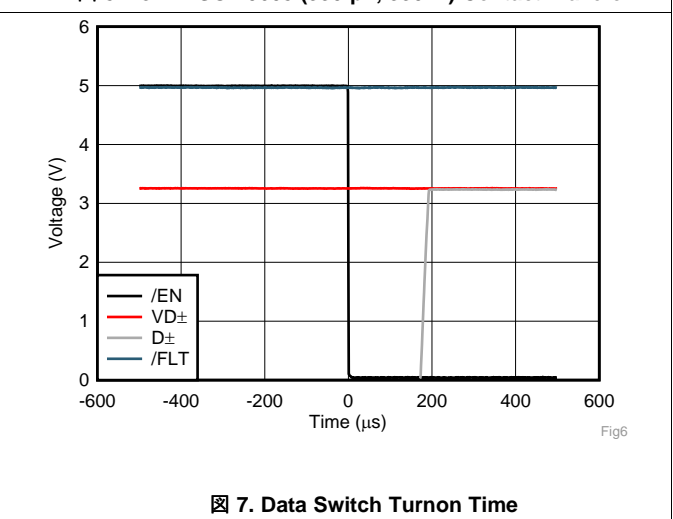


图 7. Data Switch Turnon Time

Typical Characteristics (continued)

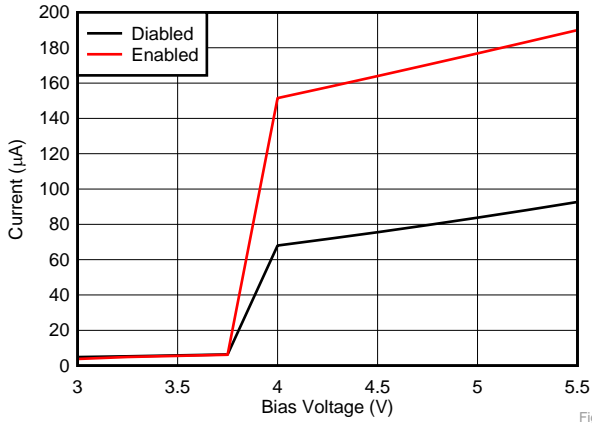


Fig7

Fig 8.  $V_{PWR}$  Operating Current vs Bias Voltage

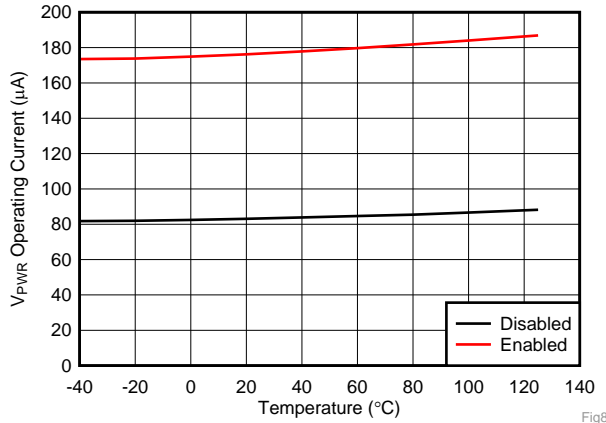
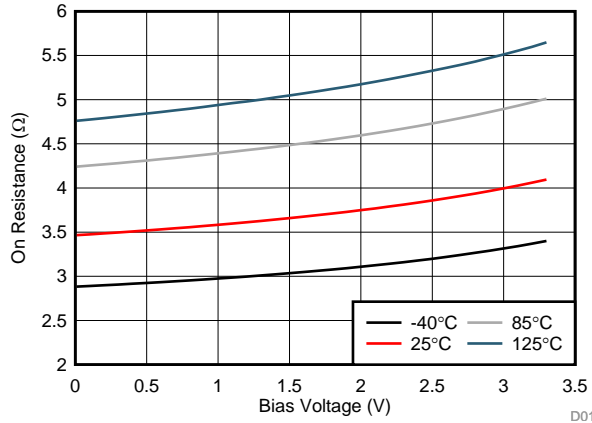


Fig8

Fig 9.  $V_{PWR}$  Operating Current vs Temperature ( $V_{PWR} = 5\text{ V}$ )



D010

Fig 10.  $VD_{\pm}$  Leakage Current at 7 V Across Temperature (Enabled)

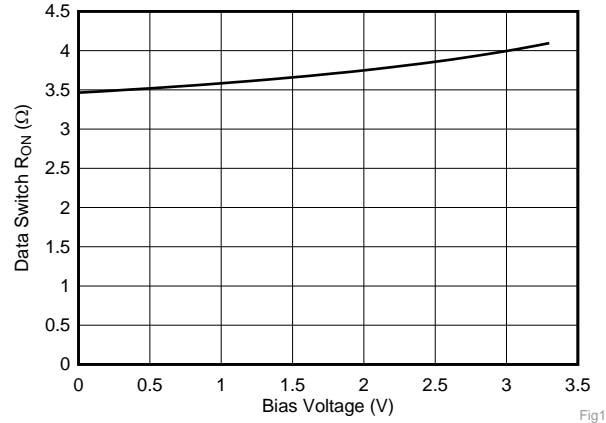
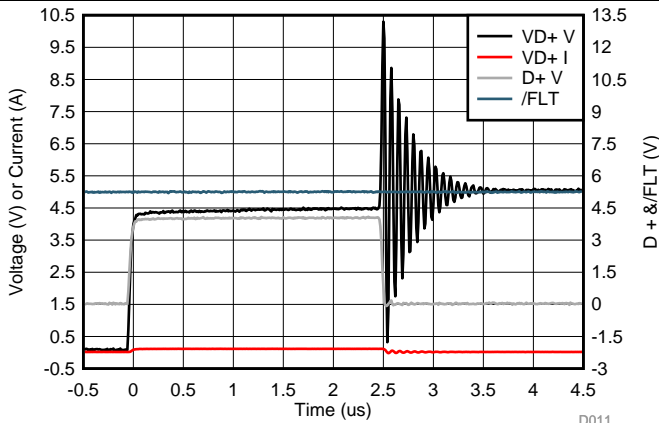


Fig1

Fig 11. Data Switch  $R_{ON}$  vs Bias Voltage



D011

Fig 12. Data Switch Short-to-5 V Response Waveform

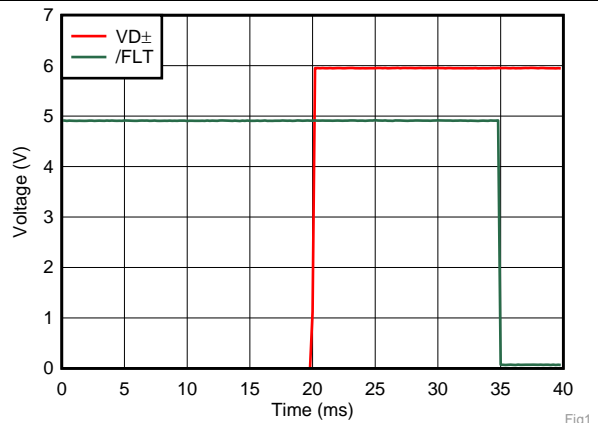
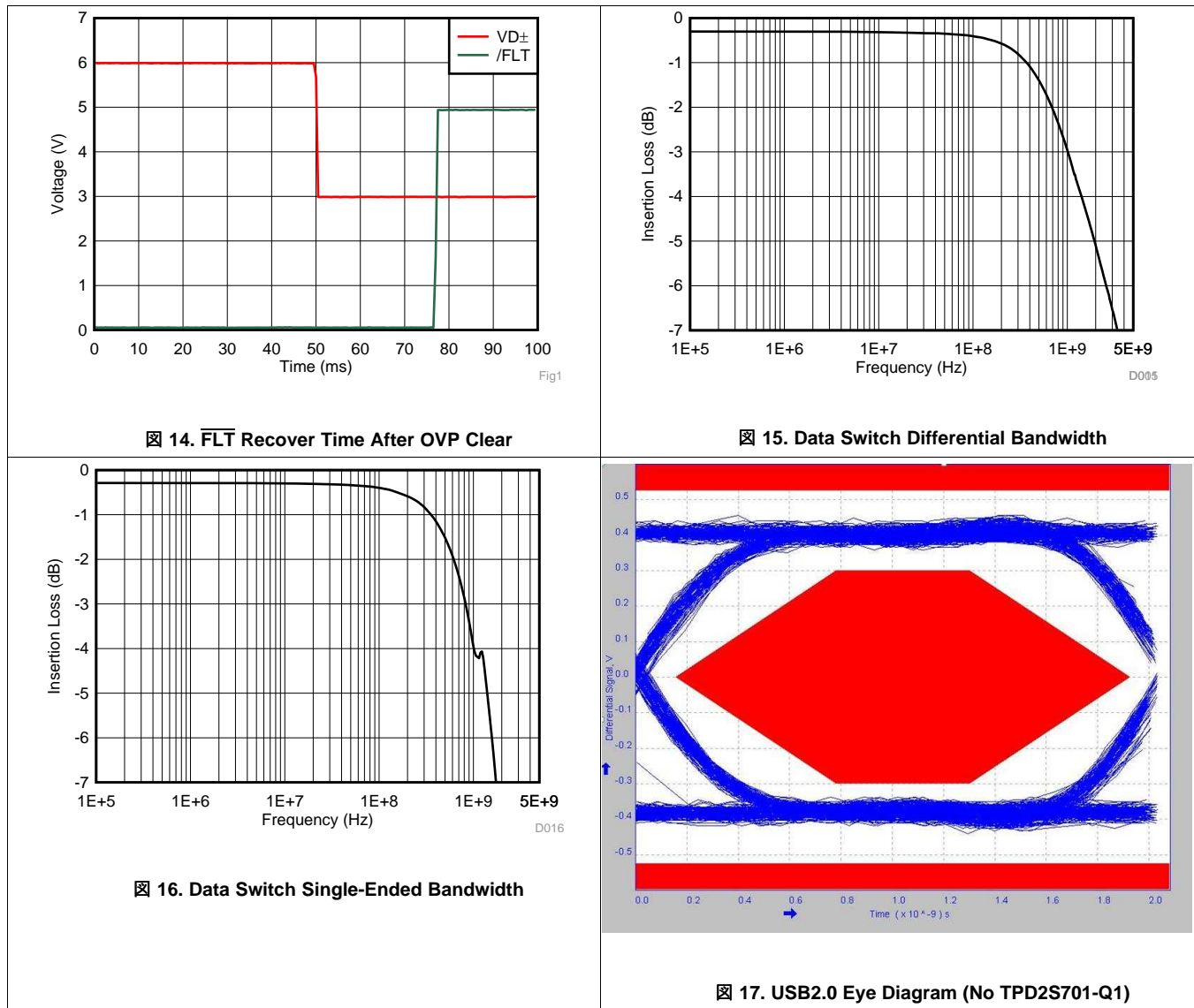


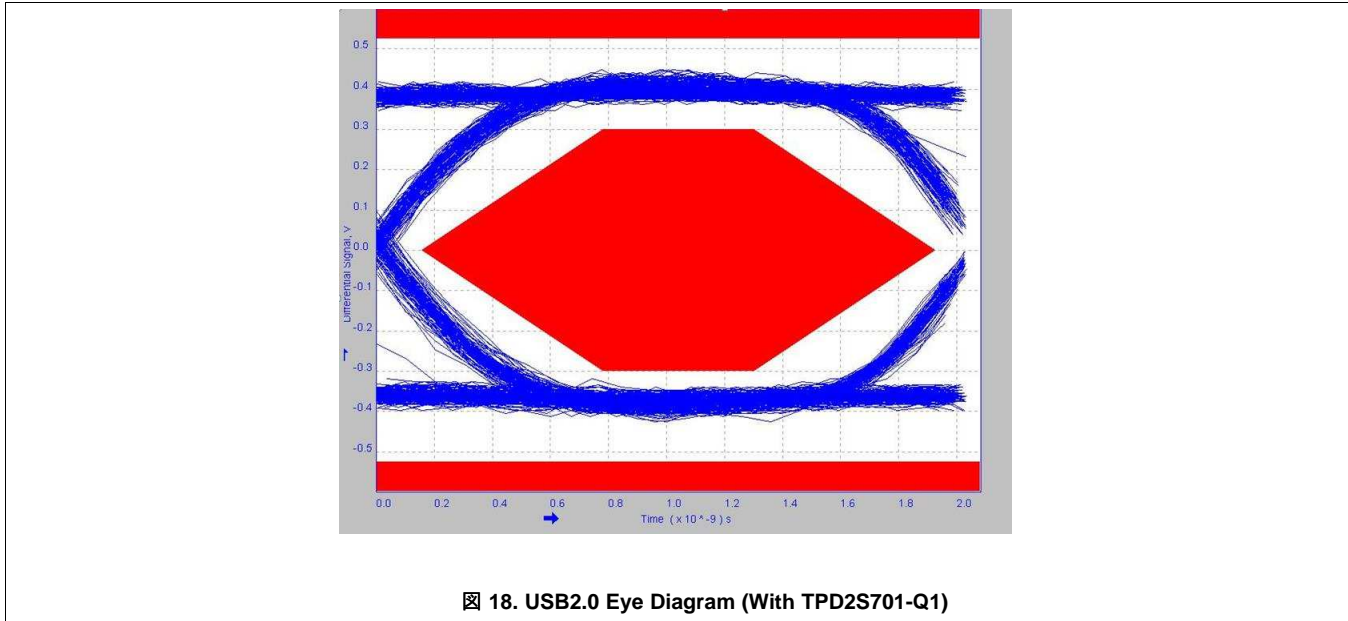
Fig1

Fig 13.  $\overline{FLT}$  Assertion Time During OVP

**Typical Characteristics (continued)**

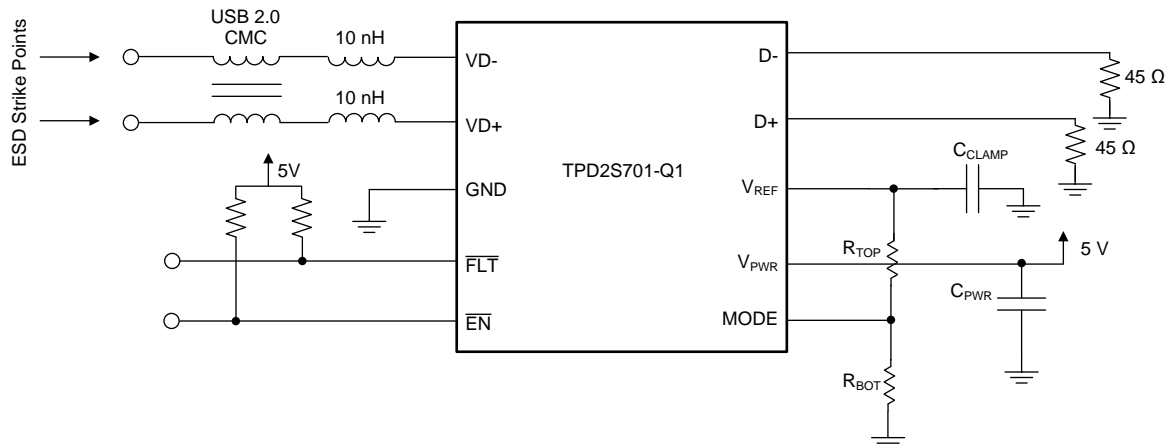


Typical Characteristics (continued)



18. USB2.0 Eye Diagram (With TPD2S701-Q1)

## 7 Parameter Measurement Information



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**19. ESD Setup**

## 8 Detailed Description

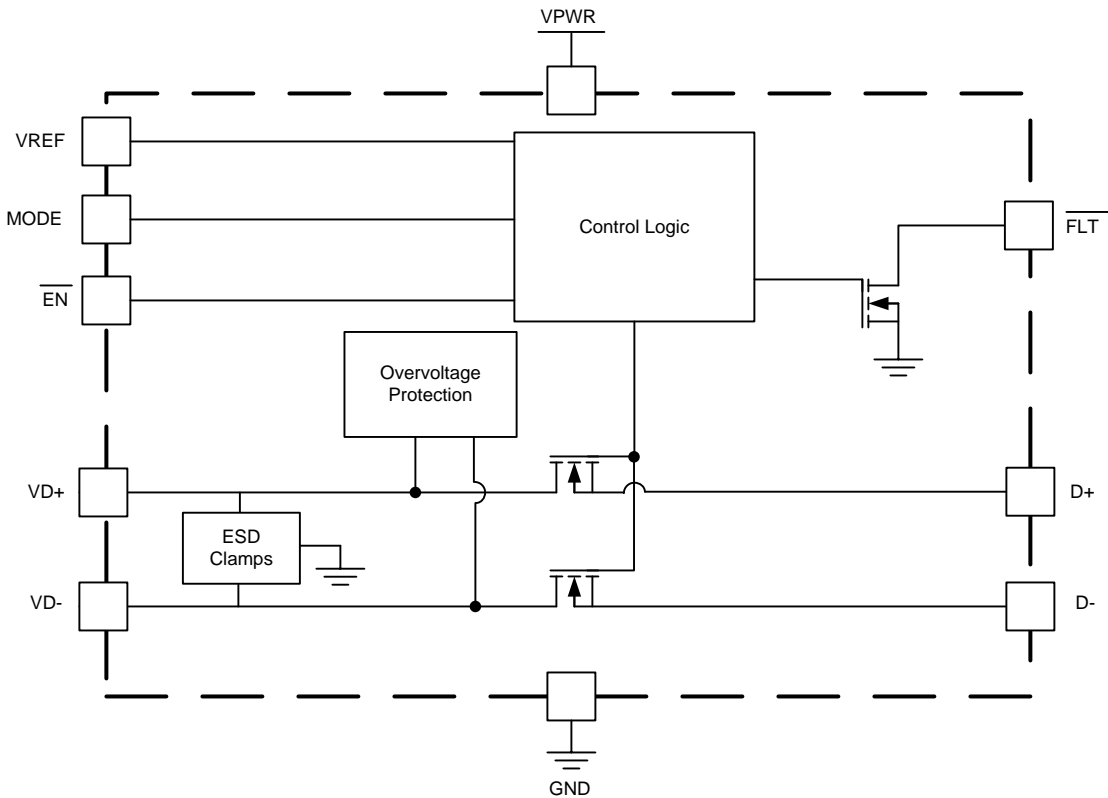
### 8.1 Overview

The TPD2S701-Q1 is a 2-Channel Data Line Short-to- $V_{BUS}$  and IEC61000-4-2 ESD protection device for automotive high-speed interfaces like USB2.0. The TPD2S701-Q1 contains two data line nFET switches which ensure safe data communication while protecting the internal system circuits from any overvoltage conditions at the VD+ and VD- pins. On these pins, this device can handle overvoltage protection up to 7-V DC. This provides sufficient protection for shorting the data lines to the USB  $V_{BUS}$  rail.

Additionally, the TPD2S701-Q1 has a  $\overline{FLT}$  pin which provides an indication when the device sees an overvoltage condition and automatically resets when the overvoltage condition is removed. The TPD2S701-Q1 also integrates IEC ESD clamps on the VD+ and VD- pins, thus eliminating the need for external TVS clamp circuits in the application.

The TPD2S701-Q1 has an internal oscillator and charge pump that controls the turnon of the internal nFET switches. The internal oscillator controls the timers that enable the charge pump and resets the open-drain  $\overline{FLT}$  output. If VD+ and VD- are less than  $V_{OVP}$ , the internal charge pump is enabled. After an internal delay, the charge-pump starts-up, turning on the internal nFET switches. At any time, if VD+ or VD- rises above  $V_{OVP}$ , TPD2S701-Q1 asserts  $\overline{FLT}$  pin LOW and the nFET switches are turned off.

### 8.2 Functional Block Diagram



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## 8.3 Feature Description

### 8.3.1 OVP Operation

When the VD+, or VD– voltages rise above  $V_{OVP}$ , the internal nFET switches are turned off, protecting the transceiver from overvoltage conditions. The response is very rapid, with the FET switches turning off in less than 1  $\mu$ s. Before the OVP condition, the  $\overline{FLT}$  pin is High-Z, and is pulled HIGH via an external resistor to indicate there is no fault. Once the OVP condition occurs, the  $\overline{FLT}$  pin is asserted LOW. When the VD+, or VD– voltages returns below  $V_{OVP} - V_{HYS-OVP}$ , the nFET switches are turned on again. When the OVP condition is cleared and the nFETs are completely turned on, the  $\overline{FLT}$  is reset to high-Z.

### 8.3.2 OVP Threshold

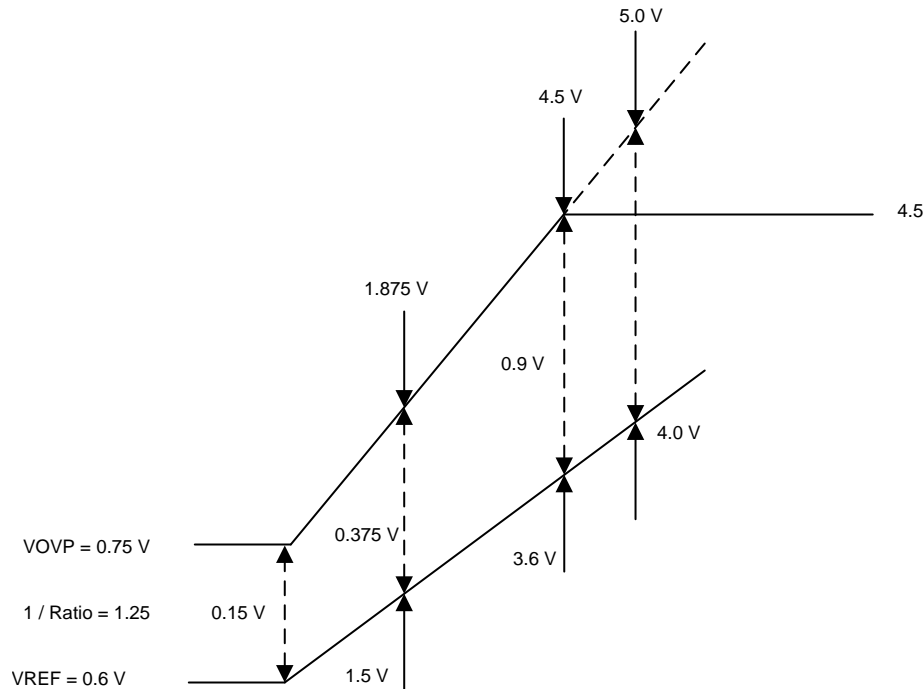


图 20. OVP Threshold

The OVP Threshold  $V_{OVP}$  is set by  $V_{REF}$  according to 式 1, 式 2 and 式 3.

$$V_{OVP} = 1.25 \times V_{REF} \quad (1)$$

$$V_{REF} \leq 3.6 \text{ V} \quad (2)$$

$$V_{OVP} = 4.5 \text{ V for } V_{REF} > 3.6 \text{ V} \quad (3)$$

式 1, 式 2 and 式 3 yield the typical  $V_{OVP}$  values. See the parametric tables for the minimum and maximum values that include variation over temperature and process. 图 20 gives a graphical representation of the relationship between  $V_{OVP}$  and  $V_{REF}$ .

$V_{REF}$  can be set either by an external regulator (Mode 0) or an internal adjustable regulator (Mode 1). See the [V<sub>REF</sub> Operation](#) section for more details on how to operate  $V_{REF}$  in Mode 0 and Mode 1.

### 8.3.3 D± Clamping Voltage

The TPD2S701-Q1 provides a differentiated device architecture which allows the system designer to control the clamping voltage the protected transceiver sees from the D+ and D– pins. This architecture allows the system designer to minimize the amount of stress the transceiver sees during ESD events. The clamping voltage that appears on the D+ and D– lines during an ESD event obeys 式 4.

$$V_{CLAMP\_DP/M} = V_{REF} + V_{BR} + IR_{DYN} \quad (4)$$



## Feature Description (continued)

Where  $V_{BR}$  approximately = 0.7 V,  $I_{RDYN}$  approximately = 1 V. By adjusting  $V_{REF}$ , the clamping voltage of the D+ and D– lines can be adjusted. As  $V_{REF}$  also controls the OVP threshold, take care to insure that the  $V_{REF}$  setting both satisfies the OVP threshold requirements while simultaneously optimizing system protection on the D+ and D– lines.

The size of the capacitor used on the  $V_{REF}$  pin also influences the clamping voltage as transient currents during ESD events flow into the  $V_{REF}$  capacitor. This causes the  $V_{REF}$  voltage to increase, and likewise the clamping voltage on D± according to 式 4. The larger capacitor that is used, the better the clamping performance of the device is going to be. See the parametric tables for the clamping performance of the TPD2S701-Q1 with a 1- $\mu$ F capacitor.

## 8.4 Device Functional Modes

The TPD2S701-Q1 has two modes of operation which vary the way the VREF pin functions. In Mode 0, the VREF pin is connected to an external regulator which sets the voltage on the VREF pin. In Mode 1, the TPD2S701-Q1 uses an adjustable internal regulator to set the VREF voltage. Mode 1 enables the system designer to operate the TPD2S701-Q1 with a single power supply, and have the flexibility to easily set the VREF voltage to any voltage between 0.6 V and 3.8 V with two external resistors.

## 9 Application and Implementation

### 注

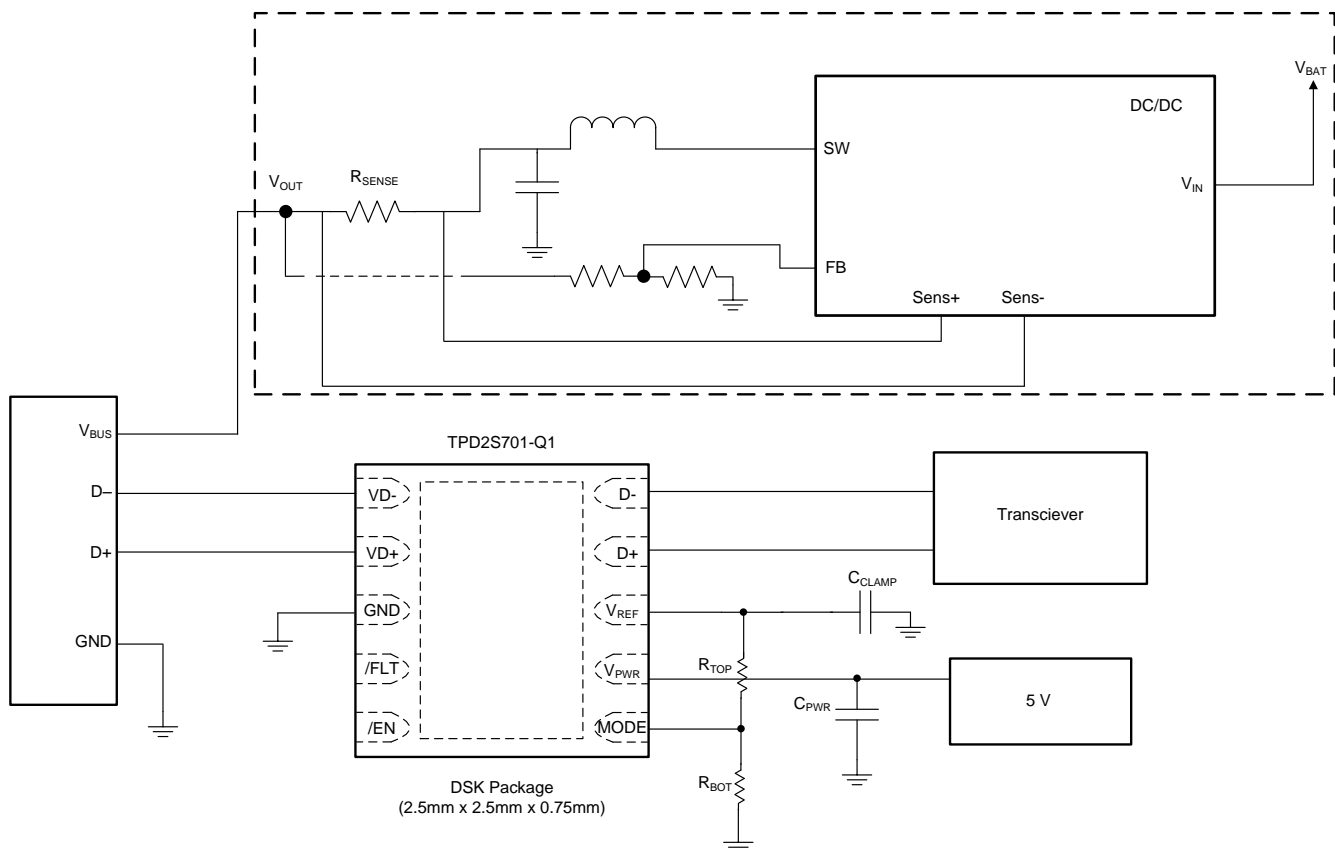
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPD2S701-Q1 offers 2-channels of short-to-VBUS protection and IEC ESD protection for automotive high speed interfaces such as USB 2.0. For the overvoltage protection (OVP), this device integrates N-channel FET's which quickly isolate (200 ns) the protected circuitry in the event of an overvoltage condition on the VD+ and VD– lines. With respect to the ESD protection, the TPD2S701-Q1 has an internal clamping diode on each data line (VD+ and VD–) which provides 8-kV contact ESD protection and 15-kV air-gap ESD protection. More details on the internal components of the TPD2S701-Q1 can be found in the [Overview](#) section.

The TPD2S701-Q1 also has the ability to vary the OVP threshold based on the configuration of the Mode pin and the voltage present on the VREF pin (0.6 V-4.5 V). This functionality is discussed in greater depth in the [OVP Threshold](#) section. Once the VREF threshold is crossed, a fault is detectable to the user through the  $\overline{\text{FLT}}$  pin, where 5 V on the pin indicates no fault is detected, and 0 V-0.4 V represents a fault condition. [Figure 21](#) shows the TPD2S701-Q1 in a typical application, interfacing between the protected internal circuitry and the connector side, where ESD vulnerability is at its highest.

### 9.2 Typical Application



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**Figure 21. USB 2.0 Port With Short-to-V<sub>BUS</sub> and IEC ESD Protection**

## Typical Application (continued)

### 9.2.1 Design Requirements

#### 9.2.1.1 Device Operation

表 1 gives the complete device functionality in response to the  $\overline{\text{EN}}$  pin, to overvoltage conditions at the connector ( $\text{VD}_{\pm}$  pins), to thermal shutdown, and to the conditions of the  $\text{V}_{\text{PWR}}$ ,  $\text{V}_{\text{REF}}$ , and MODE pins.

表 1. Device Operation Table

Functional Mode	$\overline{\text{EN}}$	MODE	VREF	VPWR	VD $_{\pm}$	TJ	$\overline{\text{FLT}}$	Comments
<b>NORMAL OPERATION</b>								
Mode 0 unpowered 1	X	$\text{R}_{\text{bot}} \leq 2.6 \text{ k}\Omega$	X	X	X	X	H	Device unpowered, data switches open
Mode 0 unpowered 2	X	$\text{R}_{\text{bot}} \leq 2.6 \text{ k}\Omega$	X	X	X	X	H	Device unpowered, data switches open
Mode 1 unpowered	X	$\text{R}_{\text{top}} \parallel \text{R}_{\text{bot}} > 14 \text{ k}\Omega$	X	X	X	X	H	Device unpowered, data switches open
Mode 0 disabled	H	$\text{R}_{\text{bot}} \leq 2.6 \text{ k}\Omega$	>UVLO	>UVLO	X	<TSD	H	Device disabled, data switches open
Mode 1 disabled	H	$\text{R}_{\text{top}} \parallel \text{R}_{\text{bot}} > 14 \text{ k}\Omega$	Set by $\text{R}_{\text{top}}$ and $\text{R}_{\text{bot}}$	>UVLO	X	<TSD	H	Device disabled, data switches open, $\text{V}_{\text{REF}}$ is disabled
Mode 0 enabled	L	$\text{R}_{\text{bot}} \leq 2.6 \text{ k}\Omega$	>UVLO	>UVLO	<OVP	<TSD	H	Device enabled, data switches closed, $\text{V}_{\text{REF}}$ is the value set by the power supply on $\text{V}_{\text{REF}}$
Mode 1 enabled	L	$\text{R}_{\text{top}} \parallel \text{R}_{\text{bot}} > 14 \text{ k}\Omega$	Set by $\text{R}_{\text{top}}$ and $\text{R}_{\text{bot}}$	>UVLO	<OVP	<TSD	H	Device enabled, data switches closed, $\text{V}_{\text{REF}}$ is the value set by the $\text{R}_{\text{top}}$ and $\text{R}_{\text{bot}}$ resistor divider
<b>FAULT CONDITIONS</b>								
Mode 0 thermal shutdown	X	$\text{R}_{\text{bot}} \leq 2.6 \text{ k}\Omega$	X	>UVLO	X	>TSD	L	Thermal shutdown, data switches opened, $\overline{\text{FLT}}$ pin asserted
Mode 1 thermal shutdown	X	$\text{R}_{\text{top}} \parallel \text{R}_{\text{bot}} > 14 \text{ k}\Omega$	Set by $\text{R}_{\text{top}}$ and $\text{R}_{\text{bot}}$	>UVLO	X	>TSD	L	Thermal shutdown, data switches opened, $\text{V}_{\text{REF}}$ is disabled, $\overline{\text{FLT}}$ pin asserted
Mode 0 OVP fault	L	$\text{R}_{\text{bot}} \leq 2.6 \text{ k}\Omega$	>UVLO	>UVLO	>OVP	<TSD	L	Data line overvoltage protection mode. OVP is set relative to the voltage on $\text{V}_{\text{REF}}$ . Data switches opened, $\overline{\text{FLT}}$ pin asserted
Mode 1 OVP fault	L	$\text{R}_{\text{top}} \parallel \text{R}_{\text{bot}} > 14 \text{ k}\Omega$	Set by $\text{R}_{\text{top}}$ and $\text{R}_{\text{bot}}$	>UVLO	>OVP	<TSD	L	Data line overvoltage protection mode. OVP is set relative to the voltage on $\text{V}_{\text{REF}}$ . Data switches opened, fault pin asserted

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 $\text{V}_{\text{REF}}$ Operation

The TPD2S701-Q1 has two modes of operation which vary the way the  $\text{V}_{\text{REF}}$  pin functions. In Mode 0, the  $\text{V}_{\text{REF}}$  pin is connected to an external regulator which sets the voltage on the  $\text{V}_{\text{REF}}$  pin. In Mode 1, the TPD2S701-Q1 uses an adjustable internal regulator to set the  $\text{V}_{\text{REF}}$  voltage. Mode 1 enables the system designer to operate the TPD2S701-Q1 with a single power supply, and have the flexibility to easily set the  $\text{V}_{\text{REF}}$  voltage to any voltage between 0.6 V and 3.8 V with two external resistors.

##### 9.2.2.1.1 Mode 0

To set the device into Mode 0, ensure that  $\text{R}_{\text{bot}}$ , resistance between the MODE pin and ground, is less than 2.6 k $\Omega$ . The easiest way to implement Mode 0 is to directly connect the mode pin to GND on your PCB. With this resistance condition met, connect  $\text{V}_{\text{REF}}$  to an external regulator to set the  $\text{V}_{\text{REF}}$  voltage.

### 9.2.2.1.2 Mode 1

To operate in Mode 1, ensure that  $R_{top} \parallel R_{bot}$ , resistance between the MODE pin and ground, is greater than 14 k $\Omega$ . This is accomplished by insuring  $R_{top} \parallel R_{bot} > 14 \text{ k}\Omega$  because when the device is initially powered up,  $V_{REF}$  is at ground until the internal circuitry recognizes if the device is in Mode 1 or Mode 2.

In Mode 1,  $V_{REF}$  is set by using an internal regulator to set the voltage. Using a resistor divider off of a feedback comparator is how to set  $V_{REF}$ , similar to a standard LDO or DC/DC.  $V_{REF}$  is set in Mode 1 according to 式 5.

$$V_{REF} = \frac{V_{MODE}(R_{TOP} + R_{BOT})}{R_{BOT}} \quad (5)$$

式 5 yields the typical value for  $V_{REF}$ . When using  $\pm 1\%$  resistors  $R_{TOP}$  and  $R_{BOT}$ ,  $V_{REF}$  accuracy is going to be  $\pm 5\%$ . Therefore, the minimum and maximum values for  $V_{REF}$  can be calculated off of the typical  $V_{REF}$ . The parametric tables above give example  $R_{TOP}$  and  $R_{BOT}$  resistors to use for standard output  $V_{REF}$  voltages for Mode 1.

### 9.2.2.2 Mode 1 Enable Timing

In Mode 1, when the TPD2S701-Q1 is disabled, the output regulator is disabled, leading  $V_{REF}$  to discharge to 0 V through  $R_{TOP}$  and  $R_{BOT}$ . It is desired for  $V_{REF}$  to be at 0 V when the device is disabled to minimize the clamping voltage during a power disabled ESD event. If  $V_{REF}$  is at 0 V, this holds  $D_{\pm}$  near ground during these fault events.

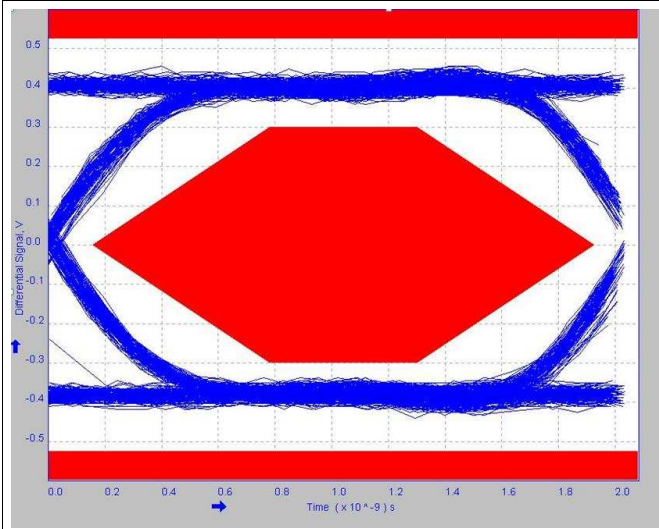
When enabling the TPD2S701-Q1,  $V_{REF}$  is quickly charged up to insure a quick turnon time of the Data FETs. Data FET turnon is gated by  $V_{REF}$  reaching 80% of its final voltage plus 150  $\mu\text{s}$  to insure a proper OVP threshold is set before passing data. This prevents false OVPs due to normal operation. Because Data FET turnon is gated by charging the  $V_{REF}$  clamping capacitor, the size of the capacitor influences the turnon time of the Data switches. The TPD2S701-Q1's internal regulator uses a constant current source to quickly charge the  $V_{REF}$  clamping capacitor, so the charging time of  $C_{VREF}$  can easily be calculated with 式 6.

$$t_{CHG\_CVREF} = \frac{C_{VREF} \times 0.8 (V_{REF\_FINAL})}{I_{CHG\_VREF}} \quad (6)$$

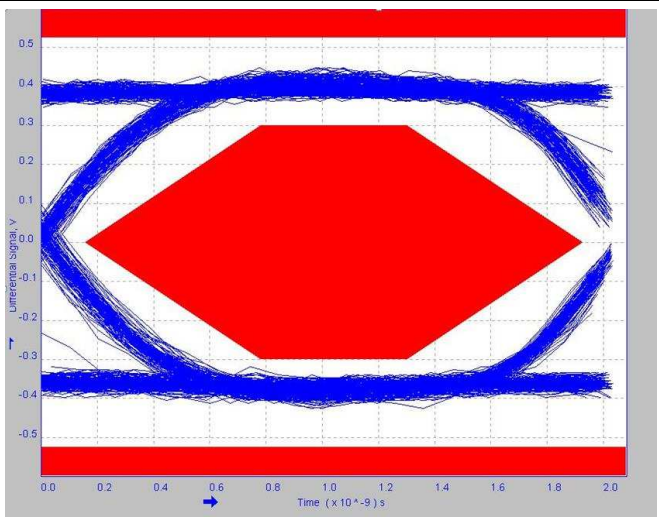
Where  $C_{VREF}$  is the clamping capacitance on  $V_{REF}$ ,  $V_{REF\_FINAL}$  is the final value  $V_{REF}$  is set to, and  $I_{CHG\_VREF} = 22 \text{ mA}$  (typical). If  $V_{REF} = 1 \text{ V}$ , 0.8 is used in the above equation because 80% of  $V_{REF}$  is the amount of time that gates the turnon of the Data FETs. Once  $t_{CHG\_CVREF}$  is calculated, the typical turnon time of the Data FETs can be calculated from 式 7.

$$t_{ON\_EN\_MODE1} = t_{CHG\_CVREF} + 150 \mu\text{s} \quad (7)$$

**9.2.3 Application Curves**



☒ 22. USB2.0 Eye Diagram (Board Only, Through Path)



☒ 23. USB2.0 Eye Diagram (System from Typical Application Schematic)

**10 Power Supply Recommendations**

**10.1 V<sub>PWR</sub> Path**

The V<sub>PWR</sub> pin provides power to the TPD2S701-Q1. A 10-μF capacitor is recommended on V<sub>PWR</sub> as close to the pin as possible for localized decoupling of transients. A supply voltage above the UVLO threshold for V<sub>PWR</sub> must be supplied for the device to power on.

**10.2 V<sub>REF</sub> Pin**

The V<sub>REF</sub> pin provides a voltage reference for the data switch OVP level as well as a bypass for ESD clamping. A 1-μF capacitor must be placed as close to the pin as possible and the supply must be set to be above the UVLO threshold for V<sub>REF</sub>.

## 11 Layout

### 11.1 Layout Guidelines

Proper routing and placement maintains signal integrity for high-speed signals. The following guidelines apply to the TPD2S701-Q1:

- Place the bypass capacitors as close as possible to the VPWR and VREF pins. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as ESD or overcurrent conditions.
- High speed traces (data switch path) must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the VD+, VD- pins as well:

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 11.2 Layout Example

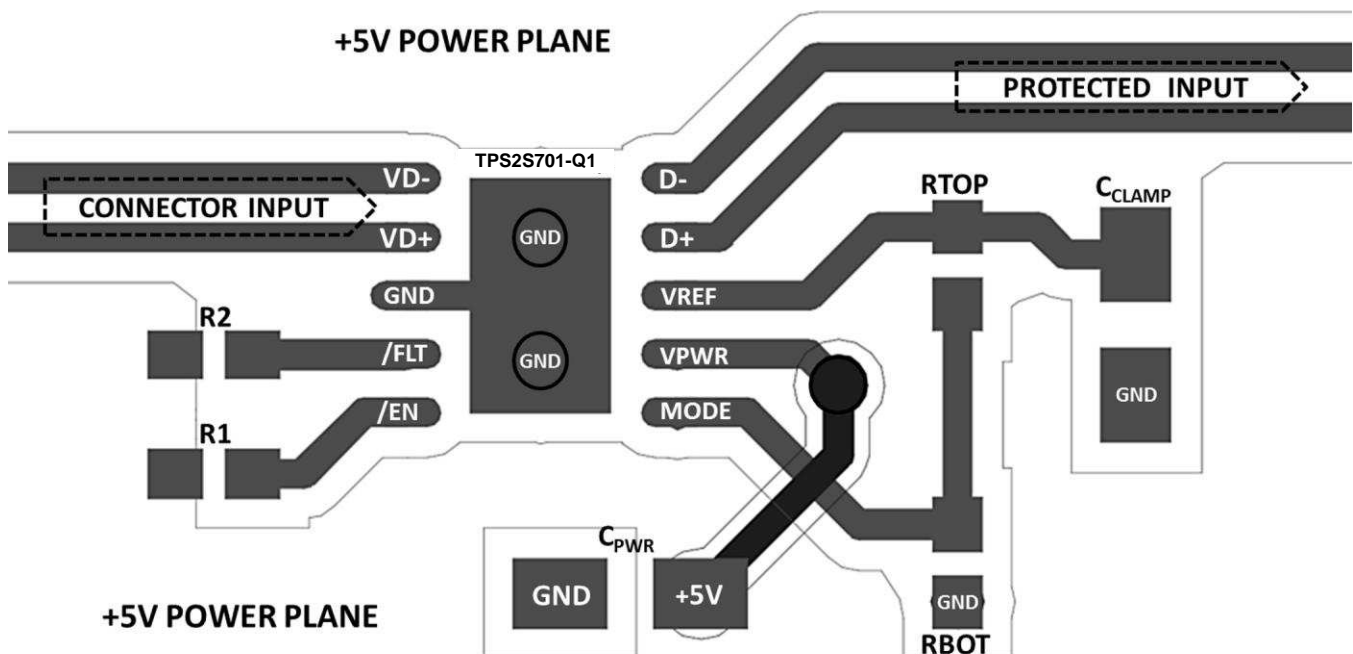


图 24. TPD2S701-Q1 Layout

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントのサポート

#### 12.1.1 関連資料

関連資料については、以下を参照してください。

[『TPD2S701-Q1評価モジュール・ユーザー・ガイド』](#)

### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.4 商標

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### 12.5 静電気放電に関する注意事項



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### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2S701QDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	15R	<b>Samples</b>
TPD2S701QDSKRQ1	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14H	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S701QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPD2S701QDSKRQ1	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S701QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0
TPD2S701QDSKRQ1	SON	DSK	10	3000	210.0	185.0	35.0

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

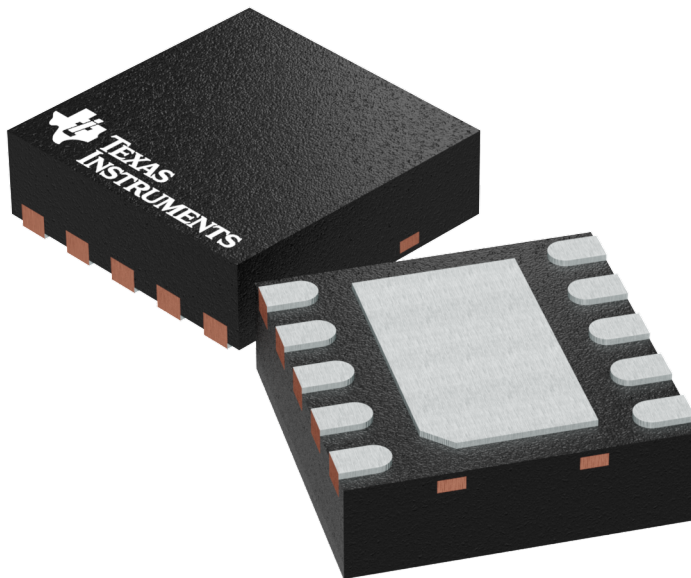
## GENERIC PACKAGE VIEW

**DSK 10**

**WSON - 0.8 mm max height**

**2.5 x 2.5 mm, 0.5 mm pitch**

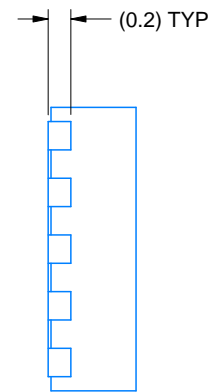
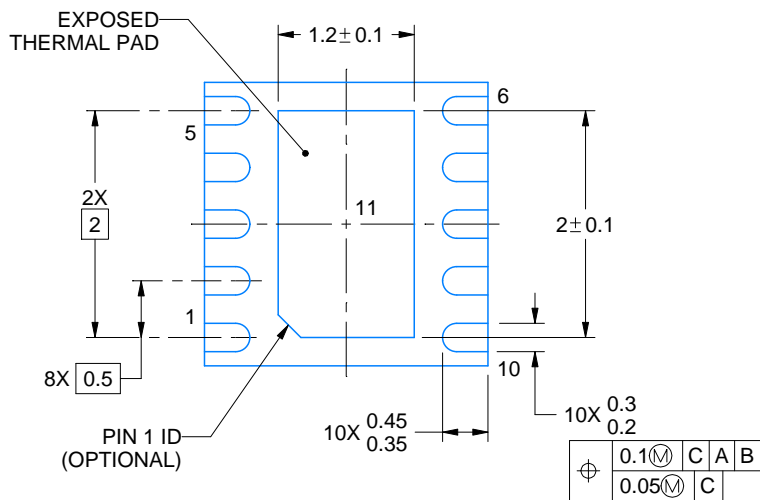
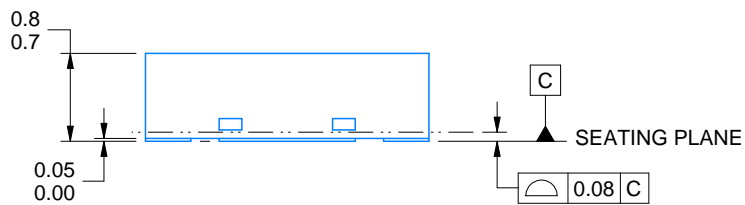
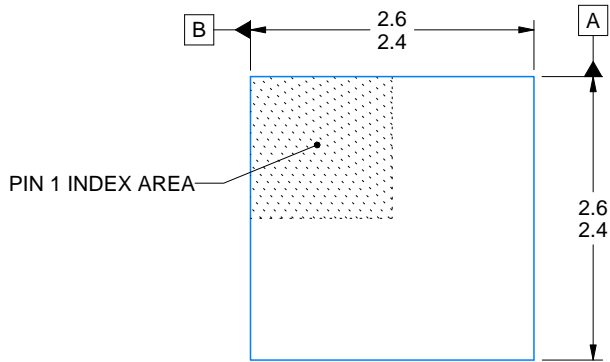
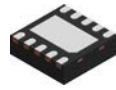
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4225304/A





4218903/B 10/2020

NOTES:

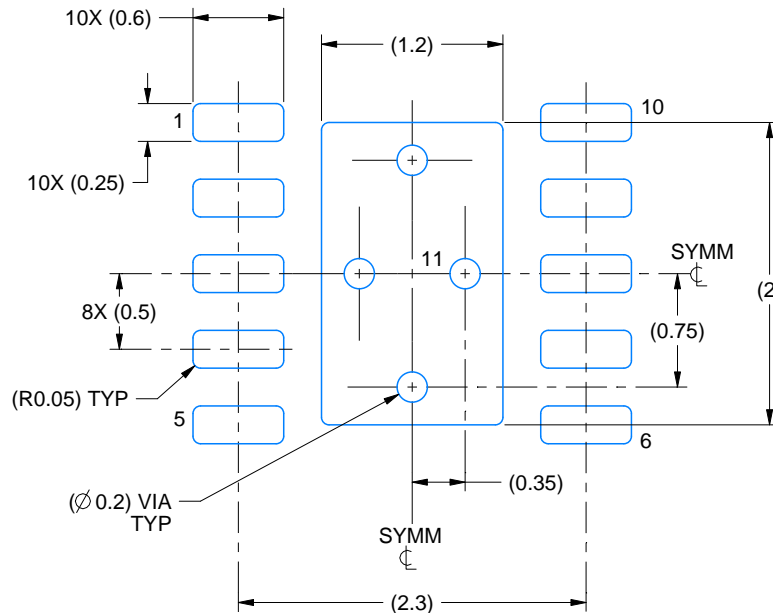
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

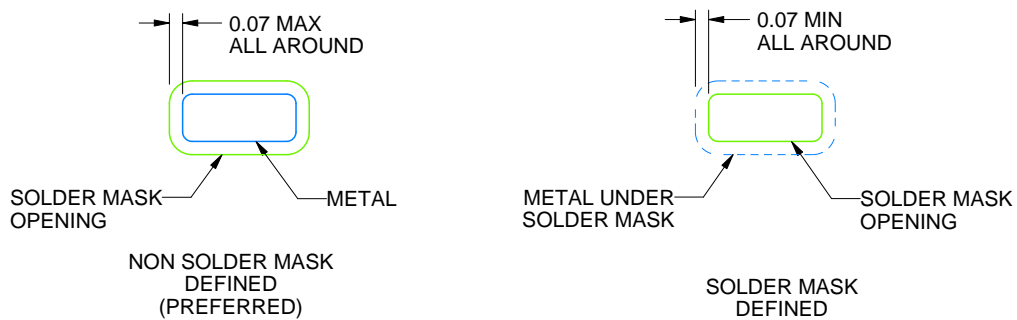
DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

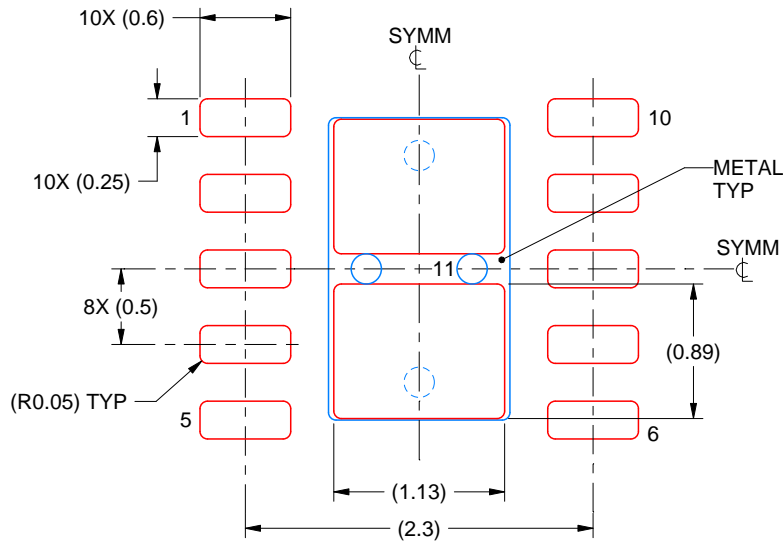
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11  
84% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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