TEXAS INSTRUMENTS
TPD6E004
JAJSQV3C – FEBRUARY 2008 – REVISED JULY 2023

TPD6E004 低容量、6 チャネル、±15kV ESD 保護アレイ、高速データ・インターフェイス用

1 特長

- JESD を上回る ESD 保護:
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2 接触放電
  - ±12kV IEC 61000-4-2 エアギャップ放電
- 1.6pF の低 I/O 容量
- 電源電圧範囲:0.9V～5.5V
- 6 チャネル・デバイス
- 省スペースの UQFN (RSE) パッケージ

2 アプリケーション

- USB
- イーサネット™
- FireWire™
- ビデオ
- 携帯電話
- SVGA ビデオ接続
- 血糖値計

3 概要

TPD6E004 デバイスは低容量の ±15kV ESD 保護ダイオード・アレイで、通信ラインに接続された敏感な電子機器を保護するよう設計されています。各チャネルは 1 対のダイオードで構成され、ESD 電流パルスを V_{CC} または GND に制御します。TPD6E004 は、IEC 61000-4-2 に規定されている ±15kV までの人体モデル (HBM)、±8kV の接触 ESD、および ±12kV のエアギャップ ESD から保護します。
このデバイスにはチャネルごとに標準値 1.6pF の容量があり、高速データ I/O インターフェイスでの使用に最適です。

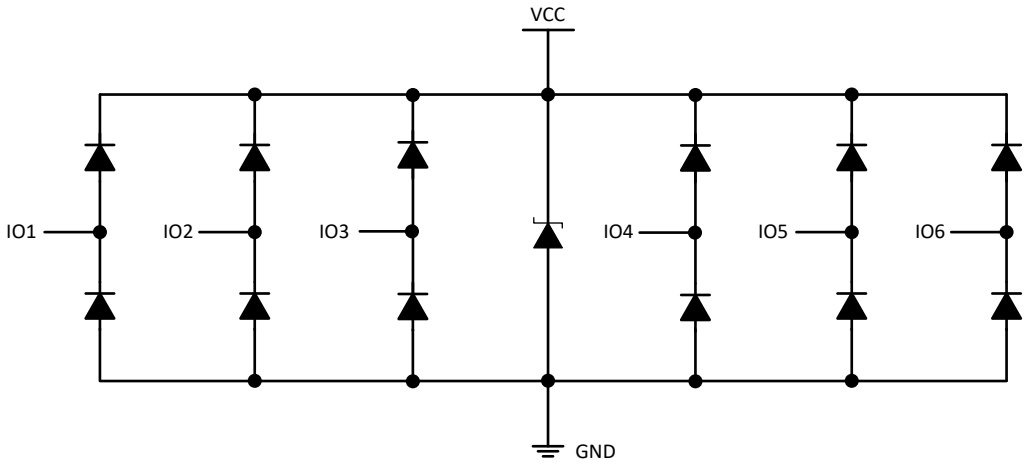
TPD6E004 は RSE パッケージで供給され、–40℃～+85℃の範囲で動作が規定されています。

TPD6E004 デバイスは 6 チャネルの ESD 構造で、USB、イーサネット、FireWire アプリケーション用に設計されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TPD6E004	RSE (UQFN、8)	1.5mm × 1.5mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (February 2016) to Revision C (July 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- パッケージ・リード・サイズを含めるよう「パッケージ情報」表を更新 ... 1

Changes from Revision A (February 2008) to Revision B (February 2016) — **Page**

- 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 ... 1

5 Pin Configuration and Functions

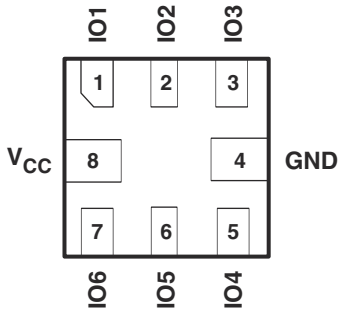


図 5-1. RSE Package, 8-Pin UQFN (Bottom View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO1	1	I/O	ESD-protected channel
IO2	2	I/O	ESD-protected channel
IO3	3	I/O	ESD-protected channel
GND	4	GND	Ground
IO4	5	I/O	ESD-protected channel
IO5	6	I/O	ESD-protected channel
IO6	7	I/O	ESD-protected channel
V_{CC}	8	PWR	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.

(1) I = input, O = output, GND = ground, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Operating voltage for pin VCC		–0.3	5.5	V
$V_{I/O}$	Operating voltage for pins IO1, IO2, IO3, IO4, IO5 and IO6		–0.3	V_{CC} + 0.3	V
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Surge Protection

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000	V
		IEC 61000-4-2 air-gap discharge	±12000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	85	°C
V_{CC}	Operating voltage for pin VCC	0.9	5.5	V
$V_{I/O}$	Operating voltage for pins IO1, IO2, IO3, IO4, IO5 and IO6	0	Minimum of: (5.8, V_{CC})	V

6.5 Thermal Information

THERMAL METRIC(1)		TPD6E004 RSE (UQFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

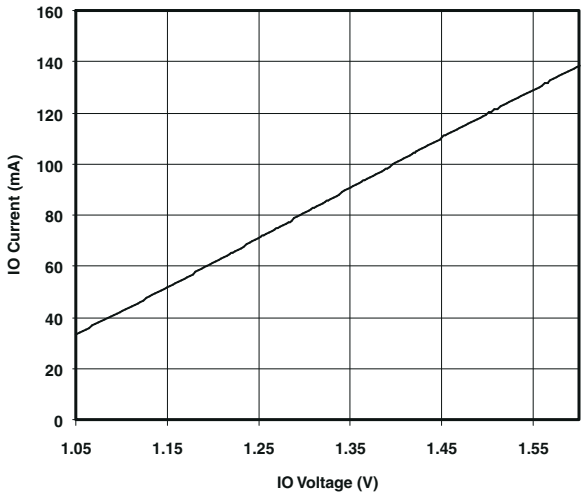
6.6 Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{CC}	Supply voltage		0.9		5.5	V
I_{CC}	Supply current				500	nA
V_F	Diode forward voltage	I_F = 1 mA		0.8		V
I_I	Channel leakage current			±1		nA
V_{BR}	Break-down voltage	I_I = 10 µA	6		8	V
$C_{I/O}$	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2, f = 10 MHz		1.6	2	pF

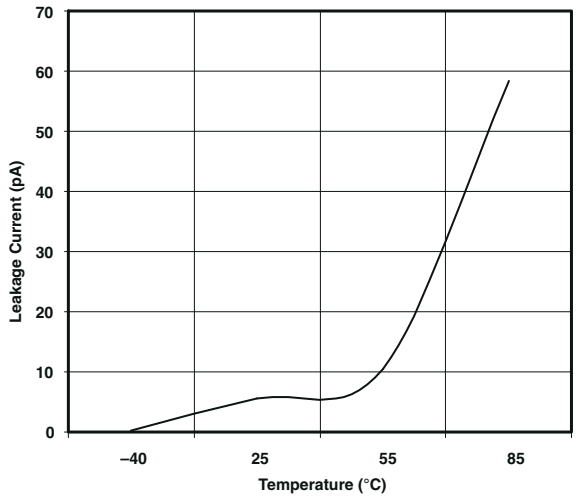
(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.

6.7 Typical Characteristics



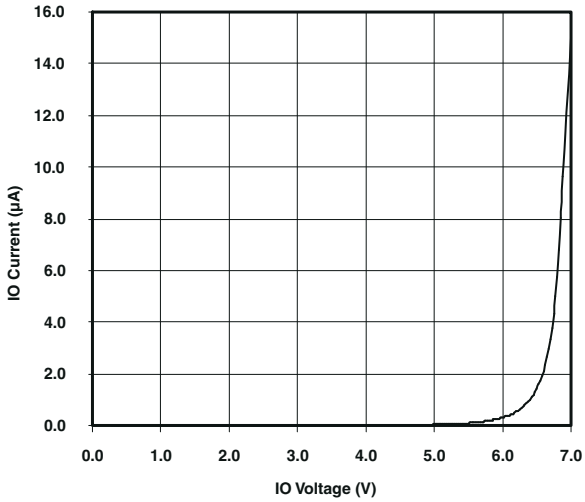
V_{CC} = 0 V, DC Sweep Across the I/O Pin

図 6-1. Forward Diode Voltage (Upper Clamp Diode)



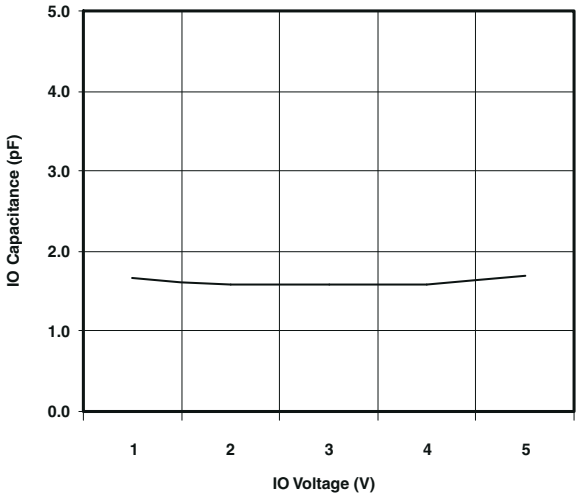
$V_{I/O}$ = 2.5 V

図 6-2. Leakage Current vs Temperature



V_{CC} = Open

図 6-3. Reverse Diode Curve Current I/O to GND



V_{CC} = 5 V

図 6-4. I/O Capacitance vs Input Voltage

7 Detailed Description

7.1 Overview

The TPD6E004 device is a six-channel TVS protection diode array. The TPD6E004 is rated to dissipate ESD strikes of ±8-kV contact and ±12-kV air-gap, as specified in the IEC 61000-4-2 international standard. This device has 1.6-pF capacitance per I/O channel, making it an excellent choice for use in high-speed data I/O interfaces.

7.2 Functional Block Diagram

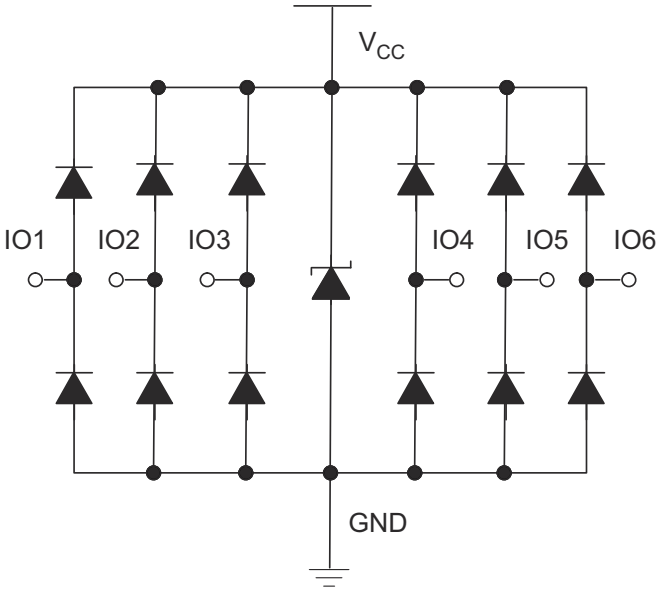


図 7-1. Logic Block Diagram

7.3 Feature Description

The TPD6E004 is a TVS that provides ESD protection for up to six channels, withstanding up to ±8-kV contact and ±12-kV air-gap ESD per IEC 61000-4-2. The monolithic technology yields exceptionally small variations in capacitance between any I/O pin of the TPD6E004. The small footprint is an excellent choice for applications where space-saving designs are important.

7.4 Device Functional Modes

The TPD6E004 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the diodes V_F of approximately –0.8 V. During ESD events, voltages as high as ±8-kV contact and ±12-kV air-gap ESD can be directed to ground through the internal diodes. When the voltages on the protected line fall below the trigger levels of TPD6E004 (usually within 10s of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPD6E004 device is a TVS diode array typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected integrated circuit (IC). The triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

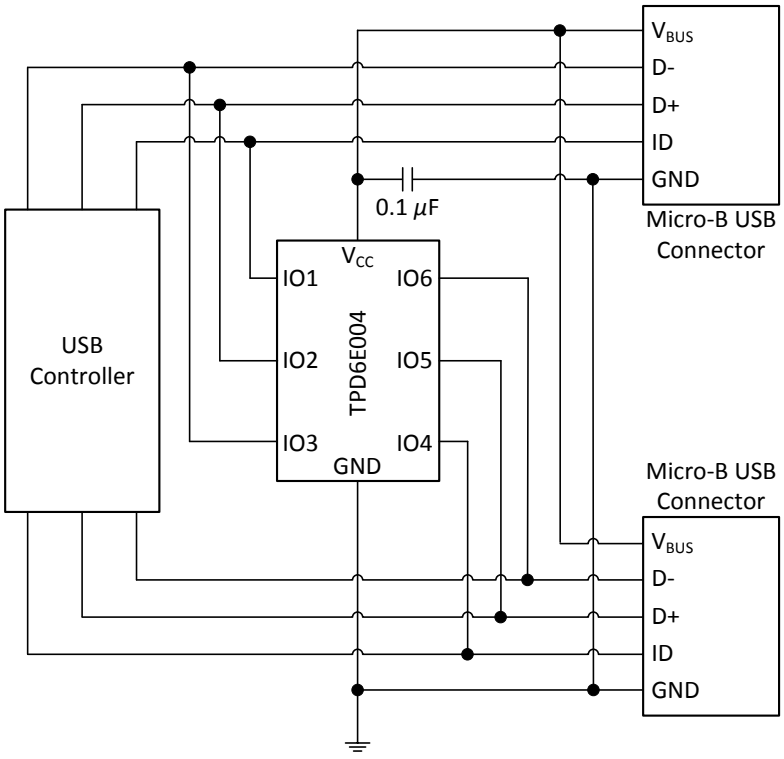


図 8-1. Two-Port Micro-B USB 2.0 Application

8.2.1 Design Requirements

For this design example, a single TPD6E004 is used to protect all the pins of two USB 2.0 Micro-B connectors. 表 8-1 lists the design parameters for the USB application.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, IO4, IO5 and IO6	0 V to 3.6 V
Signal voltage range on V_{CC}	0 V to 5.5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD6E004 ESD solution offers little or no signal distortion during normal operation due to low I/O capacitance and ultra-low leakage current specifications. The TPD6E004 is designed to protect the core circuitry and allow the system to function properly in the event of an ESD strike. For proper operation, the *Layout Guidelines* and following design guidelines must be followed:

1. Place the TPD6E004 solution close to the connectors. This allows the TPD6E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the I/O pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD6E004 consumes only µA of leakage current, but during an ESD event, V_{CC} and GND may see 15-A to 30-A of current, depending on the ESD level. A sufficient current path enables the safe discharge of all the energy associated with the ESD strike.
4. Leave any unused I/O pins floating. In this example of protecting two Micro-B USB ports, none of the I/O pins are left unused.
5. The V_{CC} pin can be connected in two different ways:
   a. If the V_{CC} pin is connected to the system power supply, then the TPD6E004 works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-µF capacitor on the device V_{CC} pin for ESD bypass.
   b. If the V_{CC} pin is not connected to the system power supply, then the TPD6E004 can tolerate a higher signal swing in the range of up to 5.8 V.

注

A 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curve

図 8-2 is a capture of the voltage clamping waveform of the TPD6E004 during a +8-kV contact IEC 61000-4-2 ESD strike.

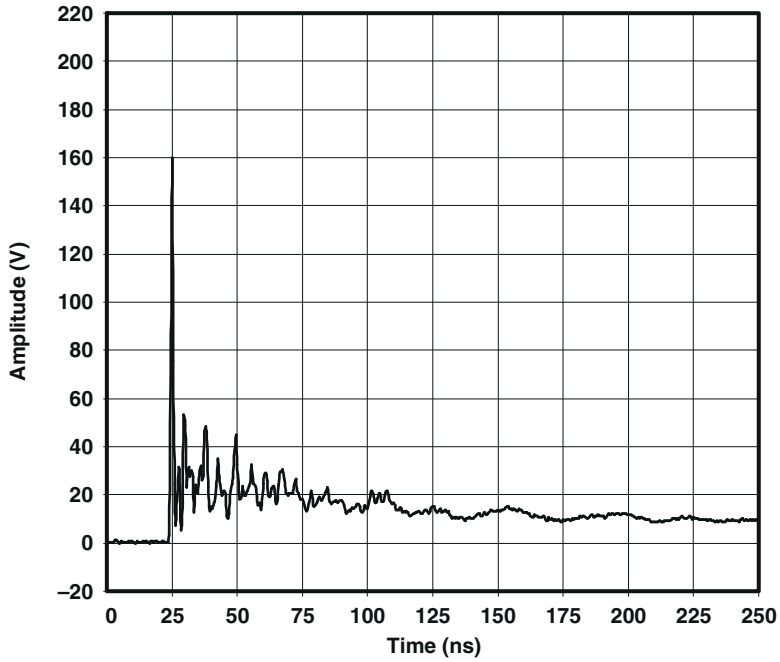


図 8-2. IEC 61000-4-2 +8-kV Contact ESD Clamping Waveform

8.3 Power Supply Recommendations

The TPD6E004 device is a passive ESD protection device, so there is no need to power it. Do not violate the maximum voltage specifications for each pin.

8.4 Layout

8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any corners less than 135° on the protected traces between the TVS and the connector. Best practice is using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Connect the ground pin to a same layer ground pour which is connected to an internal ground plane with a via. Place the via very near the ground pin.

8.4.2 Layout Example

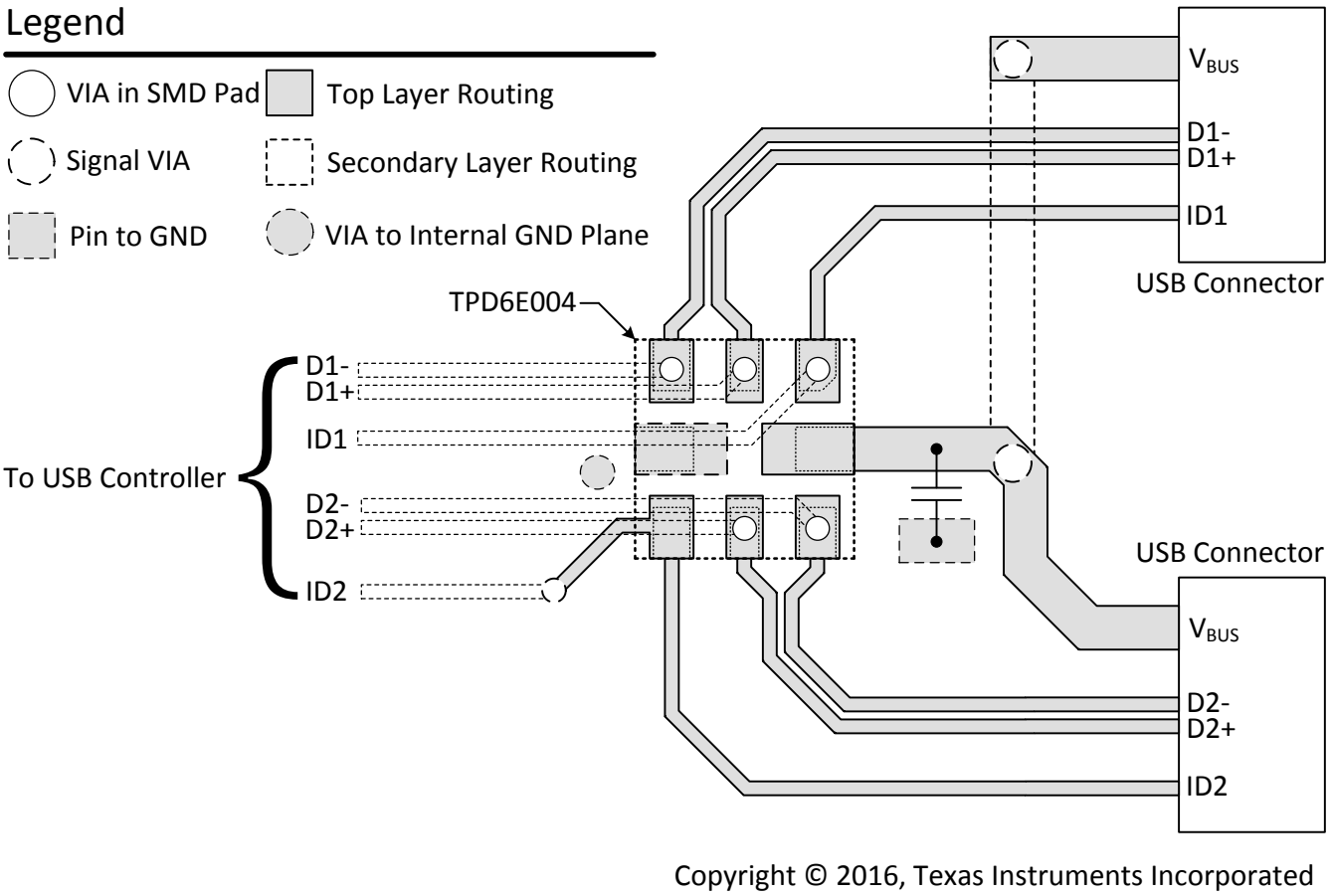


図 8-3. TPD6E004 Layout Example for Two USB 2.0 Micro-B Connectors

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*
- Texas Instrument, *ESD Protection Layout Guide*

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD6E004RSER	ACTIVE	UQFN	RSE	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

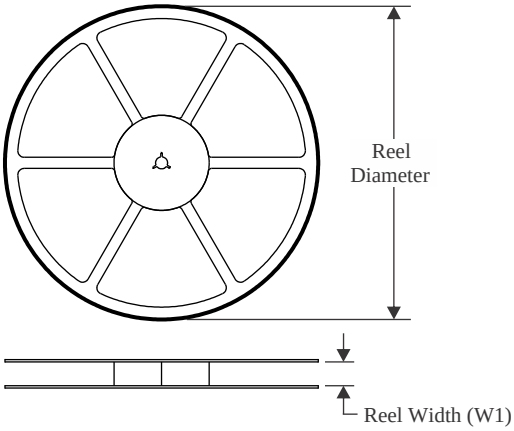
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

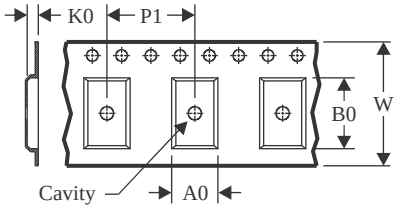
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

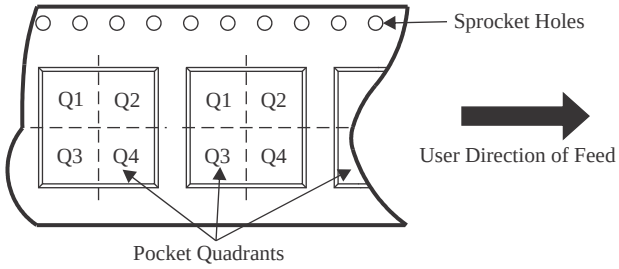


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

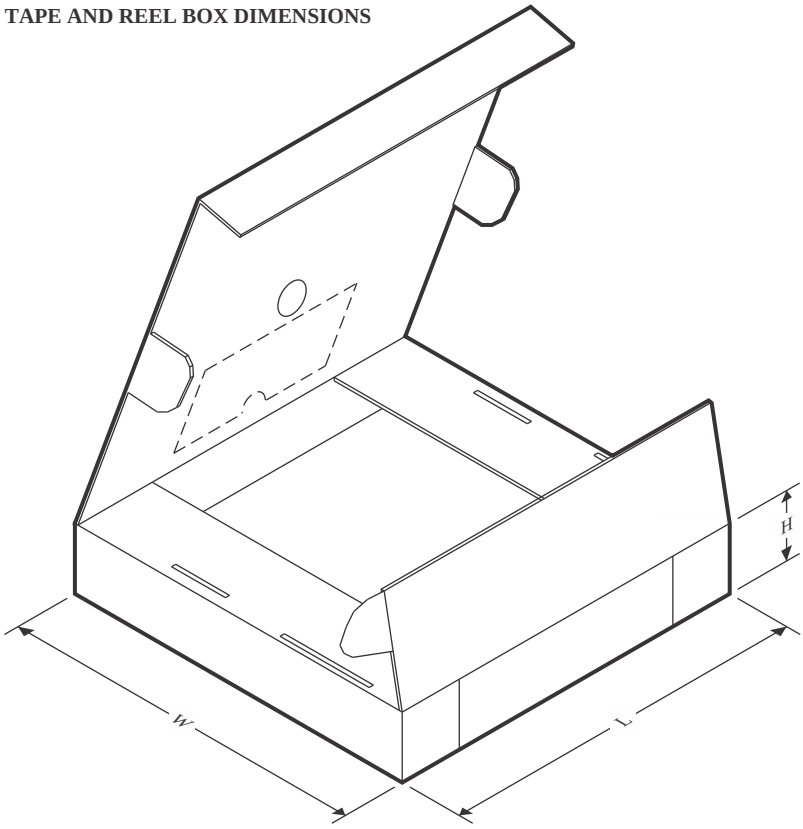
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6E004RSER	UQFN	RSE	8	3000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

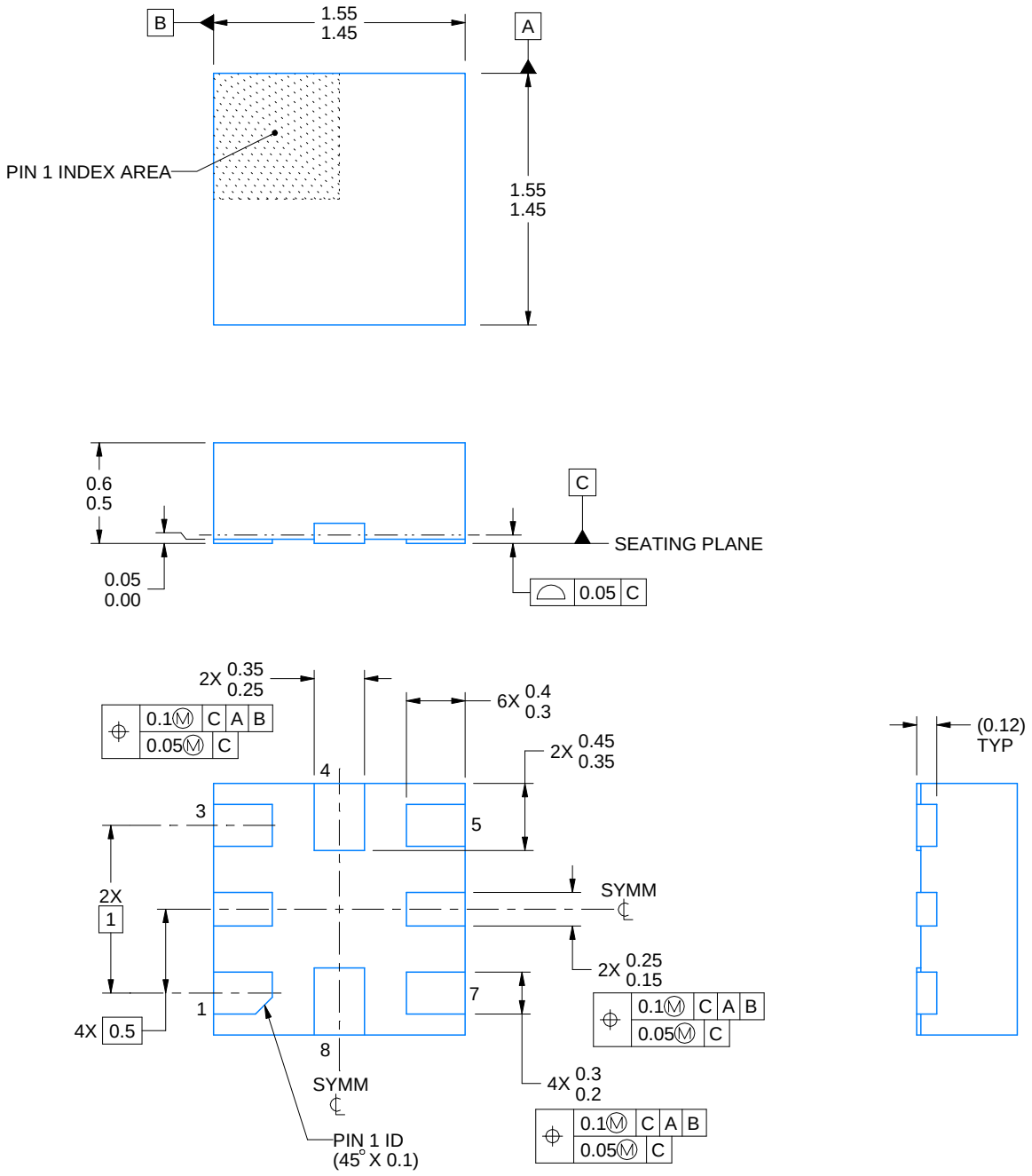
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6E004RSER	UQFN	RSE	8	3000	184.0	184.0	19.0

RSE0008A

PACKAGE OUTLINE

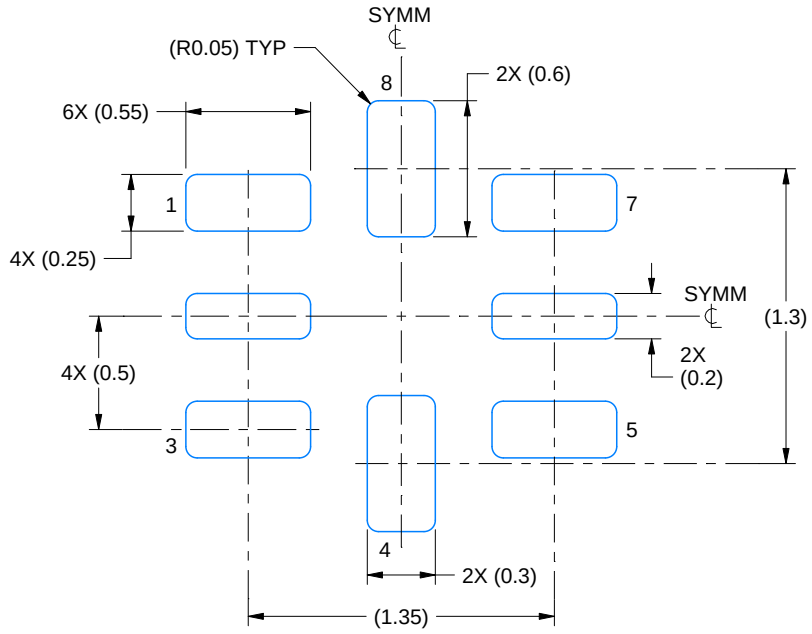
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

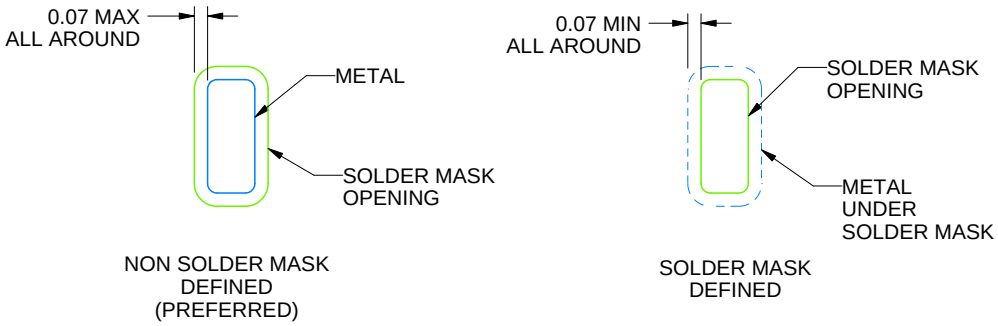


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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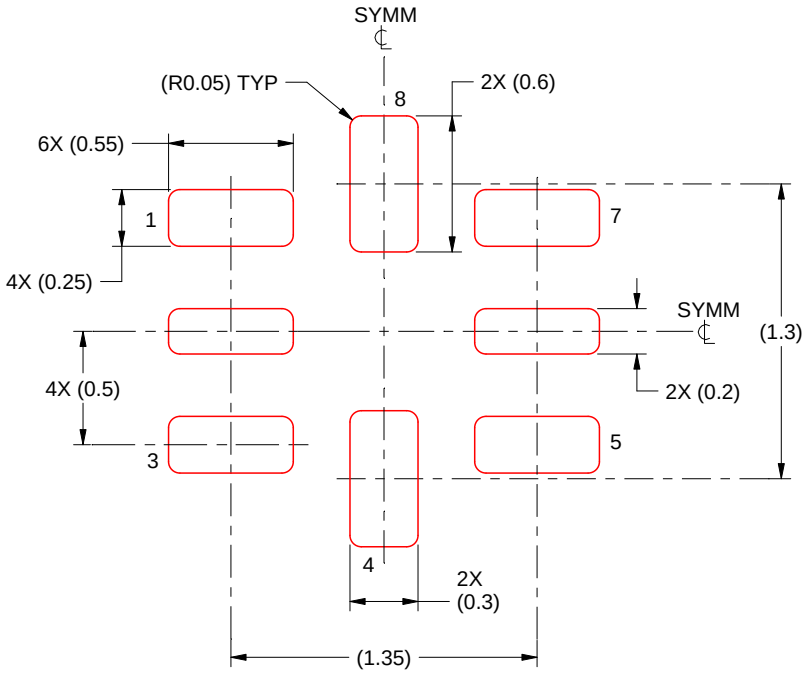
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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