TPS2061, TPS2062, TPS2063
TPS2065, TPS2066, TPS2067
JAJSPW9J – DECEMBER 2003 – REVISED AUGUST 2023

電流制限付き配電スイッチ

1 特長

- 70mΩ のハイサイド MOSFET
- 1A の連続電流
- 過熱および短絡保護
- 正確な電流制限
  (最小 1.1A、最大 1.9A)
- 動作範囲:2.7V～5.5V
- 0.6ms の立ち上がり時間 (代表値)
- 低電圧誤動作防止
- デグリッチ・フォルト・レポート ($\overline{OC}$)
- 電源投入時の $\overline{OC}$ グリッチなし
- スタンバイ時消費電流:最大 1µA
- 双方向スイッチ
- 周囲温度範囲:-40℃～85℃
- ソフトスタート機能内蔵
- UL 認定済み:ファイル番号 E169910

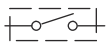
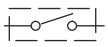
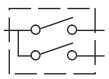
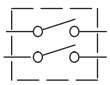
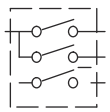
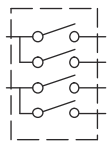
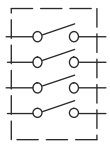
2 アプリケーション

- 大きな容量性負荷
- 短絡保護

3 概要

TPS206x 配電スイッチは、大きな容量性負荷と短絡が発生しやすいアプリケーションを対象としています。このデバイスは、1 つのパッケージに複数のパワー・スイッチを搭載する必要がある配電システム向けに、70mΩ の N チャネル MOSFET パワー・スイッチを内蔵しています。各スイッチは、ロジック・イネーブル入力によって制御されます。ゲート・ドライブは、スイッチング中の電流サージを最小限に抑えるためにパワー・スイッチの立ち上がり時間と立ち下がり時間を制御するように設計された、内部チャージ・ポンプによって提供されています。チャージ・ポンプには外付け部品が不要で、最低 2.7V の電源で動作できます。

GENERAL SWITCH CATALOG

33 mΩ, Single	80 mΩ, Single	80 mΩ, Dual	80 mΩ, Dual	80 mΩ, Triple	80 mΩ, Quad	80 mΩ, Quad
						
TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (October 2009) to Revision J (August 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Added $r_{DS(on)}$ for DBV package ... 6
- Updated TPS2065DBV electrical characteristics, including overcurrent trip threshold, high-level output supply current and undervoltage lockout ... 6
- Updated TPS2065DBV Typical Characteristics ... 14
- Moved overcurrent description from Application and Implementation section to Detailed Description section ... 21
- Added TPS2065DBV overcurrent description ... 21

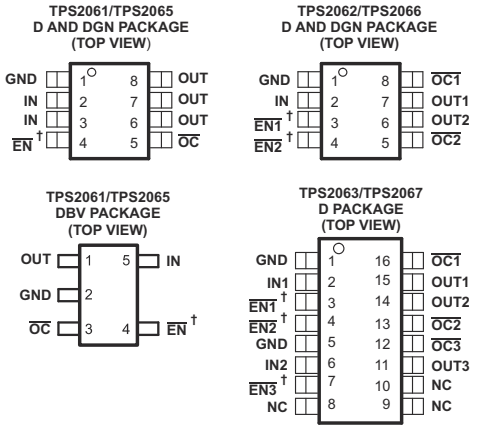
Changes from Revision H (December 2008) to Revision I (October 2009) — **Page**

- ESD の記載を変更 ... 3
- Changed the Abs Max Ratings table - Operating virtual junction temperature range From: -40°C to 125°C To: -40°C to 150°C ... 6
- Deleted Storage temperature range, T_{stg} from the Abs Max Ratings table ... 6
- Deleted MIL-STD-883C reference from ESD in the Abs Max table ... 6
- Added 3 table notes to the Dissipation Ratings table ... 6
- Added Addition values for the DBV-5 option in the Dissipation Ratings table ... 6
- Deleted Note - Not tested in production, specified by design from $r_{DS(on)}$ in the Electrical Characteristics table ... 6
- Deleted Note - Not tested in production, specified by design from t_r in the Electrical Characteristics table ... 6
- Deleted Note - Not tested in production, specified by design from t_f in the Electrical Characteristics table ... 6
- Added text to the POWER DISSIPATION section - The thermal resistance, $R_{\theta JA}$ ... 24

5 概要 (続き)

出力負荷が電流制限スレッショルドを超えた場合、または短絡が存在する場合、デバイスは定電流モードに切り替えて過電流 ($\overline{OCx}$) ロジック出力を Low にすることで、出力電流を安全なレベルに制限します。連続的に大きな過負荷と短絡が発生すると、スイッチの電力散逸が増加し、接合部温度が上昇すると、熱保護回路によってスイッチがシャットオフされ、損傷を防止します。デバイスの温度が十分に低下すると、自動的にサーマル・シャットダウンからの回復が行われます。内部回路により、有効な入力電圧が印加されるまでスイッチがオフに維持されます。この配電スイッチは、電流制限を 1.5A (代表値) に設定するように設計されています。

6 Pin Configuration and Functions



† All Enable Inputs Are Active High For TPS2065, TPS2066, and TPS2067

表 6-1. Pin Functions (TPS2061 and TPS2065)

PINS					I/O	DESCRIPTION
	D or DGN Package		DBV Package			
NAME	TPS2061	TPS2065	TPS2061	TPS2065		
$\overline{EN}$	4	-	4	-	I	Enable input, logic low turns on power switch
EN	-	4	-	4	I	Enable input, logic high turns on power switch
GND	1	1	2	2		Ground
IN	2, 3	2,3	5	5	I	Input voltage
$\overline{OC}$	5	5	3	3	O	Overcurrent, open-drain output, active-low
OUT	6, 7, 8	6, 7, 8	1	1	O	Power-switch output
PowerPAD™	-	-	-	-		Internally connected to GND; used to heat-sink the part to the circuit board traces. Should be connected to GND pin.

表 6-2. Pin Functions (TPS2062 and TPS2066)

PINS			I/O	DESCRIPTION
NAME	NO.			
	TPS2062	TPS2066		
$\overline{EN1}$	3	-	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	-	I	Enable input, logic low turns on power switch IN-OUT2
EN1	-	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	-	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1		Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2
PowerPAD™	-	-		Internally connected to GND; used to heat-sink the part to the circuit board traces. Should be connected to GND pin.

表 6-3. Pin Functions (TPS2063 and TPS2067)

PINS			I/O	DESCRIPTION
NAME	TPS2063	TPS2067		
$\overline{EN1}$	3	–	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	–	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	–	I	Enable input, logic low turns on power switch IN2-OUT3
EN1	–	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	–	4	I	Enable input, logic high turns on power switch IN1-OUT2
EN3	–	7	I	Enable input, logic high turns on power switch IN2-OUT3
GND	1, 5	1, 5		Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3
NC	8, 9, 10	8, 9, 10		No connection
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Input voltage range, $V_{I(IN)}$ (2)		-0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (2), $V_{O(OUTx)}$		-0.3 V to 6 V
Input voltage range, $V_{I(\overline{EN})}$, $V_{I(EN)}$, $V_{I(\overline{ENx})}$, $V_{I(ENx)}$		-0.3 V to 6 V
Voltage range, $V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$		-0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$		Internally limited
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		-40°C to 150°C
Electrostatic discharge (ESD) protection	Human body model	2 kV
	Charge device model (CDM)	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

7.2 Dissipating Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D-8(3)	585.82 mW	5.8582 mW/°C	322.20 mW	234.32 mW
DGN-8(2)	1712.3 mW	17.123 mW/°C	941.78 mW	684.33 mW
D-16(3)	898.47 mW	8.9847 mW/°C	494.15 mW	359.38 mW
DBV-5(1)	285 mW	2.85 mW/°C	155 mW	114 mW
	704 mW	7.04 mW/°C	387 mW	281 mW

(1) Lower ratings are for low-k printed circuit board layout (single -sided). Higher ratings are for enhanced high-k layout, (2 signal, 2 plane) with a 1mm^2 copper pad on pin 2 and 2 vias to the ground plane.
(2) Power ratings are based on the high-k board (2 signal, 2 plane) with PowerPAD™ vias to the internal ground plane.
(3) Power ratings are based on the low-k board (1 signal, 1 layer).

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$	2.7	5.5	V
Input voltage, $V_{I(\overline{EN})}$, $V_{I(EN)}$, $V_{I(\overline{ENx})}$, $V_{I(ENx)}$	0	5.5	V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$	0	1	A
Operating virtual junction temperature, T_J	-40	125	°C

7.4 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 1 A, -40°C ≤ T_J ≤ 125°C	D and DGN packages		70	135	mΩ
			DBV package		95	140	
	Static drain-source on-state resistance, 2.7-V operation	$V_{I(IN)}$ = 2.7 V, I_O = 1 A, -40°C ≤ T_J ≤ 125°C	D and DGN packages		75	150	mΩ

7.4 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V	C_L = 1 µF, R_L = 5 Ω, T_J = 25°C			0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V				0.4	1	
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V			0.05		0.5	
		$V_{I(IN)}$ = 2.7 V			0.05		0.5	
ENABLE INPUT $\overline{EN}$ OR EN								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V			2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V					0.8	
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V or 5.5 V, $V_{I(ENx)}$ = 0 V or 5.5 V			-0.5		0.5	µA
t_{on}	Turnon time	C_L = 100 µF, R_L = 5 Ω					3	ms
t_{off}	Turnoff time	C_L = 100 µF, R_L = 5 Ω					10	
CURRENT LIMIT								
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit		T_J = 25°C	1.1	1.5	1.9	A
				-40°C ≤ T_J ≤ 125°C	1.1	1.5	2.1	
I_{OC_TRIP} [2]	Overcurrent trip threshold	$V_{I(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT	TPS2061 TPS2062 TPS2065 (D and DGN package only) TPS2066		1.6	2.3	2.7	A
			TPS2063, TPS2067		1.6	2.4	3.0	
SUPPLY CURRENT (TPS2061, TPS2065)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	1	µA
				-40°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	TPS2061 TPS2065 (D and DGN packages only)	T_J = 25°C		43	60	µA
				-40°C ≤ T_J ≤ 125°C		43	70	
			TPS2065DBV	T_J = 25°C		75	95	
				-40°C ≤ T_J ≤ 125°C		75	95	
Leakage current		OUT connected to ground, $V_{I(\overline{EN})}$ = 5.5 V, or $V_{I(EN)}$ = 0 V		-40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground		T_J = 25°C		0		µA
SUPPLY CURRENT (TPS2062, TPS2066)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	1	µA
				-40°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		50	70	µA
				-40°C ≤ T_J ≤ 125°C		50	90	
Leakage current		OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		-40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground		T_J = 25°C		0.2		µA
SUPPLY CURRENT (TPS2063, TPS2067)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V		T_J = 25°C		0.5	2	µA
				-40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V		T_J = 25°C		65	90	µA
				-40°C ≤ T_J ≤ 125°C		65	110	
Leakage current		OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		-40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, INx = ground		T_J = 25°C		0.2		µA
UNDERVOLTAGE LOCKOUT (All Devices excluding TPS2065DBV)								
Low-level input voltage, IN					2		2.5	V
Hysteresis, IN		T_J = 25°C				75		mV
UNDERVOLTAGE LOCKOUT (TPS2065DBV)								

7.4 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
Low-level input voltage, IN		2		2.6	V
Hysteresis, IN	T_J = 25°C		75		mV
OVERCURRENT $\overline{OC1}$ and $\overline{OC2}$					
Output low voltage, $V_{OL(OCx)}$	$I_{O(\overline{OCx})}$ = 5 mA			0.4	V
Off-state current	$V_{O(\overline{OCx})}$ = 5 V or 3.3 V			1	µA
$\overline{OC}$ deglitch	$\overline{OCx}$ assertion or deassertion	4	8	15	ms
THERMAL SHUTDOWN(3)					
Thermal shutdown threshold		135			°C
Recovery from thermal shutdown		125			°C
Hysteresis			10		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) TPS2065DBV doesn't have overcurrent trip threshold. Current will be limited to I_{OS} under different test conditon. Check セクション 9.7 for more details.
(3) The thermal shutdown only reacts under overcurrent conditions.

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV)

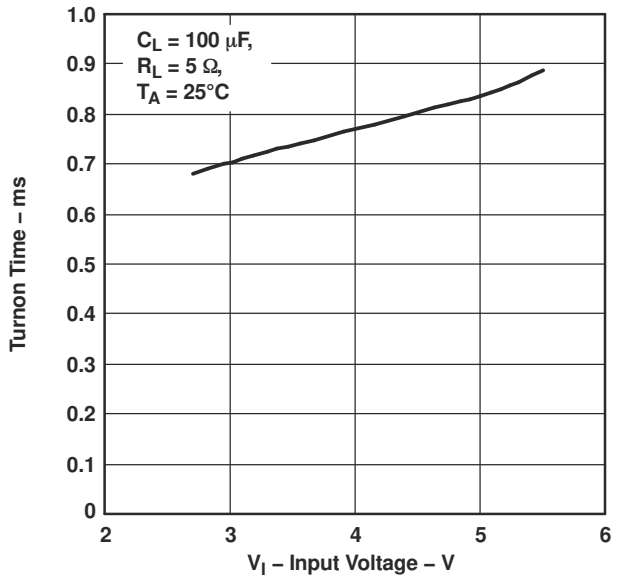


図 7-1. TURNON TIME vs INPUT VOLTAGE

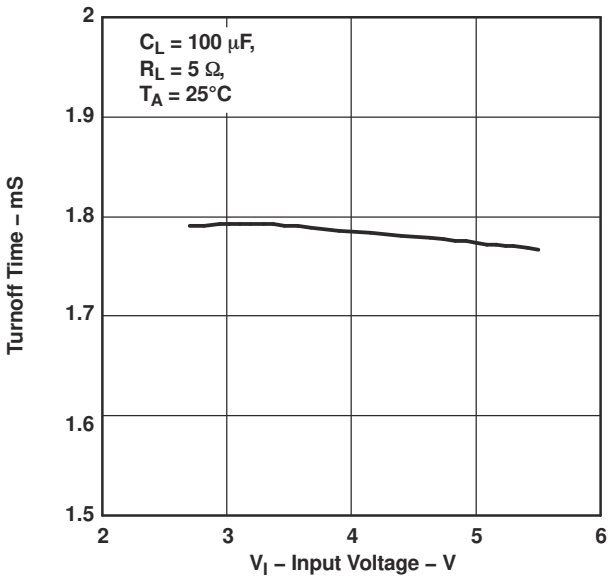


図 7-2. TURNOFF TIME vs INPUT VOLTAGE

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV) (continued)

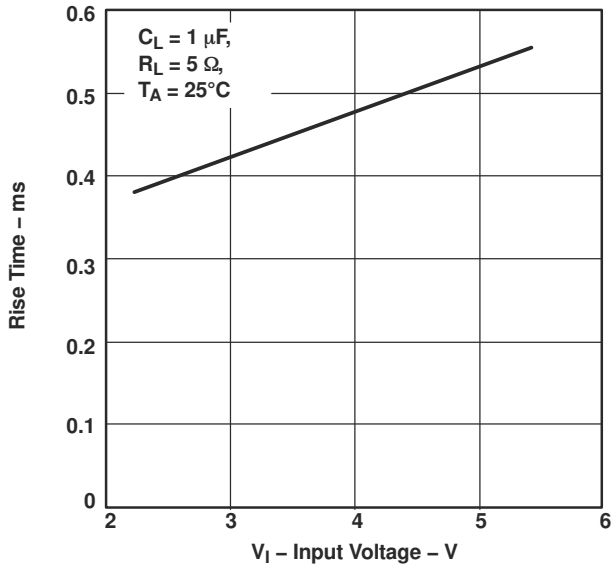


図 7-3. RISE TIME vs INPUT VOLTAGE

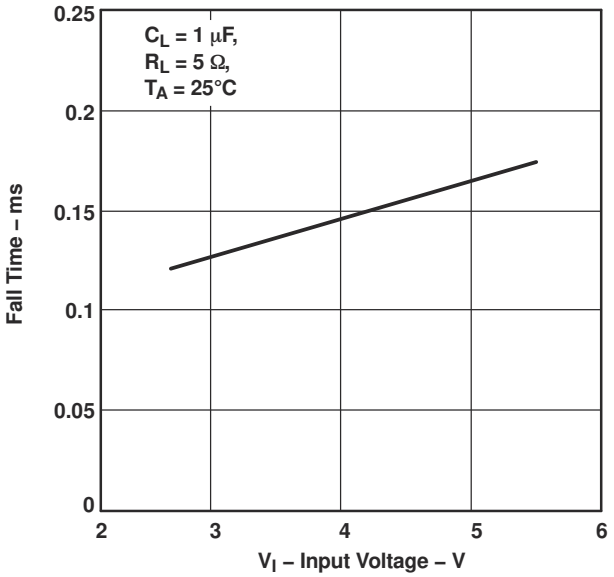


図 7-4. FALL TIME vs INPUT VOLTAGE

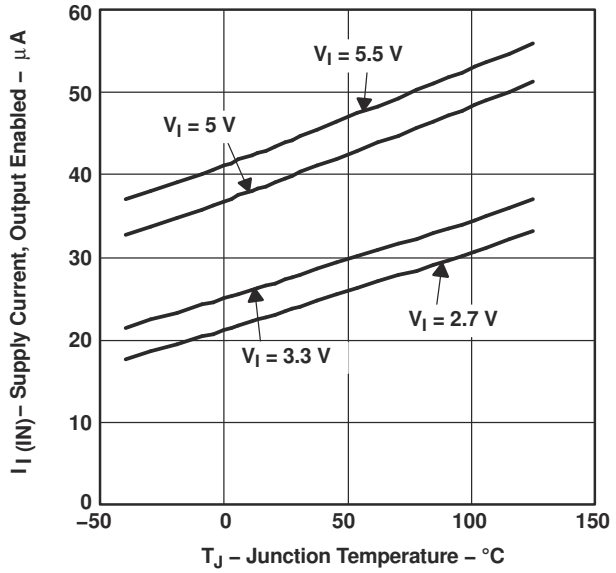


図 7-5. TPS2061, TPS2065 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

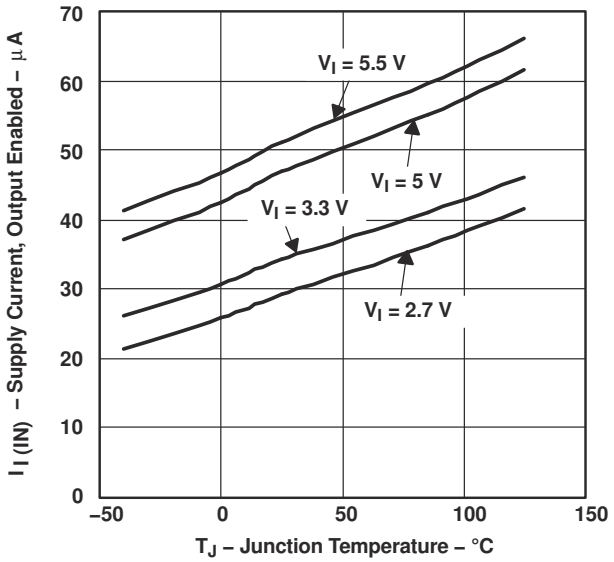


図 7-6. TPS2062, TPS2066 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV) (continued)

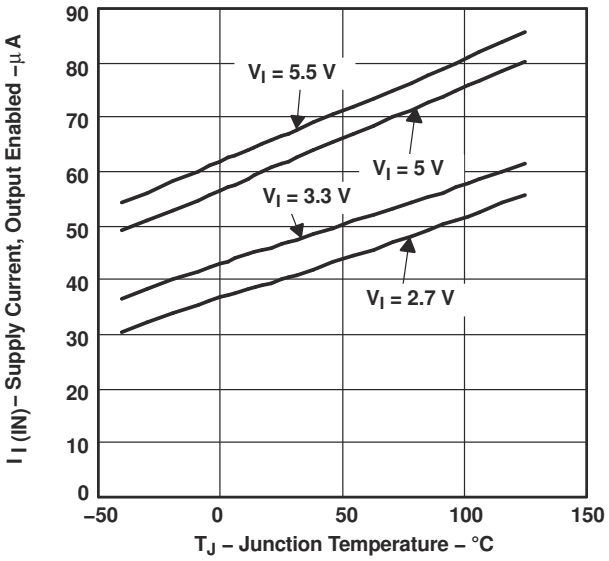


図 7-7. TPS2063, TPS2067 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

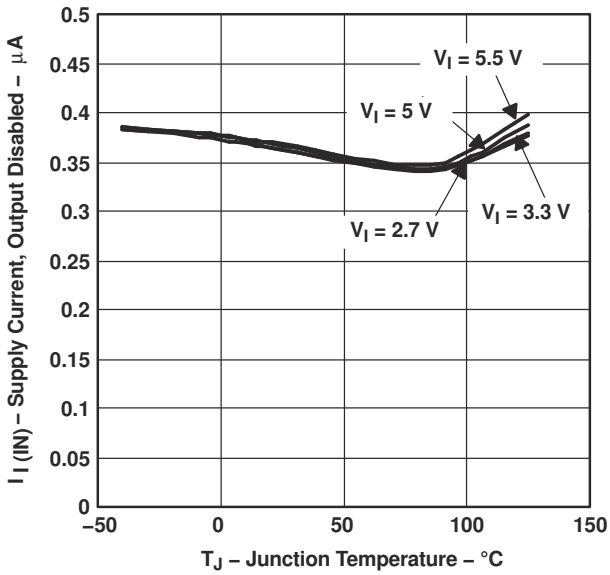


図 7-8. TPS2061, TPS2065 SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

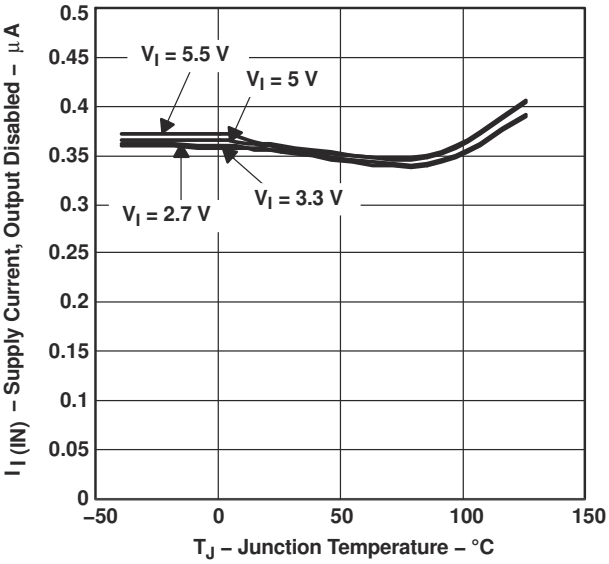


図 7-9. TPS2062, TPS2066 SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

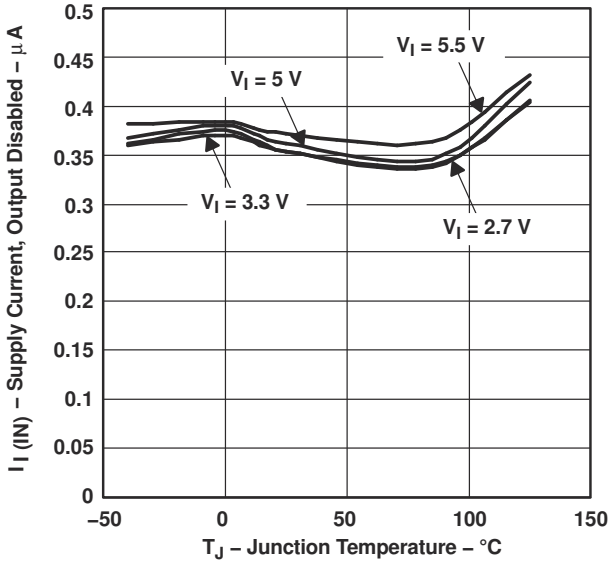


図 7-10. TPS2063, TPS2067 SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV) (continued)

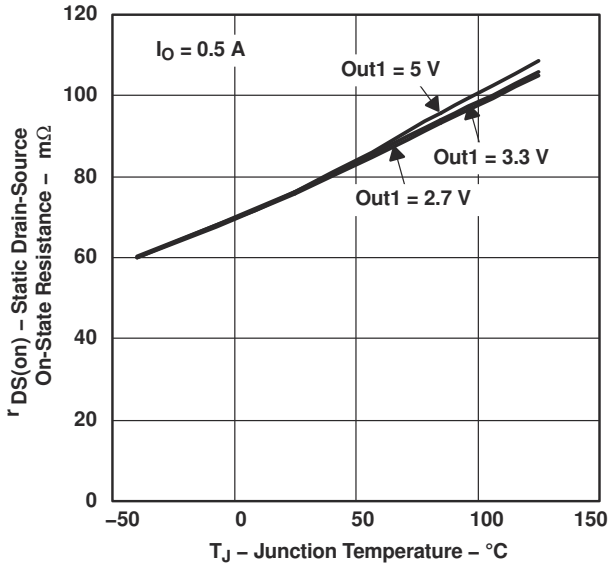


図 7-11. STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

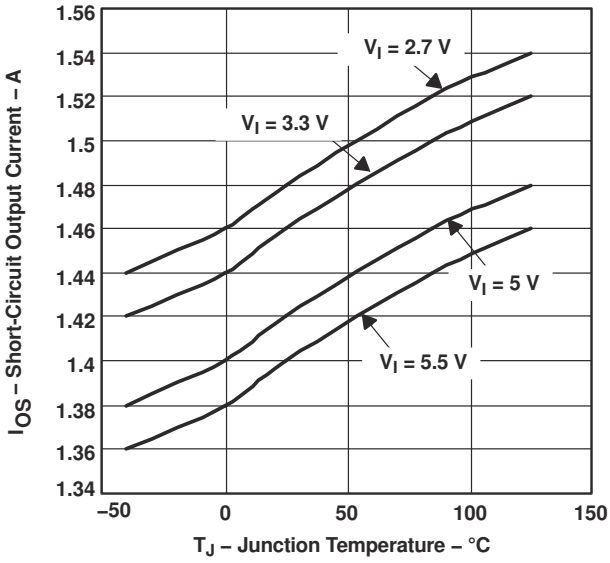


図 7-12. SHORT-CIRCUIT OUTPUT CURRENT vsJUNCTION TEMPERATURE

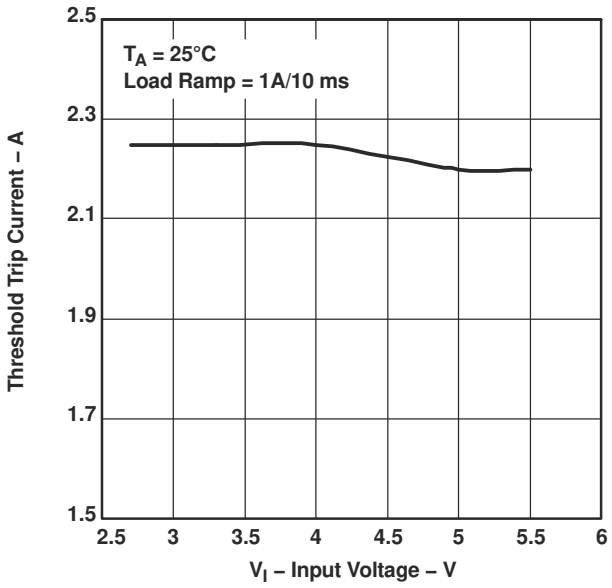


図 7-13. THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

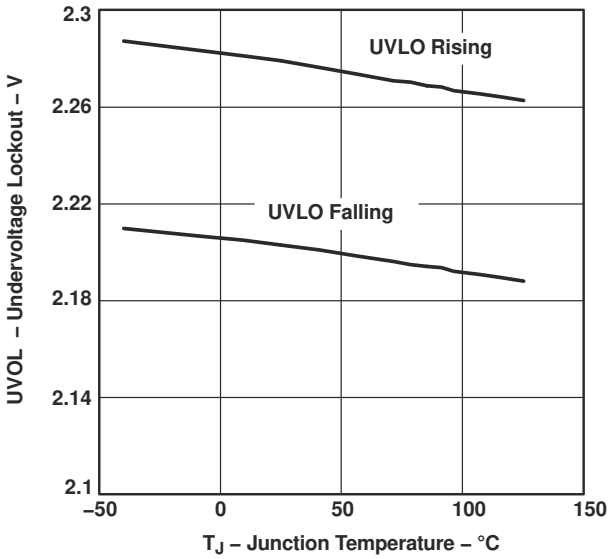


図 7-14. UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV)

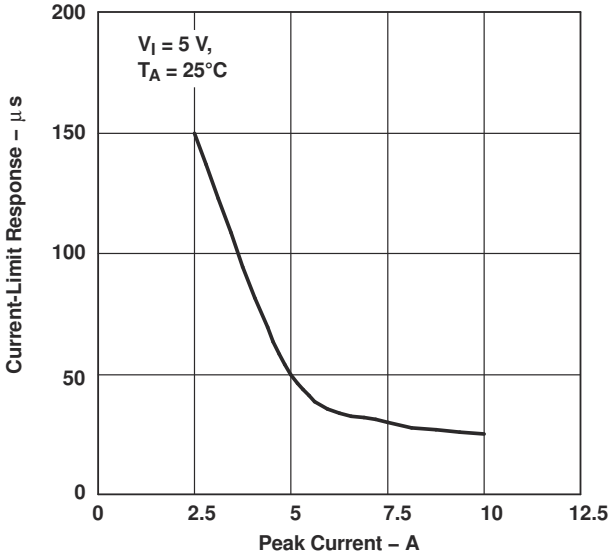


図 7-15. CURRENT-LIMIT RESPONSE vs PEAK CURRENT

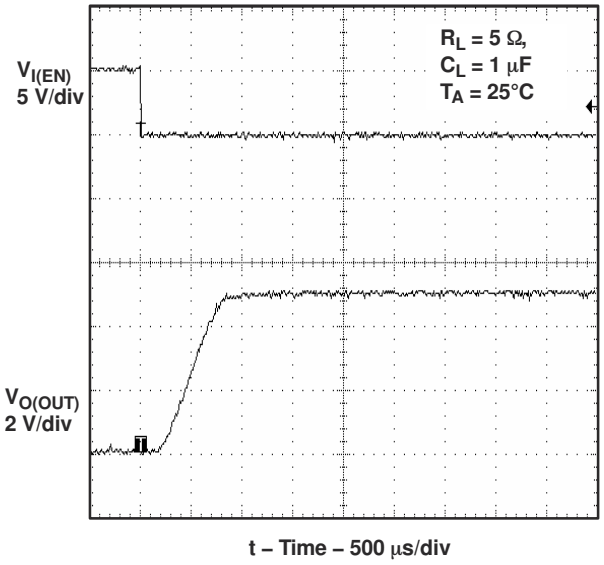


図 7-16. Turnon Delay and Rise Time With 1-µF Load

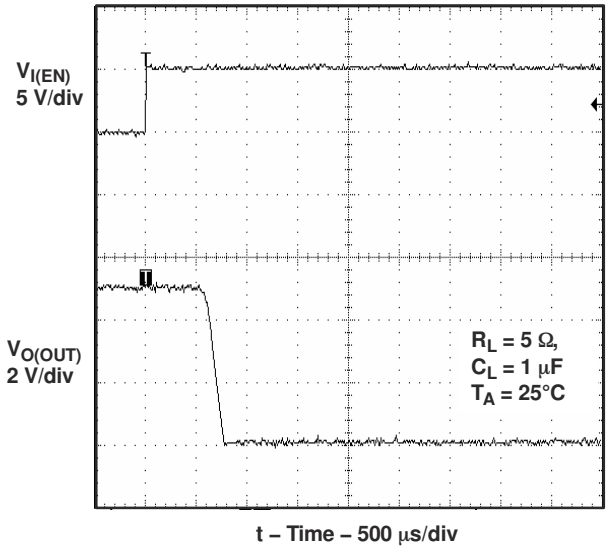


図 7-17. Turnoff Delay and Fall Time With 1-µF Load

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV) (continued)

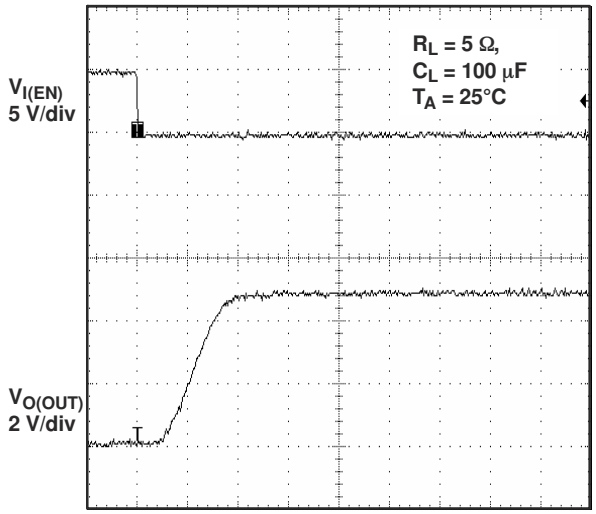


図 7-18. Turnon Delay and Rise Time With 100-µF Load

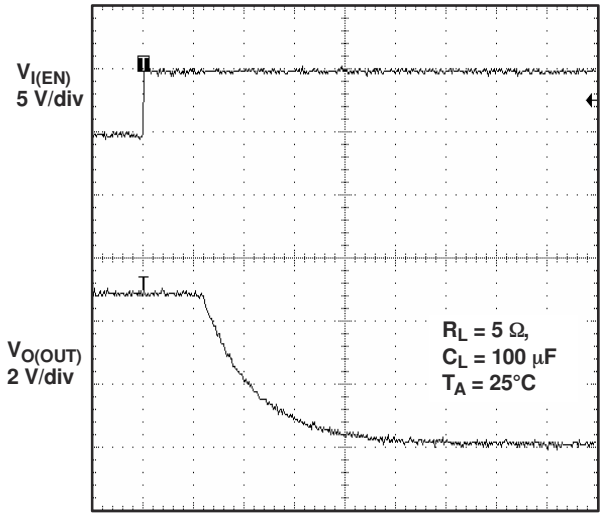


図 7-19. Turnoff Delay and Fall Time With 100-µF Load

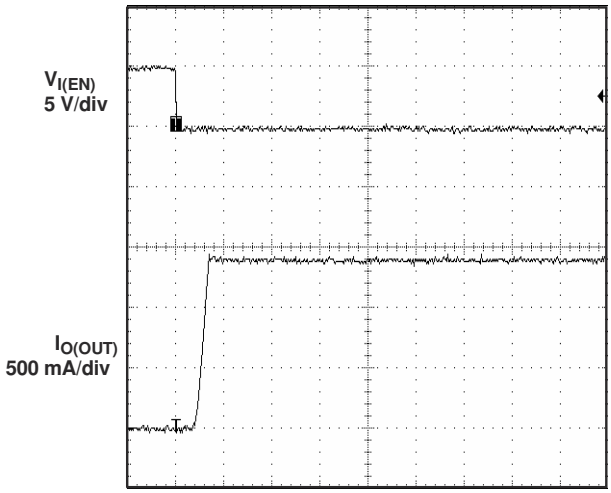


図 7-20. Short-Circuit Current, Device Enabled Into Short

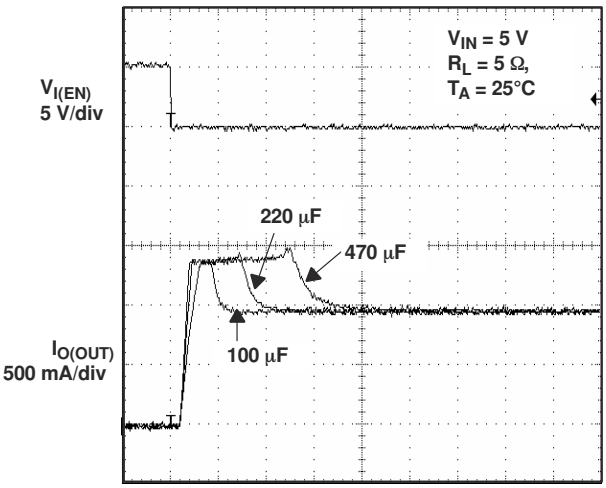


図 7-21. Inrush Current With Different Load Capacitance

7.5 Typical Characteristics(All Devices Excluding TPS2065DBV) (continued)

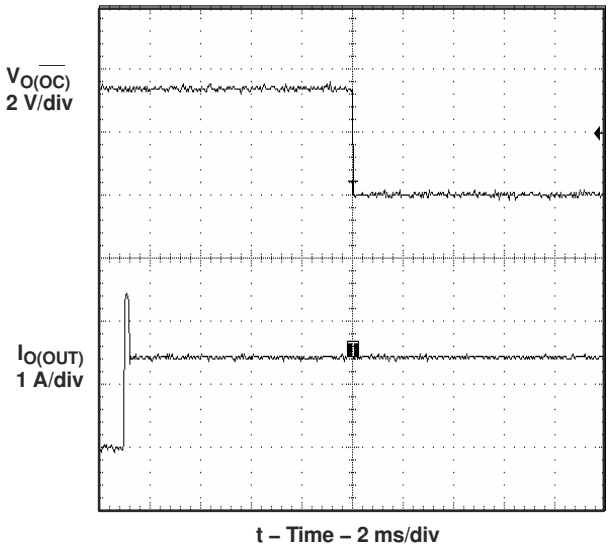


図 7-22. 2-Ω Load Connected to Enabled Device

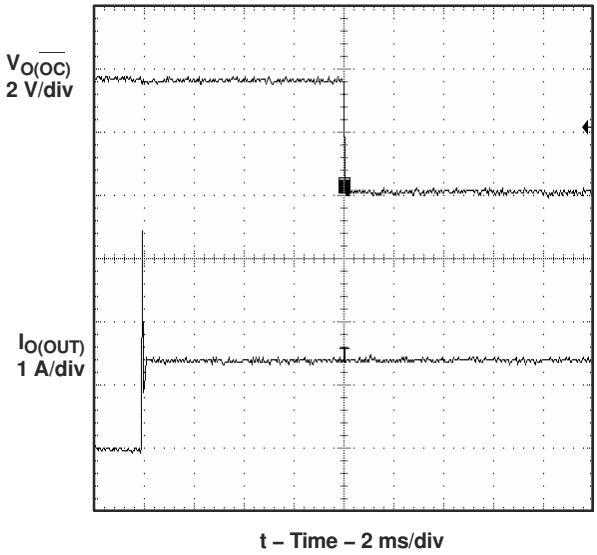


図 7-23. 1-Ω Load Connected to Enabled Device

7.6 Typical Characteristics (TPS2065DBV)

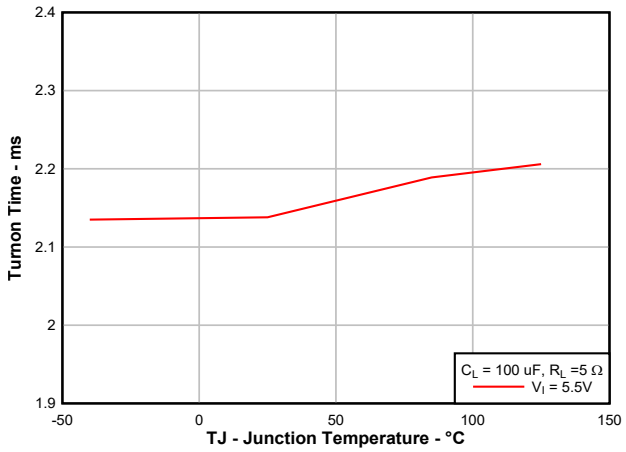


図 7-24. Turnon Time vs Junction Temperature

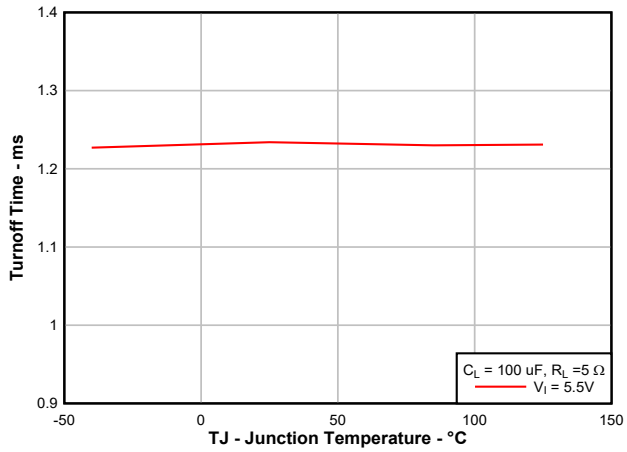


図 7-25. Turnoff Time vs Input Voltage

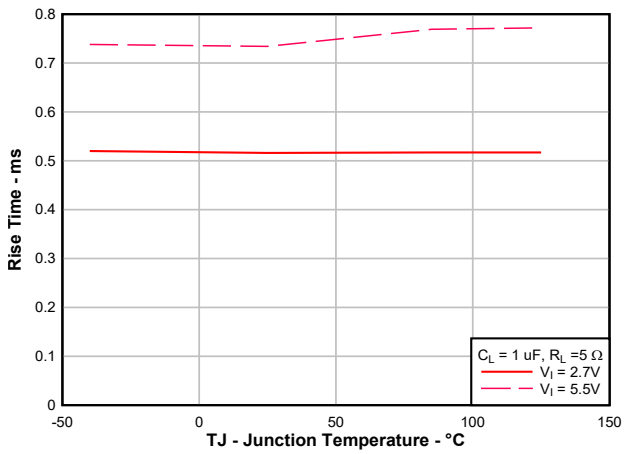


図 7-26. Rise Time vs Input Voltage

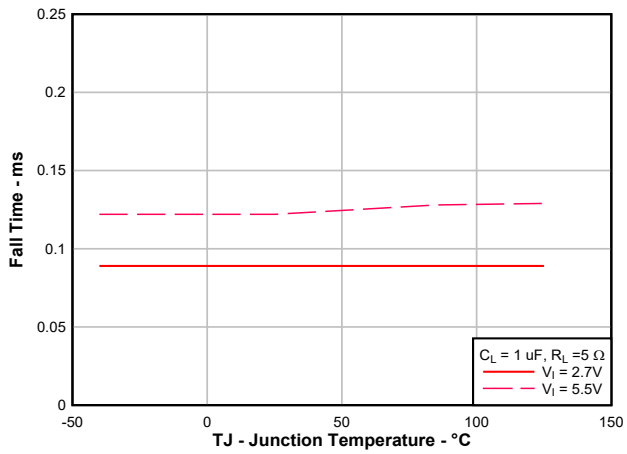


図 7-27. Fall Time vs Input Voltage

7.6 Typical Characteristics (TPS2065DBV) (continued)

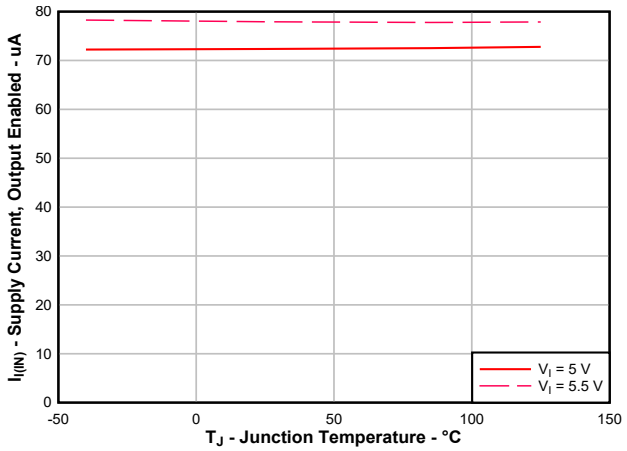


図 7-28. TPS2065DBV Supply Current, Output Enabled vs Junction Temperature

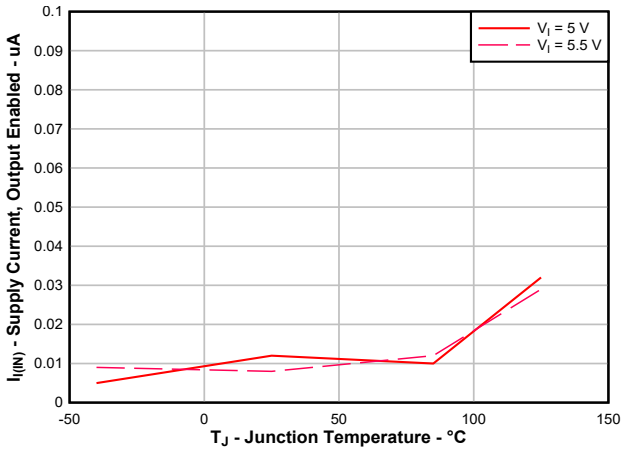


図 7-29. TPS2065DBV Supply Current, Output Disabled vs Junction Temperature

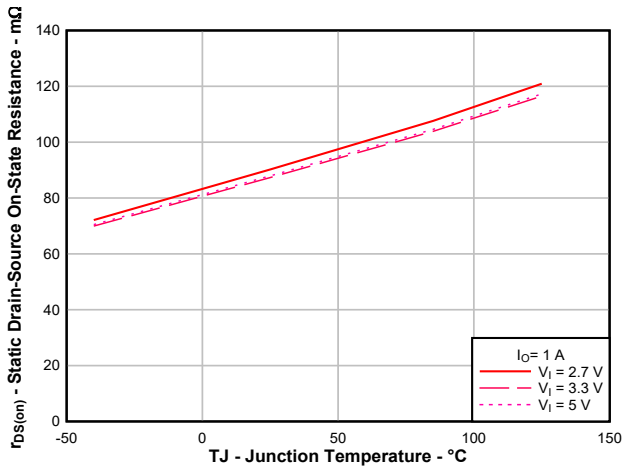


図 7-30. DBV Package Static Drain-Source on-State Resistance vs Junction Temperature

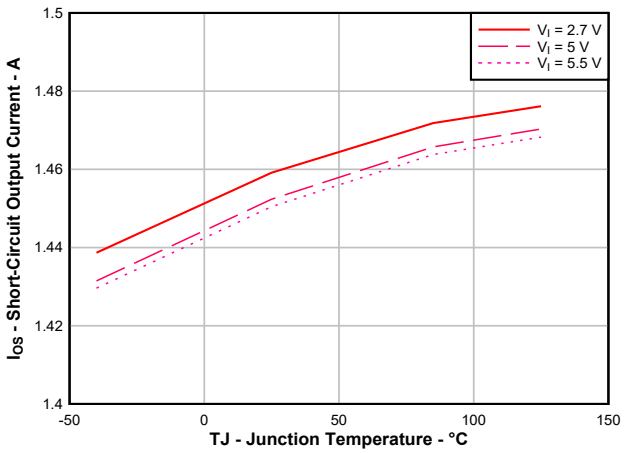


図 7-31. Short-Circuit Output Current vs Junction Temperature

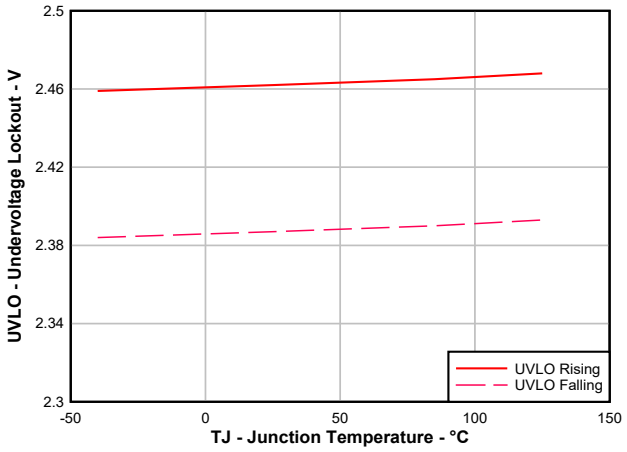


図 7-32. Undervoltage Lockout vs Junction Temperature

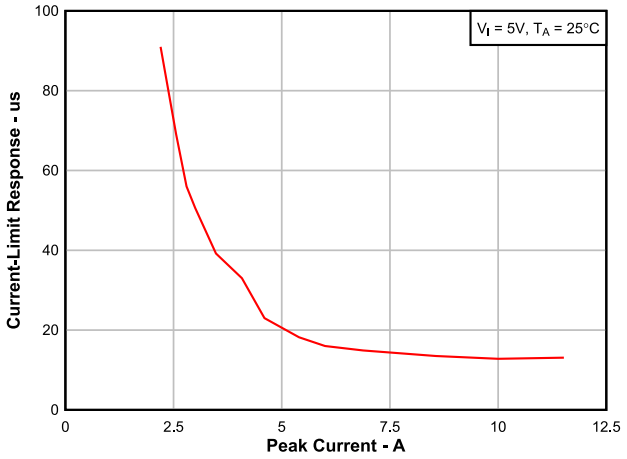


図 7-33. Current-Limit Response vs Peak Current

7.6 Typical Characteristics (TPS2065DBV) (continued)

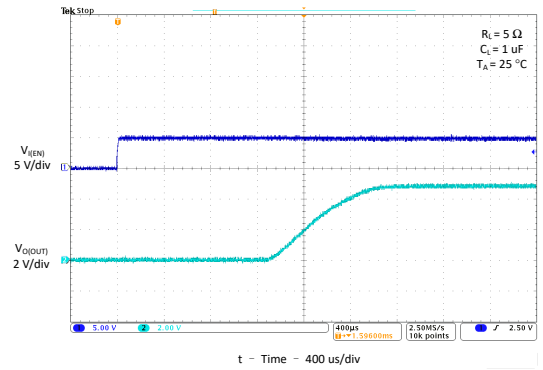


図 7-34. Turnon Delay and Rise Time With 1-µF Load

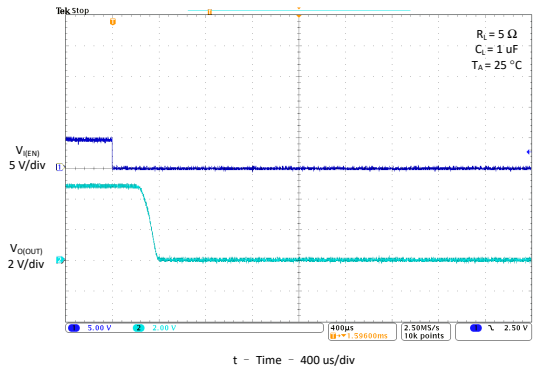


図 7-35. Turnoff Delay and Fall Time With 1-µF Load

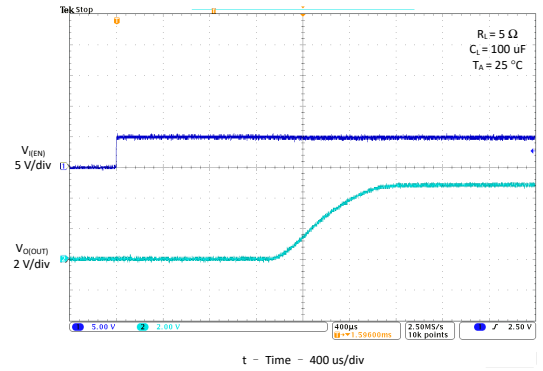


図 7-36. Turnon Delay and Rise Time With 100-µF Load

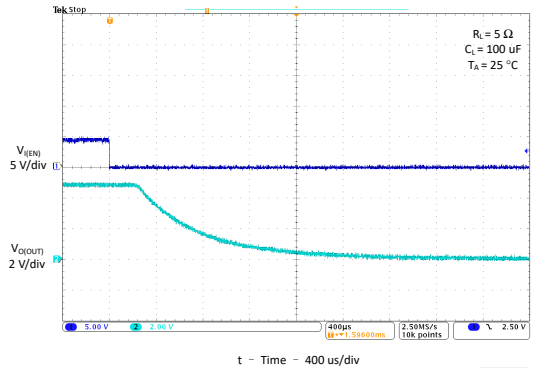


図 7-37. Turnoff Delay and Fall Time With 100-µF Load

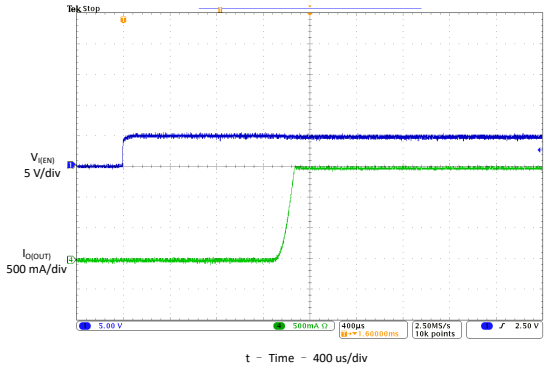


図 7-38. Short-Circuit Current, Device Enabled Into Short

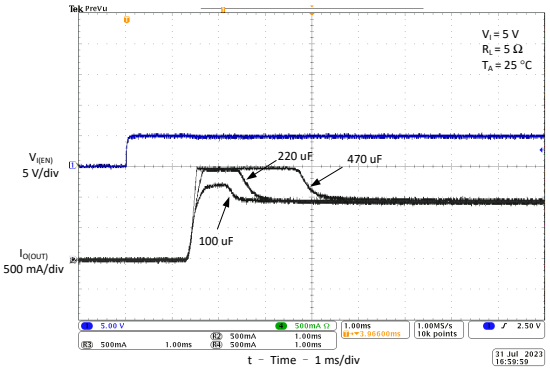


図 7-39. Inrush Current With Different Load Capacitance

7.6 Typical Characteristics (TPS2065DBV) (continued)

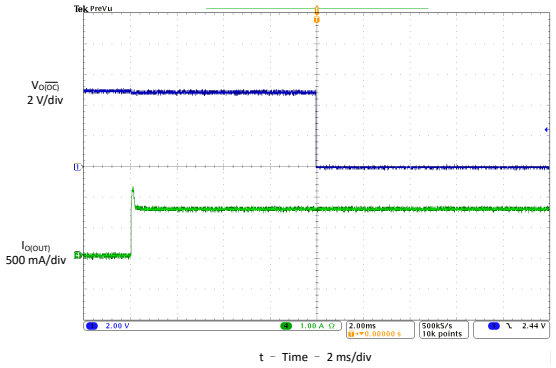


図 7-40. 3-Ω Load Connected to Enabled Device

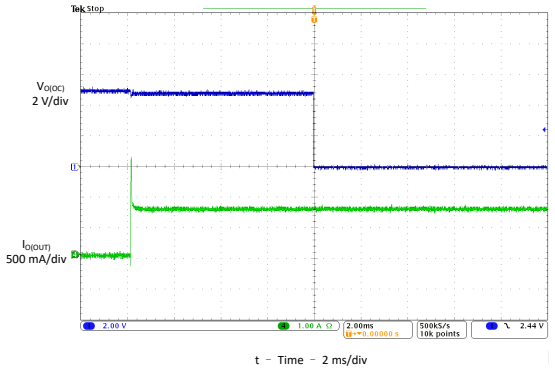


図 7-41. 2-Ω Load Connected to Enabled Device

8 Parameter Measurement Information

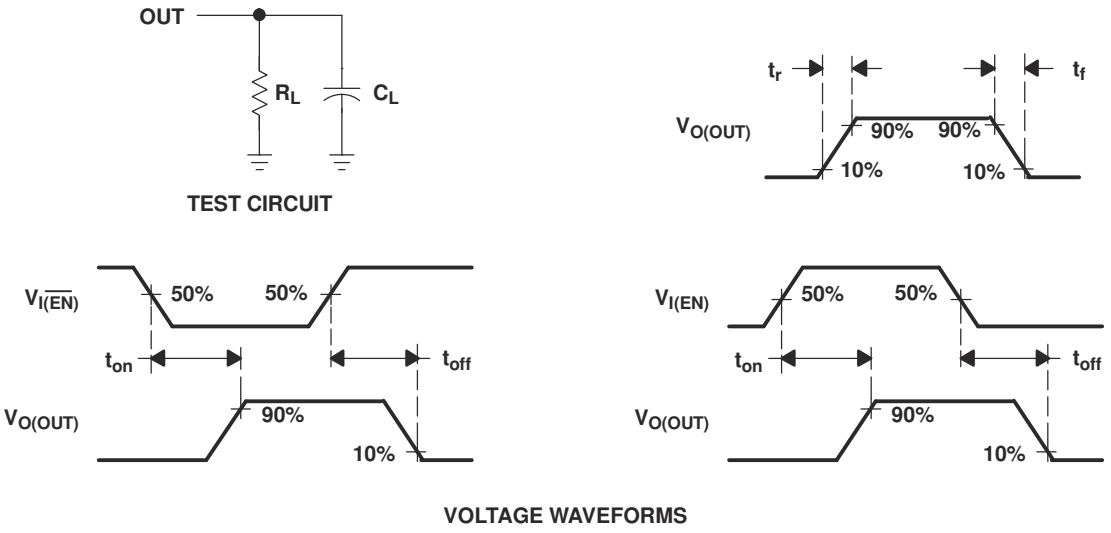
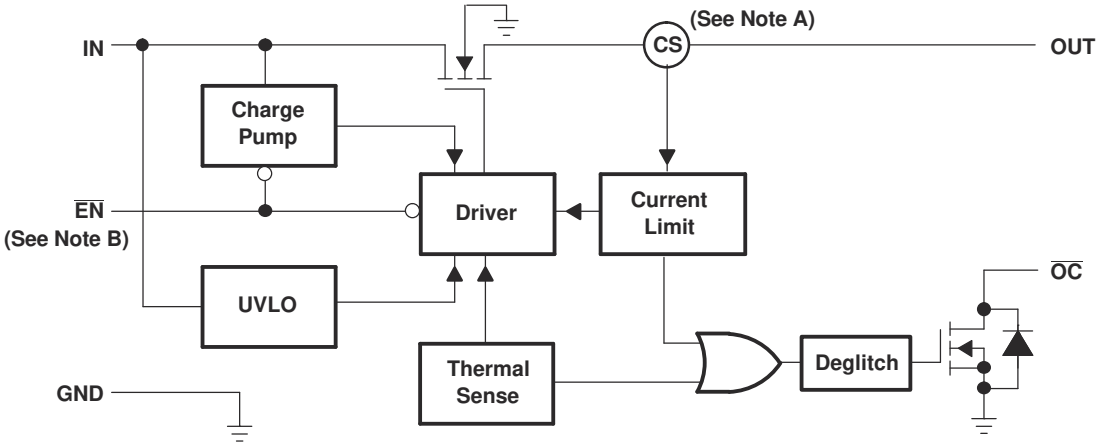


図 8-1. Test Circuit and Voltage Waveforms

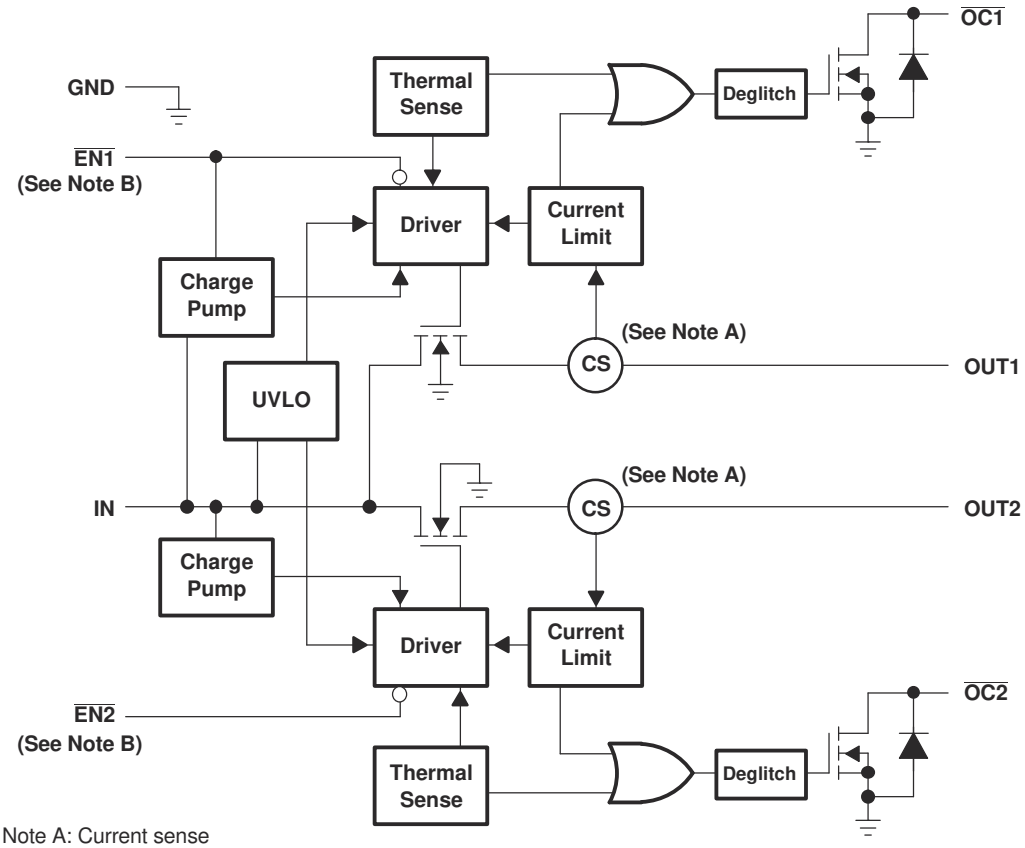
9 Detailed Description

9.1 Functional Block Diagram



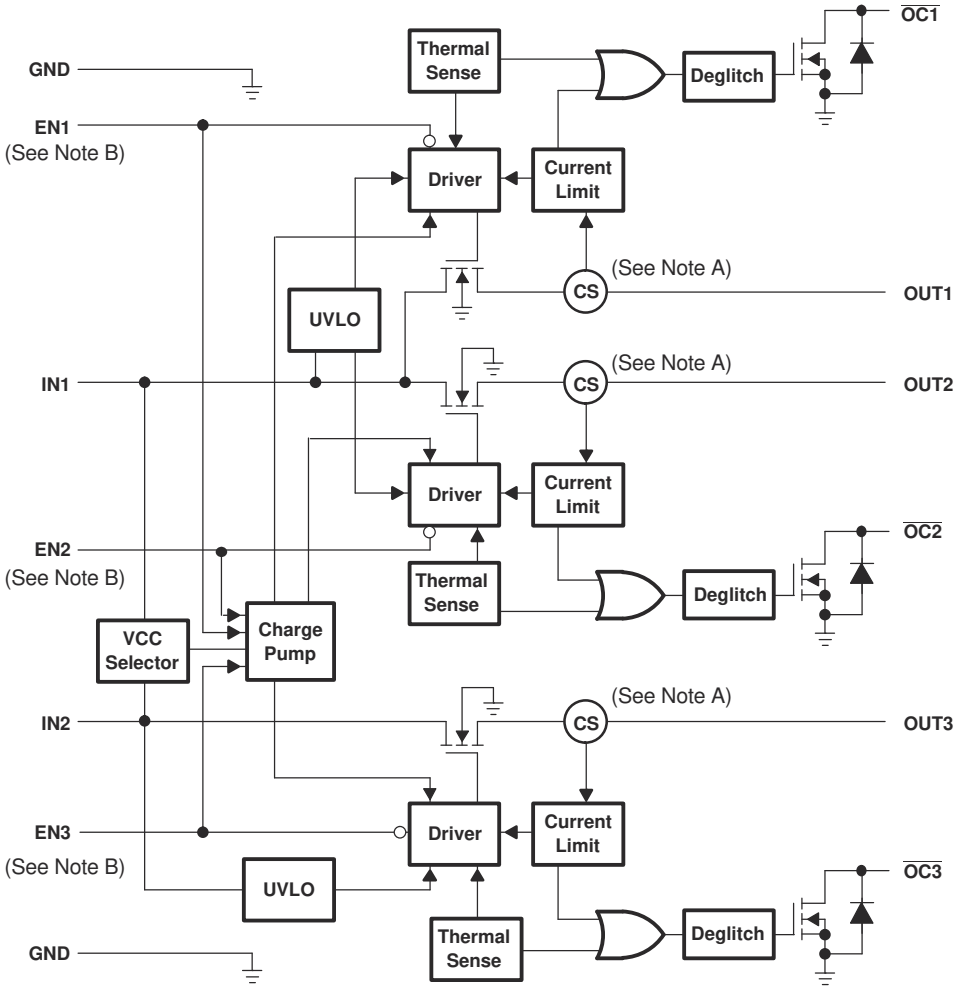
Note A: Current sense
Note B: Active low ($\overline{EN}$) for TPS2061. Active high (EN) for TPS2065.

図 9-1. TPS2061 and TPS2065



Note A: Current sense
Note B: Active low ($\overline{ENx}$) for TPS2062. Active high (ENx) for TPS2066.

図 9-2. TPS2062 and TPS2066



Note A: Current sense

Note B: Active low ($\overline{ENx}$) for TPS2063; Active high (ENx) for TPS2067

図 9-3. TPS2063 and TPS2067

9.2 Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1 A.

9.3 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

9.4 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

9.5 Enable ($\overline{ENx}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{ENx}$,

or when a logic low is present on ENx. A logic zero input on $\overline{ENx}$, or a logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

9.6 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

9.7 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

There are two kinds of current limit profiles for the TPS20xx family of devices.

All devices (excluding TPS2065DBV) have an output I vs V characteristic similar to the plot labeled **Current Limit with Peaking** in 図 9-4. This type of limiting can be characterized by two parameters, the overcurrent trip threshold (I_{OC}), and the short-circuit output current threshold (I_{OS}).

Devices TPS2065DBV have an output I vs V characteristic similar to the plot labeled **Flat Current Limit** in 図 9-4. This type of limiting can be characterized by one parameters, the short circuit current (I_{OS}).

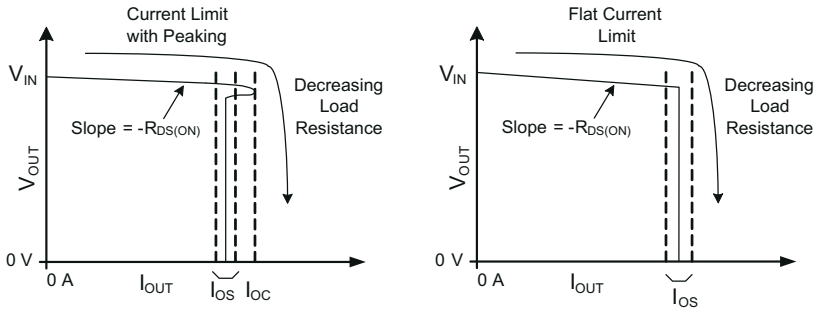


図 9-4. Current Limit Profiles

9.7.1 Overcurrent Conditions (All Devices Excluding TPS2065DBV)

Three possible overload conditions can occur for all devices exclude TPS2065DBV. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see 図 7-20 through 図 7-22). The TPS20xx senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold (I_{OC})), the device switches into constant-current mode and current is limited at the short-circuit output current threshold (I_{OS}).

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the overcurrent trip threshold (I_{OC}) is reached or until the thermal limit of the device is exceeded. The TPS20xxB is capable of delivering current up to the current-limit threshold without damaging the device. Once the overcurrent trip threshold (I_{OC}) has been reached, the device switches into its constant-current mode current is limited at the short-circuit output current threshold (I_{OS}).

9.7.2 Overcurrent Conditions (TPS2065DBV)

Three possible overload conditions can occur for TPS2065DBV. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see 図 7-38 through 図 7-41). The TPS20xx senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the short-circuit output current threshold (I_{OS}) is reached, the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. After the short-circuit output current threshold (I_{OS}) is reached, the device switches into constant-current mode.

9.8 Overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

9.9 Thermal Sense

The TPS206x implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

9.10 Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

10.1.1 Power-supply Considerations

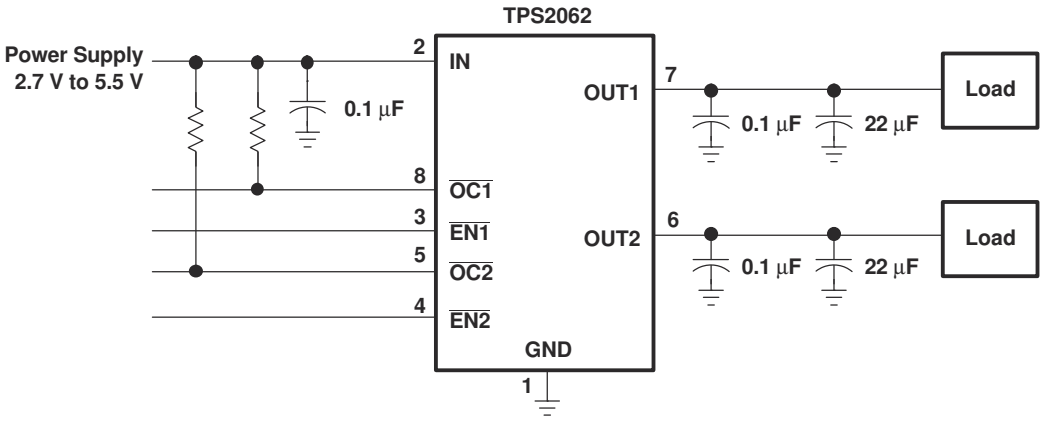


図 10-1. Typical Application

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

10.1.2 $\overline{OC}$ Response

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{OCx}$ occurs due to the 10-ms deglitch circuit. The TPS206x is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{OCx}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

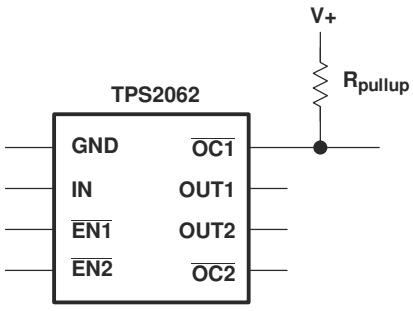


図 10-2. Typical Circuit for the $\overline{OC}$ Pin

10.1.3 Power Dissipation and Junction Temperature

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from 図 7-11. Using this value, the power dissipation per switch can be calculated by:

- $P_D = r_{DS(on)} \times I^2$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

The thermal resistance, $R_{\theta JA}$ = 1 / (DERATING FACTOR), where DERATING FACTOR is obtained from the Dissipation Ratings Table. Thermal resistance is a strong function of the printed circuit board construction , and the copper trace area connecting the integrated circuit.

Finally, calculate the junction temperature:

- $T_J = P_D \times R_{\theta JA} + T_A$

Where:

- T_A= Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

10.1.4 Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS206x implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises above a minimum of 135°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

10.1.5 Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

10.1.6 Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS206x has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

10.1.7 Host/Self-Powered and Bus-powered Hubs

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see 図 10-3). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

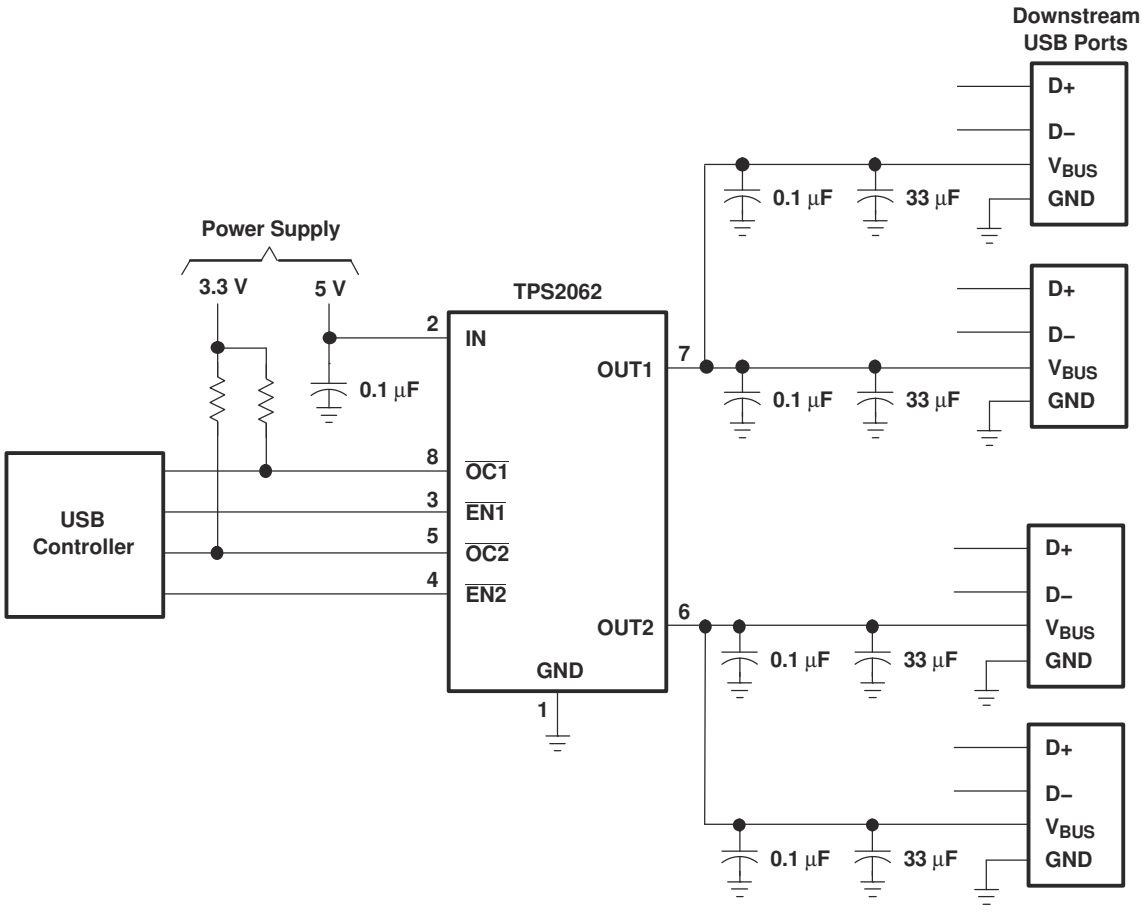


図 10-3. Typical Four-Port USB Host / Self-Powered Hub

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

10.1.8 Low-power Bus-powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see 図 10-4). With TPS206x, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.

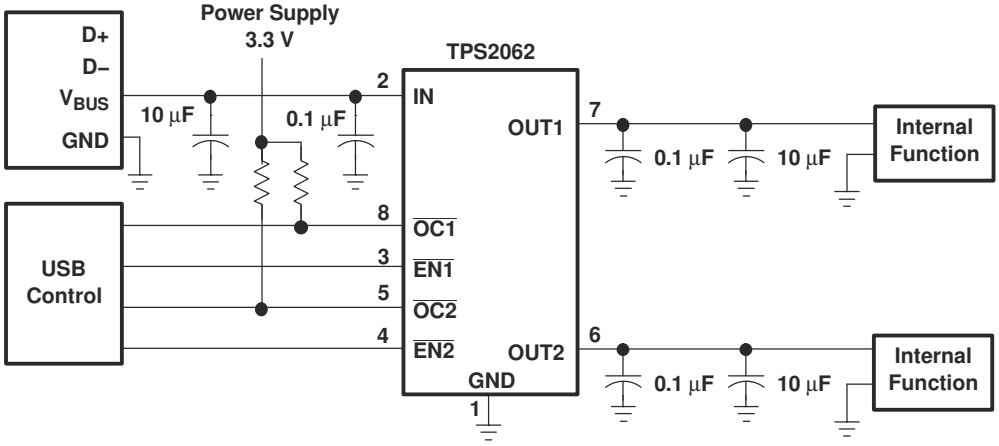


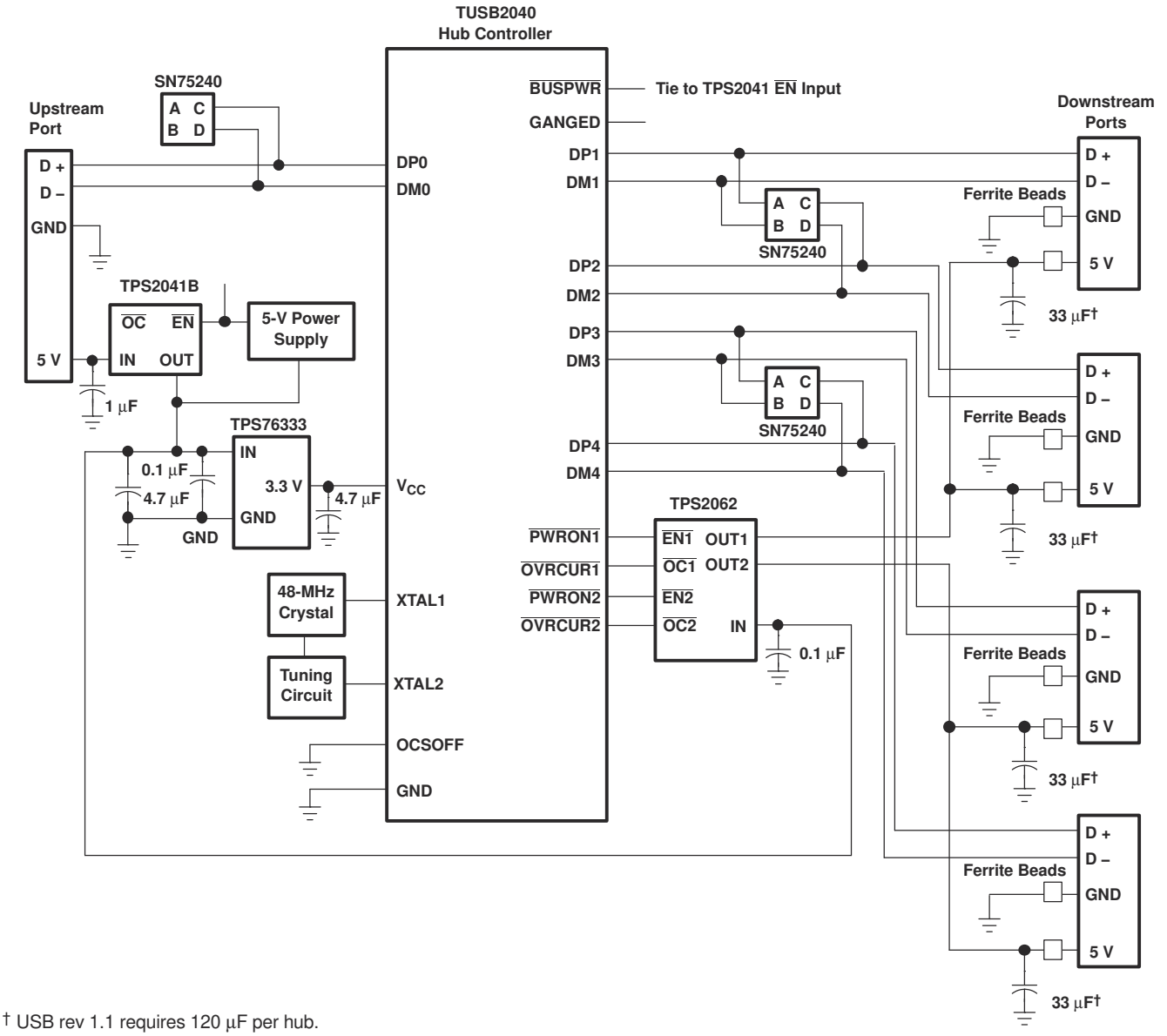
図 10-4. High-Power Bus-Powered Function

10.1.9 USB Power-distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS206x allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see 図 10-5).



† USB rev 1.1 requires 120 µF per hub.

図 10-5. Hybrid Self / Bus-Powered Hub Implementation

10.1.10 Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS206x, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS206x also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

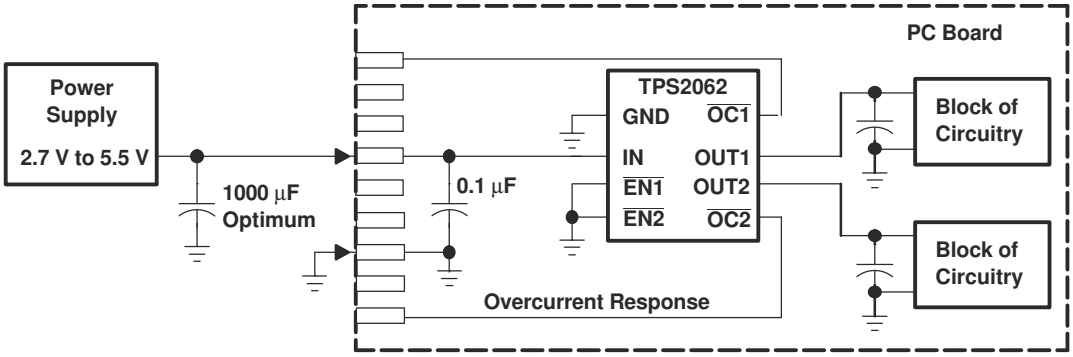


図 10-6. Typical Hot-Plug Implementation

By placing the TPS206x between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.2 Documentation Support

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

11.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2061D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2061	Samples
TPS2061DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	2061	Samples
TPS2061DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	2061	Samples
TPS2061DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2061	Samples
TPS2061DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2061	Samples
TPS2061DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2061	Samples
TPS2061DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2061	Samples
TPS2061DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2061	Samples
TPS2062D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062	Samples
TPS2062DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062	Samples
TPS2062DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2062	Samples
TPS2062DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062	Samples
TPS2062DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2062	Samples
TPS2062DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062	Samples
TPS2062DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062	Samples
TPS2063D	ACTIVE	SOIC	D	16	40	TBD	Call TI	Call TI	-40 to 125	2063	Samples
TPS2063DR	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125	2063	Samples
TPS2063DRG4	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 125	2063	Samples
TPS2065D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2065	Samples
TPS2065DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2065	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2065DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2065	Samples
TPS2065DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2065	Samples
TPS2065DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2065	Samples
TPS2065DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2065	Samples
TPS2066D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2066DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2066DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2066DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2066DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2066DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2066DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066	Samples
TPS2067D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2067	Samples
TPS2067DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2067	Samples
TPS2067DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2067	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS2062, TPS2065, TPS2066 :

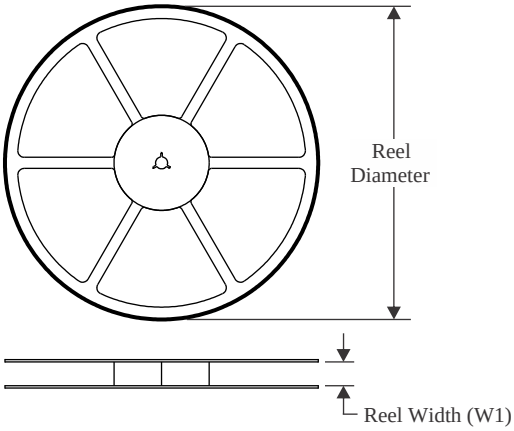
- Automotive : TPS2062-Q1, TPS2065-Q1, TPS2066-Q1

NOTE: Qualified Version Definitions:

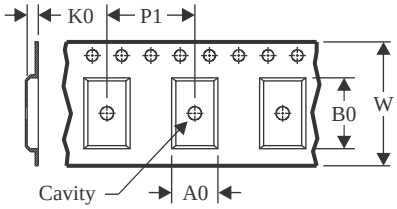
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

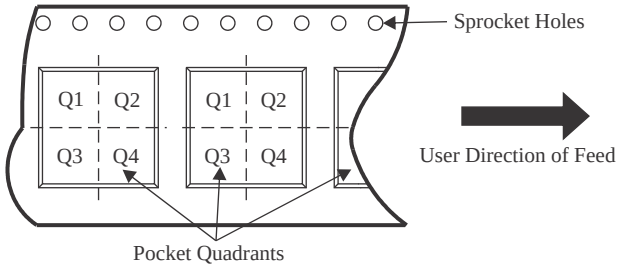


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

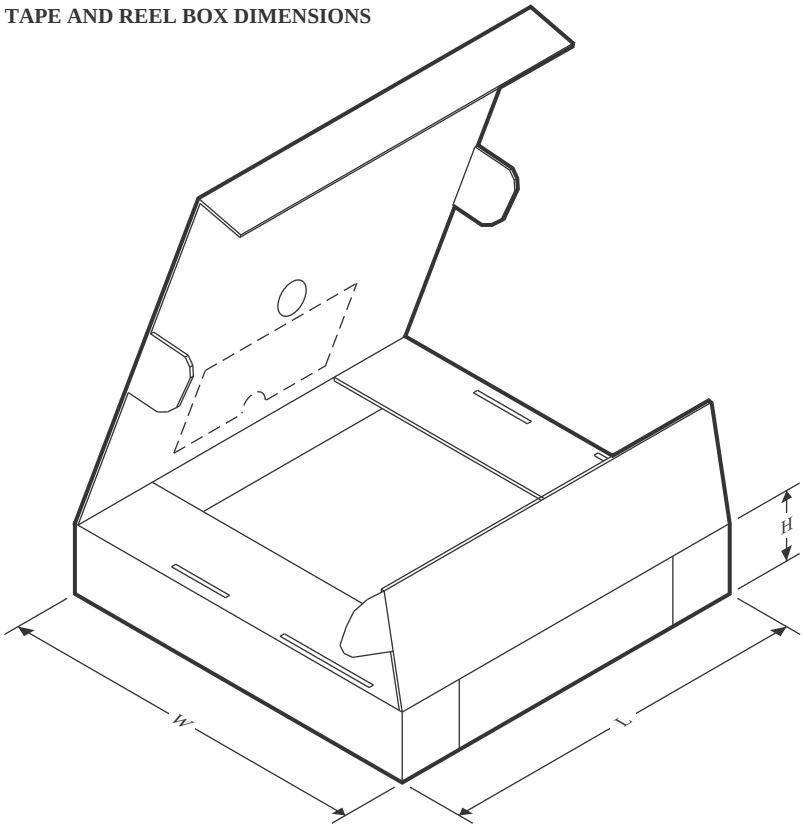
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2061DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2061DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2061DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2062DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2062DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2065DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS2065DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2065DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2066DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2066DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2067DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

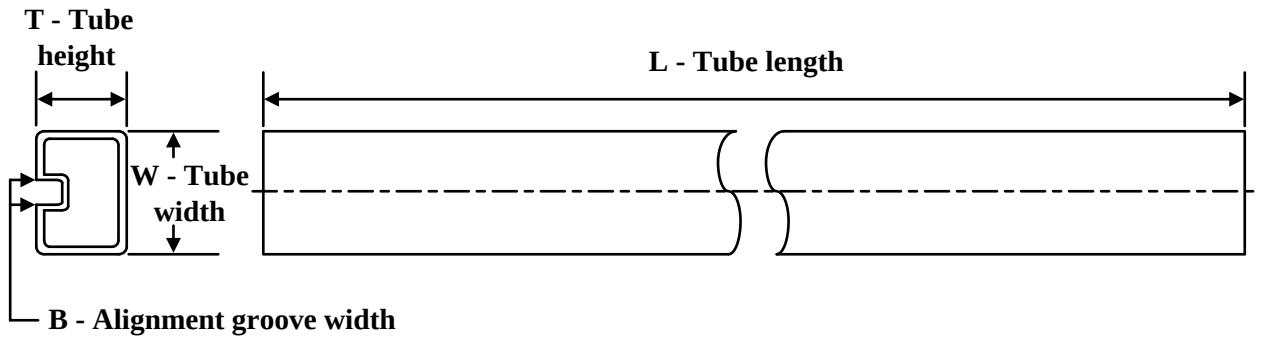
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2061DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS2061DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS2061DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2061DGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS2061DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2062DGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS2062DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2062DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2065DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2065DGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS2065DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2066DGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS2066DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2066DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2067DR	SOIC	D	16	2500	340.5	336.1	32.0

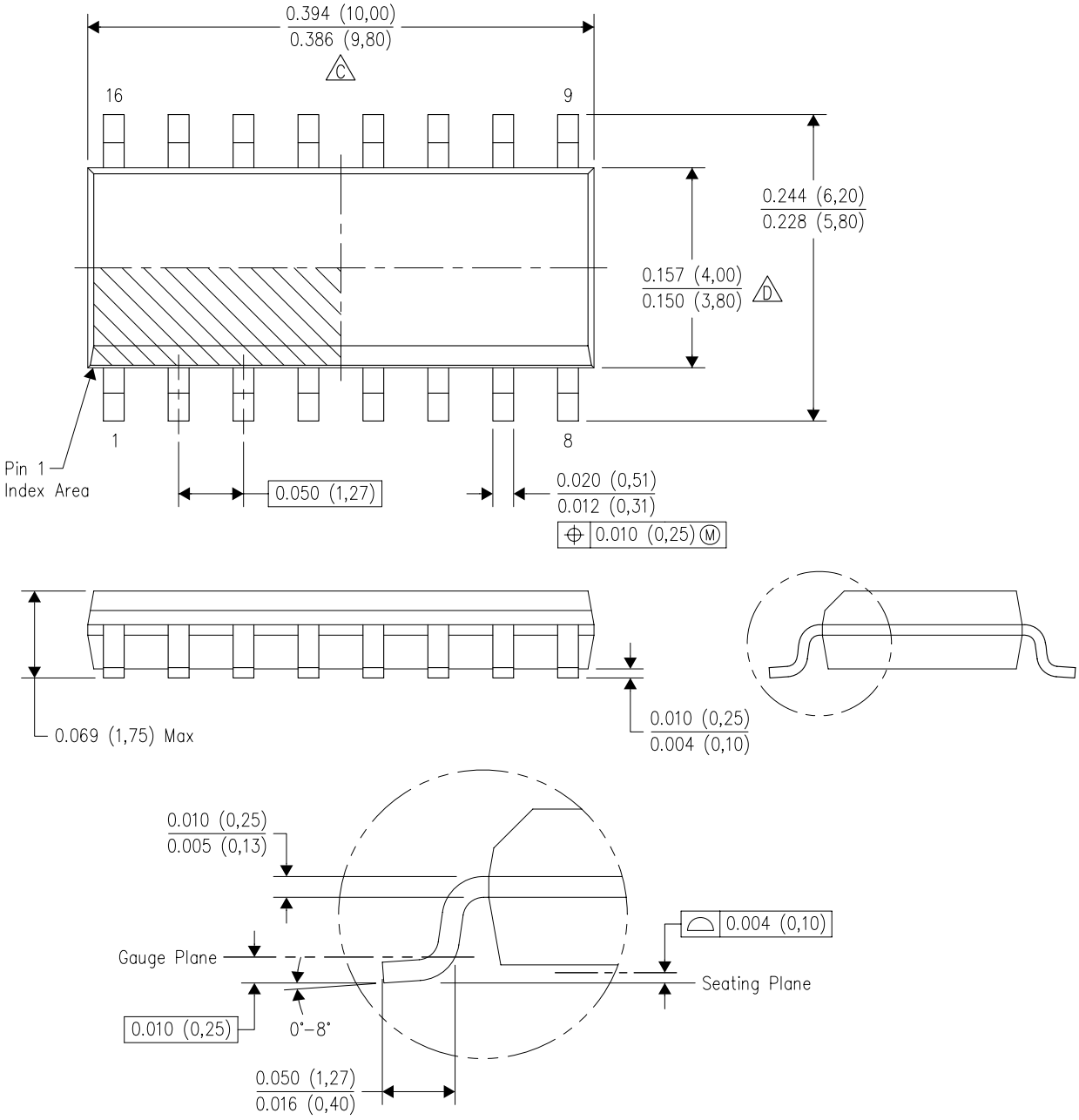
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2061D	D	SOIC	8	75	507	8	3940	4.32
TPS2061DG4	D	SOIC	8	75	507	8	3940	4.32
TPS2061DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2061DGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2062D	D	SOIC	8	75	507	8	3940	4.32
TPS2062DG4	D	SOIC	8	75	507	8	3940	4.32
TPS2062DGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2062DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2062DGNG4	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2062DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2065D	D	SOIC	8	75	507	8	3940	4.32
TPS2065DG4	D	SOIC	8	75	507	8	3940	4.32
TPS2065DGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2065DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066D	D	SOIC	8	75	507	8	3940	4.32
TPS2066DGN	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2066DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066DGNG4	DGN	HVSSOP	8	80	322	6.55	1000	3.01
TPS2067D	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

GENERIC PACKAGE VIEW

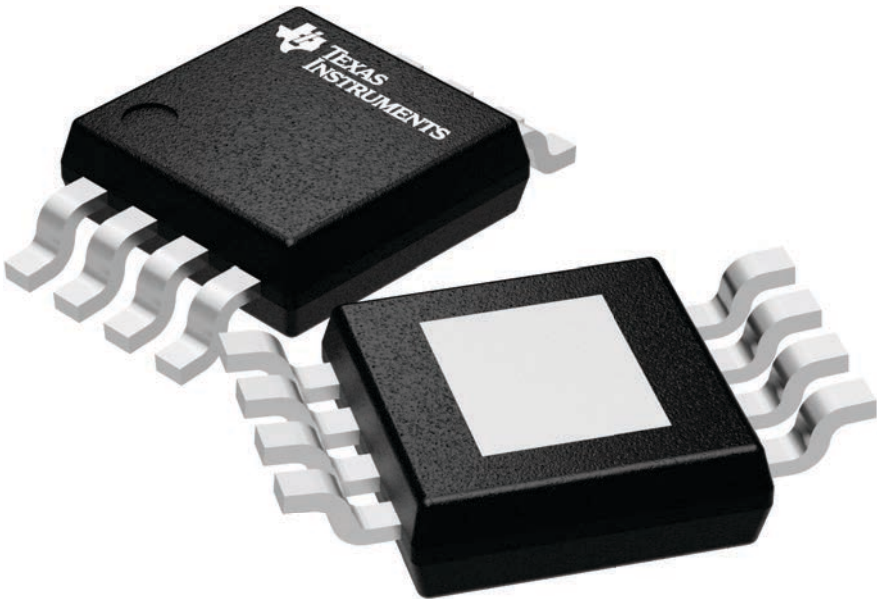
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

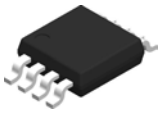
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

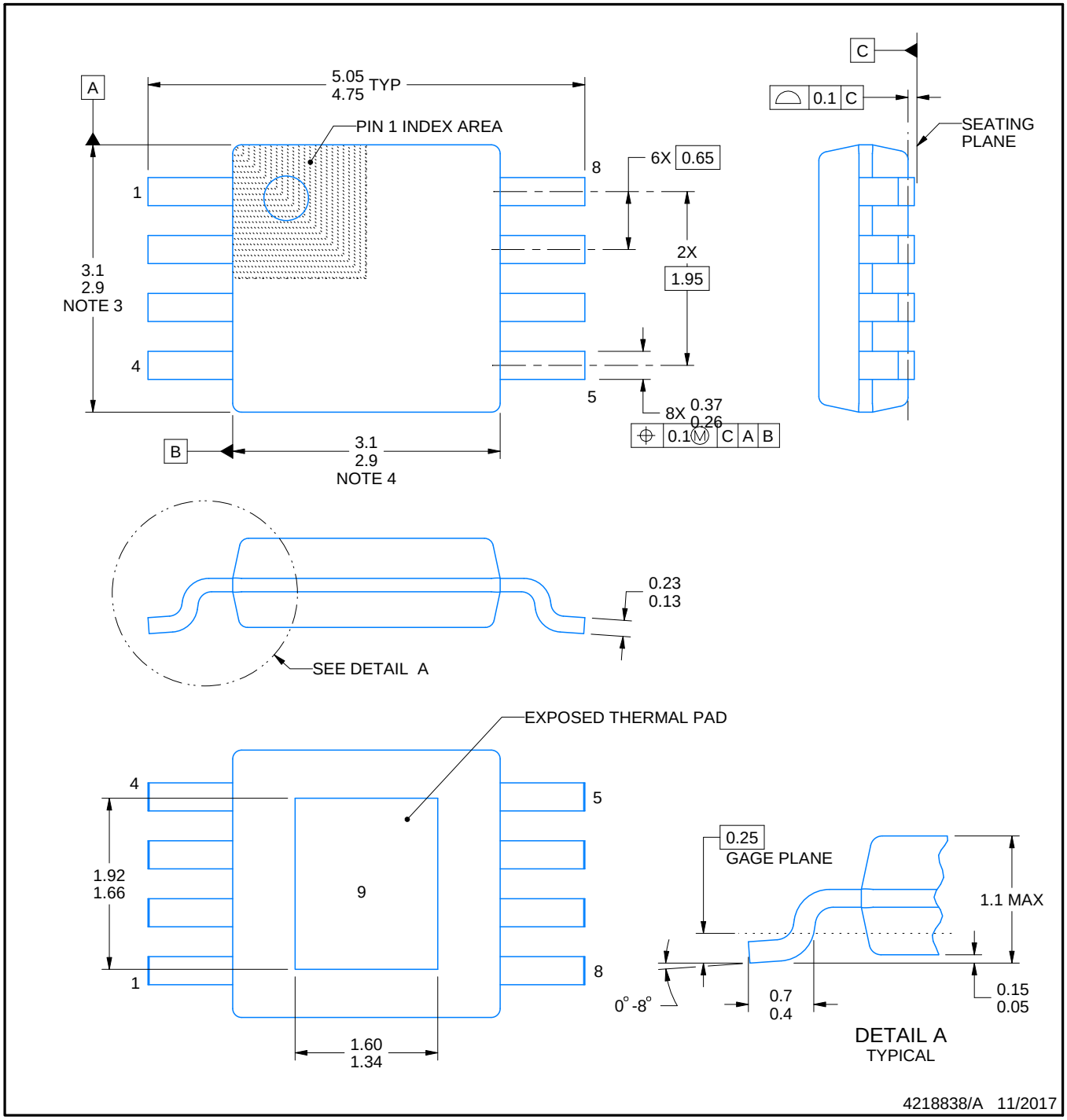
PACKAGE OUTLINE

DGN0008C



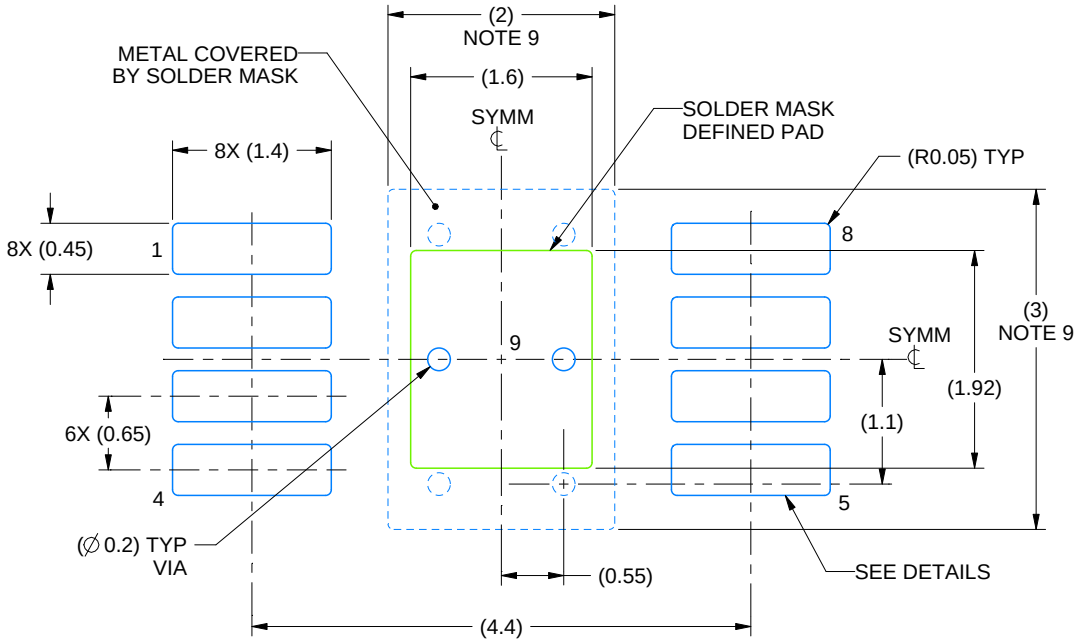
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

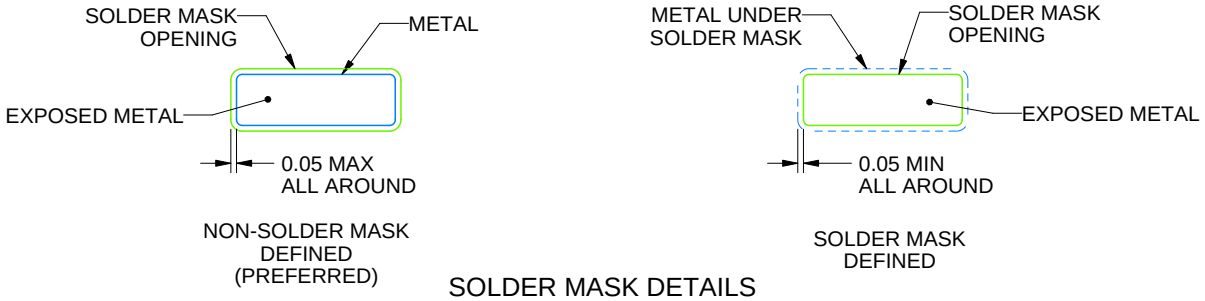


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

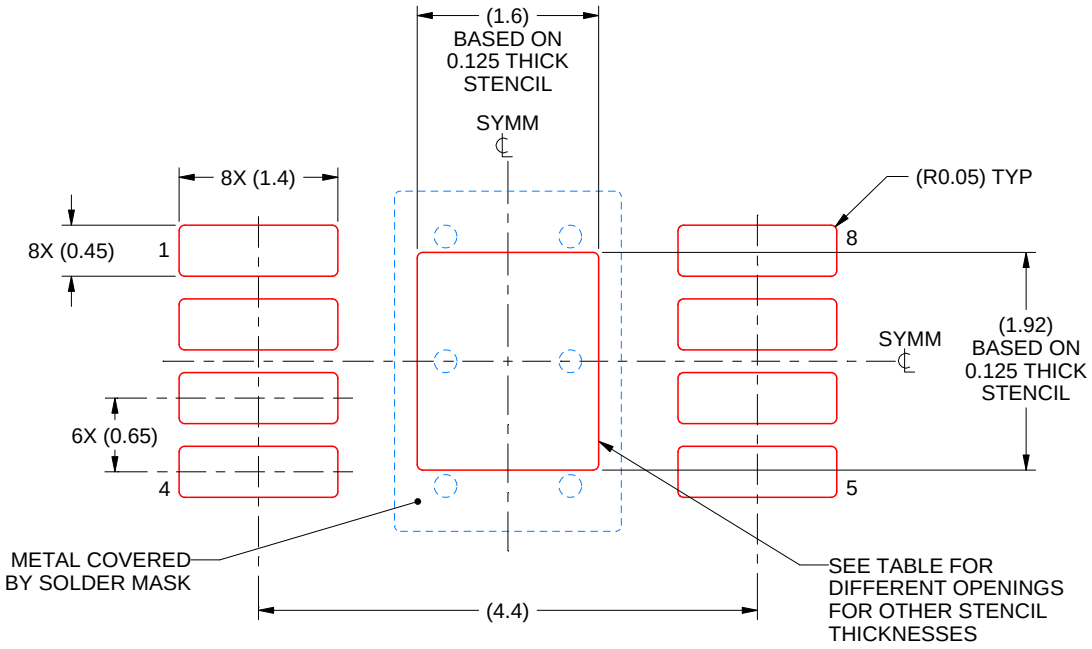


SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

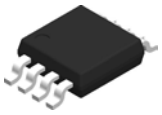
4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

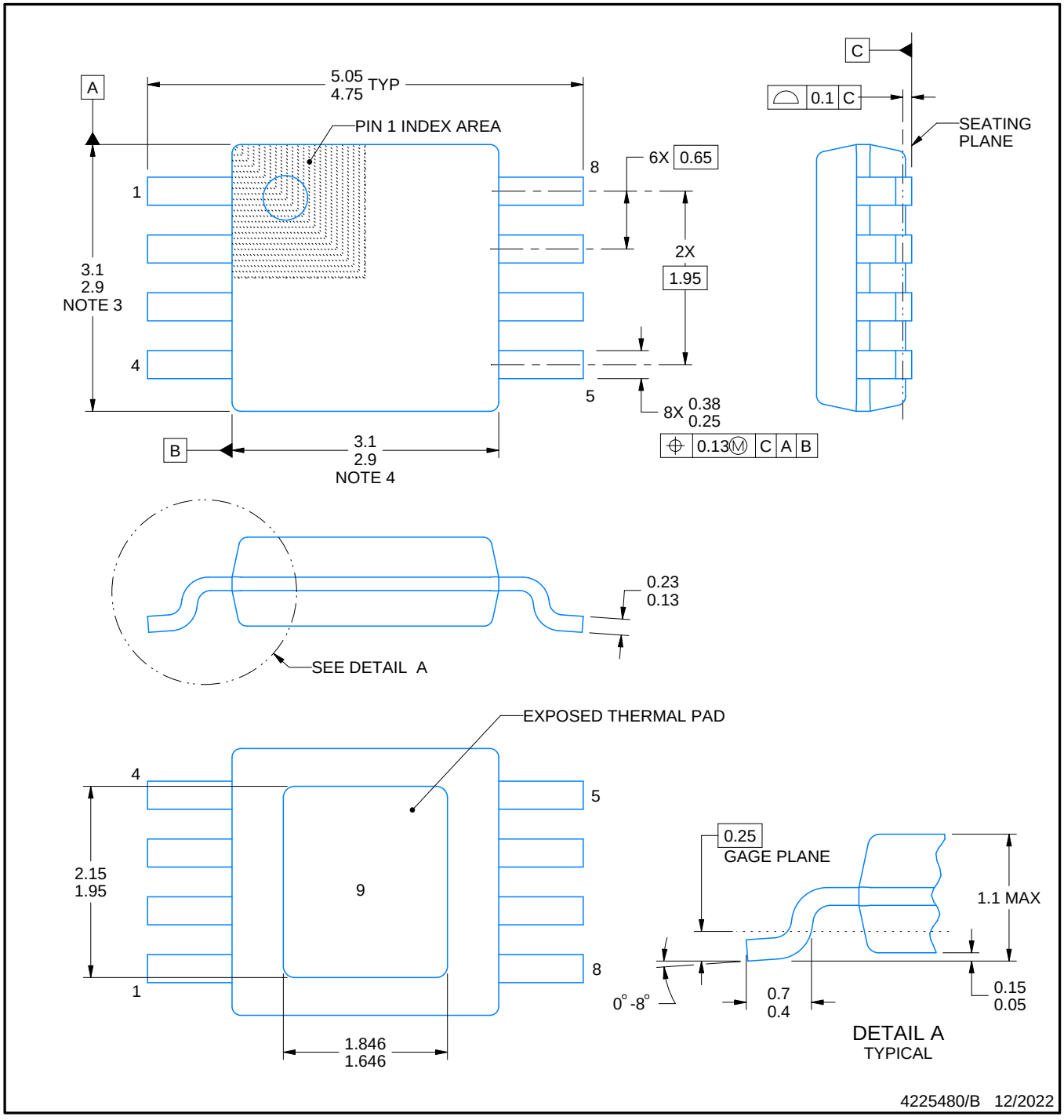
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

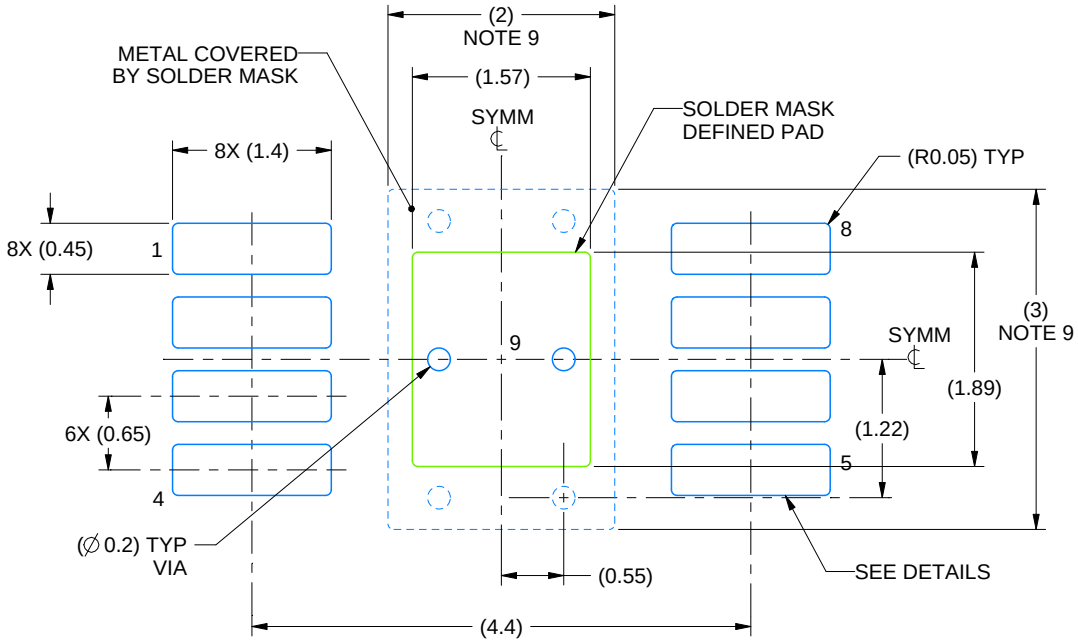
SMALL OUTLINE PACKAGE



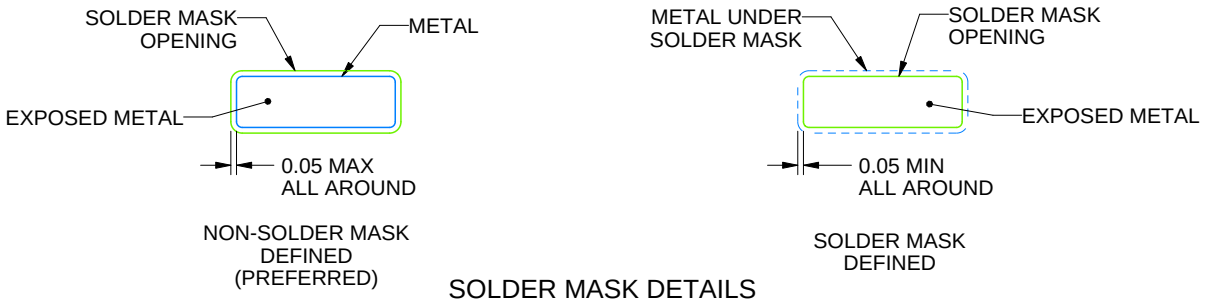
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

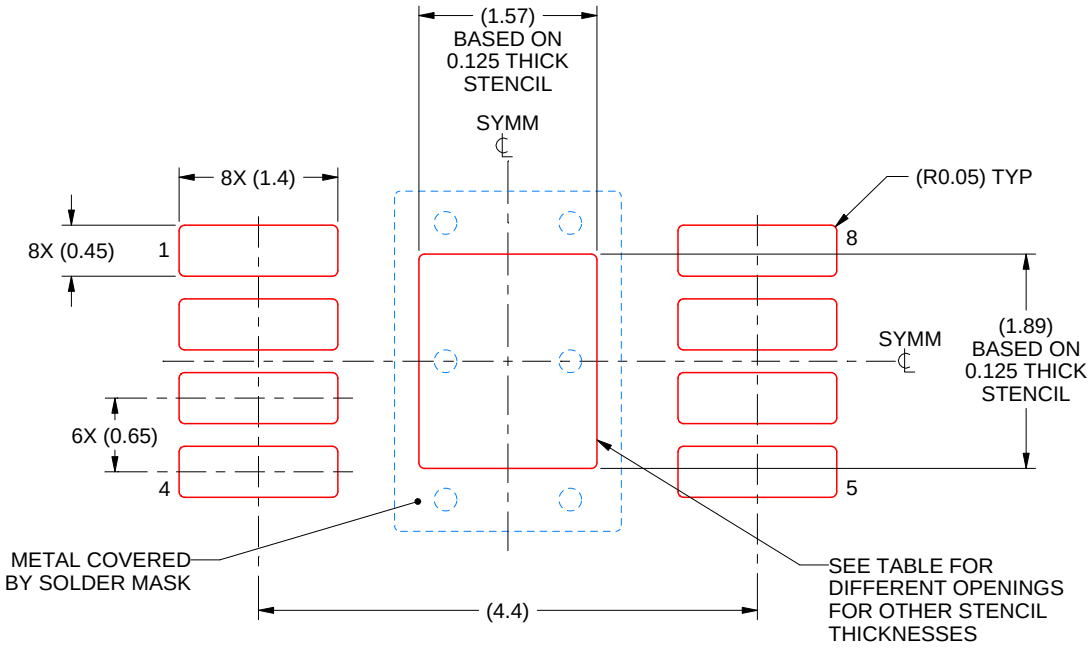


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

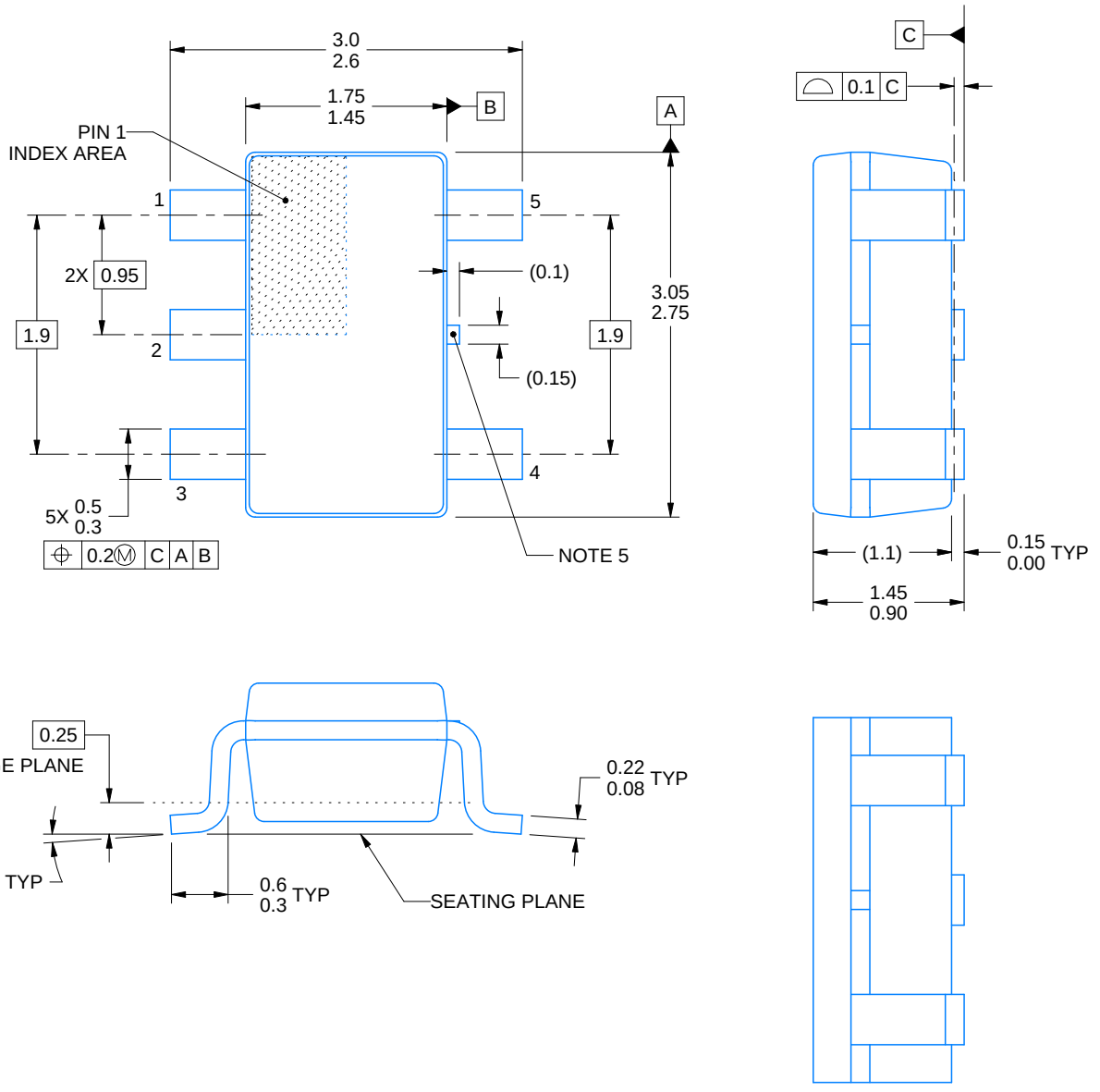
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

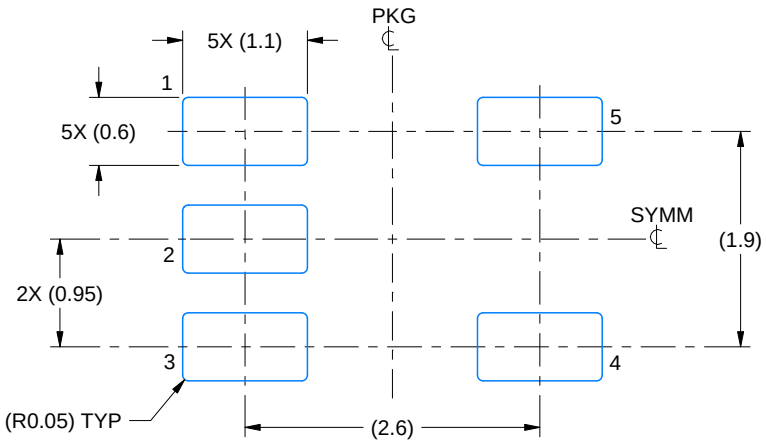


ALTERNATIVE PACKAGE SINGULATION VIEW

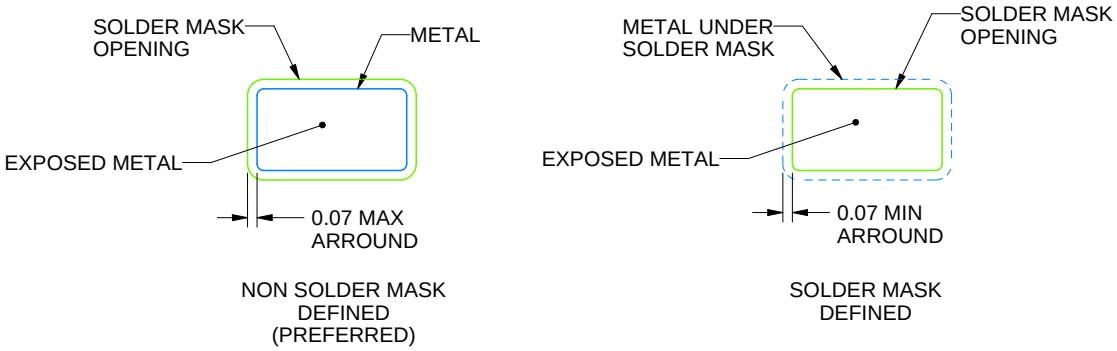
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

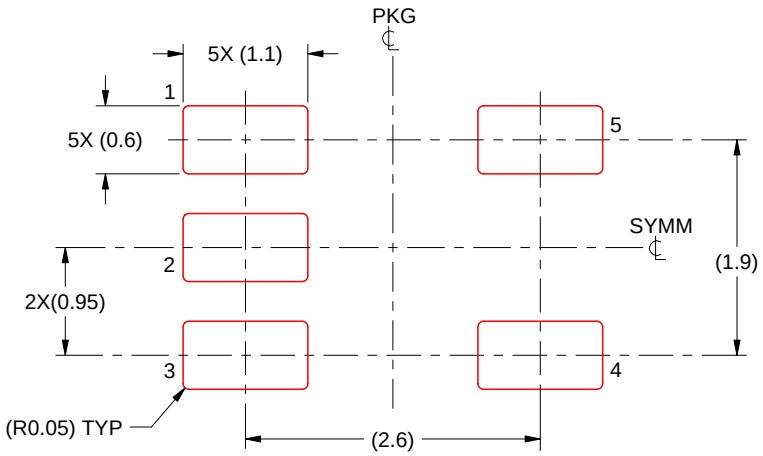


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

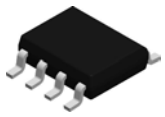


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

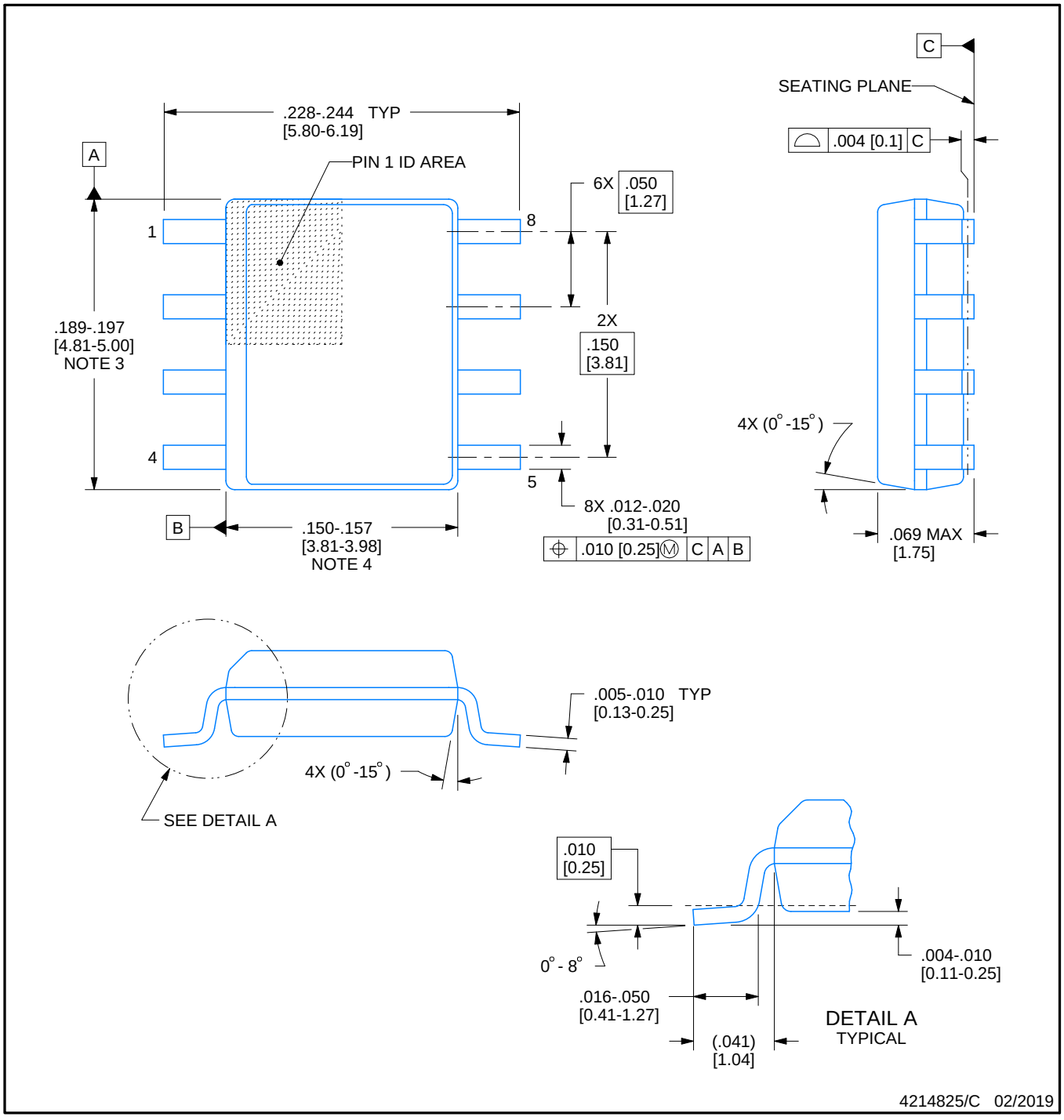


PACKAGE OUTLINE

D0008A

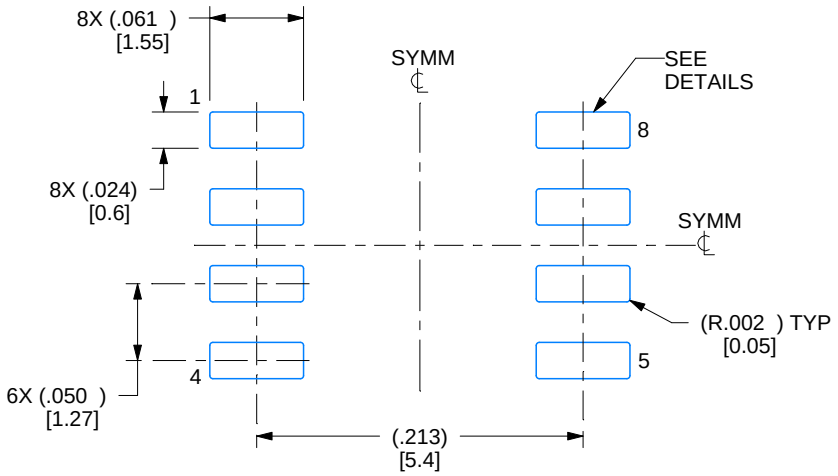
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

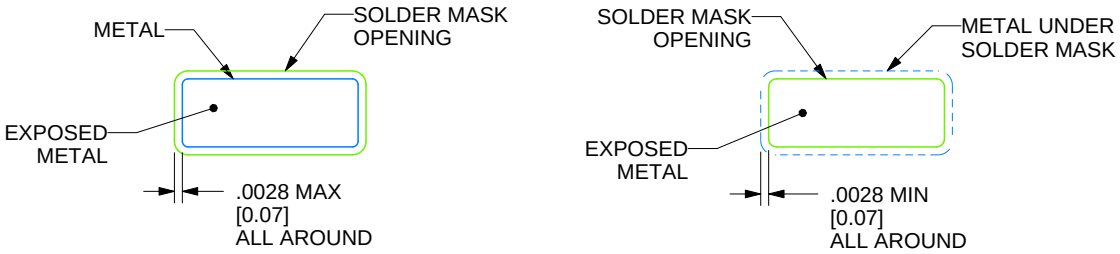


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

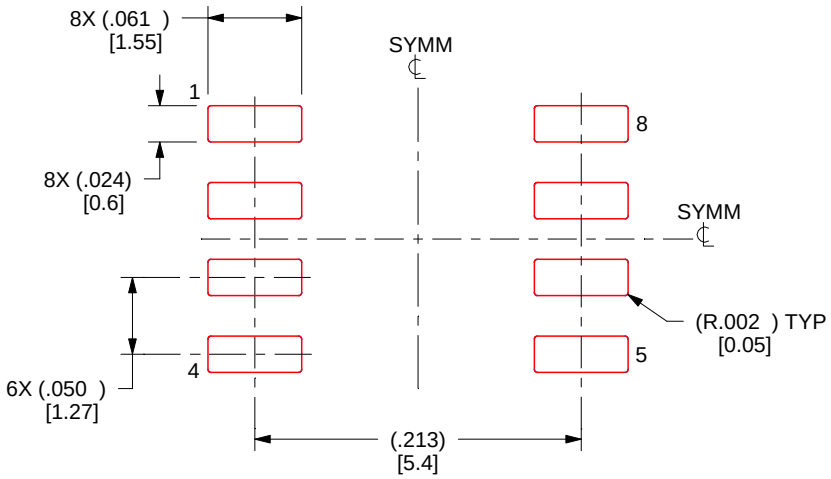
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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