

TPS20xxE 電流制限、パワー・ディストリビューション・スイッチ

1 特長

- シングル・パワー・スイッチ・ファミリ
- 既存のテキサス・インスツルメンツのスイッチ・ポートフォリオとのピン互換
- 定格電流は 1.5A および 2A
- 3.3V および 5V の電源レールをサポート
- 精度 $\pm 20\%$ の固定電流制限
- 高速過電流応答: 2 μ s
- デグリッチされた障害の報告
- 出力放電
- 逆電流ブロック
- ソフトスタート機能内蔵
- 周囲温度範囲: -40°C ~ 85°C

2 アプリケーション

- PC とノート PC
- ゲーム
- テレビ
- ネットワーク接続の周辺機器とプリンタ
- データ・センターおよびエンタープライズ・コンピューティング
- 短絡保護

3 概要

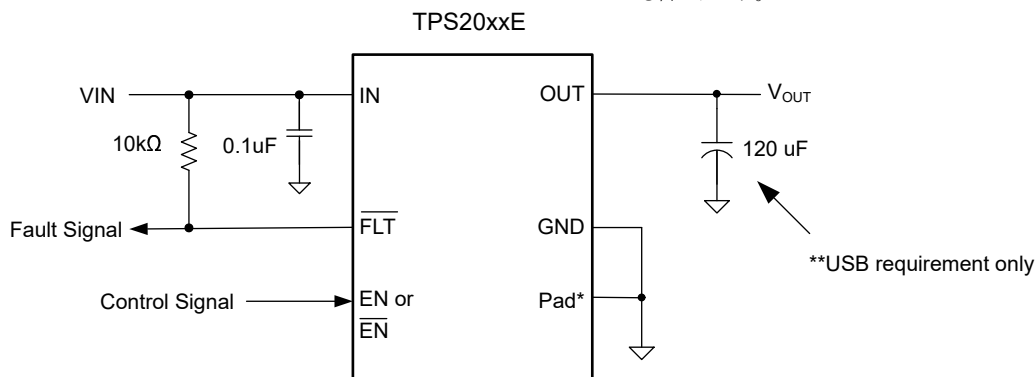
TPS20xxE パワー・ディストリビューション・スイッチ・ファミリは、大きな容量性負荷や短絡が発生しやすい USB などのアプリケーション向けに設計されています。このファミリは、1.5A または 2A の負荷を必要とするアプリケーション向けに固定電流制限スレッシュホールドを提供し、異なるパッケージで High または Low の選択によって分極を実現します。

TPS20xxE ファミリは、出力負荷が電流制限のスレッシュホールドを上回ったときに、定電流モードで動作することにより、出力電流を制限して安全なレベルに下げます。これにより、あらゆる条件下で障害時の電流が予測可能となります。高速な過負荷応答時間を達成していることから、2.7V ~ 5.5V 電源にかかる負荷を軽減し、出力の短絡が発生したときに電力を安定化します。この電源スイッチの立ち上がりおよび立ち下がり時間は、オン / オフ時の電流サージを最小限に抑えるように制御されます。

製品情報

部品番号 (1)	パッケージ (2)	パッケージ・サイズ (3)
TPS20xxE	DBV (SOT-23, 5)	2.90mm × 1.60mm
	DGN (HVSSOP, 8) PowerPAD™	3.00mm × 3.00mm
	DGK (VSSOP, 8)	3.00mm × 3.00mm

- (1) 製品比較表を参照してください。
- (2) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (3) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



* DGN only

** USB requirement that downstream facing ports are bypassed with at least 120uF per hub

代表的なアプリケーションの図



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4 Device Comparison Table

MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE	BASE PART NUMBER	PACKAGED DEVICE AND MARKING ⁽¹⁾		
				DBV (SOT-23, 5)	DGN (HVSSOP, 8)PowerPAD™	DGK (VSSOP, 8) ⁽²⁾
1.5	Y	Low	TPS2068E	2068E	2068E	-
1.5	Y	High	TPS2069E	2069E	2069E	-
2	Y	Low	TPS2000E	2000E	2000E	000E
2	Y	High	TPS2001E	2001E	2001E	001E

- (1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) "-" indicates the device is not available in this package.

5 Pin Configuration and Functions

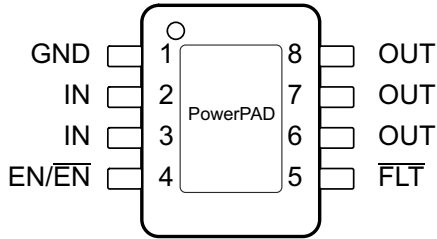


図 5-1. DGN Package 8-Pin MSOP-PowerPAD™ Top View

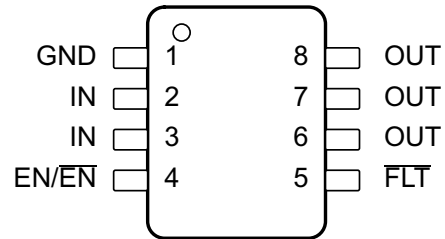


図 5-2. DGK Package 8-Pin VSSOP Top View

表 5-1. Pin Functions - 8 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/ EN	4	I	Enable input, logic high turns on power switch
FLT	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	1	—	Ground connection
IN	2, 3	PWR	Input voltage and power-switch drain; connect a 0.1- μ F or greater ceramic capacitor from IN to GND close to the IC
OUT	6, 7, 8	PWR	Power-switch output, connect to load
PowerPAD (DGN Only)	PowerPAD	—	Connect PAD to GND plane as a heatsink for the best thermal performance. PAD may be left floating if desired.

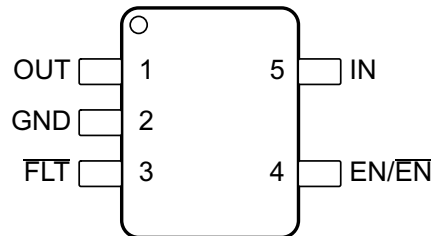


図 5-3. DBV Package 5-Pin SOT-23 Top View

表 5-2. Pin Functions - 5 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/ EN	4	I	Enable input, logic high turns on power switch
FLT	3	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	2	—	Ground connection
IN	5	PWR	Input voltage and power-switch drain; connect a 0.1- μ F or greater ceramic capacitor from IN to GND close to the IC
OUT	1	PWR	Power-switch output, connect to load.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	-0.3	6	V
V _{OUT}	Output voltage	-0.3	6	V
V _{EN}	Input voltage	-0.3	6	V
V _{FLT}	Voltage range	-0.3	6	V
I _{OUT}	Continuous output current	Internal Limited		
T _J	Junction temperature	-40	125	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins ⁽²⁾	±500	
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge, OUT pin ⁽³⁾	±8000	V
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 air-gap discharge, OUT pin ⁽³⁾	±15000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) V_{OUT} was surged on a PCB with input and output bypassing per the Typical Application Diagram on the first page with no device failures.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2.7		5.5	V
V _{EN}	Input voltage, EN or $\overline{\text{EN}}$	0		5.5	V
V _{IH}	High-level input voltage, EN or $\overline{\text{EN}}$	1.8			V
V _{IL}	Low-level input voltage, EN or $\overline{\text{EN}}$			0.8	V
I _{OUT}	Continuous output current - TPS2068E, TPS2069E			1.5	A
I _{OUT}	Continuous output current - TPS2000E, TPS2001E			2	A
T _J	Junction temperature	-40		125	°C
I _{FLT}	Sink current into $\overline{\text{FLT}}$	0		10	mA

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS20xxE			UNIT
		DBV (SOT-23)	DGN (HVSSOP) PowerPAD™	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	184.6	51.7	169.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	92.6	82.7	65.5	
R _{θJB}	Junction-to-board thermal resistance	59.9	25.2	90.5	
Ψ _{JT}	Junction-to-top characterization parameter	30.7	6.5	11.8	
Ψ _{JB}	Junction-to-board characterization parameter	59.6	25.2	89.0	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	-	6.4	-	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Unless otherwise noted: V_{IN} = 5.5 V, V_{EN} = VIN, I_{OUT} = 0 A, -40°C ≤ T_J ≤ 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH (TPS2068E, TPS2069E)						
R _{DS(ON)} (DBV)	Static drain-source on-state resistance, 5V or 3.3V operation	V _{IN} = 5 V or 3.3 V, I _O = 1.5 A, -40°C ≤ T _J ≤ 125°C		70	105	mΩ
	Static drain-source on-state resistance, 2.7V operation	V _{IN} = 2.7 V, I _O = 1.5 A, -40°C ≤ T _J ≤ 125°C		70	110	mΩ
POWER SWITCH (TPS2000E, TPS2001E)						
R _{DS(ON)} (DBV)	Static drain-source on-state resistance, 5V or 3.3V operation	V _{IN} = 5 V or 3.3 V, I _O = 2.0 A, -40°C ≤ T _J ≤ 125°C		70	105	mΩ
	Static drain-source on-state resistance, 2.7V operation	V _{IN} = 2.7 V, I _O = 2.0 A, -40°C ≤ T _J ≤ 125°C		70	110	mΩ
T_{rise} and T_{fall}						
t _r	Rise time, output	V _{IN} = 5.5 V, C _L = 1 μF, R _L = 10 Ω, T _J = 25°C		0.6	1.5	ms
		V _{IN} = 2.7 V, C _L = 1 μF, R _L = 10 Ω, T _J = 25°C		0.4	1	ms
t _f	Fall time, output	V _{IN} = 5.5 V, C _L = 1 μF, R _L = 10 Ω, T _J = 25°C	0.05		0.5	ms
		V _{IN} = 2.7 V, C _L = 1 μF, R _L = 10 Ω, T _J = 25°C	0.05		0.5	ms
ENABLE INPUT EN (TPS2068E, TPS2069E and TPS2000E)						
V _{IH}	Enable high-level input voltage	2.7 V ≤ V _{IN} ≤ 5.5 V	1.8			V
V _{IL}	Enable low-level input voltage	2.7 V ≤ V _{IN} ≤ 5.5 V			0.8	V
I _{EN}	EN pin leakage current	V _{EN} =5.5V	-0.5		0.5	μA
ENABLE INPUT EN (TPS2001E)						
V _{IH}	Enable high-level input voltage	2.7 V ≤ V _{IN} ≤ 5.5 V	1.75			V
V _{IH}	Enable high-level input voltage	2.7 V ≤ V _{IN} ≤ 5.0 V	1.6			V
V _{IH}	Enable high-level input voltage	2.7 V ≤ V _{IN} ≤ 3.5 V	1.5			V
V _{IL}	Enable low-level input voltage	2.7 V ≤ V _{IN} ≤ 5.5 V			0.8	V
I _{EN}	EN pin leakage current	V _{EN} =5.5V	-0.5		0.5	μA
T_{on} and T_{off}						
t _{on}	Turnon time	C _L = 100 μF, R _L = 10 Ω			3	ms
t _{off}	Turnoff time	C _L = 100 μF, R _L = 10 Ω			3	ms

6.5 Electrical Characteristics (続き)

Unless otherwise noted: $V_{IN} = 5.5\text{ V}$, $V_{EN} = V_{IN}$, $I_{OUT} = 0\text{ A}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISCHARGE						
R_{DCHG}	Discharge resistance	$V_{IN} = V_{OUT} = 5\text{ V}$, disabled	400	500	810	Ω
CURRENT LIMIT (TPS2068E and TPS2069E)						
I_{OS}	Short circuit output current	$V_{IN} = 5\text{ V}$, OUT connect to GND, device enable into short circuit, $T_J = 25^{\circ}\text{C}$	1.71	2.13	2.55	A
		$V_{IN} = 5\text{ V}$, OUT connect to GND, device enable into short circuit, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	1.6	2.13	2.66	A
t_{ios}	response time to short circuit	$V_{IN} = 5.0\text{ V}$, $R_L = 50\text{ m}\Omega$. See Figure 7-5 .		1.5		μs
CURRENT LIMIT (TPS2000E and TPS2001E)						
I_{OS}	Short circuit output current	$V_{IN} = 5\text{ V}$, OUT connect to GND, device enable into short circuit, $T_J = 25^{\circ}\text{C}$	2.24	2.8	3.36	A
		$V_{IN} = 5\text{ V}$, OUT connect to GND, device enable into short circuit, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$	2.1	2.8	3.5	A
t_{ios}	response time to short circuit	$V_{IN} = 5.0\text{ V}$, $R_L = 50\text{ m}\Omega$. See Figure 7-5 .		1.5		μs
SUPPLY CURRENT						
I_{SD}	Supply current, switch disable	No load on OUT, $V_{EN} = 0\text{ V}$, $T_J = 25^{\circ}\text{C}$		0.5	1	μA
		No load on OUT, $V_{EN} = 0\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		0.5	5	μA
I_{SE}	Supply current, switch enable	No load on OUT, $V_{EN} = 5.5\text{ V}$, $T_J = 25^{\circ}\text{C}$		93	118	μA
		No load on OUT, $V_{EN} = 5.5\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		93	118	μA
I_{LKG}	Leakage current	OUT connected to ground, $V_{EN} = 0\text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$		1		μA
I_{REV}	Reverse leakage current	$V_{OUT} = 5.5\text{ V}$, IN = ground, $T_J = 25^{\circ}\text{C}$		0		μA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	undervoltage lockout threshold, IN	V_{IN} rising	2		2.6	V
	Hysteresis, IN	$T_J = 25^{\circ}\text{C}$		75		mV
OVERCURRENT FLAG						
$V_{OL(OC)}$	Output low voltage	$I_{OL(OC)} = 5\text{ mA}$			180	mV
$I_{OFF_Leakage}$	Off-state leakage	$V_{OC} = 5.5\text{ V}$			1	μA
T_{OC_DEG}	/OC Flag deglitch	/OC assertion or de-assertion	6	8	12	ms
THERMAL SHUTDOWN						
T_{OTSD_R}	Thermal shutdown threshold rising threshold		155	175	195	$^{\circ}\text{C}$
	Hysteresis			10		$^{\circ}\text{C}$
THERMAL SHUTDOWN in Current Limit						
$T_{OTSD_CL_R}$	Thermal shutdown rising threshold in current limit		135	155	175	$^{\circ}\text{C}$
	Hysteresis			10		$^{\circ}\text{C}$

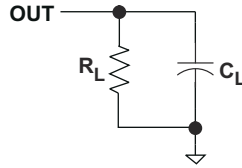


図 6-1. Output Rise and Fall Test Load

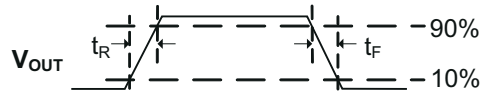


図 6-2. Power-On and Power-Off Timing

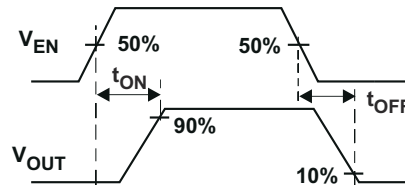


図 6-3. Enable Timing, Active High Enable

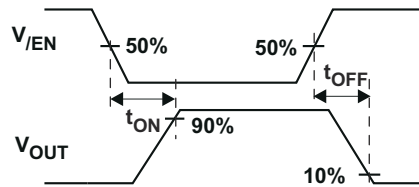


図 6-4. Enable Timing, Active Low Enable

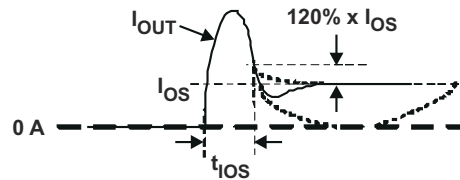


図 6-5. Output Short-Circuit Parameters

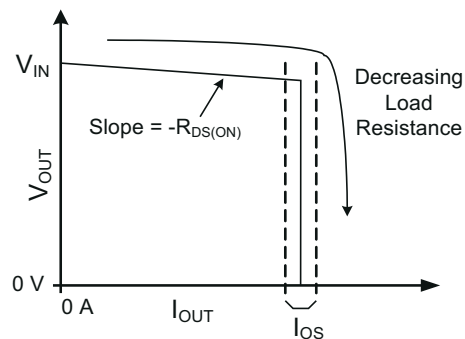
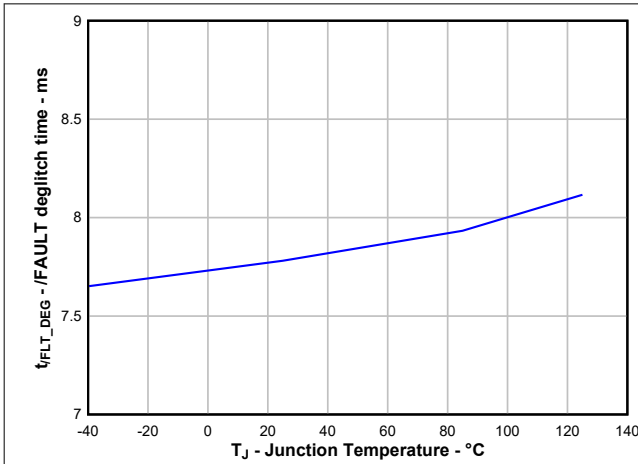
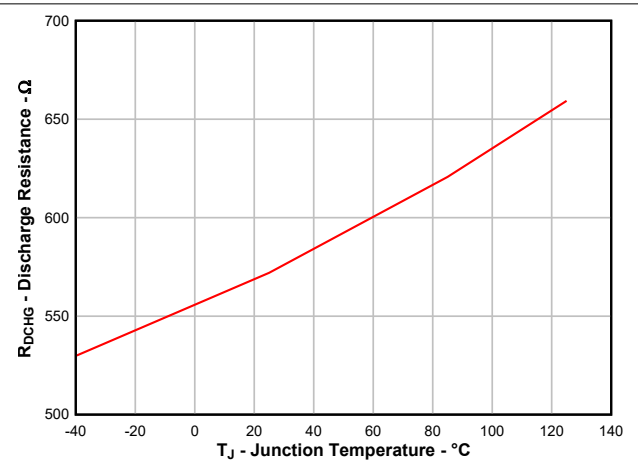


図 6-6. Output Characteristic Showing Current Limit

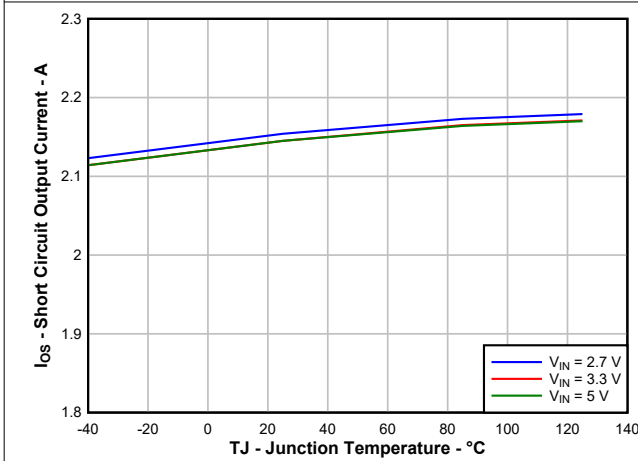
6.6 Typical Characteristics



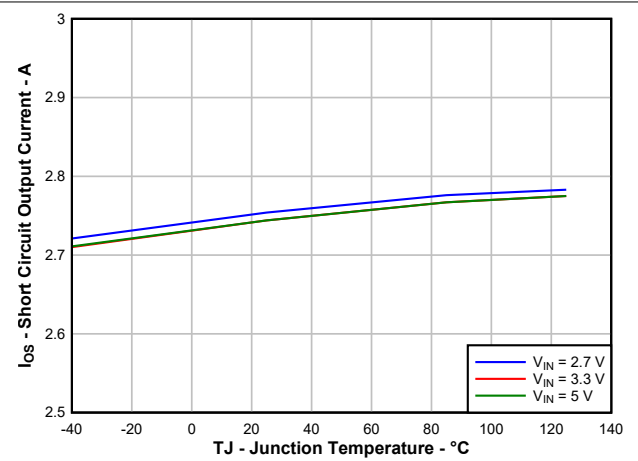
6-7. Deglitch Period (T_{FLT}) vs Temperature



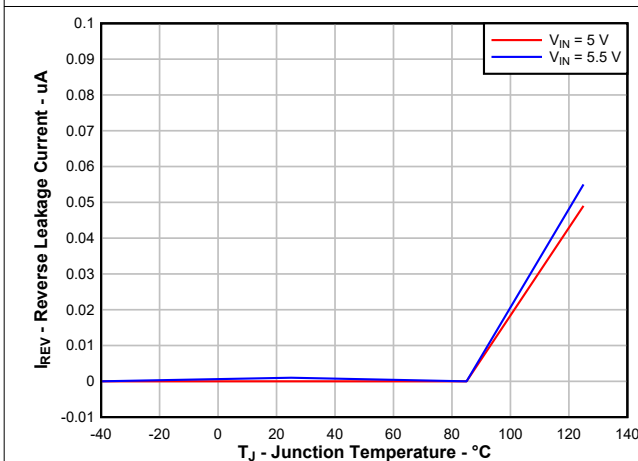
6-8. Output Discharge Resistance vs Temperature



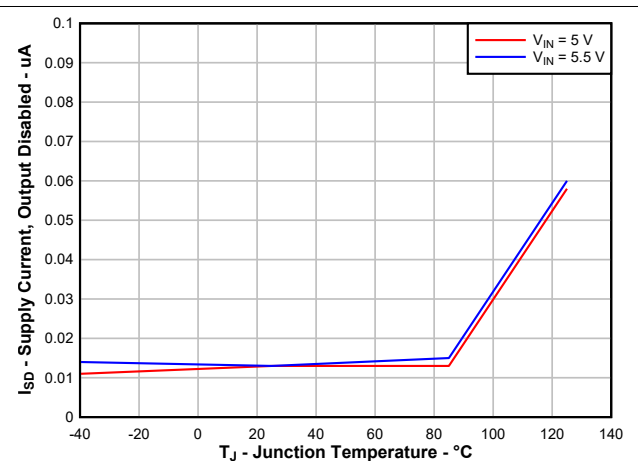
6-9. TPS2068E, TPS2069E Short Circuit Current (I_{OS}) vs Temperature



6-10. TPS2000E, TPS2001E Short Circuit Current (I_{OS}) vs Temperature

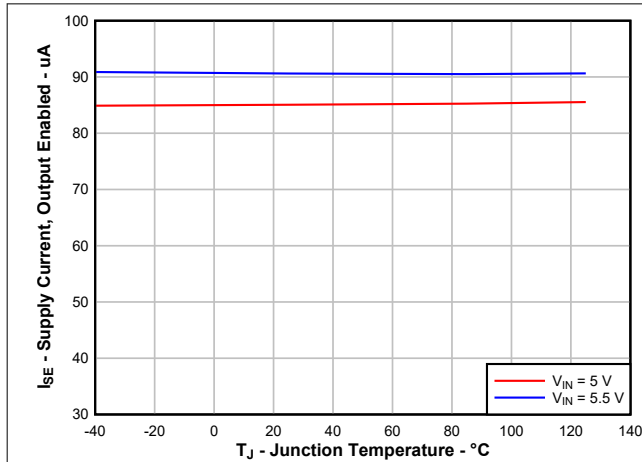


6-11. Reverse Leakage Current (I_{REV}) vs Temperature

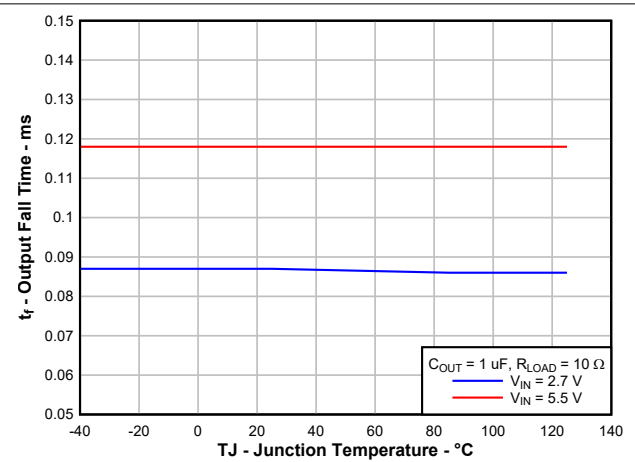


6-12. Disabled Supply Current (I_{SD}) vs Temperature

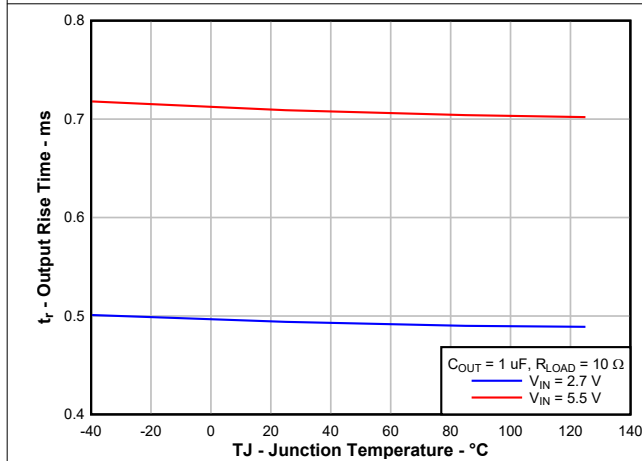
6.6 Typical Characteristics (continued)



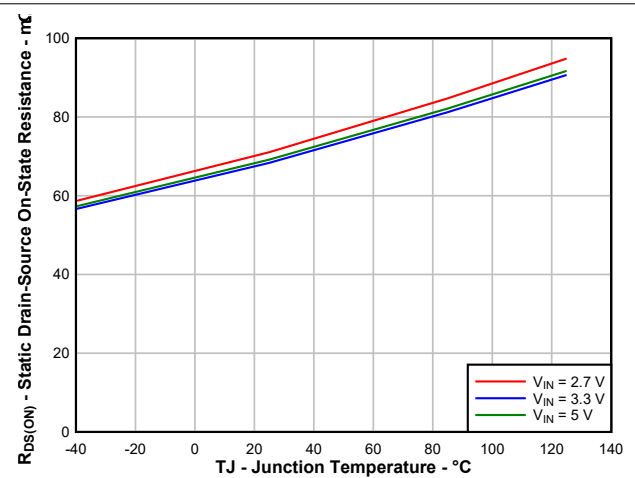
6-13. Enabled Supply Current (I_{SE}) vs Temperature



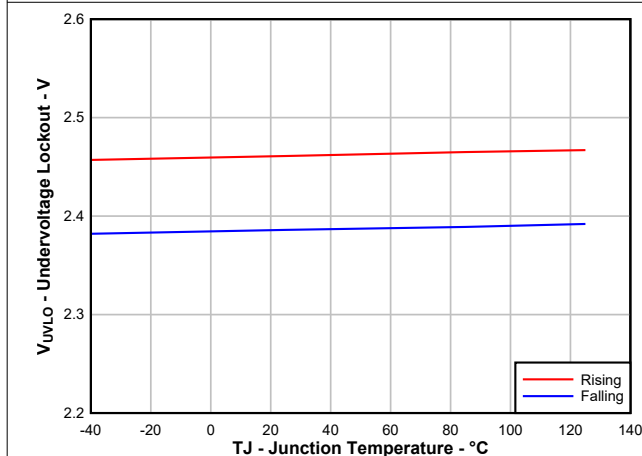
6-14. Output Fall Time (T_F) vs Temperature



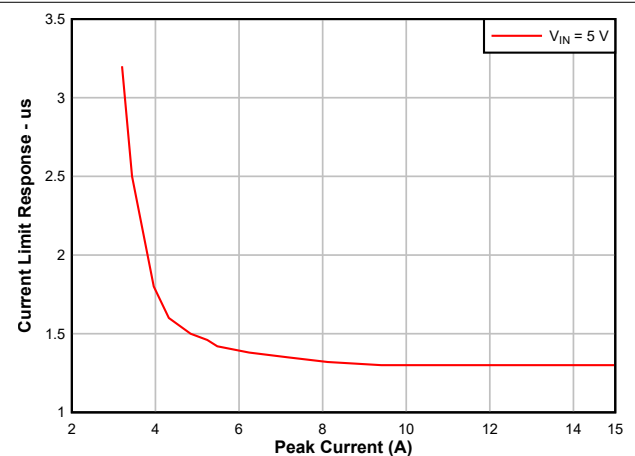
6-15. Output Rise Time (T_R) vs Temperature



6-16. Input-Output Resistance ($R_{DS(ON)}$) vs Temperature



6-17. Undervoltage Lockout vs Temperature



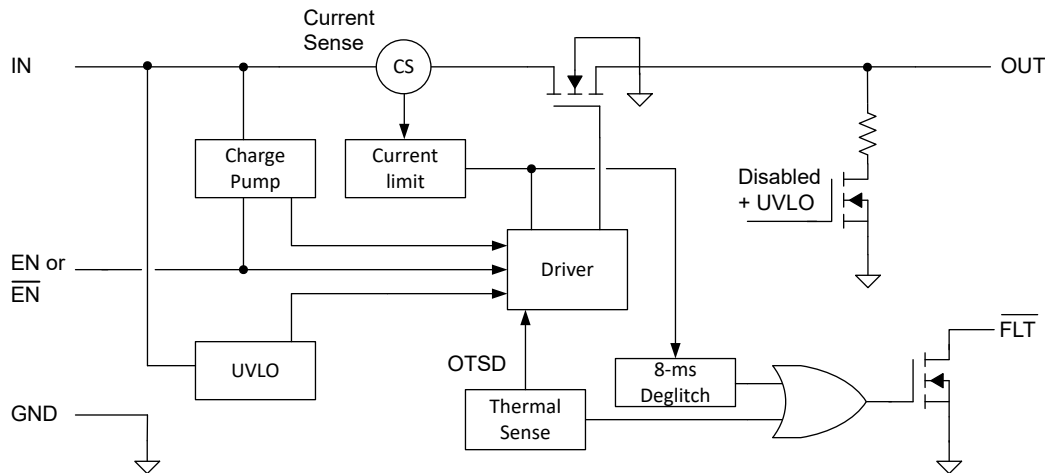
6-18. Current Limit Response (t_{IOS}) vs Peak Current

7 Detailed Description

7.1 Overview

The TPS20xxE are current-limited, power-distribution switches providing a range from 1.5 A and 2 A of continuous load current in 3.3V and 5V power rail circuits. These parts use N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. They are designed for applications where short circuits or heavy capacitive loads are encountered. Device features include enable, reverse blocking when disabled, output discharge pulldown, overcurrent protection, overtemperature protection, and deglitched fault reporting.

7.2 Functional Block Diagram



7-1. TPS20xxE Block Diagram

7.3 Feature Description

7.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted ON/OFF cycling due to input voltage drop from large current surges. $\overline{\text{FLT}}$ is high impedance when the TPS20xxE are in UVLO.

7.3.2 Enable

The logic enable input (EN, or $\overline{\text{EN}}$), controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 μA when the TPS20xxE are disabled. Disabling the TPS20xxE immediately clears an active $\overline{\text{FLT}}$ indication. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times (t_{ON} , t_{OFF}) are composed of a delay and a rise or fall time (t_{R} , t_{F}). The delay times are internally controlled. The rise time is controlled by both the TPS20xxE and the external loading (especially capacitance). TPS20xxE fall time is controlled by the loading (R and C), and the output discharge (R_{DCHG}). An output load consisting of only a resistor experiences a fall time set by the TPS20xxE. An output load with parallel R and C elements experiences a fall time determined by the (R \times C) time constant if it is longer than the t_{F} TPS20xxE.

The enable must not be left open, and may be tied to VIN or GND depending on the device.

7.3.3 Internal Charge Pump

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start

functionality. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

7.3.4 Current Limit

The TPS20xxE responds to overloads by limiting output current to the static I_{OS} levels shown in [セクション 6.5](#). When an overload condition is present, the device maintains a constant output current, with the output voltage determined by $(I_{OS} \times R_{LOAD})$. Two possible overload conditions can occur. The first overload condition occurs when either:

1. input voltage is first applied, enable is true, and a short circuit is present (load which draws $I_{OUT} > I_{OS}$)
2. input voltage is present and the TPS20xxE are enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPS20xxE ramps the output current to I_{OS} . The TPS20xxE limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in [図 8-4](#) where the device was enabled into a short, and subsequently cycles current OFF and ON as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} ([図 6-5](#) and [図 6-6](#)) when the specified overload (see [セクション 6.5](#)) is applied. The response speed and shape varies with the overload level, input circuit, and rate of application. The current limit response vary between simply settling to I_{OS} , or turnoff and controlled return to I_{OS} . Similar to the previous case, the TPS20xxE limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS20xxE thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation $[(V_{IN} - V_{OUT}) \times I_{OS}]$ driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (minimum) while in current limit. The device remains off until the junction temperature cools 10°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products that are similar to the TPS20xxE. Many older designs have an output I vs V characteristic similar to the plot labeled *Current Limit with Peaking* in [図 7-2](#). This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPS20xxE family of parts does not present noticeable peaking in the current limit, corresponding to the characteristic labeled *Flat Current Limit* in [図 7-2](#). This is why the I_{OC} parameter is not present in [セクション 6.5](#).

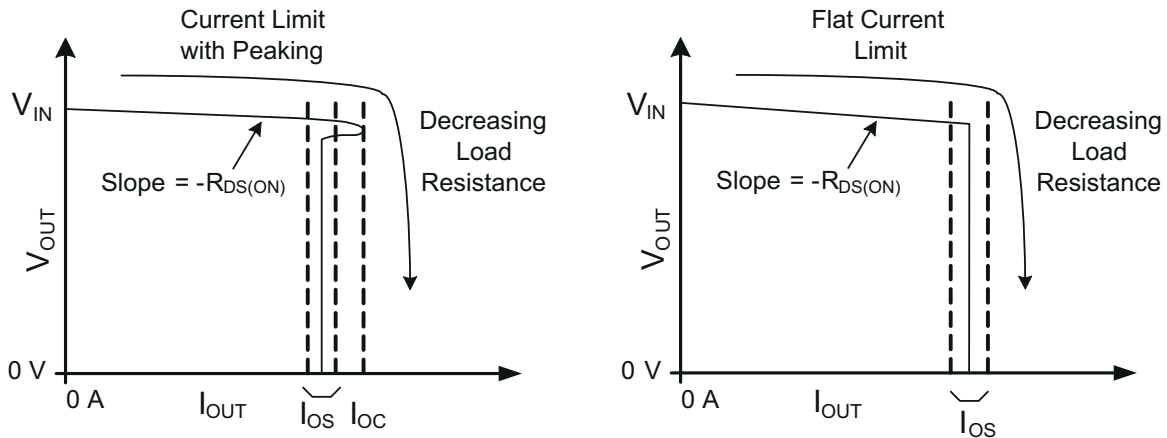


図 7-2. Current Limit Profiles

7.3.5 FLT

The FLT open-drain output is asserted (active low) during an overload or overtemperature condition. A 8-ms deglitch on both the rising and falling edges avoids false reporting at start-up and during transients. A current

limit condition shorter than the deglitch period clears the internal timer upon termination. The deglitch timer does not integrate multiple short overloads and declare a fault. This is also true for exiting from a faulted state. An input voltage with excessive ripple and large output capacitance may interfere with operation of $\overline{\text{FLT}}$ around I_{OS} as the ripple drives the TPS20xxE in and out of current limit.

If the TPS20xxE are in current limit and the overtemperature circuit goes active, $\overline{\text{FLT}}$ goes true immediately; however, the exiting this condition is deglitched. $\overline{\text{FLT}}$ is tripped just as the knee of the constant-current limiting is entered. Disabling the TPS20xxE clears an active $\overline{\text{FLT}}$ as soon as the switch turns off. $\overline{\text{FLT}}$ is high impedance when the TPS20xxE are disabled or in undervoltage lockout (UVLO).

7.3.6 Output Discharge

A 500- Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS20xxE is in UVLO or disabled. The pulldown circuit loses bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The logic enable input (EN or $\overline{\text{EN}}$) pin provides electrical ON and OFF control for the TPS20xxE. When $V_{\text{EN/EN}}$ is below 0.8 V or V_{IN} is below 2 V, the device is in shutdown mode in which the power switch is turned off and the supply current is reduced to less than 1 μA . Refer to [Enable](#) and [Undervoltage Lockout](#) sections for the detailed description of the Enable and Undervoltage Lockout functionality.

7.4.2 Active Mode

The TPS20xxE enters active mode when $V_{\text{EN/EN}}$ is above 1.8 V, and the supply voltage on the IN pin is above 2.6 V. At the onset of active mode, the power switch is turned on and the full features are enabled.

8 Application and Implementation

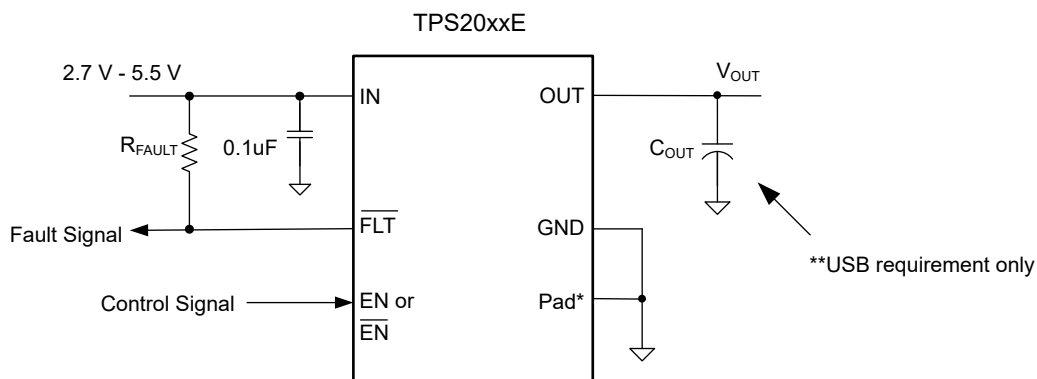
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS20xxE current-limited power switch uses N-channel MOSFETs in applications requiring continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

8.2 Typical Application



* DGN only

** USB requirement that downstream facing ports are bypassed with at least 120uF per hub

図 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the following input parameters:

1. The TPS2001EDBV operates from a 5-V to ± 0.5 -V input rail.
2. What is the normal operation current, for example, the maximum allowable current drawn by portable equipment for BC1.2 is 1500 mA, so the normal operation current is 1500 mA, and the minimum current limit of power switch must exceed 1500 mA to avoid false trigger during normal operation. For the TPS2001E device, target 2-A continuous output current application.
3. What is the maximum allowable current provided by up-stream power, the maximum current limit of power switch that must lower it to ensure power switch can protect the up-stream power when overload is encountered at the output of power switch. For the TPS2001E device, the maximum I_{OS} is 3.5 A.

8.2.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

1. Normal input operation voltage
2. Output continuous current
3. Maximum up-stream power supply output current

8.2.2.1 Input and Output Capacitance

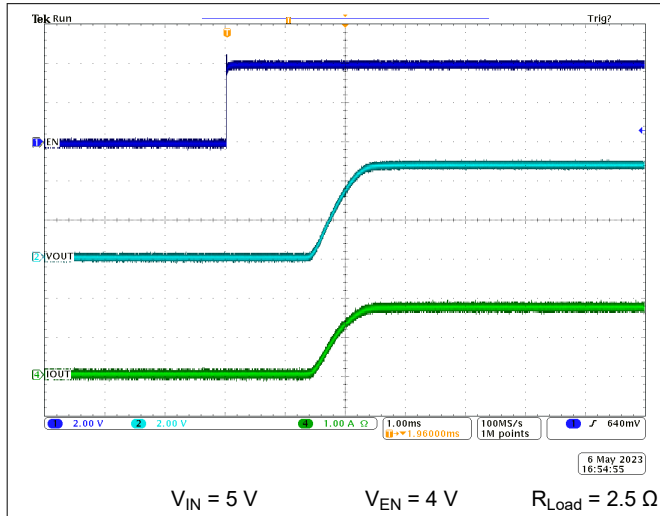
Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends placing a 0.1- μ F or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling.

All protection circuits such as the TPS20xxE has the potential for input voltage overshoots and output voltage undershoots.

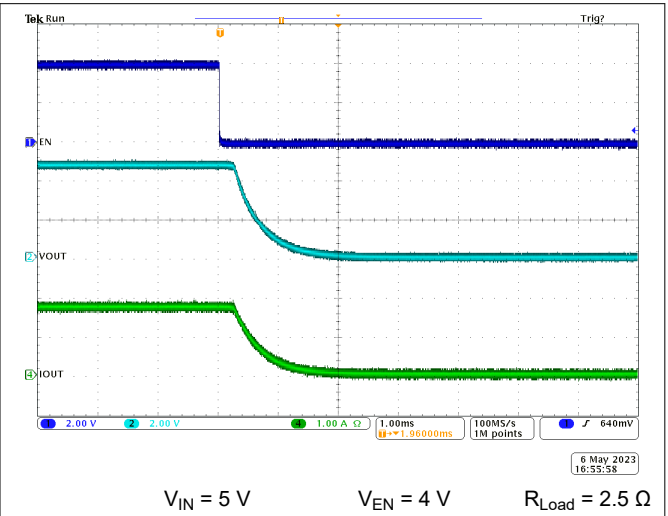
Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2× the applied. The second cause is due to the abrupt reduction of output short-circuit current when the TPS20xxE turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS20xxE output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current limit speed of the TPS20xxE to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 μF to 22 μF adjacent to the TPS20xxE input aids in both speeding the response time and limiting the transient seen on the input power bus.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS20xxE has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120- μF minimum output capacitance is required. Typically a 150- μF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 μF of capacitance, and there is potential to drive the output negative, then TI recommends a minimum of 10- μF ceramic capacitance on the output. The voltage undershoot must be controlled to less than 1.5 V for 10 μs .

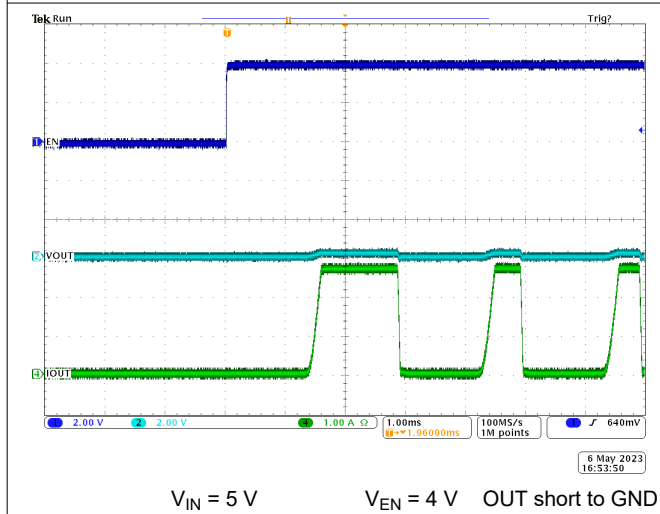
8.2.3 Application Curves



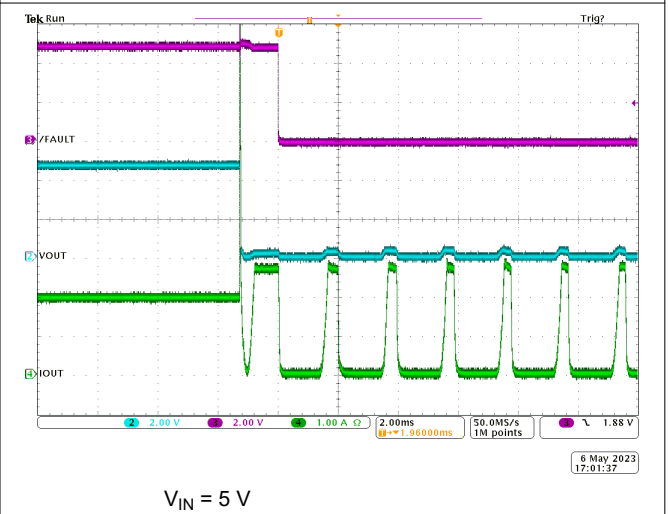
8-2. Turnon Delay and Rise Time



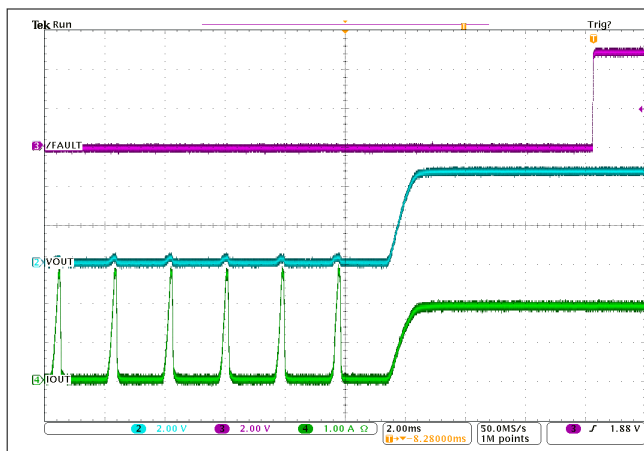
8-3. Turnoff Delay and Fall Time



8-4. TPS2001E Enable into Output Short

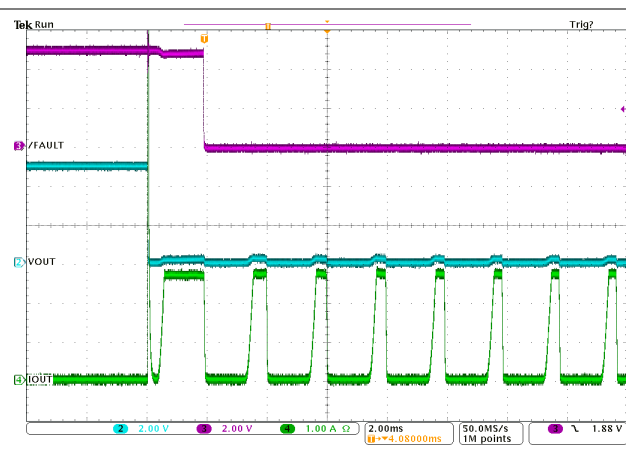


8-5. TPS2001E Full Load to Output Short



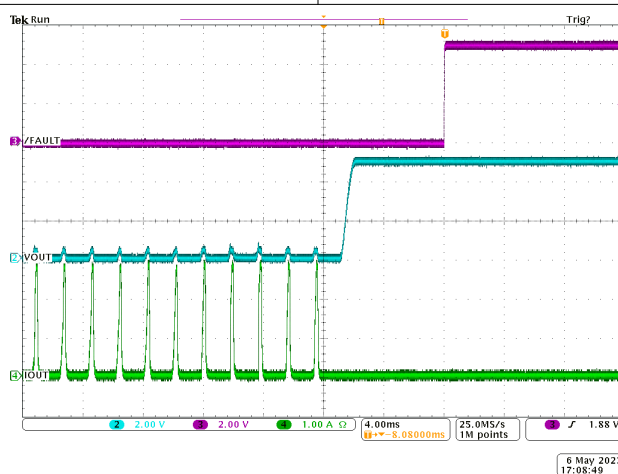
$V_{IN} = 5\text{ V}$

8-6. TPS2001E Output Short to Full Load



$V_{IN} = 5\text{ V}$

8-7. TPS2001E No Load to Output Short



$V_{IN} = 5\text{ V}$

8-8. TPS2001E Output Short to No Load

8.3 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 2.7 V to 5.5 V. The current capability of the power supply should exceed the maximum current limit of the power switch.

8.4 Layout

8.4.1 Layout Guidelines

1. Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low inductance trace.
2. Place at least 10- μF low ESR ceramic capacitor near the OUT and GND pins, and make the connections using a low inductance trace.
3. The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

8.4.2 Layout Example

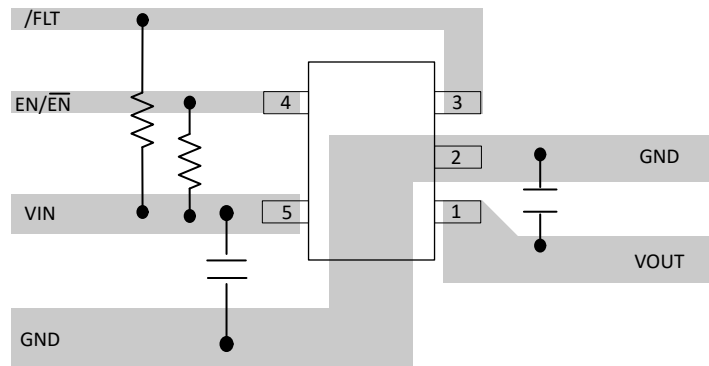


図 8-9. Recommended Layout - DBV

- Via to Bottom Layer Signal Ground Plane
- Via to Bottom Layer Signal

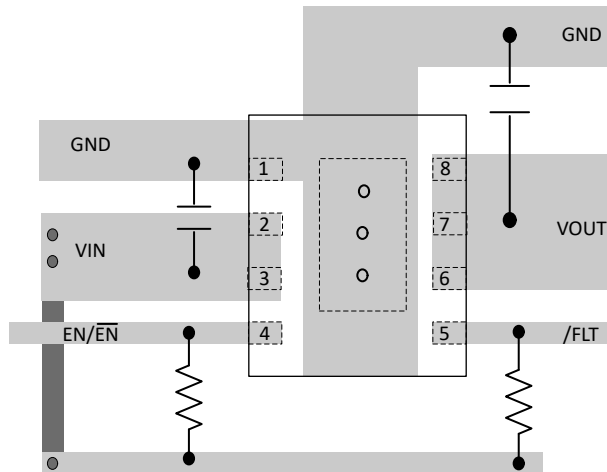


図 8-10. Recommended Layout - DGN and DGK

9 Device and Documentation Support

9.1 Documentation Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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9.4 Trademarks

PowerPAD™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.

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9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (July 2023) to Revision B (October 2023)	Page
• Added thermal information for DGN and DGK packages.....	6
• Updated enable high-level input voltage for TPS2001E.....	6

Changes from Revision * (May 2023) to Revision A (July 2023)	Page
• デバイスのステータスを「事前情報」から「量産データ」に変更.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS2001EDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS2068EDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS2069EDBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS2000EDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2000E	Samples
TPS2000EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	000E	Samples
TPS2000EDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2000E	Samples
TPS2001EDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2001E	Samples
TPS2001EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	001E	Samples
TPS2001EDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2001E	Samples
TPS2068EDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2068E	Samples
TPS2068EDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2068E	Samples
TPS2069EDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2069E	Samples
TPS2069EDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2069E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2000EDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2000EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2000EDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001EDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2001EDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2001EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001EDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2068EDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2068EDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2069EDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2069EDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2069EDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2000EDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2000EDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
TPS2000EDGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS2001EDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2001EDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2001EDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
TPS2001EDGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS2068EDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2068EDGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS2069EDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2069EDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2069EDGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0

GENERIC PACKAGE VIEW

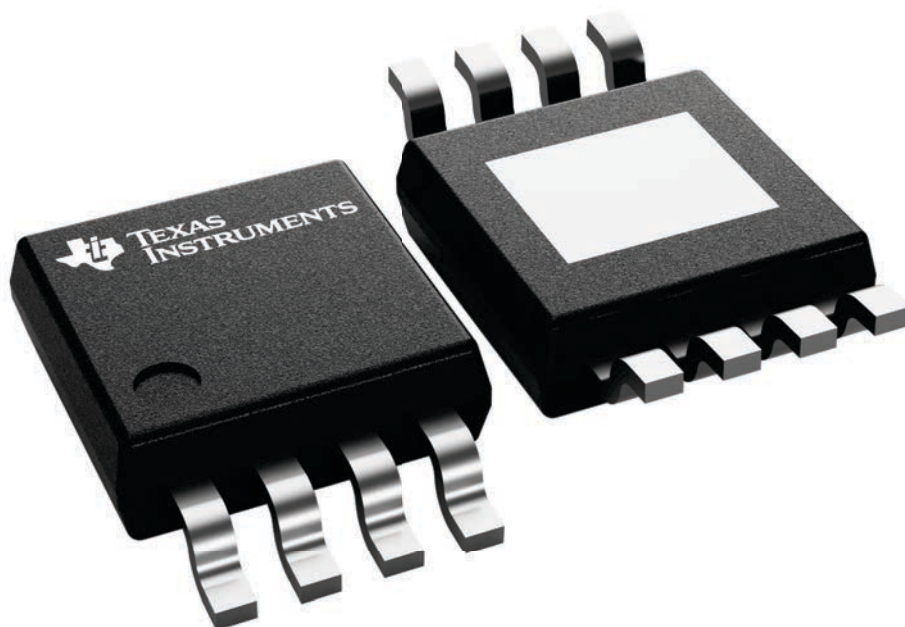
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



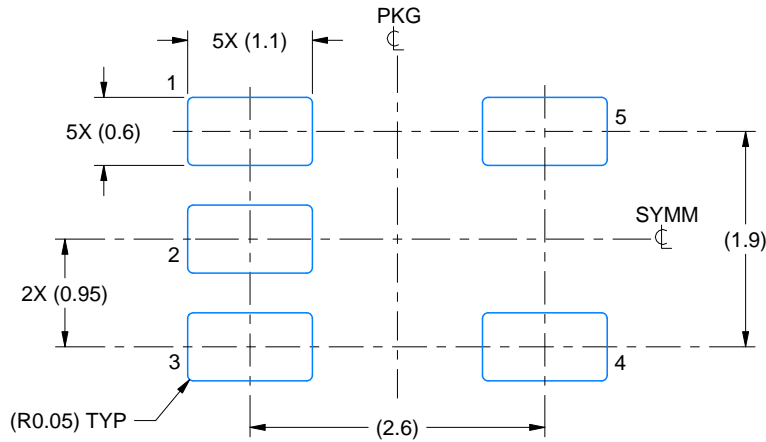
4225482/B

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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