

TPS22930 超小型、低オン抵抗ロード・スイッチ、ターンオン制御付

1 特長

- シングル・チャンネル負荷スイッチを内蔵
- 超小型 4 端子ウェハー・チップ・スケール・パッケージ (詳細は、標準寸法が示された付録を参照)
 - 0.9mm × 0.9mm、0.5mm ピッチ、0.5mm 高さ (YZV)
- 入力電圧範囲: 1.4V~5.5V
- 極小 R_{ON} 抵抗
 - $R_{ON} = 35\text{ m}\Omega$ ($V_{IN} = 5\text{ V}$ の場合)
 - $R_{ON} = 36\text{ m}\Omega$ ($V_{IN} = 3.6\text{ V}$ の場合)
 - $R_{ON} = 49\text{ m}\Omega$ ($V_{IN} = 1.8\text{ V}$ の場合)
- 連続スイッチ電流: 最大 2A
- 低静止電流: ($< 3\mu\text{A}$)
- 低制御入力スレッショルドのため、1.2V、1.8V、2.5V、3.3V ロジックを使用可能
- スルーレート制御
- 低電圧ロックアウト
- 逆電流ブロック(ディセーブル時)

2 アプリケーション

- スマートフォン/ワイヤレス・ハンドセット
- 携帯型 産業用/医療用 装置
- ポータブル・メディア・プレーヤ
- POS 端末
- GPS ナビゲーション機器
- デジタル・カメラ
- ポータブル計測装置

3 概要

TPS22930 は、ターンオン制御機能を搭載した、小型で低オン抵抗 (R_{ON}) のロード・スイッチです。このデバイスには、1.4V~5.5V の入力電圧範囲で動作する P チャンネル MOSFET が内蔵されています。本スイッチはオン/オフ入力 (ON) で制御され、低電圧制御信号と直接接続できます。TPS22930 はアクティブ HIGH イネーブルです。

TPS22930 デバイスは、逆電圧(逆電流とも呼ばれる)状況においてボディ・ダイオードを無効にすることでサーキット・ブレーカ機能を提供します。逆電流保護がアクティブになるのは、パワー・スイッチがディセーブル(オフ)になっているときのみです。デバイスは、出力電圧 (V_{OUT}) が入力 (V_{IN}) よりも高い値に駆動されているときにボディ・ダイオードを解除し、スイッチの入力側に流れる電流を停止します。さらに、低電圧誤動作防止 (UVLO) 保護機能により、入力電圧が低くなりすぎた場合はスイッチがオフになります。

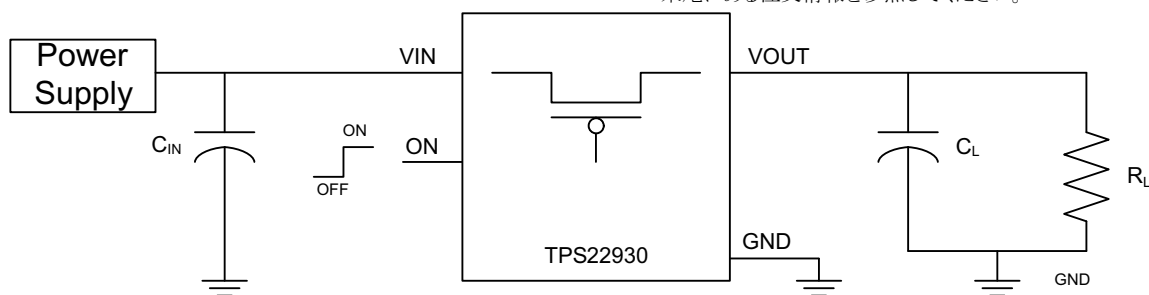
突入電流を回避するため、デバイスのスルーレートは内部的に制御されます。

TPS22930 は極小で省スペースの 4 ピン CSP パッケージで提供され、気温 -40°C ~ 85°C の範囲に渡って動作することが特長です。

製品情報(1)

部品番号	パッケージ	本体サイズ(最大)
TPS22930	DSBGA (4)	0.92 mm × 0.92 mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2021) to Revision D (July 2021)	Page
• Updated I _{RCP(leak)} spec to 2.6 μA.....	5
Changes from Revision B (February 2016) to Revision C (January 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
Changes from Revision A (June 2015) to Revision B (February 2016)	Page
• <i>ピン構成および機能を変更</i>	1
Changes from Revision * (November 2012) to Revision A (June 2015)	Page
• 「注文情報」表を削除.....	1
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Input voltage	-0.3	6	V
V _{OUT}	Output voltage	-0.3	6	V
V _{ON}	Input voltage	-0.3	6	V
I _{MAX}	Maximum continuous switch current		2	A
I _{PLS}	Maximum pulsed switch current, pulse ≤1ms, 25% duty cycle		2.5	A
T _A	Operating free-air temperature ⁽³⁾	-40	85	°C
T _J	Maximum junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A(max)} = T_{J(max)} - (R_{θJA} × P_{D(max)})

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input voltage range		1.4	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range		0	V _{IN}	V
V _{IH}	High-level input voltage, ON	V _{IN} = 3.61 V to 5.5 V	1.1	5.5	V
		V _{IN} = 1.4 V to 3.6 V	1.1	5.5	
V _{IL}	Low-level input voltage, ON	V _{IN} = 3.61 V to 5.5 V	0	0.6	V
		V _{IN} = 1.4 V to 3.6 V	0	0.4	
C _{IN}	Input capacitor		1 ⁽¹⁾		μF

- (1) Refer to *Application Information* section.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22930	UNIT
		YZV (DSBGA)	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

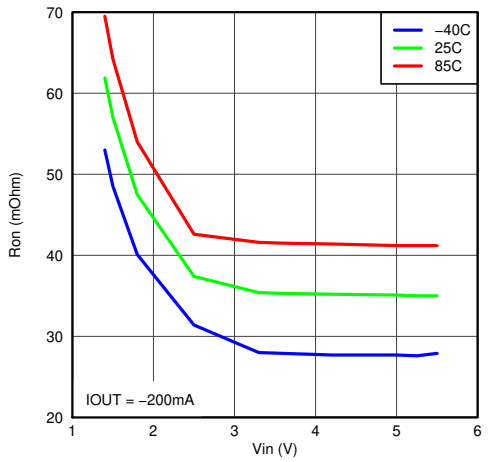
Unless otherwise note, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (Full). Typical values are for $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
I_{IN}	Quiescent current	$I_{OUT} = 0\text{ V}, V_{IN} = V_{ON} = 5.25\text{ V}$	Full		2.3	10	μA
		$I_{OUT} = 0\text{ V}, V_{IN} = V_{ON} = 4.2\text{ V}$			2.2	7	
		$I_{OUT} = 0\text{ V}, V_{IN} = V_{ON} = 3.6\text{ V}$			2.1	7	
		$I_{OUT} = 0\text{ V}, V_{IN} = V_{ON} = 2.5\text{ V}$			1.0	5	
		$I_{OUT} = 0\text{ V}, V_{IN} = V_{ON} = 1.5\text{ V}$			0.8	5	
$I_{IN(off)}$	Off supply current	$V_{OUT} = \text{Open}, V_{IN} = 5.25\text{ V}, V_{ON} = 0\text{ V}$	Full		0.3	10	μA
		$V_{OUT} = \text{Open}, V_{IN} = 4.2\text{ V}, V_{ON} = 0\text{ V}$			0.2	7	
		$V_{OUT} = \text{Open}, V_{IN} = 3.6\text{ V}, V_{ON} = 0\text{ V}$			0.2	7	
		$V_{OUT} = \text{Open}, V_{IN} = 2.5\text{ V}, V_{ON} = 0\text{ V}$			0.1	5	
		$V_{OUT} = \text{Open}, V_{IN} = 1.5\text{ V}, V_{ON} = 0\text{ V}$			0.1	5	
$I_{IN(Leak)}$	Leakage current	$V_{OUT} = 0\text{ V}, V_{IN} = 5.25\text{ V}, V_{ON} = 0\text{ V}$	Full		0.8	10	μA
		$V_{OUT} = 0\text{ V}, V_{IN} = 4.2\text{ V}, V_{ON} = 0\text{ V}$			0.2	7	
		$V_{OUT} = 0\text{ V}, V_{IN} = 3.6\text{ V}, V_{ON} = 0\text{ V}$			0.2	7	
		$V_{OUT} = 0\text{ V}, V_{IN} = 2.5\text{ V}, V_{ON} = 0\text{ V}$			0.1	5	
		$V_{OUT} = 0\text{ V}, V_{IN} = 1.5\text{ V}, V_{ON} = 0\text{ V}$			0.1	5	
I_{ON}	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	Full			0.5	μA
$I_{RCP(Leak)}$	Reverse leakage current	$V_{IN} = V_{ON} = \text{GND}, V_{OUT} = 5\text{ V},$ measured from V_{IN}	Full			2.6	
UVLO	Undervoltage lockout	V_{IN} increasing, $V_{ON} = 3.6\text{ V}, I_{OUT} = -100\text{ mA}$	Full			1.2	
		V_{IN} decreasing, $V_{ON} = 3.6\text{ V}, I_{OUT} = -100\text{ mA}$			0.5		
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance	$I_{OUT} = -200\text{ mA}$	$V_{IN} = 5.0\text{ V}$	25°C	35	44	$\text{m}\Omega$
				Full		50	
			$V_{IN} = 4.2\text{ V}$	25°C	35	44	
				Full		50	
			$V_{IN} = 3.6\text{ V}$	25°C	36	44	
				Full		50	
			$V_{IN} = 2.5\text{ V}$	25°C	39	44	
				Full		50	
			$V_{IN} = 1.8\text{ V}$	25°C	49	55	
				Full		62	
			$V_{IN} = 1.5\text{ V}$	25°C	59	66	
				Full		74	

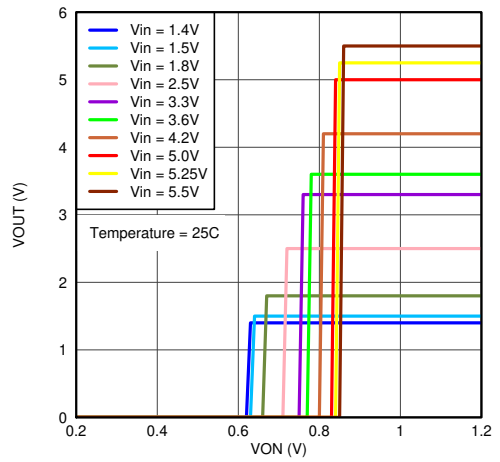
5.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5.5 V, T_A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		4.8		μs
t _{OFF}	Turn-off time			6.3		
t _R	V _{OUT} rise time			5.6		
t _F	V _{OUT} fall time			2.8		
V_{IN} = 4.2 V, T_A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		5.8		μs
t _{OFF}	Turn-off time			7.3		
t _R	V _{OUT} rise time			5.4		
t _F	V _{OUT} fall time			2.8		
V_{IN} = 3.0 V, T_A = 25°C (unless otherwise noted)						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF		7.4		μs
t _{OFF}	Turn-off time			9.5		
t _R	V _{OUT} rise time			6.3		
t _F	V _{OUT} fall time			2.9		

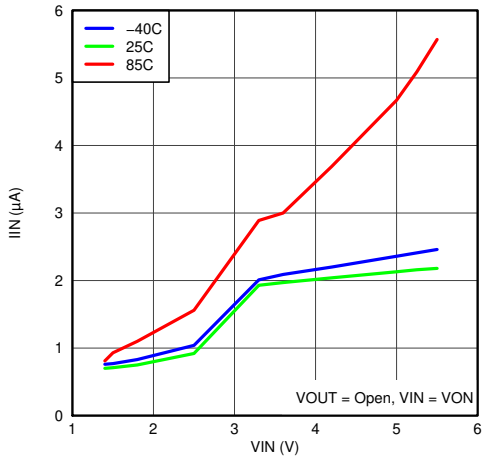
5.7 Typical Characteristics



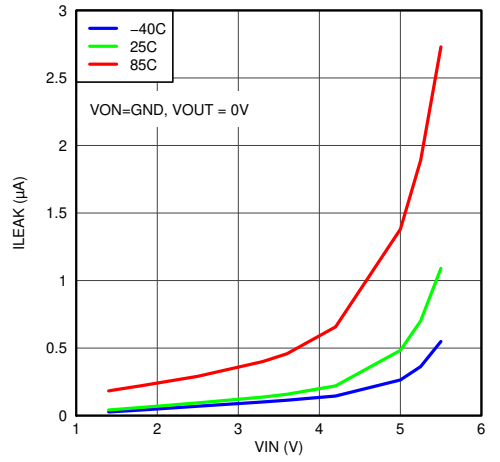
5-1. R_{ON} vs V_{IN}



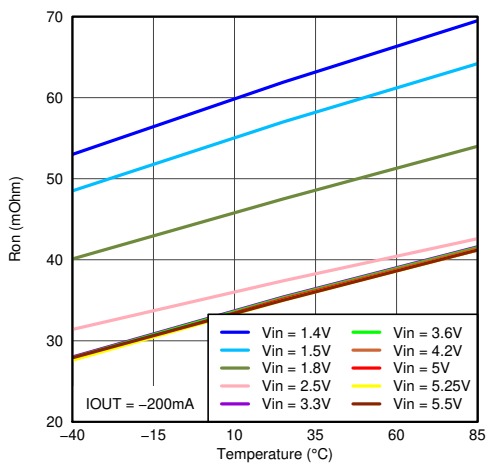
5-2. On Input Threshold



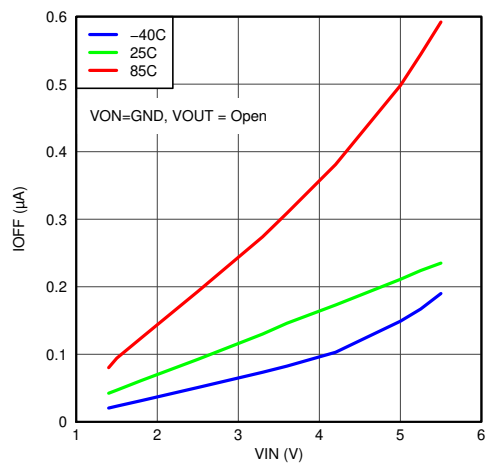
5-3. I_{IN} vs V_{IN}



5-4. $I_{IN(\text{leak})}$ vs V_{IN}

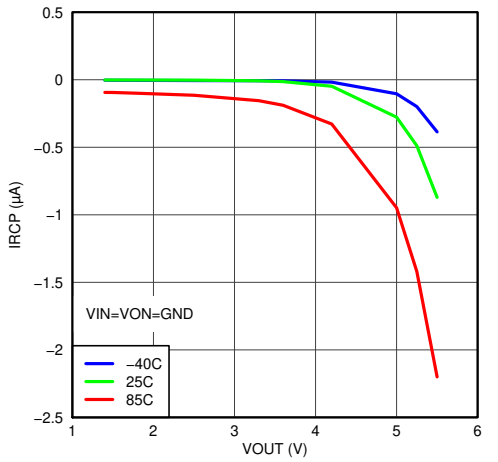


5-5. Temperature vs R_{ON}

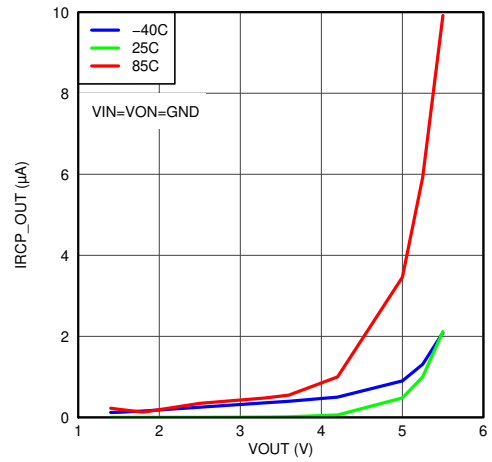


5-6. $I_{IN(\text{off})}$ vs V_{IN}

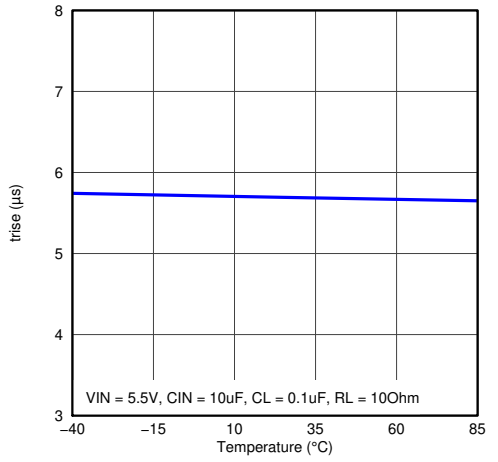
5.7 Typical Characteristics (continued)



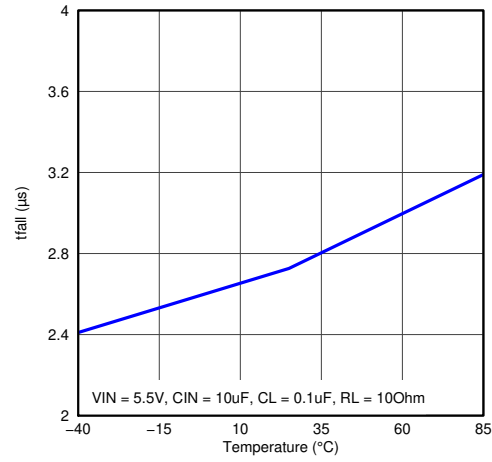
5-7. $I_{RCP(Leak)}$ vs V_{OUT} (Measured On V_{IN})



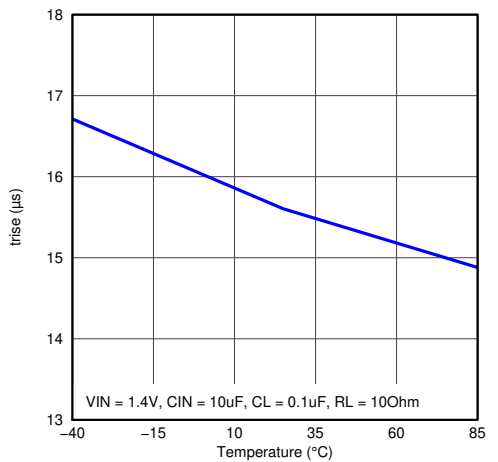
5-8. $I_{RCP(Leak)}$ vs V_{OUT} (Measured on V_{OUT})



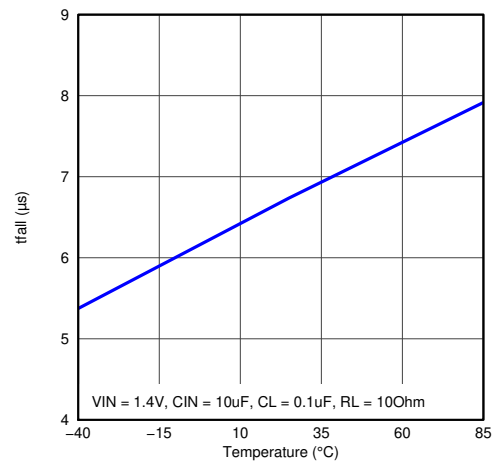
5-9. t_R vs Temperature ($V_{IN} = 5.5 V$)



5-10. t_F vs Temperature ($V_{IN} = 5.5 V$)



5-11. t_R vs Temperature ($V_{IN} = 1.4 V$)



5-12. t_F vs Temperature ($V_{IN} = 1.4 V$)

5.7 Typical Characteristics (continued)

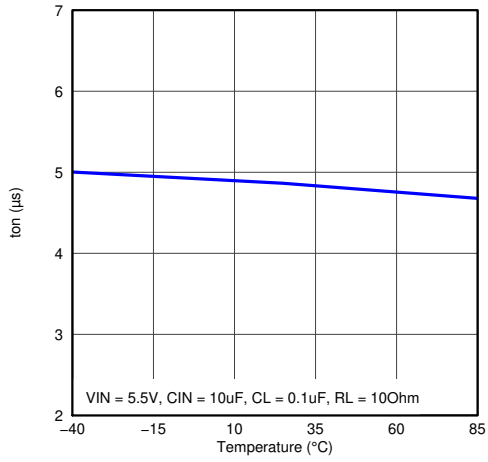


图 5-13. t_{ON} vs Temperature (V_{IN} = 5.5 V)

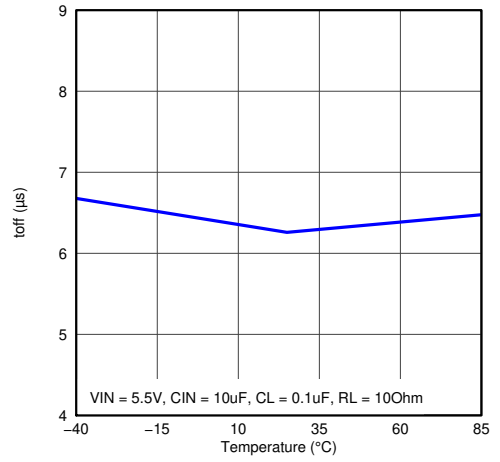


图 5-14. t_{OFF} vs Temperature (V_{IN} = 5.5 V)

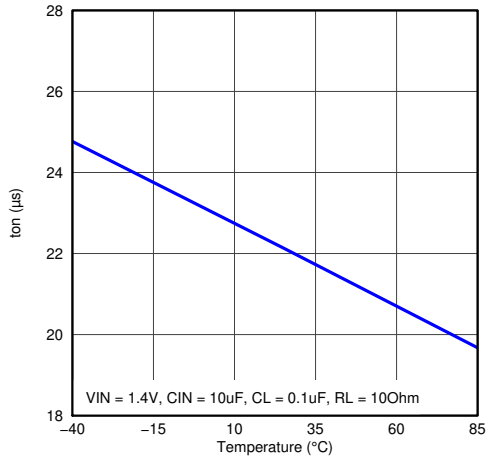


图 5-15. t_{ON} vs Temperature (V_{IN} = 1.4 V)

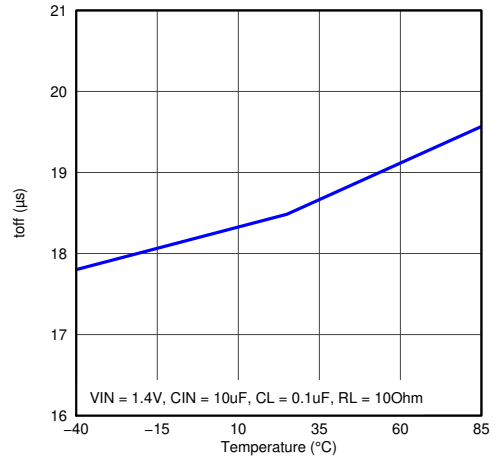


图 5-16. t_{OFF} vs Temperature (V_{IN} = 1.4 V)

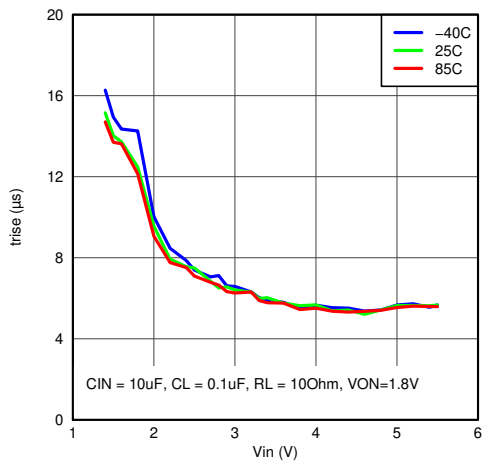
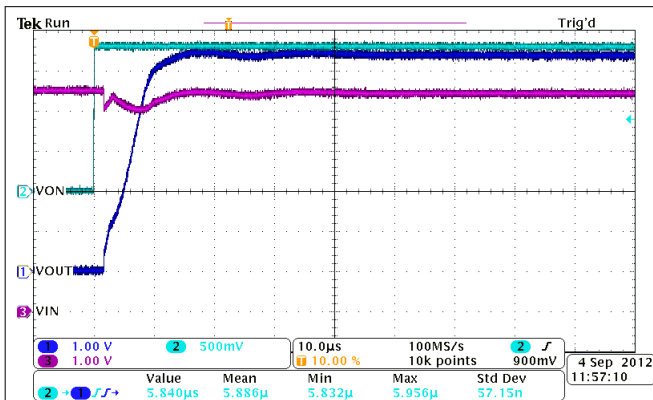
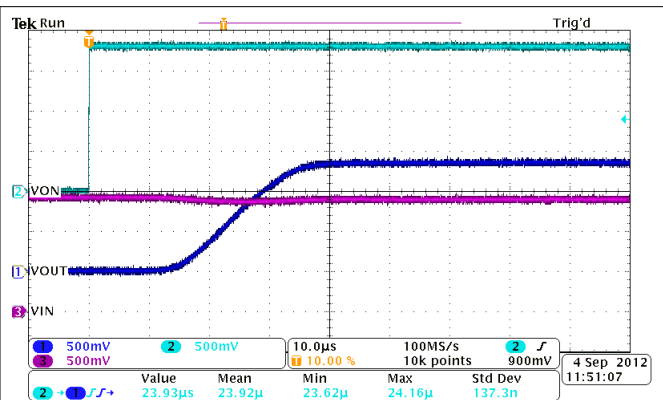


图 5-17. t_R vs V_{IN}

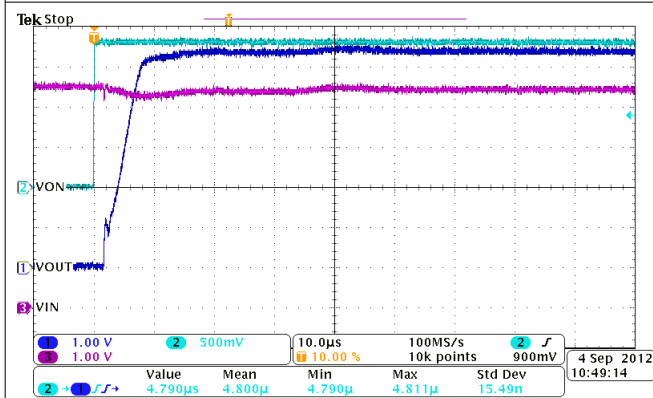
5.7.1 Typical AC Scope Captures at $T_A = 25^\circ\text{C}$



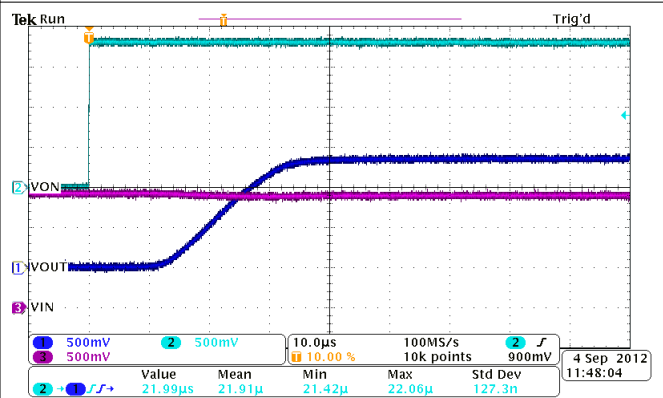
5-18. Turn-On Response Time ($V_{IN} = 5.5\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_L = 1\ \mu\text{F}$, $R_L = 10\ \Omega$)



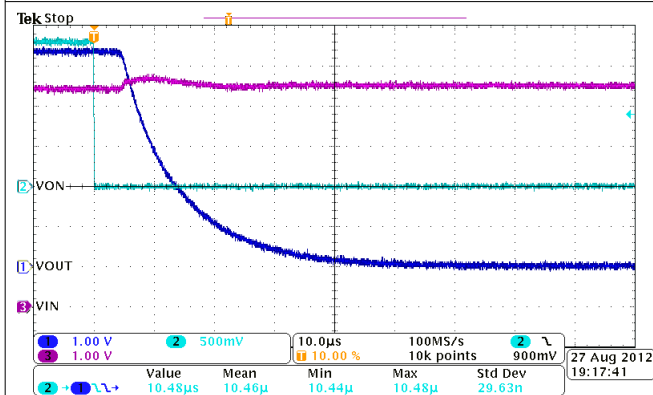
5-19. Turn-On Response Time ($V_{IN} = 1.4\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_L = 1\ \mu\text{F}$, $R_L = 10\ \Omega$)



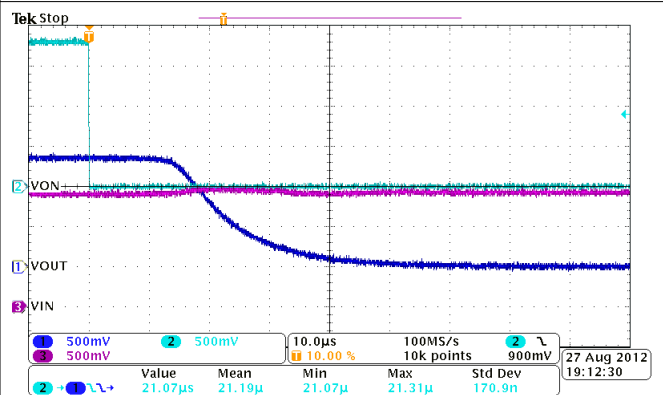
5-20. Turn-On Response Time ($V_{IN} = 5.5\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$)



5-21. Turn-On Response Time ($V_{IN} = 1.4\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$)

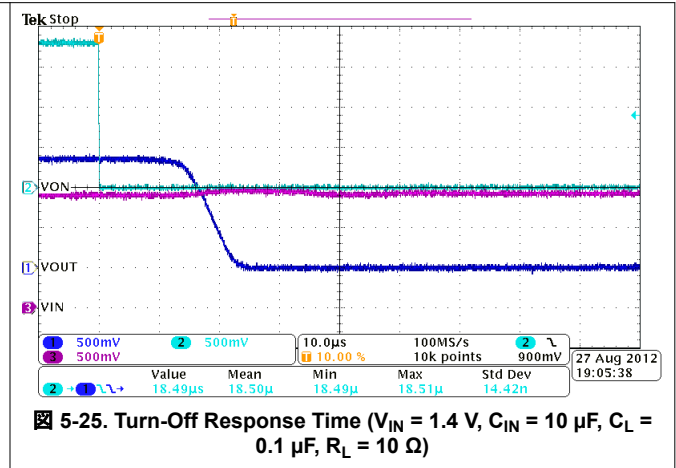
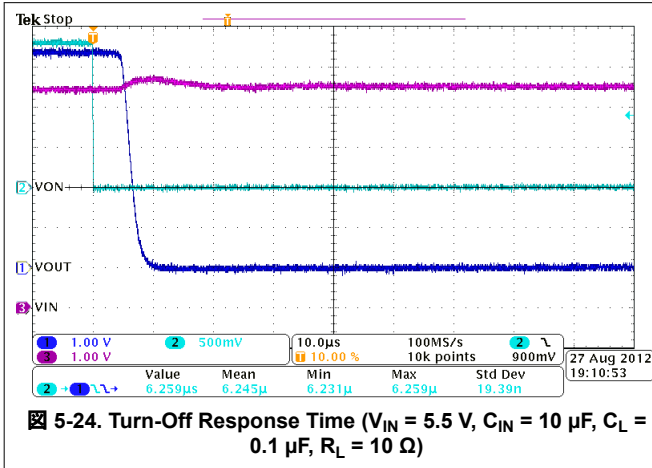


5-22. Turn-Off Response Time ($V_{IN} = 5.5\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_L = 1\ \mu\text{F}$, $R_L = 10\ \Omega$)



5-23. Turn-Off Response Time ($V_{IN} = 1.4\text{ V}$, $C_{IN} = 10\ \mu\text{F}$, $C_L = 1\ \mu\text{F}$, $R_L = 10\ \Omega$)

5.7.1 Typical AC Scope Captures at $T_A = 25^\circ\text{C}$ (continued)



6 Pin Configuration and Functions

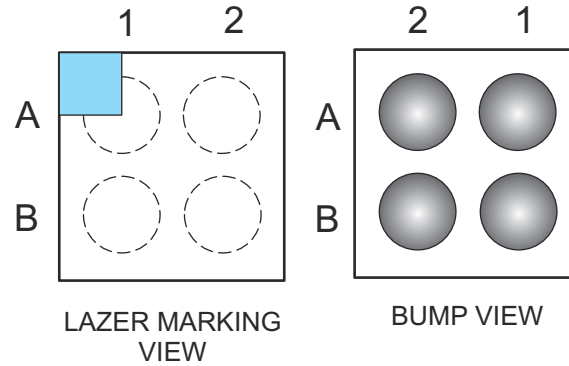


图 6-1. YZV Package 4-Pin DSBGA Bottom View

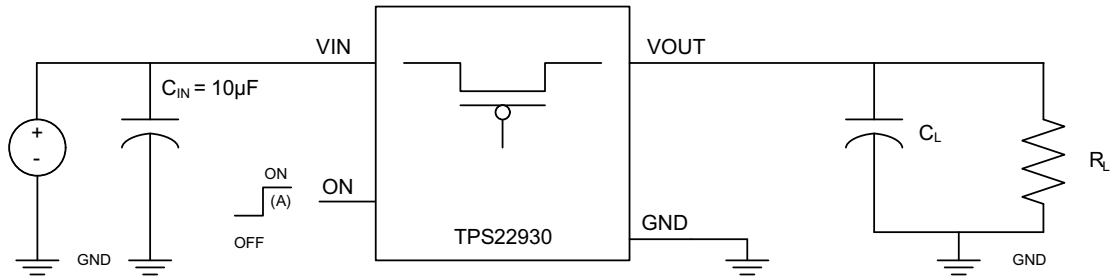
表 6-1. Pin Assignments

A	VOUT	VIN
B	GND	ON
	1	2

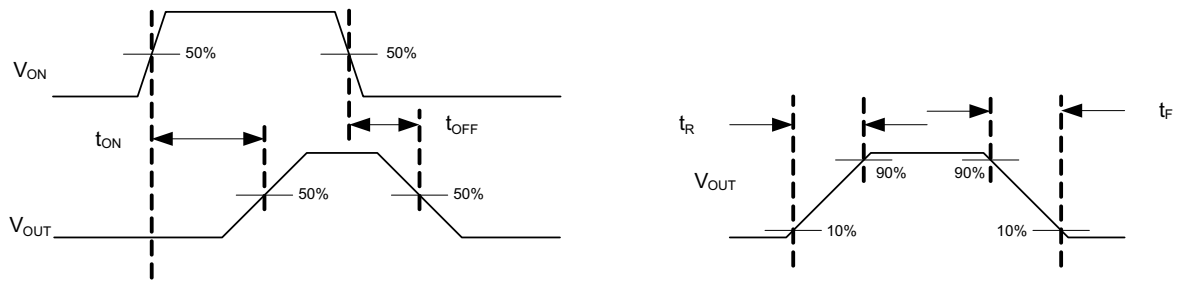
表 6-2. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	VOUT	O	Switch output.
A2	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip during transients.
B1	GND	–	Device ground.
B2	ON	I	Switch control input, active high. Do no leave floating.

7 Parameter Measurement Information



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

(A) Rise and fall times of the control signal are 100ns.

7-1. Test Circuit and t_{ON}/t_{OFF} Waveforms

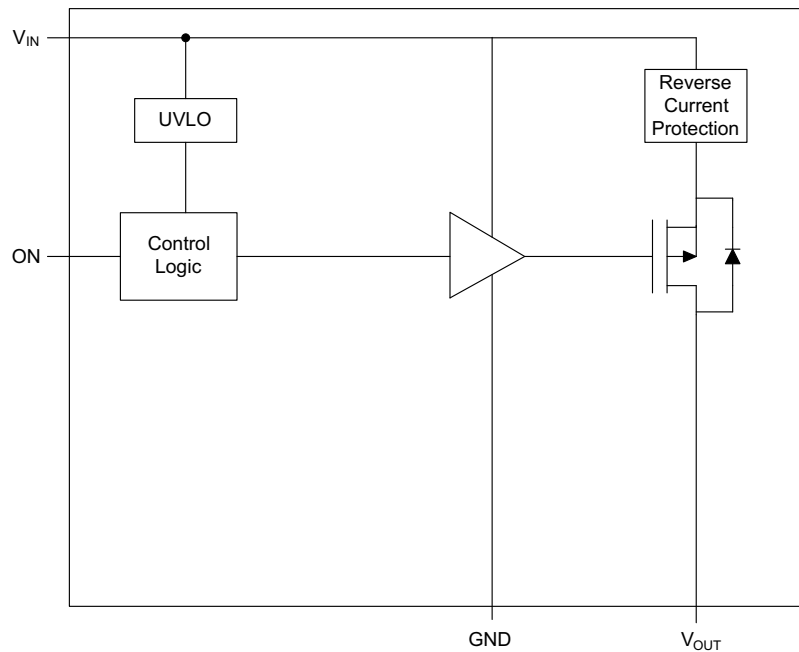
8 Detailed Description

8.1 Overview

The TPS22930 is a single channel, 2-A load switch in a 4-terminal BSGA package. A low enable threshold makes it capable of interfacing directly with low voltage control signals. In the off state, the device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. When turning on, the output will rise with a controlled slew rate to limit inrush current.

The device will also disengage the body diode when disabled to provide reverse current protection. The undervoltage lockout (UVLO) threshold will ensure the switch is turned off and will block reverse current if the V_{IN} power supply is removed.

8.2 Functional Block Diagram



8.3 Feature Description

表 8-1. Feature List

DEVICE	R_{ON} (TYP) AT 4.2 V	RISE TIME AT 4.2 V (TYP)	QUICK OUTPUT DISCHARGE ⁽¹⁾	MAXIMUM CONTINUOUS CURRENT	ENABLE
TPS22930A	35 mΩ	5.4 μs	No	2 A	Active High

(1) This feature discharges output of the switch to GND through a resistor, preventing the output from floating when the pass FET is disabled.

8.3.1 On And Off Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher GPIO voltage.

8.3.2 UVLO

UVLO turns off the switch if the input voltage drops below the under voltage lockout threshold. With the ON pin active, the input voltage rising above the under voltage lockout threshold will allow a controlled turn-on of the switch to limit current over-shoot.

The maximum UVLO of the TPS22930A is 1.2 V. This is under the minimum V_{IN} voltage and meets the system UVLO requirements. Once the device is disabled through UVLO, it will block reverse current in the case a voltage is applied to V_{OUT}

8.3.3 Reverse Current Protection

Reverse current protection (RCP) is only active when ON is asserted low. When ON is asserted high, current can flow from V_{OUT} to V_{IN} or from V_{IN} to V_{OUT} . This allows the device to function as a bi-directional switch when enabled.

8.4 Device Functional Modes

表 8-2 describes the state of the switch and the reverse current protection as determined by the ON pin.

表 8-2. Switch and Reverse Current Protection State

ON	V_{IN} to V_{Out}	RCP
H	On	Off
L	Off	On

9 Application and Implementation

Note

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9.1 Application Information

9.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, it is recommended that a capacitor be placed between V_{IN} and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 100 times higher than the output capacitor to avoid excessive voltage drop; however, a 100 to 1 ratio is not required for proper functionality of the device.

9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 100 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 100 to 1 ratio is not required for proper functionality of the device.

9.2 Typical Application

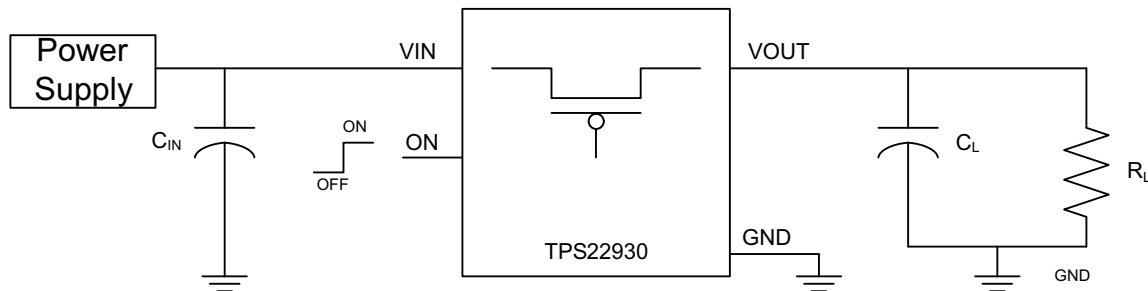


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

For this design example, the following will be used as the system requirements.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN} Range	1.5 V to 5.5 V
UVLO Threshold	< 1.5 V
Reverse Current Protection	Required
Load Current	1 A
Ambient Temperature	25 °C

9.2.2 Detailed Design Procedure

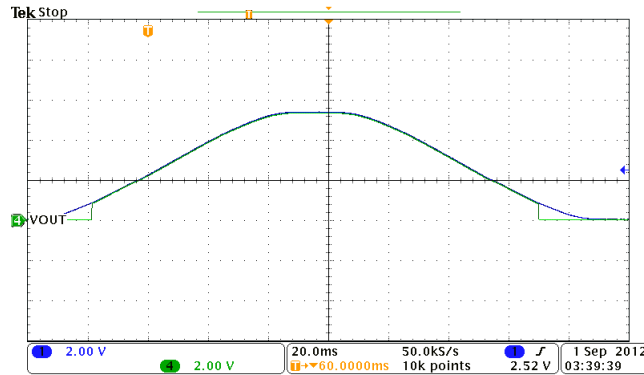
To begin the design process, the designer needs to know the following:

- Input Voltage range
- UVLO Threshold
- Load Current

- Ambient Temperature

9.2.3 Application Curve

Figure 9-2 shows the UVLO response when the device is enabled.



ON = 5 V

Figure 9-2. UVLO Response

10 Power Supply Recommendations

The device is designed to operate from a V_{IN} range of 1.5 V to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

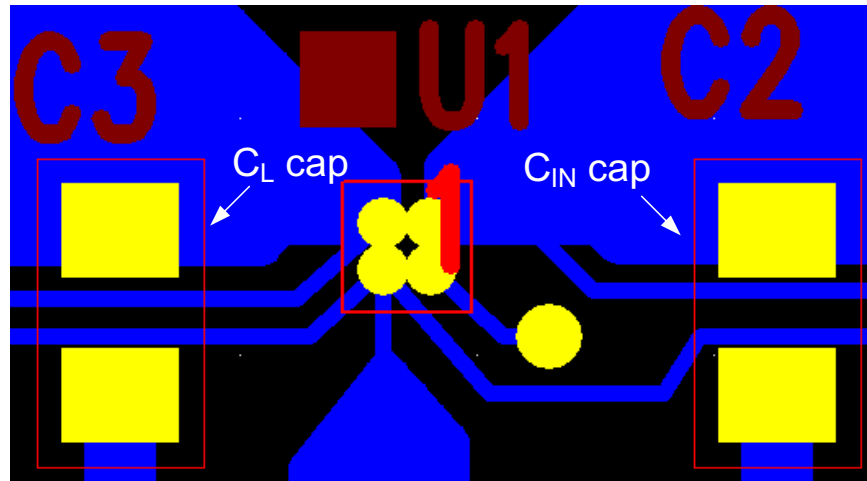
11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The ON pin cannot be left floating and must be driven either high or low for proper functionality.

Figure 11-1 shows an example of a layout.

11.2 Layout Example



☒ 11-1. Layout Recommendation

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (1)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22930)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See [Thermal Information](#) table. This parameter is highly dependent upon board layout.

The power dissipated by the device depends on the R_{ON} of the device at a given V_{IN} . To calculate the amount of power being dissipated by the device, use the following equation:

$$P_{IR} = I^2 \times R_{ON} \quad (2)$$

where

- P_{IR} = power dissipated by the device
- I = load current in amperes
- R_{ON} = resistance of the device in Ohms at a given V_{IN} (see [Electrical Characteristics](#) table)

The result from 式 2 should always be less than or equal to the result from 式 1.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

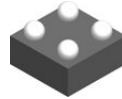
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

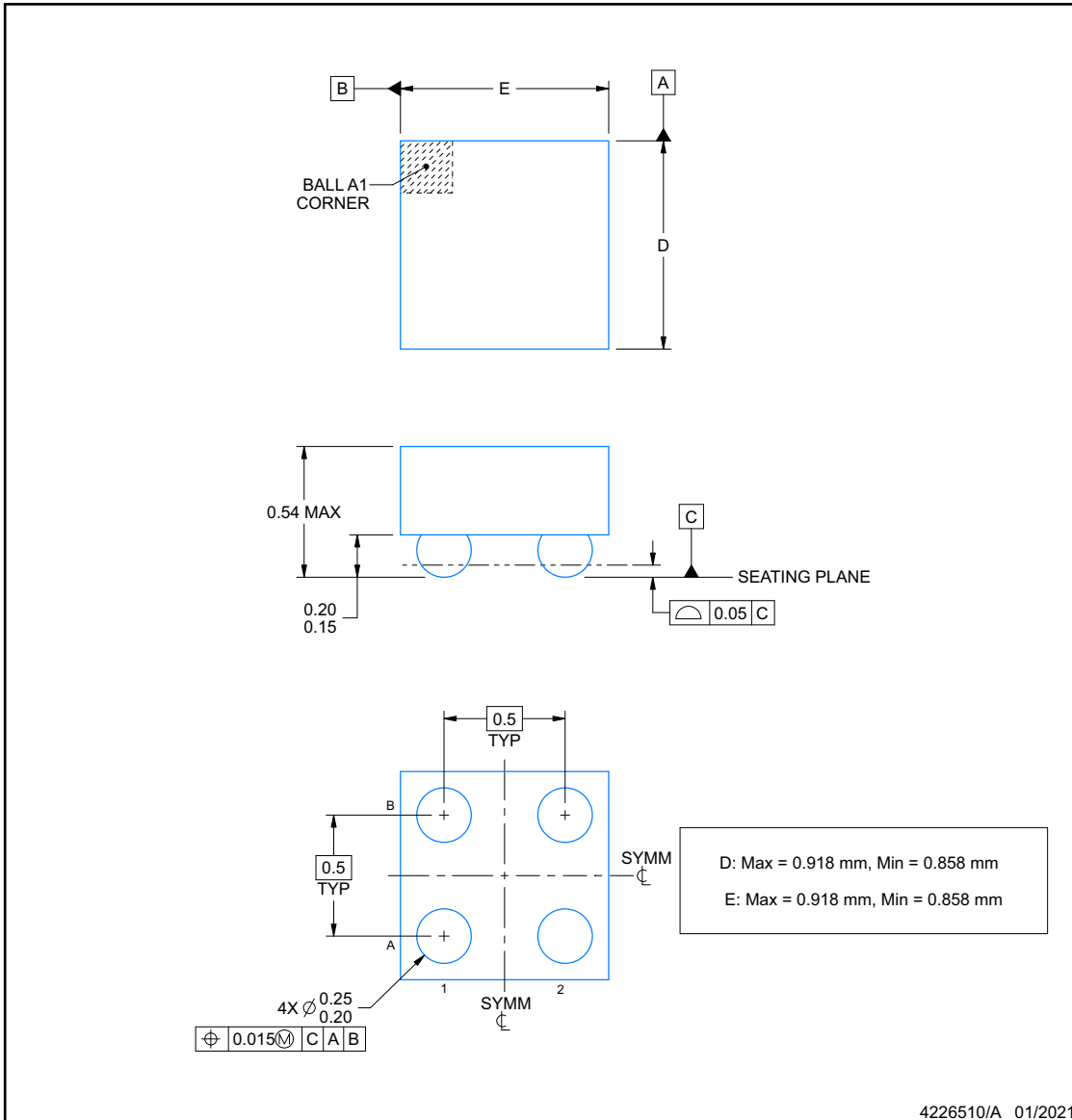
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



YZV0004-C01

PACKAGE OUTLINE
DSBGA - 0.54 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

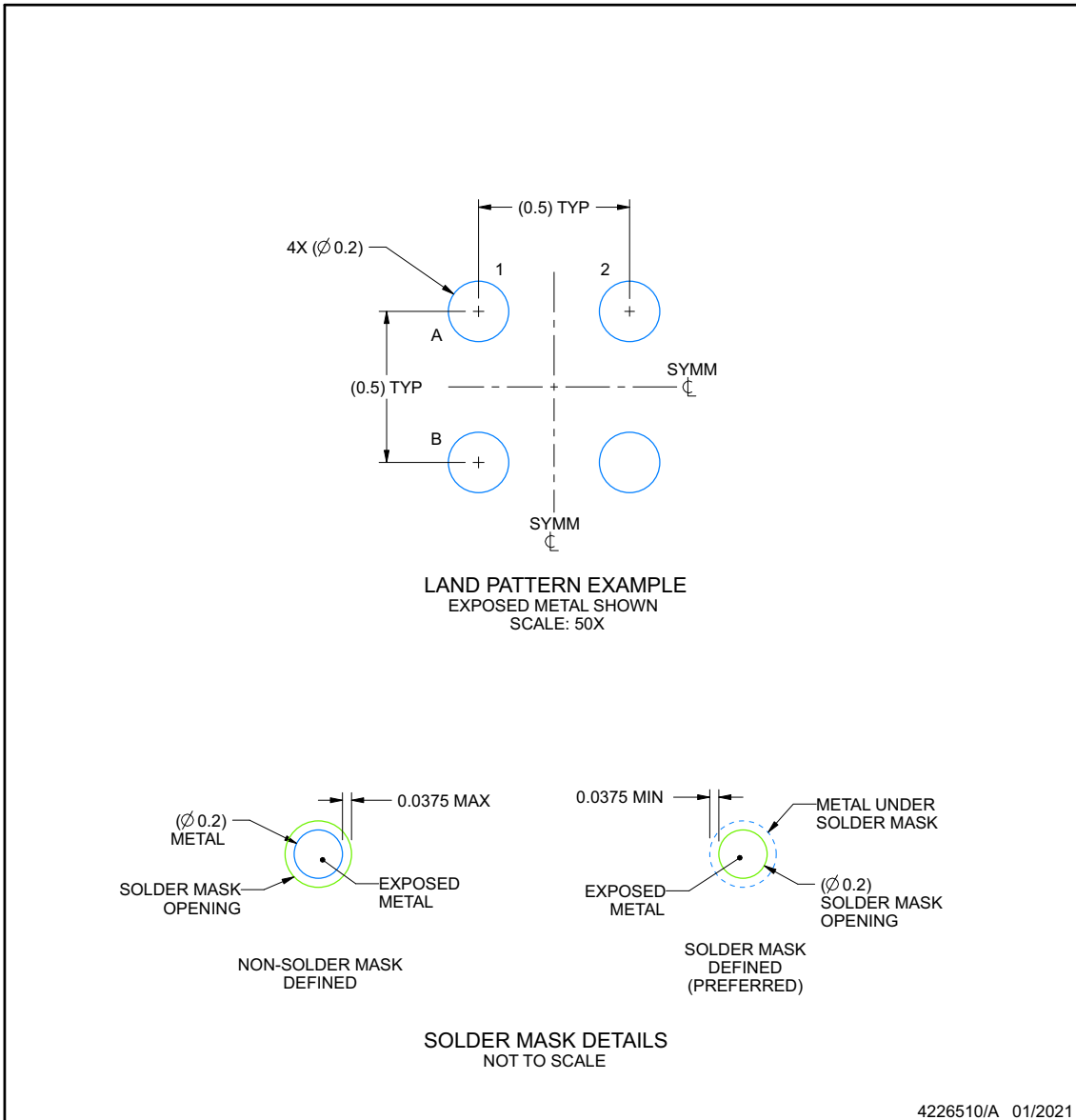
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZV0004-C01

DSBGA - 0.54 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

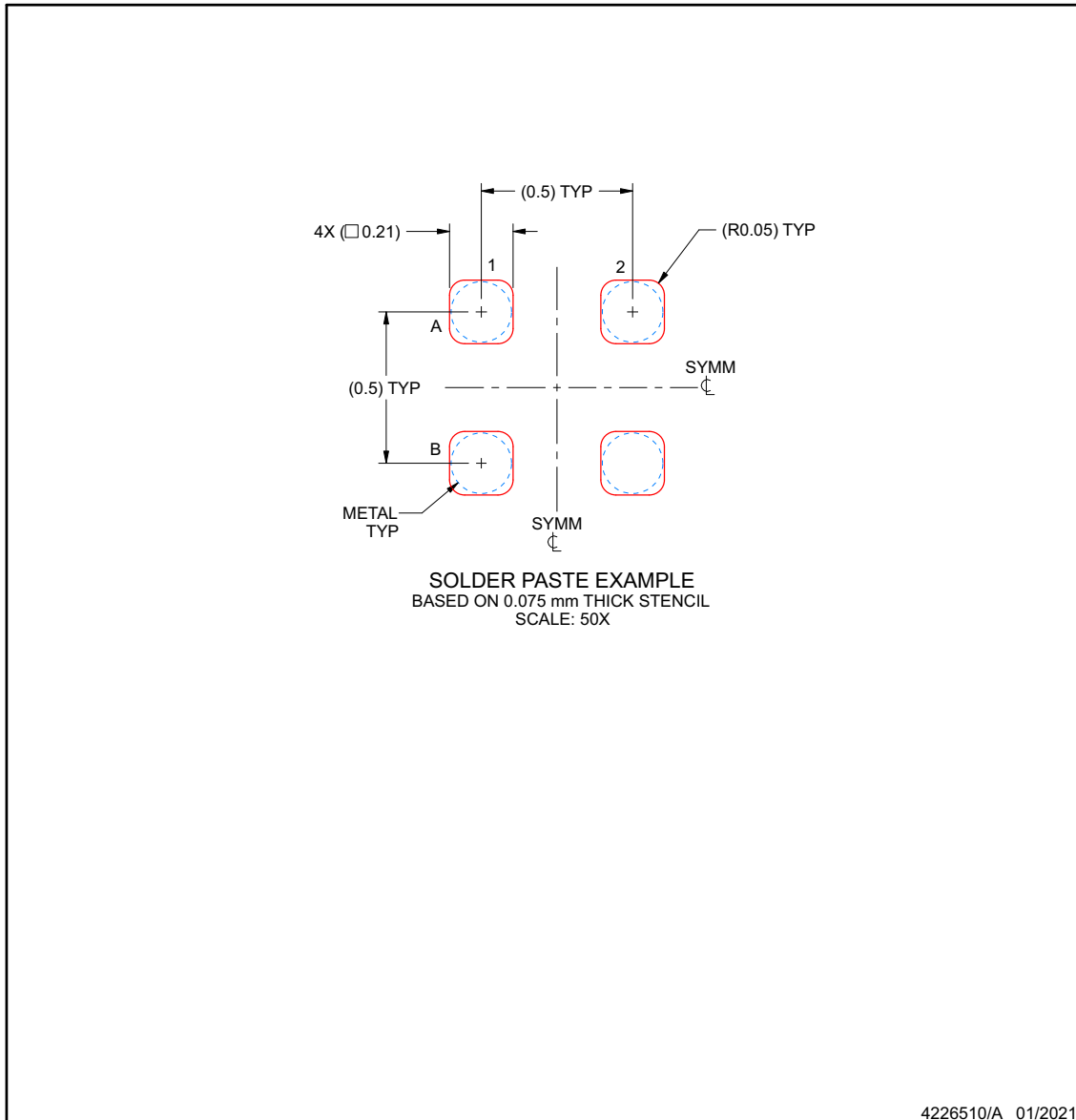
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZV0004-C01

DSBGA - 0.54 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22930AYZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q	Samples
TPS22930AYZVT	ACTIVE	DSBGA	YZV	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22930AYZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1
TPS22930AYZVT	DSBGA	YZV	4	250	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22930AYZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0
TPS22930AYZVT	DSBGA	YZV	4	250	182.0	182.0	20.0

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