TPS22966-Q1 2 チャネル、超低抵抗ロード・スイッチ

1 特長

- 車載アプリケーション用に認定済み
- 下記内容でAEC-Q100認定済み
  - デバイス温度グレード2: 動作時周囲温度範囲 –40°C～105°C
  - デバイスHBM ESD分類レベルH1C
  - デバイスCDM ESD分類レベルC6
- 統合型デュアル・チャネル負荷スイッチ
- 入力電圧範囲: 0 V～5.5V
- 極めて小さいオン抵抗 (R_{ON})
  - V_{IN} = 5V (V_{BIAS} = 5V) で R_{ON} = 16mΩ
  - V_{IN} = 3.3V (V_{BIAS} = 5V) で R_{ON} = 16mΩ
  - V_{IN} = 1.8V (V_{BIAS} = 5V) で R_{ON} = 16mΩ
- チャネルごとの最大連続スイッチ電流：4A
- 低静止電流
  - 80µA (デュアル・チャネル)
  - 80µA (シングル・チャネル)
- 制御入力スレッショルドが低いため 1.2V、1.8V、2.5V、3.3V ロジックを使用可能
- 立ち上がり時間を構成可能
- クイック出力放電 (QOD)
- サーマル・パッド付き SON 14 ピン・パッケージ

2 アプリケーション

- インフォテインメント
- ADAS (先進運転支援システム)

3 概要

TPS22966-Q1 は R_{ON} が極めて小さい、小型のデュアル・チャネル負荷スイッチで、立ち上がり時間を調整できます。0V～5.5V の入力電圧範囲で動作する 2 つの N チャネル MOSFET を内蔵しており、各チャネルで最大 4A の連続電流をサポートします。各スイッチは、低電圧制御信号と直接インターフェイス可能なオン入力とオフ入力 (ON1 および ON2) により個別に制御されます。TPS22966-Q1 は 230Ω のオンチップ抵抗を備えているため、スイッチ・オフ時のクイック出力放電が可能です。

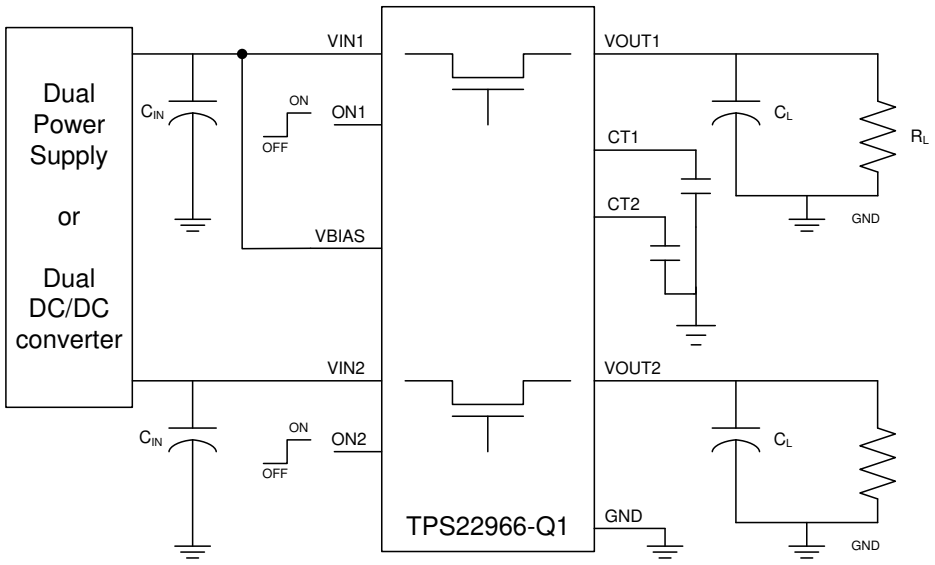
TPS22966-Q1 は、高電力に対応可能なサーマル・パッド付き、小型、省スペースの 2mm × 3mm 14-SON パッケージ (DPU) で供給されます。周囲温度–40℃～105℃での動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS22966-Q1	WSON (14)	3.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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4 改訂履歴

Revision A (March 2015) から **Revision B** に変更 **Page**

- Changed Input voltage range from 0.8 V to 0 V in the *Recommended Operating Conditions* table ... 4

2013年12月発行のものから更新 **Page**

- 「*ピン構成および機能*」セクション、「*ESD定格*」の表、「*機能概要*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

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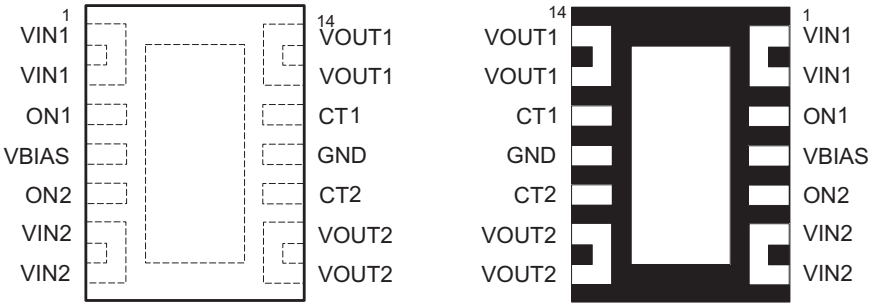
5 Pin Configuration and Functions

DPU Package
14-Pin WSON



Top View **Bottom View**

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN1	I	Switch 1 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See Application Information section for more information.
2	VIN1	I	Switch 1 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See *Application Information*for more information.
3	ON1	I	Active high switch 1 control input. Do not leave floating.
4	VBIAS	I	Bias voltage. Power supply to the device. See *Application Information* for more information.
5	ON2	I	Active high switch 2 control input. Do not leave floating.
6	VIN2	I	Switch 2 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See *Application Information* for more information.
7	VIN2	I	Switch 2 input. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See *Application Information* for more information.
8	VOUT2	O	Switch 2 output.
9	VOUT2	O	Switch 2 output.
10	CT2	O	Switch 2 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25 V for desired rise time performance.
11	GND	–	Ground
12	CT1	O	Switch 1 slew rate control. Can be left floating. Capacitor used on this pin should be rated for a minimum of 25 V for desired rise time performance.
13	VOUT1	O	Switch 1 output.
14	VOUT1	O	Switch 1 output.
15	Thermal Pad	O	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Guidelines* for layout guidelines.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage	–0.3	6	V
$V_{OUT1,2}$	Output voltage	–0.3	6	V
$V_{ON1,2}$	ON-pin voltage	–0.3	6	V
V_{BIAS}	VBIAS voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel		4	A
I_{PLS}	Maximum pulsed switch current per channel, pulse <300 µs, 2% duty cycle		6	A
T_J	Maximum junction temperature		150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage range		0	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
$V_{ON1,2}$	ON voltage range		0	5.5	V
$V_{OUT1,2}$	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1(1)		µF
T_A	Operating free-air temperature(2)		–40	105	°C

(1) Refer to *Application Information*.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

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6.4 Thermal Information

THERMAL METRIC(1)		TPS22966-Q1 DPU (WSON) 14 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	52.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	45.9	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	11.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.9	

(1) 従来および新しい熱測定値の詳細については、『*Semiconductor and IC Package Thermal Metrics*』アプリケーション・レポート (SPRA953)を参照してください。

6.5 Electrical Characteristics: V_{BIAS} = 5 V

Unless otherwise noted, the specifications apply over the operating ambient temperature, –40°C ≤ T_A ≤ 105°C (full) and V_{BIAS} = 5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 5 V		–40°C to 105°C		80	120	µA
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 5 V		–40°C to 105°C		80	120	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to 105°C			2	µA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 5 V	–40°C to 105°C		0.5	8	µA
			$V_{IN1,2}$ = 3.3 V			0.1	3	
			$V_{IN1,2}$ = 1.8 V			0.07	2	
			$V_{IN1,2}$ = 0.8 V			0.04	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to 105°C			1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance (per channel)	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		16	19	mΩ
				–40°C to 85°C			21	
				–40°C to 105°C			23	
			V_{IN} = 3.3 V	25°C		16	19	
				–40°C to 85°C			21	
				–40°C to 105°C			23	
			V_{IN} = 1.8 V	25°C		16	19	
				–40°C to 85°C			21	
				–40°C to 105°C			23	
			V_{IN} = 1.5 V	25°C		16	19	
				–40°C to 85°C			21	
				–40°C to 105°C			23	
			V_{IN} = 1.2 V	25°C		16	19	
				–40°C to 85°C			21	
				–40°C to 105°C			23	
			V_{IN} = 0.8 V	25°C		16	19	
				–40°C to 85°C			21	
				–40°C to 105°C			23	
R_{PD}	Output pulldown resistance	V_{IN} = 5.0 V, V_{ON} = 0 V, I_{OUT} = 15 mA		–40°C to 105°C		230	330	Ω

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6.6 Electrical Characteristics: V_{BIAS} = 2.5 V

Unless otherwise noted, the specifications apply over the operating ambient temperature –40°C ≤ T_A ≤ 105°C (full) and V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 2.5 V		–40°C to 105°C		32	40	µA
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 2.5 V		–40°C to 105°C		32	40	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to 105°C			2	µA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 2.5 V	–40°C to 105°C		0.13	3	µA
			$V_{IN1,2}$ = 1.8 V			0.07	2	
			$V_{IN1,2}$ = 1.2 V			0.05	2	
			$V_{IN1,2}$ = 0.8 V			0.04	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to 105°C			1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		21	24	mΩ
				–40°C to 85°C			27	
				–40°C to 105°C			29	
			V_{IN} = 1.8 V	25°C		19	22	
				–40°C to 85°C			25	
				–40°C to 105°C			27	
			V_{IN} = 1.5 V	25°C		18	21	
				–40°C to 85°C			24	
				–40°C to 105°C			26	
			V_{IN} = 1.2 V	25°C		18	21	
				–40°C to 85°C			24	
				–40°C to 105°C			26	
			V_{IN} = 0.8 V	25°C		17	20	
				–40°C to 85°C			23	
				–40°C to 105°C			25	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		Full		280	330	Ω

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6.7 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1559		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		6		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1991		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		665		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		732		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		161		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		371		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		14		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		544		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2410		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		7		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2412		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1181		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1575		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		124		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		927		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		14		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1089		

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6.8 Typical Characteristics

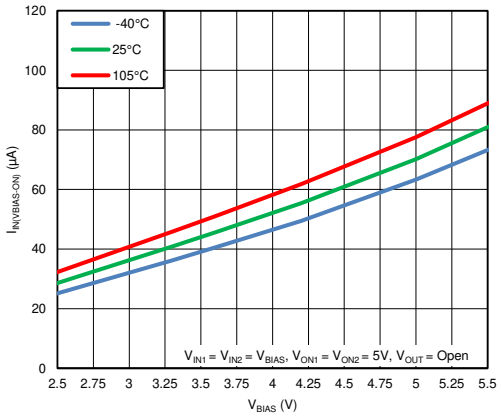

図 1. Quiescent Current vs. V_{BIAS} (Both Channels)

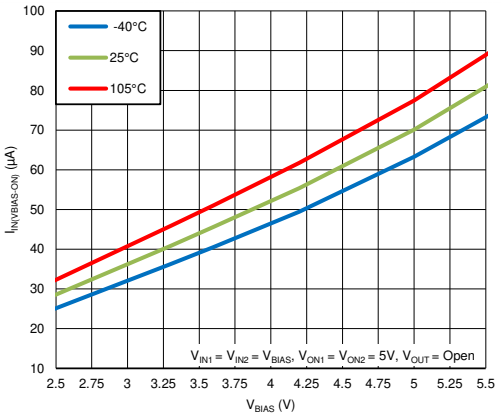

図 2. Quiescent Current vs. V_{BIAS} (Single Channel)

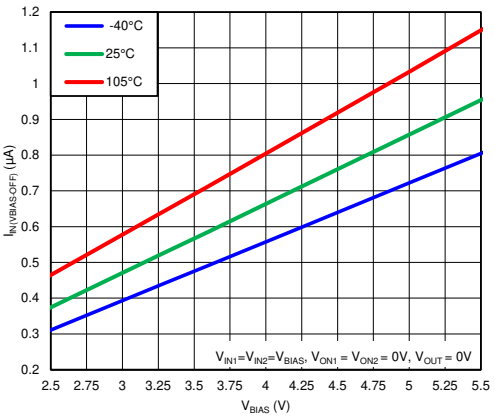

図 3. Shutdown Current vs. V_{BIAS} (Both Channels)

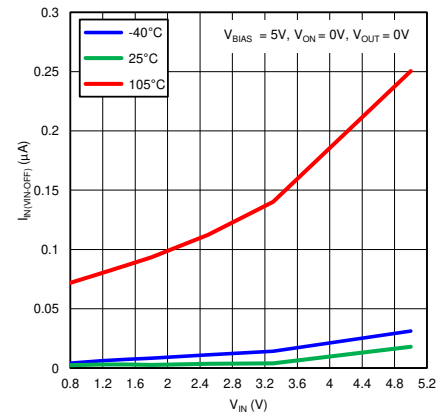

図 4. Off-State VIN Current vs. V_{IN} (Single Channel)

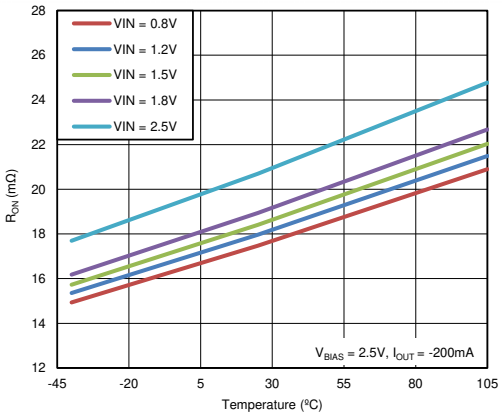

図 5. R_{ON} vs. Temperature (V_{BIAS} = 2.5 V, Single Channel)

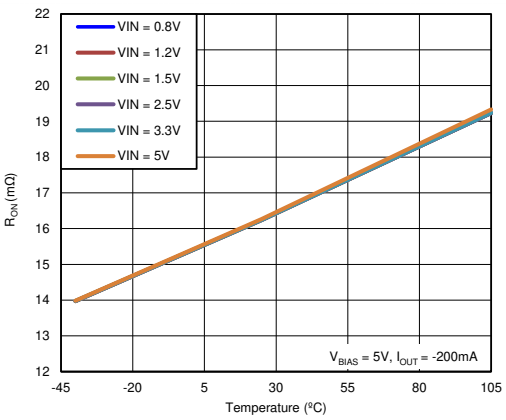

図 6. R_{ON} vs. Temperature (V_{BIAS} = 5 V, Single Channel)

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Typical Characteristics (continued)

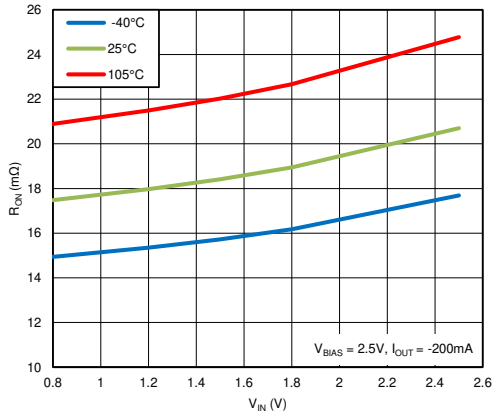

図 7. R_{ON} vs. V_{IN} (V_{BIAS} = 2.5 V, Single Channel)

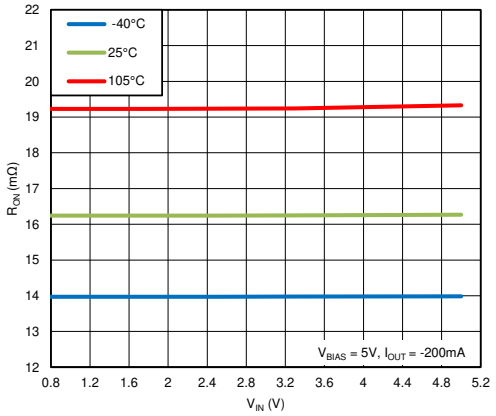

図 8. R_{ON} vs. V_{IN} (V_{BIAS} = 5 V, Single Channel)

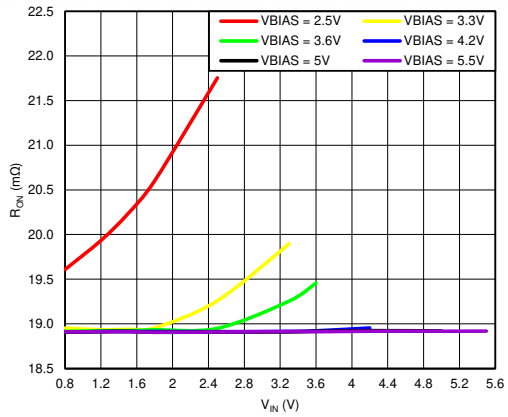

図 9. R_{ON} vs. V_{IN} (T_A = 25°C, Single Channel)

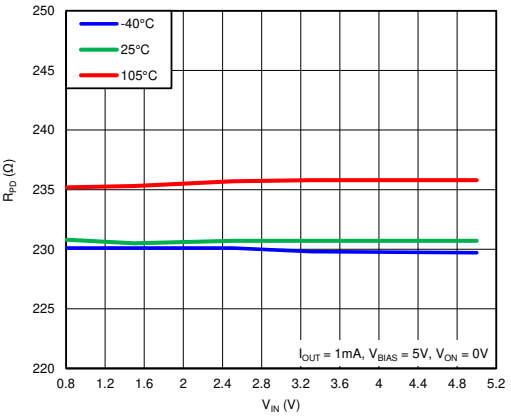

図 10. R_{PD} vs. V_{IN} (V_{BIAS} = 5 V, Single Channel)

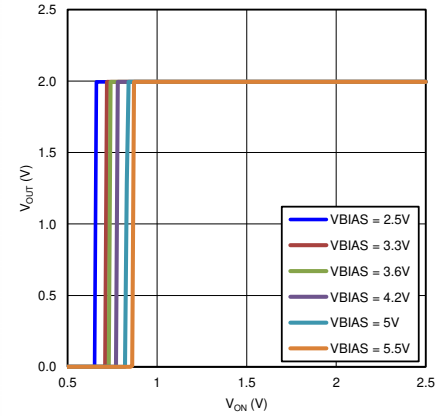

図 11. V_{OUT} vs. V_{ON} (T_A = 25°C, Single Channel)

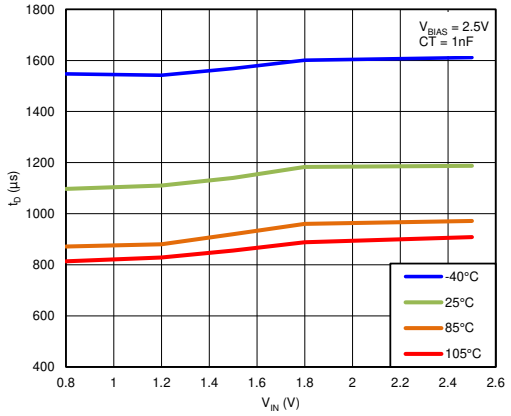

図 12. t_D vs. V_{IN} (V_{BIAS} = 2.5 V, CT = 1 nF)

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Typical Characteristics (continued)

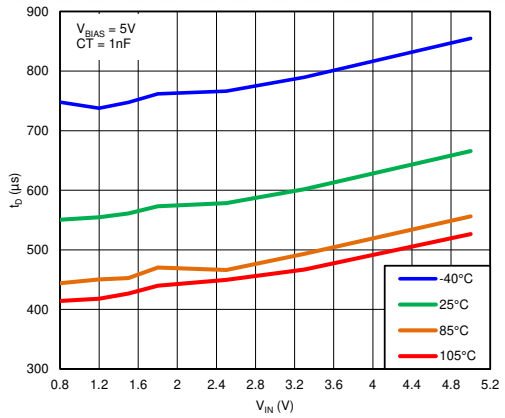

図 13. t_D vs. V_{IN} (V_{BIAS} = 5 V, CT = 1 nF)

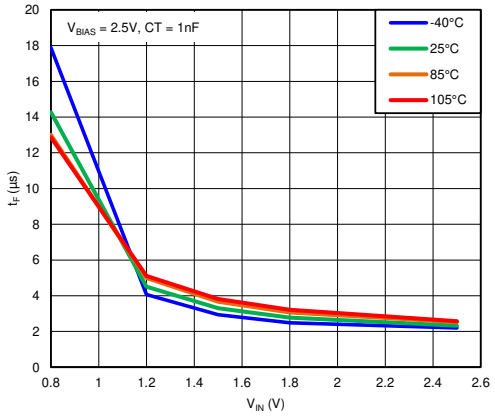

図 14. t_F vs. V_{IN} (V_{BIAS} = 2.5 V, CT = 1 nF)

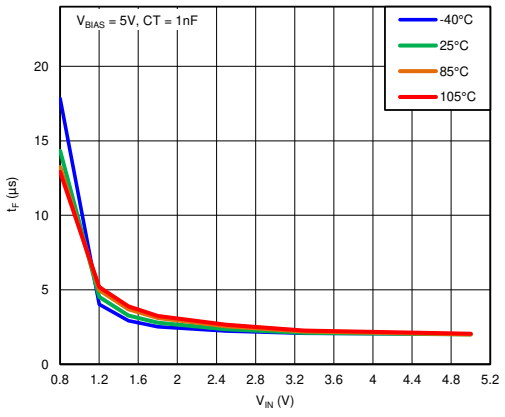

図 15. t_F vs. V_{IN} (V_{BIAS} = 5 V, CT = 1 nF)

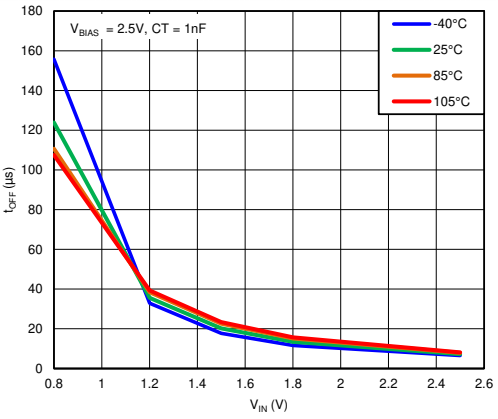

図 16. t_{OFF} vs. V_{IN} (V_{BIAS} = 2.5 V, CT = 1 nF)

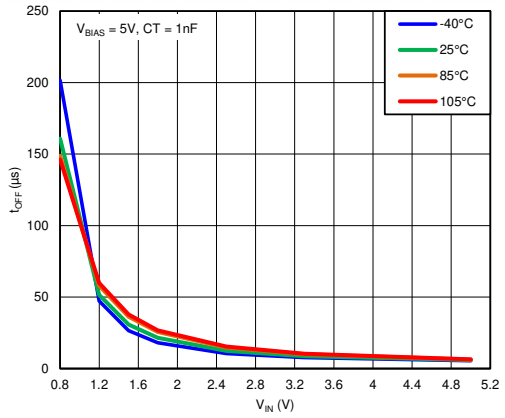

図 17. t_{OFF} vs. V_{IN} (V_{BIAS} = 5 V, CT = 1 nF)

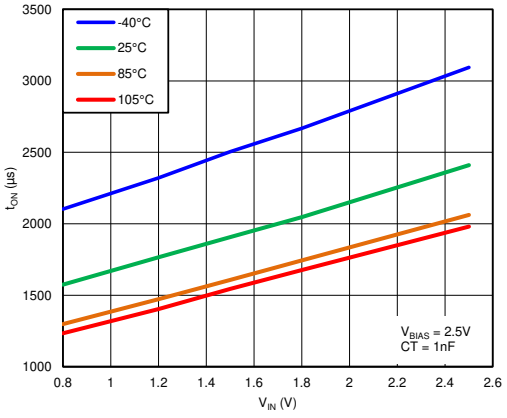

図 18. t_{ON} vs. V_{IN} (V_{BIAS} = 2.5 V, CT = 1 nF)

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Typical Characteristics (continued)

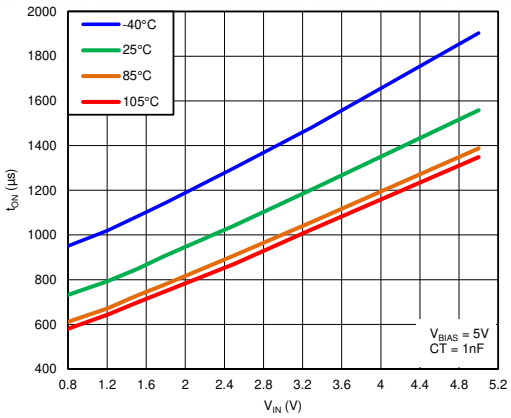

図 19. t_{ON} vs. V_{IN} (V_{BIAS} = 5 V, CT = 1 nF)

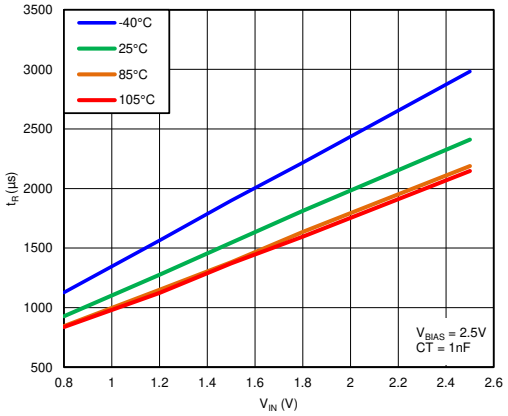

図 20. t_R vs. V_{IN} (V_{BIAS} = 2.5 V, CT = 1 nF)

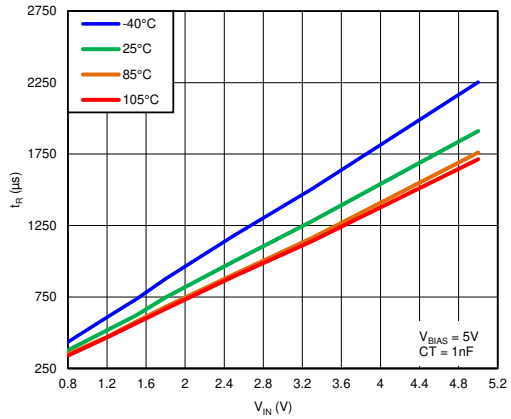

図 21. t_R vs. V_{IN} (V_{BIAS} = 5 V, CT = 1 nF)

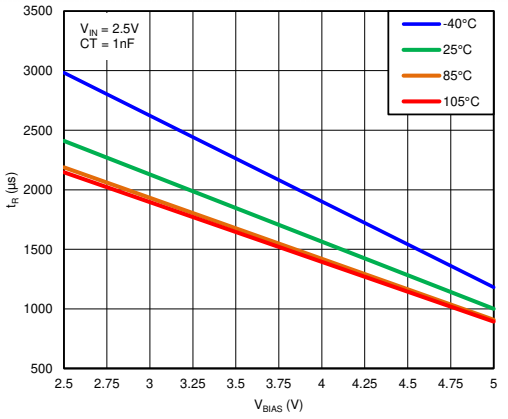

図 22. t_R vs. V_{BIAS} (V_{IN} = 2.5 V, CT = 1 nF)

6.8.1 Typical AC Scope Captures at T_A = 25ºC, CT = 1 nF

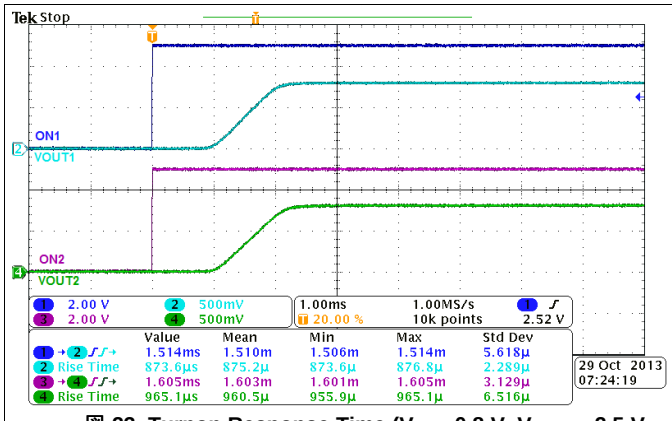

図 23. Turnon Response Time (V_{IN} = 0.8 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

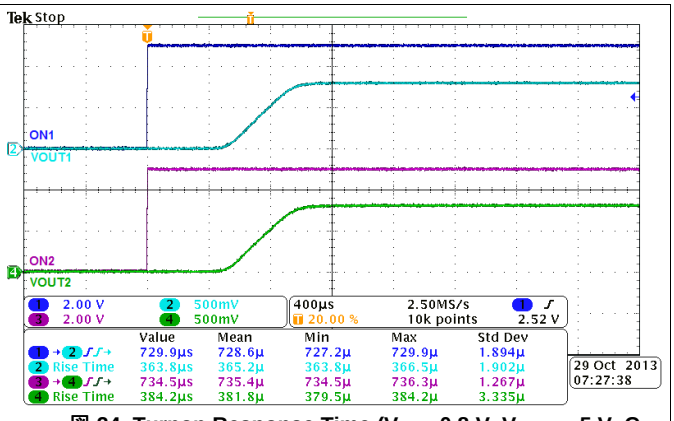

図 24. Turnon Response Time (V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

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Typical AC Scope Captures at T_A = 25ºC, CT = 1 nF (continued)

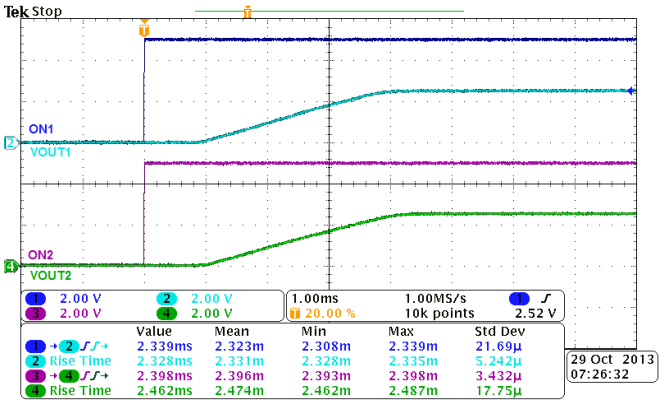

図 25. Turnon Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

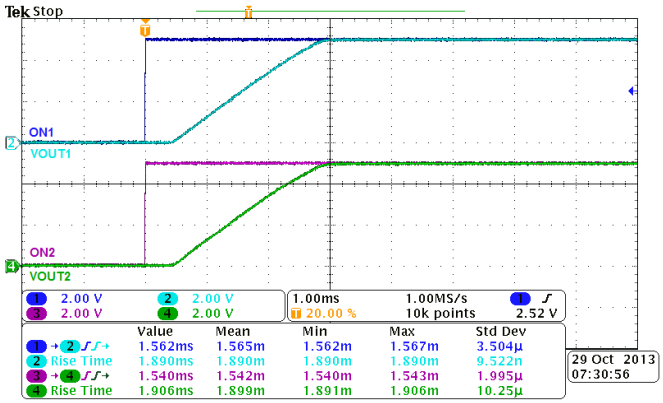

図 26. Turnon Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

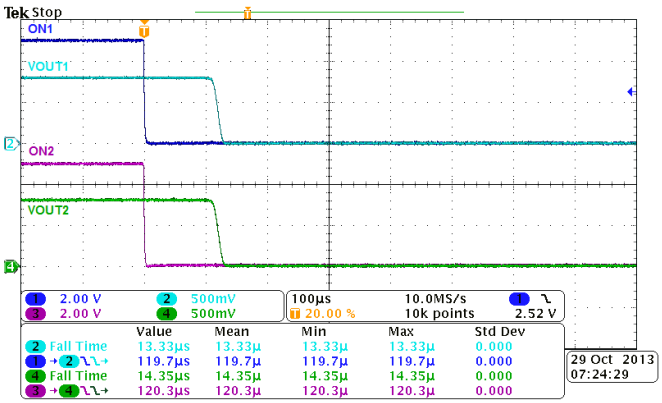

図 27. Turnoff Response Time (V_{IN} = 0.8 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

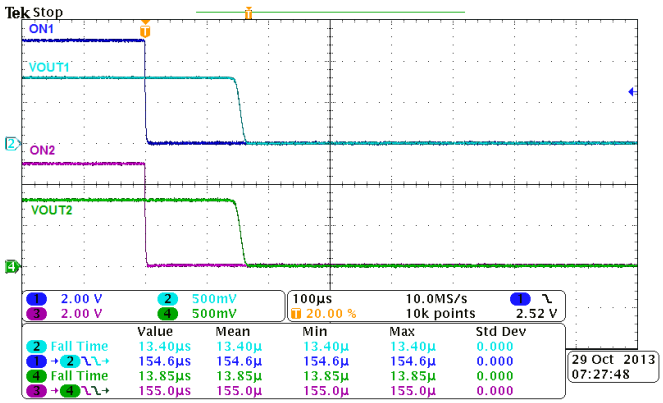

図 28. Turnoff Response Time (V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

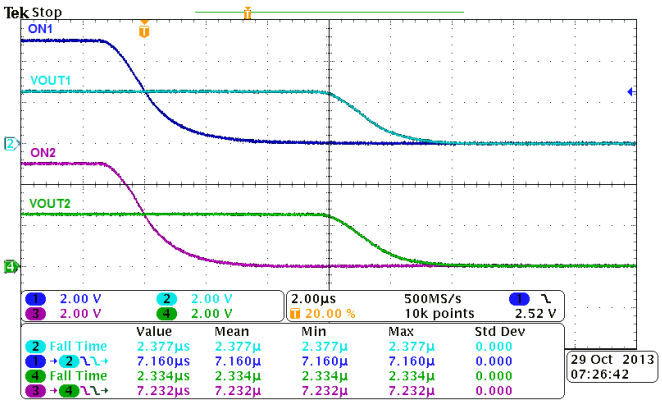

図 29. Turnoff Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

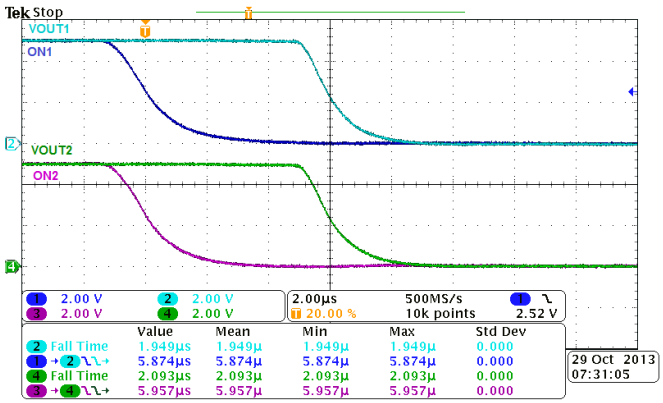

図 30. Turnoff Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

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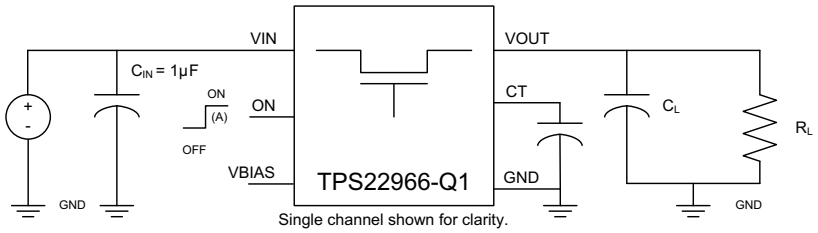
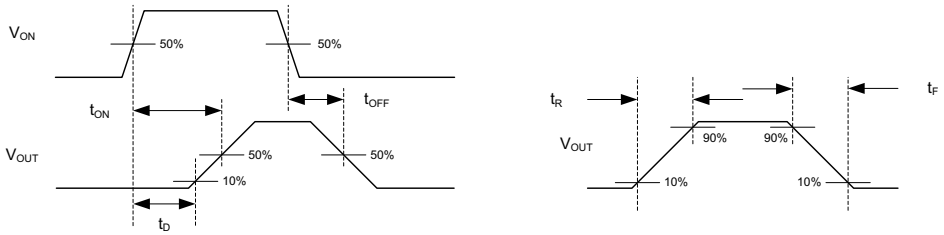
7 Parameter Measurement Information



TEST CIRCUIT



TIMING WAVEFORMS

(A) Control signal rise and fall times are 100 ns.

図 31. Test Circuit and Timing Waveforms

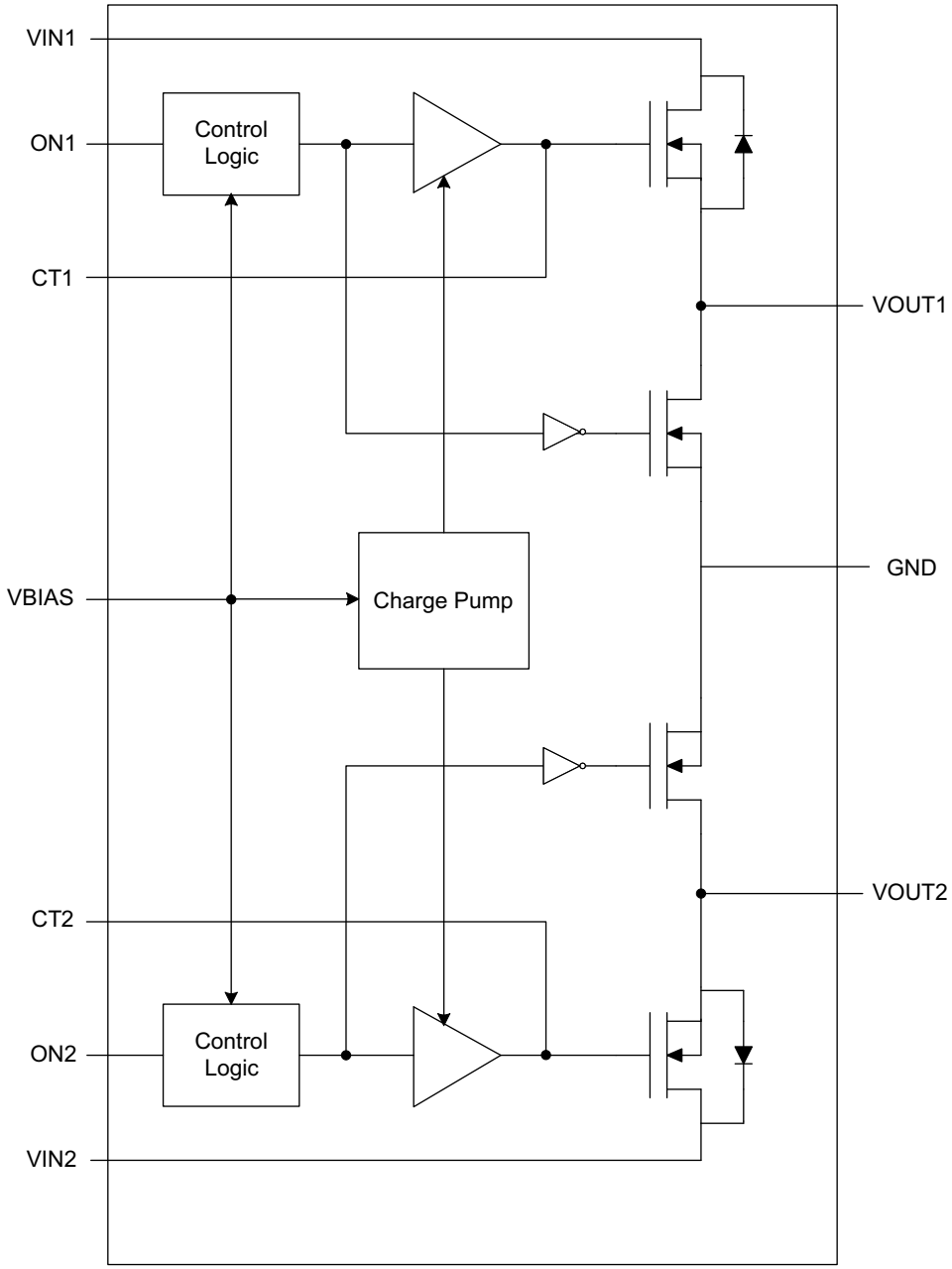
8 Detailed Description

8.1 Overview

The device is a dual-channel, 4-A automotive load switch in a 14-pin SON package. To reduce the voltage drop in high current rails, the device implements a low-resistance N-channel MOSFET.

The device has a programmable slew rate for applications that require specific rise-time. The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Quick Output Discharge

Each channel of the TPS22966-Q1 includes a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 230-Ω and prevents the output from floating while the switch is disabled.

8.3.2 ON/OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

8.3.3 Adjustable Rise Time

A capacitor to GND on the CTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V should be used on the CTx pin. An approximate formula for the relationship between CTx and slew rate is (the equation below accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CTx = 0 pF. Use 表 1 to determine rise times for when CTx = 0 pF):

$$SR = 0.32 \times CT + 13.7 \quad (1)$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CTx pin (in pF)
- The units for the constant 13.7 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. 表 1 shows rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

表 1. Rise Time Values

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1µF, C_{IN} = 1µF, R_L = 10Ω TYPICAL VALUES at 25°C, V_{BIAS} = 5V, 25V X7R 10% CERAMIC CAP						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	124	88	63	60	53	49	42
220	481	323	193	166	143	133	109
470	855	603	348	299	251	228	175
1000	1724	1185	670	570	469	411	342
2200	3328	2240	1308	1088	893	808	650
4700	7459	4950	2820	2429	1920	1748	1411
10000	16059	10835	6040	5055	4230	3770	3033

8.4 Device Functional Modes

表 2. Functional Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during start-up, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see *Adjustable Rise Time*).

9.1.3 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in *Electrical Characteristics*. See 図 32 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage.

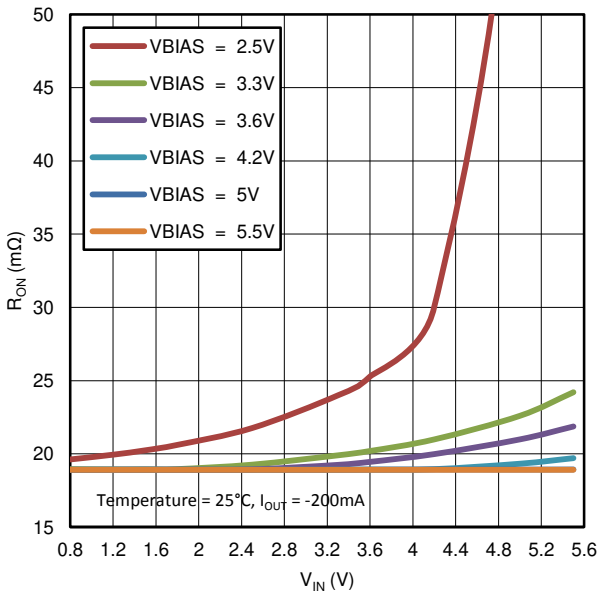

図 32. R_{ON} vs. V_{IN} (Single Channel)

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Application Information (continued)

9.1.4 Safe Operating Area (SOA)

The SOA curves in 図 33 show the continuous current carrying capability of the device versus ambient temperature (T_A) to ensure reliable operation over 100,000 hours of device lifetime. Each curve represents a specific percent of time that the switch is on.

The 100% curve represents use for a full 24 hours in a day. The 75% curve indicates 18 hours of use in a day while the 12.5% curve shows 3 hours of use per day.

Examples on how to use this plot:

- The application has an ambient temperature of 60°C and the switch will be on 100% of the time. The maximum continuous current that can be applied is approximately 2.1 A.
- The application requires the switch to be on 12.5% of the time and the current while on will be 3 A. The maximum ambient temperature is approximately 100°C.
- The application requires 2 A and will be operated at 70°C. The switch can be on for a maximum of 75% of the time.
- It is expected that most applications will not have specific use cases as defined in the examples above. Different use cases can be combined to generate a more complete view of a specific application. This example shows use under various conditions simplified to an average use case. The application requires operation at 4 A for 25% of the time, 1 A for 25% of the time and is off the remaining 50% of the time. Ambient temperature will vary from 25°C to 50°C. Will there be any limitations? The average current can be calculated as (4 A × 25% + 1 A * 25% + 0 A * 50%). The average current calculates to be 1.25 A. Assuming worst case temperature of 50°C, the resulting application is within the safe operating area.

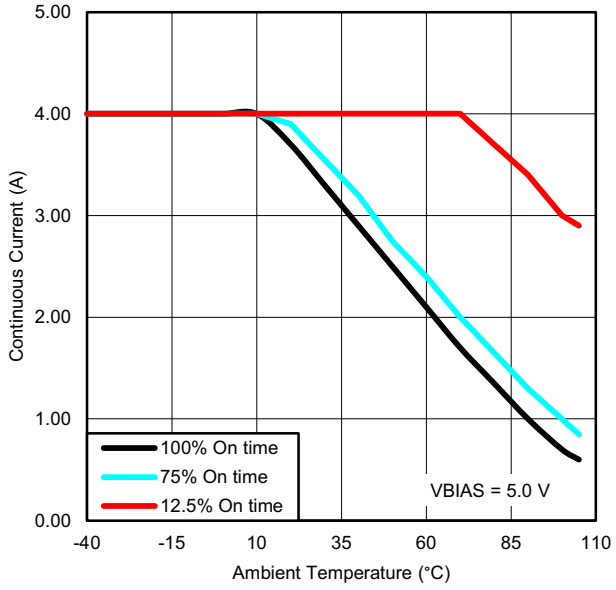

図 33. Safe Operating Area

9.2 Typical Application

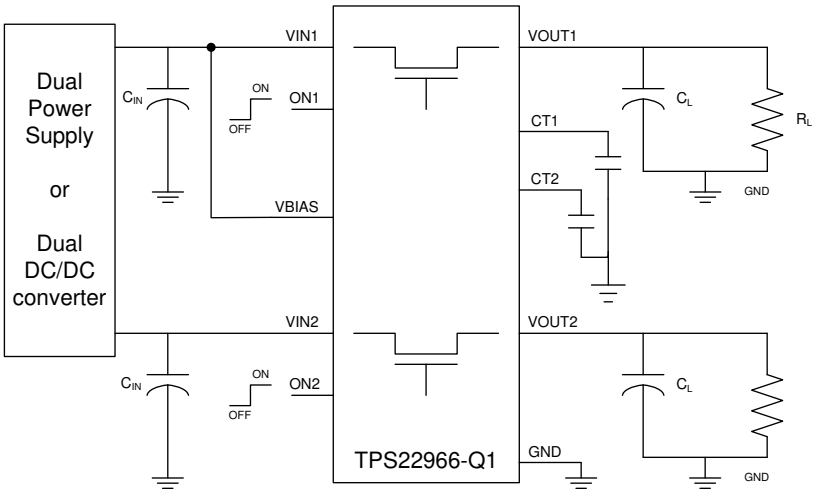

図 34. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 3 as the input parameters.

表 3. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	3.3 V
Bias voltage	5 V
Load capacitance (C_L)	22 µF
Maximum acceptable inrush current	400 mA

9.2.2 Detailed Design Procedure

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using 式 2:

Inrush Current = C × dV/dt

where

- C = output capacitance
- dV = output voltage
- dt = rise time (2)

The TPS22966-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using 表 3 and the inrush current equation.

400 mA = 22 µF × 3.3 V/dt (3)

dt = 181.5 µs (4)

To ensure an inrush current of less than 400 mA, choose a CT value that will yield a rise time of more than 181.5 µs. See the oscilloscope captures in for an example of how the CT capacitor can be used to reduce inrush current.

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9.2.3 Application Curves

V_{BIAS} = 5 V ; V_{IN} = 3.3 V ; C_L = 22 µF

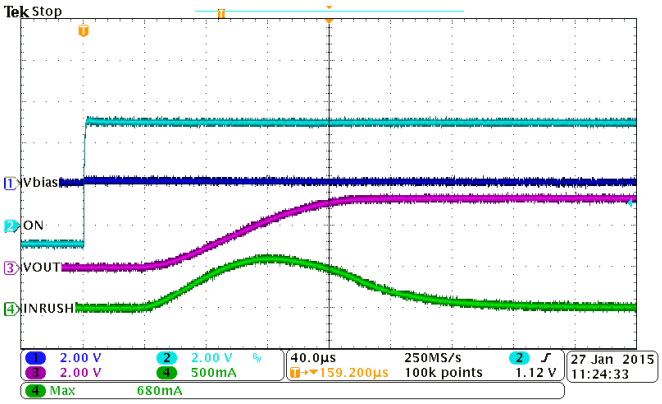

図 35. Inrush Current With CT = 0 pF

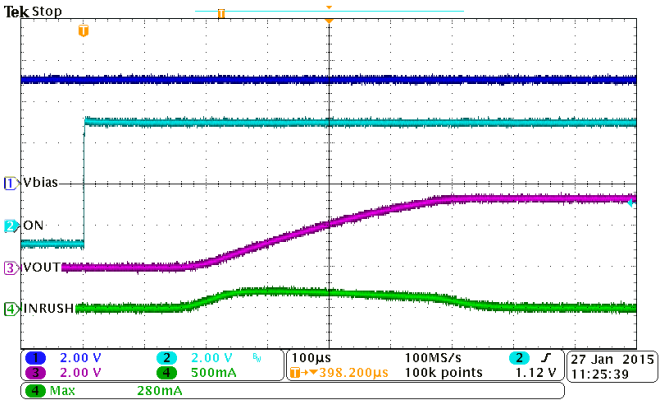

図 36. Inrush Current With CT = 220 pF

10 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN voltage range of 0 V to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 uF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This will cause the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (5)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22966-Q1)
- T_A = ambient temperature
- Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

図 37 shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

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11.2 Layout Example

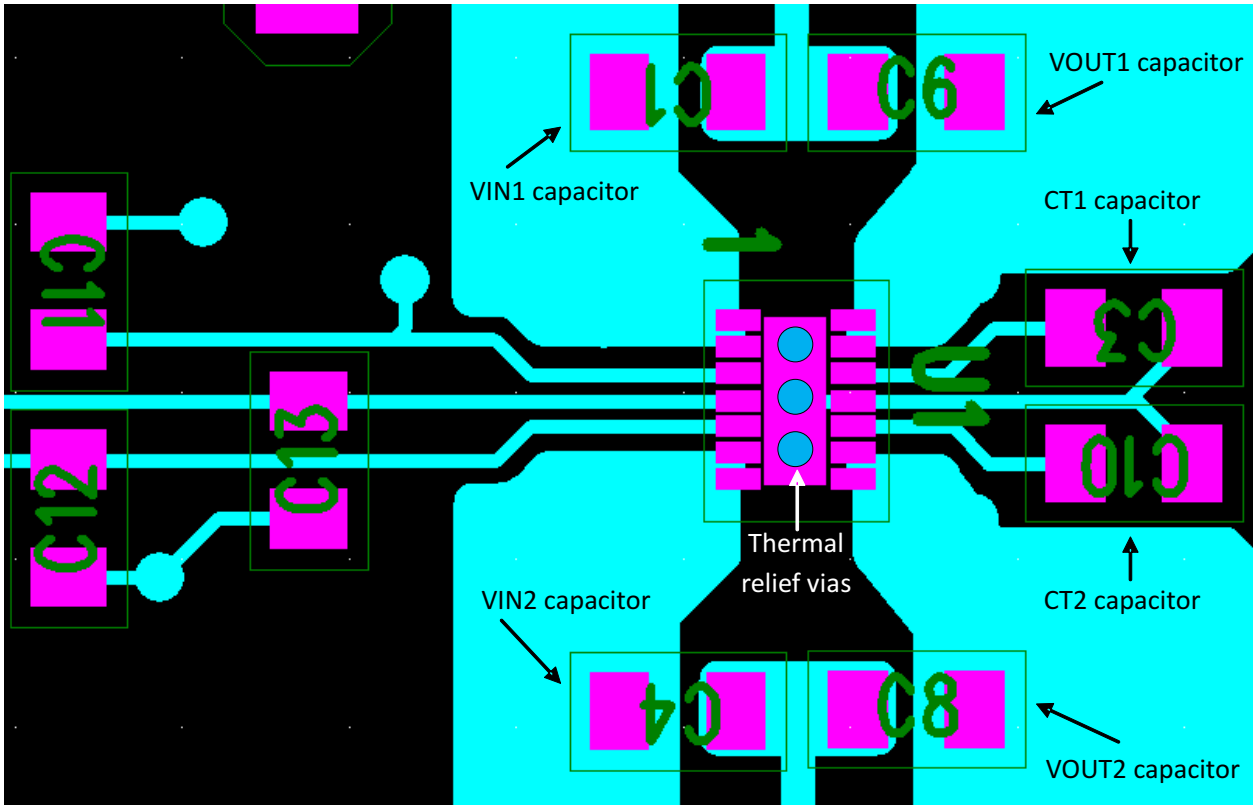

図 37. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 商標

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12.2 静電気放電に関する注意事項

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12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12.4 ドキュメントの更新通知を受け取る方法

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12.5 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22966TDPURQ1	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	966TQ1	Samples
TPS22966TDPUTQ1	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	966TQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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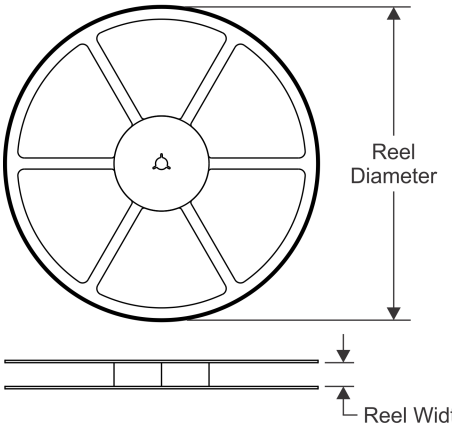
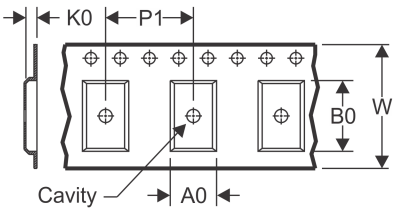
TAPE AND REEL INFORMATION

REEL DIMENSIONS

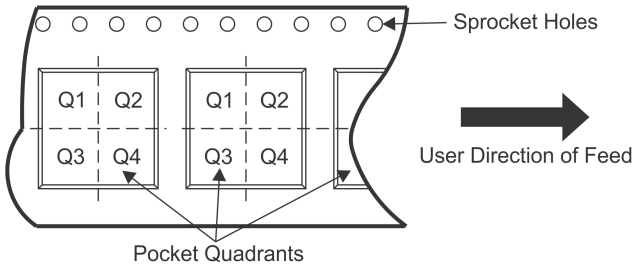


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

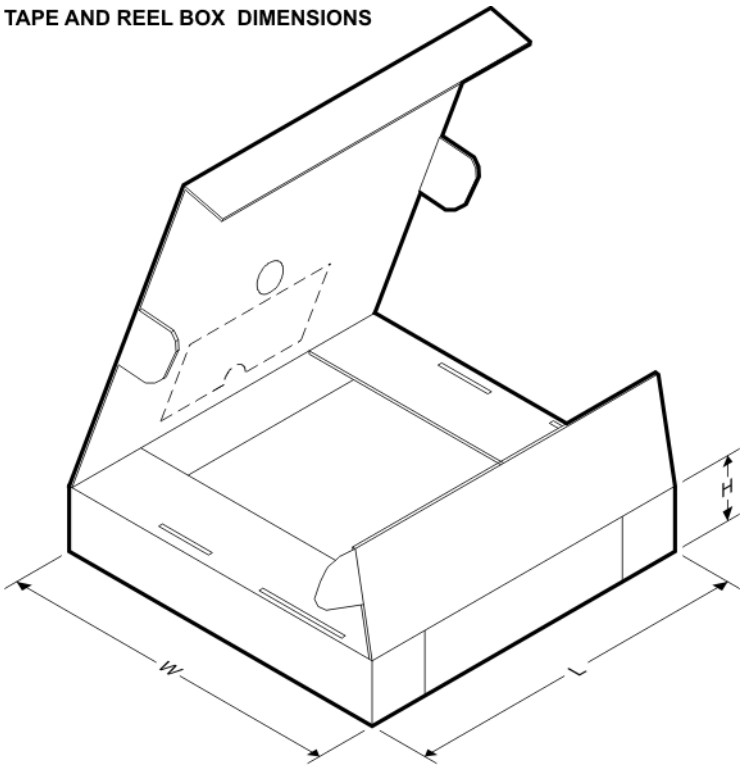
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22966TDPURQ1	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22966TDPUTQ1	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

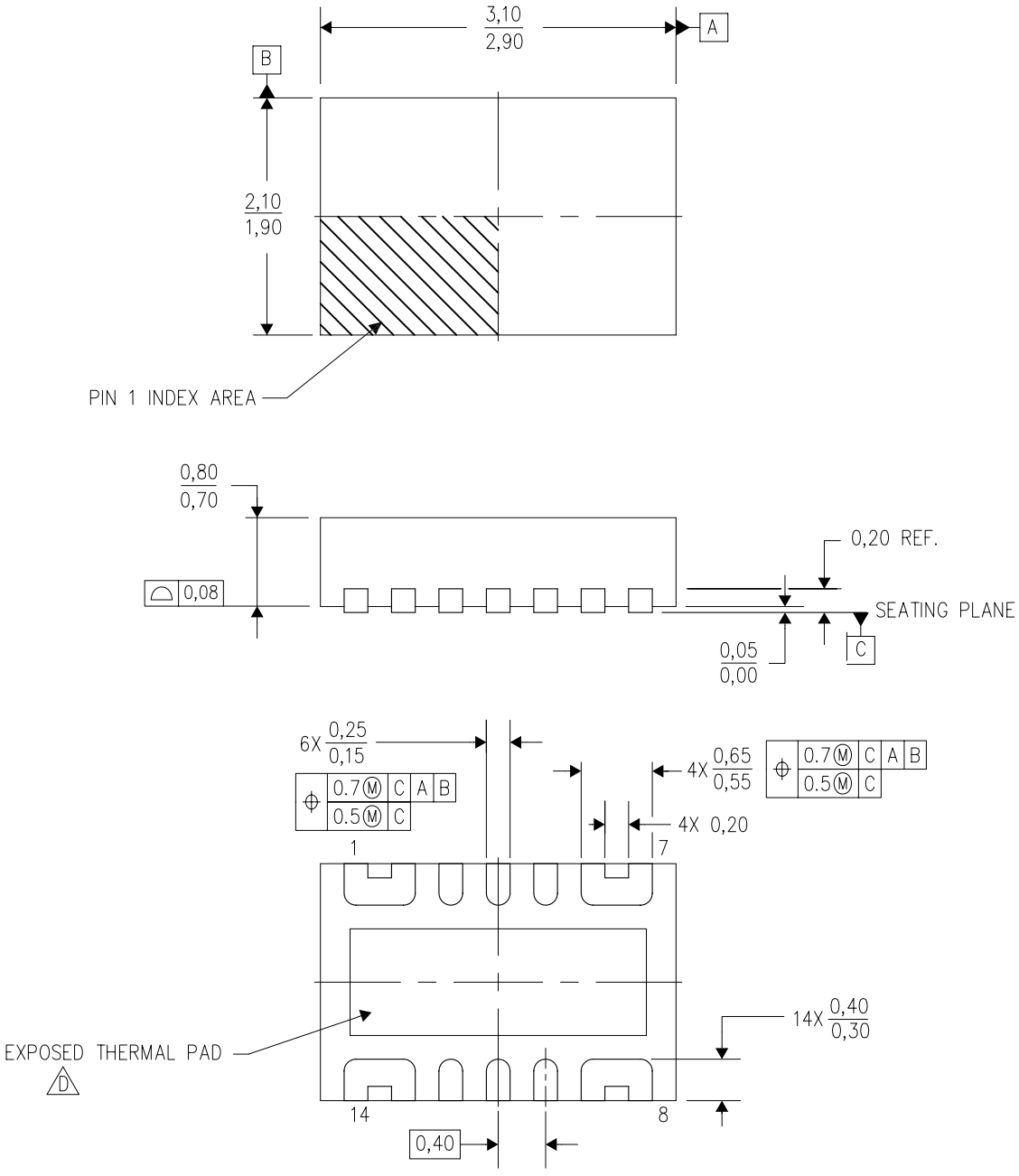
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22966TDPURQ1	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22966TDPUTQ1	WSON	DPU	14	250	210.0	185.0	35.0

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is Pb–free.

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