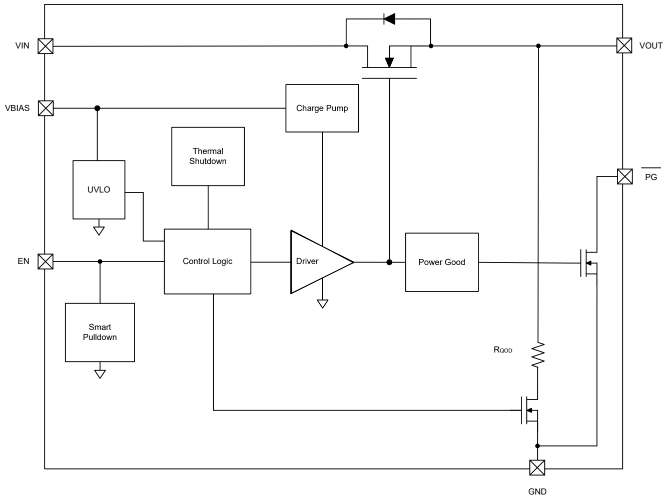
TPS22999 突入電流レギュレーション搭載、4.5V、1.5A、オン抵抗 7.5mΩ、高速ターンオン、ロード・スイッチ

1 特長

- 動作時入力電圧範囲 (V_{IN}):0.1V～4.5V
- バイアス電圧範囲:2.3V～5.5V
- 最大連続電流:1.5A
- オン抵抗 (R_{ON}):7.5mΩ (標準値)
- レギュレートされた突入電流
- 急速出力放電内蔵:5.3Ω
- オープン・ドレインのパワー・グッド ($\overline{PG}$) 信号
- ターンオン時間:200µs 未満 (V_{IN} = 1.0V 時)
- サーマル・シャットダウン
- VBIAS 電源低電圧誤動作防止 (UVLO)
- 低い消費電力:
    - オン状態 (I_Q):10µA (標準値)
    - オフ状態 (I_{SD}):2.7µA (標準値)
- EN ピンのスマート・プルダウン ($R_{PD,EN}$)
    - EN ≧ V_{IH} (I_{ON}):25nA (標準値)
    - EN ≦ V_{IL} ($R_{PD,ON}$):500kΩ (標準値)

2 アプリケーション

- ウェアラブル
- ソリッドステート・ドライブ (SSD)
- PC とノート PC
- 産業用 PC
- 光学モジュール



TPS22999 のブロック図

3 概要

TPS22999 は、高速ターンオン時間を実現しながら、低い突入電流を維持するよう設計されたシングル チャネル ロード スイッチです。このデバイスには、0.1V～V_{BIAS} -1.0V の入力電圧範囲で動作できる N チャネル MOSFET が内蔵されており、最大連続 1.5A の電流に対応します。

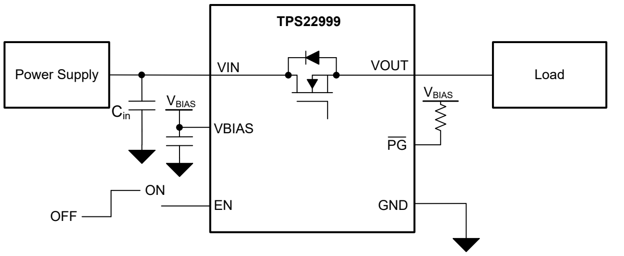
このスイッチは 1 本のイネーブル・ピン (EN) で制御されます。このイネーブル・ピンは低電圧の GPIO 信号 (V_{IH} = 0.8V) と直接接続できます。TPS22999 デバイスは、スイッチオフ時の 5.3Ω のクイック出力放電パスを内蔵し、信頼性の高いシステム動作を実現します。本デバイスには、メイン MOSFET が完全に最小抵抗になっていることを示すパワー・グッド ($\overline{PG}$) 信号があります。この PG 信号を使って下流の負荷を有効にできます。サーマル・シャットダウン機能を内蔵しているため、高温環境でも確実に保護されます。

TPS22999 は、0.35mm ピッチの
8 ピン WCSP パッケージ (YCH) で供給され、-40℃～+105℃の自由気流温度範囲に渡って
動作することが特徴です。

パッケージ情報

部品番号	パッケージ[1]	パッケージ・サイズ[2]
TPS22999	YCH (DSBGA、8)	1.4mm × 0.7mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



TPS22999 の代表的なアプリケーション

English Data Sheet: SLVSH34

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4 Pin Configuration and Functions

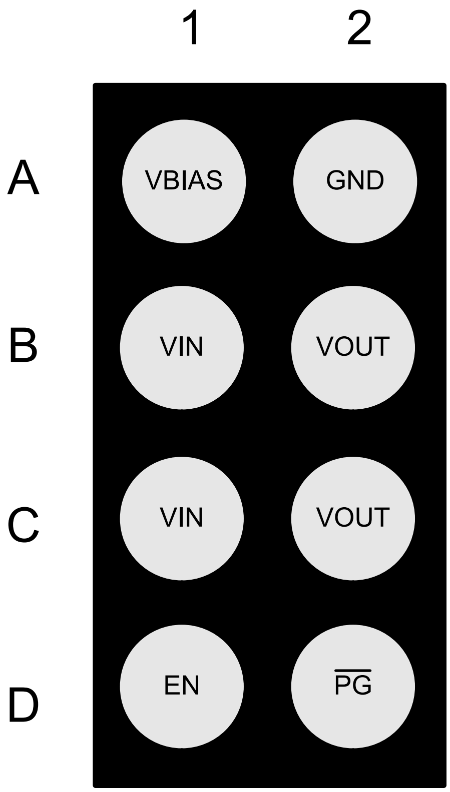


図 4-1. TPS22999 YCH Package, 8-Pin DSBGA (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VBIAS	A1	I	Device bias supply. Connect a 0.1-µF capacitor to ground.
GND	A2	—	Device ground
VIN	B1, C1	I	Switch input
VOUT	B2, C2	O	Switch output
EN	D1	I	Switch enable
$\overline{PG}$	D2	O	Open drain power-good signal, asserted low when the MOSFET has been fully enhanced. Connect to ground if unused.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{EN}, V_{PG}	Control pin voltage	–0.3	6	V
I_{MAX}	Maximum current		1.5	A
I_{MAX_PLS}	Maximum current (24 hours)		4.5	A
T_J	Junction temperature		Internally Limited	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.1		V_{BIAS} – 1.0	V
V_{OUT}	Output voltage, EN > V_{IH}	0.1		V_{IN}	V
V_{BIAS}	Bias voltage	2.3		5.5	V
V_{IH}	EN pin high voltage range	0.8		5.5	V
V_{IL}	EN pin low voltage range	0		0.35	V
C_{OUT}	Output capacitor(1)	0		70	µF
V_{PG}	$\overline{PG}$ pin voltage	0		5.5	V
T_A	Ambient temperature	–40		105	°C

(1) Effective output capacitance required for stability

5.4 Thermal Information

THERMAL METRIC[1] [2]		TPS22999 YCH (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	34.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

5.5 Electrical Characteristics (VBIAS = 5.5 V)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							
$I_{SD,VBIAS}$	VBIAS shutdown current	EN = 0 V	25°C		2.7		µA
			–40°C to 85°C			4	µA
			–40°C to 105°C			5	µA
$I_{Q,VBIAS}$	VBIAS quiescent current	EN > V_{IH}	25°C		10		µA
			–40°C to 85°C			18	µA
			–40°C to 105°C			20	µA
$I_{Q,VIN}$	VIN quiescent current	EN > V_{IH}	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			1.5	µA
$I_{SD,VIN}$	VIN shutdown current	EN = 0 V, V_{IN} = 4.5 V	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			3	µA
I_{EN}	EN pin leakage	EN = VBIAS	–40°C to 105°C		0.1		µA
Performance							

5.5 Electrical Characteristics (VBIAS = 5.5 V) (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
R_{ON}	On-resistance	VIN = 4.5 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 3.3 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.8 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.0 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.78 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.5 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
$V_{OL,PG}$	Power-Good VOL	I_{PG} = 500uA	-40°C to 105°C			0.2	V
V_{BIAS_UVLO}	V_{BIAS} undervoltage lockout	Falling	–40°C to 105°C	1.65	1.85	2.05	V
		Hysteresis	–40°C to 105°C		0.150		V
		Rising	–40°C to 105°C	1.8	2.0	2.2	V
I_{INRUSH}	Regulated inrush current	C_L = 60uF, $V_{IN} \le 1$ V	–40°C to 105°C		0.95	1.33	A
		C_L = 60uF, $V_{IN} > 1$ V	–40°C to 105°C		0.95	1.4	A
$V_{HYS,EN}$	Enable pin hysteresis	VIN = 4.5 V	–40°C to 105°C		75		mV
$R_{PD,EN}$	Smart pulldown Resistance	EN < V_{IL}	25°C		500		kΩ
			–40°C to 105°C			750	kΩ
R_{QOD}	QOD resistance	VIN = 1.0 V	25°C		5.3		Ω
			–40°C to 105°C			10	Ω
Protection							
TSD	Thermal shutdown		-	116	131	146	°C

5.6 Electrical Characteristics (VBIAS = 3.4 V)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							
$I_{SD,VBIAS}$	VBIAS shutdown current	EN = 0 V	25°C		2.2		µA
			–40°C to 85°C			4	µA
			–40°C to 105°C			5	µA

5.6 Electrical Characteristics (VBIAS = 3.4 V) (続き)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{Q,VBIAS}$	VBIAS quiescent current	EN > V_{IH}	25°C		10		µA
			–40°C to 85°C			18	µA
			–40°C to 105°C			20	µA
$I_{Q,VIN}$	VIN quiescent current	EN > V_{IH}	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			1.5	µA
$I_{SD,VIN}$	VIN shutdown current	EN = 0 V, V_{IN} = 2.4 V	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			2	µA
I_{EN}	EN pin leakage	EN = VBIAS	–40°C to 105°C		0.1		µA
Performance							
R_{ON}	On-resistance	VIN = 2.4 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.8 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.0 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.78 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.5 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
I_{INRUSH}	Regulated inrush current	C_L = 60 µF, $V_{IN} \leq$ 1 V	–40°C to 105°C		0.95	1.33	A
		C_L = 60 µF, V_{IN} > 1 V	–40°C to 105°C		0.95	1.4	A
$V_{OL,PG}$	Power-Good V_{OL}	I_{PG} = 500 µA	–40°C to 105°C			0.2	V
$V_{HYS,EN}$	Enable pin hysteresis	VIN = 2.4 V	–40°C to 105°C		75		mV
$R_{PD,EN}$	Smart pulldown resistance	EN < V_{IL}	25°C		500		kΩ
			–40°C to 105°C			750	kΩ
R_{QOD}	QOD resistance	VIN = 1.0 V	25°C		8.3		Ω
			–40°C to 105°C			19	Ω
Protection							

5.7 Electrical Characteristics (VBIAS = 2.3 V)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							

5.7 Electrical Characteristics (VBIAS = 2.3 V) (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{SD,VBIAS}$	VBIAS shutdown current	EN = 0 V	25°C		2.1		µA
			–40°C to 85°C			3.5	µA
			–40°C to 105°C			4	µA
$I_{Q,VBIAS}$	VBIAS quiescent current	EN > V_{IH}	25°C		7.5		µA
			–40°C to 85°C			18	µA
			–40°C to 105°C			20	µA
$I_{Q,VIN}$	VIN quiescent current	EN > V_{IH}	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			1.5	µA
$I_{SD,VIN}$	VIN shutdown current	EN = 0 V, V_{IN}= 1.3 V	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			2	µA
I_{EN}	EN pin leakage	EN = VBIAS	–40°C to 105°C		0.1		µA
Performance							
R_{ON}	On-resistance	VIN = 1.3 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.0 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.78 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.5 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
I_{INRUSH}	Regulated inrush current	C_L = 60 µF	–40°C to 105°C		0.9	1.33	A
$V_{OL,PG}$	Power-Good VOL	I_{PG} = 500 µA	–40°C to 105°C			0.2	V
$V_{HYS,EN}$	Enable pin hysteresis	VIN = 1.3 V	–40°C to 105°C		75		mV
$R_{PD,EN}$	Smart pulldown Resistance	EN < V_{IL}	25°C		500		kΩ
			–40°C to 105°C			750	kΩ
R_{QOD}	QOD resistance	VIN = 1.0 V	25°C		16		Ω
			–40°C to 105°C			35	Ω
Protection							
TSD	Thermal shutdown		-	116	131	146	°C

5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Measured 350 µs after Vbias > 2.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = 4.5 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			440	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		200		µs

5.8 Switching Characteristics (続き)

over operating free-air temperature range (unless otherwise noted). Measured 350 µs after Vbias > 2.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		40		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		850		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 3.3 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			365	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		170		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		30		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		750		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 1.8 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			255	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		95		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		30		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		900		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 1.0 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			200	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		60		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		27		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		800		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 0.78 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			182	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		40		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		30		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		780		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 0.5 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			170	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		30		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		27		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		750		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs

5.9 Timing Diagrams

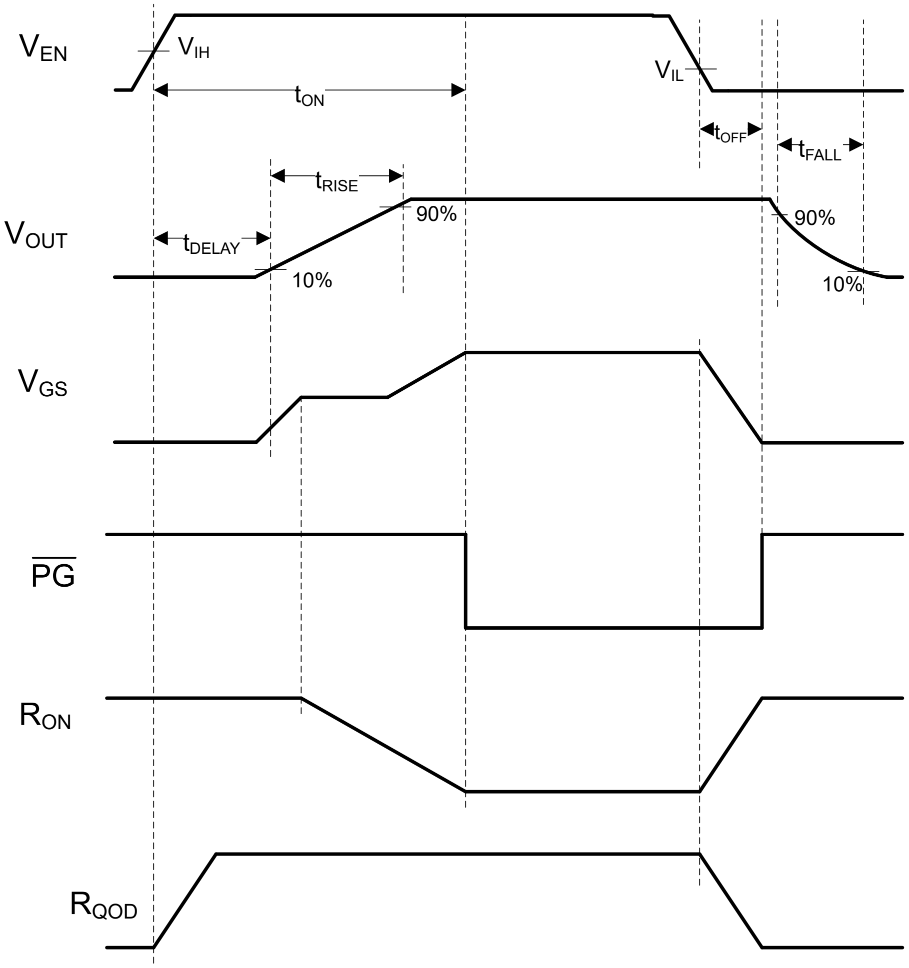


図 5-1. TPS22999 Timing Diagram

5.10 Typical Characteristics

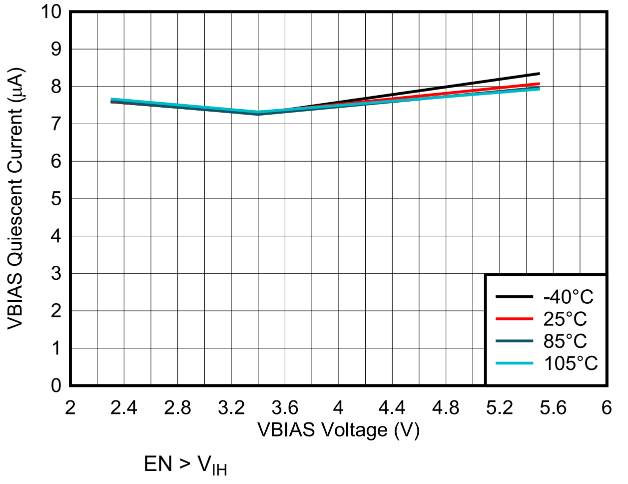


図 5-2. VBIAS Quiescent Current vs VBIAS Voltage

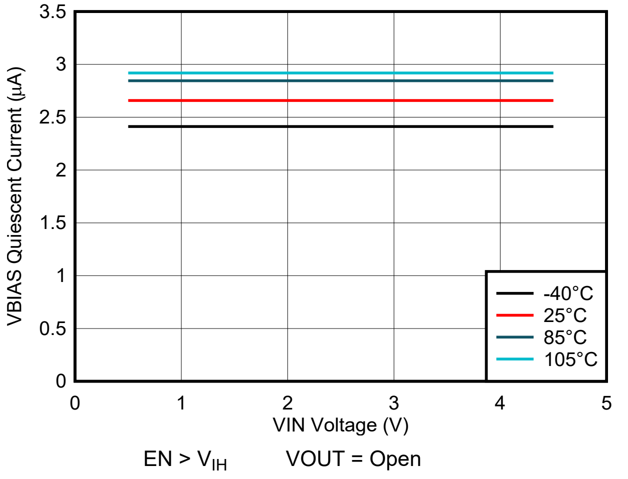


図 5-3. VBIAS Quiescent Current vs VIN Voltage

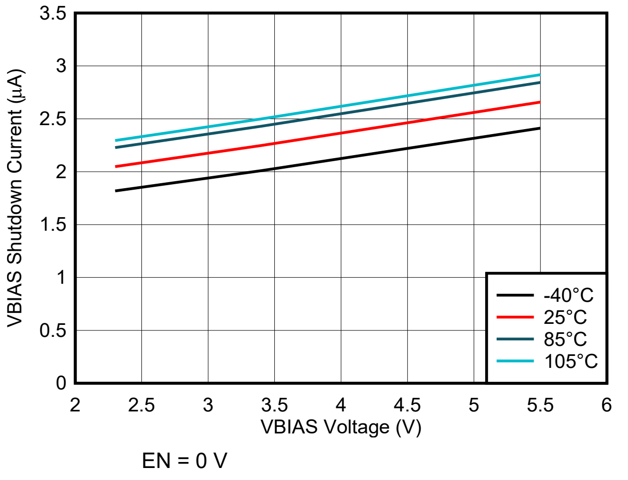


図 5-4. VBIAS Shutdown Current vs VBIAS Voltage

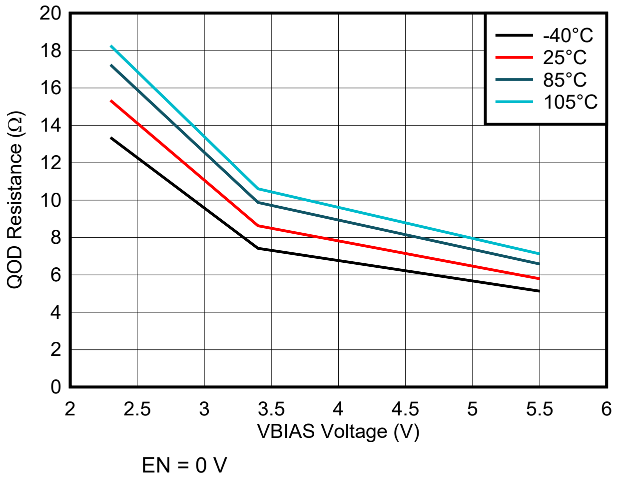


図 5-5. QOD Resistance vs VBIAS Voltage

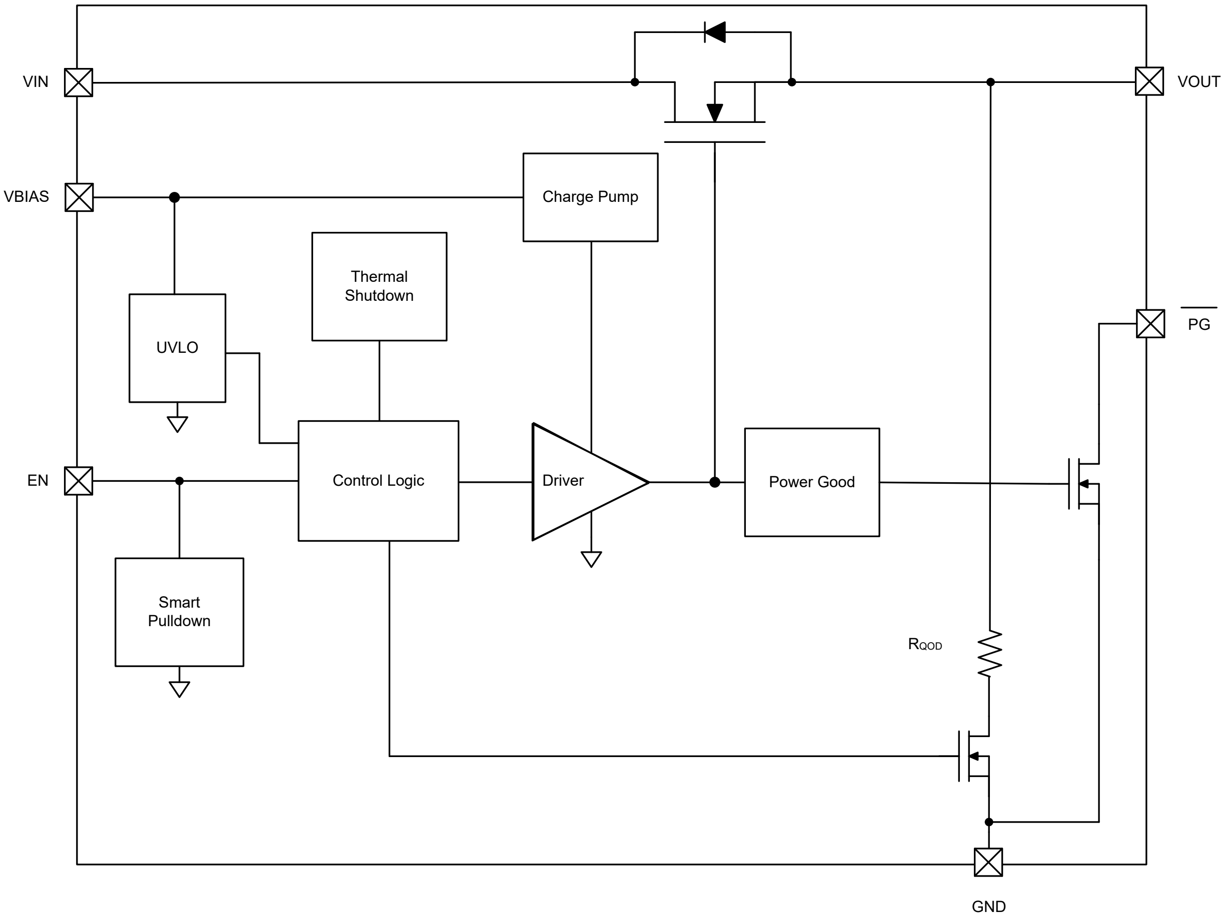
6 Detailed Description

6.1 Overview

The TPS22999 device is a single-channel load switch with a 7.5-mΩ power MOSFET designed to operate up to 1.5 A. The voltage range is 0.1 V to 4.5 V. The device regulates inrush current upon turn-on while providing a fast turn-on time.

The switch is controlled by an enable pin (EN), which is capable of interfacing directly with low voltage GPIO signals down to the V_{IH} level of 0.8 V. The TPS22999 device has an integrated 10-Ω quick output discharge when switch is turned off. There is a Power-Good ($\overline{PG}$) signal on the device that indicates when the main MOSFET is fully turned on and the on-resistance is at final value.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 ON and OFF Control

The EN pin controls the state of the switch. The EN pin is compatible with standard GPIO logic threshold so the EN pin can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pulldown is used to keep the EN pin from floating until the system sequencing is complete. After the EN pin is deliberately driven high (≥ V_{IH}), the Smart Pulldown is disconnected to prevent unnecessary power loss. See the following table for when the EN Pin Smart Pulldown is active.

EN Pin Voltage	EN Pin Function
≤ V_{IL}	Pulldown active
≥ V_{IH}	No pulldown

6.3.2 Regulated Inrush Current

Depending on the rise time at power-up, output load capacitances can cause large inrush currents that are limited only by parasitic resistance and inductances present in wiring and interconnections. These high currents can cause input voltage supply droop which can harm or cause malfunction in other circuits in the system.

To prevent these problems, TPS22999 regulates the inrush current(I_{INRUSH}) to a 1-A typical during the turn-on phase. This regulation enables the system to operate reliably while maintaining a fast turn-on time.

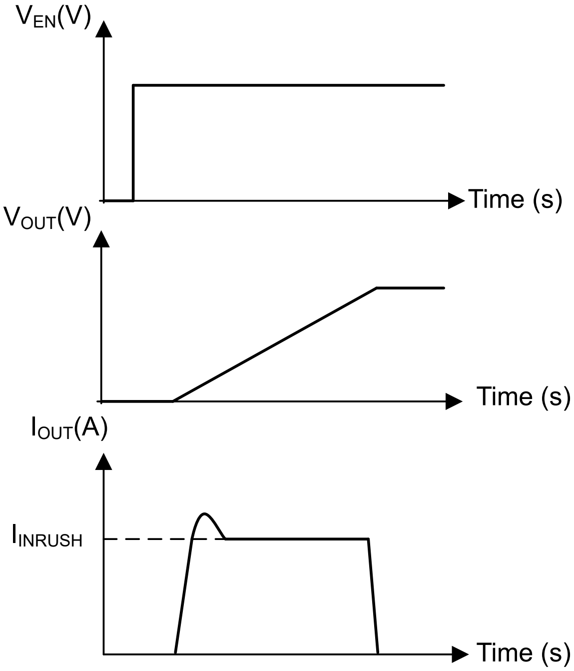


図 6-1. Regulated Inrush Current Behavior

6.3.3 Integrated Quick Output Discharge

TPS22999 integrates Quick Output Discharge (QOD). When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 10 Ω and prevents the output from floating while the switch is disabled while helping safely discharge output capacitances to ground.

6.3.4 Thermal Shutdown

When the device temperature reaches 131°C (typical), the device latches itself off to prevent thermal damage. The $\overline{\text{PG}}$ pin is deasserted to signal the output has been latched off. While T_J is over the T_{ABS} threshold, the output remains disabled even if the EN pin is toggled. After T_J decreases below the T_{ABS} threshold, the device does not enable the channel until the EN pin is toggled.

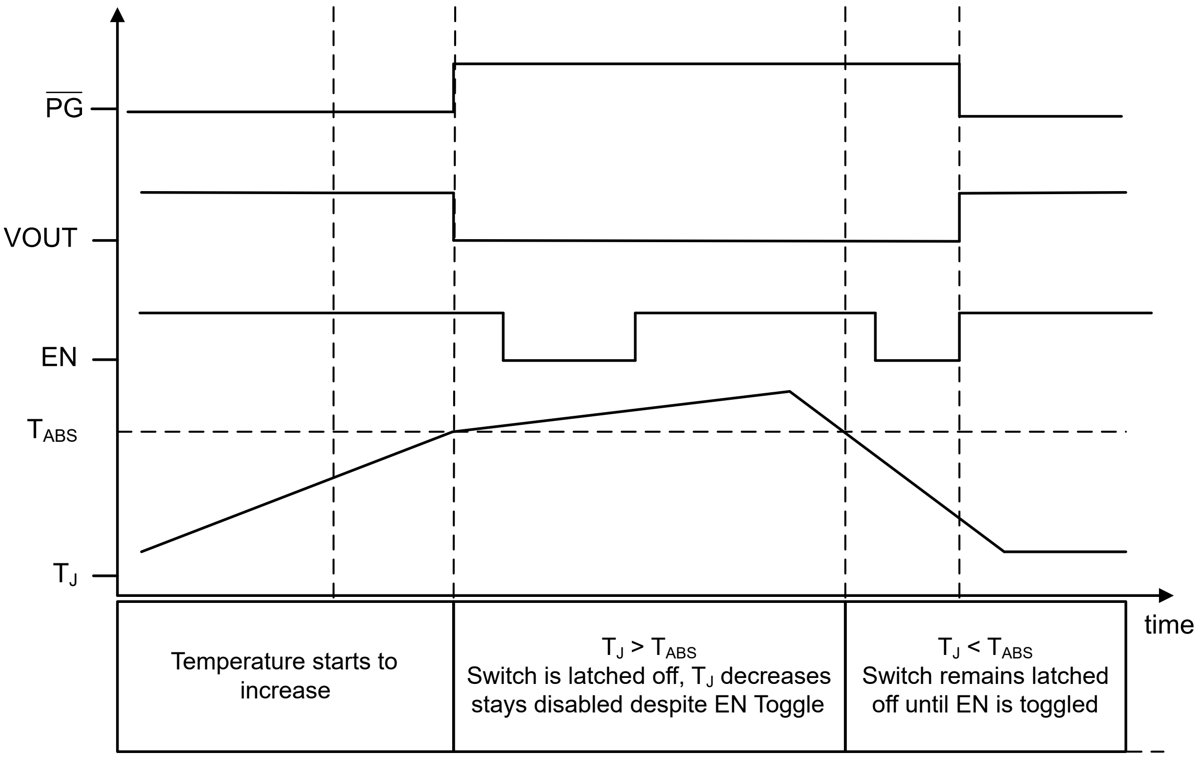


図 6-2. Thermal Shutdown Behavior

6.3.5 Power-Good (PG) Signal

The TPS22999 device has a Power-Good ($\overline{PG}$) output signal to indicate the gate of the pass FET is driven high and the switch is on with the on-resistance close to final value (full load ready). The signal is an active low and open drain output which can be connected to a voltage source through an external pullup resistor, R_{PU}. This voltage source can be VOUT from the TPS22999 device or another external voltage. VBIAS is required for PG to have a valid output.

6.4 Device Functional Modes

The following table summarizes the device functional modes:

EN	Fault Condition	VOUT State	nPG
L	N/A	Hi-Z	Hi-Z
H	None	V_{IN} (through R_{ON})	LO
X	Thermal shutdown	Hi-Z	Hi-Z

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

7.2 Typical Application

This typical application demonstrates how to use the TPS22999 device to limit start-up inrush current.

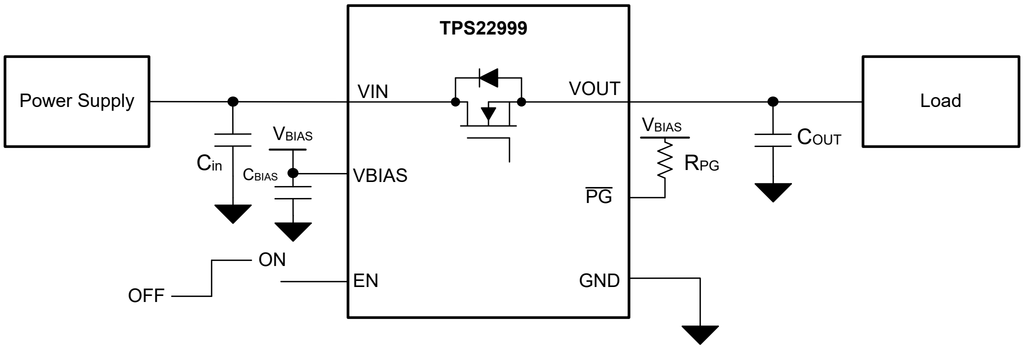


図 7-1. TPS22999 Basic Application

表 7-1. Component Descriptions

DESIGN PARAMETER	TYPICAL VALUES	DESCRIPTION
C_{IN}	1 µF	Filtering voltage transients
C_{OUT}	100 nF	Filtering voltage transients
C_{BIAS}	0.1 µF	Filtering voltage transients and noises
R_{PG}	10 kΩ	Pullup resistor for the open-drain output

7.2.1 Design Requirements

For this example, the values below are used as the design parameters.

表 7-2. Design Parameters

PARAMETER	VALUE
V_{BIAS}	3.4 V
V_{IN}	1.8 V
Load capacitance	60 µF
Inrush current	1 A

7.2.2 Detailed Design Procedure

When the switch is enabled, the switch charges up the output capacitance from 0 V to the set value (1.8 V in this example). This charge arrives in the form of inrush current. As the inrush current is controlled by the device, the time to fully charge up a capacitor can be calculated with the following formula:

$t_{charge}=V_{IN} / I_{inrush} \times C_L$

where:

- C_L is the output capacitance.
- I_{inrush} is the inrush current limited internally by the device
- V_{IN} is the input voltage

The TPS22999 offers an internally set inrush current limit (0.9-A typical with 3.4-V V_{BIAS}), which allows the customer to calculate the time to fully charge up a load capacitance.

$$t_{charge} = 1.8\text{ V} / 0.9\text{ A} \times 60\ \mu\text{F} \tag{1}$$

$$t_{charge} = 130\ \mu\text{s} \tag{2}$$

With TPS22999, the time to charge up a 60-µF capacitor to 1.8-V V_{IN} voltage is 130-µs typical at 3.4-V V_{BIAS} voltage.

7.3 Power Supply Recommendations

The TPS22999 device is designed to operate with a VIN range of 0.1 V to V_{BIAS} –1 V. Regulate the VIN power supply well and place as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input. TI recommends to connect a 0.1-uF capacitance to V_{BIAS}.

7.4 Layout

7.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, place the input and output capacitors close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

7.4.2 Layout Example

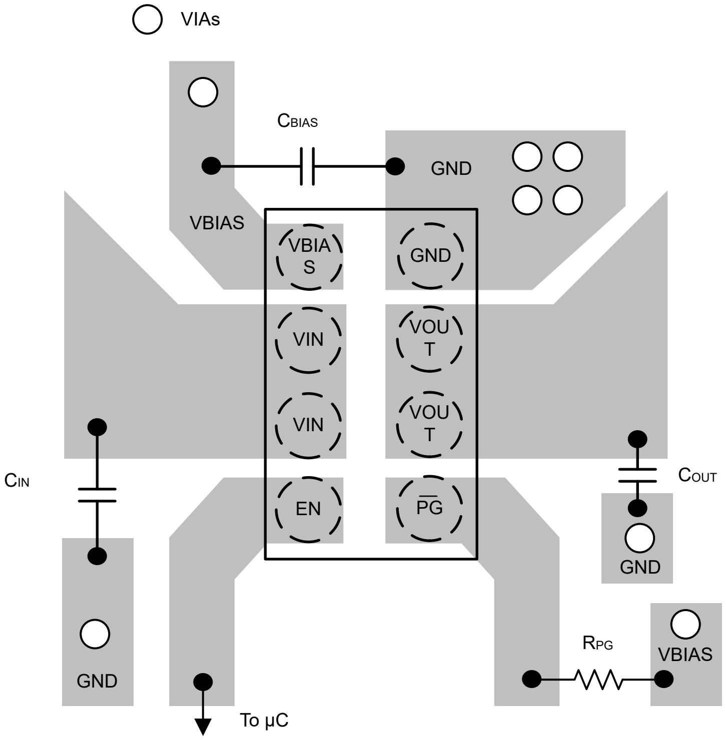


図 7-2. TPS22999 Layout Example

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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8.3 Trademarks

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8.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2023) to Revision A (November 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22999YCHR	ACTIVE	DSBGA	YCH	8	12000	TBD	Call TI	Call TI	-40 to 105		Samples
TPS22999YCHR	ACTIVE	DSBGA	YCH	8	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	R	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

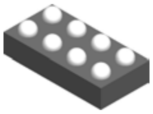
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

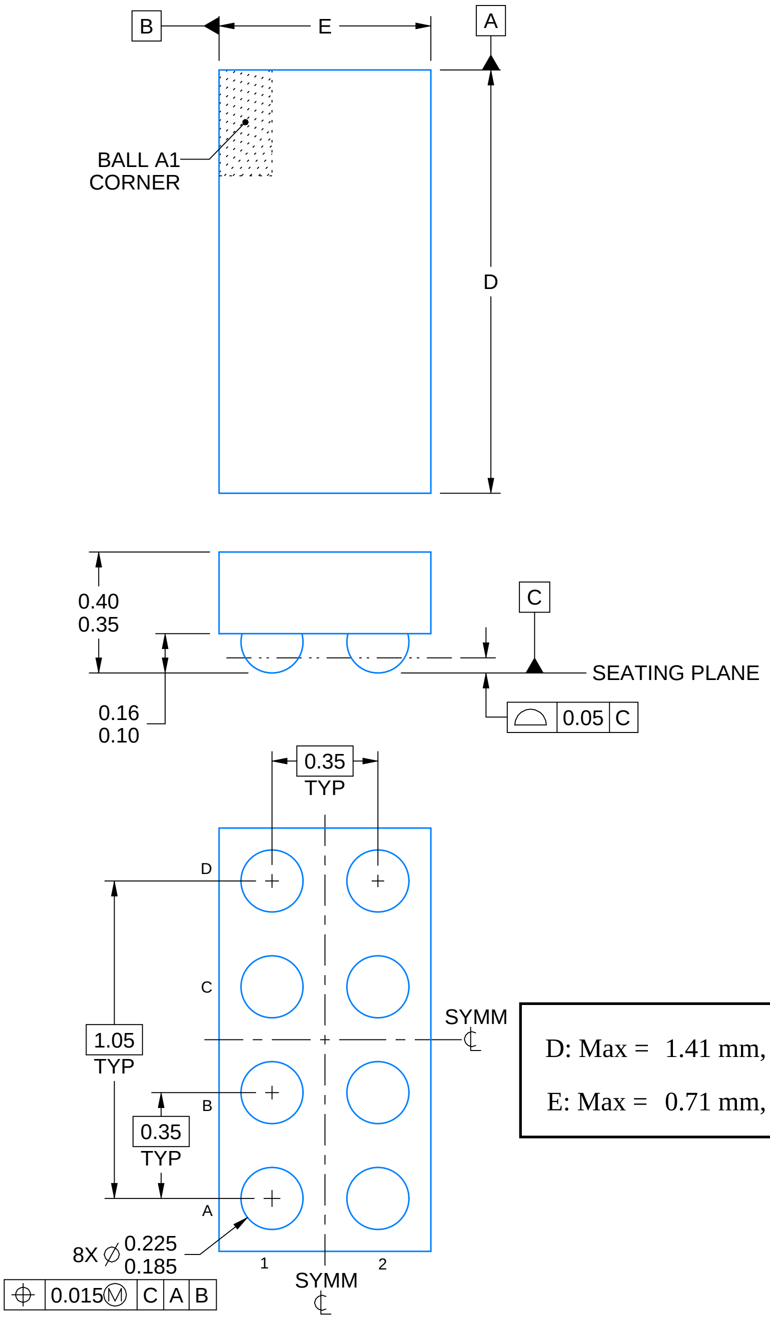
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.41 mm, Min = 1.35 mm

E: Max = 0.71 mm, Min = 0.65 mm

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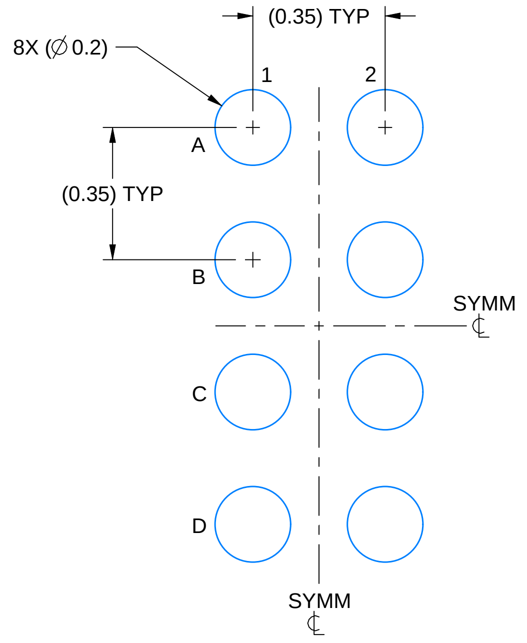
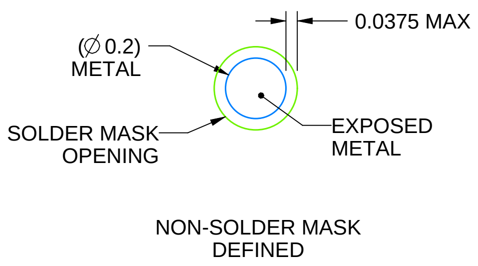
NOTES:

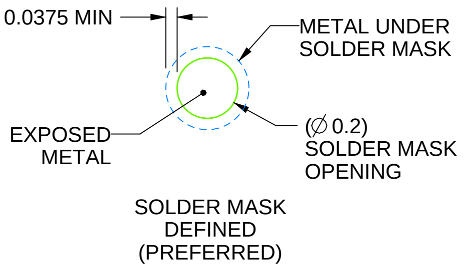
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



NON-SOLDER MASK
DEFINED



SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS
NOT TO SCALE

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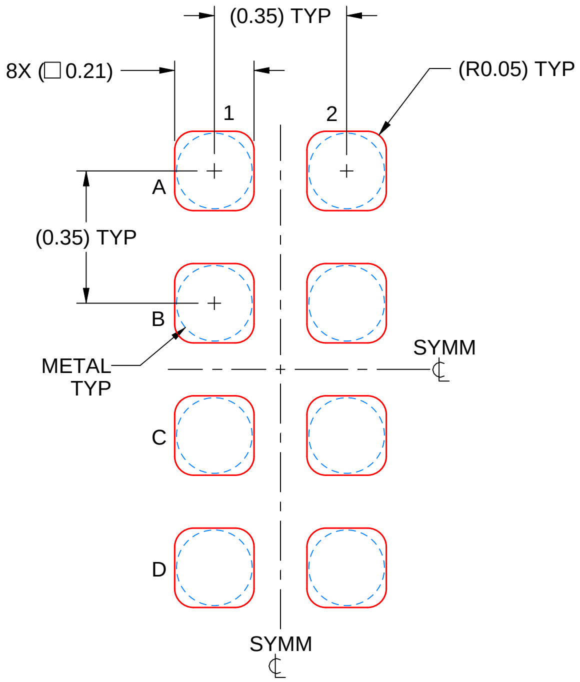
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265