TPS241x フル機能 N+1 および OR 接続電力レール・コントローラ

1 特長

- N+1 および OR 接続用の外部 FET を制御
- 広い電源電圧範囲: 3V～16.5V
- 0.8V～16.5V のバスを制御
- リニアまたはオン/オフ制御方式
- N チャネル MOSFET 用の内蔵チャージ・ポンプ
- デバイスの迅速なターンオフによりバスの整合性を保護
- 活線挿入時の正のゲート制御
- ソフト・ターンオンによりバスの過渡を低減
- 入力電圧の監視
- 短絡ゲートの監視
- MOSFET 制御状態インジケータ
- 産業用温度範囲：-40℃～85℃
- 業界標準の 14 ピン TSSOP パッケージ

2 アプリケーション

- ラック・サーバー (ラックマウント)
- ラック・サーバー (ブレード)
- 商用ネットワーク / サーバー PSU (電源)
- バッテリ・バックアップ・ユニット
- テレコム・システム

3 概要

TPS241x コントローラは、外部 N チャネル MOSFET と組み合わせることで、順方向電圧の低いダイオードの機能をエミュレートします。このデバイスを使用すると、N+1 構成で複数の電源を共通のバスに接続でき、または複数の冗長化入力電源バスを結合できます。TPS2410 はリニア・ターンオン制御方式を採用しており、TPS2411 はオン/オフ制御方式を採用しています。

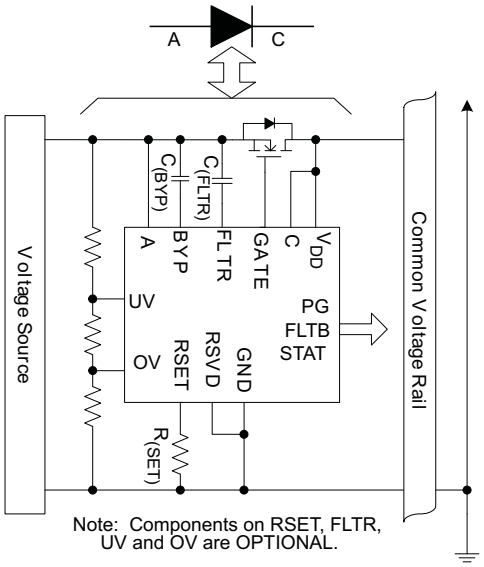
TPS2410x はサーバーやテレコムなどの広範なシステムに応用できます。これらのアプリケーションは多くの場合、N+1 冗長化電源、冗長化電源バス、またはこれらの両方を使用しています。これらの冗長化電源には、フォルトおよび活線挿入時の逆電流を防止するため、ダイオード OR と等価な機能が必要です。TPS241x と N チャネル MOSFET を使用すると、ショットキー・ダイオードより小さな電力損失でこの機能を実現できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS2410 TPS2411	TSSOP (14)	5.00mm×4.40mm
	UQFN (14)	2.50mm×2.50mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーションの図



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4 改訂履歴

Revision D (August 2019) から **Revision E** に変更 **Page**

- Changed Gate positive drive MAX voltage from 11.5 to 12.5 in the *Electrical Characteristics: TPS2410, 11* [(2) (3) (4) (5) (6) (7) (8)] table ... 9

Revision C (June 2019) から **Revision D** に変更 **Page**

- 「*製品情報*」表、「*ESD 定格*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- 「*アプリケーション*」の一覧を変更 ... 1
- Added the RMS (UQFN) pin configuration ... 6

Revision B (November, 2006) から **Revision C** に変更 **Page**

- Changed I/O entry and description of STAT in the *Pin Functions* table ... 5
- Changed STAT pullup voltage in the *Functional Block Diagram* ... 11
- Changed STAT definition ... 13
- Changed figure to show STAT connection ... 18

5 概要（続き）

正確な電圧センシング、プログラム可能な高速ターンオフ・スレッショルド、入力フィルタ処理により、広範な実装とバス特性に応じて動作をカスタマイズできます。

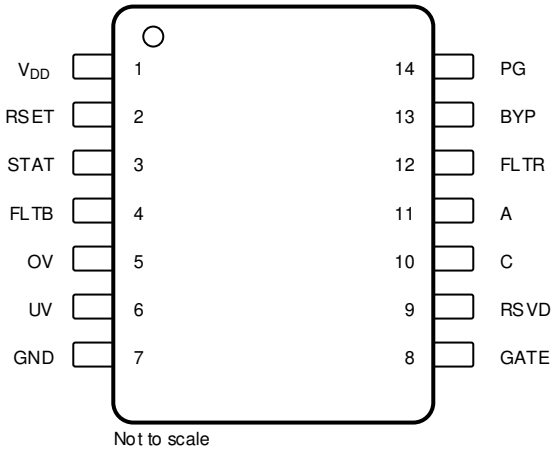
バス電圧の UV/OV、オン/オフ状態、MOSFET ゲートの短絡を検出するため、多くの監視機能を備えています。

6 Device Comparison

	TPS2410	TPS2411	TPS2412	TPS2413
Linear gate control	√		√	
ON/OFF gate control		√		√
Adjustable turn-off threshold	√	√	√	√
Fast comparator filtering	√	√		
Voltage monitoring	√	√		
Enable control	√	√		
Mosfet fault monitoring	√	√		
Status pin	√	√		

7 Pin Configuration and Functions

PW Package
TSSOP 14 Pin
Top View

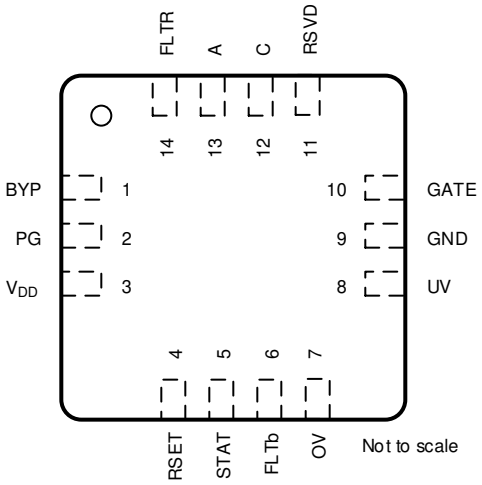


Not to scale

Pin Functions, PW

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	PWR	Input power for the gate drive charge pump and internal controls. V_{DD} must be connected to a supply voltage ≥ 3 V.
RSET	2	I	Connect a resistor to ground to program the turn-off threshold. Leaving RSET open results in a slightly positive $V_{(A-C)}$ turn-off threshold.
STAT	3	I/O	STAT is a multifunction pin. A high output indicates that the MOSFET gate is being driven high. Overdriving STAT low while GATE is high shifts the fast-turnoff threshold negative. STAT has a weak pull-up to V_{DD}.
FLTB	4	O	Open drain fault output. Fault is active (low) for any of the following conditions: • Insufficient V_{DD} • GATE should be high but is not. • The MOSFET should be ON but the forward voltage exceeds 0.4 V.
OV	5	I	OV is a voltage monitor that contributes to the PG output, and also causes the MOSFET to turn off if it is above the 0.6-V threshold. OV is programmable via an external resistor divider. An OV voltage above 0.6 V indicates a bus voltage that is too high.
UV	6	I	UV is a voltage monitor that contributes to the PG output. The UV input has a 0.6 V threshold and is programmable via an external resistor divider. A UV voltage above 0.6V indicates a bus voltage that is above its minimum acceptable voltage. A low UV input does not effect the gate drive.
GND	7	PWR	Device ground.
GATE	8	O	Connect to the gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
RSVD	9	PWR	This pin must be connected to GND.
C	10	I	Voltage sense input that connects to the simulated diode cathode. Connect to the MOSFET drain in the typical configuration.
A	11	I	Voltage sense input that connects to the simulated diode anode. A also serves as the reference for the charge-pump bias supply on BYP. Connect to the MOSFET source in the typical configuration.
FLTR	12	I	A capacitor connected from FLTR to A filters the input to the fast comparator. Filtering allows the TPS2410 to ignore spurious transients on the A and C inputs. This pin may be left open to achieve the fastest response time.
BYP	13	I/O	Connect a storage capacitor from BYP to A to filter the gate drive supply voltage.
PG	14	O	An open-drain Power Good indicator. PG is open if the UV input is above its threshold, the OV is below its threshold, and the internal UVLO is satisfied.

RMS Package
UQFN 14 Pin
Top View



Pin Functions, RMS

PIN		I/O	DESCRIPTION
NAME	NO.		
BYP	1	I/O	Connect a storage capacitor from BYP to A to filter the gate drive supply voltage.
PG;	2	O	An open-drain Power Good indicator. PG is open if the UV input is above its threshold, the OV is below its threshold, and the internal UVLO is satisfied.
V_{DD}	3	PWR	Input power for the gate drive charge pump and internal controls. V_{DD} must be connected to a supply voltage ≥ 3 V.
RSET	4	I	Connect a resistor to ground to program the turn-off threshold. Leaving RSET open results in a slightly positive $V_{(A-C)}$ turn-off threshold.
STAT	5	I/O	STAT is a multifunction pin. A high output indicates that the MOSFET gate is being driven high. Overdriving STAT low while GATE is high shifts the fast-turnoff threshold negative. STAT has a weak pull-up to V_{DD}.
FLTB	6	O	Open drain fault output. Fault is active (low) for any of the following conditions: • Insufficient V_{DD} • GATE should be high but is not. • The MOSFET should be ON but the forward voltage exceeds 0.4 V.
OV	7	I	OV is a voltage monitor that contributes to the PG output, and also causes the MOSFET to turn off if it is above the 0.6-V threshold. OV is programmable via an external resistor divider. An OV voltage above 0.6 V indicates a bus voltage that is too high.
UV	8	I	UV is a voltage monitor that contributes to the PG output. The UV input has a 0.6 V threshold and is programmable via an external resistor divider. A UV voltage above 0.6V indicates a bus voltage that is above its minimum acceptable voltage. A low UV input does not effect the gate drive.
GND	9	PWR	Device ground.
GATE	10	O	Connect to the gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
RSVD	11	PWR	This pin must be connected to GND.
C	12	I	Voltage sense input that connects to the simulated diode cathode. Connect to the MOSFET drain in the typical configuration.
A	13	I	Voltage sense input that connects to the simulated diode anode. A also serves as the reference for the charge-pump bias supply on BYP. Connect to the MOSFET source in the typical configuration.
FLTR	14	I	A capacitor connected from FLTR to A filters the input to the fast comparator. Filtering allows the TPS2410 to ignore spurious transients on the A and C inputs. This pin may be left open to achieve the fastest response time.

8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
	A, C, FLTR, V_{DD}, STAT voltage	–0.3	18	V
	A above C voltage(2)		7.5	V
	C above A voltage		18	V
	GATE(3), BYP voltage	–0.3	30	V
	BYP(3) to A voltage	–0.3	13	V
	GATE above BYP voltage		0.3	V
	FLTR(3) to C voltage	–0.3	0.3	V
	OV, UV voltage	–0.3	5.5	V
	RSET voltage(3)	–0.3	7	V
	FLTB, PG voltage	–0.3	18	V
	STAT, PG, FLTB sink current		40	mA
	GATE short to A or C or GND	Indefinite		
T_J	Maximum junction temperature	Internally limited		°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the section "Bidirectional Blocking and Protection of C."
(3) Voltage should not be applied to these pins.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

8.3 Recommended Operating Conditions

voltages are referenced to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
A, C	Input voltage range TPS2410	$V_{DD} = V_{(C)}$ (1)	3		16.5	V
		$3 \le V_{DD} \le 16.5$ V	0.8		16.5	
A to C	Operating voltage(2)				5	V
OV, UV	Voltage range		0		5.25	V
STAT, PG, FLTB	Continuous sinking current				6.8	mA
$R_{(RSET)}$	Resistance range(3)		1.5		∞	kΩ
$C_{(FLTR)}$	Capacitance Range(3)		0		1000	pF
$C_{(BYP)}$	Capacitance Range(3) (4)		800	2200	10k	pF
T_J	Operating junction temperature		–40		125	°C
T_A	Operating free-air temperature		–40		85	°C

(1) V_{DD} must exceed 3 V to meet GATE drive specifications
(2) See the section "Bidirectional Blocking and Protection of C."
(3) Voltage should not be applied to these pins.
(4) Capacitors should be X7R, 20% or better

8.4 Thermal Information

THERMAL METRIC[1]		TPS2410 TPS2411		UNIT
		PW (TSSOP)	RMS (UQFN)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	148.3	82.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.1	33.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.7	32.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.9	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.8	32.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics*, application report.

8.5 Electrical Characteristics: TPS2410, 11[1] [2] [3] [4] [5] [6] [7]

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(A)}$, $V_{(C)}$, V_{DD}					
V_{DD} UVLO	V_{DD} rising	2.25		2.5	V
	Hysteresis		0.25		
A current	| $I_{(A)}$ |, Gate in active range		0.66	1	mA
	| $I_{(A)}$ |, Gate saturated high		0.1		
C current	| $I_{(C)}$ |, V_{AC} ≤ 0.1 V			10	µA
V_{DD} current	Worst case, gate in active range		4.25	6	mA
	Gate saturated high		1.2		
UV / OV / PG					
UV threshold voltage	$V_{(UV)}$ rising, $V_{(OV)}$ = 0 V, PG goes high	0.583	0.6	0.615	V
OV threshold voltage	$V_{(OV)}$ rising, $V_{(UV)}$ = 1 V, PG goes low	0.583	0.6	0.615	V
Response time	50-mV overdrive		0.3	0.6	µs
Hysteresis	$V_{(UV)}$ and $V_{(OV)}$		7		mV
PG sink current	$V_{(UV)}$ = 0 V, $V_{(OV)}$ = 0 V, $V_{(PG)}$ = 0.4 V	4			mA
UV / OV leakage current (source or sink)				1	µA
PG leakage current (source or sink)	$V_{(UV)}$ = 1 V, $V_{(OV)}$ = 0 V, 0 ≤ $V_{(PG)}$ ≤ 5 V			1	µA
FLTB					
Sink current	$V_{(FLTB)}$ = 0.4 V, $V_{(GATE-)A}$ = 0 V, $V_{(A-C)}$ = 0.1 V	4			mA
$V_{(GATE-A)}$ fault threshold	$V_{(A)}$ = $V_{(C)}$ + 20 mV, $V_{(GATE-A)}$ falling until FLTB switches low	0.5	0.78	1	V
$V_{(A-C)}$ fault threshold	$V_{(A-C)}$ = 0.1 V, increase $V_{(A-C)}$ until FLTB switches low	0.325	0.425	0.525	V
Deglitch on assertion			3.4		ms
Leakage current (source or sink)				1	µA
STAT					
Sink current	$V_{(STAT)}$ = 0.4 V, $V_{(A)}$ = $V_{(C)}$ + 0.1 V	4			mA
Input threshold	V_{DD} ≥ 3 V		V_{DD}/2		V
Response time	From fast turn-off initiation			50	ns

(1) [3 V ≤ $V_{(A)}$ ≤ 18 V, $V_{(C)}$ = V_{DD}] or [0.8 V ≤ $V_{(A)}$ ≤ 3 V, 3 V ≤ V_{DD} ≤ 18 V]
(2) $C_{(FLTR)}$ = open, $C_{(BYP)}$ = 2200 pF, $R_{(RSET)}$ = open, STAT = open, FLT = open
(3) UV = 1 V, OV = GND
(4) –40°C ≤ T_J ≤ 125°C
(5) Positive currents are into pins
(6) Typical values are at 25°C
(7) All voltages are with respect to GND.

Electrical Characteristics: TPS2410, 11(1) (2) (3) (4) (5) (6) (7) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source pull-up resistance		30	46	60	kΩ
FLTR					
Filter resistance	$R_{(FLTR-C)}$		520		Ω
TURN ON					
TPS2410 forward turn-on and regulation voltage		7	10	13	mV
TPS2410 forward turn-on / turn-off difference	$R_{(RSET)}$ = open		7		mV
TPS2411 forward turn-on voltage		7	10	13	mV
TURN OFF					
Fast turn-off threshold voltage	GATE sinks > 10 mA at $V_{(GATE-A)}$ = 2 V				mV
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = open	1	3	5	
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = 28.7 kΩ	-17	-13.25	-10	
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = 3.24 kΩ	-170	-142	-114	
Additional threshold shift with STAT held low			-157		mV
Turn-off delay	$V_{(A)}$ = 12 V, $V_{(A-C)}$: 20 mV → -20 mV, $V_{(GATE-A)}$ begins to decrease		70		ns
Turn-off time	$V_{(A)}$ = 12 V, $C_{(GATE-GND)}$ = 0.01 µF, $V_{(A-C)}$: 20 mV → -20 mV, measure the period to $V_{(GATE)} = V_{(A)}$		130		ns
GATE					
Gate positive drive voltage, $V_{(GATE-A)}$	V_{DD} = 3 V, $V_{(A-C)}$ = 20 mV	6	7	8	V
	5 V ≤ V_{DD} ≤ 18 V, $V_{(A-C)}$= 20 mV	9	10.2	12.5	
Gate source current	$V_{(A-C)}$ = 50 mV, $V_{(GATE-A)}$ = 4 V	250	290	350	µA
Soft turn-off sink current (TPS2410)	$V_{(A-C)}$ = 4 mV, $V_{(GATE-A)}$ = 2 V	2	5		mA
Fast turn-off pulsed current, $I_{(GATE)}$	$V_{(A-C)}$ = -0.1 V				A
	$V_{(GATE)}$ = 8 V	1.75	2.35		
	$V_{(GATE)}$ = 5 V	1.25	1.75		
	Period	7.5	12.5		µs
Sustain turn-off current, $I_{(GATE)}$	$V_{(A-C)}$ = –0.1 V, $V_{(C)} = V_{DD}$, 3 ≤ V_{DD} ≤ 18 V, 2 V ≤ $V_{(GATE)}$ ≤ 18 V	15	19.5		mA
MISCELLANEOUS					
Thermal shutdown temperature	Temperature rising, T_J		135		°C
Thermal hysteresis			10		°C

8.6 Typical Characteristics

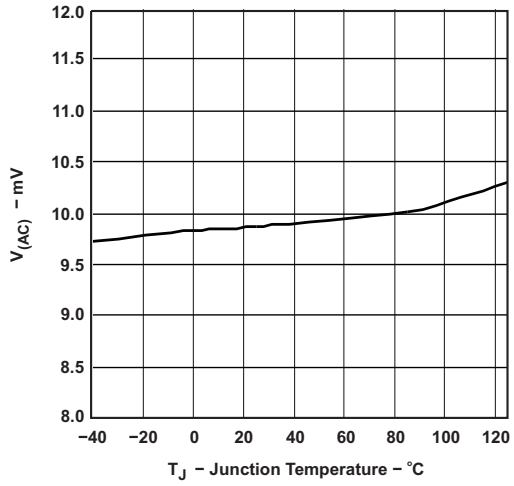


Figure 1. TPS2410 $V_{(AC)}$ Regulation Voltage vs Temperature

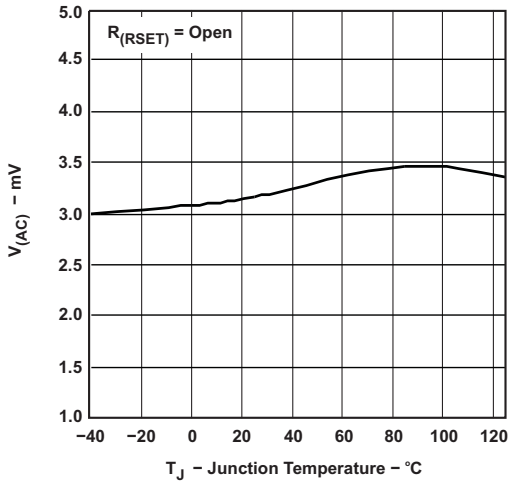


Figure 2. Fast Turnoff Threshold vs Temperature

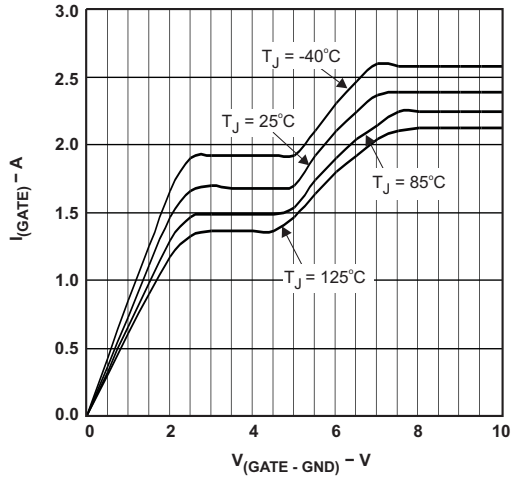


Figure 3. Pulsed Gate Sinking Current vs Gate Voltage

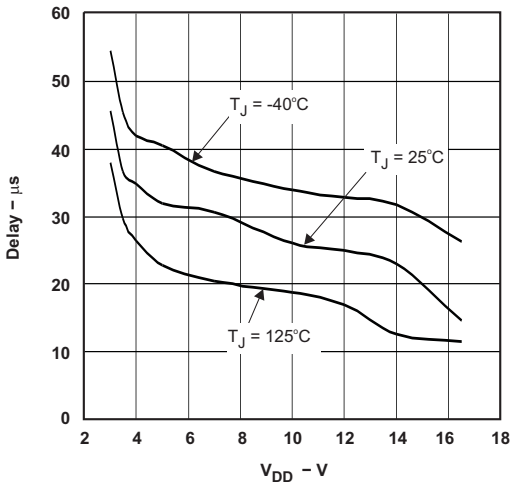


Figure 4. Turnon Delay vs V_{DD} (Power Applied Until Gate Is Active)

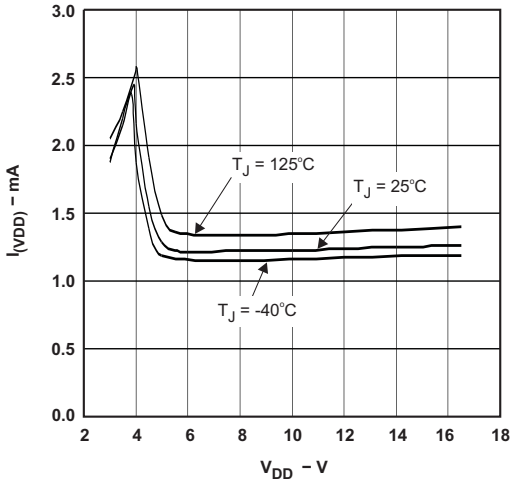


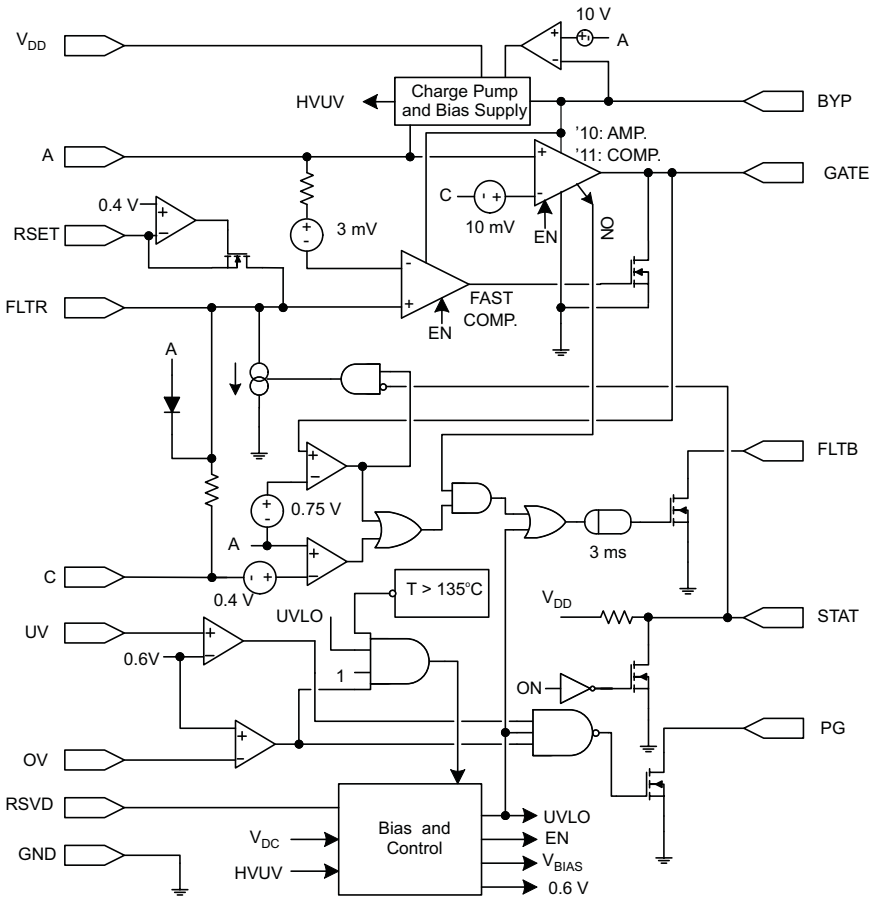
Figure 5. V_{DD} Current vs V_{DD} Voltage (Gate Saturated High)

9 Detailed Description

9.1 Overview

The TPS2410 and TPS2411 are designed to allow output ORing in N+1 power supply applications (see Figure 10) and input-power bus ORing in redundant source applications (see Figure 11). The device and external MOSFET emulate a discrete diode to perform this unidirectional power combining function. The advantage to this emulation is lower forward voltage drop and the ability to tune operation.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Device Pins

The following descriptions refer to the pinout of the device.

9.3.1.1 A, C:

The A pin serves as the simulated diode anode and the C as the cathode. GATE is driven high when $V_{(AC)}$ exceeds 10 mV. Both devices provide a strong GATE pull-down when $V_{(AC)}$ is less than the programmable fast turn-off threshold. The TPS2410 has a soft pull-down when $V_{(AC)}$ is less than 10 mV but above the fast turn-off threshold.

Several internal comparator and amplifier circuits monitor these two pins. The inputs are protected from excess differential voltage by a clamp diode and series resistance. If C falls below A by more than about 0.7 V, a small current flows out of A. Protect the internal circuits with an external clamp if C can be more than 6 V lower than A. A small signal clamp diode and 1-kΩ resistor, or circuit per Figure 13 are suitable.

Feature Description (continued)

The internal charge pump output, which provides bias power to the comparators and voltage to drive GATE, is referenced to A. Some charge pump current appears on A due to this topology. The A and C pins should be Kelvin connected to the MOSFET source and drain. A and C connections should also be short and low impedance, with special attention to the A connection. Residual noise from the charge pump can be reduced with a bypass capacitor at A if the application permits.

9.3.1.2 BYP:

BYP is the internal charge pump output, and the positive supply voltage for internal comparator circuits and GATE driver. A capacitor must be connected from BYP to A. While the capacitor value is not critical, a 2200-pF ceramic is recommended. Traces to this part must be kept short and low impedance to provide adequate filtering. Shorting this pin to a voltage below A damages the TPS2410/11.

9.3.1.3 FLTR:

The internal fast comparator input may be filtered by placing a small capacitor from FLTR to A. This is useful in situations where the ambient noise or transients might falsely trigger a MOSFET turnoff. While $C_{(FLTR)}$ suppresses small transients, large voltage reversals have a relatively small additional turn-off delay.

FLTR is clamped to C and should only be used with a capacitor as shown in Figure 6. Connections to FLTR should be short and direct to minimize parasitic capacitive loading and crosstalk. The filter pin may not be shorted to any other voltage.

9.3.1.4 FLTB:

The FLTB pin is the open-drain fault output. FLTB sinks current when the MOSFET should be enabled, but either there is no GATE voltage, $V_{(AC)}$ is greater than 0.4 V with GATE driven ON, the internal UVLO is not satisfied. FLTB has a 3-ms deglitch filter on the falling edge to prevent transients from creating false signals. FLTB may not be valid at voltages below the internal V_{DD} UVLO.

9.3.1.5 GATE:

Gate connects to the external N channel MOSFET gate. GATE is driven positive with respect to A by a driver operating from the voltage on BYP. A time-limited high current discharge source pulls GATE to GND when the fast turn-off comparator is activated. The high-current discharge is followed by a sustaining pull-down. The turn-off circuits are disabled by the thermal shutdown, leaving a resistive pull-down to keep the gate from floating. The gate connection should be kept low impedance to maximize turn-off current.

9.3.1.6 GND:

This is the input supply reference. GND should have a low impedance connection to the ground plane. It carries several Amperes of rapid-rising discharge current when the external MOSFET is turned off, and also carries significant charge pump currents.

9.3.1.7 RSET:

A resistor connected from this pin to GND sets the MOSFET fast turn-off comparator threshold. The threshold is slightly positive when the RSET pin is left open. Current drawn by the resistor programs the turn-off voltage to increasing negative values. The TPS2411 must have a negative threshold programmed to avoid an unstable condition at light load. The expression for R(RSET) in terms of the fast comparator-trip voltage, $V_{(OFF)}$, follows.

$$R_{(RSET)} = \left(\frac{-470.02}{V_{(OFF)} - 0.00314} \right) \quad (1)$$

The units of the numerator are (V × V/A). $V_{(OFF)}$ is positive for $V_{(A)}$ greater than $V_{(C)}$, $V_{(OFF)}$ is less than 3 mV, and $R_{(RSET)}$ is in ohms.

9.3.1.8 RSVD:

Connect to ground.

Feature Description (continued)

9.3.1.9 STAT

STAT is a multifunction pin. STAT outputs the status of the GATE pin drive. The internal weak pull-up pulls STAT to V_{DD} when GATE is being driven high and $V_{(GATE)}$ is 0.4 V greater than $V_{(A)}$. If STAT is externally pulled below $V_{DD}/2$ while the pin is high, the turnoff threshold is shifted negative (~157 mV) from the RSET programmed value. Interconnecting the STAT pins of redundant devices, in systems that normally have both devices on, reduces the likelihood that both devices turn off in the event of a transient. See the *Functional Block Diagram*, *INPUT ORing and STAT*, and Figure 11.

9.3.1.10 UV, OV, PG:

These signals are used to monitor an input voltage for proper range. PG sinks current to GND if UV is below its threshold, OV is above its threshold, or $V_{D\ D}$ is below the internal UVLO. PG may not be valid when V_{DD} is below the UVLO.

A high input on OV causes GATE to be driven low. UV does not effect the MOSFET operation. This permits OV to be used as an active-high disable.

OV and UV should be connected to ground when not used, and PG may be left open. Multiple PG pins to be wire ORed using a common pull-up resistor.

9.3.1.11 V_{DD}:

V_{DD} is the primary supply for the gate drive charge pump and other internal circuits. This pin must be connected a source that is 3 V or greater when the external MOSFET is to be turned on. V_{DD} may be greater or lower than the controlled bus voltage.

A 0.01-µF bypass capacitor, or 10-Ω and a 0.0 1-µF filter, is recommended because charge pump currents are drawn through V_{DD}.

9.3.2 Gate Drive, Charge Pump and $C_{(BYP)}$

Gate drive of 270 µA typical is generated by an internal charge pump and current limiter. A separate supply, V_{DD}, is provided to avoid having the large charge pump currents interfere with voltage sensing by the A and C pins. The GATE drive voltage is referenced to $V_{(A)}$ as GATE is only driven high when $V_{(A)} > V_{(C)}$. The recommended capacitor on BYP (bypass) must be used in order to form a quiet supply for the internal high-speed comparator. $V_{(GATE)}$ must not exceed $V_{(BYP)}$.

9.3.3 Fast Comparator Input Filtering – $C_{(FLTR)}$

The FLTR (filter) pin enables a simple method of filtering the input to the fast turn-off comparator as demonstrated in Figure 6. To minimize the impact of a bus fault, the ORing controller turns off the external MOSFET as fast as possible when a voltage reversal occurs. However, having a fast reaction increases the likelihood that noise or non-fault transients may cause false triggering. Examples of such transients are ESD, EFT, RF induction, step loads, and insertion of high-inrush units. The effect of the filter on a time-domain transient are illustrated by assuming a step input from positive to negative. The expression for the time to reach 0 V across the fast comparator inputs follows, where the variables are defined in Figure 6.

$$t_{DLY} = -\left(R \times C_{(FLTR)}\right) \times \ln\left(\frac{v_2}{v_2 - v_1}\right) \quad (2)$$

Figure 6 graphically illustrates that the external MOSFET is turned off after a longer delay for a small transient than a large voltage reversal. For example, the delay from 10 mV forward to 10-mV reverse is about 52 ns (R = 520 Ω, C = 150 pF), while the delay for a 100-mV reverse transient is 7 ns. It is unlikely that the transient in a real system is a step response, making exact calculations on the effect of the R-C filter to a specific transient difficult.

The need for a $C_{(FLTR)}$, and its value, is dependent on the electrical noise environment of the particular system. If the electrical environment is understood, the need for the filter, or its value, is selected based on approximations or simulations. If the system is not understood or does not exist when the TPS2410 circuit design is completed, it is recommended that a $C_{(FLTR)}$ of 100 pF be included in initial schematics. Evaluation of system performance may allow removal of $C_{(FLTR)}$. The tolerance of the internal resistance is about ±25% including temperature variations.

Feature Description (continued)

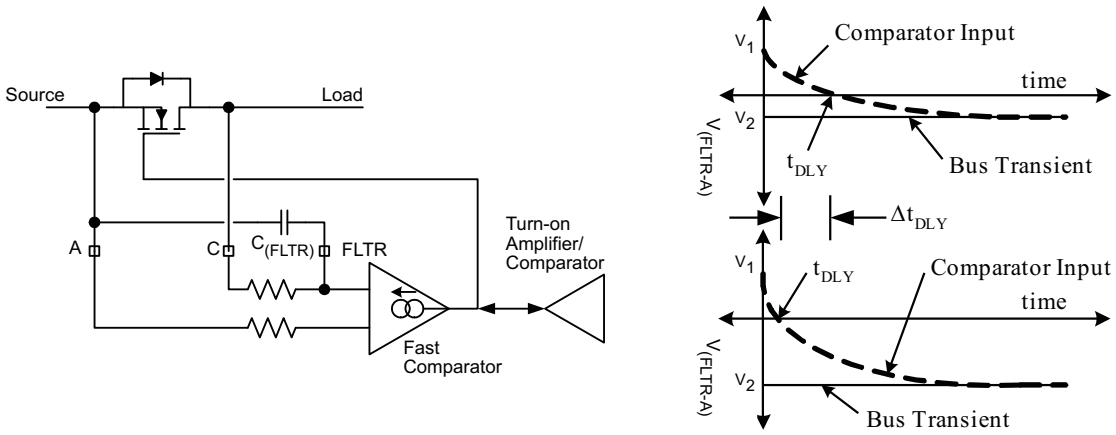


Figure 6. Fast Comparator Input Filtering

9.3.4 UV, OV, and PG

The UV and OV inputs can be used in a several ways. These include voltage monitoring and forcing the pass MOSFET off.

A voltage bus may be monitored for undervoltage with the UV pin, and overvoltage with the OV pin. Figure 7 demonstrates a basic three resistor divider, however, two separate two resistor dividers may be used. PG is high if $V_{(UV)}$ exceeds the UV threshold, and $V_{(OV)}$ is below the OV threshold, else PG is low. Each of these inputs has a 0.6-V threshold and 7 mV of hysteresis. Optionally, UV and OV may be independently disabled by connecting them to ground, and PG may be left floating if not used. The state of PG is undefined until the internal UVLO is satisfied.

GATE is forced low if $V_{(OV)}$ exceeds 0.6 V. This allows OV to be used as an enable as shown in Figure 7. This can be used for testing purposes, or control of back-to-back MOSFETs to force an output off even though $V_{(AC)}$ is greater than 10 mV.

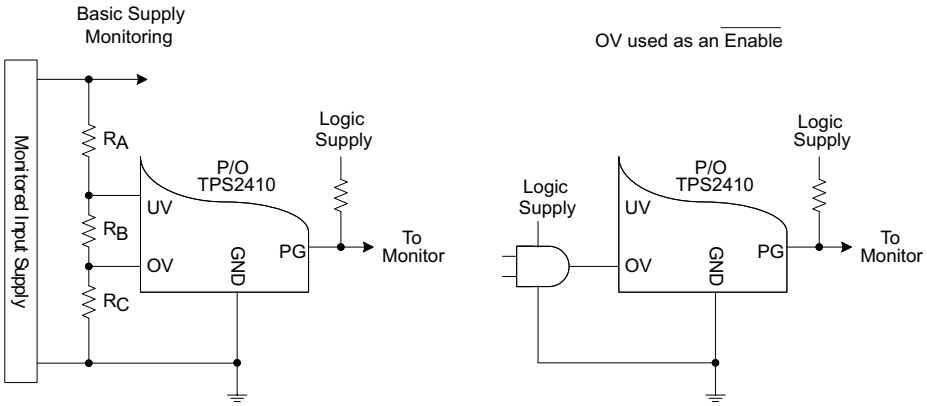


Figure 7. UV, OV, AND PG

9.3.5 Input ORing and Stat

STAT provides information regarding the state of the MOSFET gate drive. STAT is pulled to V_{DD}, through a 46-kΩ internal pullup, if GATE is being driven high and $V_{(GATE)}$ exceeds $V_{(A)}$ plus 0.4 V. The STAT pin may be directly connected to low-voltage logic by using the logic gate input ESD clamp to control the voltage or by using a much lower pullup resistor (that is, 5 kΩ) to the logic supply voltage. STAT must be allowed to rise above $V_{DD}/2$ to avoid effecting the reverse turn-off threshold.

Feature Description (continued)

Interconnecting STAT pins can be used to reduce the occurrence of both MOSFETs turning off in topologies such as Figure 11 that normally have both MOSFETs ON. This might occur when there is a noise transient on both buses due to fans cycling on and off, or an ac mains disturbance. If both MOSFETs are ON, and then an ORing circuit turns OFF, the second ORing circuit fast turnoff threshold is shifted negative by 157 mV from the RSET programmed value because STAT is pulled low. This reduces the probability that it too turns off as the arrival of the transient, and speed of both circuits, is unlikely to be matched. Maintaining at least one device ON avoids both a bus transient due to the current interruption, and momentary downstream hotswap overload when the ORing recovers. The function of STAT is not limited to the topology of Figure 11 and may be used to dynamically shift the fast turnoff threshold. The internal circuit shown in the *FUNCTIONAL BLOCK DIAGRAM* assists in designing these applications.

Figure 8 shows how STAT and OV can be used to latch the TPS2410 off. This is useful when a system operation benefits from preventing a failed power module from repeatedly disturbing the bus, and may be used in conjunction with back-to-back MOSFETs. The OV pin must be help low until $V_{(GATE)}$ is 0.4 V above $V_{(A)}$ in order to accomplish a reset.

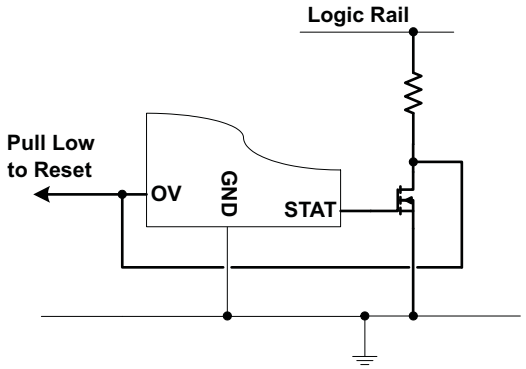


Figure 8. Use of STAT and OV to Latch TPS2411 OFF

9.4 Device Functional Modes

9.4.1 TPS2410 vs TPS2411 – MOSFET Control Methods

The TPS2410 turns the MOSFET on with a linear control loop that regulates $V_{(AC)}$ to 10 mV as shown in Figure 9. With the gate low, and $V_{(AC)}$ increasing to 10 mV, the amplifier drives GATE high with all available output current until regulation is reached. The regulator controls $V_{(GATE)}$ to maintain $V_{(AC)}$ at 10 mV as long as the MOSFET $r_{DS(on)} \times I_{(DRAIN)}$ is less than this the regulated voltage. The regulator drives GATE high, turning the MOSFET fully ON when the $r_{DS(on)} \times I_{(DRAIN)}$ exceeds 10 mV; otherwise, $V_{(GATE)}$ is near $V_{(A)}$ plus the MOSFET gate threshold voltage. If the external circuits force $V_{(AC)}$ below 10 mV and above the programmed fast turnoff, GATE is slowly turned off. GATE is rapidly pulled to ground if $V_{(AC)}$ falls to the RSET programmed fast turn-off threshold.

The TPS2411 turns the MOSFET on and off like a comparator with hysteresis as shown in Figure 9. GATE is driven high when $V_{(AC)}$ exceeds 10 mV, and rapidly turned off if $V_{(AC)}$ falls to the RSET programmed fast turn-off threshold.

System designs should account for the inherent delay between a device circuit becoming forward biased, and the MOSFET actually turning ON. The delay is the result of the MOSFET gate capacitance charge from ground to its threshold voltage by the 270 μA gate current. If there are no additional sources holding the ORed rail voltage up, the MOSFET internal diode conductd and maintain voltage on the ORed output, but there is some voltage droop. This condition is analogous to the power source being ORed in this case. The DC/DC converter output voltage droops when its load increases from zero to a high value. Load sharing techniques that keep all ORed sources active solve this condition.

Device Functional Modes (continued)

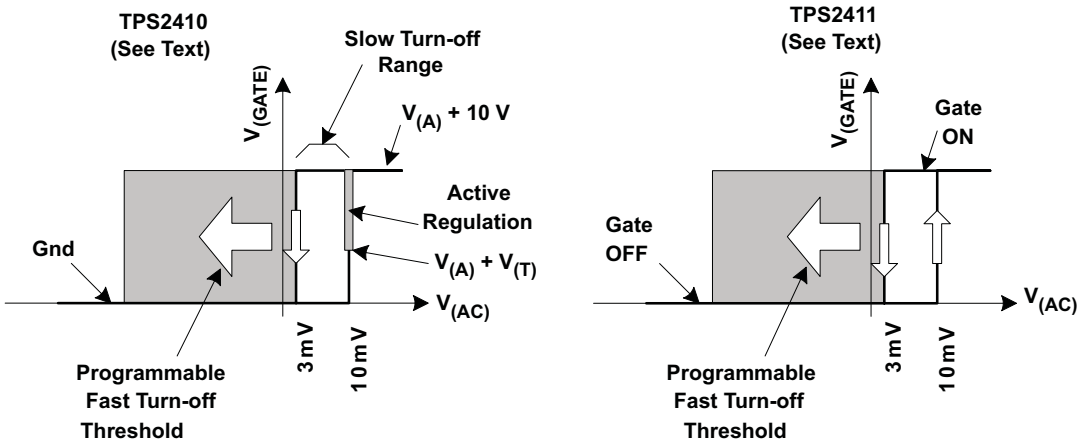


Figure 9. TPS2410, TPS2411 Operation

The operation of the two parts is summarized in Table 1.

Table 1. Operation as a Function of V_{AC}

	$V_{(AC)}$ ≤ Turnoff Threshold(1)	Turnoff Threshold(1) ≤ V_{AC} ≤ 10 mV		$V_{(AC)}$ > 10 mV
		$V_{(AC)}$ Forced < 10 mV	(MOSFET $r_{DS(on)}$ × I_{LOAD}) ≤ 10 mV	
TPS2410	Strong GATE pull-down (OFF)	Weak GATE pull-down (OFF)	$V_{(AC)}$ regulated to 10 mV	GATE pulled high (ON)
TPS2411	Strong GATE pull-down (OFF)	Depends on previous state (Hysteresis region)		GATE pulled high (ON)

(1) Turnoff threshold is established by the value of RSET.

The TPS2410 control method yields several benefits. First, the low current GATE driver provides a gentle turn-on and turn-off for slowly rising and falling input voltage. Second, it reduces the tendency for on/off cycling of a comparator based solution at light loads. Third, it avoids reverse currents if the fast turn-off threshold is left positive. The drawback to this method is that the MOSFET appears to have a high resistance at light load when the regulation is active. A momentary output voltage droop occurs when a large step load is applied from a light-load condition. The TPS2410 is a better solution for a mid-rail bus that is re-regulated.

The TPS2411 turns the MOSFET on if $V_{(AC)}$ is greater than 10 mV, and hard off when $V_{(AC)}$ is less than the RSET programmed threshold. There is no linear control range and slow turn-off. The disadvantage is that the turn-off threshold must be negative (unless a specified load is always present) permitting a continuous reverse current. Under a dynamic reverse voltage fault, the lower threshold voltage may permit a higher peak reverse current. There are a number of advantages to this control method. Step loads from a light load condition are handled without a voltage droop beyond I × R. If the redundant converter fails, applications with redundant synchronous converters may permit a small amount of reverse current at light load in order to assure that the MOSFET is all ready on. The TPS2411 is a better solution for low-voltage busses that are not re-regulated, and that may see large load steps transients.

These applications recommendations are meant as a starting point, with the needs of specific implementations over-riding them.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Typical Connections

10.1.1 N+1 Power Supply

The N+1 power supply configuration shown in Figure 10 is used where multiple power supplies are paralleled for either higher capacity, redundancy or both. If it takes N supplies to power the load, adding an extra, identical unit in parallel permits the load to continue operation in the event that any one of the N supplies fails. The supplies are ORed together, rather than directly connected to the bus, to isolate the converter output from the bus when it is plugged-in or fails short. The TPS2410 and TPS2411 with an external MOSFET emulates the function of the ORing diode.

It is possible for a malfunctioning converter in an ORed topology to create a bus overvoltage if the loading is less than the converter's capacity (that is, N = 1). The ORed topology shown cannot protect the bus from this condition, even if the ORing MOSFET can be turned off. One common solution is to use two MOSFETs in a back-to-back configuration to provide bidirectional blocking. See the section on *BIDIRECTIONAL BLOCKING AND PROTECTION OF C*.

ORed supplies are usually designed to share power by various means, although the desired operation could implement an active and standby concept. Sharing approaches include both passive, or voltage droop, and active methods. Not all of the output ORing devices may be active depending on the sharing control method, bus loading, distribution resistences, and device settings.

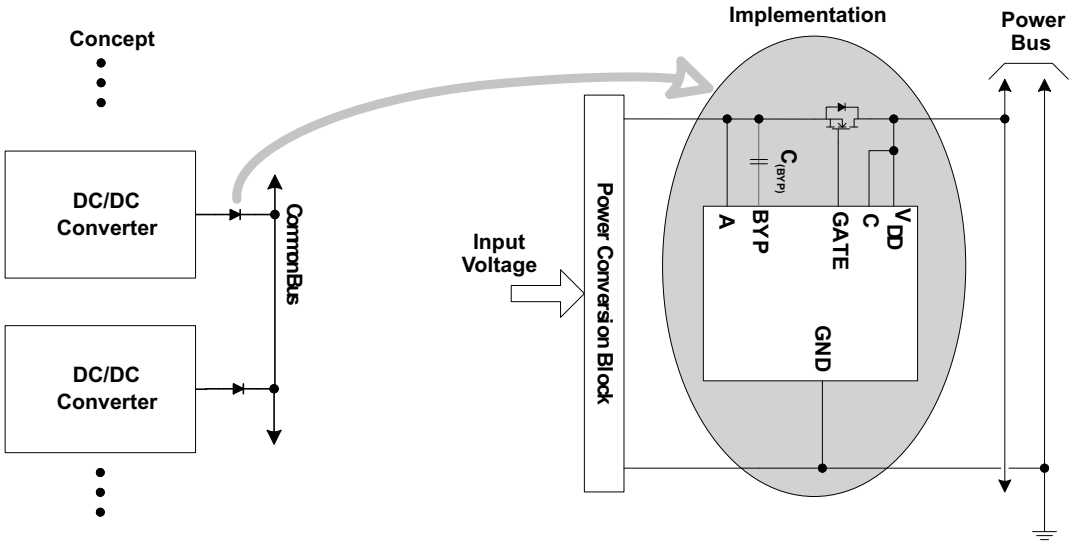


Figure 10. N+1 Power Supply Example

Typical Connections (continued)

10.1.2 Input ORing

Figure 11 shows how redundant buses may be ORed to a common point to achieve higher reliability. It is possible to have both MOSFETs ON at once if the bus voltages are matched, or the combination of tolerance and regulation causes both TPS2410 and TPS2411 circuits to see a forward voltage. The ORing MOSFET disconnects the lower-voltage bus, protecting the remaining bus from potential overload by a fault.

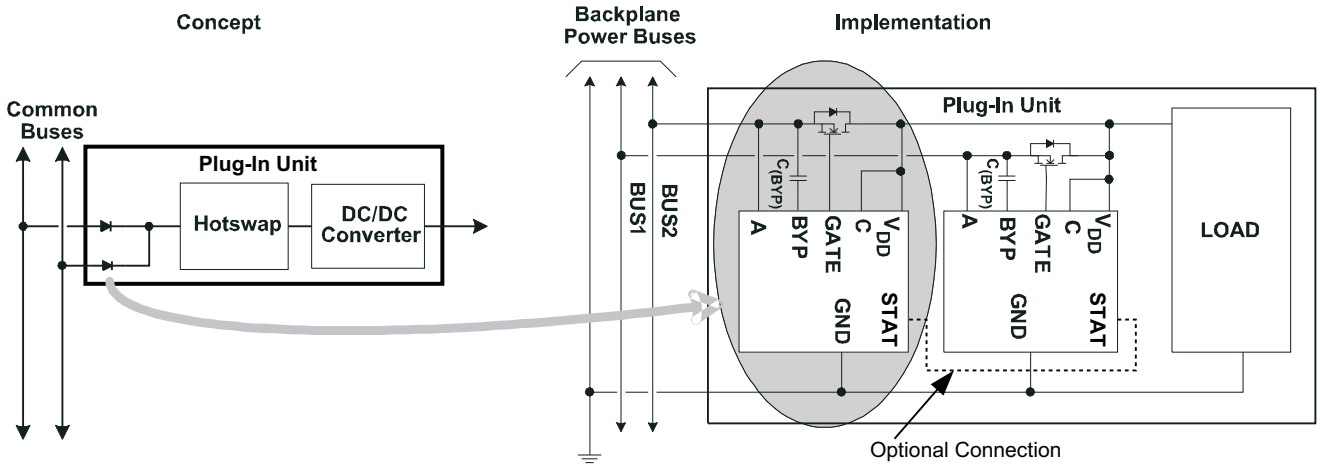


Figure 11. Example ORing of Input Power Buses

10.2 Typical Application Examples

10.2.1 V_{DD}, BYP, and Powering Options

The separate V_{DD} pin provides flexibility for operational power and controlled rail voltage. While the internal UVLO has been set to 2.5 V, the device requires at least 3 V to generate the specified GATE drive voltage. Sufficient BYP voltage to run internal circuits occurs at V_{DD} voltages between 2.5 V and 3 V. There are three choices for power, A, C, or a separate supply, two of which are demonstrated in Figure 12. One choice for voltage rails over 3.3 V is to power from C, since it is typically the source of reliable power. Voltage rails below 3.3 V, that is, 2.5 V and below, should use a separate supply such as 5 V. A separate V_{DD} supply can be used to control voltages above it, for example 5 V powering V_{DD} to control a 12-V bus.

V_{DD} is the main source of power for the internal control circuits. The charge pump that powers BYP draws most of its power from V_{DD}. The input should be low impedance, making a bypass capacitor a preferred solution. A 10-Ω series resistor may be used to limit inrush current into the bypass capacitor, and to provide noise filtering for the supply.

BYP is the interconnection point between a charge pump, $V_{(AC)}$ monitor amplifiers and comparators, and the gate driver. $C_{(BYP)}$ must be used to filter the charge pump. A 2200 pF is recommended, but the value is not critical.

Typical Application Examples (continued)

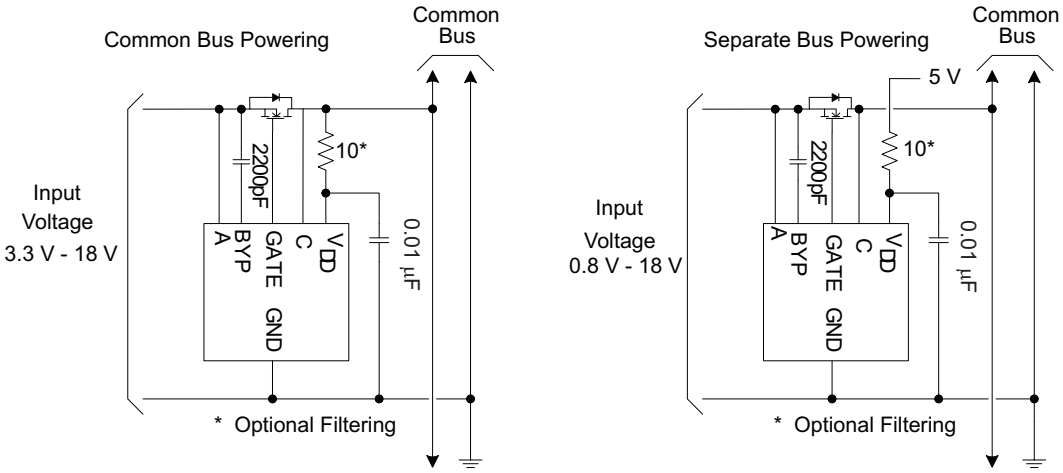


Figure 12. V_{DD} Powering Examples

10.2.2 Bidirectional Blocking and Protection of C

The TPS2410 and TPS2411 may be used in applications where bidirectional blocking is desired. This may occur in situations where two different voltages are ORed together, and operation from the lower voltage is desired. Another important application allows isolation of a redundant unit that is generating too high an output voltage. There are two considerations, first is the selection of the V_{DD} source, and second is protection of the C pin from excessive current. Figure 13 provides an example of this type of application.

V_{DD} needs to have voltage applied when A is to be connected to the load. Connecting V_{DD} to C only works when voltage on C is always present before A is connected. V_{DD} may be connected to A, a separate supply, or have voltage from A ORed with voltage from C. OV may be used to force GATE low, even when $V_{(A)}$ is greater than $V_{(C)}$, by driving OV to a voltage between 0.6 V and less than 5.25 V.

The C pin must be protected from excessive current if $V_{(A)}$ can exceed $V_{(C)}$ by more than 5.5 V. With a single MOSFET, $V_{(C)}$ is never more than a diode drop lower than $V_{(A)}$. When $V_{(AC)}$ is greater than a diode drop, a small current flows out of the C pin into the load. If $V_{(AC)}$ exceeds 5.5 V, a current limiting circuit should be used to protect C. Figure 13 provides an example circuit. Inserting this protection circuit creates a small offset in the forward regulation and threshold voltage.

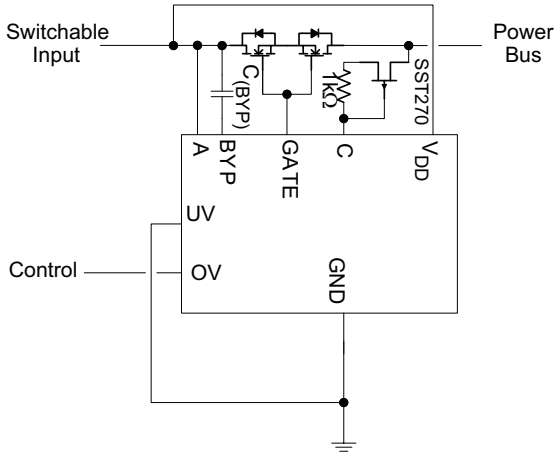


Figure 13. Bidirectional Blocking Example

Typical Application Examples (continued)

10.2.3 ORing Examples

Applications with the TPS2410 and TPS2411 are not limited to ORIng of identical sections. The device and external MOSFET form a general purpose function block. Figure 14 shows a circuit with ORing between a discrete diode and a TPS2410 MOSFET section. This circuit can be used to combine two different voltages in cases where the output is re-regulated, and the additional voltage drop in the Input 1 path is not a concern. An example is ORing of an ac adapter on Input 1 with a lower voltage on Input 2 Figure 15 shows an improved efficiency version of the first in which a P MOSFET replaces the simple diode. This circuit may not be useful in applications where Input 1 may be shorted because the P MOSFET is not managed, permitting reverse current flow. Input 2 should be the lower of the two voltage rails. If Input 1 was the lower voltage rail and connected first, then Input 2 is connected, there is a momentary reverse current in the P MOSFET. The reverse current occurs because the STAT signal does not go high until V_{GATE} ramps above Input 2 (the higher voltage) by 0.4 V. The Input 1 to Input 2 difference voltage momentarily appears across the PMOS device which is turned on until STAT switches high, causing a reverse current. The highest efficiency with the best fault tolerance is provided by two TPS2410 MOSFET sections.

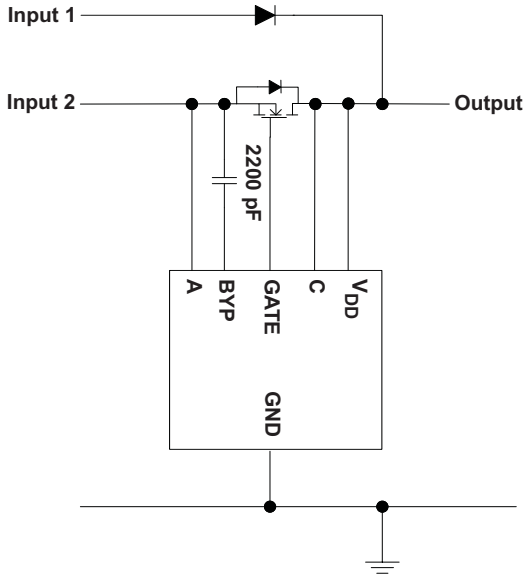


Figure 14. ORing Circuit

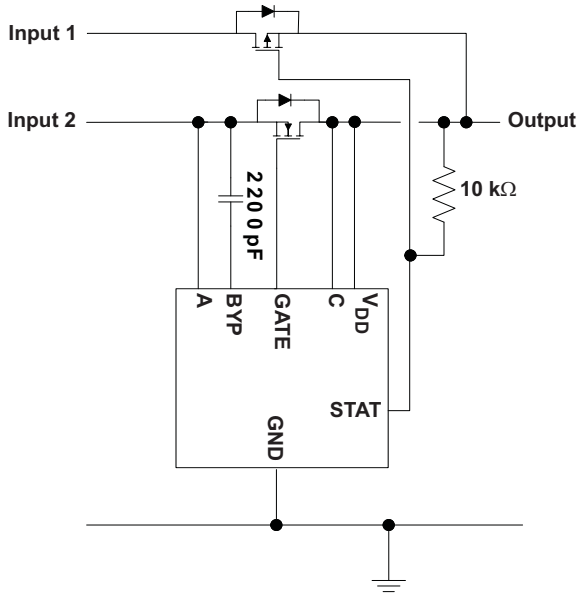


Figure 15. P MOSFET Circuit

The TPS2410 may be a better choice in applications where inputs may be removed, causing an open-circuit input. If the MOSFET was ON when the input is removed, V_{AC} is virtually zero. If the reverse turn-off threshold is programmed negative, the device does not pull GATE low. A system interruption can then be created if a short is applied to the floating input. For example, if an ac adapter is first connected to the unit, and then connected to the ac mains, the adapter output capacitors look like a momentary short to the unit. A TPS2410 with RSET open turns the MOSFET OFF when the input goes open circuit.

10.2.4 Design Requirements

10.2.4.1 MOSFET Selection and $R_{(RSET)}$

MOSFET selection criteria include voltage rating, voltage drop, power dissipation, size, and cost. The voltage rating consists of both the ability to withstand the rail voltage with expected transients, and the gate breakdown voltage. The MOSFET gate rating should be the minimum of 12 V or the controlled rail voltage. Typically this requires a ±20 V GATE voltage rating.

While $r_{DS(on)}$ is often chosen with the power dissipation, voltage drop, size and cost in mind, there are several other factors to be concerned with in ORing applications. When using the TPS2410, the minimum voltage across the device is 10 mV. A device that would have a lower voltage drop at full-load would be over-specified. When using a TPS2411 or TPS2410 with RSET programmed to a negative voltage, the permitted static reverse current is equal to the turn-off threshold divided by the $r_{DS(on)}$. While this current may actually be desirable in some systems, the amount may be controlled by selection of $r_{DS(on)}$ and RSET. The practical range of $r_{DS(on)}$ runs from the low milliohms to 40 mΩ for a single MOSFET.

MOSFETs may be paralleled for lower voltage drop (power loss) at high current. For TPS2410 operation, one should plan for only one of the MOSFETs to carry current until the 10 mV regulation point is exceeded and the loop forces GATE fully ON. TPS2411 operation does not rely on linear range operation, so the MOSFETs are all ON or OFF together except for short transitional times. Beyond the control issues, current sharing depends on the resistance match including both the $r_{DS(on)}$ and the connection resistance.

The TPS2410 may be used without a resistor on RSET If the turnoff $V_{(AC)}$ threshold is about 3 mV. The TPS2411 may only be operated without an RSET programming resistor if the loading provides a higher $V_{(AC)}$. A larger negative turnoff threshold reduces sensitivity to false tripping due to noise on the bus, but permits larger static reverse current. Installing a resistor from RSET to ground creates a negative shift in the fast turn-off threshold per Equation 3.

$$R_{(RSET)} = \left(\frac{-470.02}{V_{(OFF)} - 0.00314} \right) \tag{3}$$

To obtain a –10 mV fast turnoff ($V_{(A)}$ is less than $V_{(C)}$ by 10 mV), $R_{(RSET)}$ = (–470.02/ (–0.01–0.00314)) ≈ 35,700Ω. If a 10 mΩ $r_{DS(on)}$ MOSFET was used, the reverse turnoff current is calculated as follows.

$$I_{(TURN\_OFF)} = \frac{V_{(THRESHOLD)}}{r_{DS(on)}}$$

$$I_{(TURN\_OFF)} = \frac{-10\ mV}{10\ m\Omega}$$

$$I_{(TURN\_OFF)} = -1\ A \tag{4}$$

The sign indicates that the current is reverse, or flows from the MOSFET drain to source (C to A).

The turn-off speed of a MOSFET is influenced by the effective gate-source and gate-drain capacitance (C_{ISS}). Since these capacitances vary a great deal between different vendor parts and technologies, they should be considered when selecting a MOSFET where the fastest turn-off is desired.

10.2.4.2 TPS2410 Regulation-loop Stability

The TPS2410 uses an internal linear error amplifier to keep the external MOSFET from saturating at light load. This feature has the benefits of setting a turn-off above 0 V, providing a soft turn-off for slowly decaying input voltages, and helps droop-sharing redundancy at light load.

Although the control loop has been designed to accommodate a wide range of applications, there are a few guidelines to be followed to assure stability.

- Select a MOSFET $C_{(ISS)}$ of 1 nF or greater
- Use low ESR bulk capacitors on the output C terminal, typically greater than 100 μF with less than 50 mΩ ESR
- Maintain some minimum operational load (e.g. 100 mA or more)

Symptoms of stability issues include $V_{(AC)}$ undershoot and possible fast turn-off on large-transient recovery, and a worst-case situation where the gate continually cycles on and off. These conditions are solved by following the rules above. Loop stability should not be confused with tripping the fast comparator due to $V_{(AC)}$ tripping the gate off.

Although not common, a condition may arise where the dc/dc converter transient response may cause the GATE to cycle on and off at light load. The converter experiences a load spike when GATE transitions from OFF to ON because the ORed bus capacitor voltage charges abruptly by as much as a diode drop. The load spike may cause the supply output to droop and overshoot, which can result in the ORed capacitor peak charging to the overshoot voltage. When the supply output settles to its regulated value, the ORed bus may be higher than the source, causing the device to turn the GATE off. While this may not actually cause a problem, its occurrence may be mitigated by control of the power supply transient characteristic and increasing its output capacitance while increasing the ORed load to capacitance ratio. Adjusting the TPS2410 turn-off threshold or using STAT if possible to desensitize the redundant ORing device may help as well. Careful attention to layout and charge-pump noise around the device helps with noise margin.

The linear gate driver has a pull-up current of 290 μA and pull-down current of 3 mA typical.

10.2.5 Detailed Design Procedure

The following is a summarized design procedure:

1. Choose between the TPS2410 or TPS2411, see TPS2410 vs TPS2411 – MOSFET Control Methods.
2. Choose the V_{DD} source. Table 2 provides a guide for where to connect V_{DD} that covers most cases. V_{DD} may be directly connected to the supply, but an $R_{(VDD)}$ / $C_{(VDD)}$ of 10 Ω / 0.01 μF is recommended.

Table 2. V_{DD} Connection Guide

V_A < 3 V	3 V ≤ V_A ≤ 3.5 V	V_A > 3.5 V
Bias Supply > 3 V	V_A or Bias Supply > 3 V. V_C if always > 3 V	V_C, V_A or Bias for special configurations

3. Noise voltage and impedance at the A pin should be kept low. $C_{(A)}$ may be required if there is noise on the bus, or A is not low impedance. If either of these is a concern, a $C_{(A)}$ of 0.01 μF or more may be required.
4. Select $C_{(BYP)}$ as 2200 pF, X7R, 25-V or 50-V ceramic capacitor.
5. If the noise and transient environment is not well known, design $C_{(FLTR)}$ in, then experimentally determine if it is required. Start with a 100 pF, X7R, 25-V or 50-V ceramic capacitor and adjust if necessary.
6. Select M1 based on considerations of voltage drop, power dissipated, voltage ratings, and gate capacitance. See sections: MOSFET Selection and RSET and TPS2410 Regulation-Loop Stability.
7. Select $R_{(RSET)}$ based on which MOSFET was chosen and reverse current considerations – see MOSFET Selection and RSET. If the noise and transient environment is not well known, make provision for $R_{(RSET)}$ even when using the TPS2410.
8. Configure the UV and OV inputs per the desired behavior – UV, OV, and PG. Calculate the resistor dividers.
9. Add optional interface for PG, FLTB, and STAT as desired.
10. Make sure to connect RSVD to ground.

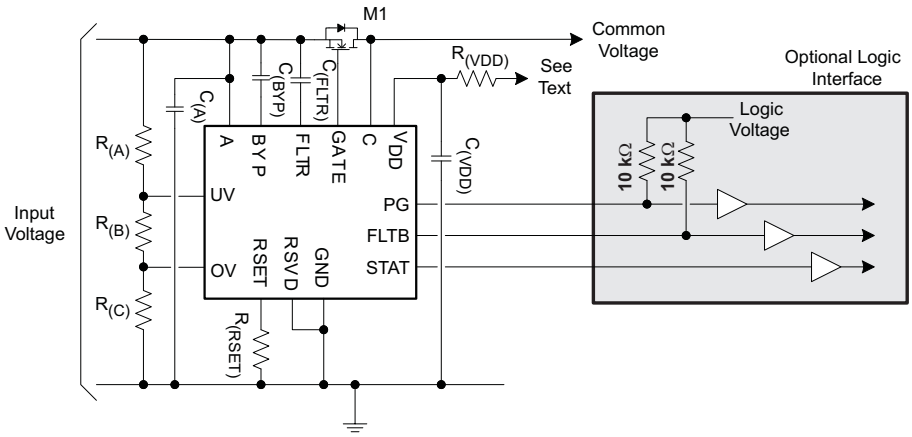
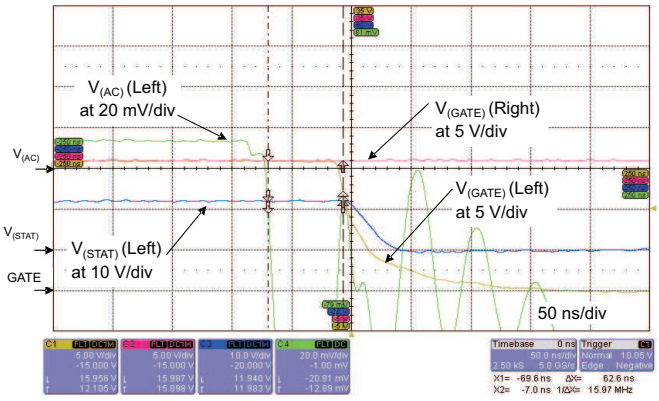


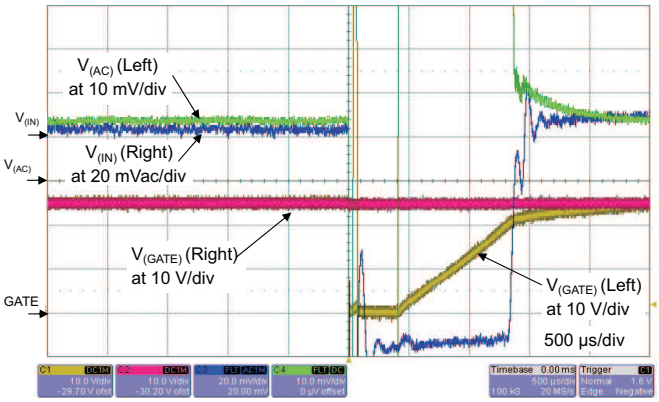
Figure 16. Design Template

10.2.6 Application Curves



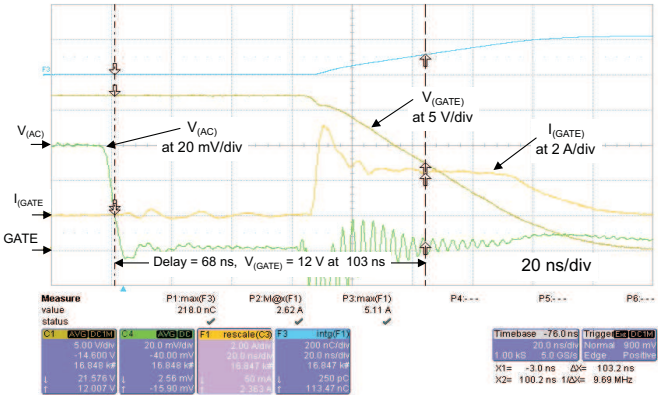
V_{DD} = 12 $I_{(LOAD)}$ = 5 A

Figure 17. Typical Turnoff with Two Ored Devices Active vs IRL3713 Transient Applied to Left Side



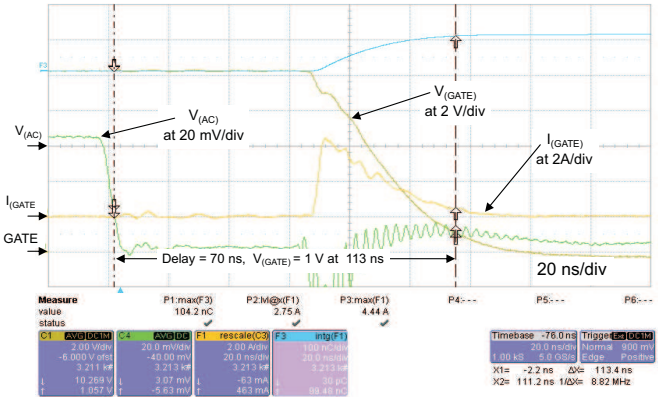
V_{DD} = 3 V V_A = 18 V $I_{(LOAD)}$ = 5 A

Figure 18. Typical Turnoff and Recovery with Two Ored Devices Active vs IRL3713 Transient Applied to Left Side



$C_{(GATE)}$ = 10 nF $V_{(AC)}$ = -20 mV
V_{DD} = V_A = 12 V

Figure 19. Turnoff Time



$C_{(GATE)}$ = 10 nF $V_{(AC)}$ = -20 mV V_{DD} = 5
V_A = 1 V

Figure 20. Turnoff Time

11 Power Supply Recommendations

11.1 Recommended Operating Range

The maximum recommended bus voltage is lower than the absolute maximum voltage ratings on A, C, and V_{DD} solely to provide margin for transients on the bus. Most power systems experience transient voltages above the normal operating level. Short transients, or voltage spikes, may be clamped by the ORing MOSFET to an output capacitor and/or voltage rail depending on the system design. Transient protection, that is, a TVS diode (transient voltage suppressor, a type of Zener diode), may be required on the input or output if the system design does not inherently limit transient voltages below the device absolute maximum ratings. If a TVS is required, it must protect to the absolute maximum ratings at the worst case clamping current. The devices operate properly up to the absolute maximum voltage ratings on A, C, and V_{DD}.

11.2 System Design and Behavior with Transients

The power system, perhaps consisting of multiple supplies, interconnections, and loads, is unique for every product. A power distribution has low impedance, and low loss, which yields high Q by its nature. While the addition of lossy capacitors helps at low frequencies, their benefit at high frequencies is compromised by parasitics. Transient events with rise times in the 10-ns range may be caused by inserting or removing units, load fluctuations, switched loads, supply fluctuations, power supply ripple, and shorts. These transients cause the distribution to ring, creating a situation where ORing controllers may trip off unnecessarily. In particular, when an ORing device turns off due to a reverse current fault, there is an abrupt interruption of the current, causing a fast ringing event. Since this ringing occurs at the same point in the topology as the other ORing controllers, they are the most likely to be effected.

The ability to operate in the presence of noise and transients is in direct conflict with the goal of precise ORing with rapid response to actual faults. A fast response reduces peak stress on devices, reduces transients, and promotes un-interrupted system operation. However, a control with small thresholds and high speed is most likely to be falsely tripped by transients that are not the result of a fault. The power distribution system should be designed to control the transient voltages seen by fast-responding devices such as ORing and hotswap devices.

The TPS2410 was designed with several features to help tune its speed and sensitivity to individual systems. The FLTR pin provides a convenient place to filter the bus voltage before it causes undesired tripping (see Fast Comparator Input Filtering – $C_{(FLTR)}$). Some applications may find it possible to use RSET to advantage by setting the reverse turn-off threshold more negative. Last, the STAT pin may be used to desensitize the turnoff threshold of an on-line TPS2410 when a redundant TPS2410 has turned off. This is especially attractive in dual redundant systems (see Input ORing and STAT). Ultimately, the performance may have to be tuned to fit the characteristics of each particular system.

12 Layout

12.1 Layout Considerations

See Figure 16 for reference designations.

1. The TPS2410 and TPS2411, M1, and associated components should be used over a ground plane.
2. The GND connection should be short with multiple vias to ground.
3. $C_{(VDD)}$ should be adjacent to the V_{DD} pin with a minimal ground connection length to the plane.
4. The GATE connection should be short and wide (this is, 0.025" minimum).
5. The C pin should be Kelvin connected to M1.
6. The A pin should be a short, wide, Kelvin connection to M1 and the bus.
7. $C_{(BYP)}$, $C_{(FLTR)}$, and $R_{(RSET)}$ should be kept immediately adjacent to the TPS2410 and TPS2411 with short leads.
8. Do not run noisy signals adjacent to FLTR.

12.2 Layout Example

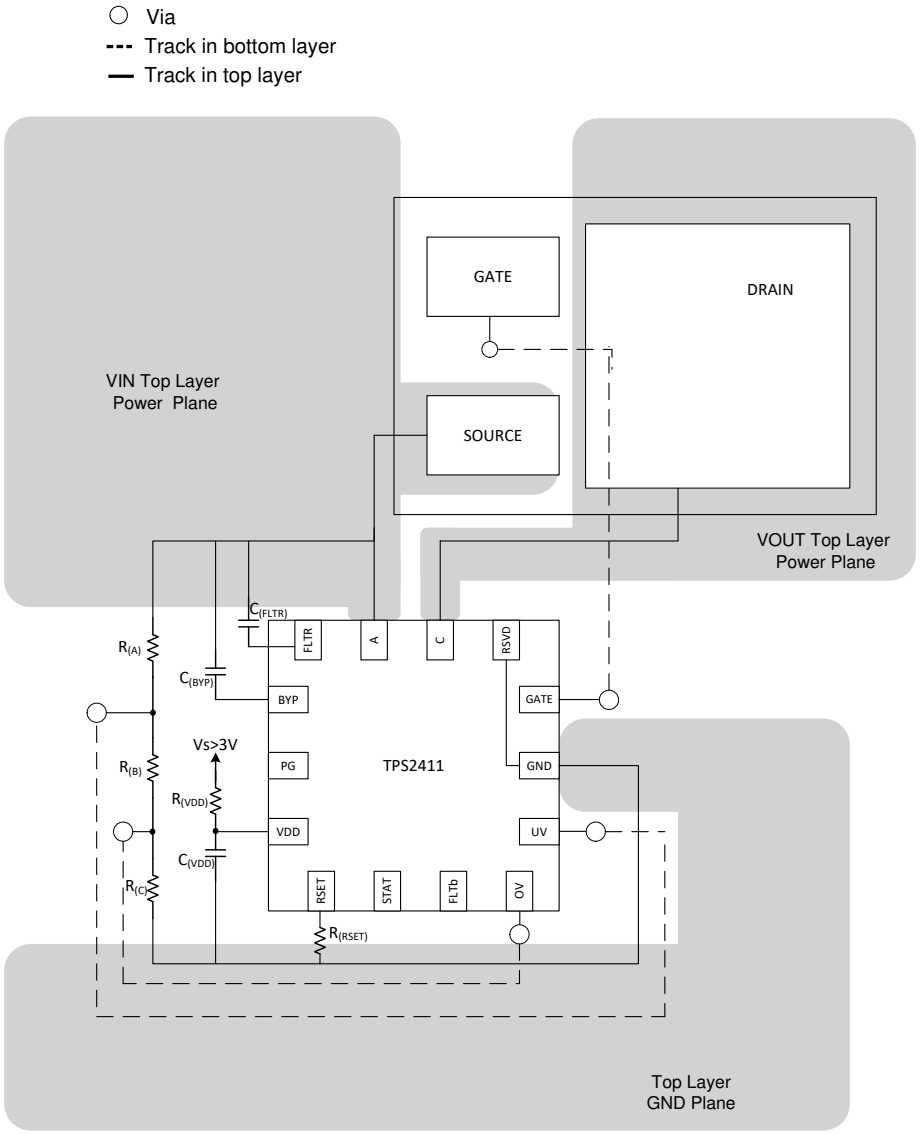


Figure 21. Example Layout

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS2410	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS2411	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

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13.4 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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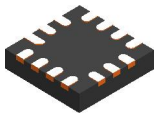
13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

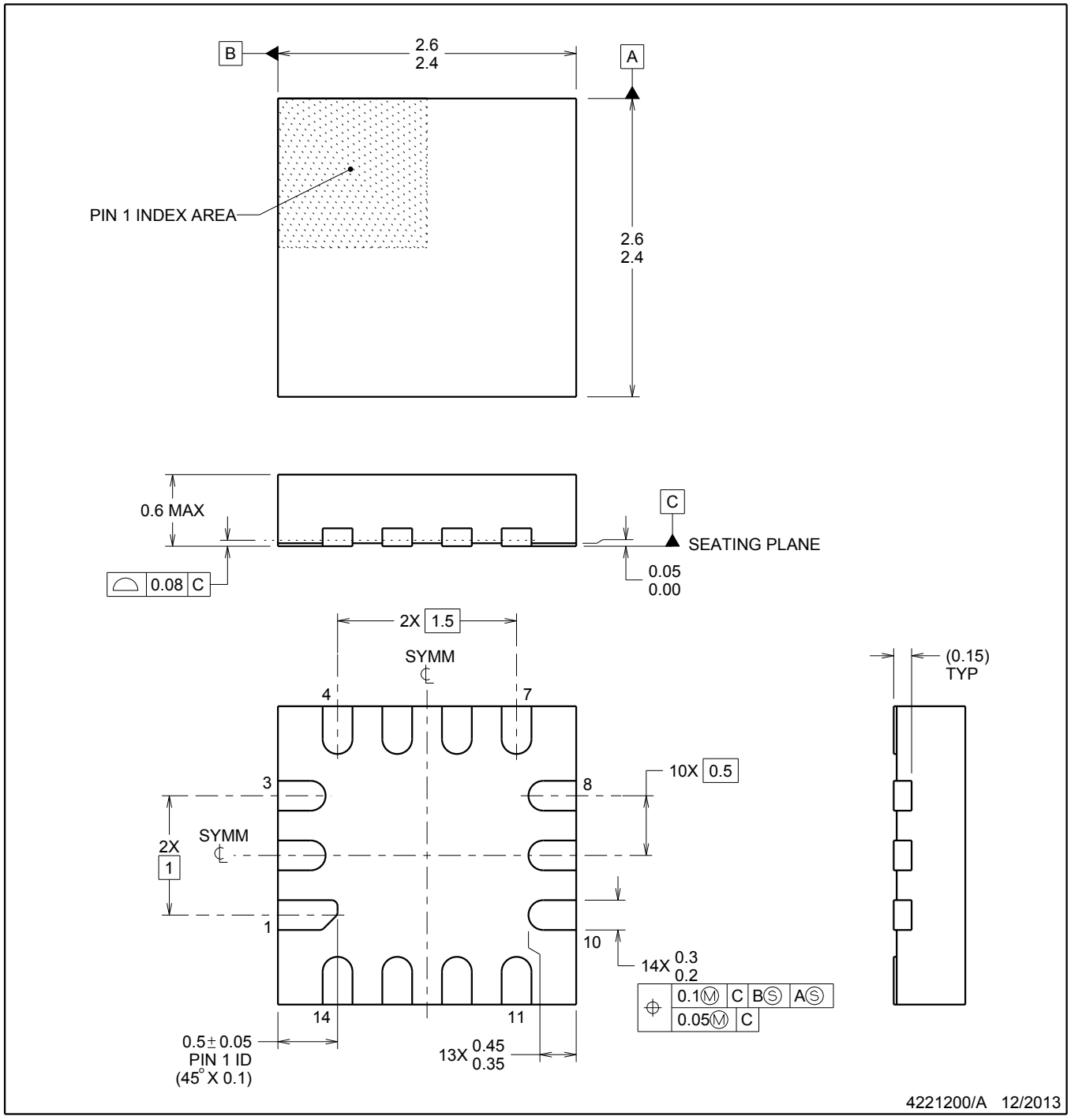
以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。



RMS0014A

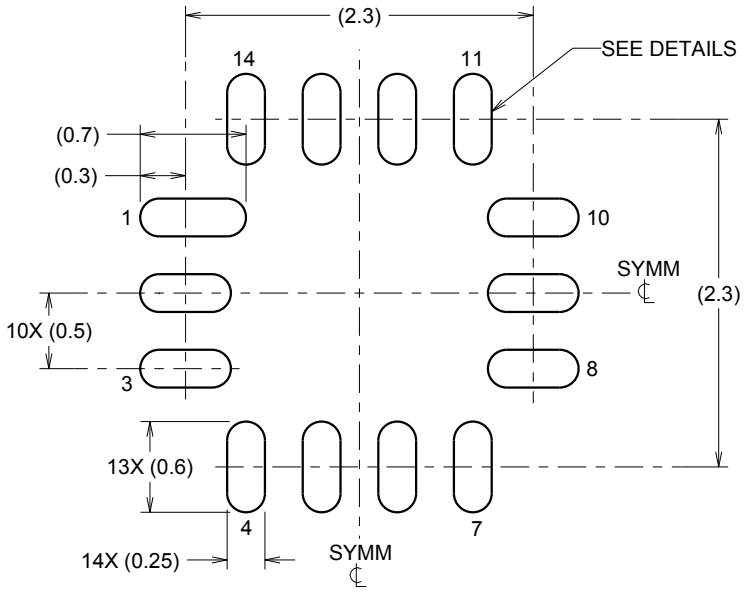
UQFN - 0.6 mm max height

UQFN

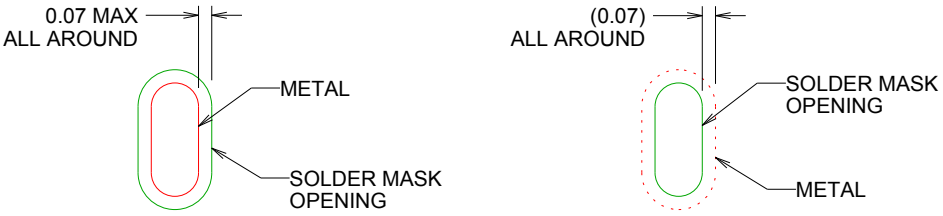


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

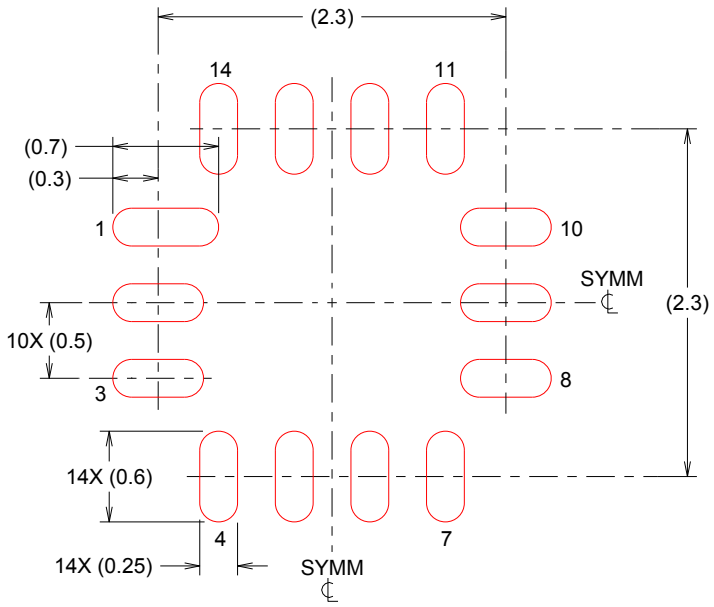
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221200/A 12/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

4221200/A 12/2013

NOTES: (continued)

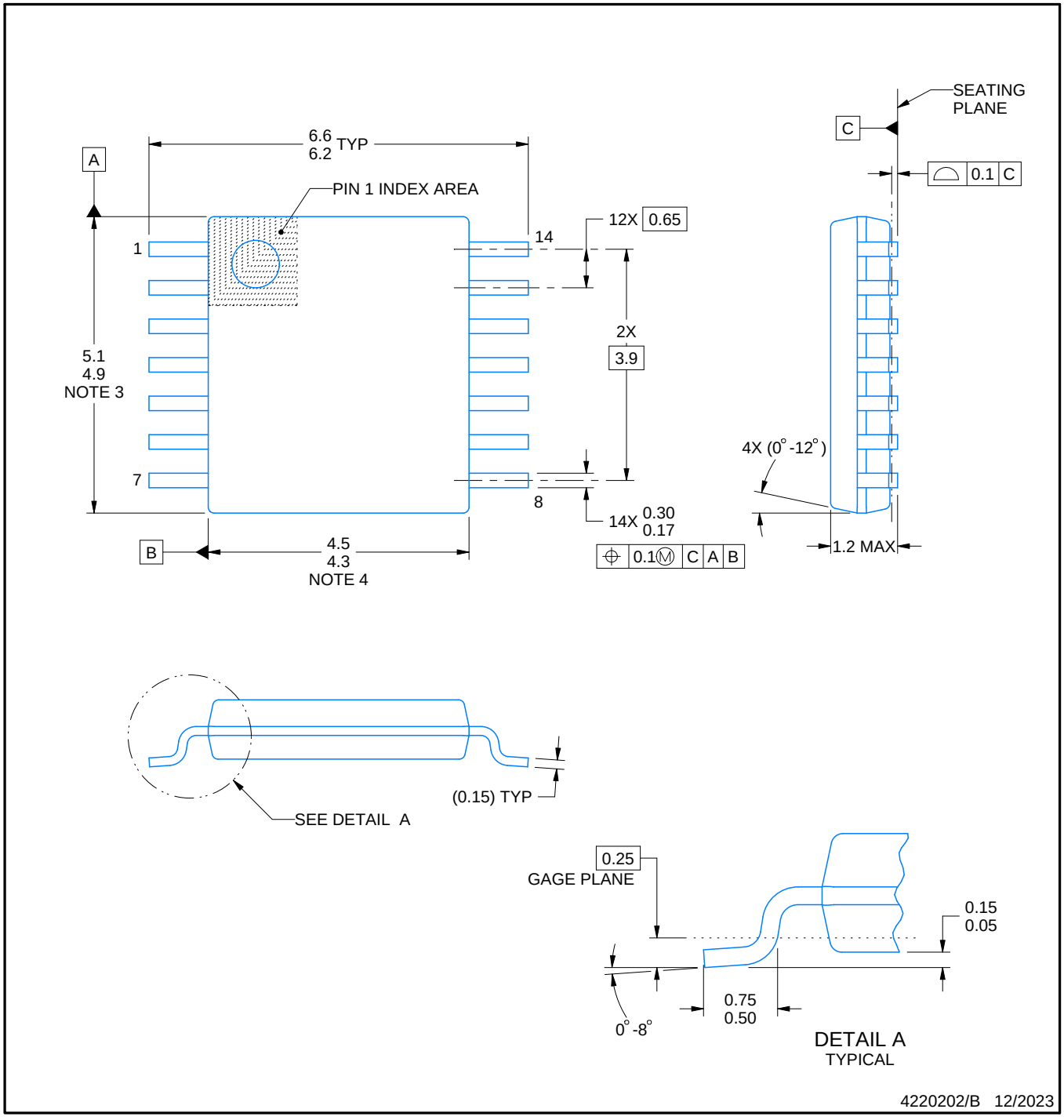
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

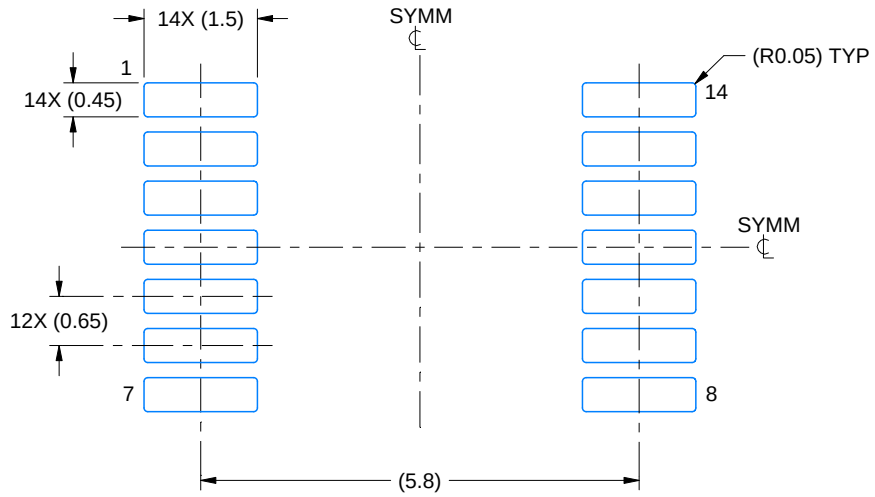
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

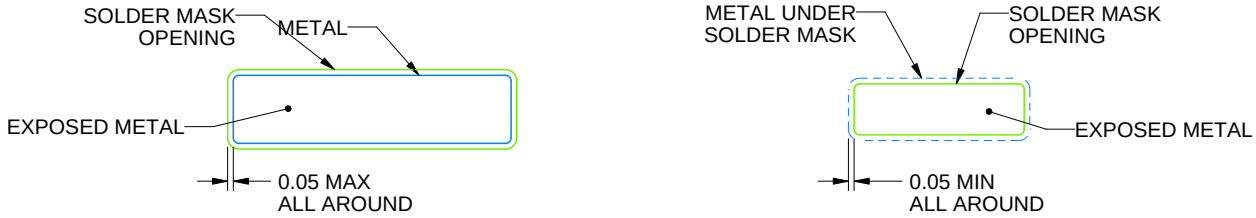


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

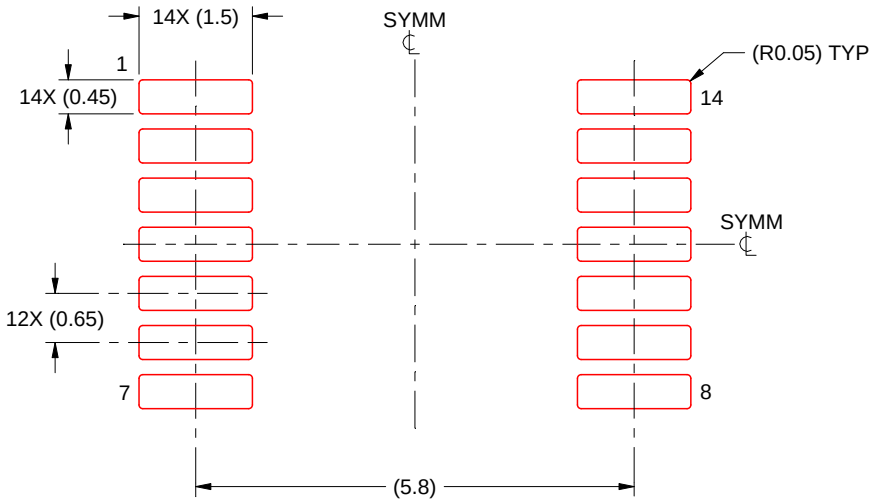


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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