TPS2549-Q1 ケーブル補償機能搭載、車載 USB 充電ポート･コントローラ / パワー･スイッチ

1 特長

- 下記内容で AEC-Q100 認定済み:
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C5
- 動作電圧範囲: 4.5V ~ 6.5V
- 47mΩ (標準値) のハイサイド MOSFET
- 最大連続出力電流: 3.2A
- ケーブル補償用の±5% CS 出力
- USB バッテリ充電仕様 1.2 準拠の CDP モード
- DCP モードの自動選択:
  - BC1.2 および YD/T 1591-2009 準拠の短絡モード
  - 2.7V デバイダ 3 モード
  - 1.2V モード
- システム更新用の D+および D-クライアント･ モード
- D+および D-の V_{BUS} への短絡保護
- D+および D-の±8kV 接触放電および±15kV 空中放電 ESD 定格(IEC 61000-4-2)
- 接合部温度範囲: -40°C ~ 125°C
- 3mm×3mm の 16 ピン QFN パッケージ

2 アプリケーション

- 車載用 USB ポート (ホストおよびハブ)
- 車載用インフォテイメント･ システム

3 概要

TPS2549-Q1 デバイスは、上流の電源を制御できる電流センス出力を備えた USB 充電ポート･ コントローラおよびパワー･ スイッチです。これによって、充電電流が大きい場合でも、USB ポートで 5V を維持できます。この機能は、USB ケーブルが長く、高速な充電を行う携帯機器によって大きな電圧低下が発生するようなシステムで重要です。

TP2549-Q1 47mΩ パワー･ スイッチは、隣接ポートの負荷が重くなった際に電流制限値を下げることでポート･ パワー･ マネージメントに対応する選択可能な 2 つのプログラマブル電流制限機能を備えています。これは、複数のポートがあり、上流の電源がすべてのポートに最大電流を同時に供給できないシステムに重要です。

DCP_Auto スキーマは、接続されているデバイスと通信するための正しい D+および D-設定を検出して選択するため、最大電流で高速な充電が可能です。内蔵の CDP 検出機能により、ほとんどの携帯機器を最大 1.5A で高速に充電でき、同時にデータ通信も行えます。

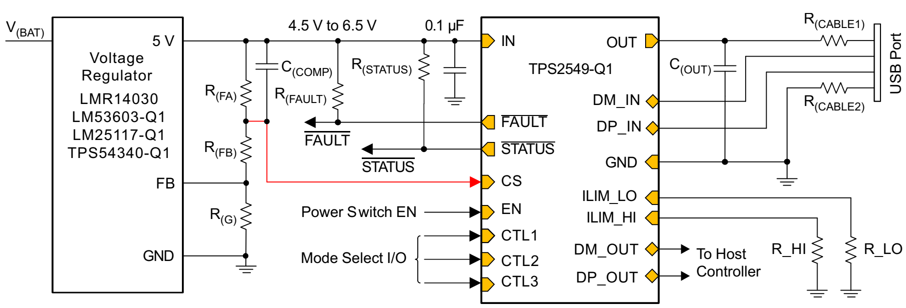
独自のクライアント･ モード機能により、データ･ ライン接続を維持したまま内部のパワー･ スイッチをオフにして電力の競合を回避しながら、クライアント機器のソフトウェア更新を可能にします。

さらに、TPS2549-Q1 デバイスには D+ および D– について V_{BUS} への短絡保護が内蔵されており、D+ や D– が予期せず V_{BUS} へ短絡したときの損傷を防止します。アプリケーションの実装面積を節約するため、TPS2549-Q1 デバイスは ESD 保護も内蔵し、D+ および D– への外付け回路なしで IEC61000-4-2 に合格できます。

製品情報 (1) (1 ページ)

型番	パッケージ	本体サイズ (公称)
TPS2549-Q1	WQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (July 2016) to Revision C (August 2020) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Added Note (2) to Absolute Maximum Ratings table ... 4
- Added Footnote to Recommended Operating Conditions table ... 4
- Added paragraph to Typical Application section for clarification ... 29

Changes from Revision A (October 2015) to Revision B (July 2016) — **Page**

- 最大出力電流を 3.2A に変更 ... 1
- Changed maximum output current in *Recommended Operating Conditions* ... 4
- Changed minimum current-set resistance in *Recommended Operating Conditions* ... 4
- Added a row to the CURRENT LIMIT section in *Electrical Characteristics* ... 5
- Added a row to the CABLE COMPENSATION section of *Electircal Characteristics* ... 5
- Added *Receiving Notification of Documentation Updates* section ... 36

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- デバイスのステータスを先行量産から量産に変更 ... 1

5 Pin Configuration and Functions

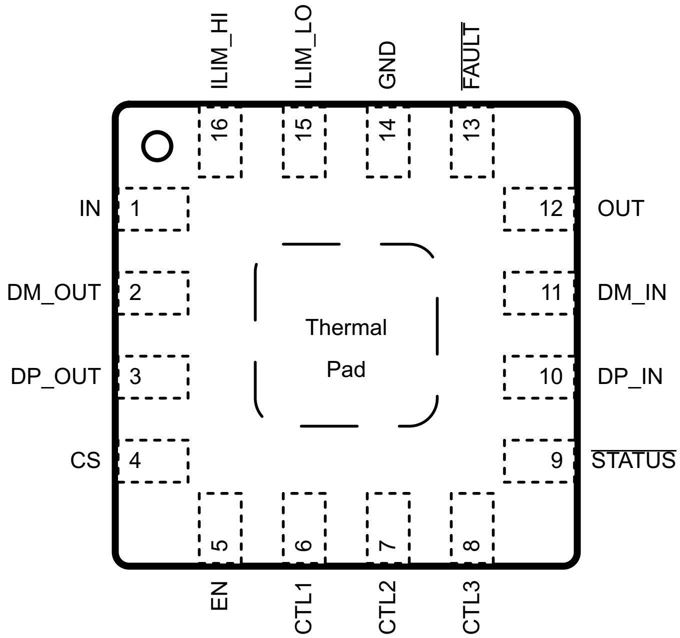

図 5-1. RTE Package 16-Pin WQFN Top View

Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
CS	4	O	Provide sink current proportional to output current. For cable compensation, connect to the feedback divider of the up-stream voltage regulator.
CTL1	6	I	Logic-level control inputs for controlling the charging mode and the signal switches; (see 表 8-2). These pins tie directly to IN or GND without a pullup or pulldown resistor.
CTL2	7	I	
CTL3	8	I	
DM_IN	11	I/O	D– data line to downstream connector
DM_OUT	2	I/O	D– data line to upstream USB host controller
DP_IN	10	I/O	D+ data line to downstream connector
DP_OUT	3	I/O	D+ data line to upstream USB host controller
EN	5	I	Logic-level control input for turning the power switch and the signal switches on/off. When EN is low, the device is disabled, the signal and power switches are OFF.
FAULT	13	O	Active-low open-drain output, asserted during overtemperature, overcurrent, and DP_IN and DM_IN overvoltage conditions. See 表 8-1.
GND	14	—	Ground connection; should be connected externally to the thermal pad.
ILIM_HI	16	I	Connect external resistor to ground to set the high current-limit threshold.
ILIM_LO	15	I	Connect external resistor to ground to set the low current-limit threshold and the load-detection current threshold.
IN	1	PWR	Input supply voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
OUT	12	PWR	Power-switch output
STATUS	9	O	Active-low open-drain output, asserted when the load exceeds the load-detection threshold
Thermal pad	—	—	Thermal pad on bottom of package. The thermal pad is internally connected to GND and is used to heat-sink the device to the circuit board. Connect the thermal pad to the GND plane.

(1) I = Input, O = Output, I/O = Input and output, PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

Voltages are with respect to GND unless otherwise noted[(1)]

			MIN	MAX	UNIT
	Voltage range	CS, CTL1, CTL2, CTL3, EN, FAULT, ILIM_HI, ILIM_LO, IN, OUT, STATUS	–0.3	7	V
		DM_IN, DM_OUT, DP_IN, DP_OUT	–0.3	5.7[(2)]	V
		IN to OUT	–7	7	V
	Continuous current in SDP, CDP or client mode	DP_IN to DP_OUT or DM_IN to DM_OUT	–100	100	mA
	Continuous current in BC1.2 DCP mode	DP_IN to DM_IN	–35	35	mA
	Continuous output current	OUT	Internally limited		A
$I_{(SRC)}$	Continuous output source current	ILIM_HI, ILIM_LO	Internally limited		A
$I_{(SNK)}$	Continuous output sink current	FAULT, STATUS		25	mA
		CS	Internally limited		A
T_J	Operating junction temperature		–40	Internally limited	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If there is any risk for VBUS, DM_IN, DP_IN pins see voltage stresses beyond those listed under Absolute Maximum Ratings, for example, shorting to Car battery, please check TPS25840-Q1 and TPS254900A-Q1 with higher absolute maximum ratings

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2,000[(2)]	V
		Charged-device model (CDM), per AEC Q100-011		±750[(3)]	
		IEC[(4)]	IEC61000-4-2 contact discharge, DP_IN and DM_IN	±8,000	
			IEC61000-4-2 air di scharge, DP_IN and DM_IN	±15,000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5
(4) Surges per IEC61000-4-2, 1999 applied between DP_IN/DM_IN and output ground of the TPS2549Q1EVM-729 (SLVUAK6) evaluation module.

6.3 Recommended Operating Conditions

Voltages are with respect to GND unless otherwise noted.

			MIN	NOM	MAX	UNIT
$V_{(IN)}$	Supply voltage	IN	4.5		6.5	V
	Input voltage	CTL1, CTL2, CTL3, EN	0		6.5	V
		DM_IN, DM_OUT, DP_IN, DP_OUT	0		3.6	V
$I_{(OUT)}$	Output continuous current	OUT (–40°C ≤ T_A ≤ 85°C)			3.2[(1)]	A
	Continuous current in SDP, CDP or client mode	DP_IN to DP_OUT or DM_IN to DM_OUT	–30		30	mA
	Continuous current in BC1.2 DCP mode	DP_IN to DM_IN	–15		15	mA
	Continuous output sink current	FAULT, STATUS			10	mA
$R_{(ILIM\_xx)}$	Current limit-set resistors		10.4		1000	kΩ
T_J	Operating junction temperature		–40		125	°C

(1) Operating at output continuous current greater than 3.2A is possible, however lifetime will be degraded.

6.4 Thermal Information

THERMAL METRIC[1]		TPS2549-Q1 RTE (WQFN) 16 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	44.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	53.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	17.6	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	1	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	17.6	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(CTL1)}$ = $V_{(CTL2)}$ = $V_{(CTL3)}$ = $V_{(IN)}$. $R_{(FAULT)}$ = $R_{(STATUS)}$ = 10 kΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT – POWER SWITCH						
$r_{DS(on)}$	On-resistance[1]	T_J = 25°C		47	57	mΩ
		–40°C ≤ T_J ≤ 85°C		47	72	
		–40°C ≤T_J ≤ 125°C		47	80	
$I_{lkg(OUT)}$	Reverse leakage current on OUT pin	V_{OUT} = 6.5 V, V_{IN} = V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C, measure $I_{(OUT)}$			2	µA
OUT - DISCHARGE						
$R_{(DCHG)}$	OUT discharge resistance		400	500	630	Ω
EN, CTL1, CTL2, CTL3 INPUTS						
	Input pin rising logic threshold voltage		1	1.35	2	V
	Input pin falling logic threshold voltage		0.85	1.15	1.65	V
	Hysteresis[2]			200		mV
	Input current	Pin voltage = 0 V or 6.5 V	–1		1	µA
CURRENT LIMIT						
I_{OS}	OUT short-circuit current limit	$R_{(ILIM\_LO)}$ = 210 kΩ	205	255	305	mA
		$R_{(ILIM\_LO)}$ = 80.6 kΩ	600	660	720	
		$R_{(ILIM\_LO)}$ = 23.2 kΩ	2145	2300	2455	
		$R_{(ILIM\_HI)}$ = 20 kΩ	2500	2670	2840	
		$R_{(ILIM\_HI)}$ = 19.1 kΩ	2620	2800	2975	
		$R_{(ILIM\_HI)}$ = 15.4 kΩ	3255	3470	3685	
		$R_{(ILIM\_HI)}$ = 14.7 kΩ	3411	3637	3862	
		$R_{(ILIM\_HI)}$ = 12.9 kΩ	3920	4175	4435	
		$R_{(ILIM\_HI)}$ = 10.4 kΩ	4830	5145	5460	
		$R_{(ILIM\_HI)}$ shorted to GND	5500	7000	8000	

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(IN\_OFF)}$	Disabled IN supply current	$V_{(EN)}$ = 0 V, $V_{(OUT)}$ = 0 V, –40°C ≤ T_J ≤ 85°C		0.1	5	µA
$I_{(IN\_ON)}$	Enabled IN supply current	$V_{(CTL)1} = V_{(CTL2)} = V_{(CTL3)} = V_{(IN)}$		220	300	µA
		$V_{(CTL1)} = V_{(CTL2)}$ = 0 V, $V_{(CTL3)} = V_{(IN)}$		226	300	
		$V_{(CTL2)} = V_{(IN)}$, $V_{(CTL1)} = V_{(CTL3)}$ = 0 V		150	220	
		$V_{(CTL1)} = V_{(IN)}$, $V_{(CTL2)} = V_{(CTL3)}$ = 0 V		115	190	
UNDERVOLTAGE LOCKOUT, IN						
$V_{(UVLO)}$	IN rising UVLO threshold voltage		3.9	4.1	4.3	V
	Hysteresis(3)	T_J = 25°C		100		mV
FAULT						
	Output low voltage	$I_{(FAULT)}$ = 1 mA			100	mV
	Off-state leakage	$V_{(FAULT)}$ = 6.5 V			2	µA
STATUS						
	Output low voltage	$I_{(STATUS)}$ = 1 mA			100	mV
	Off-state leakage	$V_{(STATUS)}$ = 6.5 V			2	µA
THERMAL SHUTDOWN						
$T_{(OTSD2)}$	Thermal shutdown threshold		155			°C
$T_{(OTSD1)}$	Thermal shutdown threshold in current-limit		135			°C
	Hysteresis(3)			20		°C
LOAD DETECT ($V_{CTL1} = V_{CTL2} = V_{CTL3} = V_{IN}$)						
$I_{(LD)}$	I_{OUT} load detection threshold	$R_{(ILIM\_LO)}$ = 80.6 kΩ, rising load current	630	700	770	mA
	Hysteresis(3)			50		mA
DP_IN AND DM_IN SHORT-TO-V_{BUS} PROTECTION						
$V_{(OV)}$	Overvoltage protection trip threshold	DP_IN and DM_IN rising	3.7	3.9	4.15	V
	Hysteresis(3)			100		mV
$R_{(DCHG\_Data)}$	Discharge resistance after OVP	$V_{(DP\_IN)} = V_{(DM\_IN)}$ = 5 V	160	210	240	kΩ
CABLE COMPENSATION						
$I_{(CS)}$	Sink current	Load = 3.2 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	228	240	252	µA
		Load = 3 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	214	225	236	
		Load = 2.4 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	171	180	189	
		Load = 2.1 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	149	158	166	
		Load = 1 A, 2.5 V ≤ $V_{(CS)}$ ≤ 6.5 V	70	75	80	

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)} = V_{(IN)}$, $V_{(CTL1)} = V_{(CTL2)} = V_{(CTL3)} = V_{(IN)}$. $R_{(FAULT)} = R_{(STATUS)}$ = 10 kΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
$R_{(HS\_ON)}$	DP and DM switch on-resistance	$V_{(DP\_OUT)} = V_{(DM\_OUT)}$ = 0 V, $I_{(DP\_IN)} = I_{(DM\_IN)}$ = 30 mA		2	4	Ω
		$V_{(DP\_OUT)} = V_{(DM\_OUT)}$ = 2.4 V, $I_{(DP\_IN)} = I_{(DM\_IN)}$ = –15 mA		2.9	6	
$\lvert\Delta R_{(HS\_ON)}\rvert$	Switch resistance mismatch between DP and DM channels	$V_{(DP\_OUT)} = V_{(DM\_OUT)}$ = 0 V, $I_{(DP\_IN)} = I_{(DM\_IN)}$ = 30 mA		0.05	0.15	Ω
		$V_{(DP\_OUT)} = V_{(DM\_OUT)}$ = 2.4 V, $I_{(DP\_IN)} = I_{(DM\_IN)}$ = –15 mA		0.05	0.15	
$C_{(IO\_OFF)}$	DP/DM switch off-state capacitance[4]	V_{EN} = 0 V, $V_{(DP\_IN)} = V_{(DM\_IN)}$ = 0.3 V, Vac = 0.03 V_{PP} , f = 1 MHz		6.7		pF
$C_{(IO\_ON)}$	DP/DM switch on-state capacitance[4]	$V_{(DP\_IN)} = V_{(DM\_IN)}$ = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		10		pF
	Off-state isolation[4]	V_{EN} = 0 V, f = 250 MHz		27		dB
	On-state cross-channel isolation[4]	f = 250 MHz		23		dB
$I_{lkg(OFF)}$	Off-state leakage current, DP_OUT and DM_OUT	V_{EN} = 0 V, $V_{(DP\_IN)} = V_{(DM\_IN)}$ = 3.6 V, $V_{(DP\_OUT)} = V_{(DM\_OUT)}$ = 0 V		0.1	1.5	µA
BW	Bandwidth (–3 dB)[4]	$R_{(L)}$ = 50 Ω		925		MHz
CHARGING DOWNSTREAM PORT DETECT						
$V_{(DM\_SRC)}$	DM_IN CDP output voltage	$V_{(DP\_IN)}$ = 0.6 V, –250 µA < $I_{(DM\_IN)}$ < 0 µA	0.5	0.6	0.7	V
$V_{(DAT\_REF)}$	DP_IN rising lower window threshold for V_{DM_SRC} activation		0.36		0.4	V
	Hysteresis[4]			50		mV
$V_{(LGC\_SRC)}$	DP_IN rising upper window threshold for VDM_SRC de-activation		0.8		0.88	V
$V_{(LGC\_SRC\_HYS)}$	Hysteresis[4]			100		mV
$I_{(DP\_SINK)}$	DP_IN sink current	$V_{(DP\_IN)}$ = 0.6 V	40	75	100	µA
BC1.2 DCP MODE						
$R_{(DPM\_SHORT)}$	DP_IN and DM_IN shorting resistance			125	200	Ω
DIVIDER3 MODE						
$V_{(DP\_DIV3)}$	DP_IN output voltage		2.57	2.7	2.84	V
$V_{(DM\_DIV3)}$	DM_IN output voltage		2.57	2.7	2.84	V
$R_{(DP\_DIV3)}$	DP_IN output impedance	$I_{(DP\_IN)}$ = –5 µA	24	30	36	kΩ
$R_{(DM\_DIV3)}$	DM_IN output impedance	$I_{(DM\_IN)}$ = –5 µA	24	30	36	kΩ
1.2-V MODE						
$V_{(DP\_1.2V)}$	DP_IN output voltage		1.12	1.2	1.26	V
$V_{(DM\_1.2V)}$	DM_IN output voltage		1.12	1.2	1.26	V
$R_{(DP\_1.2V)}$	DP_IN output impedance	$I_{(DP\_IN)}$ = –5 µA	84	100	126	kΩ
$R_{(DM\_1.2V)}$	DM_IN output impedance	$I_{(DM\_IN}$ = –5 µA	84	100	126	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(3) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

(4) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

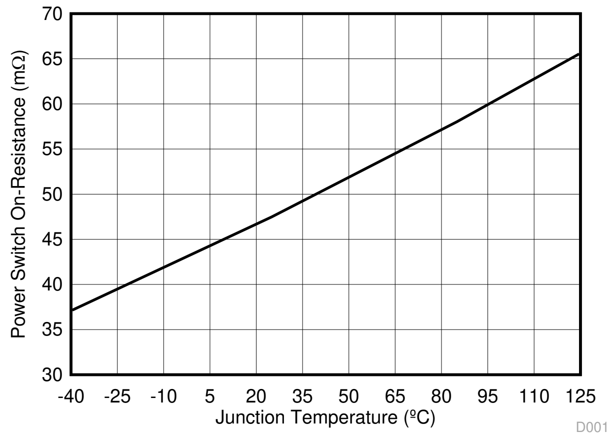
6.6 Switching Characteristics

Unless otherwise noted –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 6.5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(CTL1)}$ = $V_{(CTL2)}$ = $V_{(CTL3)}$ = $V_{(IN)}$. $R_{(FAULT)}$ = $R_{(STATUS)}$ = 10 kΩ, $R_{(ILIM\_HI)}$ = 19.1 kΩ, $R_{(ILIM\_LO)}$ = 80.6 kΩ. Positive current is into pins. Typical value is at 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	OUT voltage rise time	$V_{(IN)}$ = 5 V, $C_{(L)}$ = 1 µF, $R_{(L)}$ = 100 Ω (see 図 7-1 and 図 7-2)	0.7	1.14	2	ms
t_f	OUT voltage fall time		0.2	0.35	0.6	ms
t_{on}	OUT voltage turnon time	$V_{(IN)}$ = 5 V, $C_{(L)}$ = 1 µF, $R_{(L)}$ = 100 Ω (see 図 7-1 and 図 7-4)		4.15	6	ms
t_{off}	OUT voltage turnoff time			1.8	3	ms
$t_{(DCHG\_L)}$	Long OUT discharge hold time (SDP, CDP, or client mode to DCP_Auto)	Time $V_{(OUT)}$ < 0.7 V (see 図 7-3)	1.1	2	2.9	s
$t_{(DCHG\_S)}$	Short OUT discharge hold time (DCP_Auto to SDP, CDP, or client mode)	Time $V_{(OUT)}$ < 0.7 V (see 図 7-3)	186	320	450	ms
$t_{(IOS)}$	OUT short-circuit response time(1)	$V_{(IN)}$ = 5 V, $R_{(SHORT)}$ = 50 mΩ (see 図 6-25)		2		µs
$t_{(OC\_OUT\_FAULT)}$	OUT $\overline{\text{FAULT}}$ deglitch time	Bidirectional deglitch applicable to current limit condition only (no deglitch assertion for OTSD)	5.5	8	11.5	ms
t_{pd}	Analog switch propagation delay (1)	$V_{(IN)}$ = 5 V		0.14		ns
$t_{(SK)}$	Analog switch skew between opposite transitions of the same port (t_{PHL} – t_{PLH}) (1)	$V_{(IN)}$ = 5 V		0.02		ns
$t_{(LD\_SET)}$	Load-detect set time	$V_{(IN)}$ = 5 V (See 図 6-27)	120	210	280	ms
$t_{(LD\_RESET)}$	Load-detect reset time	$V_{(IN)}$ = 5 V (See 図 6-28)	1.8	3	4.2	s
$t_{(OV\_D)}$	DP_IN and DM_IN over-voltage protection response time	$V_{(OUT)}$ = 5 V (See 図 6-29)		2		µs
$t_{(OV\_D\_FAULT)}$	DP_IN and DM_IN $\overline{\text{FAULT}}$ degltich time	$V_{(OUT)}$ = 5 V (See 図 6-30)	11	16	23	ms

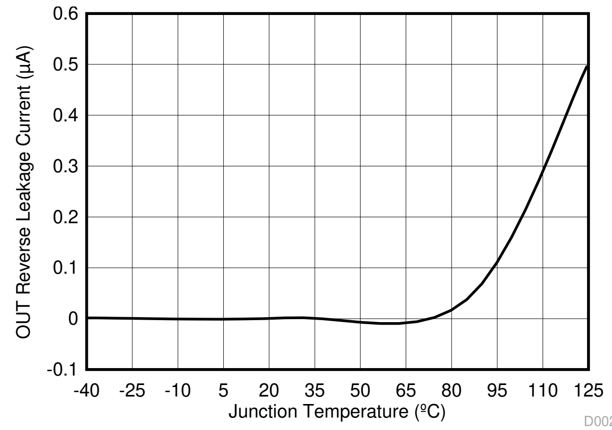
(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.7 Typical Characteristics



V_{IN} = 5 V

図 6-1. Power Switch On-Resistance vs Temperature



V_{IN} = 5 V

図 6-2. Reverse Leakage Current vs Temperature

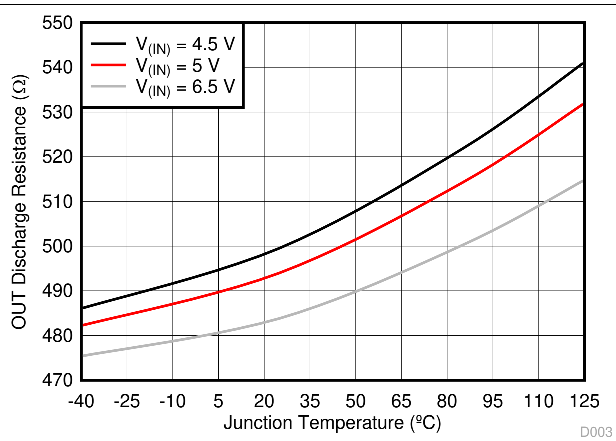
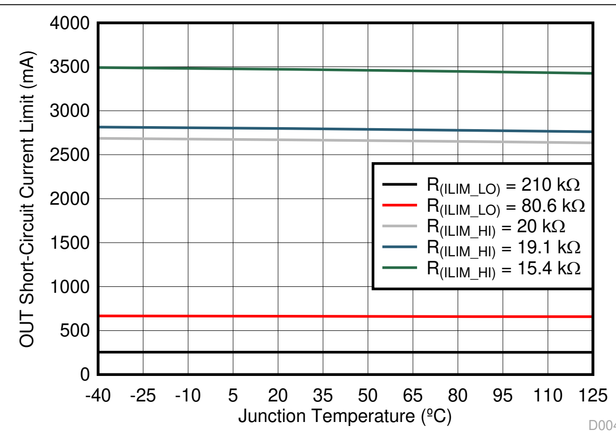
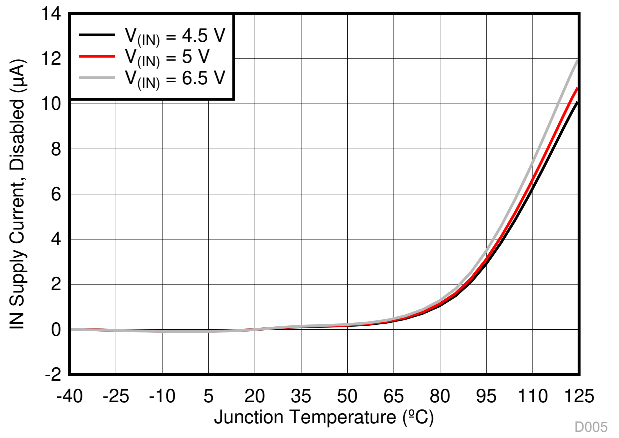


図 6-3. OUT Discharge Resistance vs Temperature



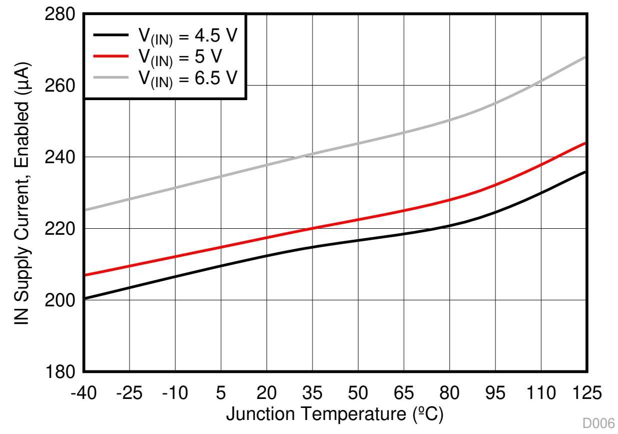
V_{IN} = 5 V

図 6-4. OUT Short-Circuit Current Limit vs Temperature



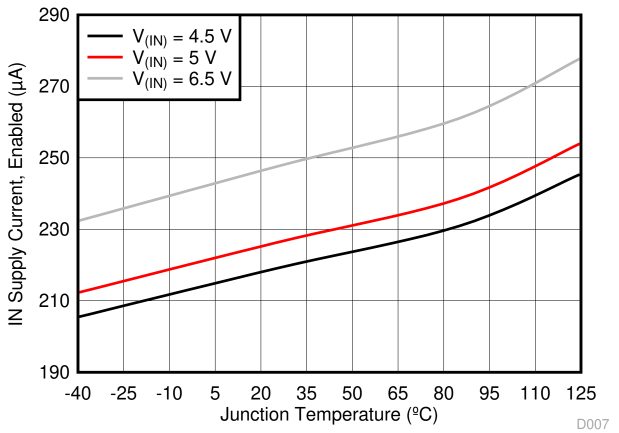
CTL1 = 1 CTL2 = 1 CTL3 = 1

図 6-5. Disabled IN Supply Current vs Temperature



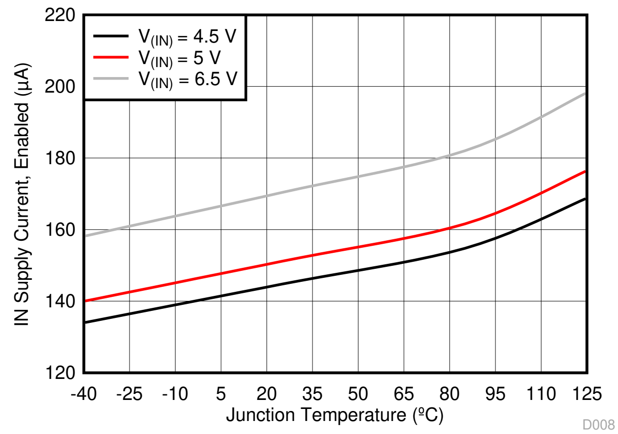
CTL1 = 1 CTL2 = 1 CTL3 = 1

図 6-6. Enabled IN Supply Current – CDP (111) vs Temperature



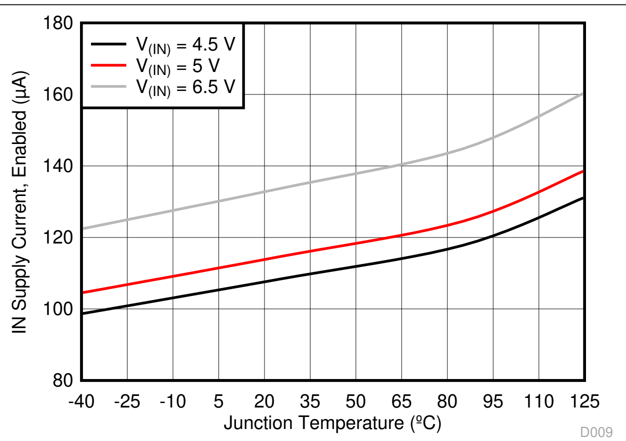
CTL1 = 0 CTL2 = 0 CTL3 = 1

図 6-7. Enabled IN Supply Current – DCP_Auto (001) vs Temperature



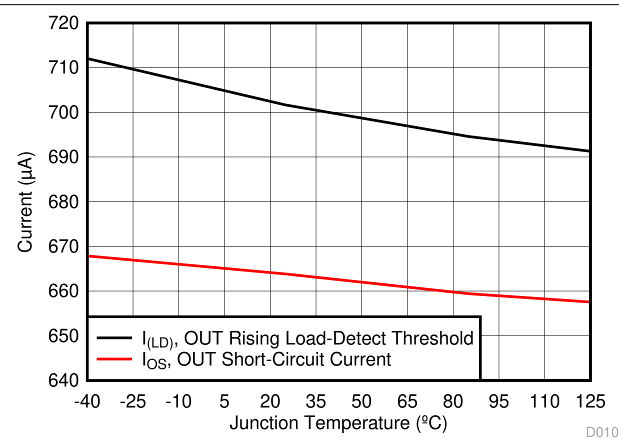
CTL1 = 0 CTL2 = 1 CTL3 = 0

図 6-8. Enabled IN Supply Current – SDP (010) vs Temperature



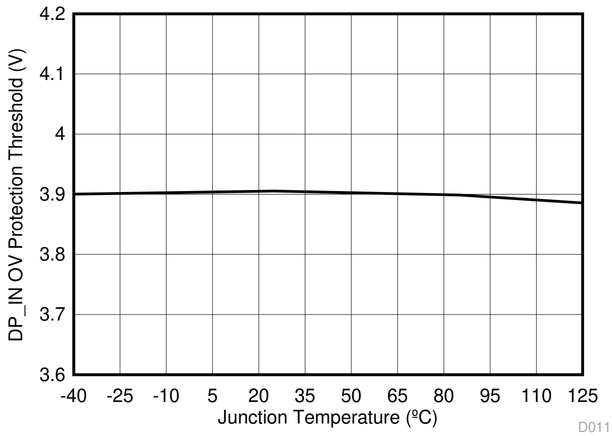
CTL1 = 1 CTL2 = 0 CTL3 = 0

図 6-9. Enabled IN Supply Current – Client Mode (100) vs Temperature



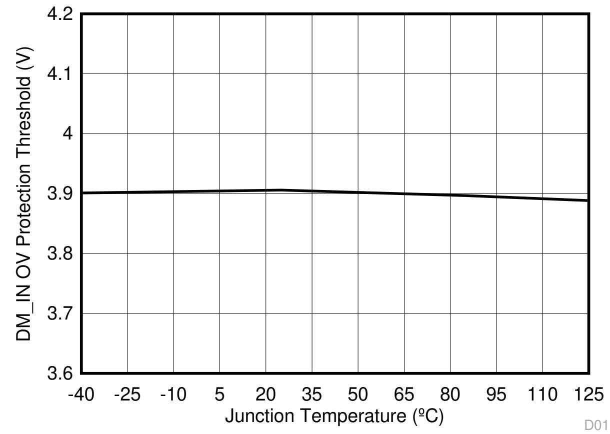
$R_{(ILIM\_LO)}$ = 80.6 kΩ

図 6-10. I_{OUT} Rising Load-Detect Threshold and OUT Short-Circuit Current Limit vs Temperature



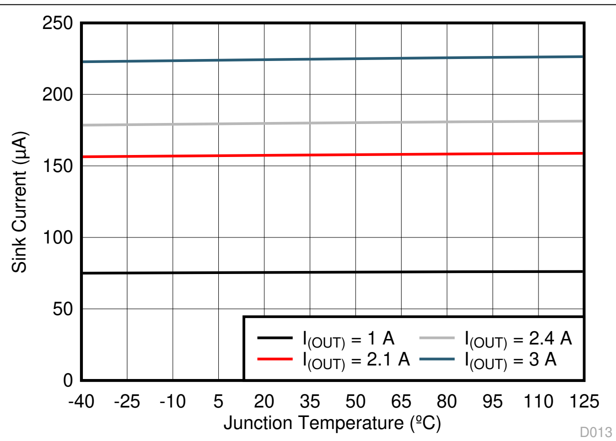
V_{IN} = 5 V

図 6-11. DP_IN Overvoltage Protection Threshold vs Temperature



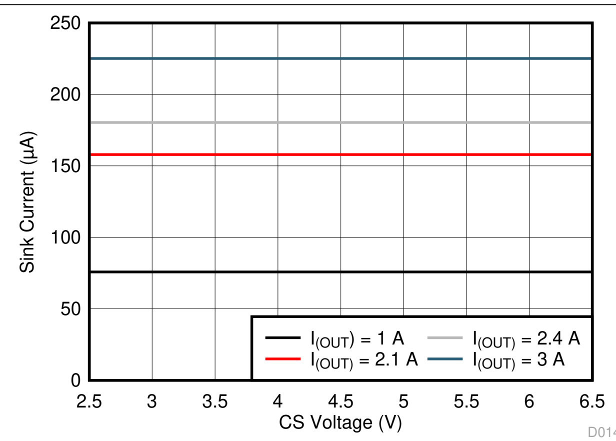
V_{IN} = 5 V

図 6-12. DM_IN Overvoltage Protection Threshold vs Temperature



V_{IN} = 5 V V_{CS} = 2. 5 V

図 6-13. I_{CS} vs Temperature



V_{IN} = 6.5 V

図 6-14. I_{CS} vs V_{CS} Voltage

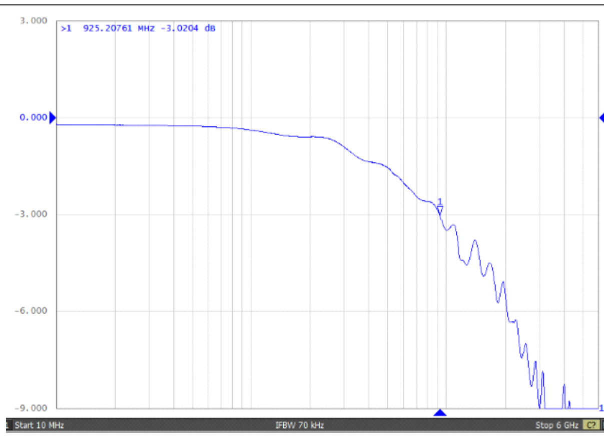


図 6-15. Data Transmission Characteristics vs Frequency

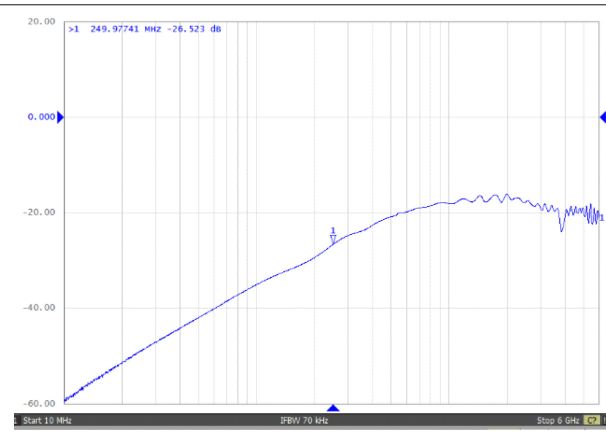


図 6-16. Off-State Data-Switch Isolation vs Frequency

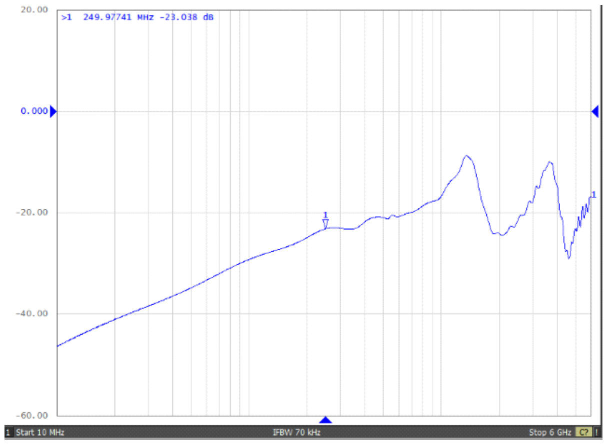


図 6-17. On-State Cross-Channel Isolation vs Frequency

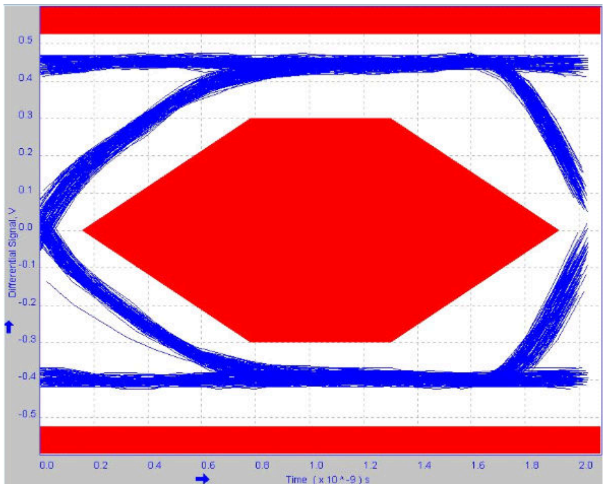


図 6-18. Eye Diagram Using USB Compliance Test Pattern, Bypassing the TPS2549-Q1 Data Switch

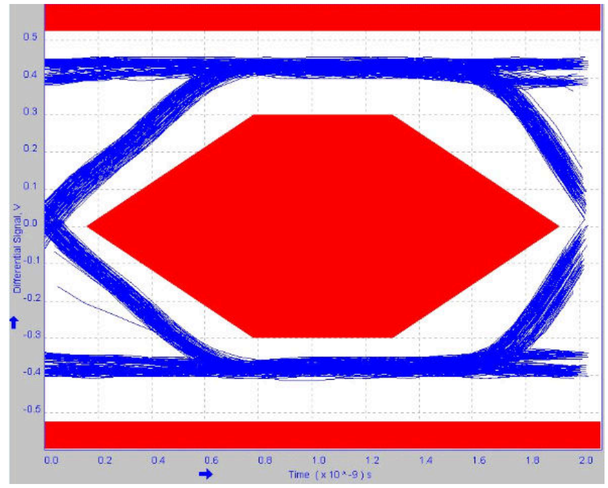


図 6-19. Eye Diagram Using USB Compliance Test Pattern, Through the TPS2549-Q1 Data Switch

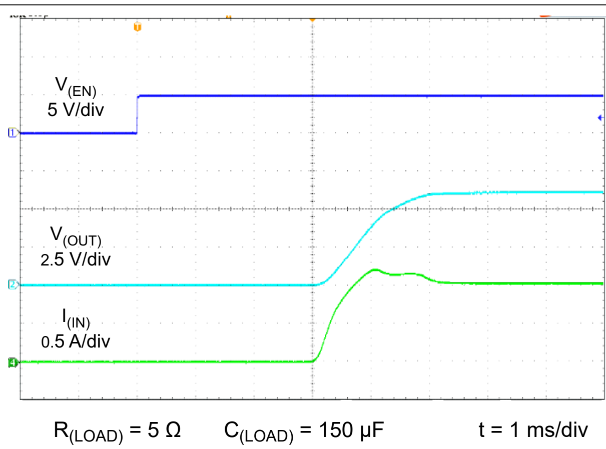


図 6-20. Turnon Response

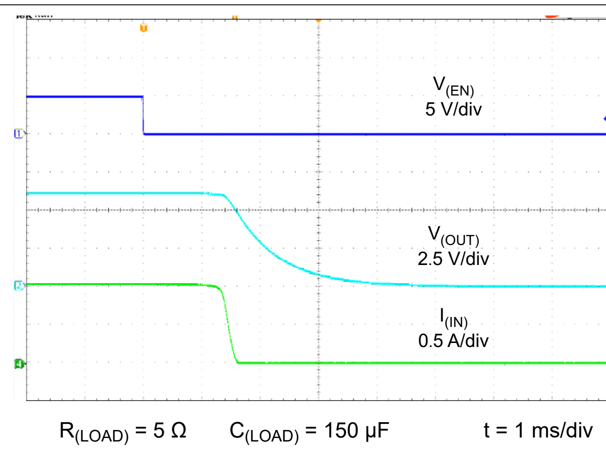


図 6-21. Turnoff Response

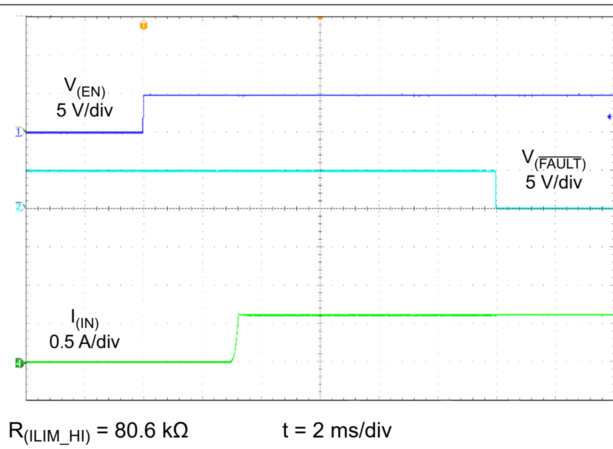


図 6-22. Enable Into Short

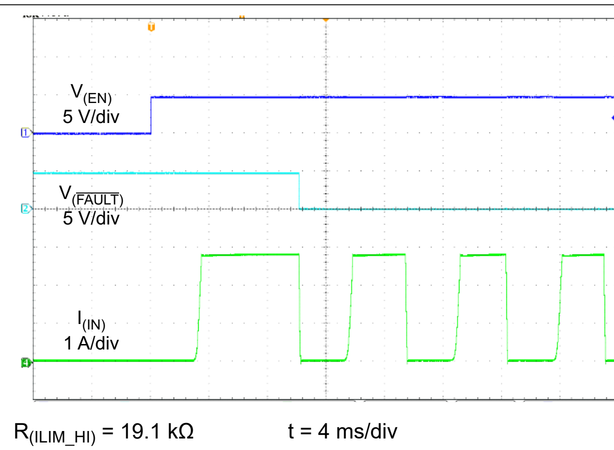


図 6-23. Enable Into Short – Thermal Cycling

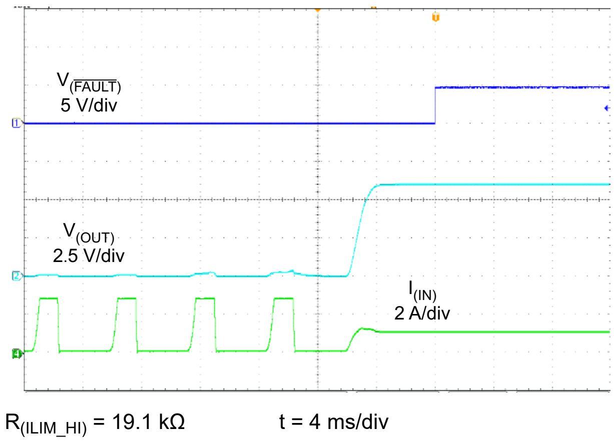


図 6-24. Short-Circuit to Full-Load Recovery

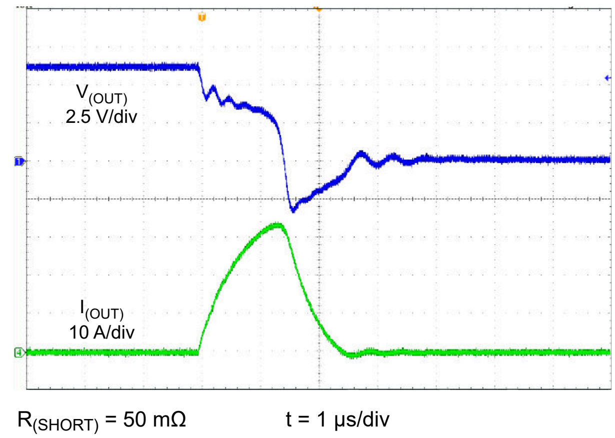


図 6-25. Hot-Short Response Time

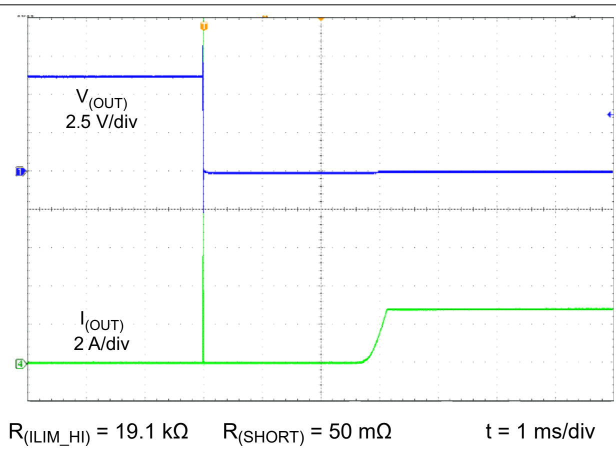


図 6-26. Hot Short

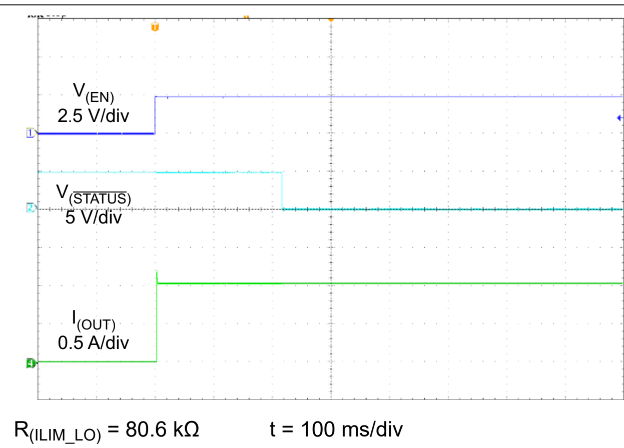


図 6-27. Load-Detection Set Time

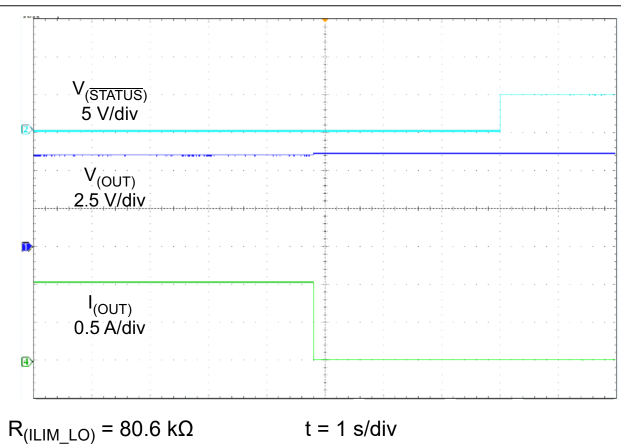


図 6-28. Load Detection Reset Time

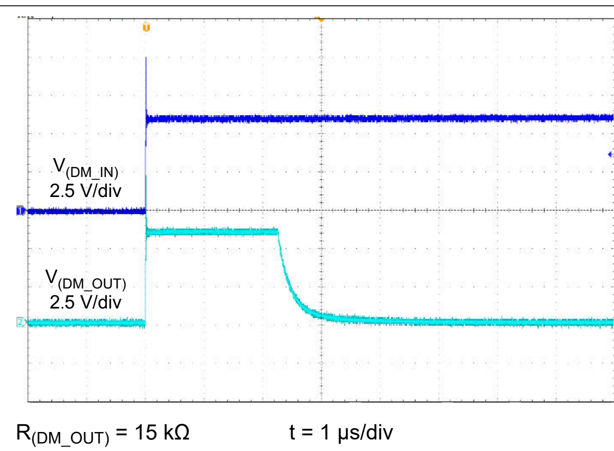


図 6-29. DM_IN Short to V_{BUS} Response Time

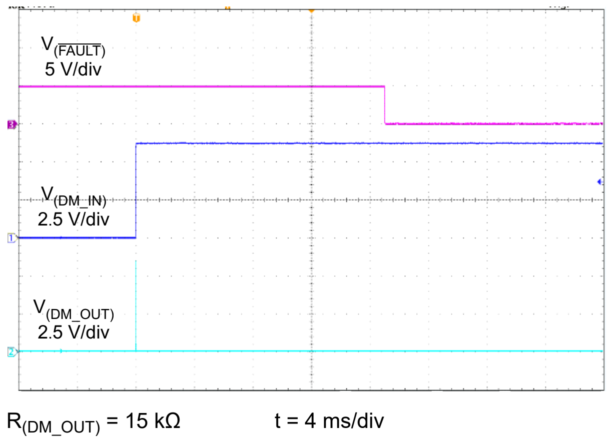


図 6-30. DM_IN Short to V_{BUS}

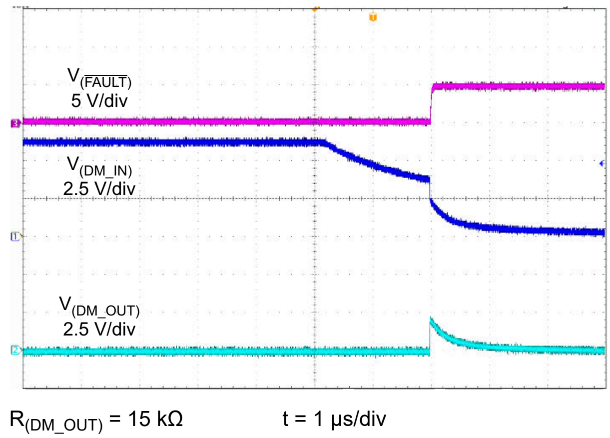


図 6-31. DM_IN Short-to-V_{BUS} Recovery

7 Parameter Measurement Information

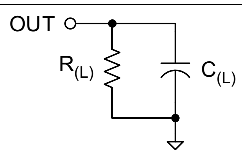


図 7-1. OUT Rise-Fall Test Load Figure

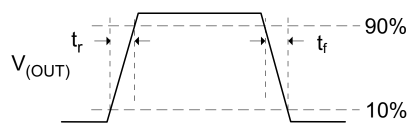


図 7-2. Power-On and -Off Timing

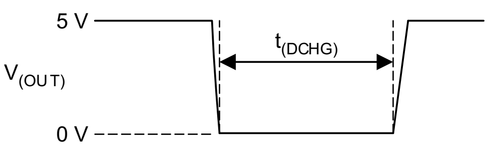


図 7-3. OUT Discharge During Mode Change

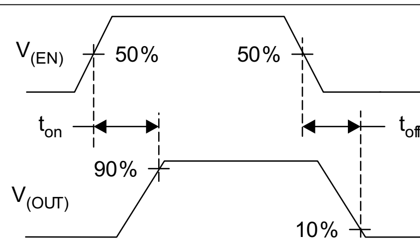


図 7-4. Enable Timing, Active-High Enable

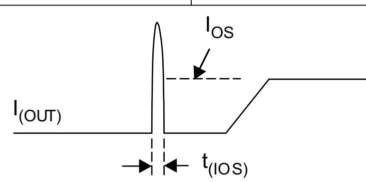


図 7-5. Output Short-Circuit Parameters

8 Detailed Description

8.1 Overview

The TPS2549-Q1 device is a USB charging controller and power switch which integrates D+ and D– short to V_{BUS} protection, cable compensation and IEC ESD protection, and is suitable for automotive USB charging and USB port-protection applications.

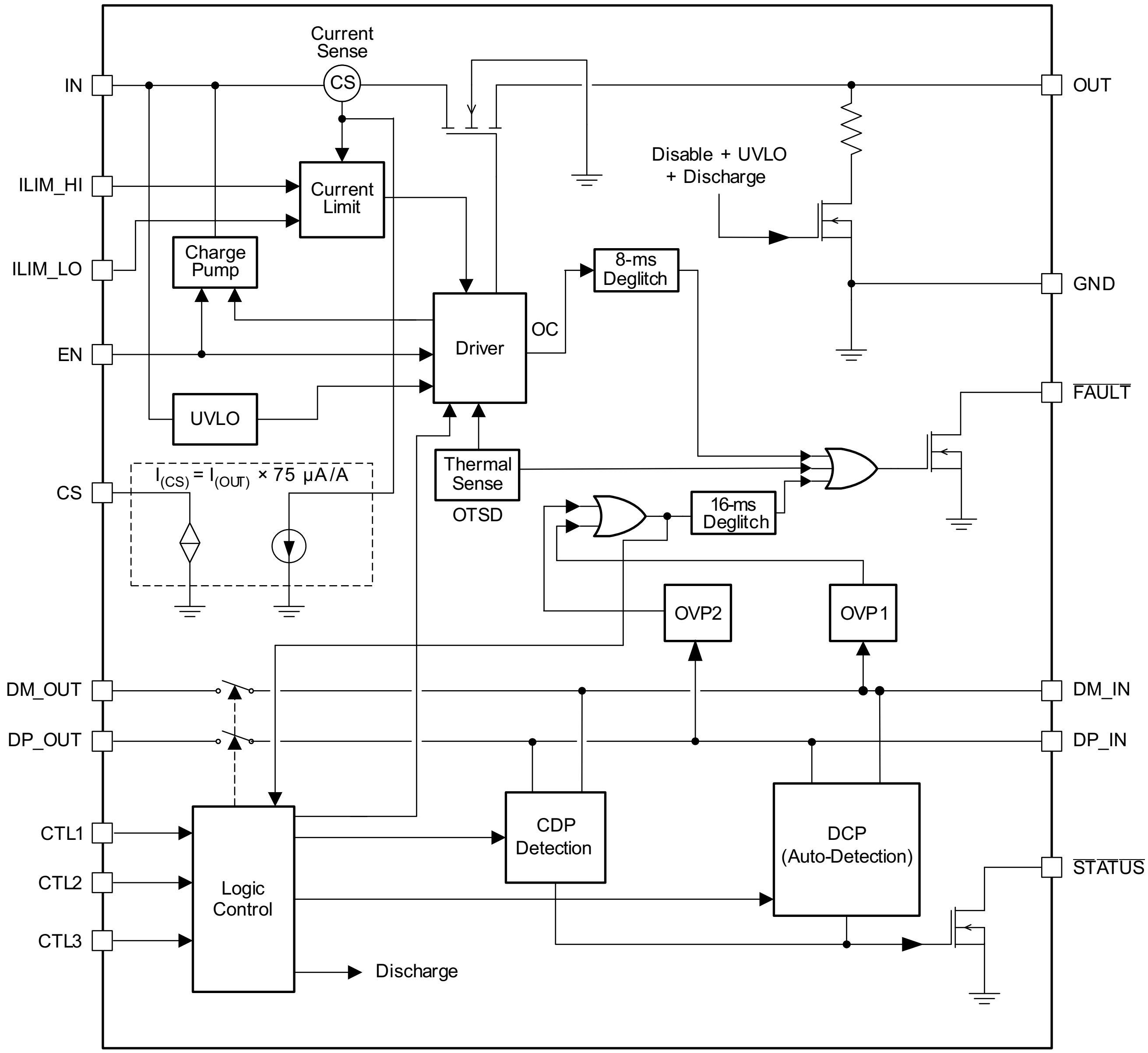
The TPS2549-Q1 device integrates a current-limited, power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads can be encountered. The device allows the user to program the current-limit threshold via an external resistor. The device enters constant-current mode when the load exceeds the current limit threshold.

The TPS2549-Q1 device also integrates CDP mode, defined in the BC1.2 specification, to enable up to 1.5-A fast charging of most of portable devices, meanwhile supporting data communication. In addition, the device integrates the DCP-auto feature to enable fast-charging of most portable devices including pads, tablets, and smart phones.

The TPS2549-Q1 device integrates a cable compensation (CS) feature to compensate the voltage drop in long cables and keep the remote USB port output voltage constant.

Additionally, the device integrates an IEC ESD cell to provide ESD protection up to ±8 kV (contact discharge) and ±15 kV (air discharge) per IEC 61000-4-2 on DP_IN and DM_IN, and integrates short-to-V_{BUS} overvoltage protection on DP_IN and DM_IN to protect the upstream USB transceiver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 FAULT Response

The device features an active-low, open-drain fault output. $\overline{\text{FAULT}}$ goes low when there is a fault condition. Fault detection includes overtemperature, overcurrent, or DP_IN, DM_IN overvoltage. Connect a 10-kΩ pullup resistor from $\overline{\text{FAULT}}$ to IN.

表 8-1 summarizes the conditions that generate a fault and actions taken by the device.

表 8-1. Fault Conditions

EVENT	CONDITION	ACTION
Overcurrent on $V_{(OUT)}$	$I_{(OUT)} > I_{OS}$	The device regulates switch current at I_{OS} until thermal cycling occurs. The fault indicator asserts and de-asserts with an 8-ms deglitch (The device does not assert $\overline{FAULT}$ on overcurrent in SDP1 and DCP1 modes).
Overvoltage on the data lines	DP_IN or DM_IN > 3.9 V	The device immediately shuts off the USB data switches. The fault indicator asserts with a 16-ms deglitch, and de-asserts without deglitch.
Overtemperature	T_J > OTSD2 in non-current-limited or T_J > OTSD1 in current-limited mode.	The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts immediately when the junction temperature exceeds OTSD2 or OTSD1 while in a current-limiting condition. The device has a thermal hysteresis of 20°C.

8.3.2 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator 5-V output to the VPD_IN (input voltage of portable device), the total resistance of power switch $r_{DS(on)}$ and cable resistance causes an IR drop at the PD input.. So the charging current of most portable devices is less than their expected maximum charging current.

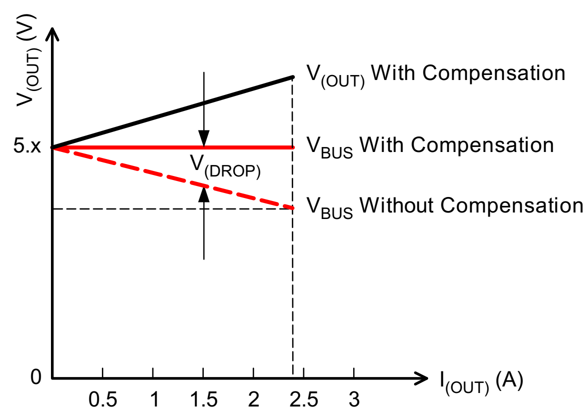


図 8-1. Voltage Drop

TPS2549-Q1 device detects the load current and generates a proportional sink current that can be used to adjust output voltage of the upstream regulator to compensate the IR drop in the charging path. The gain $G_{(CS)}$ of the sink current proportional to load current is 75 µA/A.

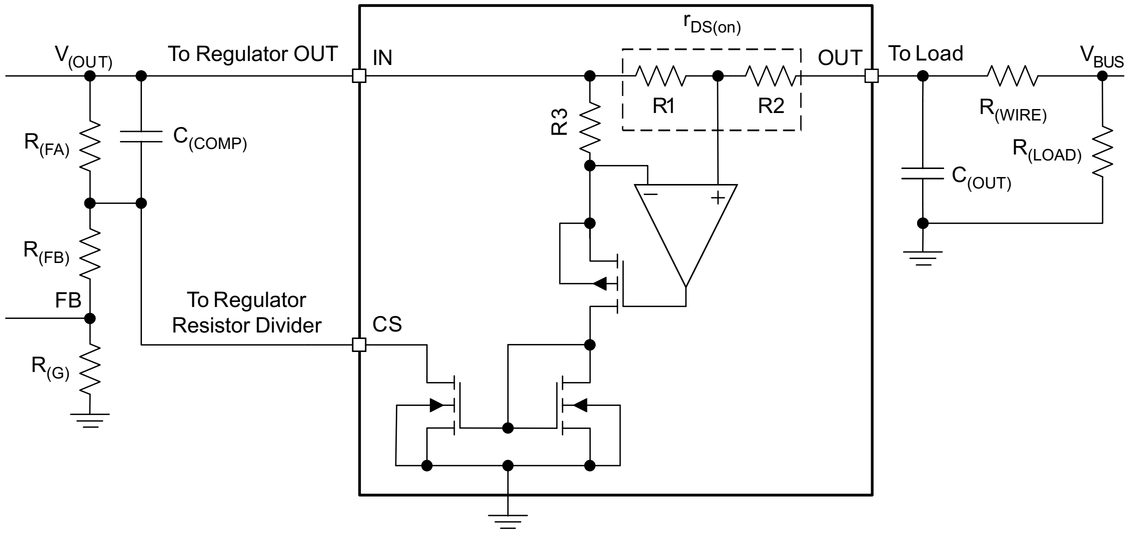


図 8-2. Cable Compensation Equivalent Circuit

8.3.2.1 Design Procedure

To start the procedure, the total resistance, including power switch $r_{DS(on)}$ and wire resistance $R_{(WIRE)}$, must to be known.

1. Choose $R_{(G)}$ following the voltage-regulator feedback resistor-divider design guideline.
2. Calculate $R_{(FA)}$ according to 式 1.

$$R_{FA} = (r_{DS(on)} + R_{(WIRE)}) / G_{(CS)} \tag{1}$$

3. Calculate $R_{(FB)}$ according to Equation 2.

$$R_{(FB)} = \frac{V_{(OUT)}}{V_{(FB)} / R_{(G)}} - R_{(G)} - R_{(FA)} \tag{2}$$

4. $C_{(COMP)}$ in parallel with $R_{(FA)}$ is needed to stablilize $V_{(OUT)}$ when $C_{(OUT)}$ is large. Start with $C_{(COMP)} \geq 3 \times G_{(CS)} \times C_{(OUT)}$, then adjust $C_{(COMP)}$ to optimize the load transient of the voltage regulator output. $V_{(OUT)}$ stability should always be verified in the end application circuit.

8.3.3 D+ and D– Protection

D+ and D– protection consists of ESD and OVP (overvoltage protection). The DP_IN and DM_IN pins integrate an IEC ESD cell to provide ESD protection up to ±15 kV air discharge and ±8 kV contact discharge per IEC 61000-4-2 (See the *ESD Ratings* section for test conditions). Overvoltage protection (OVP) is provided for short-to-V_{BUS} conditions in the vehicle harness to prevent damaging the upstream USB transceiver. Short-to-GND protection for D+ and D– is provided by the upstream USB transceiver.

The ESD stress seen at DP_IN and DM_IN is impacted by many external factors like the parasitic resistance and inductance between ESD test points and the DP_IN and DM_IN pins. For air discharge, the temperature and humidity of the environment can cause some difference, so the IEC performance should always be verified in the end-application circuit.

8.3.4 Output and D+ or D– Discharge

To allow a charging port to renegotiate current with a portable device, the TPS2549-Q1 device uses the OUT discharge function. This function turns off the power switch while discharging OUT with a 500-Ω resistance, then turns the power switches to back on reassert the OUT voltage.

For DP_IN and DM_IN, when OVP is triggered, the device turns on an internal discharge path with 210-Ω resistance. On removal of OVP, this path can discharge the remnant charges to automatically turn on analog switch and turn off this discharge path, thus back into normal mode.

8.3.5 Port Power Management (PPM)

PPM is the intelligent and dynamic allocation of power. PPM is for systems that have multiple charging ports but cannot power them all simultaneously.

8.3.5.1 Benefits of PPM

The benefits of PPM include the following:

- Delivers better user experience
- Prevents overloading of system power supply
- Allows for dynamic power limits based on system state
- Allows every port to potentially be a high-power charging port
- Allows for smaller power-supply capacity because loading is controlled

8.3.5.2 PPM Details

All ports are allowed to broadcast high-current charging. The current-limit is based on ILIM_HI. The system monitors the $\overline{\text{STATUS}}$ pin to see when high-current loads are present. Once the allowed number of ports asserts $\overline{\text{STATUS}}$, the remaining ports are toggled to a non-charging port. The non-charging port current-limit is based on the ILIM_LO setting. The non-charging ports are automatically toggled back to charging ports when a charging port de-asserts $\overline{\text{STATUS}}$.

$\overline{\text{STATUS}}$ asserts in a charging port when the load current is above ILIM_LO + 40 mA for 210 ms (typical). $\overline{\text{STATUS}}$ de-asserts in a charging-port when the load current is below ILIM_LO – 10 mA for 3 seconds (typical).

8.3.5.3 Implementing PPM in a System With Two Charging Ports (CDP and SDP1)

図 8-3 shows the implementation of the two charging ports with data communication, each with a TPS2549-Q1 device and configured in CDP mode. In this example, the 5-V power supply for the two charging ports is rated at less than 3.5 A. Both TPS2549-Q1 devices have ILIM_LO of 1 A and ILIM_HI of 2.4 A. In this implementation, the system can support only one of the two ports at 2.4-A charging current, whereas the other port is set to SDP1 mode and $I_{(LIMIT)}$ corresponds to 1 A. In SDP1 mode, $\overline{\text{FAULT}}$ does not assert for overcurrent.

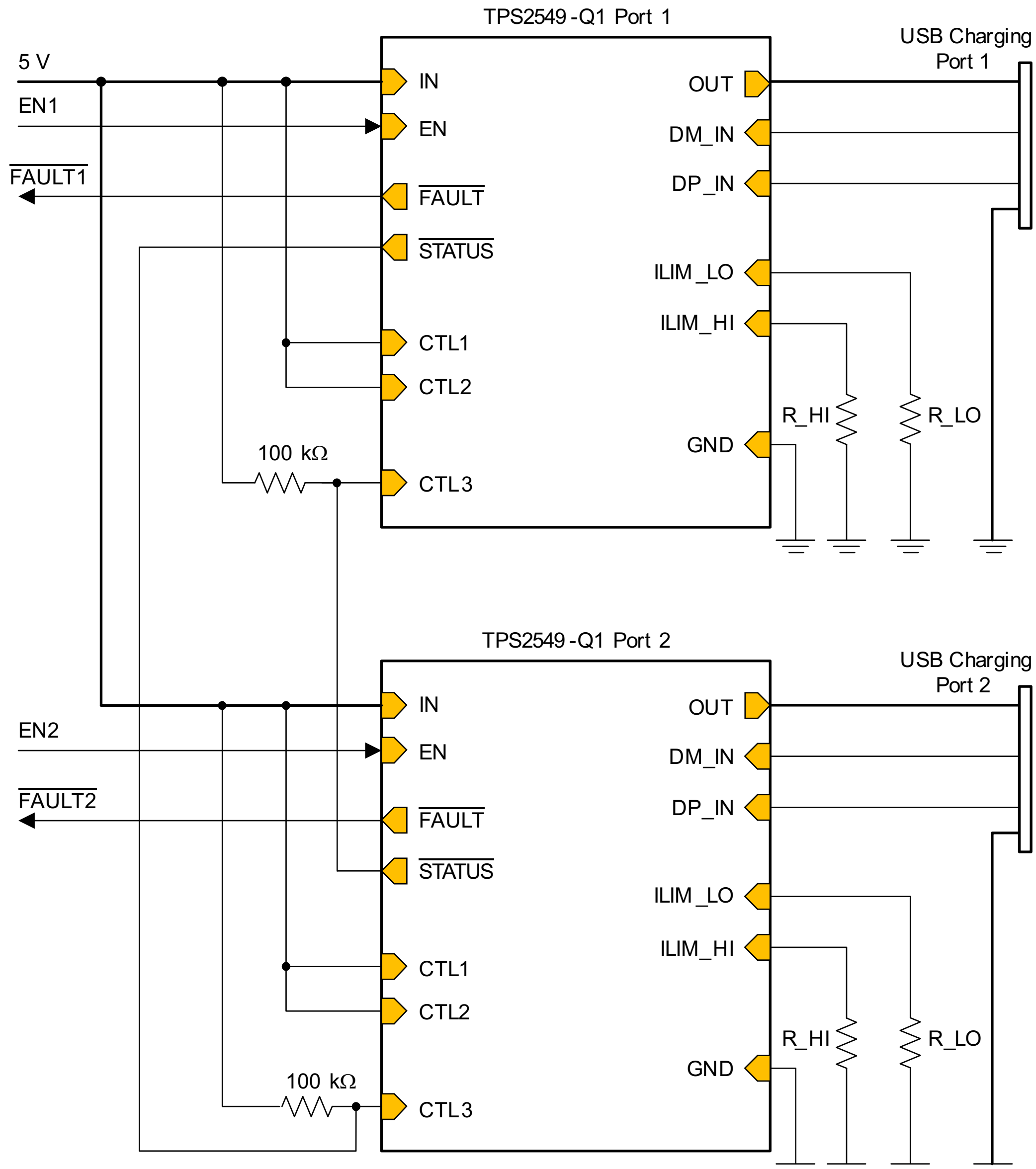


図 8-3. PPM With CDP and SDP1

8.3.5.4 Implementing PPM in a System With Two Charging Ports (DCP and DCP1)

図 8-4 shows the implementation of the two charging-only ports, each with a TPS2549-Q1 device and configured in DCP mode. In this example, the 5-V power supply for the two charging ports is rated at less than 3.5 A. Both TPS2549-Q1 devices have ILIM_LO of 1 A and ILIM_HI of 2.4 A. In this implementation, the system can support only one of the two ports at 2.4-A charging current, whereas the other port is set to DCP1 mode and $I_{(LIMIT)}$ corresponds to 1 A. In DCP1 mode, $\overline{\text{FAULT}}$ does not assert for overcurrent.

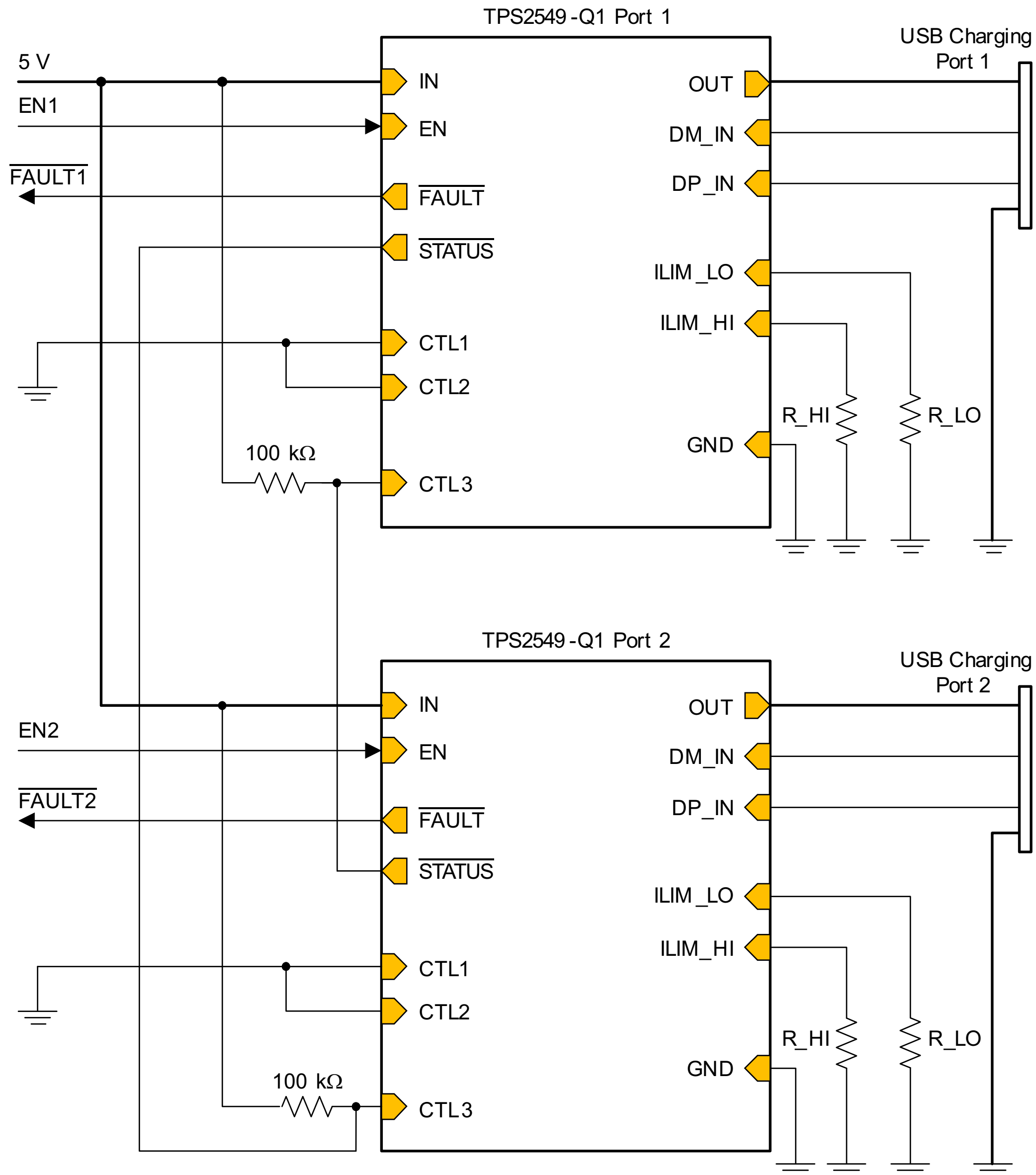


図 8-4. PPM With DCP and DCP1

8.3.6 CDP and SDP Auto Switch

The TPS2549-Q1 device is equipped with a CDP and SDP auto-switch feature to support some popular phones in the market. These popular phones do not comply with the BC1.2 specification because they fail to establish a data connection in CDP mode. These phones use primary detection (used to distinguish between an SDP and different types of charging ports) to only identify ports as SDP (data, no charge) or DCP (no data, charge). These phones do not recognize CDP (data, charge) ports. When connected to a CDP port, these phones classify the port as a DCP and only charge the battery. Because the charging ports are configured as CDP, users do not receive the expected data connection.

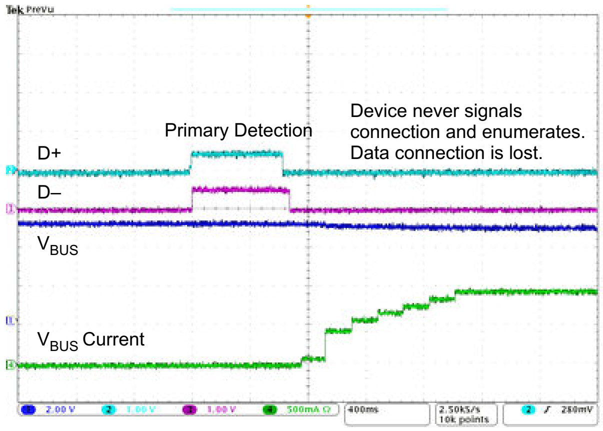


図 8-5. CDP and SDP Auto-Switch

To remedy this problem, the TPS2549-Q1 device employs a CDP and SDP auto-switch scheme to ensure these BC1.2 noncompliant phones establish data connection using the following steps.

1. The TPS2549-Q1 device determines when a noncompliant phone has wrongly classified a CDP port as a DCP port and has not made a data connection.
2. The TPS2549-Q1 device automatically completes an OUT (V_{BUS}) discharge and reconfigures the port as an SDP.
3. When reconfigured as an SDP, the phone detects a connection to an SDP and establishes a data connection.
4. The TPS2549-Q1 device then switches automatically back to a CDP without doing an OUT (V_{BUS}) discharge.
5. The phone continues to operate as if connected to an SDP because OUT (V_{BUS}) was not interrupted. The port is now ready in CDP if a new device is attached.

8.3.7 Overcurrent Protection

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output is shorted before the device enables or before the application of $V_{(IN)}$. The TPS2549-Q1 device senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents flow for 2 µs (typical) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is presented long enough to activate overtemperature protection. The device remains off until the junction temperature cools to approximately 20°C and then restarts. The device continues to cycle on and off until the overcurrent condition is removed.

8.3.8 Undervoltage Lockout

The undervoltage-lockout (UVLO) circuit disables the device until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

8.3.9 Thermal Sensing

Two independent thermal-sensing circuits protect the TPS2549-Q1 device if the temperature exceeds recommended operating conditions. These circuits monitor the operating temperature of the power-distribution switch and disable operation. The device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an overcurrent condition. When the device is in a current-limiting condition, the first thermal sensor turns off the power switch when the die temperature exceeds OTSD1. If the device is not in a current-limiting condition, the second thermal sensor turns off the power switch when the die temperature exceeds OTSD2. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and then on until the fault is removed. The open-drain false-reporting output, $\overline{\text{FAULT}}$, is asserted (low) during an overtemperature shutdown condition.

8.3.10 Current Limit Setting

The TPS2549-Q1 has two independent current-limit settings that are each programmed externally with a resistor. The ILIM_HI setting is programmed with $R_{(ILIM\_HI)}$ connected between ILIM_HI and GND. The ILIM_LO setting is programmed with $R_{(ILIM\_LO)}$ connected between ILIM_LO and GND. Consult the device truth table (表 8-2) to see when each current limit is used. Both settings have the same relation between the current limit and the programming resistor.

$R_{(ILIM\_LO)}$ is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

- The TPS2549-Q1 device is configured as DCP(001) or CDP(111).
- Load detection is not used.

The following equation calculates the value of resistor for programming the typical current limit:

$$I_{(OSnom)}\ (mA) = \frac{53762\ (V)}{R_{(ILIM\_xx)}{}^{1.0021}\ (k\Omega)} \tag{3}$$

$R_{(ILIM\_xx)}$ corresponds to either $R_{(ILIM\_HI)}$ or $R_{(ILIM\_LO)}$, as appropriate.

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPS2549-Q1 current limit and the tolerance of the external programming resistor must be taken into account. The following equations approximate the TPS2549-Q1 minimum and maximum current limits to within a few milliamperes and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal—no variation—external programming resistor. To take resistor tolerance into account, first determine the minimum and maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the programming resistor, use the maximum resistor value in the $I_{(OS\_min)}$ equation and the minimum resistor value in the $I_{(OS\_max)}$ equation.

$$I_{(OSmin)}\ (mA) = \frac{50409\ (V)}{R_{(ILIM\_xx)}{}^{0.9982}\ (k\Omega)} - 35 \tag{4}$$

$$I_{(OSmax)}\ (mA) = \frac{57813\ (V)}{R_{(ILIM\_xx)}{}^{1.0107}\ (k\Omega)} + 41 \tag{5}$$

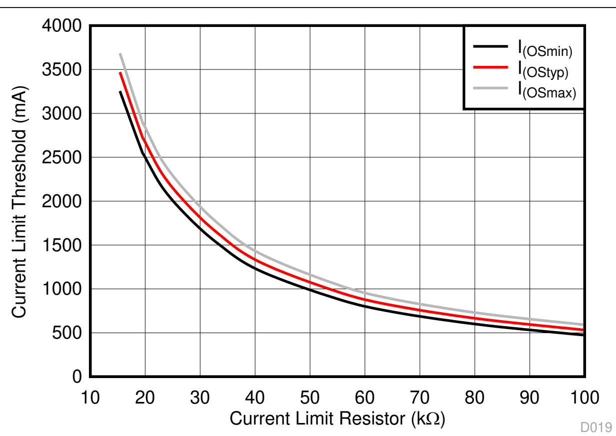


図 8-6. Current Limit Setting vs Programming Resistor I

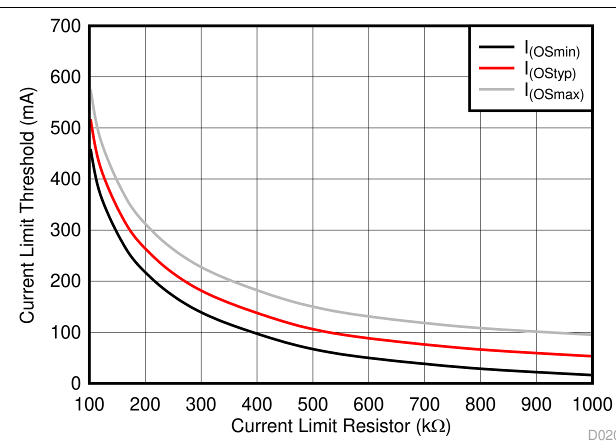


図 8-7. Current Limit Setting vs Programming Resistor II

The routing of the traces to the $R_{(ILIM\_xx)}$ resistors should have a sufficiently low resistance so as to not affect the current-limit accuracy. The ground connection for the $R_{(ILIM\_xx)}$ resistors is also very important. The resistors must reference back to the TPS2549-Q1 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPS2549-Q1 GND pin.

8.4 Device Functional Modes

8.4.1 Device Truth Table (TT)

The device truth table (表 8-2) lists all valid combinations for the three control pins (CTL1 through CTL3), and the corresponding charging mode of each pin combination. The TPS2549-Q1 device monitors the CTL inputs and transitions to whichever charging mode it is commanded to go to. For example, if the USB port is a charging-only port, then the user must set the CTL pins of the TPS2549-Q1 device to correspond to the DCP-auto charging mode. However, when the USB port requires data communication, then the user must set control pins to correspond to the SDP or CDP mode, and so on.

表 8-2. Truth Table

CTL1	CTL2	CTL3	CURRENT LIMIT SETTING	MODE	STATUS OUTPUT (ACTIVE-LOW)	FAULT OUTPUT (ACTIVE-LOW)	CS FOR CABLE COMPENSATION	NOTES
0	0	0	Lo	DCP1(1)	OFF	ON(2)	ON	DCP includes divider 3, 1.2-V mode, and BC1.2 mode
0	0	1	Hi	DCP(1)	ON	ON	ON	DCP includes divider 3, 1.2-V mode, and BC1.2 mode
0	1	X	Lo	SDP	OFF	ON	ON	Standard SDP port
1	0	X	NA	Client mode	OFF	OFF	OFF	No current limit, power switch disabled, data switch bypassed
1	1	0	Lo	SDP1(3)	OFF	ON(2)	ON	Standard SDP port
1	1	1	Hi	CDP(3)	ON	ON	ON	CDP-SDP auto switch mode

(1) No OUT discharge when changing between 000 and 001
(2) $\overline{\text{FAULT}}$ not asserted on overcurrent
(3) No OUT discharge when changing between 110 and 111

8.4.2 USB Specification Overview

The following overview references various industry standards. TI recommends consulting the most up-to-date standards to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge batteries. USB ports are a convenient location for charging because of an available 5-V power source. Universally accepted standards are required to ensure host and client-side devices operate together in a system to ensure power-management requirements are met. Traditionally, host ports following the USB-2.0 specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, the client-side device sets the power allotment from the host to ensure the total current draw does not exceed 500 mA. In general, each USB device is granted 100 mA and can request more current in 100-mA unit steps up to 500 mA. The host grants or denies additional current based on the available current. A USB-3.0 host port not only provides higher data rate than a USB-2.0 port but also raises the unit load from 100 mA to 150 mA. Providing a minimum current of 900 mA to downstream client-side devices is required.

Additionally, the success of USB has made the micro-USB and mini-USB connectors a popular choice for wall-adapter cables. A micro-USB or mini-USB allows a portable device to charge from both a wall adapter and USB port with only one connector. As USB charging has gained popularity, the 500-mA minimum defined by USB 2.0, or 900 mA for USB 3.0, has become insufficient for many handset and personal media players, which require a higher charging rate. Wall adapters provide much more current than 500 or 900 mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500-mA and 900-mA minimum defined by USB 2.0 and USB 3.0, respectively, while still using a single micro-USB or mini-USB input connector.

The TPS2549-Q1 device supports four of the most-common USB-charging schemes found in popular hand-held media and cellular devices.

- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider 3 mode
- 1.2-V mode

The BC1.2 specification includes three different port types:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are defined as charging ports.

表 8-3 lists the difference between these port types.

表 8-3. Operating Modes Table

PORT TYPE	SUPPORTS USB2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	YES	0.5
SDP (USB 3.0)	YES	0.9
CDP	YES	1.5
DCP	NO	1.5

8.4.3 Standard Downstream Port (SDP) Mode — USB 2.0 and USB 3.0

An SDP is a traditional USB port that follows USB 2.0 or USB 3.0 protocol. A USB 2.0 SDP supplies a minimum of 500 mA per port and supports USB 2.0 communications. A USB 3.0 SDP supplies a minimum of 900 mA per port and supports USB 3.0 communications. For both types, the host controller must be active to allow charging.

8.4.4 Charging Downstream Port (CDP) Mode

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5 A per port. A CDP provides power and meets the USB 2.0 requirements for device enumeration. USB-2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP handshaking process occurs in two steps. During step one, the portable equipment outputs a nominal 0.6-V output on the D+ line and reads the voltage input on the D– line. The portable device detects the connection to an SDP if the voltage is less than the nominal data-detect voltage of 0.3 V. The portable device detects the connection to a CDP if the D– voltage is greater than the nominal data detect voltage of 0.3 V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine whether the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6-V output on the D– line and reads the voltage input on the D+ line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detects voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V.

8.4.5 Dedicated Charging Port (DCP) Mode

A DCP only provides power and does not support data connection to an upstream port. As shown in the following sections, a DCP is identified by the electrical characteristics of the data lines. The TPS2549-Q1 only emulates one state, DCP-auto state. In the DCP-auto state, the device charge-detection state machine is activated to selectively implement charging schemes involved with the shorted, divider3 and 1.2 v modes. The shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, whereas the divider3 and 1.2 V modes are employed to charge devices that do not comply with the BC1.2 DCP standard.

8.4.5.1 DCP BC1.2 and YD/T 1591-2009

Both standards specify that the D+ and D– data lines must be connected together with a maximum series impedance of 200 Ω, as shown in 図 8-8.

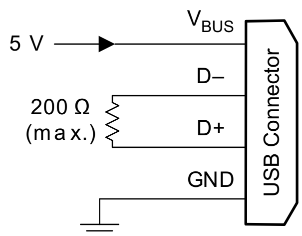


図 8-8. DCP Supporting BC1.2 and YD/T 1591-2009

8.4.5.2 DCP Divider-Charging Scheme

The device supports divider3, as shown in 図 8-9. In the Divider3 charging scheme the device applies 2.7 V and 2.7 V to D+ and D– data lines.

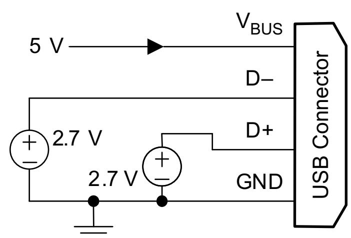


図 8-9. Divider 3 Mode

8.4.5.3 DCP 1.2-V Charging Scheme

The DCP 1.2-V charging scheme is used by some hand-held devices to enable fast charging at 2 A. The TPS2549-Q1 device supports this scheme in DCP-auto state before the device enters BC1.2 shorted mode. To simulate this charging scheme, the D+ and D– lines are shorted and pulled up to 1.2 V for a fixed duration. Then the device moves to DCP shorted mode as defined in the BC1.2 specification and as shown in 図 8-10.

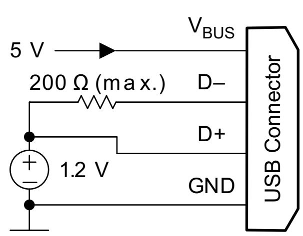


図 8-10. 1.2-V Mode

8.4.6 DCP Auto Mode

As previously discussed, the TPS2549-Q1 device integrates an auto-detect state machine that supports all the DCP charging schemes. The auto-detect state machine starts in the Divider3 scheme. However, if a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS2549-Q1 device responds by turning the power switch back on without output discharge and operating in 1.2-V mode briefly before entering BC1.2 DCP mode. Then the auto-detect state machine stays in that mode until the device releases the data line, in which case the auto-detect state machine goes back to the Divider3 scheme. When a Divider3-compliant device is attached, the TPS2549-Q1 device stays in the Divider3 state.

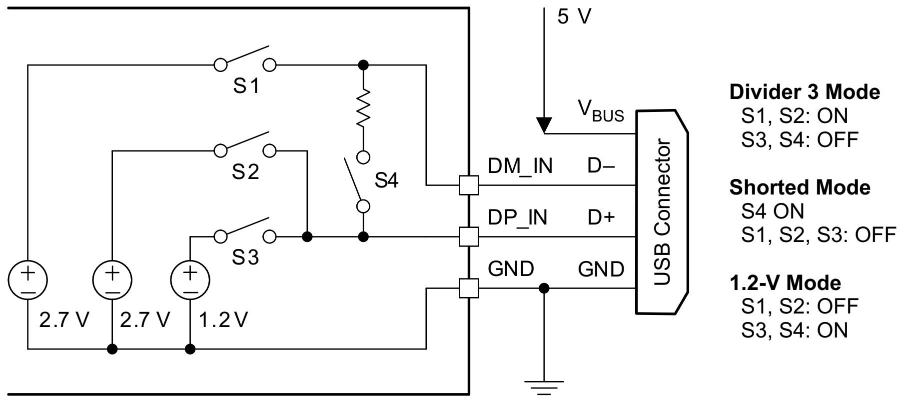


図 8-11. DCP Auto Mode

8.4.7 Client Mode

The TPS2549-Q1 device integrates client mode as shown in 図 8-12. The internal power switch is OFF and only the data analog switch is ON to block OUT power. This mode can be used for some software programming via the USB port.

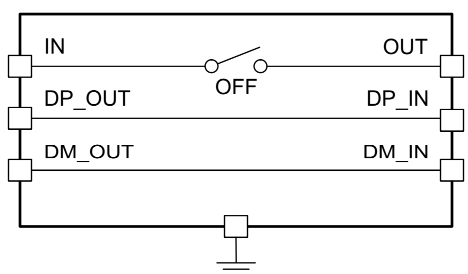


図 8-12. Client-Mode Equivalent Circuit

8.4.8 High-Bandwidth Data-Line Switches

The TPS2549-Q1 device passes the D+ and D– data lines through the device to enable monitoring and handshaking while supporting the charging operation. A wide-bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data-line switches are turned on in any of the CDP, SDP, or client operating modes. The EN input must be at logic high for the data line switches to be enabled.

Note

- While in CDP mode, the data switches are ON, even during CDP handshaking.
- The data line switches are OFF if EN is low, or if in DCP mode. The switches are not automatically turned off if the power switch (IN to OUT) is in current-limit.
- The data switches are only for a USB-2.0 differential pair. In the case of a USB-3.0 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPS2549-Q1 device.
- Data switches are OFF during OUT (V_{BUS}) discharge.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2549-Q1 device is a USB charging-port controller and power switch with cable compensation. It is typically used for automotive USB port protection and as a USB charging controller. The following design procedure can be used to select components for the TPS2549-Q1 device. This section presents a simplified discussion of how to design cable compensation.

9.2 Typical Application

Automotive USB port charging requires a voltage regulator to convert battery voltage to 5-V V_{BUS} output. Because the V_{BUS}, D+, and D– pins of a USB port are exposed, there is a need for a protection device that has V_{BUS} overcurrent and D+ and D– ESD protection. An additional need is a charging controller with integrated CDP and DCP charging protocols on D+ and D– to support fast charging. A schematic of an application circuit with cable compensation is shown in 図 9-1. An LMR14030 device is used as the voltage regulator, and the TPS2549-Q1 device is used as the charging controller with protection features.

Nowadays, automotive products have higher safety requirements; the exposed pins including VBUS / D+ / D- may also short to battery in real applications. More details can be learned through this application note: SLVAEI5. The TPS2549-Q1 has short to VBUS protection, but does not support short to battery protection. If short circuit to battery protection is needed, the TPS254900A-Q1 or TPS25830-Q1 are recommended options.

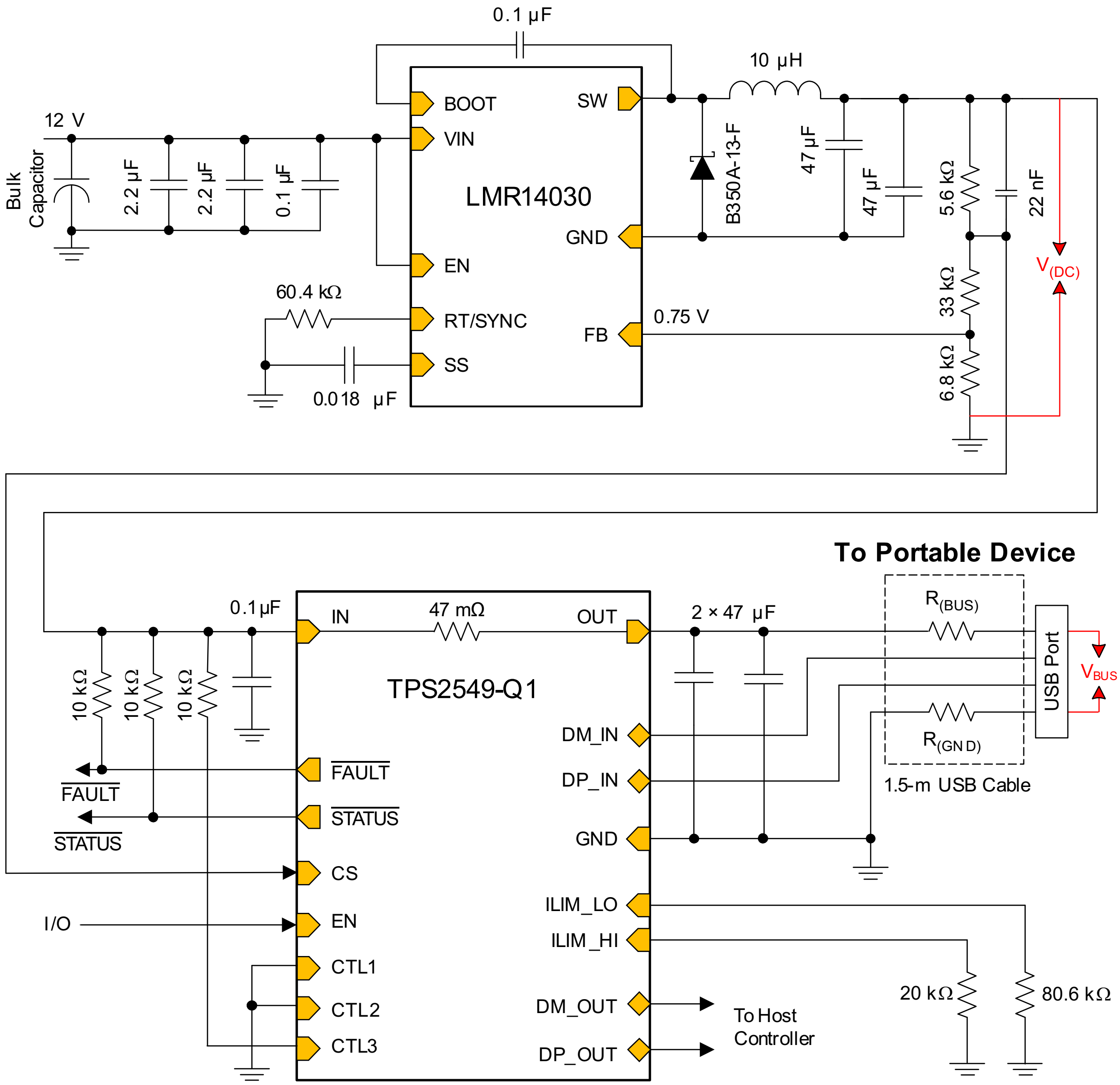


図 9-1. Typical Application Schematic: USB Port Charging With Cable Compensation

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, $V_{(IN)}$	12 V
Output voltage, $V_{(DC)}$	5 V
Total parasitic resistance including TPS2549-Q1 $r_{DS(on)}$	420 mΩ
Maximum continuous output current, $I_{(OUT)}$	2.4 A
Current limit, $I_{(LIM)}$	2.5 A to 2.9 A

9.2.2 Detailed Design Procedure

To begin the design process, a few parameters must be decided upon. The designer needs to know the following:

- Total resistance including power switch $r_{DS(on)}$, cable resistance, and the contact resistance of connectors
- The maximum continuous output current for the charging port. The minimum current-limit setting of TPS2549-Q1 device must be higher than this current.
- The maximum output current of the upstream dc-dc converter. The maximum current-limit setting of TPS2549-Q1 device must be lower than this current.

9.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. All protection circuits including the TPS2549-Q1 device have the potential for input voltage droop, overshoot, and output-voltage undershoot.

For all applications, TI recommends a 0.1-µF or greater ceramic bypass capacitor between IN and GND, placed as close as possible to the device for the local noise decoupling.

The TPS2549-Q1 device is used for 5-V power rail protection when a hot-short occurs on the output or when plugging in a capacitive load. Due to the limited response time of the upstream power supply, a large load transient can deplete the charge on the output capacitor of the power supply, causing a voltage droop. If the power supply is shared with other loads, ensure that voltage droop from current surges of the other loads do not force the TPS2549-Q1 device into UVLO. Increasing the upstream power supply output capacitor can reduce this droop. Shortening the connection impedance (resistance and inductance) between the TPS2549-Q1 device and the upstream power supply can also help reduce the voltage droop and overshoot on the TPS2549-Q1 input power bus.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the IN terminal is in the high-impedance state (before turnon). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of output short-circuit current when the TPS2549-Q1 device turns off and energy stored in the input inductance drives the input voltage high. Applications with large input inductance (for example, connecting the evaluation board to the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute maximum voltage of the device.

For output capacitance, consider the following three application situations.

The first, output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS2549-Q1 has abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. Second, for USB-port application, because the OUT pin is exposed to the air, the application must withstand ESD stress without damage. Because there is no internal IEC ESD cell as on DP_IN and DM_IN, using a low-ESR capacitance can make this pin robust. Third, when plugging in apacitive load such as the input capacitor of any portable device, having a large output capacitance can help reduce the peak current and up-stream power supply output voltage droop. So for TPS2549-Q1 output capacitance, recommended practice is typically adding two 47-µF ceramic capacitors.

9.2.2.2 Cable Compensation Calculation

Based on the known total resistance, 表 9-1 shows the calculation.

表 9-1. Cable Compensation Calculation

	CALCULATION EQUATION(1)	CALCULATED VALUE	ASSEMBLY VALUE
$V_{(DC)}$ (V) without load		5	
$R_{(G)}$ (kΩ)		6.8	6.8
$R_{(total)}$ (Ω)		0.42	
$G_{(CS)}$ (mA/A)		0.075	
$R_{(FA)}$ (kΩ)	$R_{(FA)} = R_{(total)} / G_{(CS)}$	5.6	5.6
$V_{(FB)}$ (V)		0.75	
$R_{(FB)}$ (kΩ)	$R_{(FB)} = [V_{(DC)} / (V_{(FB)} / R_{(G)})] – R_{(G)} – R_{(FA)}$	32.93	33
$V_{(CS)}$ (V)(2)	$V_{CS} = (V_{(FB)} / R_{(G)}) \times (R_{(G)} + R_{(FB)})$	4.39	
Maximum I_{OS} (A) at 20 kΩ		2.84	
$V_{(DC,max)}$ output (V)(3)	$V_{(DC,max)} = 5 + I_{(OS,max)} \times G_{(CS,max)} \times R_{(FA)}$	6.25	
$C_{(OUT)}$ (µF)			2 × 47
$C_{(COMP)}$ (nF)(4)	$C_{(COMP)} \geq 3 \times G_{(CS)} \times C_{(OUT)}$	≥21.15	22

(1) See 図 8-2 and *Design Procedure*.
(2) Ensure that V_{CS} exceeds 2.5 V.
(3) Ensure that the maximum dc-dc output voltage is lower than 6.5 V when considering $I_{(OS,max)}$ and $G_{(CS,max)}$.
(4) C_{COMP} impacts load-transient performance, so the output performance should always be verified in the end application circuit.

9.2.2.3 Power Dissipation and Junction Temperature

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The following analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system-level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system-level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}^2 \quad (6)$$

where:

P_D = Total power dissipation (W)

$r_{DS(on)}$ = Power-switch on-resistance (Ω)

I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (7)$$

where:

T_A = Ambient temperature (°C)

$R_{\theta JA}$ = Thermal resistance (°C/W)

P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the *refined* $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $R_{\theta JA}$, and thermal resistance is highly dependent on the individual package and board layout.

9.3 Application Curves

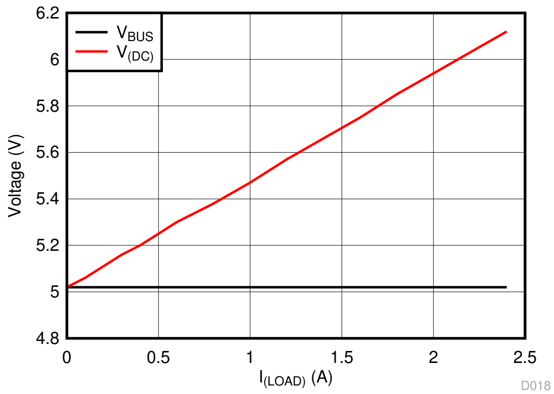


図 9-2. $V_{(DC)}$ and V_{BUS} vs $I_{(LOAD)}$ Output

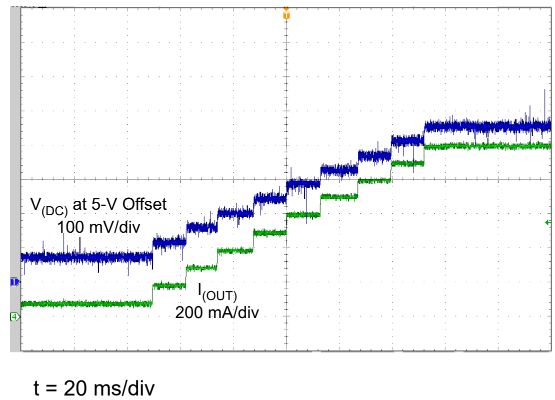


図 9-3. Plugging In a Portable Device, $V_{(DC)}$

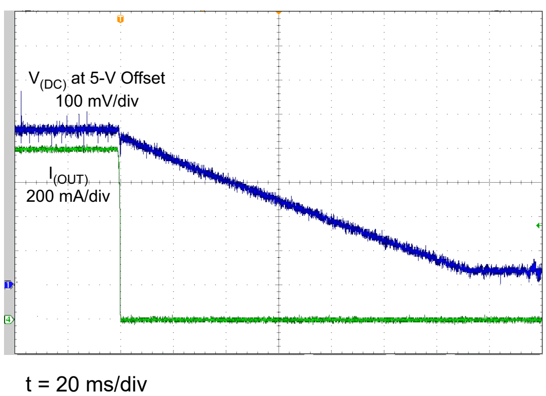


図 9-4. Unplugging a Portable Device, $V_{(DC)}$

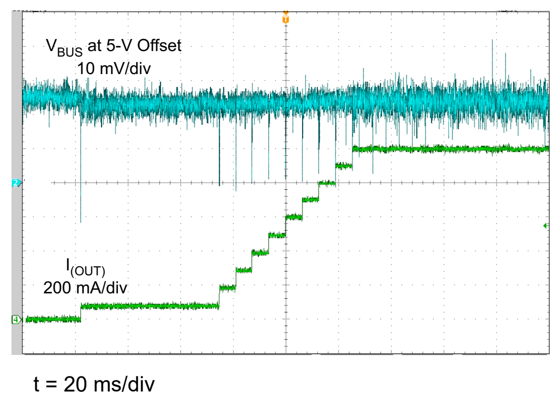


図 9-5. Plugging In Portable Device, V_{BUS}

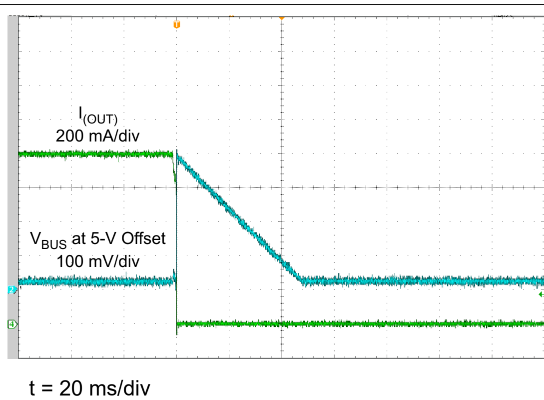


図 9-6. Unplugging Portable Device, V_{BUS}

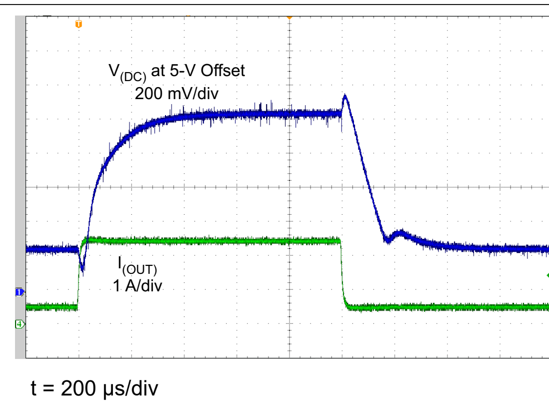


図 9-7. 0.5-A ↔ 2.4-A Load Transient With 100-mA/µs Slew Rate, $V_{(DC)}$

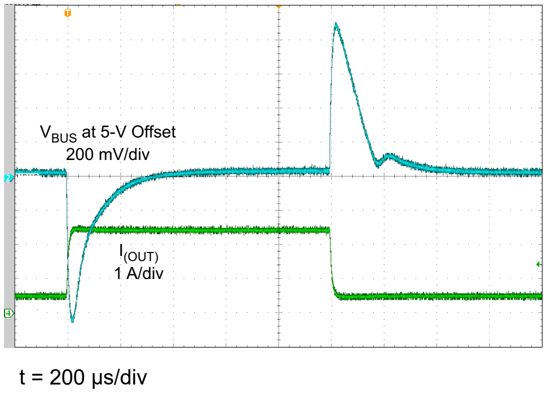


図 9-8. 0.5-A ↔ 2.4-A Load Transient With 100-mA/µs Slew Rate, V_{BUS}

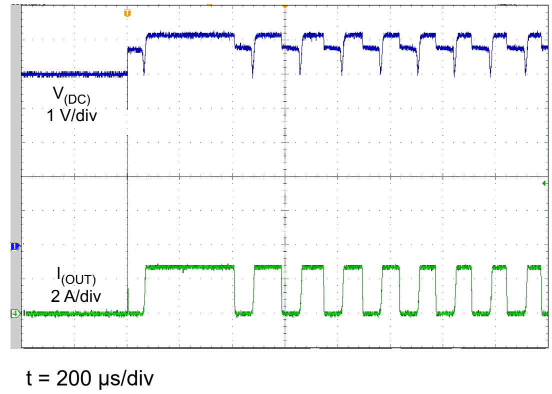


図 9-9. V_{BUS} Shorted to GND, $V_{(DC)}$

10 Power Supply Recommendations

The TPS2549-Q1 device is designed for a supply-voltage range of 4.5 V ≤ V_{IN} ≤ 6.5 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. The power supply should be rated higher than the TPS2549-Q1 current-limit setting to avoid voltage droops during overcurrent and short-circuit conditions.

11 Layout

11.1 Layout Guidelines

- For the trace routing of DP_IN, DM_IN, DP_OUT, and DM_OUT: Route these traces as micro-strips with nominal differential impedance of 90 Ω. Minimize the use of vias in the high-speed data lines. Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities. For more information, see the *High Speed USB Platform Design Guideline* from Intel.
- The trace routing from the upstream regulator to the TPS2549-Q1 IN pin should as short as possible to reduce the voltage drop and parasitic inductance.
- The traces routing from the R_{ILIM_HI} and R_{ILIM_LO} resistors to the device should be as short as possible to reduce parasitic effects on the current-limit accuracy.
- The thermal pad should be directly connected to the PCB ground plane using a wide and short copper trace.
- The trace routing from the CS pin to the feedback divider of the upstream regulator should not be routed near any noise sources that can capacitively couple to the feedback divider.

11.2 Layout Example

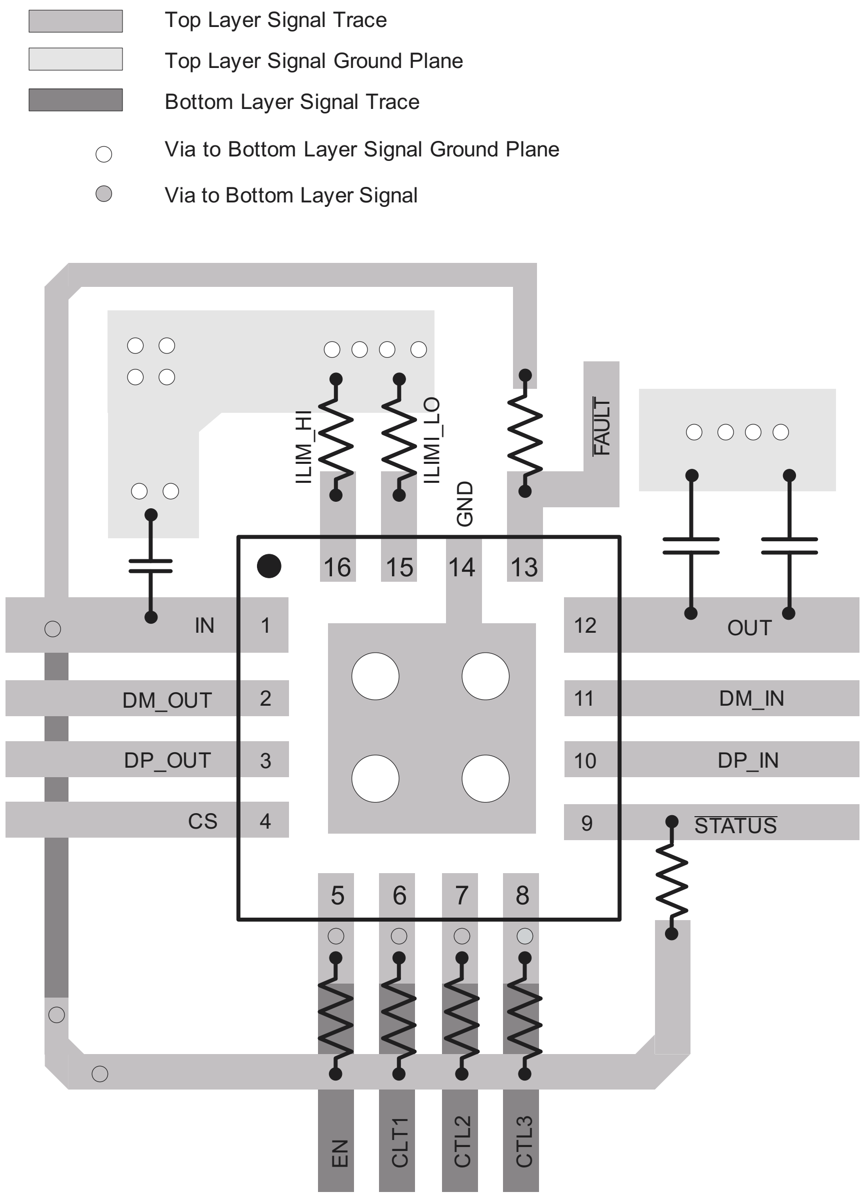


図 11-1. TPS2549-Q1 Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

High Speed USB Platform Design Guidelines, Intel

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2549IRTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2549Q	Samples
TPS2549IRTETQ1	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2549Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

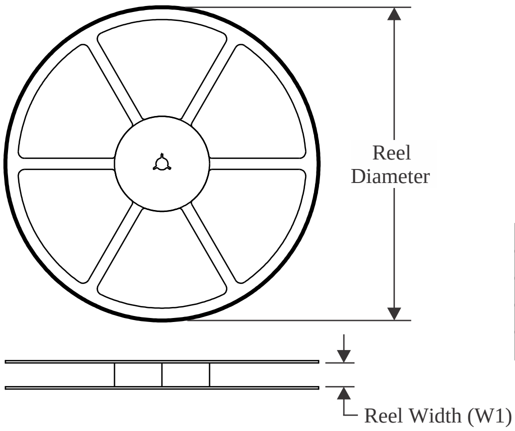
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

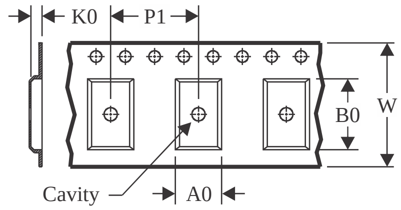
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

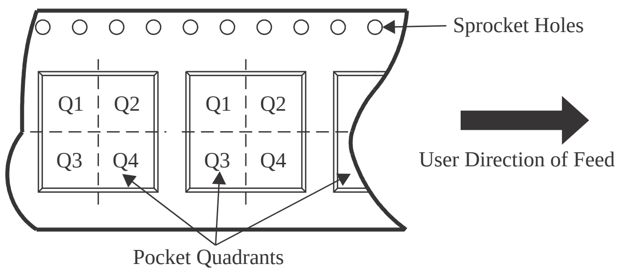


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

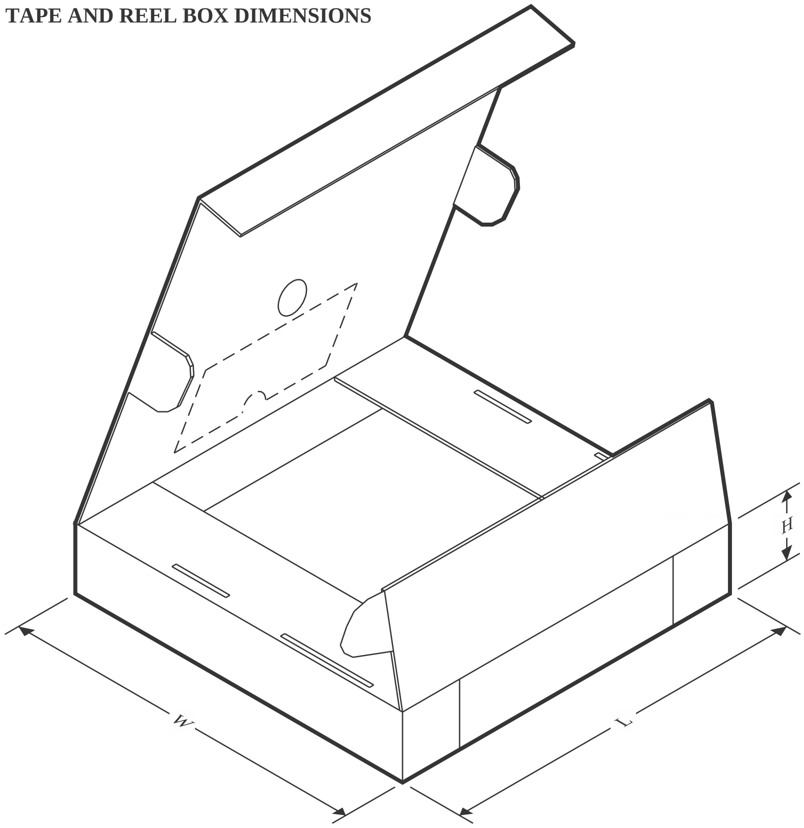
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2549IRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2549IRTETQ1	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2549IRTERQ1	WQFN	RTE	16	3000	346.0	346.0	33.0
TPS2549IRTETQ1	WQFN	RTE	16	250	210.0	185.0	35.0

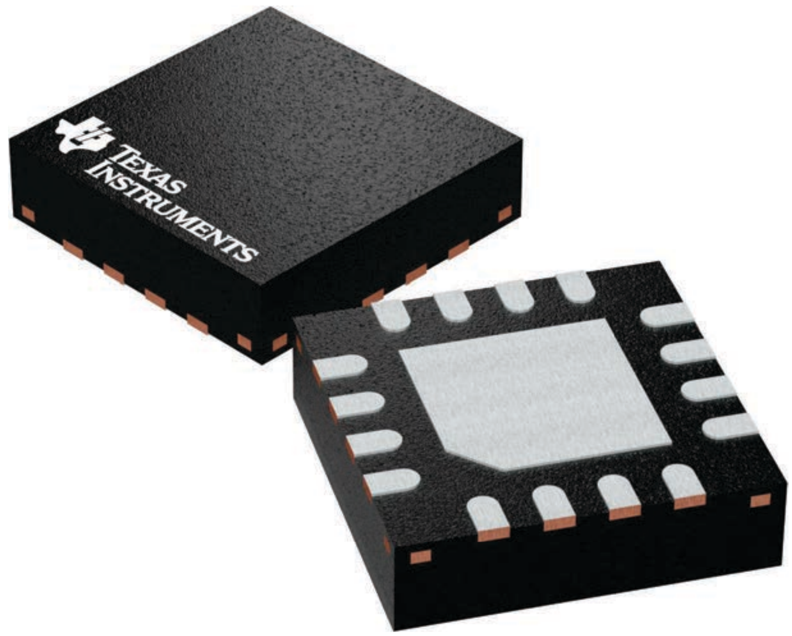
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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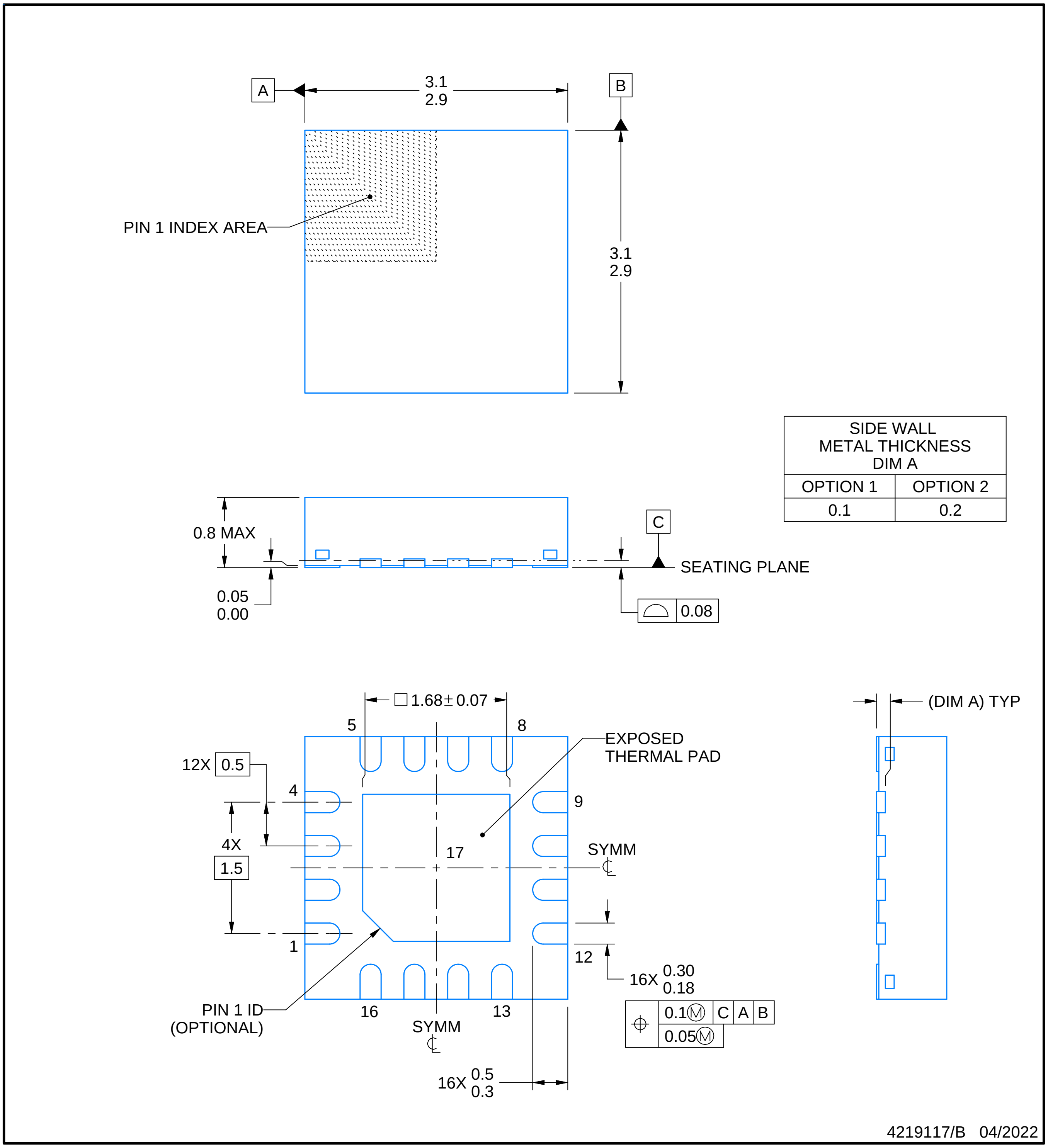
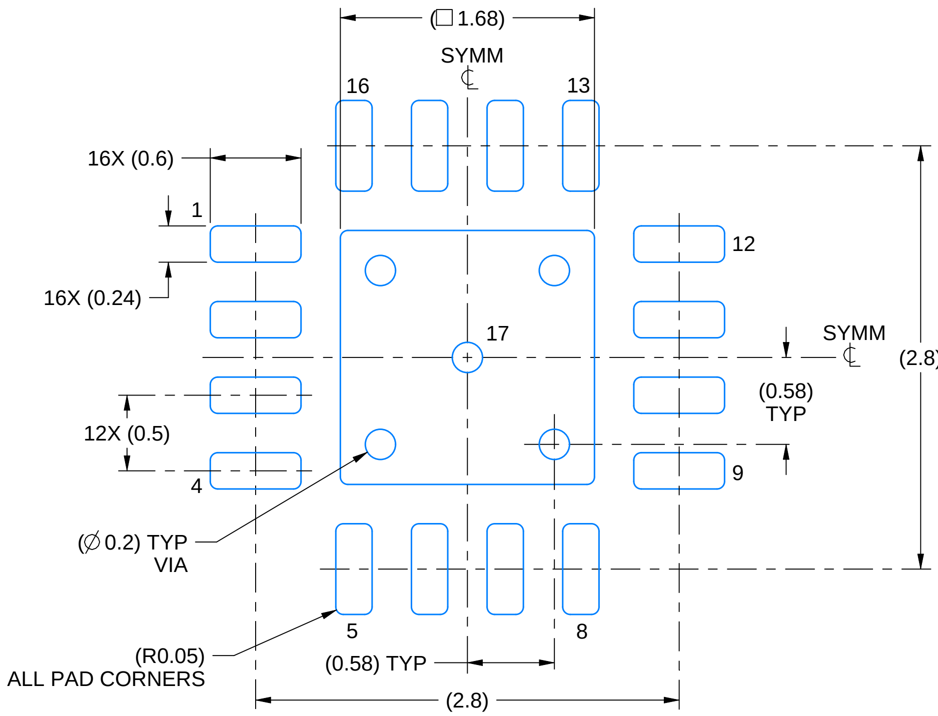
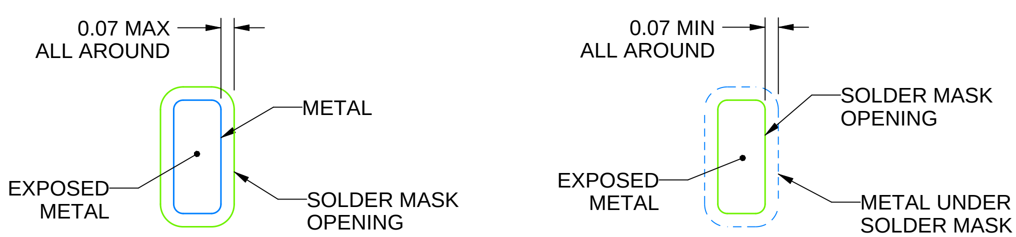


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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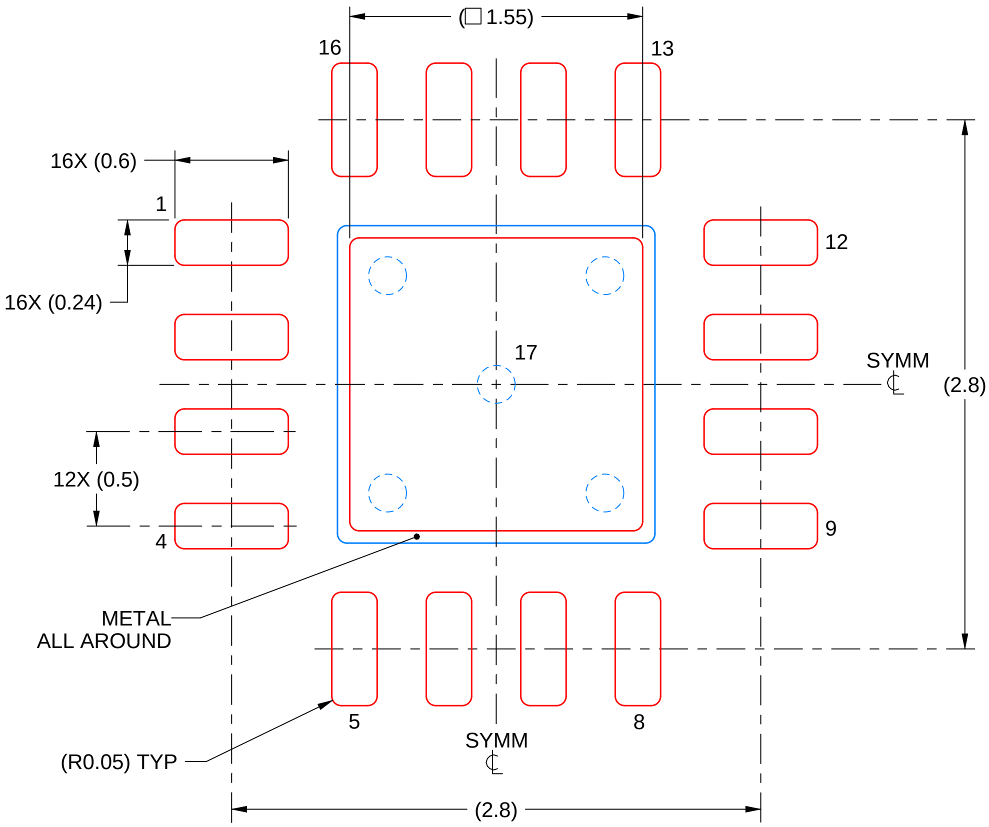
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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