

# TPS25820、TPS25821 USB Type-C™ 1.5Aソース・コントローラおよび電源スイッチ

## 1 特長

- USB Type-C™リリース1.3準拠のソース・コントローラ
- CCライン上のSTD/1.5A電流能力のアダプティブメント
- コネクタの取り付け/取り外し検出
- スーパー・スピードの極性判定
- $V_{BUS}$ と $V_{CONN}$  (TPS25820)の印加および放電、内部で固定された電流制限付き
- Type-Cコネクタに何も接続されていないとき、動作電流 $1.0\mu\text{A}$  (標準値)
- $64\text{m}\Omega$  (標準値)のハイサイドOUT MOSFET
- USBの電流制限要件に適合
  - $1.7\text{A}$ 、 $\pm 7\%$ 精度のOUT電流制限
  - 高速な過電流応答:  $1.5\mu\text{s}$  (標準値)
- CC1およびCC2の、 $\pm 8\text{kV}$ 接触放電および $\pm 15\text{kV}$ 空中放電ESD定格(IEC 61000-4-2)
- IEC/UL 認定
  - US-33101-UL: IEC 60950-1:2005、AMD1:2009、AMD2:2013
  - US-33102-UL: IEC 62368-1:2014

## 2 アプリケーション

- USB 2.0または3.x Type-Cのホストおよびハブ・ポート
- ノート/デスクトップPCおよびタブレット
- LCDモニタ/ドッキング・ステーションおよび充電クレードル
- Type-C USB壁面充電器、パワーバンク、CLA
- セットトップ・ボックスおよびオーディオ/ビデオ・システム

## 3 概要

TPS25820/21はUSB Type-Cソース・コントローラで、1.5A定格のUSB電源スイッチが内蔵されています。TPS25820/21は、Type-C構成チャネル(CC)ラインをモニタして、USBシンクの取り付けを検出します。シンクが取り付けられた場合、TPS25820/21は $V_{BUS}$ に電力を印加し、パススルーのCCラインを経由して、選択可能な $V_{BUS}$ 電流ソーシング能力をシンクに通知します。シンクにE-Markedケーブルが接続されると、TPS25820は $V_{CONN}$ 電力もケーブルの $V_{CONN}$ ピンに印加します。TPS25821は $V_{CONN}$ 電力を印加せず、USB 2.0やデータなしの充電用実装など、 $V_{CONN}$ が必要ない機能向けです。

TPS25820/21は、何も接続されていないとき $1.0\mu\text{A}$  (標準値)を消費します。 $\overline{\text{FAULT}}$ 出力は、スイッチが過電流または過熱状態のときに信号を発します。 $\overline{\text{SINK}}$ 出力は、シンクが接続されているときに信号を出力し、 $\overline{\text{POL}}$ 出力はケーブルのスーパー・スピード・ラインの極性を示します。

### 製品情報<sup>(1)</sup>

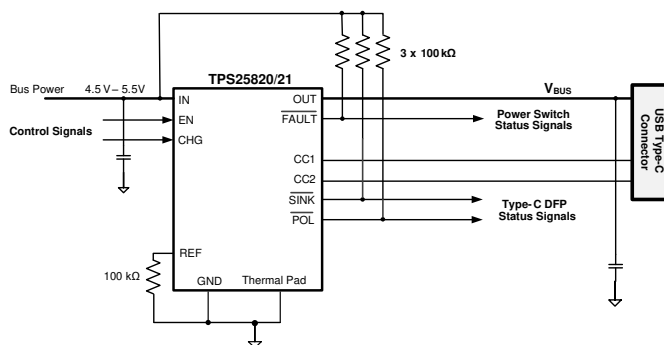
型番	パッケージ	本体サイズ(公称)
TPS25820	WSON (12)	3.00mm×2.00mm
TPS25821	WSON (12)	3.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### デバイスの比較

型番	$V_{CONN}$
TPS25820	あり
TPS25821	なし

### 概略回路図



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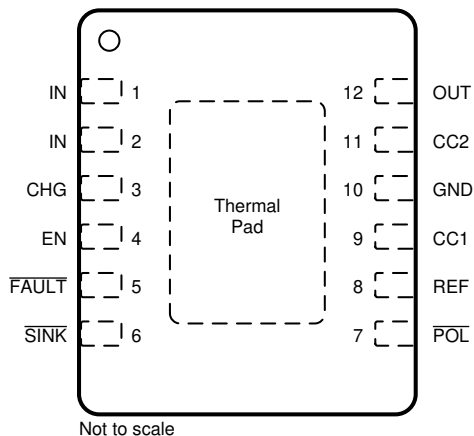
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## 4 改訂履歴

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## 5 Pin Configuration and Functions

**DSS Package  
12-Pin WSON  
Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
IN	1, 2	I	Device input supply. $V_{BUS}$ internal power switch input supply. $V_{CONN}$ internal power switch input supply for the TPS25820.
CHG	3	I	Charge logic input to select between standard USB or 1.5-A Type-C current sourcing ability.
EN	4	I	Logic input to turn the device on and off.
$\overline{\text{FAULT}}$	5	O	Open-drain logic output that asserts when the device is in overtemperature and/or $V_{BUS}$ is in current limit condition.
$\overline{\text{SINK}}$	6	O	Open-drain logic output that asserts when a Type-C Sink is identified on the CC lines.
$\overline{\text{POL}}$	7	O	Open-drain logic output that signals which Type-C CC pin is connected to the cable CC line. This gives the information needed to mux the super speed lines. Asserted when the CC2 pin is connected to the cable CC line.
REF	8	I	Analog input used to make a current reference. Connect a 0.5%, 100-ppm, 100-k $\Omega$ resistor between this pin and GND.
CC1	9	I/O	Analog input/output that connects to the Type-C receptacle CC1 pin.
GND	10	–	Ground
CC2	11	I/O	Analog input/output that connects to the Type-C receptacle CC2 pin.
OUT	12	O	$V_{BUS}$ power switch output.
Thermal Pad	–	–	Thermal pad on bottom of package.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltages are respect to GND (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage, V	IN, EN, CHG, REF, OUT, $\overline{\text{FAULT}}$ , CC1, CC2, $\overline{\text{SINK}}$ , $\overline{\text{POL}}$	-0.3	6	V
Pin positive source current, $I_{\text{SRC}}$	OUT, REF, CC1, CC2		Internally limited	A
Pin positive sink current, $I_{\text{SNK}}$	OUT (while applying $V_{\text{BUS}}$ )		2.5	A
	CC1, CC2 (while TPS25820 applying $V_{\text{CONN}}$ )		1	A
	$\overline{\text{FAULT}}$ , $\overline{\text{SINK}}$ , $\overline{\text{POL}}$		Internally limited	mA
Operating junction temperature, $T_{\text{J}}$		-40	180	°C
Storage temperature range, $T_{\text{stg}}$		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{\text{(ESD)}}$ <sup>(1)</sup> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(2)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±500	
	IEC61000-4-2 contact discharge, CC1 and CC2 <sup>(4)</sup>	±8000	
	IEC61000-4-2 air-gap discharge, CC1 and CC2 <sup>(4)</sup>	±15000	

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.

(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(4) Surges per IEC61000-4-2, 1999 applied between CC1/CC2 and output ground of the TPS25820EVM-835.

### 6.3 Recommended Operating Conditions

Voltages are with respect to GND (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
$V_{\text{I}}$	Supply voltage			4.5	5.5	V
$V_{\text{I}}$	Input voltage			0	5.5	V
$V_{\text{IH}}$	High-level input voltage			2		V
$V_{\text{IL}}$	Low-level voltage				0.8	V
$V_{\text{PU}}$	Pull-up voltage			0	5.5	V
$I_{\text{SRC}}$	Positive source current				1.5	A
		CC1 or CC2 when supplying $V_{\text{CONN}}$			250	mA
$I_{\text{SNK}}$	Positive sink current (100 ms moving average)	$\overline{\text{SINK}}$ , $\overline{\text{POL}}$			5	mA
		$\overline{\text{FAULT}}$			10	
$I_{\text{SNK\_PULSE}}$	Positive repetitive pulse sink current				Internally Limited	mA
$T_{\text{J}}$	Operating junction temperature			-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS25820, TPS25821	UNIT
		DSS (WSON)	
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	57.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	53.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	24.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	24.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

–40°C ≤ T<sub>J</sub> ≤ 125°C, 4.5 V ≤ V<sub>IN</sub> ≤ 5.5 V, V<sub>EN</sub> = V<sub>CHG</sub> = V<sub>IN</sub>, R<sub>REF</sub> = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I<sub>OUT</sub> and I<sub>OS</sub> defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUT - POWER SWITCH</b>						
R <sub>DS(on)</sub>	On resistance <sup>(1)</sup>	T <sub>J</sub> = 25°C, I <sub>OUT</sub> = 1.5 A		64	70	mΩ
		–40°C ≤ T <sub>J</sub> ≤ 85°C, I <sub>OUT</sub> = 1.5 A		64	85	
		–40°C ≤ T <sub>J</sub> ≤ 125°C, I <sub>OUT</sub> = 1.5 A		64	98	
I <sub>REV</sub>	OUT to IN reverse leakage current	V <sub>OUT</sub> = 5.5 V, 0 ≤ V <sub>IN</sub> ≤ 5.5 V, V <sub>EN</sub> = 0 V, –40°C ≤ T <sub>J</sub> ≤ 85°C, measure I <sub>IN</sub>		0	3	μA
<b>OUT - CURRENT LIMIT</b>						
I <sub>OS</sub>	Short circuit current limit <sup>(1)</sup>		1.6	1.72	1.84	A
		R <sub>REF</sub> = 10 Ω			4.0	
<b>OUT - DISCHARGE</b>						
	Discharge resistance	V <sub>OUT</sub> = 4 V	400	500	600	Ω
	Bleed discharge resistance	V <sub>OUT</sub> = 4 V, No Sink termination on CC lines, time > t <sub>w_OUT_DCHG</sub>	90	150	250	kΩ
V <sub>TH</sub>	Rising threshold for not discharged				800	mV
<b>REF</b>						
I <sub>OS</sub>	Short circuit current	R <sub>REF</sub> = 10 Ω	9.5		17.5	μA
V <sub>O</sub>	Output voltage		0.78	0.8	0.82	V
<b>FAULT</b>						
V <sub>OL</sub>	Output low voltage	I <sub>FAULT</sub> = 1 mA			250	mV
I <sub>OFF</sub>	Off-state leakage	V <sub>FAULT</sub> = 5.5 V			1	μA
<b>CC1/CC2 - V<sub>CONN</sub> POWER SWITCH (TPS25820)</b>						
R <sub>DS(on)</sub>	On resistance	T <sub>J</sub> = 25°C, I <sub>CCx</sub> = 250 mA		480	530	mΩ
		–40°C ≤ T <sub>J</sub> ≤ 85°C, I <sub>CCx</sub> = 250 mA		480	645	
		–40°C ≤ T <sub>J</sub> ≤ 125°C, I <sub>CCx</sub> = 250 mA		480	755	
<b>CC1/CC2 - V<sub>CONN</sub> POWER SWITCH - CURRENT LIMIT (TPS25820)</b>						
I <sub>OS</sub>	Short circuit current limit <sup>(1)</sup>		315	370	425	mA
		R <sub>REF</sub> = 10 Ω			1000	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

**Electrical Characteristics (continued)**

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $4.5\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $V_{\text{EN}} = V_{\text{CHG}} = V_{\text{IN}}$ ,  $R_{\text{REF}} = 100\text{ k}\Omega$ . Typical values are at  $25^{\circ}\text{C}$ . All voltages are with respect to GND.  $I_{\text{OUT}}$  and  $I_{\text{OS}}$  defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CC1/CC2 – CONNECT MANAGEMENT</b>						
$I_{\text{SRC}}$	Sourcing current	$V_{\text{CHG}} = 0\text{ V}$ , $0\text{ V} \leq V_{\text{CCx}} \leq 1.5\text{ V}$ , after $V_{\text{SINK}} = 0\text{ V}$	73	80	85	$\mu\text{A}$
		$0\text{ V} \leq V_{\text{CCx}} \leq 1.5\text{ V}$ , after $V_{\text{SINK}} = 0\text{ V}$	168	180	190	
		$V_{\text{CHG}} = 0\text{ V}$ or $V_{\text{IN}}$ , $0\text{ V} \leq V_{\text{CCx}} \leq 1.5\text{ V}$ , before $V_{\text{SINK}} = 0\text{ V}$	64	80	96	
$I_{\text{REV}}$	Reverse leakage current	CCx is the CC pin under test, CCy is the other CC pin. $V_{\text{CCx}} = 5.5\text{ V}$ , CCy floating, $V_{\text{EN}} = 0\text{ V}$ or $0\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ , $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ , $I_{\text{REV}}$ is current into CCx pin.		0	5	$\mu\text{A}$
		CCx is the CC pin under test, CCy is the other CC pin. $V_{\text{CCx}} = 5.5\text{ V}$ , CCy = $0\text{ V}$ , $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ , $I_{\text{REV}}$ is current into CCx pin.		5	10	
<b>CC1/CC2 – CONNECT MANAGEMENT – <math>V_{\text{CONN}}</math> DISCHARGE MODE</b>						
	Discharge resistance (TPS25820)	CC pin that was providing $V_{\text{CONN}}$ before detach: $V_{\text{CCX}} = 4\text{ V}$	400	500	600	$\Omega$
$V_{\text{TH}}$	Falling threshold for discharged (TPS25820)	CC pin that was providing $V_{\text{CONN}}$ before detach	570	600	630	mV
	Discharged threshold hysteresis (TPS25820)			100		mV
<b>SINK, POL</b>						
$V_{\text{OL}}$	Output low voltage	$I_{\text{SNK\_PIN}} = 1\text{ mA}$			250	mV
$I_{\text{OFF}}$	Off-state leakage	$V_{\text{PIN}} = 5.5\text{ V}$			1	$\mu\text{A}$
<b>EN, CHG - LOGIC INPUTS</b>						
$V_{\text{TH}}$	Rising threshold voltage for output logic change			1.45	1.8	V
$V_{\text{TH}}$	Falling threshold voltage for output logic change		1.00	1.35		V
	Hysteresis <sup>(2)</sup>			100		mV
$I_{\text{IN}}$	Input current	$V_{\text{PIN}} = 0\text{ V}$ or $5.5\text{ V}$	-0.5		0.5	$\mu\text{A}$
<b>OVER TEMPERATURE SHUT DOWN</b>						
$T_{\text{TH\_OTSD2}}$	Rising threshold temperature for device shutdown		155			$^{\circ}\text{C}$
	Hysteresis <sup>(2)</sup>			20		$^{\circ}\text{C}$
$T_{\text{TH\_OTSD1}}$	Rising threshold temperature for OUT/ $V_{\text{CONN}}$ switch shutdown in current limit		135			$^{\circ}\text{C}$
	Hysteresis <sup>(2)</sup>			20		$^{\circ}\text{C}$
<b>IN</b>						
$V_{\text{TH}}$	Rising threshold voltage for not UVLO		3.9	4.1	4.3	V
	Hysteresis <sup>(2)</sup>			100		mV

(2) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

## Electrical Characteristics (continued)

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $4.5\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $V_{\text{EN}} = V_{\text{CHG}} = V_{\text{IN}}$ ,  $R_{\text{REF}} = 100\text{ k}\Omega$ . Typical values are at  $25^{\circ}\text{C}$ . All voltages are with respect to GND.  $I_{\text{OUT}}$  and  $I_{\text{OS}}$  defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{I}}$	Disabled supply current	$V_{\text{EN}} = 0\text{ V}$ , $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$			1	$\mu\text{A}$
	Enabled supply current with CC lines open	$-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$		1	4	
	Enabled supply current with dangling Ra cable attached			150	195	
	Enabled supply current with Sink attached via cable that is electronically marked (includes IN current that provides the CC output current to the sink Rd resistor)	$V_{\text{CHG}} = 0\text{ V}$		232	275	
				332	380	
Enabled supply current with Sink attached via cable that is not electronically marked (includes IN current that provides the CC output current to the sink Rd resistor)	$V_{\text{CHG}} = 0\text{ V}$		210	250		
			310	355		

## 6.6 Switching Characteristics

$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ,  $4.5\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $V_{\text{EN}} = V_{\text{CHG}} = V_{\text{IN}}$ ,  $R_{\text{REF}} = 100\text{ k}\Omega$ . Typical values are at  $25^{\circ}\text{C}$ . All voltages are with respect to GND.  $I_{\text{OUT}}$  and  $I_{\text{OS}}$  defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUT - POWER SWITCH</b>						
$t_r$	Output voltage rise time	$V_{\text{IN}} = 5\text{ V}$ , $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$ (measure between 10% and 90% of final value)	0.5	0.8	1.2	ms
$t_f$	Output voltage fall time		0.2	0.3	0.4	ms
$t_{\text{on}}$	Output voltage turn-on time	$V_{\text{IN}} = 5\text{ V}$ , $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$	2.1	3.2	4.5	ms
$t_{\text{off}}$	Output voltage turn-off time		0.8	1.3	1.9	ms
$t_{w\_OUT\_DCHG}$	$R_{\text{DCHG}}$ application time at OUT turn off	$V_{\text{OUT}} = 1\text{ V}$ , time $I_{\text{SNK\_OUT}} > 1\text{ mA}$ after Sink termination removed from CC lines	169	262	361	ms
<b>OUT - CURRENT LIMIT</b>						
$t_{\text{IOS}}$	Current limit response time to short circuit	$V_{\text{IN}} - V_{\text{OUT}} = 1\text{ V}$ , $R_L = 10\text{ m}\Omega$ (see <a href="#">1</a> )		1.5	4	$\mu\text{s}$
<b>FAULT</b>						
$t_{\text{DEGA}}$	Asserting deglitch due to overcurrent		5.6	8.2	10.6	ms
$t_{\text{DEGA}}$	Asserting deglitch due to overtemperature in current limit			0		ms
$t_{\text{DEGD}}$	De-asserting deglitch		5.6	8.2	10.6	ms
<b>CC1/CC2 - <math>V_{\text{CONN}}</math> POWER SWITCH (TPS25820)</b>						
$t_r$	Output voltage rise time	$V_{\text{IN2}} = 5\text{ V}$ , $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$	0.13	0.22	0.3	ms
$t_f$	Output voltage fall time		0.18	0.22	0.26	ms
$t_{\text{on}}$	Output voltage turn-on time	$V_{\text{IN2}} = 5\text{ V}$ , $C_L = 1\text{ }\mu\text{F}$ , $R_L = 100\text{ }\Omega$	1.4	2.2	3.2	ms
$t_{\text{off}}$	Output voltage turn-off time		0.25	0.33	0.4	ms
	Minimum $V_{\text{CONN}}$ discharge time	TPS25820	42	65	90	ms
<b>CC1/CC2 - <math>V_{\text{CONN}}</math> POWER SWITCH - CURRENT LIMIT (TPS25820)</b>						
$t_{\text{res}}$	Current limit response time to short circuit	$V_{\text{IN}} - V_{\text{CCX}} = 1\text{ V}$ , $R = 10\text{ m}\Omega$ (see <a href="#">1</a> )		1	4	$\mu\text{s}$
<b>SINK, POL</b>						
$t_{\text{DEGA}}$	Asserting deglitch		100	150	200	ms
$t_{\text{DEGD}}$	De-asserting deglitch		7.9	12.5	17.7	ms

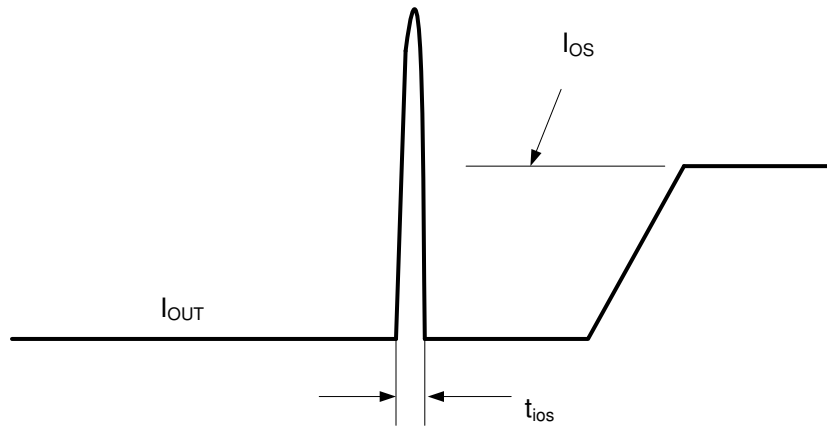
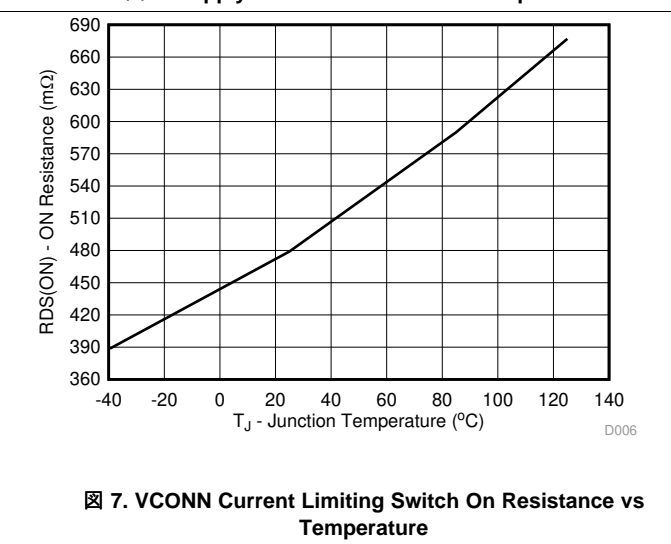
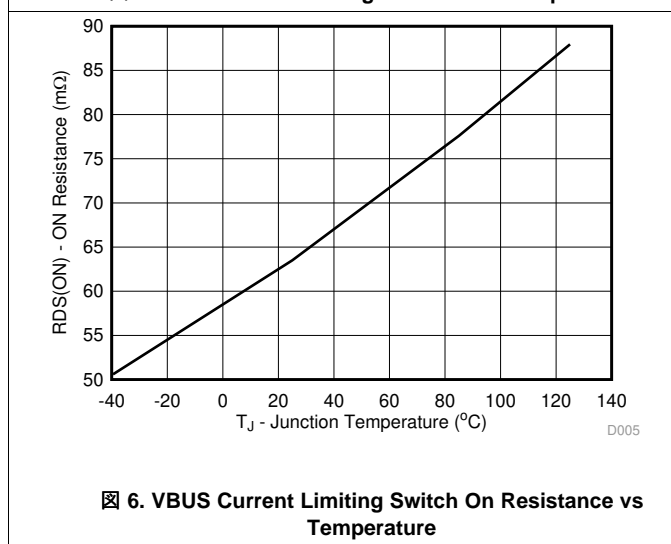
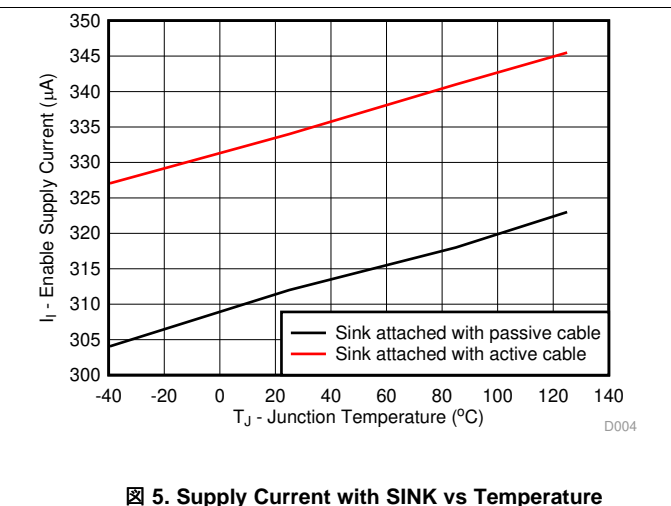
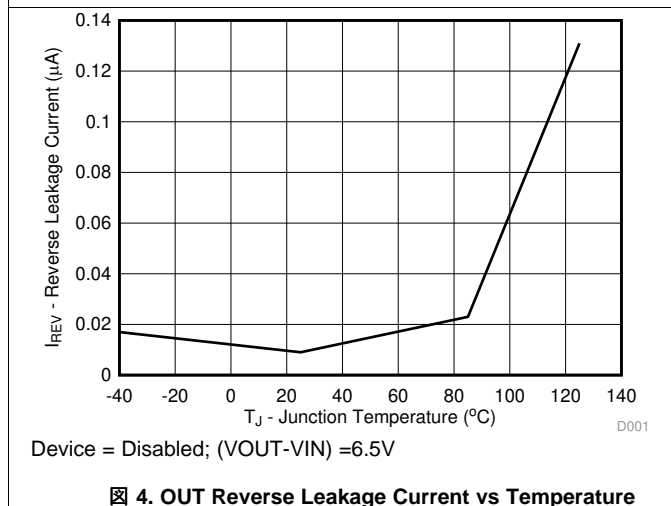
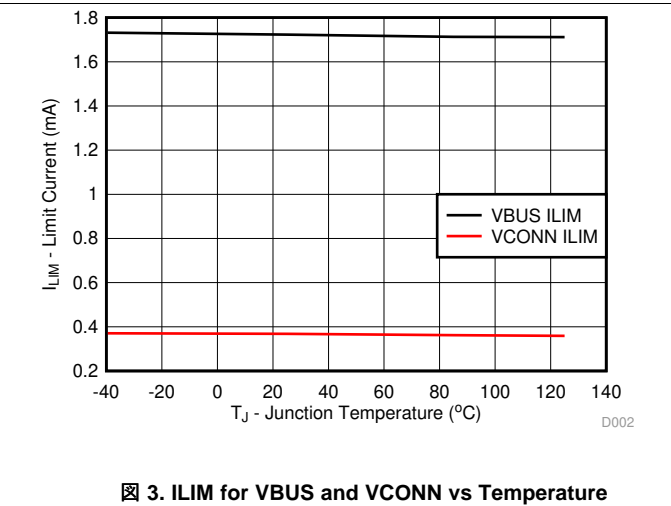
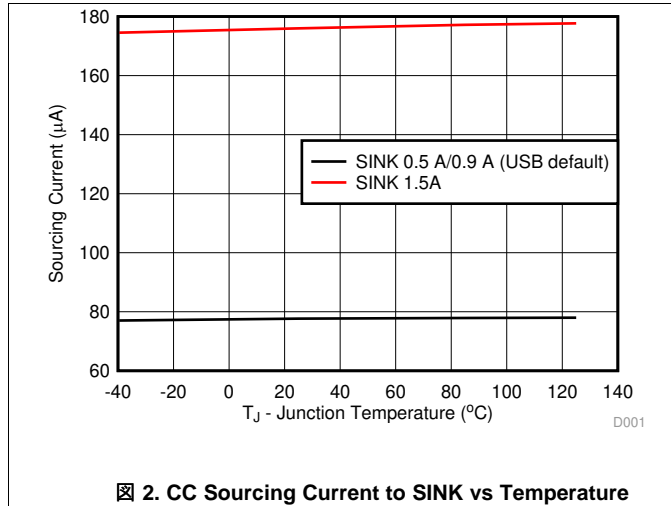


图 1. Output Short Circuit Parameter Diagram



## 6.7 Typical Characteristics



## 7 Detailed Description

### 7.1 Overview

The TPS25820 and TPS25821 devices are highly integrated USB Type-C source controllers with built-in power switches developed for the USB Type-C connector and cable. The TPS25820 supports VCONN, while the TPS25821 does not. The devices provide all of the functionality needed to support a USB Type-C DFP in a system where USB power delivery (PD) source capabilities (for example,  $V_{BUS} > 5\text{ V}$ ) are not implemented. The devices are designed to be compliant to the USB Type-C specification, release 1.3 which added new requirements to discharge VCONN.

#### 7.1.1 USB Type C Basic

For a detailed description of the Type-C spec refer to the USB-IF website to download the latest released version. Some of the basic concepts of the Type-C spec that pertains to understanding the operation of the TPS25820/21 (a Downward Facing Port, DFP device) are described as follows.

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacles since the Type-C cable is plug-able in either direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB Type-C ports operate in one of below three data modes:

- Host mode: the port can only be host (also provider of power)
- Device mode: the port can only be device (also consumer of power)
- Dual-Role mode: the port can be either host or device

Port types:

- DFP (Downstream Facing Port): Host, specifically associated with flow of data (Host or Hub) in a USB link
- Source: Port that asserts  $R_p$  (pull-up resistor) on CC pin and provides power on VBUS when attached to a Sink (device). At power-up a DFP is a source.
- UFP (Upstream Facing Port): Device, specifically associated with flow of data (device) in a USB link
- Sink: Port that asserts  $R_d$  (pull-down) on CC pin and consumes power from VBUS when attached. At power-up a UFP is a sink
- DRP (Dual-Role Port): Host or Device

Valid Source-to-Sink connections:

- [表 1](#) describes valid Source-to-Sink connections
- Source to Source or Sink to Sink have no function

**表 1. Valid Source-to-Sink Connections**

POWER ROLES	SOURCE ONLY	SINK ONLY	DUAL ROLE POWER (DRP)
Source Only	Not allowed	Allowed	Allowed
Sink Only	Allowed	Not allowed	Allowed
Dual Role Power (DRP)	Allowed	Allowed	Allowed

#### 7.1.2 Configuration Channel

The function of the configuration channel is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally the Configuration Channel (CC) is used to serve the following purposes:

- Detect connect to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish Source and Sink roles between two connected ports
- Discover and configure power: USB Type-C current modes or USB Power Delivery
- Discovery and configure optional Alternate and Accessory modes

- Enhances flexibility and ease of use

Typical flow of DFP to UFP configuration is shown in 8:

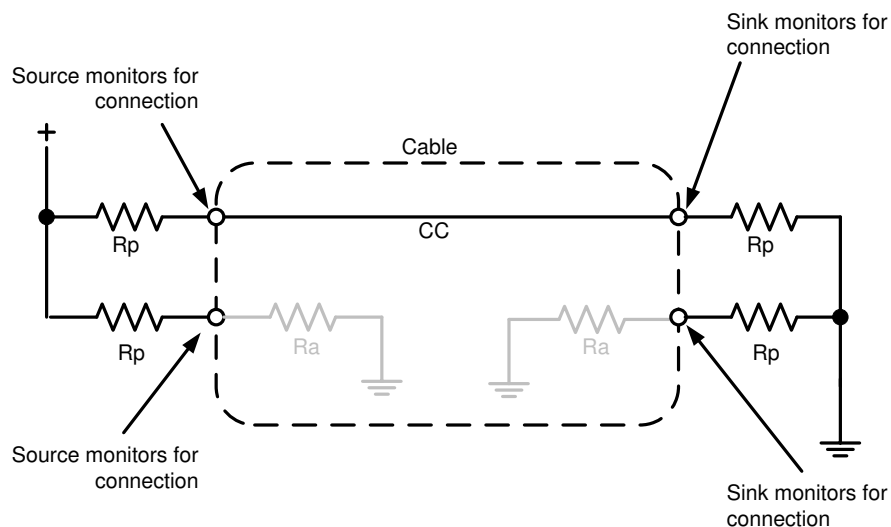


8. DFP to UFP Connect Flow

### 7.1.3 Detecting a Connection

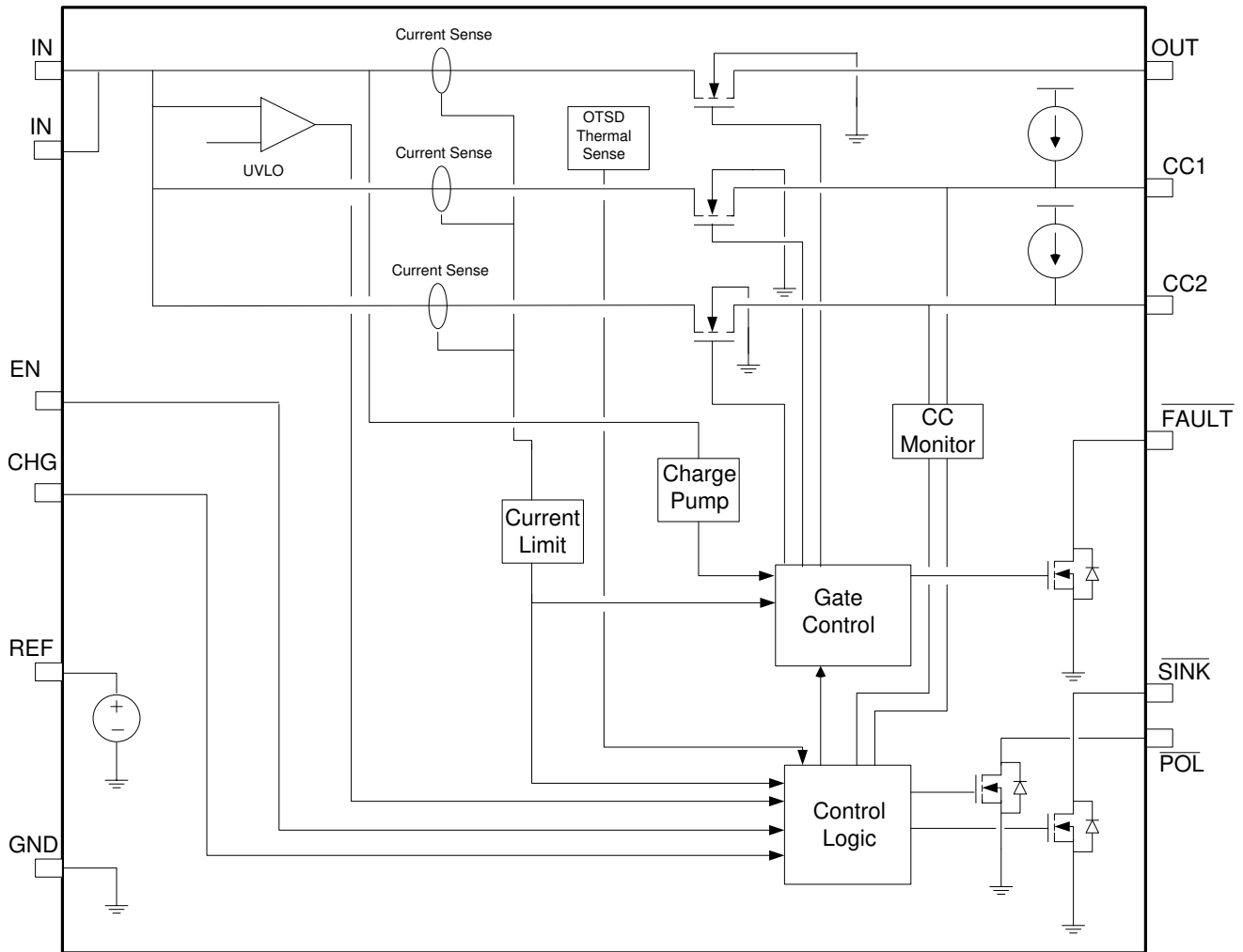
Sources and DRPs fulfill the role of detecting a valid connection over USB Type-C. 9 shows a Source to Sink connection made with Type-C cable. As shown in 9, the detection concept is based on being able to detect terminations in the product which has been attached. A pull-up and pull-down termination model is used. A pull-up termination can be replaced by a current source.

- In the Source-Sink connection the Source monitors both CC pins for a voltage lower than the unterminated voltage.
- A Sink advertises  $R_d$  on both its CC pins (CC1 and CC2).
- A powered cable advertises  $R_a$  on its  $V_{CONN}$  pin.



9. Source-Sink Connection Mechanism

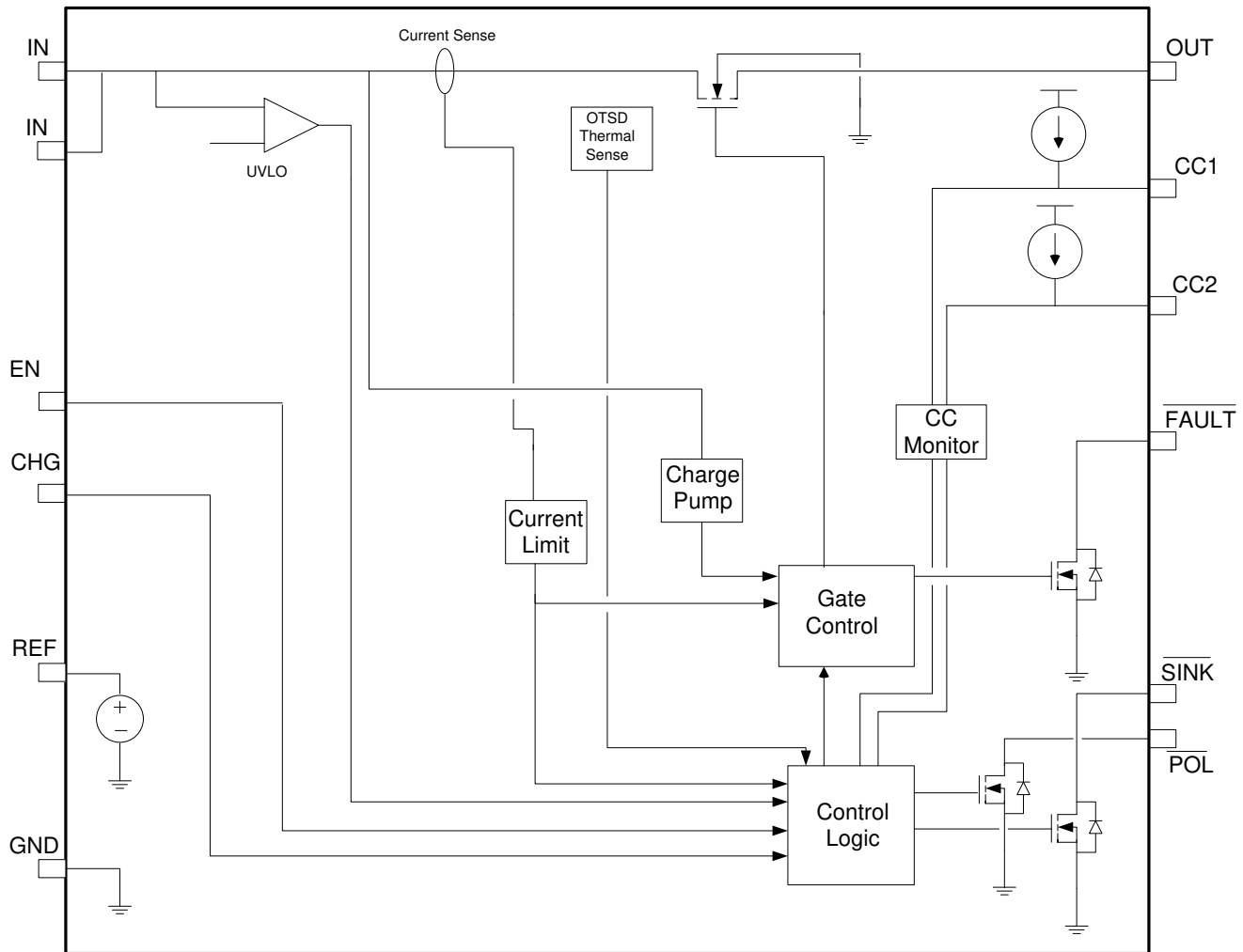
**7.2 Functional Block Diagrams**



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**Figure 10. TPS25820 Functional Block Diagram**

## Functional Block Diagrams (continued)



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图 11. TPS25821 Functional Block Diagram

### 7.3 Feature Description

Both the TPS25820 and TPS25821 are source (i.e. DFP) Type-C port controllers with integrated power switches for  $V_{BUS}$ . The TPS25820 also has integrated power switches for  $V_{CONN}$ . Refer to the functional block diagrams (图 10 and 图 11). The TPS25820/21 devices do not support BC1.2 charging modes, because it does not interact with USB D+ and D- data lines. However supporting DCP mode of BC1.2 can be easily accomplished in data-less ports like wall chargers and CLAs by simply tying a 100- $\Omega$  resistor between the D+ and D- pins of the Type-C connector.

The TPS25820 has a built-in  $V_{CONN}$  current limiting switch and can be used to implement USB 3.1 DFP, whereas the TPS25821 does not implement a  $V_{CONN}$  current limiting switch hence is used in the implementation in USB 2.0 DFP ports or as a USB source only port. Other than the  $V_{CONN}$  current limiting switch there are no other functional differences between the TPS25820 and TPS25821.

#### 7.3.1 Configuration Channel Pins CC1 and CC2

The TPS25820/21 devices have two pins, CC1 and CC2 that serve to detect an attachment to the port and resolve cable orientation. These pins are also used to establish the current broadcast to a valid sink and configure  $V_{CONN}$  (TPS25820 only).

## Feature Description (continued)

表 2 lists the TPS25820/21 response to various attachments to its port.

**表 2. Response to Attachments**

TPS25820/21 TYPE-C PORT	CC1	CC2	TPS25820/21 RESPONSE <sup>(1)</sup>			
			OUT	V <sub>CONN</sub> <sup>(2)</sup> On CC1 or CC2	POL	SINK
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z
Sink Connected	Rd	OPEN	IN	NO	Hi-Z	LOW
Sink Connected	OPEN	Rd	IN	NO	LOW	LOW
Powered Cable/No Sink Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z
Powered Cable/No Sink Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z
Powered Cable/Sink Connected	Rd	Ra	IN	CC2	Hi-Z	LOW
Powered Cable/Sink Connected	Ra	Rd	IN	CC1	LOW	LOW
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z

(1) POL and SINK are open drain outputs; pull high with 100 kΩ to IN when used. Tie to GND or leave open when not used.

(2) TPS25820 Only

### 7.3.2 Current Capability Advertisement and VBUS Overload Protection

The TPS25820/21 supports two Type-C current advertisements as defined by the USB Type-C standard. Current broadcast to a connected Sink is controlled by the CHG pin. For each broadcast level the device protects itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement by setting the current limit as shown in 表 3.

**表 3. USB Type-C Current Advertisement**

CHG	CC CAPABILITY BROADCAST	CURRENT LIMIT
0	STD (500 mA for USB 2.0 port)	1.67 A
0	STD (900 mA for USB 3.1 port)	1.67 A
1	1.5 A	1.67 A

Under overload conditions, the internal current-limit regulator limits the output current on the OUT pin as shown in the Electrical Characteristics table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by ( $I_{OS} \times R_{LOAD}$ ). Two possible overload conditions can occur. The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws  $I_{OUT} > I_{OS}$ ), or 2) input voltage is present and the TPS25820/21 is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS25820/21 ramps the output current to  $I_{OS}$ .

In either case the TPS25820/21 will limit the load current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in 图 16 where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

### 7.3.3 FAULT Response

The FAULT pin is an open drain output that asserts (active low) after a deglitch time ( $t_{DEGLA}$ ) when device OUT current exceeds its programmed value and/or overtemperature threshold is crossed. The FAULT signal remains asserted until the fault condition is removed for  $t_{DEGLD}$ . The TPS25820/21 are designed to eliminate false overcurrent fault reporting by using an internal deglitch circuit.

Connect FAULT with a 100-kΩ pull-up resistor to IN. FAULT can be left open or tied to GND when not used.

### 7.3.4 Thermal Shutdown

The device has two internal overtemperature shutdown thresholds,  $T_{TH\_OTSD1}$  and  $T_{TH\_OTSD2}$ , to protect the internal FET from damage and overall safety of the system. When the device temperature exceeds  $T_{TH\_OTSD1}$ , any switch in current limit (OUT switch or VCONN switch) is disabled. The device does auto-retry recovery by re-enabling the switch when die temperature decreases by 20°C. When  $T_{TH\_OTSD2}$  is exceeded all open drain outputs are left open and the device is disabled such that minimum power/heat is dissipated. The device does auto-retry recovery by attempting to power-up when die temperature decreases by 20°C.

### 7.3.5 REF

A 100-kΩ resistor is connected from this pin to GND. This pin sets the reference current required to bias the internal circuitry of the device. The overload current limit tolerance and CC currents depend upon the accuracy of this resistor. A ±0.5% low temp CO resistor, or better, yields the best current limit accuracy and overall device performance. If the CC capability broadcast will only be set to STD (CHG pulled low) then up to a ±10% resistor may be used as long as the additional error in the current limit is acceptable.

### 7.3.6 Plug Polarity Detection

Reversible Type-C plug orientation is reported by the  $\overline{POL}$  pin when a Sink is connected, however when no Sink is attached,  $\overline{POL}$  remains de-asserted irrespective of cable plug orientation. 表 2 describes the  $\overline{POL}$  state based on which device CC pin detects  $V_{Rd}$  from an attached Sink pull-down. In a typical USB 3.x DFP port, this pin controls a superspeed data MUX for proper data connectivity irrespective of plug orientation. See 图 20.

### 7.3.7 Sink Attachment Indicator

The attachment of a Type-C sink is reported by  $\overline{SINK}$ . See 表 2.

### 7.3.8 Device Enable Control

The logic enable pin controls the power switch and device supply current. The supply current is reduced to less than 1 μA when a logic low is present on EN. The EN pin provides a convenient way to turn on or turn off the device while it is powered. When this pin is pulled high, the device is turned on or enabled. When the device is disabled (EN pulled low), the internal FETs tied to IN are disconnected, all open drain outputs are left open (Hi-Z), and the CC1/CC2 monitor block is turned off. The EN pin should not be left floating.

### 7.3.9 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

## 7.4 Device Functional Modes

The TPS25820/21 is a Type-C controller with integrated power switch that supports all Type-C functions in a downstream facing port (DFP). It is also used to manage current advertisement and protection to a connected sink and active cable. The device starts its operation by monitoring the IN bus. When IN exceeds the undervoltage lockout threshold, the device samples the EN pin. A high level on this pin enables the device and normal operation begins. Having successfully completed its start-up sequence, the device now actively monitors its CC1 and CC2 pins for attachment to a sink. When a sink is detected on either the CC1 or CC2 pin the internal MOSFET starts to turn-on after the required de-bounce time is met. The internal MOSFET starts conducting and allows current to flow from IN to OUT. For the TPS25820 if Ra is detected on the other CC pin (not connected to sink), VCONN is applied to allow current to flow from IN to the CC pin connected to Ra. For a complete listing of various device operational modes refer to 表 2.

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS25820/21 are Type-C source controllers. The TPS25820 supports all Type-C DFP required functions to support a USB 3.x port and the TPS25821 supports all required functions for a USB 2.0 DFP. The TPS25820/21 only applies power to  $V_{BUS}$  when it detects a sink is attached and removes power when it detects the sink is detached. The device exposes its identity via its CC pin advertising its current capability based on the CHG pin setting. The TPS25820/21 also limits its advertised current internally and provides robust protection against faults on the system  $V_{BUS}$  power rail.

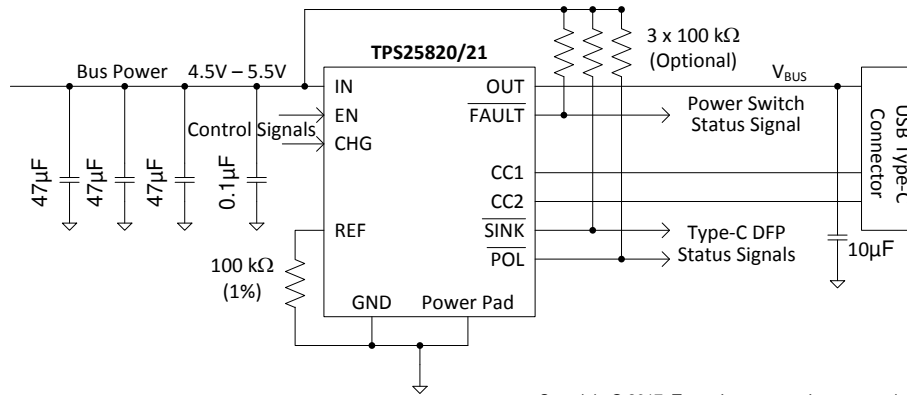
After a connection is established by the TPS25820/21, the TPS25820/21 device is capable of providing  $V_{CONN}$  to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable.  $V_{CONN}$  is internally current limited. The TPS25820/21 do not support Type-C optional accessory modes (Ra/Ra and Rd/Rd in 表 2).

The following design procedure can be used to implement a full featured Type-C source.

### 8.2 Typical Applications

#### 8.2.1 Type-C Source Port Implementation without BC 1.2 Support

图 12 shows a minimal Type-C source implementation capable of supporting 5-V and 1.5-A charging.



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图 12. Type-C Source Port Implementation without BC 1.2 Support

#### 8.2.1.1 Design Requirements

##### 8.2.1.1.1 Input and Output Capacitance Considerations

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. For all applications, a 0.1- $\mu$ F or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits, including those of the TPS25820/21 device, have the potential for input voltage overshoots and output voltage undershoots. Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the IN pin is high-impedance (before OUT turn-on, i.e. not connected to a Type-C sink device). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of



## Typical Applications (continued)

output short-circuit current when the device turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the output is shorted. Applications with large input inductance (for instance, connecting the evaluation board to the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute maximum voltage of the device.

The fast current-limit speed of the TPS25820/21 device to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1  $\mu\text{F}$  to 22  $\mu\text{F}$  adjacent to the input aids in both response time and limiting the transient seen on the input power bus. Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the device has abruptly reduced the OUT current. Energy stored in the inductance drives the OUT voltage down, and potentially negative, as it discharges. An application with large output inductance (such as from a cable) benefits from the use of a high-value output capacitor to control voltage undershoot.

Since the source is considered cold socketed when not attached to a sink, the output capacitance should be placed at the IN pin rather than the OUT pin, which has been commonly used in USB Type-A ports. A 120- $\mu\text{F}$  capacitance is recommended in this situation. It is also recommended to a ceramic capacitor less than 10  $\mu\text{F}$  on the OUT pin for better voltage bypass and compliance to Type-C spec.

### 8.2.1.1.2 System Level ESD Protection

System-level ESD (per EN61000-4-2) may occur as the result of a cable being plugged in, or a user touching the USB receptacle or cable plug exposed pins. The recommended capacitor on the OUT pin helps reduce the severity of ESD hit on the VBUS path thereby protecting the OUT pin of device. The device has ESD protection built into the CC1 and CC2 pins so that no external protection is necessary as long as proper trace layout guidelines are practiced. Refer to the Layout Guidelines section for external component placement and routing recommendations.

### 8.2.1.2 Detailed Design Procedure

Design considerations are listed below:

- Place at least 120  $\mu\text{F}$  of bypass capacitance close to the IN pins versus OUT as Type C is a cold socket connector.
- A <10- $\mu\text{F}$  bypass capacitor is recommended placed near Type-C receptacle  $V_{\text{BUS}}$  pin to handle load transients.
- Depending on the max current level advertisement supported by the Type-C port in the system, set CHG levels accordingly.
- EN and CHG pins can be tied directly to GND or IN without a pull-up resistor.
  - CHG can also be dynamically controlled by a  $\mu\text{C}$  to change the current advertisement level to the sink.
- When an open drain output of the TPS25820 is not used, it can be left as NC or tied to GND or when used, pulled up to IN supply via a 100-k $\Omega$  resistor.
- Connect a 0.5% 100-k $\Omega$  resistor between the REF and GND pins placing it close to the device pin and isolated from switching noise on the board.

Typical Applications (continued)

8.2.1.3 Application Curves

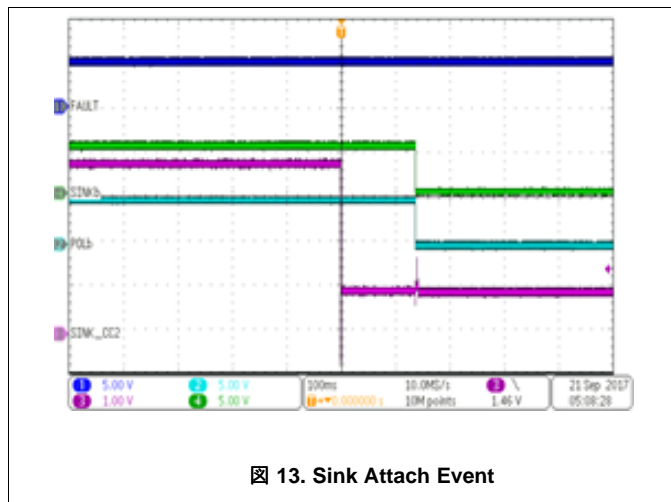


Figure 13. Sink Attach Event

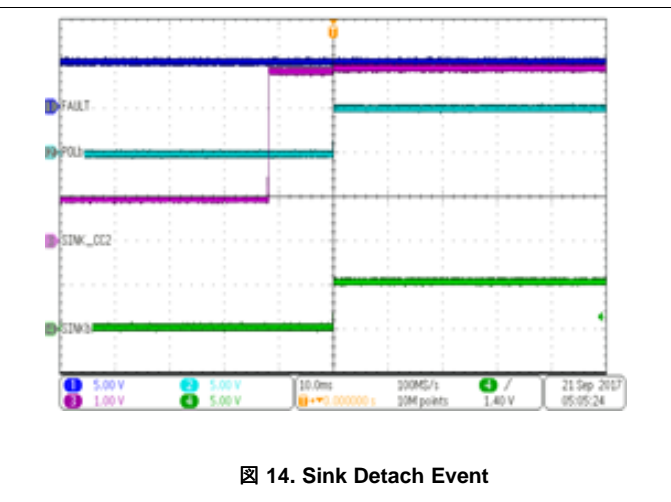
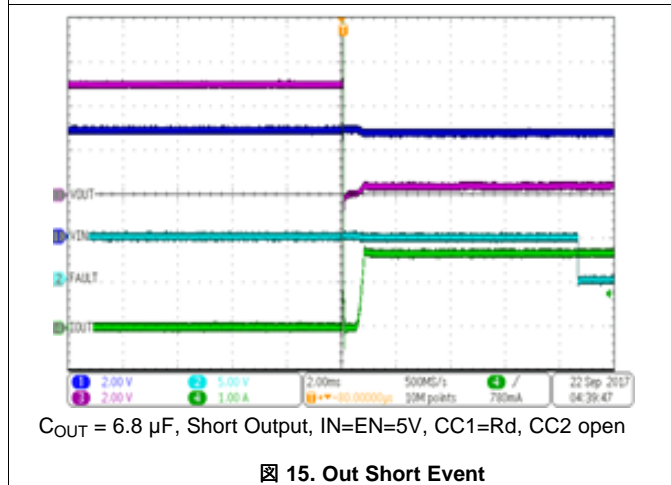


Figure 14. Sink Detach Event



$C_{OUT} = 6.8 \mu\text{F}$ , Short Output,  $I_N = I_{EN} = 5\text{V}$ ,  $CC1 = R_d$ ,  $CC2$  open

Figure 15. Out Short Event

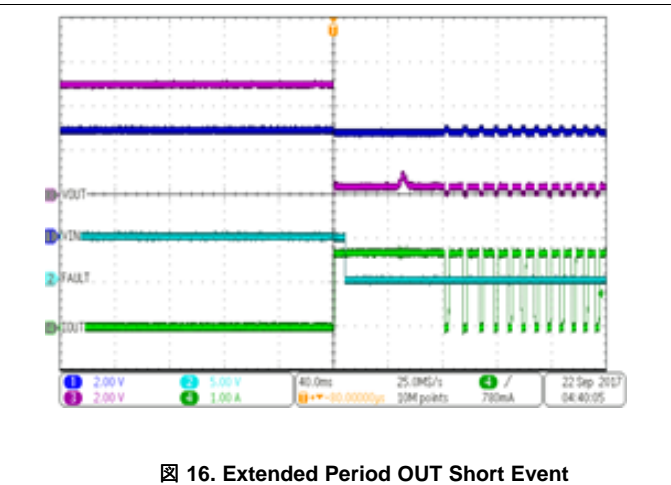


Figure 16. Extended Period OUT Short Event

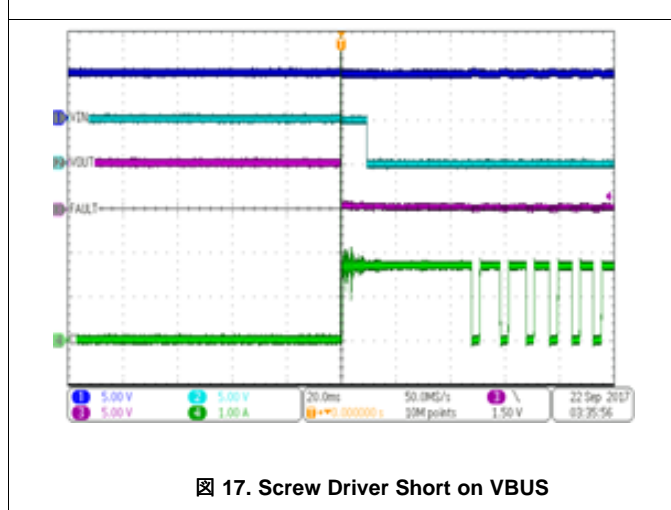
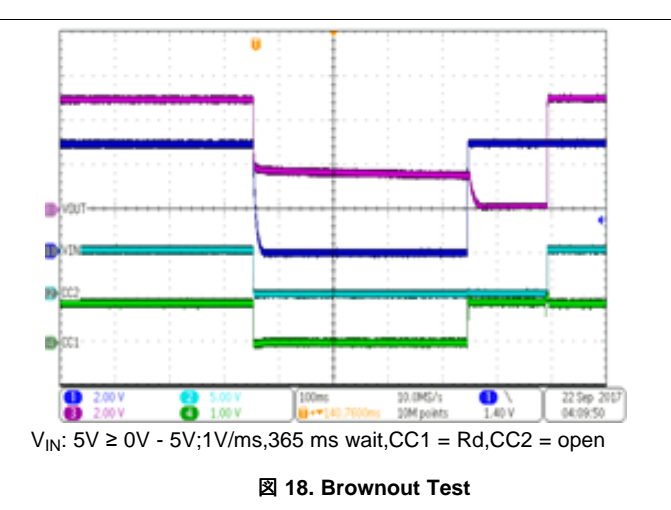


Figure 17. Screw Driver Short on VBUS



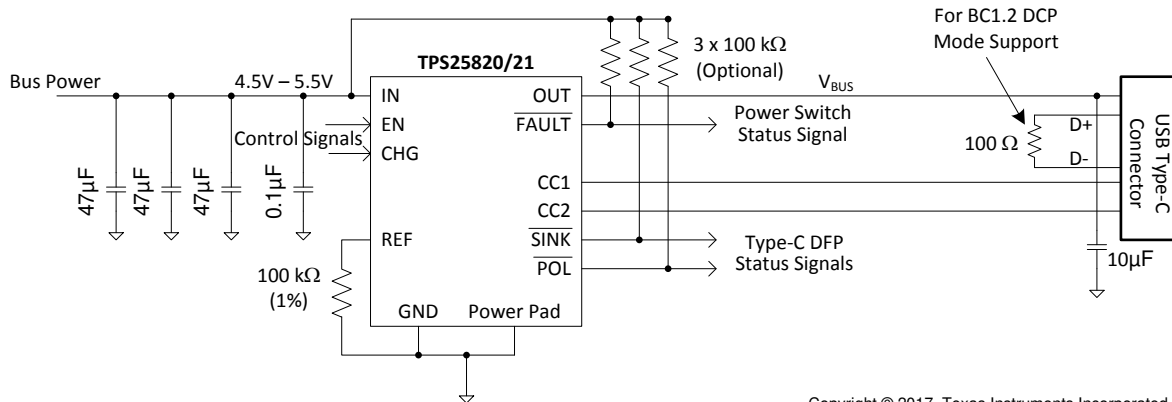
$V_{IN} : 5\text{V} \geq 0\text{V} - 5\text{V}; 1\text{V/ms}, 365 \text{ms wait}, CC1 = R_d, CC2 = \text{open}$

Figure 18. Brownout Test

## Typical Applications (continued)

### 8.2.2 Type -C Source Port Implementation with BC 1.2 (DCP Mode) Support

BC1.2 charging is not supported in the TPS25820/21, however adding BC1.2 DCP (Dedicated Charging Port) support with the TPS25820/21 can be done by having the D+ and D- shorted together with a maximum impedance of 200  $\Omega$  between them and left floating with respect to ground. This is shown in [Figure 19](#). However with DCP implementation the port will not support any data transfer, but is capable of advertising charge currents up to 1.5 A to a legacy device that is connected using a Type-C to Type-A or Micro-B cable. This type of port allows for wall chargers and car chargers with high-charge capability without the need for enumeration. [Figure 19](#) shows a Type-C source implementation capable of supporting 5-V and 1.5-A charging in a Type-C port that is also able to support charging of legacy devices when used with a Type-C -  $\mu$ B cable assembly.



**Figure 19. Type-C Source Port Implementation with BC 1.2 (DCP Mode) Support**

#### 8.2.2.1 Design Requirements

Refer to [Design Requirements](#) for the Design Requirements.

#### 8.2.2.2 Detailed Design Procedure

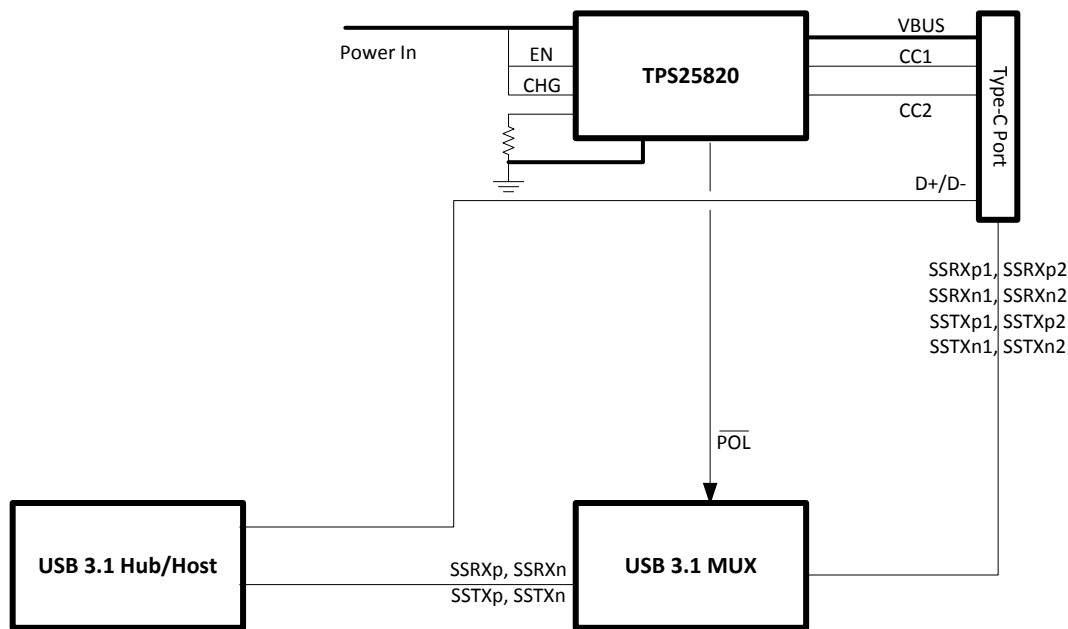
Refer to [Detailed Design Procedure](#) for the Detailed Design Procedure.

#### 8.2.2.3 Application Curves

Refer to [Application Curves](#) for the Application Curves.

### 8.2.3 Implementing a USB 3.1 Type-C Charging Port with the TPS25820

[Figure 20](#) shows a conceptual implementation of USB 3.1 capable Type-C DFP, used in notebook, desktop, LCD monitor or dock application where both USB data and charging is supported. USB 2.0 data lines are connected directly to Type-C receptacle while USB 3.1 data is connected through a USB 3.1 MUX. The TPS25820 controls the USB 3.1 MUX via its POL pin. In this implementation if the USB host/hub is capable of supporting BC1.2 charging then it is possible to support both BC1.2 and Type-C charging from the same Type-C port.

**Typical Applications (continued)**


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**20. USB 3.1 Type-C Charging Port**
**8.2.3.1 Design Requirements**

 Refer to [Design Requirements](#) for the Design Requirements.

**8.2.3.2 Detailed Design Procedure**

 Refer to [Detailed Design Procedure](#) for the Detailed Design Procedure.

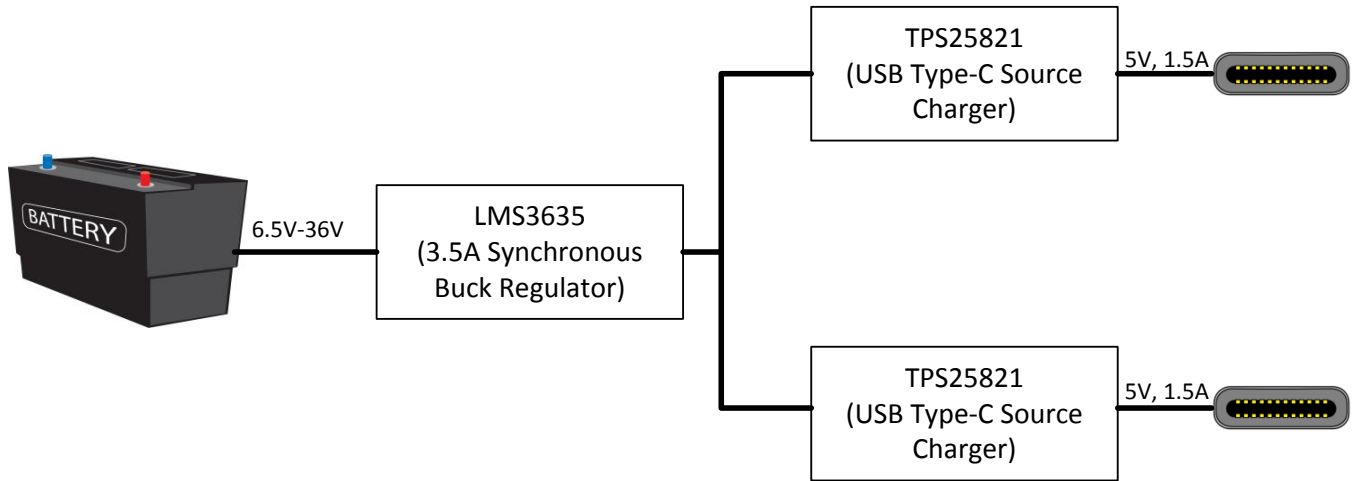
**8.2.3.3 Application Curves**

 Refer to [Application Curves](#) for the Application Curves.

**8.2.4 Implementing TPS25821 in USB Car Chargers**

Given its small footprint, highly integrated design and ultralow standby current, the TPS25821 is ideal for use in cigarette lighter adapter (CLA) USB car chargers capable of supporting Type-C 1.5-A and BC1.2 DCP charging from same Type-C port. This makes it suitable for fast charging phones with either  $\mu\text{B}$  or Type-C connector. [21](#) shows such an implementation for a two port CLA design. The LMS3635 was chosen for its wide VIN and high efficiency to allow for the compact design needed in a CLA body.

## Typical Applications (continued)



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☒ 21. USB Car Charger

### 8.2.4.1 Design Requirements

Refer to [Design Requirements](#) for the Design Requirements.

### 8.2.4.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#) for the Detailed Design Procedure.

### 8.2.4.3 Application Curves

Refer to [Application Curves](#) for the Application Curves.

## 9 Power Supply Recommendations

The device has one power supply input, IN, which is the chip supply. It is connected to the OUT pin via a power integrated MOSFET and in the case of the TPS25820 it also is MUXed either to CC1 or CC2 pin in the Type-C receptacle depending on cable plug polarity.

USB Specification Revision 2.0 and 3.1 requires VBUS voltage at the connector be between 4.75 V to 5.5 V. Depending on layout and routing from supply to the connector, the voltage droop on VBUS has to be tightly controlled especially when providing 1.5 A. Locate the input supply close to the device. For all applications, a ceramic bypass capacitor between OUT and GND less than 10  $\mu\text{F}$  is recommended and should be placed as close to the Type-C connector and device as possible for local noise decoupling. The power supply should be rated higher than the current limit set to avoid voltage droops during overcurrent and short-circuit conditions. Also see [Input and Output Capacitance Considerations](#) on chip by-passing considerations.

## 10 Layout

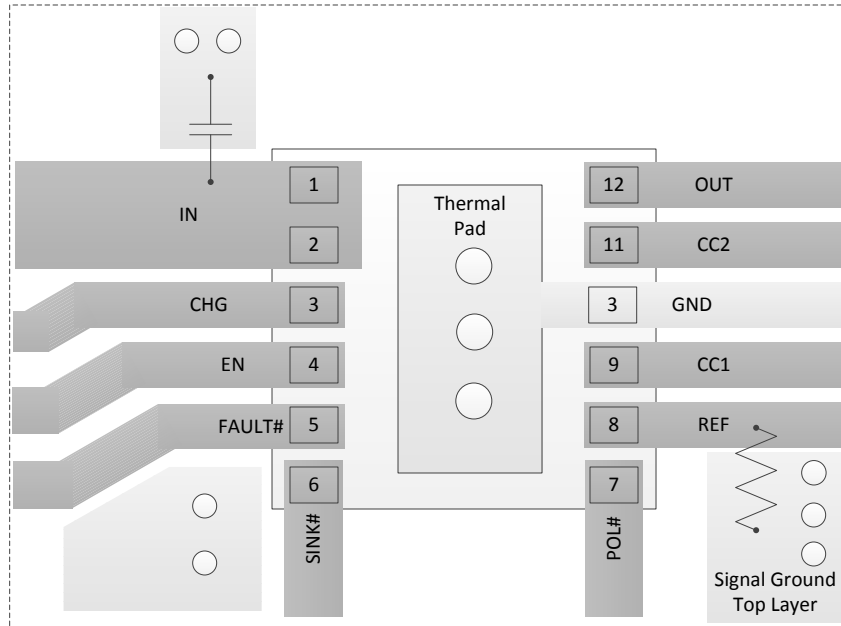
### 10.1 Layout Guidelines

Layout best practices as it applies to the TPS25820/21 are listed below.

- For all applications a ceramic capacitor less than 10  $\mu\text{F}$  is recommended near the Type-C receptacle and another 120- $\mu\text{F}$  ceramic capacitor placed close to the IN pin.
  - The optimum placement of the 120- $\mu\text{F}$  capacitor is closest to the IN and GND pins of the device.
  - Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN pin, and the GND pin of the IC. See [Figure 22](#) for a PCB layout example.
- High current carrying power path connections to the device should be as short as possible and should be sized to carry at least twice the full-load current.
  - Have the input and output traces as short as possible. The most common cause of voltage drop failure in USB power delivery is the resistance associated with the VBUS trace. Trace length, maximum current being supplied for normal operation, and total resistance associated with the VBUS trace must be taken into account while budgeting for voltage drop.
  - For example, a power carrying trace that supplies 1.5 A, at a distance of 20 inches, 0.100-in. wide, with 2-oz. copper on the outer layer will have a total resistance of approximately 0.046  $\Omega$  and voltage drop of 0.07 V. The same trace at 0.050-in.-wide will have a total resistance of approximately 0.09  $\Omega$  and voltage drop of 0.14 V.
  - Make power traces as wide as possible.
- The resistor attached to the REF pin of the device has several requirements:
  - It is recommended to use a 0.5% 100-k $\Omega$  resistor.
  - It should be connected to pins REF and GND.
  - The trace routing between the REF and GND pins of the device should be as short as possible to reduce parasitic effects on the current limit and current advertisement accuracy. These traces should not have any coupling to switching signals on the board.
- Locate all TPS25820/21 pull-up resistors for open-drain outputs close to their connection pin. Pull-up resistors should be 100 k $\Omega$ .
  - When a particular open drain output is not used/needed in the system leave the associated pin open or tied to GND.
- Keep the CC lines close to the same length.
- Thermal Considerations:
  - When properly mounted, the thermal pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to Technical Briefs: *PowerPad™ Thermally Enhanced Package* (TI literature Number [SLMA002](#)) and *PowerPAD™ Made Easy* (TI Literature Number [SLMA004](#)) or more information on using this thermal pad package.
  - The thermal via land pattern specific to the TPS25820/21 can be downloaded from the device web page at [www.ti.com](http://www.ti.com).
  - Obtaining acceptable performance with alternate layout schemes is possible; however the layout example in the following section has been shown to produce good results and is intended as a guideline.

## 10.2 Layout Example

- Top Layer Signal Trace
- Top Layer Signal Ground Plane
- Bottom Layer Signal Ground Plane
- Via to Bottom Layer Ground Plane



☒ 22. Layout Example



## 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

#### 11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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### 11.2 ドキュメントのサポート

#### 11.2.1 関連資料

関連資料については、以下を参照してください。

- 『放熱特性の優れたPowerPad™パッケージ』(TI文書番号SLMA002)
- 『PowerPAD™の簡単な使用方法』(TI文書番号SLMA004)
- 『TPS25810EVM-745ユーザー・ガイド』(SLVUA10)
- 『高電圧DFPからのTPS25810の保護』(SLVA751)

#### 11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS25820	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
TPS25821	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

#### 11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.6 商標

E2E is a trademark of Texas Instruments.

#### 11.7 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25820DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25820	<a href="#">Samples</a>
TPS25820DSST	ACTIVE	WSON	DSS	12	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25820	<a href="#">Samples</a>
TPS25821DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25821	<a href="#">Samples</a>
TPS25821DSST	ACTIVE	WSON	DSS	12	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25821	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



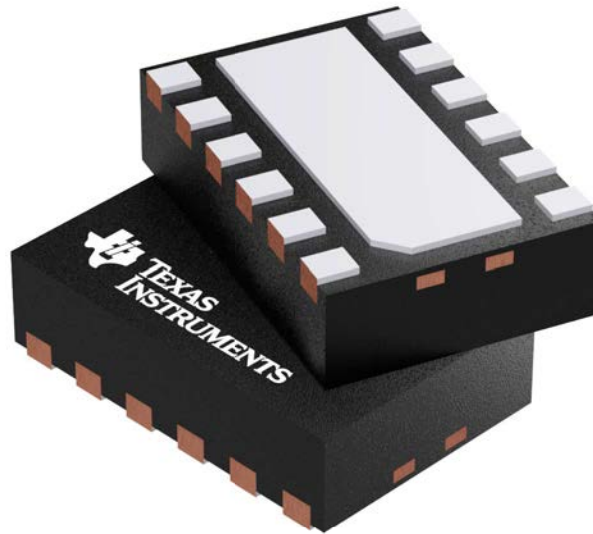
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25820DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS25820DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS25821DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS25821DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

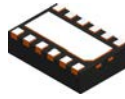

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25820DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS25820DSST	WSON	DSS	12	250	210.0	185.0	35.0
TPS25821DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS25821DSST	WSON	DSS	12	250	210.0	185.0	35.0



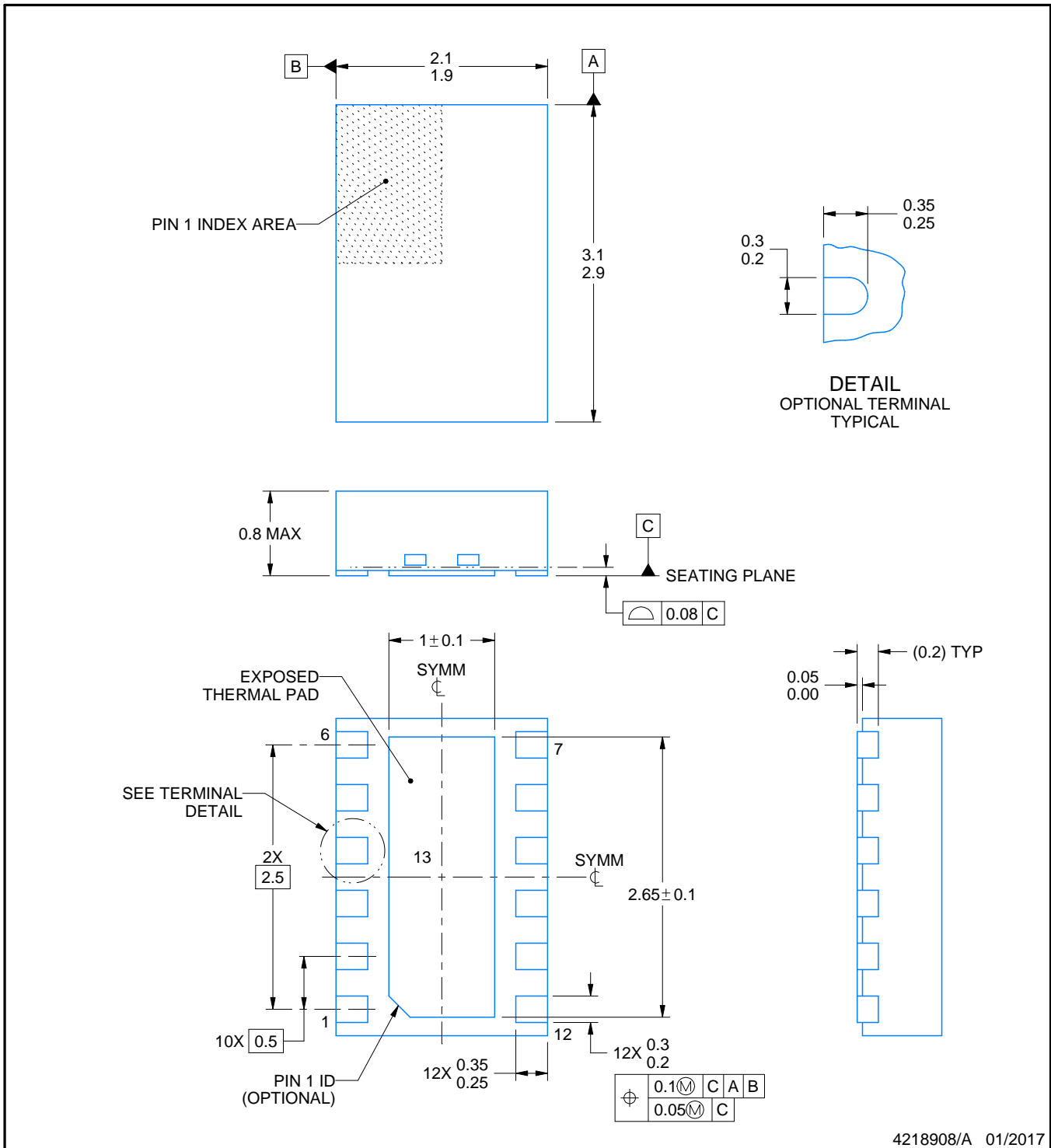
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

# DSS0012B



# PACKAGE OUTLINE WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218908/A 01/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

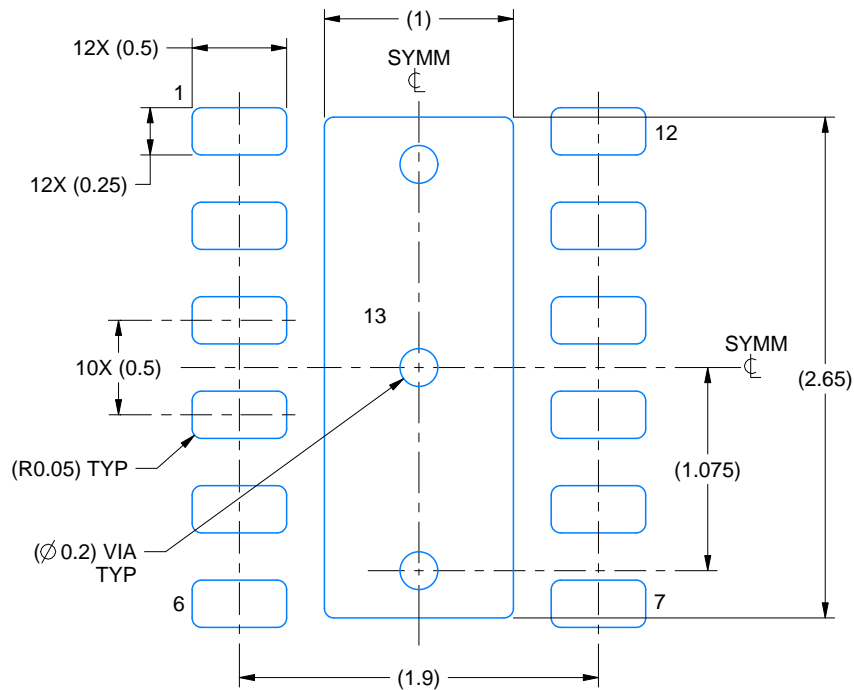


# EXAMPLE BOARD LAYOUT

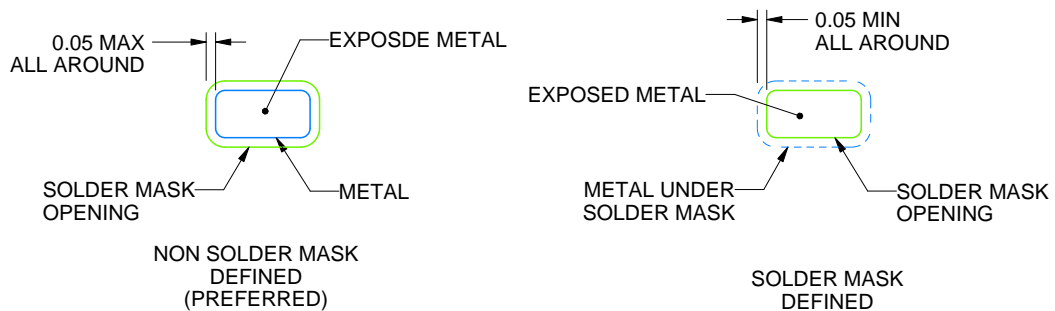
DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



SOLDER MASK DETAILS

4218908/A 01/2017

NOTES: (continued)

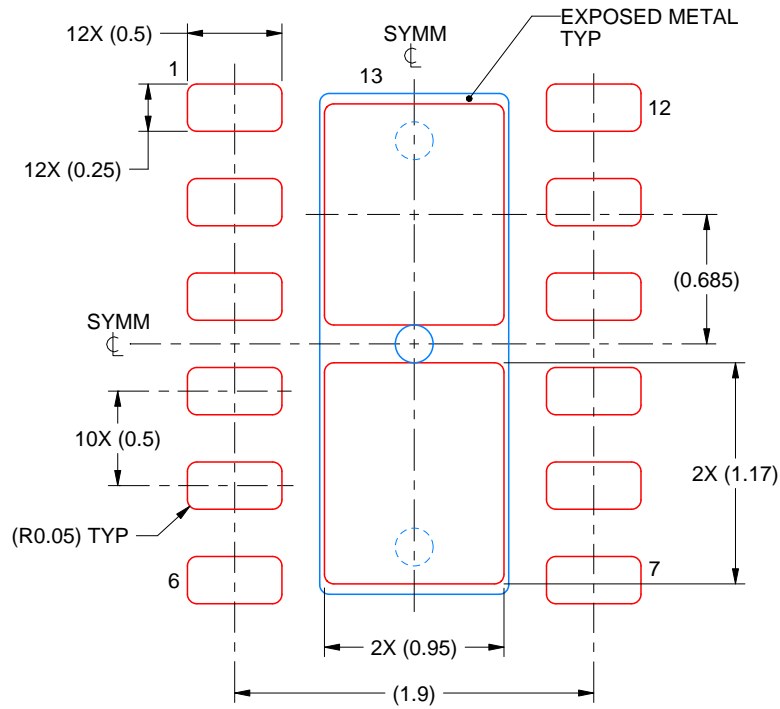
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:  
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218908/A 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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