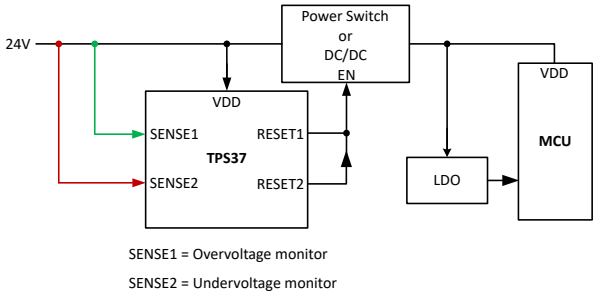
TPS37 ワイド V_{IN}、65V デュアル・チャネル過電圧 / 低電圧 (OV/UV) 検出器、プログラマブル・センス / リセット機能付き

1 特長

- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- 広い電源電圧範囲:2.7V～65V
- 65V 定格の SENSE および RESET ピン
- 低静止電流:1µA (標準値)
- 電圧スレッショルドを柔軟にかつ幅広く選択可能 表 11-1
  - 2.7V～36V (誤差 1.5% 以下)
  - 800mV オプション (誤差 1% 以下)
- ヒステリシス内蔵 (V_{HYS})
  - パーセンテージ・オプション:2%～13% (1% 刻み)
  - 固定オプション:V_{TH} < 8V = 0.5V、1V、1.5V、2V、2.5V
- リセット時間遅延をプログラム可能
  - 10nF = 12.8ms、10µF = 12.8s
- 検出時間遅延をプログラム可能
  - 10nF = 1.28ms、10µF = 1.28s
- マニュアル・リセット ($\overline{MR}$) 機能
- 出力トポロジ:オープン・ドレインまたはプッシュプル

2 アプリケーション

- アナログ入力モジュール
- CPU (PLC コントローラ)
- サーボ・ドライブ制御モジュール
- サーボ・ドライブの電力段モジュール
- サーボ・ドライブ機能安全モジュール
- HVAC (空調) バルブおよびアクチュエータの制御



代表的なアプリケーション回路

3 概要

TPS37 は、過電圧 (OV) および低電圧 (UV) 状態の高速検出のための、入力範囲が広く静止電流が小さいウィンドウ・スーパーバイザのファミリです。各デバイスは、高精度の内部基準電圧、2 つの独立した構成可能な電圧コンパレータ、抵抗デバイダを内蔵しています。TPS37 は、ファクトリ・オートメーション、モータ駆動、ビル・オートメーションなどの各種産業用アプリケーションの 12V/24V 電源レールに直接接続し、それを監視できます。SENSE ピンに組み込まれたヒステリシスは、電源電圧レール監視中のリセット信号の誤検出を防止します。

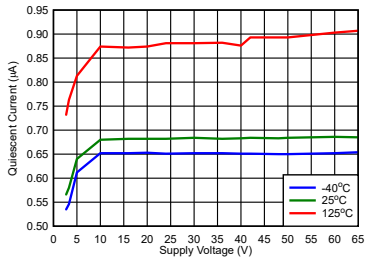
VDD ピンと SENSE ピンが独立しているため、信頼性が高いシステムが求める冗長性を実現できます。SENSE は VDD から切り離されているため、VDD よりも高い電圧と低い電圧を監視できます。SENSE ピンは高インピーダンス入力であるため、任意で外付け抵抗を使用できます。CTSx および CTRx ピンを使うことで、RESET 信号の立ち上がり / 立ち下がりエッジの遅延を調整できます。また、CTSx は、監視対象の電圧レールの電圧グリッチを無視することで、デバウンサとして機能します。CTRx は、システムを強制的にリセットするための手動リセット ($\overline{MR}$) として動作します。

TPS37 は WSON または SOT-23 パッケージで供給されます。IEC60664 のガイドラインに基づいて VDD と GND との間の沿面距離を増やすため、中央パッドはどこにも接続されていません。TPS37 は -40℃～+125℃の T_A で動作します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS37	WSON (10) (DSK)	2.5mm × 2.5mm
TPS37	SOT-23 (14) (DYY)	4.1mm × 1.9mm

(1) パッケージの詳細については、このデータシートの末尾の外形図を参照してください。



I_{DD} と V_{DD} との代表的な関係

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4 Revision History

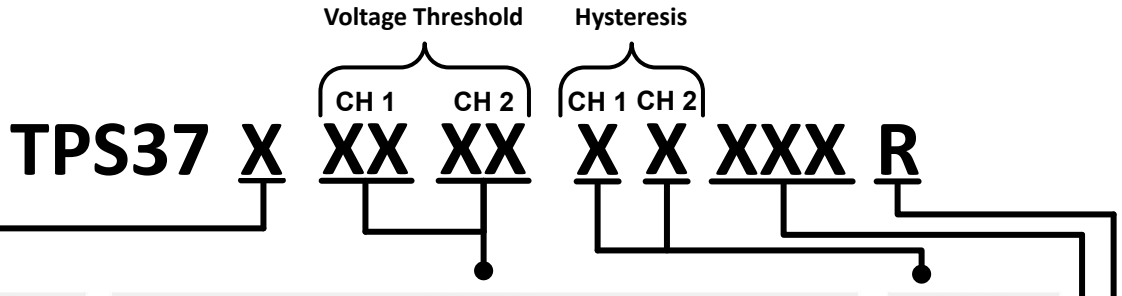
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (December 2021) to Revision E (August 2023)	Page
• 機能安全に関する記述を追加し、ラッチ機能を削除	1
• Added Vit and Vhyst timing diagram	10
• Added CTS and CTR value plots	13

Changes from Revision C (September 2021) to Revision D (December 2021)	Page
• 「事前情報」から「量産データ」のリリースに変更	1

5 Device Comparison

Contact TI sales representatives or consult TI's E2E forum for details and availability; minimum order quantities may apply.



Topology

Suffix	CH1	CH2
A	OV OD L	UV OD L
B	OV PP H	UV OD L
C	OV OD L	UV OD H
D	OV PP H	UV OD H
E	OV OD H	UV OD H
F	OV OD H	UV OD L
G	OV PP L	UV OD H
H	OV PP L	UV OD L

Threshold Voltage

100mV steps				400mV steps		500mV steps		1V steps	
Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT
01	800mV	70	7.0V	A0	10.4V	D0	20.5V	F0	31.0V
27	2.7V	71	7.1V	A1	10.8V	D1	21.0V	F1	32.0V
28	2.8V	72	7.2V	A2	11.2V	D2	21.5V	F2	33.0V
29	2.9V	73	7.3V	A3	11.6V	D3	22.0V	F3	34.0V
30	3.0V	74	7.4V	A4	12.0V	D4	22.5V	F4	35.0V
31	3.1V	75	7.5V	A5	12.4V	D5	23.0V	F5	36.0V
32	3.2V	76	7.6V	A6	12.8V	D6	23.5V		
33	3.3V	77	7.7V	A7	13.2V	D7	24.0V		
34	3.4V	78	7.8V	A8	13.6V	D8	24.5V		
35	3.5V	79	7.9V	A9	14.0V	D9	25.0V		
36	3.6V	80	8.0V	B0	14.4V	E0	25.5V		
37	3.7V	81	8.1V	B1	14.8V	E1	26.0V		
38	3.8V	82	8.2V	B2	15.2V	E2	26.5V		
39	3.9V	83	8.3V	B3	15.6V	E3	27.0V		
40	4.0V	84	8.4V	B4	16.0V	E4	27.5V		
41	4.1V	85	8.5V	B5	16.4V	E5	28.0V		
42	4.2V	86	8.6V	B6	16.8V	E6	28.5V		
43	4.3V	87	8.7V	B7	17.2V	E7	29.0V		
44	4.4V	88	8.8V	B8	17.6V	E8	29.5V		
45	4.5V	89	8.9V	B9	18.0V	E9	30.0V		
46	4.6V	90	9.0V	C0	18.4V				
47	4.7V	91	9.1V	C1	18.8V				
48	4.8V	92	9.2V	C2	19.2V				
49	4.9V	93	9.3V	C3	19.6V				
50	5.0V	94	9.4V	C4	20.0V				
51	5.1V	95	9.5V						
52	5.2V	96	9.6V						
53	5.3V	97	9.7V						
54	5.4V	98	9.8V						
55	5.5V	99	9.9V						
56	5.6V	00	10.0V						
57	5.7V								
58	5.8V								
59	5.9V								
60	6.0V								
61	6.1V								
62	6.2V								
63	6.3V								
64	6.4V								
65	6.5V								
66	6.6V								
67	6.7V								
68	6.8V								
69	6.9V								

Hysteresis

Suffix	CH1
2	2%
3	3%
4	4%
5	5%
6	6%
7	7%
8	8%
9	9%
A	10%
B	11%
C	12%
D	13%
E	0.5V
F	1V
G	1.5V
H	2V
I	2.5V

Package

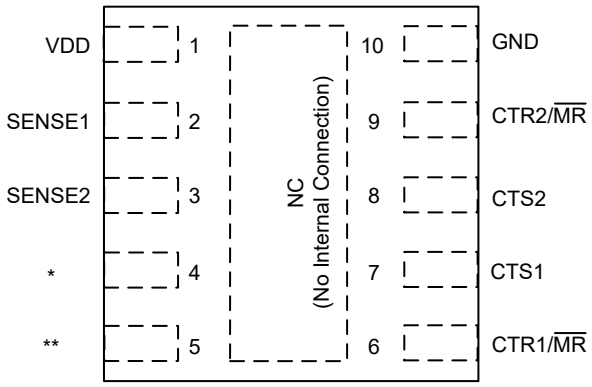
Suffix	Name
DSK	WSON
DYY	SOT-23

Reel

Suffix	Name
R	Large

1. Sense logic: OV = overvoltage; UV = undervoltage
2. Reset topology: PP = Push-Pull; OD = Open-Drain
3. Reset logic: L = Active-Low; H = Active-High
4. A to I hysteresis options are only available for 2.7 V to 8 V threshold options

6 Pin Configuration and Functions

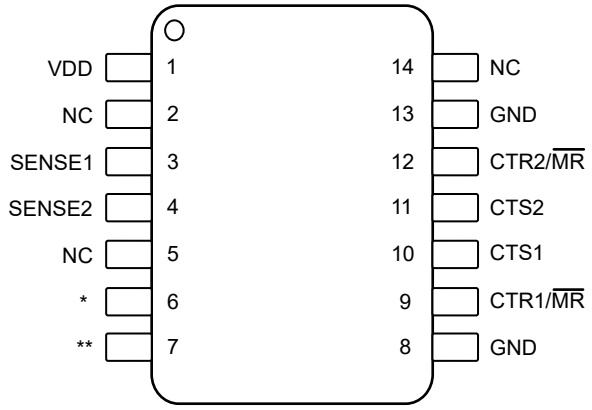


* Pin 4 Options
1. RESET1_OV##
2. RESET1_OV##

** Pin 5 Options
1. RESET2_UVOD
2. RESET2_UVOD

OD (Open-Drain) or PP (Push-Pull)

図 6-1. DSK Package, 10-Pin WSON, TPS37 (Top View)



* Pin 6 Options
1. RESET1_OV##
2. RESET1_OV##

** Pin 7 Options
1. RESET2_UVOD
2. RESET2_UVOD

OD (Open-Drain) or PP (Push-Pull)

図 6-2. DYY Package, 14-Pin SOT-23, TPS37 (Top View)

表 6-1. Pin Functions

PIN NAME	WSON (DSK) PIN NUM.	SOT23 (DYY) PIN NUM.	I/O	DESCRIPTION
VDD	1	1	I	**Input Supply Voltage:** Bypass with a 0.1 µF capacitor to GND.
SENSE1	2	3	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on SENSE1 pin transitions above the upper threshold voltage of V_{IT+}, $\overline{RESET1}$/RESET1 asserts after the sense time delay, set by CTS1. When the voltage on the SENSE1 pin transitions below the upper threshold voltage of V_{IT+} - V_{HYS}, $\overline{RESET1}$/RESET1 deasserts after the reset time delay, set by CTR1. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
SENSE2	3	4	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on SENSE2 pin transitions below the lower threshold voltage of V_{IT-}, $\overline{RESET2}$/RESET2 asserts after the sense time delay, set by CTS2. When the voltage on the SENSE2 pin transitions above the lower threshold voltage of V_{IT-} + V_{HYS}, $\overline{RESET2}$/RESET2 deasserts after the reset time delay, set by CTR2. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
$\overline{RESET1}$/ RESET1	4	6	O	**Output Reset Signal For Channel 1:** See セクション 5 for output topology options. $\overline{RESET1}$/RESET1 asserts when SENSE1 rises outside of the upper voltage threshold. $\overline{RESET1}$/RESET1 remains asserted for the reset time delay period after SENSE1 transitions out of an overvoltage (OV) fault condition. For active low open-drain reset output, an external pullup resistor is required. Do not place external pullup resistors on push-pull outputs. Reset output signal for: **SENSE1** Sensing Topology: **Overvoltage (OV)** Output topology: **Open Drain or Push Pull, Active Low or Active High**
$\overline{RESET2}$/ RESET2	5	7	O	**Output Reset Signal For Channel 2:** See セクション 5 for output topology options. $\overline{RESET2}$/RESET2 asserts when SENSE2 falls outside of the lower voltage threshold. $\overline{RESET2}$/RESET2 remains asserted for the reset time delay period after SENSE2 transitions out of an undervoltage (UV) fault condition. For active low open-drain reset output, an external pullup resistor is required. Reset output signal for: **SENSE2** Sensing Topology: **Undervoltage (UV)** Output topology: **Open Drain, Active Low or Active High**
CTR1/ $\overline{MR}$	6	9	-	**Channel 1 RESET Time Delay:** User-programmable reset time delay for $\overline{RESET1}$/RESET1. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. **Manual Reset:** If this pin is driven low, the $\overline{RESET1}$/RESET1 output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high.
CTR2/ $\overline{MR}$	9	12	-	**Channel 2 RESET Time Delay:** User-programmable reset time delay for $\overline{RESET2}$/RESET2. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. **Manual Reset:** If this pin is driven low, the $\overline{RESET2}$/RESET2 output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high.
GND	10	8, 13	-	**Ground.** All GND pins must be electrically connected to the board ground.
NC	PAD	2, 5, 14	-	The PAD for the **DSK** package is not internally connected, the PAD can be connected to GND or be left floating. For the **DYY** package, NC stands for “No Connect”. The pins are to be left floating.
CTS1	7	10	O	**Channel 1 SENSE Time Delay:** Capacitor programmable sense delay: CTS1 pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{RESET1}$/RESET1 delay time to assert.
CTS2	8	11	O	**Channel 2 SENSE Time Delay:** Capacitor programmable sense delay: CTS2 pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{RESET2}$/RESET2 delay time to assert.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted (1)

		MIN	MAX	UNIT
Voltage	VDD, V_{SENSE1},V_{SENSE2}, V_{RESET1}, V_{RESET2}, $V_{\overline{RESET1}}$, $V_{\overline{RESET2}}$	–0.3	70	V
Voltage	V_{CTS1}, V_{CTS2}, V_{CTR1}, V_{CTR2}	–0.3	6	V
Current	I_{RESET1}, I_{RESET2}, $I_{\overline{RESET1}}$, $I_{\overline{RESET2}}$		10	mA
Temperature (2)	Operating junction temperature, T_J	–40	150	°C
Temperature (2)	Operating Ambient temperature, T_A	–40	150	°C
Temperature (2)	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	2.7		65	V
Voltage	V_{SENSE1},V_{SENSE2}, V_{RESET1}, V_{RESET2}, $V_{\overline{RESET1}}$, $V_{\overline{RESET2}}$	0		65	V
Voltage	V_{CTS1}, V_{CTS2}, V_{CTR1}, V_{CTR2}	0		5.5	V
Current	I_{RESET1}, I_{RESET2}, $I_{\overline{RESET1}}$, $I_{\overline{RESET2}}$	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS37		UNIT
		DSK	DYY	
		10-PIN	14-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.4	131.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.3	61.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.2	56.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.2	56.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	34.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR1/$\overline{MR}$ = CTR2/$\overline{MR}$ = CTS1 = CTS2 = open, output reset pull-up resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5 V, and load C_{LOAD} = 10 pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and VDD = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
V_{DD}	Supply Voltage		2.7		65	V
UVLO (1)	Undervoltage Lockout	V_{DD} Falling below $V_{DD\ (MIN)}$			2.7	V
V_{POR}	Power on Reset Voltage (2) $\overline{RESET}$, Active Low (Open-Drain, Push-Pull)	$V_{OL(MAX)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			1.4	V
V_{POR}	Power on Reset Voltage (2) RESET, Active High (Push-Pull)	$V_{OH(MIN)}$ = 0.8 x V_{DD} $I_{OUT\ (Source)}$ = 15 µA			1.4	V
I_{DD}	Supply current into VDD pin	V_{IT} = 800 mV $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$		1	2.6	µA
		V_{IT} = 2.7 V to 36 V $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$		1	2	µA
SENSE (Input)						
I_{SENSE}	Input current (SENSE1, SENSE2)	V_{IT} = 800 mV			100	nA
I_{SENSE}	Input current (SENSE1, SENSE2)	V_{IT} < 10 V			0.8	µA
I_{SENSE}	Input current (SENSE1, SENSE2)	10 V < V_{IT} < 26 V			1.2	µA
I_{SENSE}	Input current (SENSE1, SENSE2)	V_{IT} > 26 V			2	µA
V_{ITN}	Input Threshold Negative (Undervoltage)	V_{IT} = 2.7 V to 36 V	-1.5		1.5	%
		V_{IT} = 800 mV (3)	0.792	0.800	0.808	V
V_{ITP}	Input Threshold Positive (Overvoltage)	V_{IT} = 2.7 V to 36 V	-1.5		1.5	%
		V_{IT} = 800 mV (3)	0.792	0.800	0.808	V
V_{HYS}	Hysteresis Accuracy (4)	V_{IT} = 0.8 V and 2.7 V to 36 V V_{HYS} Range = 2% to 13% (1% step)	-1.5		1.5	%
		V_{IT} = 2.7 V to 8 V V_{HYS} = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V (V_{ITP} - V_{HYS}) ≥ 2.4 V, OV Only	-1.5		1.5	%
RESET (Output)						
$I_{lkg(OD)}$	Open-Drain leakage (RESET1, RESET2)	V_{RESET} = 5.5 V V_{ITN} < V_{SENSE} < V_{ITP}			300	nA
		V_{RESET} = 65 V V_{ITN} < V_{SENSE} < V_{ITP}			300	nA
V_{OL} (5)	Low level output voltage	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 5 mA			300	mV
V_{OH_DO}	High level output voltage dropout (V_{DD} - V_{OH} = V_{OH_DO}) (Push-Pull only)	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 500 uA			100	mV
V_{OH} (5)	High level output voltage (Push-Pull only)	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 5 mA	0.8V_{DD}			V

7.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR1/$\overline{MR}$ = CTR2/$\overline{MR}$ = CTS1 = CTS2 = open, output reset pull-up resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5 V, and load C_{LOAD} = 10 pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and VDD = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR1 / $\overline{MR}$, CTR2 / $\overline{MR}$)		877	1000	1147	Kohms
R_{CTS}	Internal resistance (C_{TS1}, C_{TS2})		88	100	122	Kohms
Manual Reset ($\overline{MR}$)						
$V_{\overline{MR}\_IH}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic high input	VDD = 2.7 V	2200			mV
$V_{\overline{MR}\_IH}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic high input	VDD = 65 V	2500			mV
$V_{\overline{MR}\_IL}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic low input	VDD = 2.7 V			1300	mV
$V_{\overline{MR}\_IL}$	CTR1 / $\overline{MR}$ and CTR2 / $\overline{MR}$ pin logic low input	VDD = 65 V			1300	mV

(1) When V_{DD} voltage falls below UVLO, reset is asserted for Output 1 and Output 2. V_{DD} slew rate ≤ 100 mV / µs
(2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below VPOR, the output cannot be determined. V_{DD} dv/dt ≤ 100mV/µs
(3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
(4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
(5) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

7.6 Timing Requirements

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR1/$\overline{MR}$ = CTR2/$\overline{MR}$ = CTS1 = CTS2 = open (1), output reset pull-up resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5V, and C_{LOAD} = 10 pF. VDD and SENSE slew rate = 1V / µs. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and VDD = 16 V and V_{IT} = 6.5 V (V_{IT} refers to either V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters						
t_{CTR}	Reset release time delay (CTR1/$\overline{MR}$, CTR2/$\overline{MR}$) (2)	VIT = 2.7 V to 36 V C_{CTR1} = C_{CTR2} = Open 20% Overdrive from Hysteresis			100	µs
		VIT = 800 mV C_{CTR1} = C_{CTR2} = Open 20% Overdrive from Hysteresis			40	µs
t_{CTS}	Sense detect time delay (CTS1, CTS2) (3)	VIT = 2.7 V to 36 V C_{CTS1} = C_{CTS2} = Open 20% Overdrive from V_{IT}		34	90	µs
		VIT = 800 mV C_{CTS1} = C_{CTS2} = Open 20% Overdrive from V_{IT}		8	17	µs
t_{SD}	Startup Delay (4)	$C_{CTR1/\overline{MR}}$ = $C_{CTR2/\overline{MR}}$ = Open			2	ms

(1) C_{CTR1} = Reset delay channel 1, C_{CTR2} = Reset delay channel 2, C_{CTS1} = Sense delay channel 1, C_{CTS2} = Sense delay channel 2

(2) **CTR Reset detect time delay:**
Overvoltage active-LOW output is measure from $V_{ITP\ -\ HYS}$ to V_{OH}
Undervoltage active-LOW output is measure from $V_{ITN\ +\ HYS}$ to V_{OH}
Overvoltage active-HIGH output is measure from $V_{ITP\ -\ HYS}$ to V_{OL}
Undervoltage active-HIGH output is measure from $V_{ITN\ +\ HYS}$ to V_{OL}

(3) **CTS Sense detect time delay:**
Active-low output is measure from V_{IT} to V_{OL} (or V_{Pullup})
Active-high output is measured from V_{IT} to V_{OH}
V_{IT} refers to either V_{ITN} or V_{ITP}

(4) During the power-on sequence, VDD must be at or above $V_{DD\ (MIN)}$ for at least t_{SD} before the output is in the correct state based on V_{SENSE}.
t_{SD} time includes the propagation delay (C_{CTR1} = C_{CTR2} = Open). Capaicitor in C_{CTR1} or C_{CTR2} will add time to t_{SD}.

7.7 Timing Diagrams

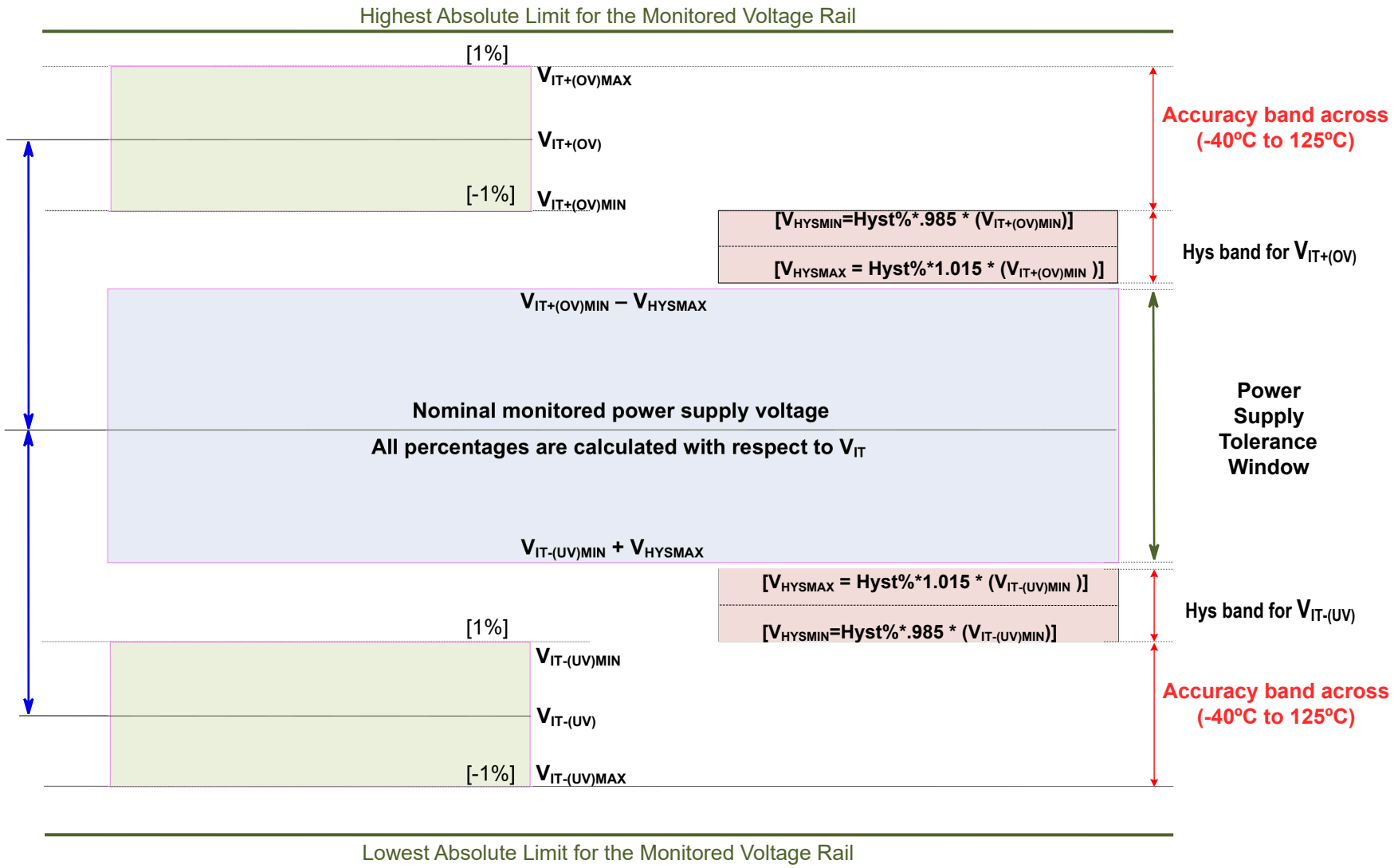
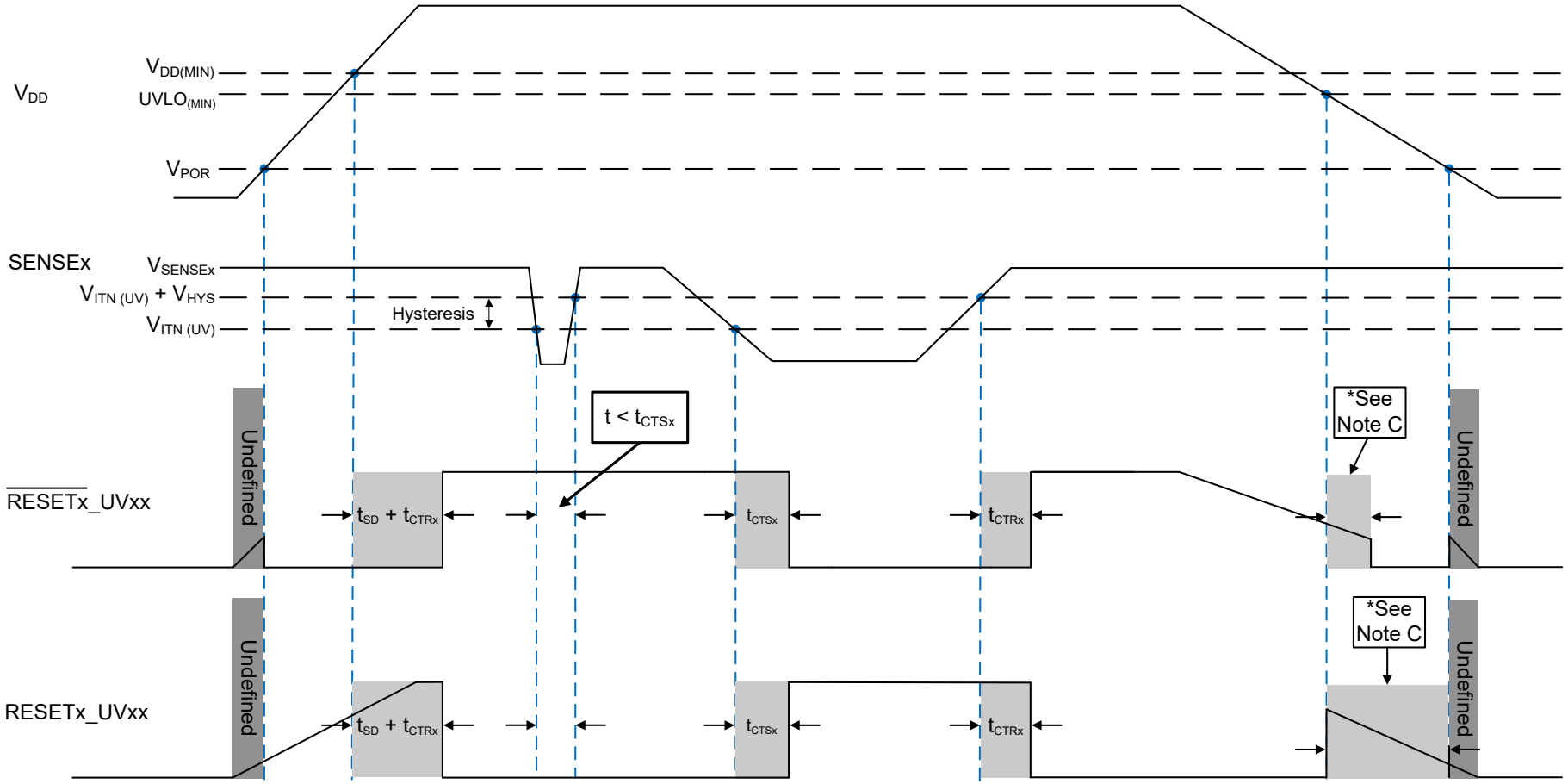
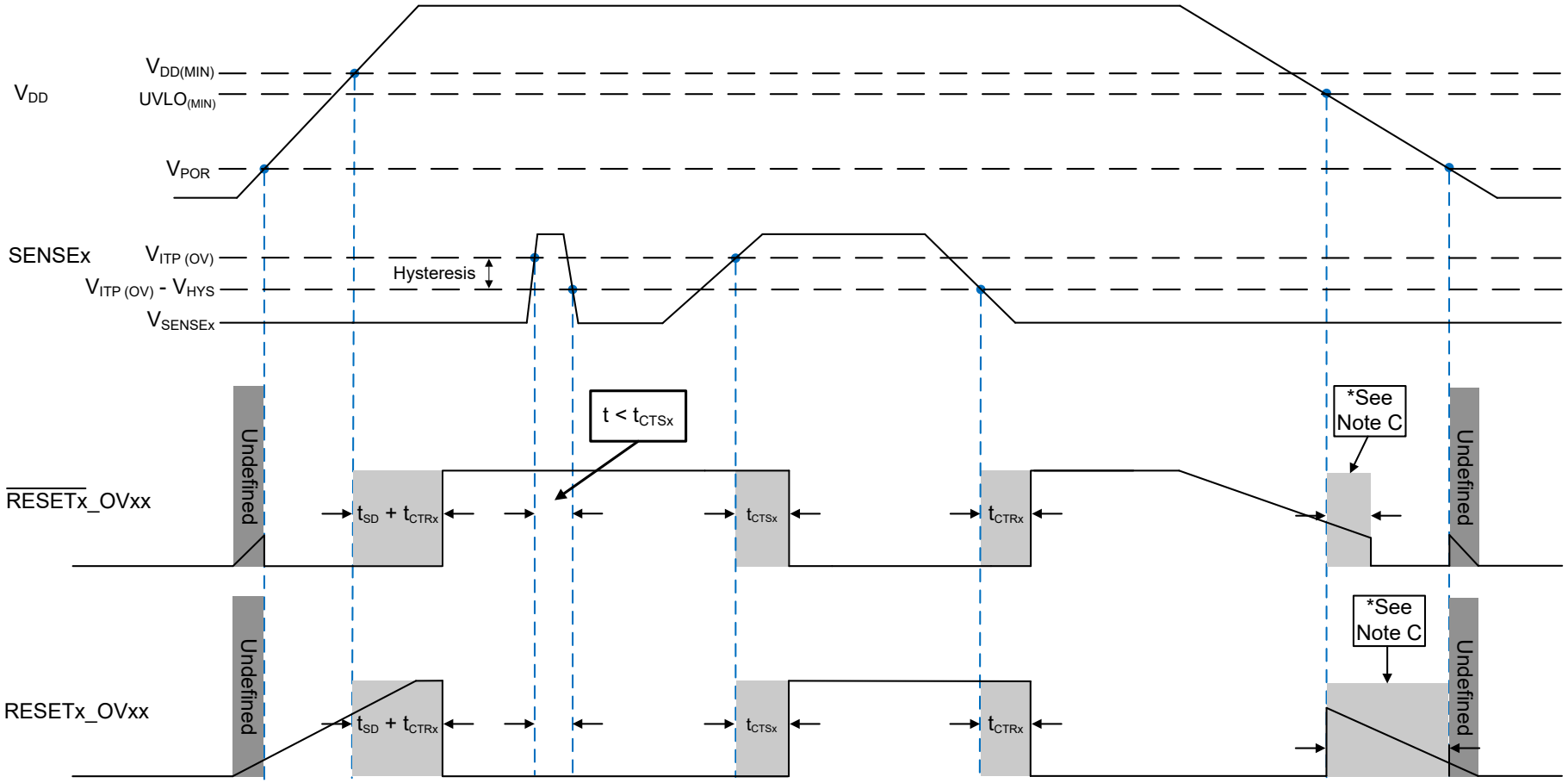


図 7-1. Voltage Threshold and Hysteresis Accuracy



A. For open-drain output option, the timing diagram assumes the $\overline{\text{RESETx}}$_UVOD / RESETx_UVOD pin is connected via an external pull-up resistor to VDD.
B. Be advised that this diagram shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTRx}) time.
C. $\overline{\text{RESETx}}$_UVxx / RESETx_UVxx is asserted when VDD goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTRx}, is reached.

図 7-2. SENSEx Undervoltage (UV) Timing Diagram

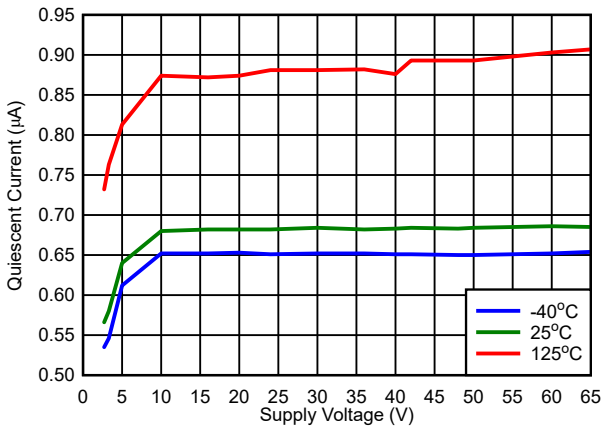


A. For open-drain output option, the timing diagram assumes the $\overline{\text{RESETx}}$_OVOD / RESETx_OVOD pin is connected via an external pull-up resistor to VDD.
B. Be advised that this diagram shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTRx}) time.
C. $\overline{\text{RESETx}}$_OVxx / RESETx_OVxx is asserted when VDD goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTRx}, is reached.

図 7-3. SENSEx Overvoltage (OV) Timing Diagram

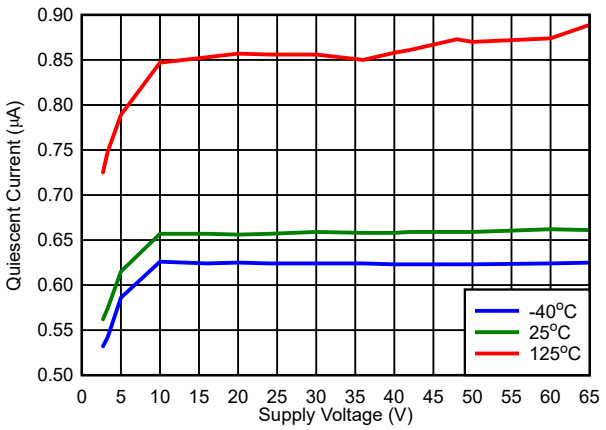
7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS37 device. Test conditions are T_A = 25°C, R_{PU} = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.



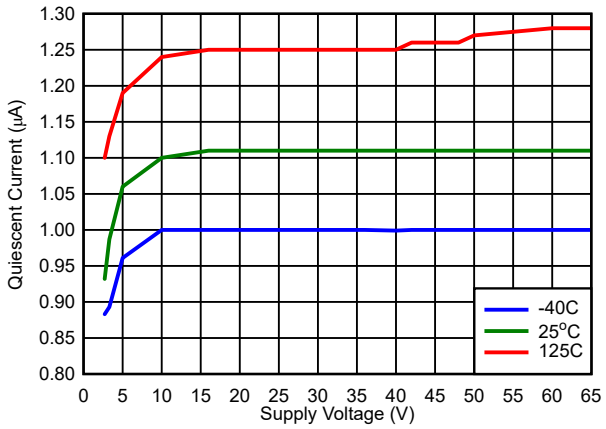
$\overline{RESET}$ = High, V_{IT} = 2.7 V

図 7-4. V_{DD} vs I_{DD} ($\overline{RESET}$ = High, V_{IT} = 2.7 V)



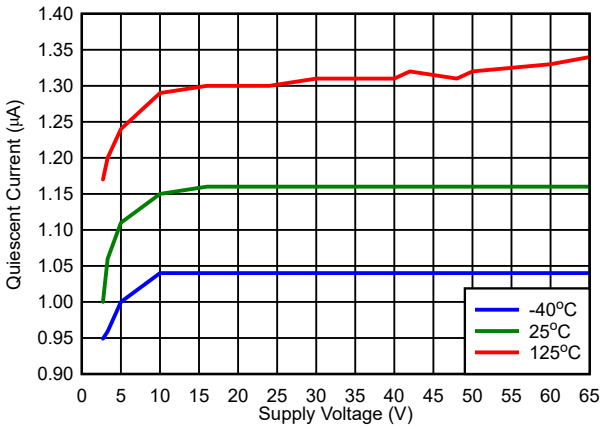
$\overline{RESET}$ = Low, V_{IT} = 2.7 V

図 7-5. V_{DD} vs I_{DD} ($\overline{RESET}$ = Low, V_{IT} = 2.7 V)



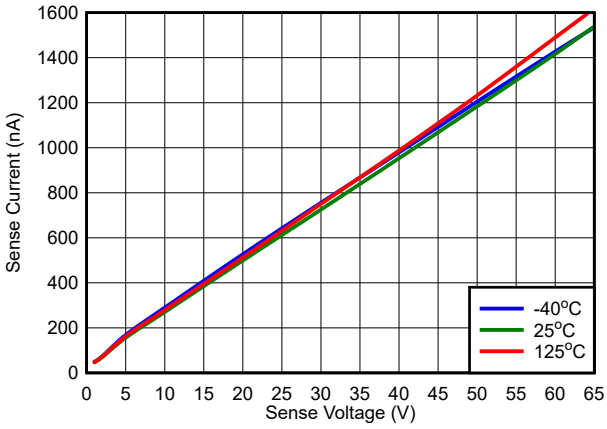
$\overline{RESET}$ = High, V_{IT} = 0.8 V

図 7-6. V_{DD} vs I_{DD} ($\overline{RESET}$ = High, V_{IT} = 0.8 V)



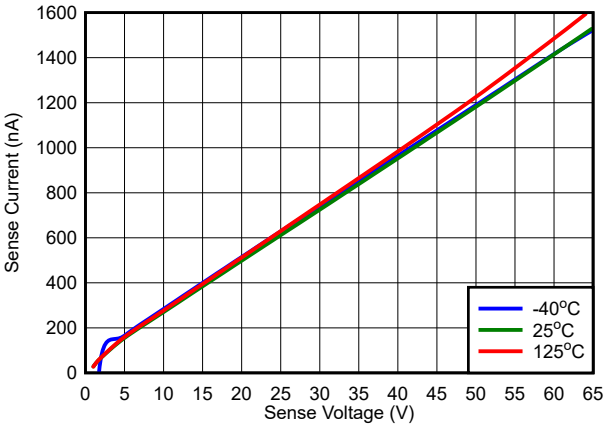
$\overline{RESET}$ = Low, V_{IT} = 0.8 V

図 7-7. V_{DD} vs I_{DD} ($\overline{RESET}$ = Low, V_{IT} = 0.8 V)



V_{DD} = 2.7 V

図 7-8. V_{SENSE} vs I_{SENSE}

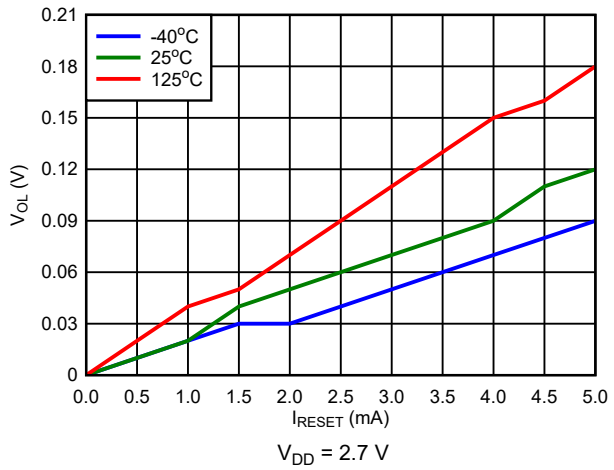


V_{DD} = 65 V

図 7-9. V_{SENSE} vs I_{SENSE}

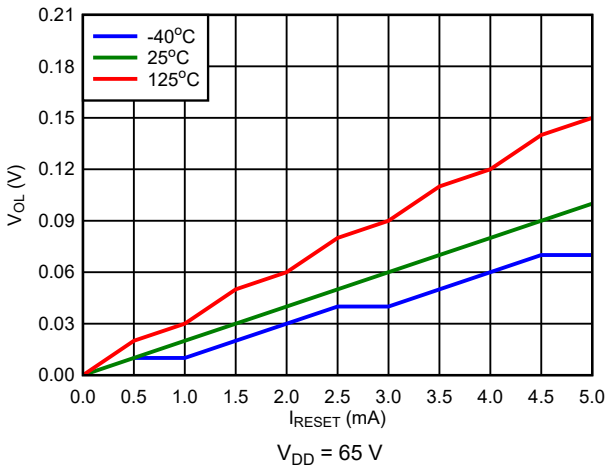
7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS37 device. Test conditions are T_A = 25°C, R_{PU} = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.



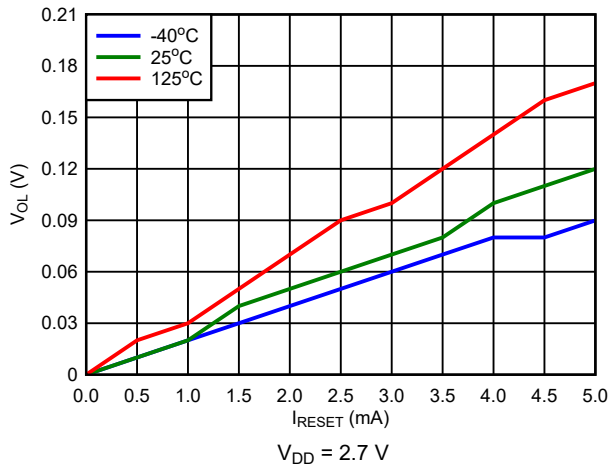
V_{DD} = 2.7 V

図 7-10. Open-Drain Active Low V_{OL} vs I_{RESET}



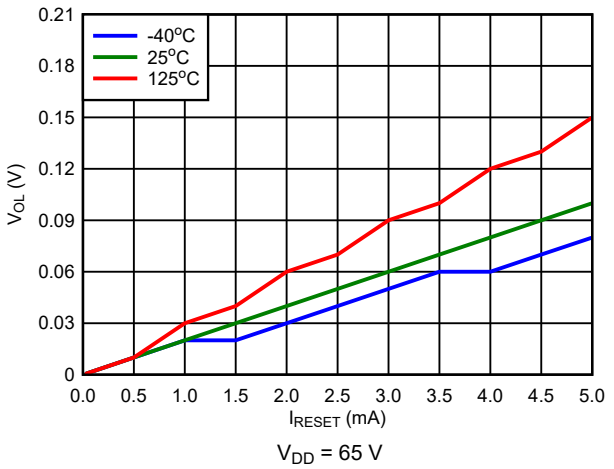
V_{DD} = 65 V

図 7-11. Open-Drain Active Low V_{OL} vs I_{RESET}



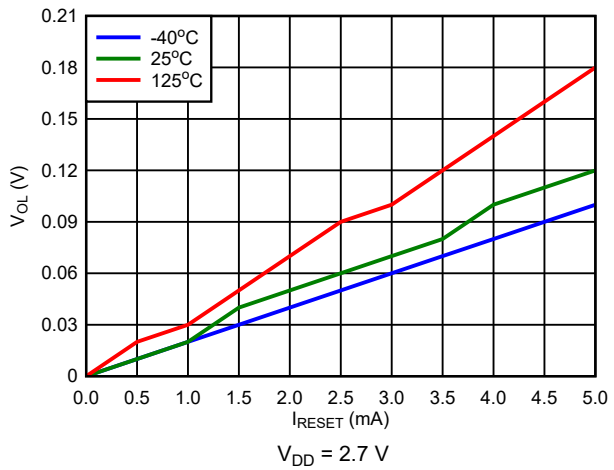
V_{DD} = 2.7 V

図 7-12. Open-Drain Active High V_{OL} vs I_{RESET}



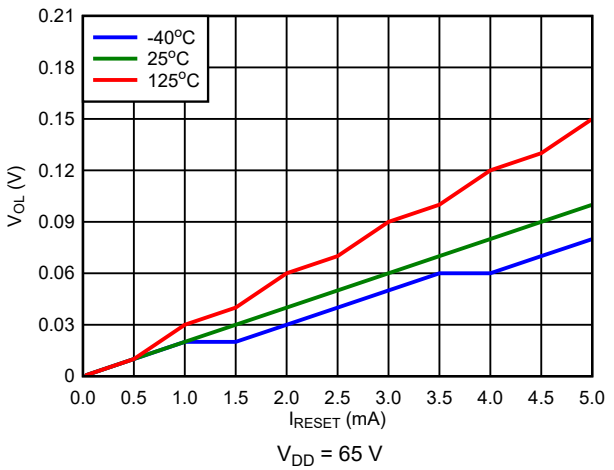
V_{DD} = 65 V

図 7-13. Open-Drain Active High V_{OL} vs I_{RESET}



V_{DD} = 2.7 V

図 7-14. Push-Pull Active High V_{OL} vs I_{RESET}



V_{DD} = 65 V

図 7-15. Push-Pull Active High V_{OL} vs I_{RESET}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS37 device. Test conditions are T_A = 25°C, R_{PU} = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

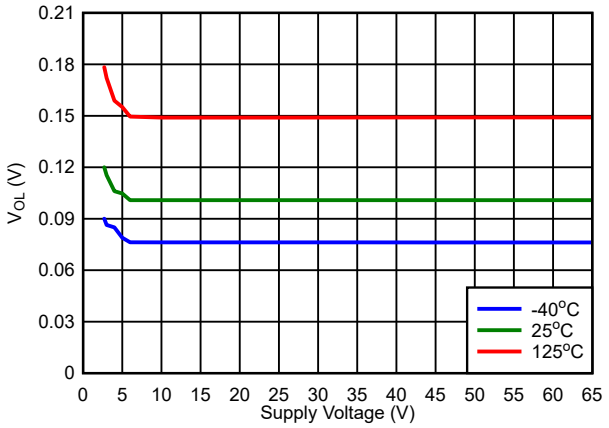


図 7-16. Open-Drain Active Low V_{OL} vs V_{DD}

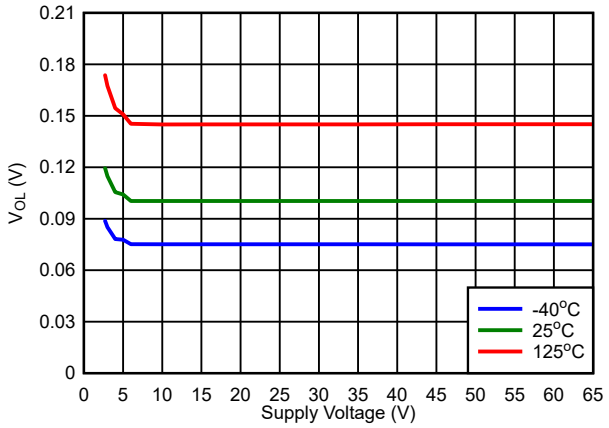


図 7-17. Open-Drain Active High V_{OL} vs V_{DD}

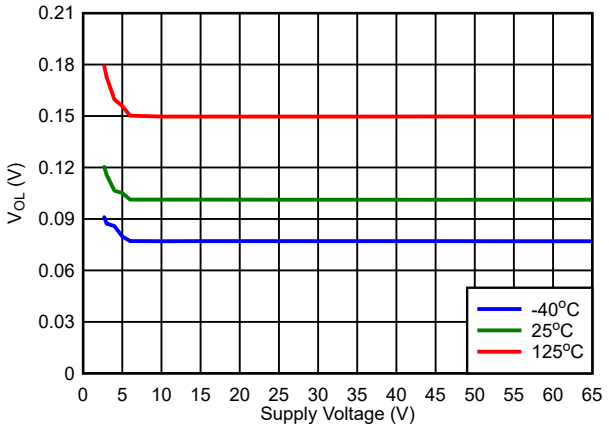


図 7-18. Push-Pull Active Low V_{OL} vs V_{DD}

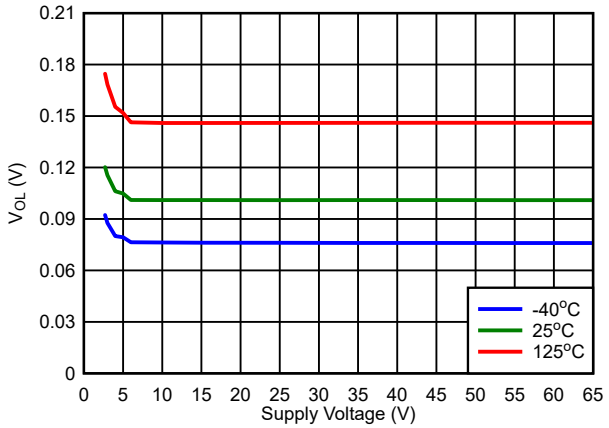


図 7-19. Push-Pull Active High V_{OL} vs V_{DD}

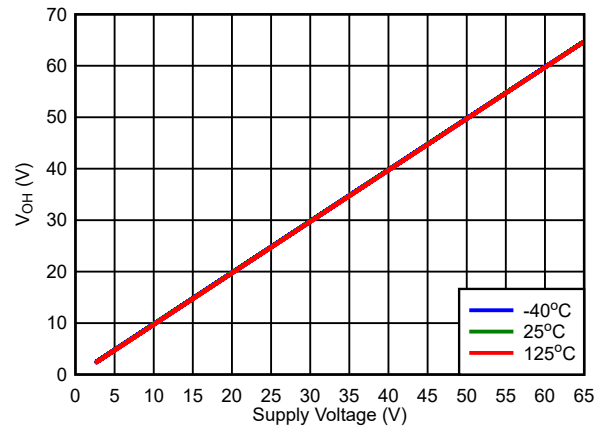


図 7-20. Push-Pull Active Low V_{OH} vs V_{DD}

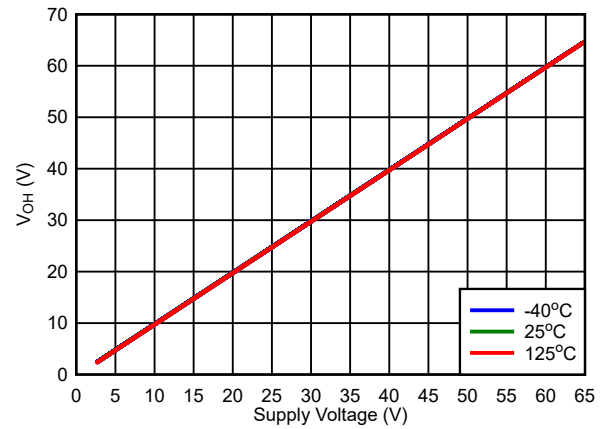


図 7-21. Push-Pull Active High V_{OH} vs V_{DD}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS37 device. Test conditions are T_A = 25°C, R_{PU} = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

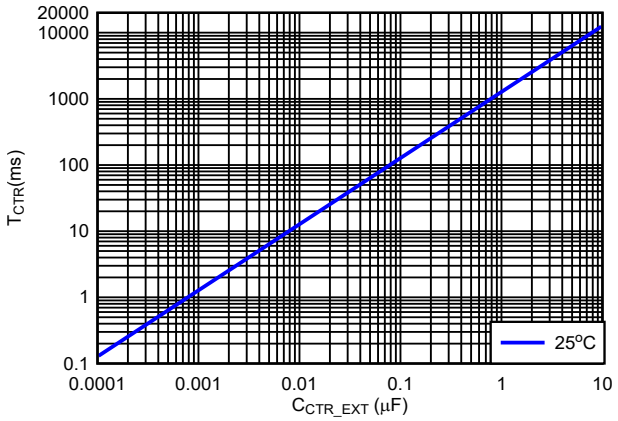


図 7-22. T_{CTR} vs C_{CTR}

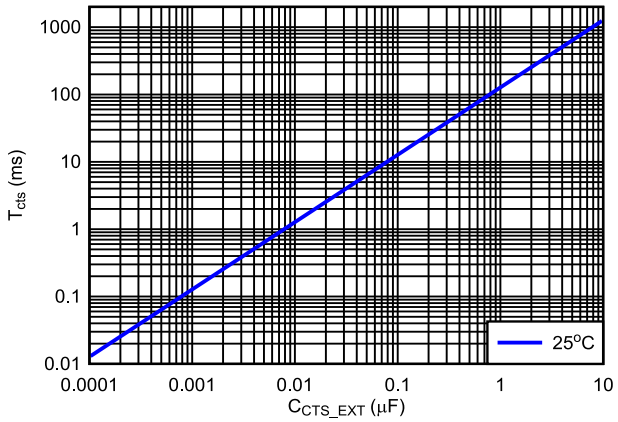


図 7-23. T_{CTS} vs C_{CTS}

8 Detailed Description

8.1 Overview

The TPS37 is a family of high voltage and low quiescent current reset IC with fixed threshold voltage. Voltage divider is integrated to eliminate the need for external resistors and eliminate leakage current that comes with resistor dividers. However, it can also support external resistor if required by application, the lowest threshold 800 mV (bypass internal resistor ladder) is recommenced for external resistors use case to take advantage of faster detection time and lower I_{SENSE} current.

VDD, SENSE and RESET pins can support 65 V continuous operation; both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while SENSE pins are connected to a higher voltage. One thing of note, the TPS37 does not have clamps within the device so external circuits or devices must be added to limit the voltages to the absolute max limit.

Additional features include programmable sense time delay (CTS1, CTS2) and reset delay time and manual reset (CTR1 / $\overline{MR}$, CTR2 / $\overline{MR}$).

8.2 Functional Block Diagram

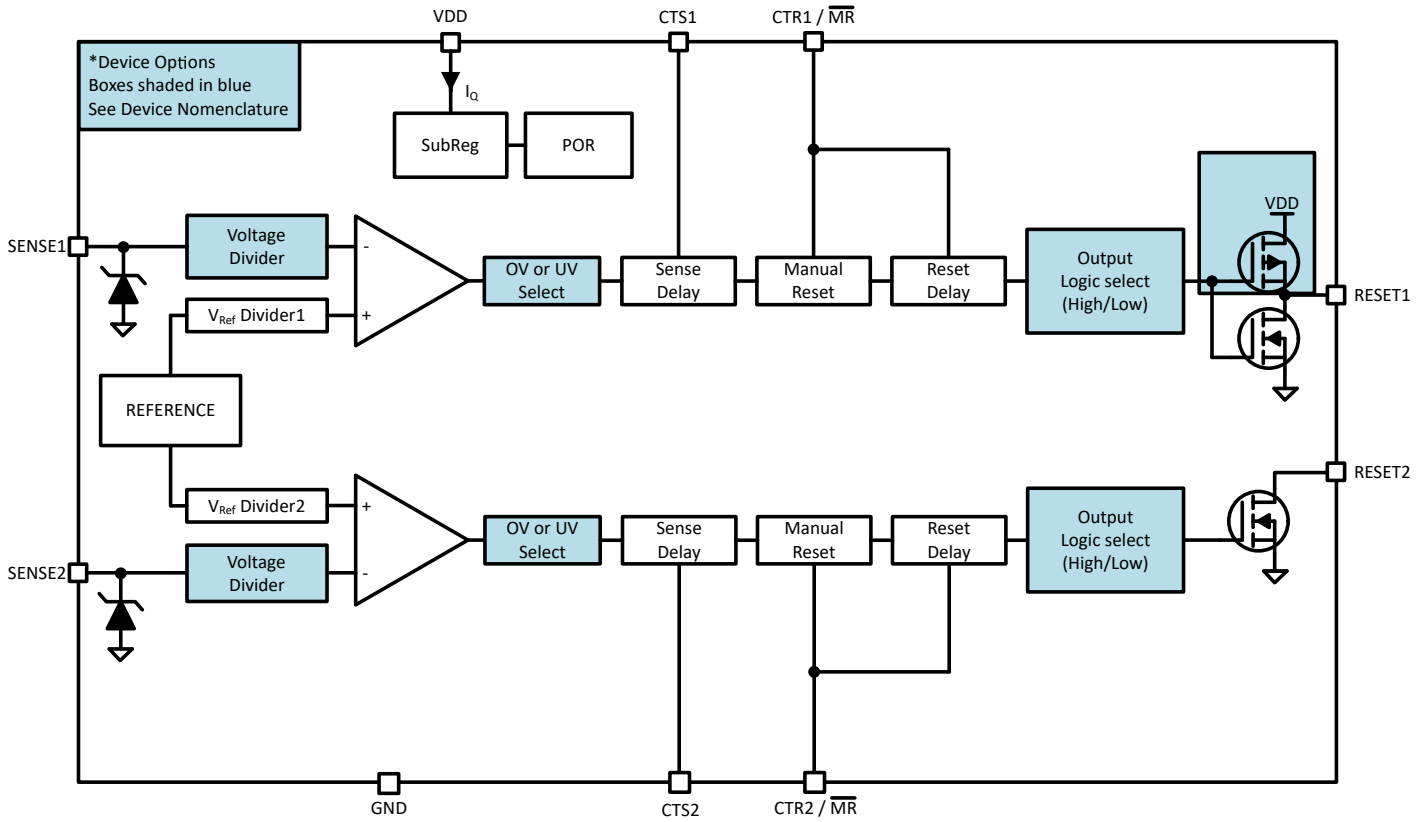


図 8-1. Functional Block Diagram [1]

[1] Refer to セクション 5 for complete list of topologies and output logic combination

8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1 µF capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET}, meaning that VDD can be higher or lower than the other pins.

8.3.1.1 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the output pins will be in reset, regardless of the voltage at SENSE pins.

8.3.1.2 Power-On Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

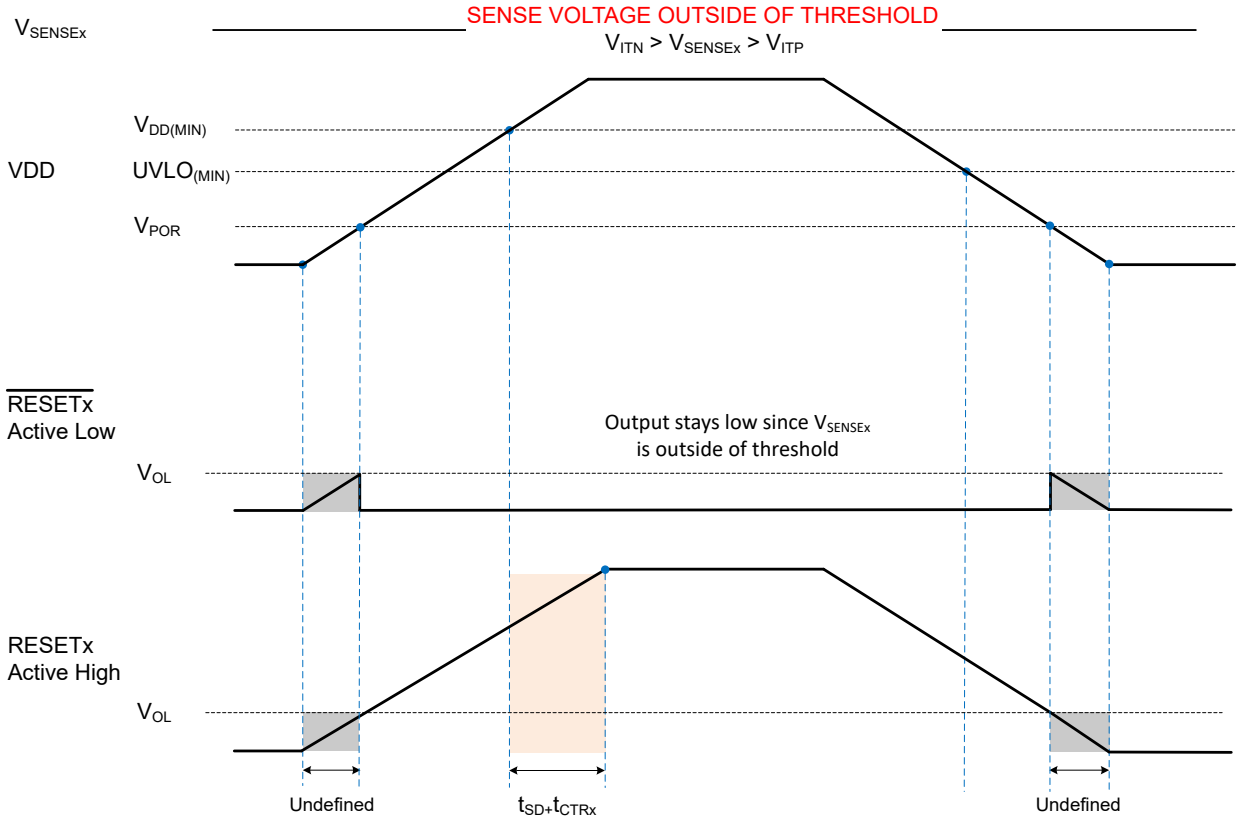


図 8-2. Power Cycle (SENSE Outside of Nominal voltage) [2]

[2] Figure assumes an external pull-up resistor is connected to the reset pin via VDD

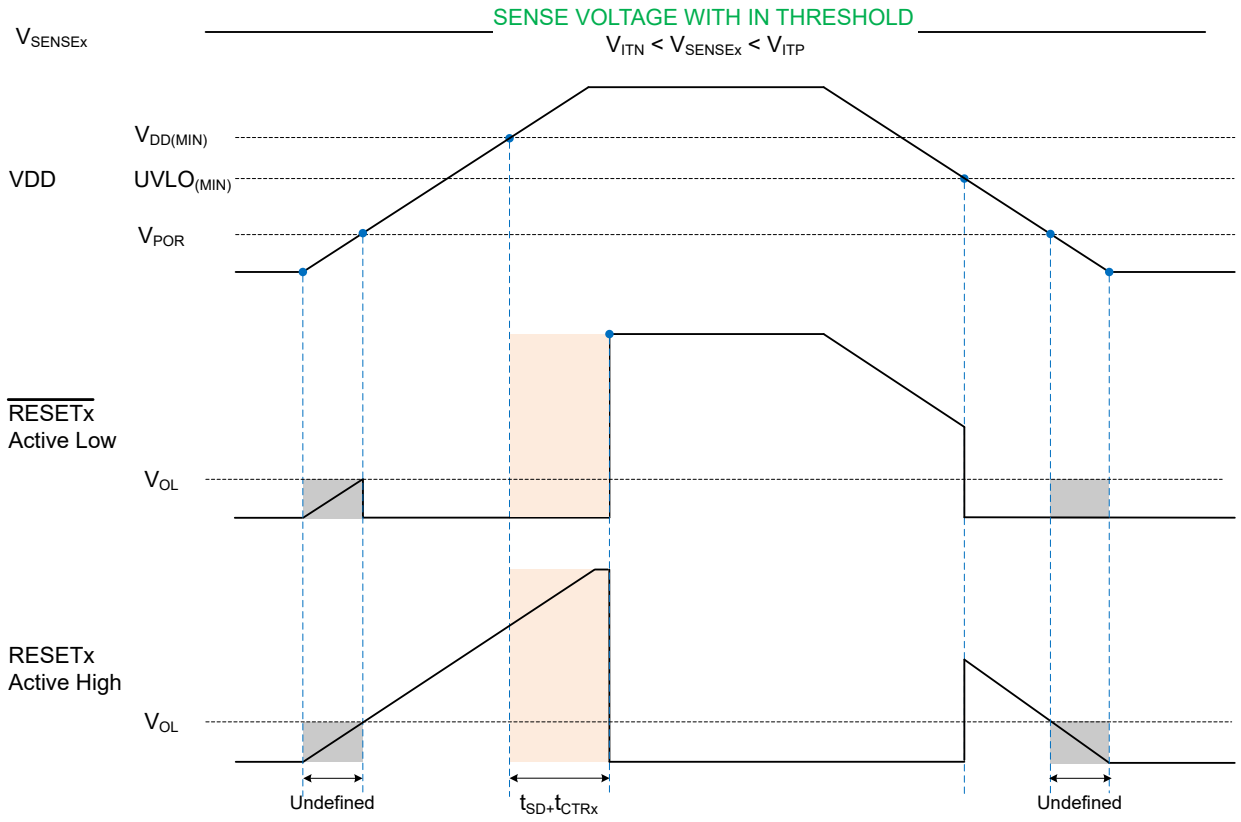


図 8-3. Power Cycle (SENSE Within Nominal voltage) [3]

[3] Figure assumes an external pull-up resistor is connected to the reset pin via VDD

8.3.2 SENSE

The TPS37 high voltage family integrates two voltage comparators, a precision reference voltage and trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Device also has built-in hysteresis that provides noise immunity and ensures stable operation.

Channels are independent of each other, meaning that SENSE1 and SENSE2 and respective outputs can be connected to different voltage rails.

Although not required in most cases, for noisy applications good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSEx inputs in order to reduce sensitivity to transient voltages on the monitored signal. SENSE1 and SENSE2 pins can be connected directly to VDD pin.

8.3.2.1 SENSE Hysteresis

Built-in hysteresis to avoid erroneous output reset release. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

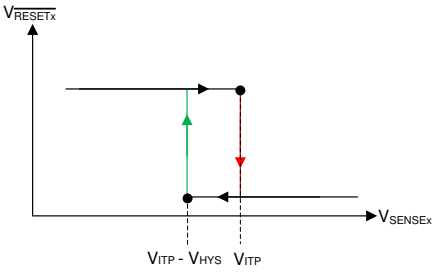


図 8-4. Hysteresis (Overvoltage Active-Low)

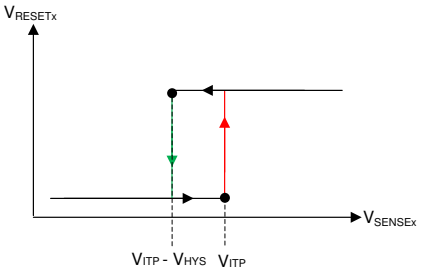


図 8-5. Hysteresis (Overvoltage Active-High)

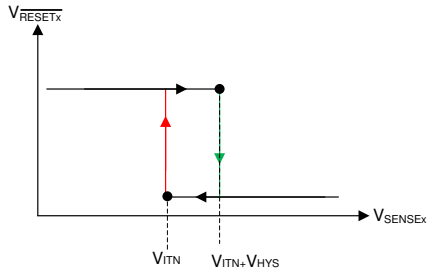


図 8-6. Hysteresis (Undervoltage Active-High)

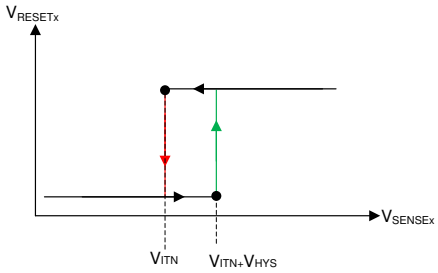


図 8-7. Hysteresis (Undervoltage Active-Low)

表 8-1. Common Hysteresis Lookup Table

TARGET			DEVICE ACTUAL HYSTERESIS OPTION
DETECT THRESHOLD	TOPOLOGY	RELEASE VOLTAGE (V)	
18.0 V	Overvoltage	17.5 V	-3%
18.0 V	Overvoltage	16.0 V	-11%
17.0 V	Overvoltage	16.5 V	-3%
16.0 V	Overvoltage	15.0 V	-6%
15.0 V	Overvoltage	14.0 V	-7%
6.0 V	Undervoltage	6.5 V	0.5 V
5.5 V	Undervoltage	6 V	0.5 V
8 V	Undervoltage	9 V	1 V
5 V	Undervoltage	7.5 V	2.5 V

表 8-1 shows a sample of hysteresis and voltage options for the TPS37. For threshold voltages ranging from 2.7 V to 8 V, one option is to select a fixed hysteresis value ranging from 0.5 V to 2.5 V in increments of 0.5 V. Additionally, a second option can be selected where the hysteresis value is a percentage of the threshold voltage. The percentage of voltage hysteresis ranges from 2% to 13%.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is ($V_{ITN(UV)}$ + V_{HYS}) and for the overvoltage (OV) channel is ($V_{ITP(OV)}$ - V_{HYS}). For a visual understanding of the UV and OV release voltage, see SENSEx Undervoltage (UV) Timing Diagram and SENSEx Overvoltage (OV) Timing Diagram. The accuracy of the release voltage, or stated in the セクション 7.5 as *Hysteresis Accuracy* is ±1.5%. Expanding what is shown in 表 8-1, below are a few voltage hysteresis examples that include the hysteresis accuracy:

Undervoltage (UV) Channel

V_{ITN} = 0.8 V

Voltage Hysteresis (V_{HYS}) = 5% = 40 mV

Hysteresis Accuracy = ±1.5% = 39.4 mV or 40.6 mV

Release Voltage = V_{ITN} + V_{HYS} = 839.4 mV to 840.6 mV

Overvoltage (OV) Channel

V_{ITP} = 8 V

Voltage Hysteresis (V_{HYS}) = 2 V

Hysteresis Accuracy = ±1.5% = 1.97 V or 2.03 V

Release Voltage = V_{ITP} - V_{HYS} = 5.97 V to 6.03 V

8.3.3 Output Logic Configurations

TPS37 has two channels with separate sense pins and reset pins that can be configured independently of each other. Channel 1 is available as Open-Drain and Push-Pull while channel 2 is only available as Open-Drain topology.

The available output logic configuration combinations are shown in 表 8-2.

表 8-2. TPS37 Output Logic

DESCRIPTION	NOMENCLATURE	VALUE	
GPN	**TPS37 (+ topology)**	**CHANNEL 1**	**CHANNEL 2**
Topology (OV and UV only) both channels are either OV or UV • UV = Undervoltage • OV = Overvoltage • PP = Push-Pull • OD = Open-Drain • L = Active low • H = Active high	TPS37A	OV OD L	UV OD L
	TPS37B	OV PP H	UV OD L
	TPS37C	OV OD L	UV OD H
	TPS37D	OV PP H	UV OD H
	TPS37E	OV OD H	UV OD H
	TPS37F	OV OD H	UV OD L
	TPS37G	OV PP L	UV OD H
	TPS37H	OV PP L	UV OD L

8.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the (I_{lkg}) current provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS37 open-drain output pin.

8.3.3.2 Push-Pull

Push-Pull output does not require an external resistor since is the output is internally pulled-up to VDD during V_{OH} condition and output will be connected to GND during V_{OH} condition.

8.3.3.3 Active-High (RESET)

RESET (active-high), denoted with no bar above the pin label. RESET remains low (V_{OL}, deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.3.4 Active-Low ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ (active low) denoted with a bar above the pin label. $\overline{\text{RESET}}$ remains high voltage (V_{OH}, deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.4 User-Programmable Reset Time Delay

TPS37 has adjustable reset release time delay with external capacitors. Channel timing are independent of each other.

- A capacitor in CTR1 / $\overline{MR}$ program the reset time delay of Output 1.
- A capacitor in CTR2 / $\overline{MR}$ program the reset time delay of Output 2.
- No capacitor on these pins gives the fastest reset delay time indicated in the セクション 7.6.

8.3.4.1 Reset Time Delay Configuration

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR1 pin and GND, CTR2 for channel 2. In this section CTRx represent either channel 1 or channel 2.

The relationship between external capacitor $C_{CTRx\_EXT\ (typ)}$ and the time delay $t_{CTRx\ (typ)}$ is given by 式 1.

$$t_{CTRx\ (typ)} = -\ln(0.28) \times R_{CTRx\ (typ)} \times C_{CTRx\_EXT\ (typ)} + t_{CTRx\ (no\ cap)} \quad (1)$$

$R_{CTRx\ (typ)}$ = is in kilo ohms (kOhms)

$C_{CTRx\_EXT\ (typ)}$ = is given in microfarads (µF)

$t_{CTRx\ (typ)}$ = is the reset time delay (ms)

The reset delay varies according to three variables: the external capacitor (C_{CTRx_EXT}), CTR pin internal resistance (R_{CTRx}) provided in セクション 7.5, and a constant. The minimum and maximum variance due to the constant is show in 式 2 and 式 3:

$$t_{CTRx\ (min)} = -\ln(0.31) \times R_{CTRx\ (min)} \times C_{CTRx\_EXT\ (min)} + t_{CTRx\ (no\ cap\ (min))} \quad (2)$$

$$t_{CTRx\ (max)} = -\ln(0.25) \times R_{CTRx\ (max)} \times C_{CTRx\_EXT\ (max)} + t_{CTRx\ (no\ cap\ (max))} \quad (3)$$

The recommended maximum reset delay capacitor for the TPS37 is limited to 10 µF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 5% of the programmed reset time delay.

8.3.5 User-Programmable Sense Delay

TPS37 has adjustable sense release time delay with external capacitors. Channel timing are independent of each other. Sense delay is used as a de-glitcher or ignoring known transients.

- A capacitor in CTS1 program the excursion detection on SENSE1.
- A capacitor in CTS2 program the excursion detection on SENSE2.
- No capacitor on these pins gives the fastest detection time indicated in the セクション 7.6.

8.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS1 pin and GND, CTS2 for channel 2. In this section CTSx represent either channel 1 or channel 2.R

The relationship between external capacitor $C_{CTSx\_EXT\ (typ)}$ and the time delay $t_{CTSx\ (typ)}$ is given by 式 4.

$$t_{CTSx\ (typ)} = -\ln(0.28) \times R_{CTSx\ (typ)} \times C_{CTSx\_EXT\ (typ)} + t_{CTSx\ (no\ cap)} \quad (4)$$

R_{CTSx} = is in kilo ohms (kOhms)

C_{CTSX_EXT} = is given in microfarads (µF)

t_{CTSx} = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTSx_EXT}), CTS pin internal resistance (R_{CTSx}) provided in セクション 7.5, and a constant. The minimum and maximum variance due to the constant is show in 式 5 and 式 6:

$$t_{CTSx\ (min)} = -\ln(0.31) \times R_{CTSx\ (min)} \times C_{CTSx\_EXT\ (min)} + t_{CTSx\ (no\ cap\ (min))} \quad (5)$$

$$t_{CTSx\ (max)} = -\ln(0.25) \times R_{CTSx\ (max)} \times C_{CTSx\_EXT\ (max)} + t_{CTSx\ (no\ cap\ (max))} \quad (6)$$

The recommended maximum sense delay capacitor for the TPS37 is limited to 10 µF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time between fault events to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or time duration between fault events needs to be greater than 10% of the programmed sense time delay.

8.3.6 Manual RESET (CTR1 / $\overline{MR}$) and (CTR2 / $\overline{MR}$) Input

The manual reset input allows a processor or other logic circuits to initiate a reset. In this section $\overline{MR}$ is a generic reference to (CTR1 / $\overline{MR}$) and (CTR2 / $\overline{MR}$). A logic low on $\overline{MR}$ causes $\overline{RESET1}$ to assert on reset output. After $\overline{MR}$ is left floating, $\overline{RESET1}$ will release the reset if the voltage at SENSE1 pin is at nominal voltage. $\overline{MR}$ should not be driven high, this pin should be left floating or connected to a capacitor to GND, this pin can be left unconnected if is not used.

If the logic driving the $\overline{MR}$ cannot tri-state (floating and GND) then a logic-level FET should be used as illustrated in 図 8-8.

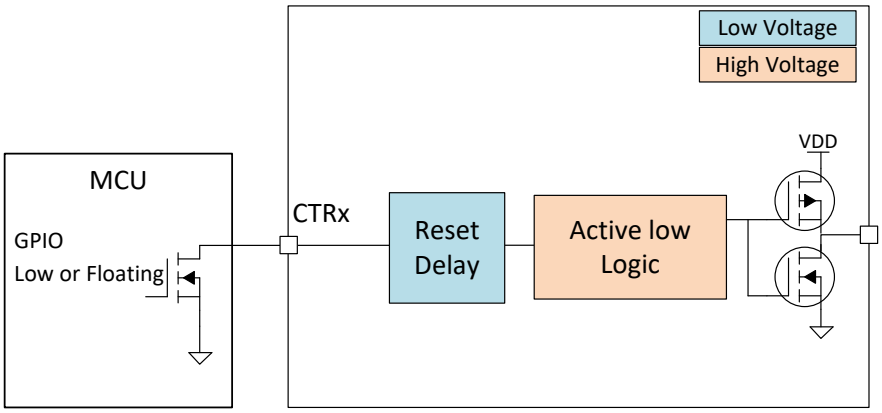


図 8-8. Manual Reset Implementation

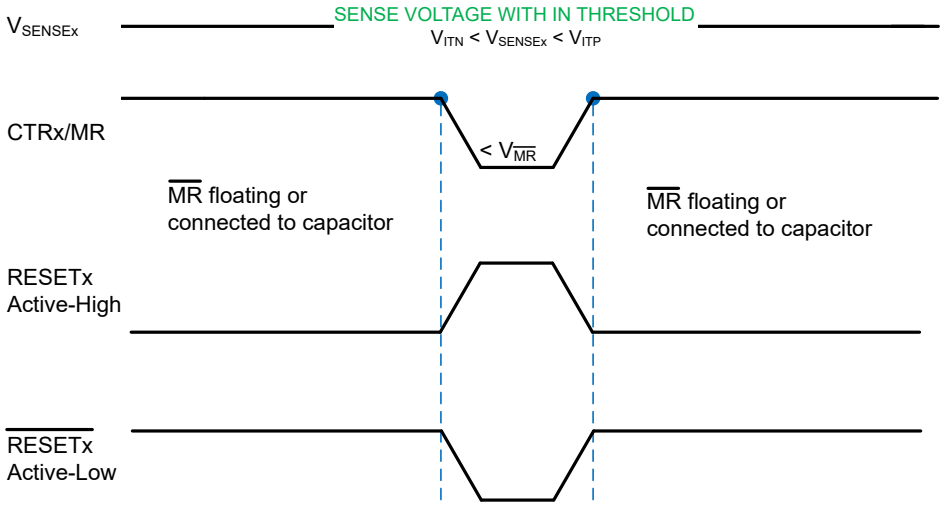


図 8-9. Manual Reset Timing Diagram

表 8-3. $\overline{MR}$ Functional Table

$\overline{MR}$	SENSE ON NOMINAL VOLTAGE	RESET STATUS
Low	Yes	Reset asserted
Floating	Yes	Fast reset release when SENSE voltage goes back to nominal voltage
Capacitor	Yes	Programmable reset time delay
High	Yes	NOT Recommended

9 Device Functional Modes

表 9-1. Undervoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR (1) / $\overline{MR}$ PIN	VDD PIN	OUTPUT (2) ($\overline{RESET}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Undervoltage Detection	SENSE > $V_{ITN(UV)}$	SENSE < $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Undervoltage Detection	SENSE < $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Normal Operation	SENSE < $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$ + HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Manual Reset	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Low	V_{DD} > $V_{DD(MIN)}$	Low
UVLO Engaged	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{POR} < V_{DD} < $V_{DD(MIN)}$	Low
Below V_{POR}, Undefined Output	SENSE > $V_{ITN(UV)}$	SENSE > $V_{ITN(UV)}$	Open or capacitor connected	V_{DD} < V_{POR}	Undefined

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

表 9-2. Overvoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR (1) / $\overline{MR}$ PIN	VDD PIN	OUTPUT (2) ($\overline{RESET}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Overvoltage Detection	SENSE < $V_{ITN(OV)}$	SENSE > $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Overvoltage Detection	SENSE > $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Normal Operation	SENSE > $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$ - HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Manual Reset	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Low	V_{DD} > $V_{DD(MIN)}$	Low
UVLO Engaged	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{POR} < V_{DD} < UVLO	Low
Below V_{POR}, Undefined Output	SENSE < $V_{ITN(OV)}$	SENSE < $V_{ITN(OV)}$	Open or capacitor connected	V_{DD} < V_{POR}	Undefined

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Adjustable Voltage Thresholds

式 7 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored V_{MON} for undervoltage (UV) using channel 2 of the TPS37A010122DSKR variant. Using 式 7 and shown in 図 10-1, R_1 is the top resistor of the resistor divider that is between V_{MON} and V_{SENSE2}, R_2 is the bottom resistor that is between V_{SENSE2} and GND, V_{MON} is the voltage rail that is being monitored and V_{SENSE2} is the input threshold voltage. The monitored UV threshold, denoted as V_{MON-}, where the device will assert a reset signal occurs when $V_{SENSE2} = V_{IT-(UV)}$ or, for this example, V_{MON-} = 10.8V which is 90% from 12 V. Using 式 7 and assuming R_2 = 10kΩ, R_1 can be calculated shown in 式 8 where I_{R1} is represented in 式 9:

$$V_{SENSE2} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

$$R_1 = (V_{MON-} - V_{SENSE2}) \div I_{R1} \quad (8)$$

$$I_{R1} = I_{R2} = V_{SENSE2} \div R_2 \quad (9)$$

Substituting 式 9 into 式 8 and solving for R_1 in 式 7, R_1 = 125kΩ. The TPS37A010122DSKR is typically meant to monitor a 0.8 V rail with ±2% voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} would need to go above V_{IT-} + V_{HYS}. For this example, V_{MON} = 11.016 V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance R_{SENSE} can be calculated by the SENSE voltage V_{SENSE} divided by the SENSE current I_{SENSE} as shown in 式 11. V_{SENSE} can be calculated using 式 7 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using 式 10.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (10)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (11)$$

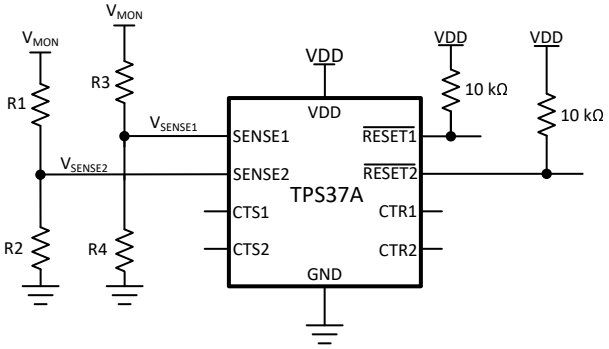


図 10-1. Adjustable Voltage Threshold with External Resistor Dividers

10.1.1 Application Curves

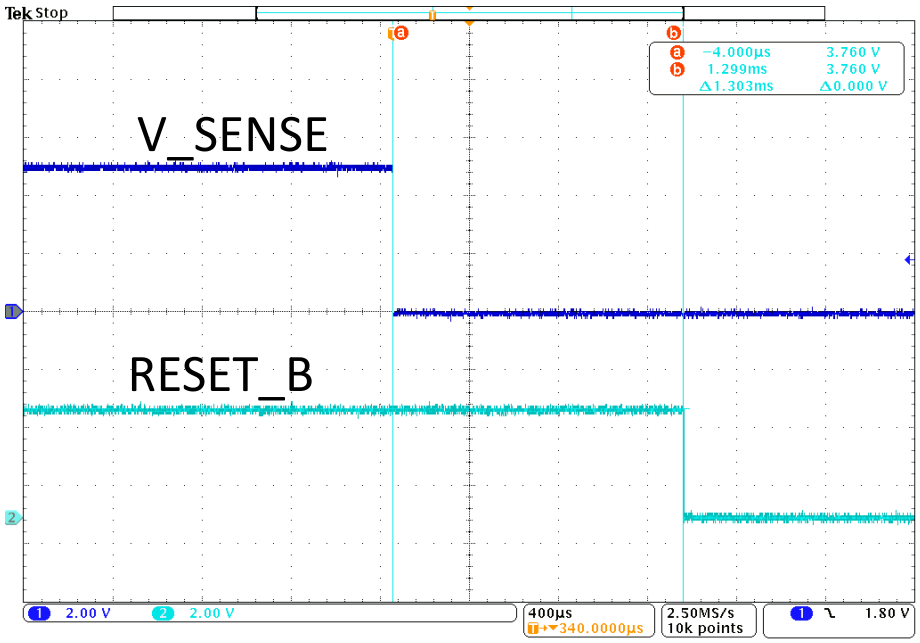


図 10-2. Undervoltage Reset Waveform

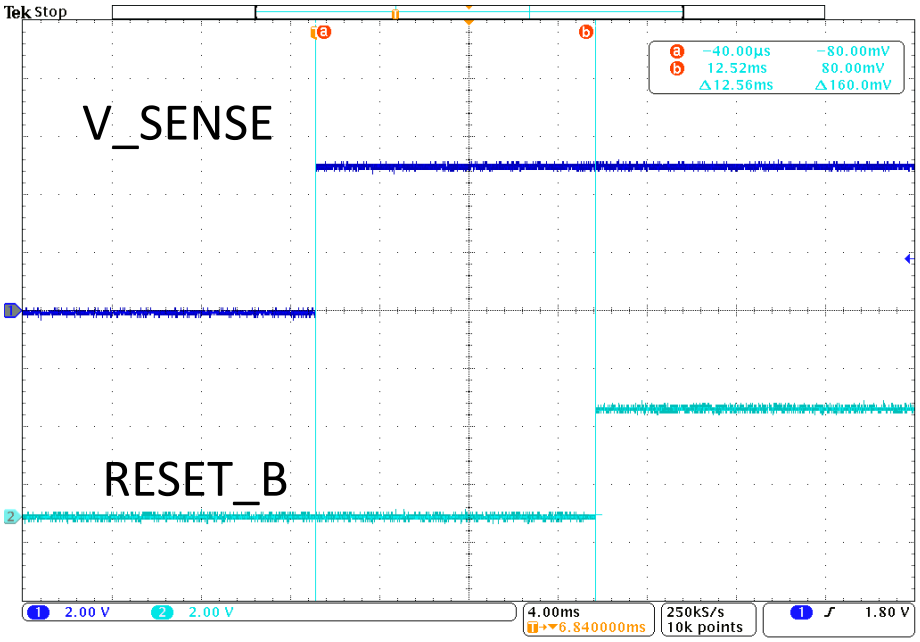


図 10-3. Undervoltage Recovery Waveform

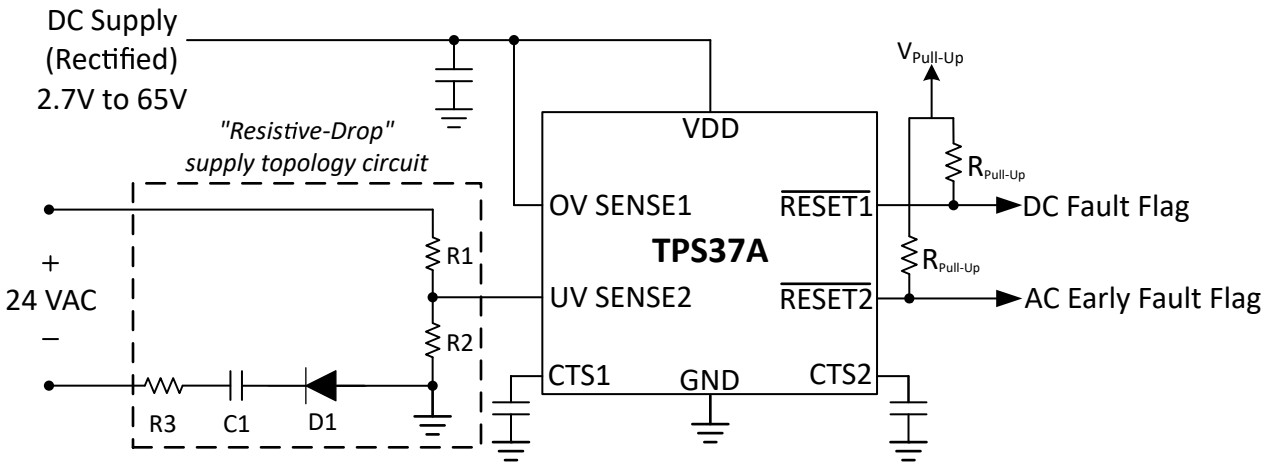
10.2 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

10.2.1 Typical Application

10.2.1.1 Design 1: High Voltage – Fast AC Signal Monitoring For Power Fault Detection

In many industrial and factory automation applications, there are multiple power rails that power various subsystems within the application. Some of these power rails include 24 / 48 VAC AC sources with a known operating frequency that requires a full-bridge rectifier and capacitors to convert its signal to a DC voltage where it can be monitored by a voltage supervisor. One drawback with the described conversion is the response time of the DC voltage when the AC power rail experiences a change of operating frequency or voltage amplitude. Due to the output filter of the full-bridge rectifier, the detection in the change of voltage or operating frequency may require several AC cycles before the voltage supervisor outputs a fault condition. The direct monitoring of the AC source by using a “Resistive-Drop” supply topology circuit provides the user a fast transient fault detection. In this design example, the TPS37A is being highlighted with the ability to offer a unique “window operating” solution by monitoring the output of the AC source for over or undervoltage operation.



* The circuit solution is not isolated and one must take into account when planning to use in high power systems.

図 10-4. Sensing an AC Signal for Power Fault Detection

10.2.1.1.1 Design Requirements

This design requires voltage supervision on an AC, with a known operating frequency, power supply rail. The overvoltage fault sensing is achieved by monitoring the DC output of a full bridge rectifier while the undervoltage fault is detected by inputting a half wave signal and its voltage frequency and magnitude are being monitored. The target output of this TPS37A application is for 5 V reset logic.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 24 VAC 800 Hz power supply for undervoltage and overvoltage conditions. Trigger undervoltage fault at 5 V and overvoltage fault at 24 V.	TPS37A provides voltage monitoring with 1.5% max accuracy with adjustable/non-adjustable variations.
Maximum Input Voltage	Operate with power supply input up to 34 V.	The TPS37A can support a VDD of up to 65 V.
Output logic voltage	Open-Drain Output Topology	An open-drain output is recommended to provide the a 5 V reset signal.
SENSE Delay when a fault is detected	$\overline{\text{RESET}}$ delay of at least 0.625 ms which is the time between half wave cycles	C_{CTS2} = 5.6 nF sets 717 µs delay
Voltage Monitor Accuracy	Maximum voltage monitor accuracy of 1.5%.	The TPS37A has 1.5% maximum voltage monitor accuracy.

10.2.1.1.2 Detailed Design Procedure

The main advantage of this unique application is being able to monitor a single AC source with a known operating frequency AC source rail. Because the TPS37A is an over and undervoltage detector with delay

function, detecting faults either from a change of operating frequency range or voltage amplitude of the AC source is achievable.

図 10-4 illustrates an example of how the TPS37A is monitoring an AC source. Input to SENSE1 of TPS37A is monitoring a full wave rectifier DC signal. The DC signal is the result from the rectification of the 24 VAC source and monitors the AC source for overvoltage events due to a change of voltage amplitude or an increase to operating frequency. Input to SENSE2 of TPS37A will monitor the AC source by using a "resistive-drop" supply topology circuit. The unique circuit resistively divides the AC voltage signal and provides only the positive half wave 図 10-5 into SENSE2 input. The half wave signal does not go through any output filter and hence any change to the AC voltage or operating frequency can be rapidly detected. Knowing the operating frequency of the AC source and converting to the time domain, the TPS37A SENSE2 delay can be programmed, by the capacitor on CTS2 pin, to equal or be greater than one-half of the operating period (the frequency of the half wave rectification signal) or the half cycle shown in 図 10-5. When the half wave voltage amplitude falls below the SENSE2 threshold voltage, the SENSE2 time delay counter begins to increment. If the next half wave voltage amplitude exceeds the SENSE2 threshold voltage, the SENSE2 time delay counter will reset and the TPS37A $\overline{\text{RESET2}}$ pin will indicate no fault was detected. Conversely, if the voltage amplitude of the half wave does not reach the SENSE2 threshold voltage within the programmed time delay of t_{CTS}, a fault will occur. Also, a fault can occur if the operating frequency from the AC source decreases, resulting in lower AC voltage amplitude at the programmed time delay t_{CTS}.

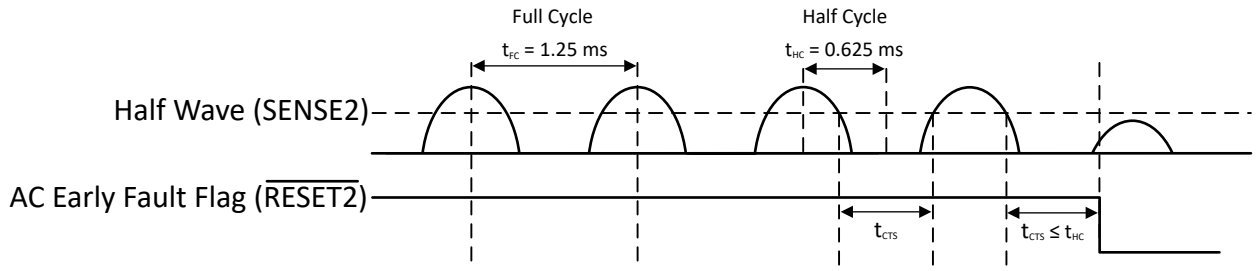


図 10-5. Design 2 Timing Diagram

The TPS37A, with its ability of having a wide VDD range from 2.7 V to 65 V and under and overvoltage detection, offers a unique “window operating” AC power rail monitoring solution. Combining SENSE delay feature with the "resistive-drop" supply circuitry, detecting an undervoltage event on the half cycle of the AC power rail provides a fast power fault response. Likewise, the TPS37A provides an overvoltage monitoring and SENSE delay fault detection for the same AC power rail. With under and overvoltage supervision of the AC power rail, applications needing a specific operating DC range to protect its subsystems is achieve through TPS37A. Good design practice recommends using a 0.1-µF capacitor on the VDD pin and this capacitance may need to increase if using an adjustable version with a resistor divider.

Note that this design solution is not isolated and one must take into account when planning to use in high power systems.

10.3 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.4 V (V_{POR}) to 65 V (max operation). Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin.

10.3.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using 式 12:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} – T_A) / R_{\theta JA}) \quad (12)$$

The actual power being dissipated in the device can be represented by 式 13:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} \quad (13)$$

p_{RESET} is calculated by 式 14 or 式 15

$$p_{RESET\ (PUSHPULL)} = VDD - V_{RESET} \times I_{RESET} \quad (14)$$

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \quad (15)$$

式 12 and 式 13 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be de-rated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by 式 16:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (16)$$

10.4 Layout

10.4.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSEx pins, placing a 10 nF to 100 nF capacitor between the SENSEx pins and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS1, CTS2, CTR1, or CTR2, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- For open-drain variants, place the pull-up resistors on $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ pins as close to the pins as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).

- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

10.4.2 Layout Example

The DSK layout example in 図 10-6 shows how the TPS37 is laid out on a printed circuit board (PCB) with user-defined delays.

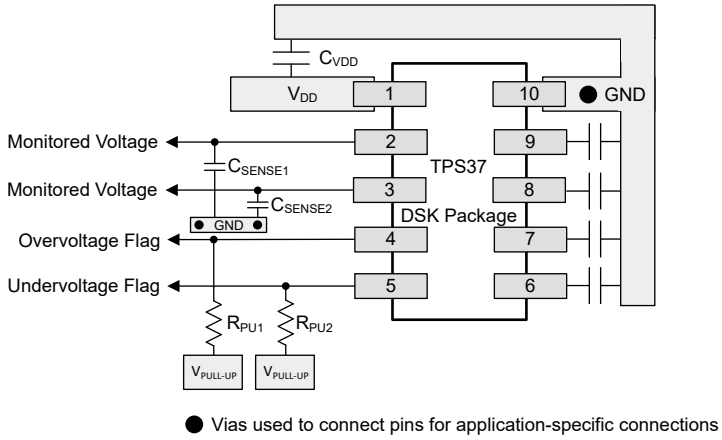


図 10-6. TPS37 DSK Package Recommended Layout

The DYY layout example in 図 10-7 shows how the TPS37 is laid out on a printed circuit board (PCB) with user-defined delays.

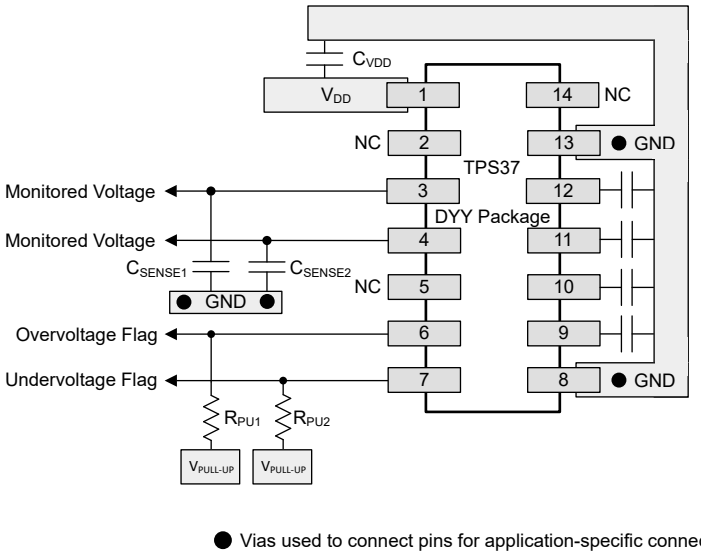


図 10-7. TPS37 DYY Package Recommended Layout

10.4.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in 図 10-8 the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

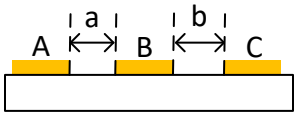


図 10-8. Creepage Distance

図 10-8 details:

- A = Left pins (high voltage)
- B = Central pad (not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltage)
- Creepage distance = a + b

11 Device and Documentation Support

11.1 Device Nomenclature

セクション 5 shows how to decode the function of the device based on its part number

表 11-1 shows TPS37 possible voltage options per channel. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

表 11-1. Voltage Options

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS
01	800 mV (divider bypass)	**70**	7.0 V	**A0**	10.4 V	**D0**	20.5 V	**F0**	31.0 V
27	2.7 V	**71**	7.1 V	**A1**	10.8 V	**D1**	21.0 V	**F1**	32.0 V
28	2.8 V	**72**	7.2 V	**A2**	11.2 V	**D2**	21.5 V	**F2**	33.0 V
29	2.9 V	**73**	7.3 V	**A3**	11.6 V	**D3**	22.0 V	**F3**	34.0 V
30	3.0 V	**74**	7.4 V	**A4**	12.0 V	**D4**	22.5 V	**F4**	35.0 V
31	3.1 V	**75**	7.5 V	**A5**	12.4 V	**D5**	23.0 V	**F5**	36.0 V
32	3.2 V	**76**	7.6 V	**A6**	12.8 V	**D6**	23.5 V		
33	3.3 V	**77**	7.7 V	**A7**	13.2 V	**D7**	24.0 V		
34	3.4 V	**78**	7.8 V	**A8**	13.6 V	**D8**	24.5 V		
35	3.5 V	**79**	7.9 V	**A9**	14.0 V	**D9**	25.0 V		
36	3.6 V	**80**	8.0 V	**B0**	14.4 V	**E0**	25.5 V		
37	3.7 V	**81**	8.1 V	**B1**	14.8 V	**E1**	26.0 V		
38	3.8 V	**82**	8.2 V	**B2**	15.2 V	**E2**	26.5 V		
39	3.9 V	**83**	8.3 V	**B3**	15.6 V	**E3**	27.0 V		
40	4.0 V	**84**	8.4 V	**B4**	16.0 V	**E4**	27.5 V		
41	4.1 V	**85**	8.5 V	**B5**	16.4 V	**E5**	28.0 V		
42	4.2 V	**86**	8.6 V	**B6**	16.8 V	**E6**	28.5 V		
43	4.3 V	**87**	8.7 V	**B7**	17.2 V	**E7**	29.0 V		
44	4.4 V	**88**	8.8 V	**B8**	17.6 V	**E8**	29.5 V		
45	4.5 V	**89**	8.9 V	**B9**	18.0 V	**E9**	30.0 V		
46	4.6 V	**90**	9.0 V	**C0**	18.4 V				
47	4.7 V	**91**	9.1 V	**C1**	18.8 V				
48	4.8 V	**92**	9.2 V	**C2**	19.2 V				
49	4.9 V	**93**	9.3 V	**C3**	19.6 V				
50	5.0 V	**94**	9.4 V	**C4**	20.0 V				
51	5.1 V	**95**	9.5 V						
52	5.2 V	**96**	9.6 V						
53	5.3 V	**97**	9.7 V						
54	5.4 V	**98**	9.8 V						
55	5.5 V	**99**	9.9 V						
56	5.6 V	**00**	10.0 V						
57	5.7 V								
58	5.8 V								
59	5.9 V								
60	6.0 V								

表 11-1. Voltage Options (continued)

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS	NOMEN-CLATURE	VOLTAGE OPTIONS
61	6.1 V								
62	6.2 V								
63	6.3 V								
64	6.4 V								
65	6.5 V								
66	6.6 V								
67	6.7 V								
68	6.8 V								
69	6.9 V								

11.2 サポート・リソース

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11.3 Trademarks

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11.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS37A010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2KAL	Samples
TPS37B010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2K8L	Samples
TPS37E010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32HL	Samples
TPS37F010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2K9L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS37 :

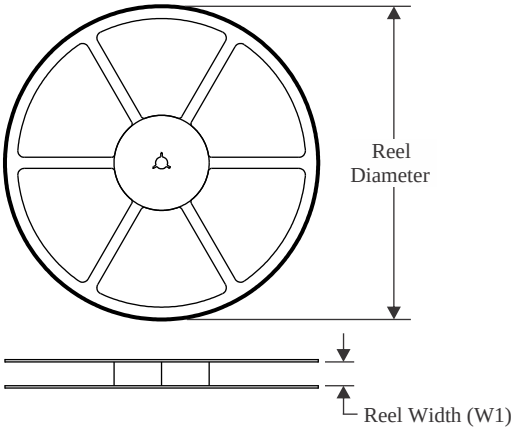
- Automotive : TPS37-Q1

NOTE: Qualified Version Definitions:

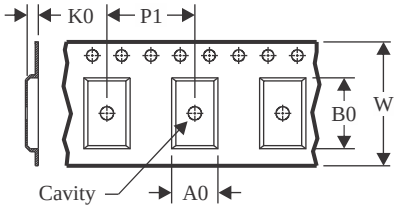
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

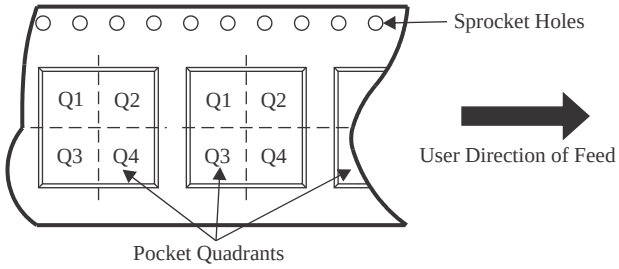


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

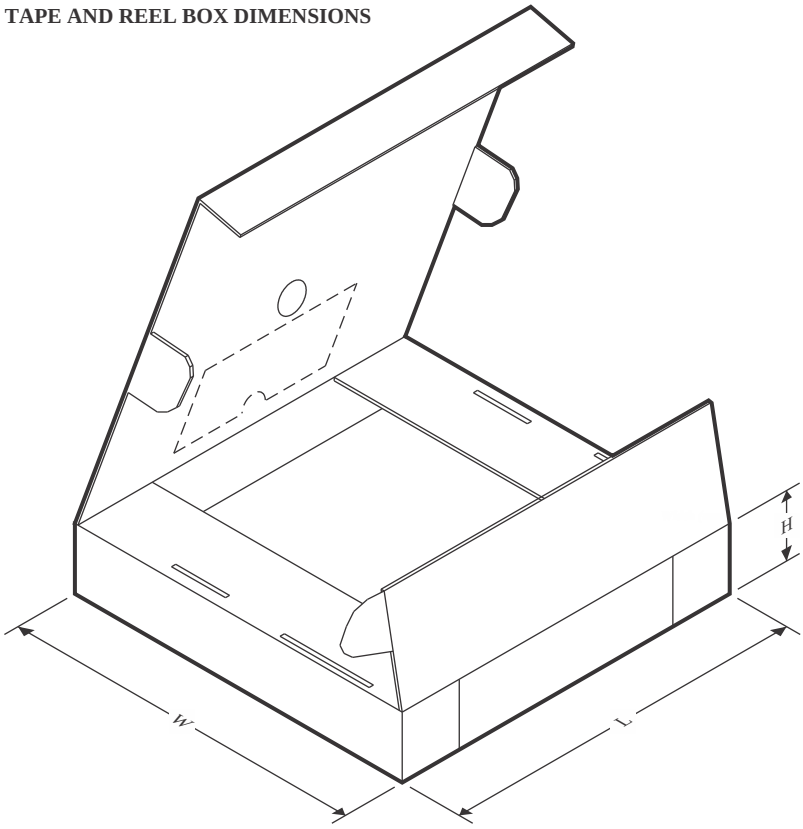
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS37A010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS37B010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS37E010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS37F010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



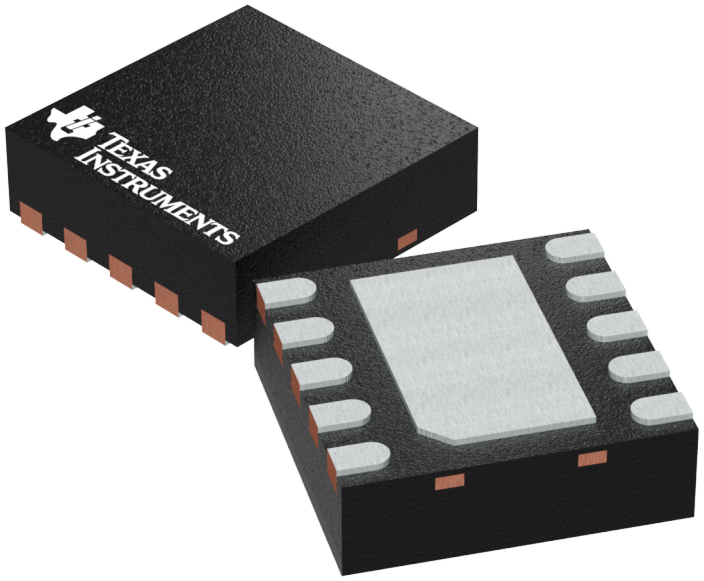
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS37A010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0
TPS37B010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0
TPS37E010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0
TPS37F010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0

DSK 10 WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



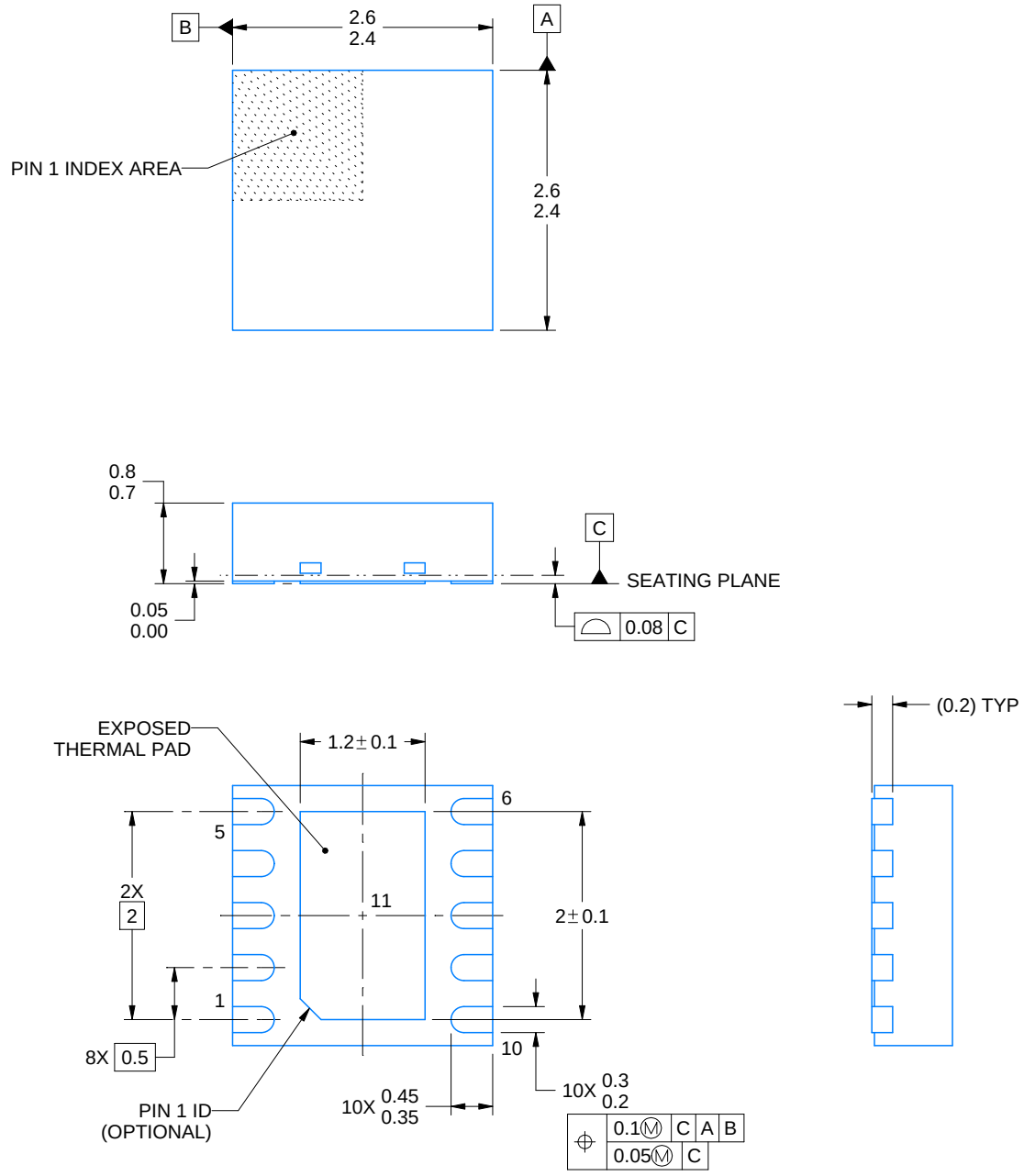
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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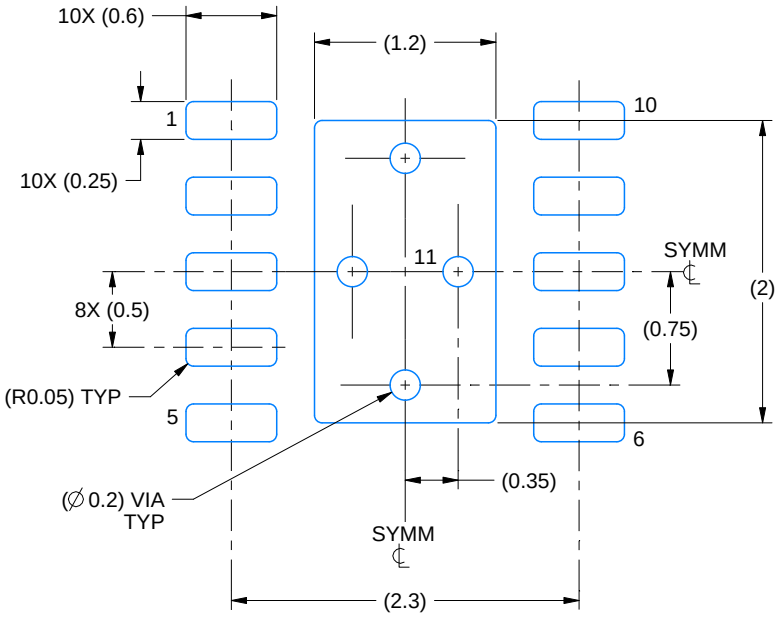
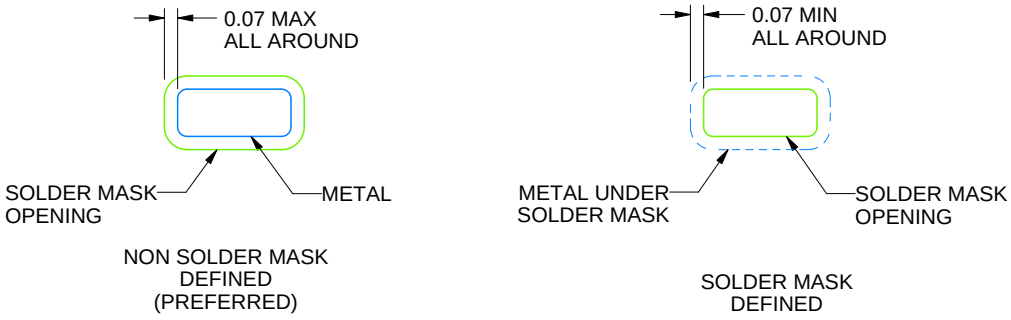
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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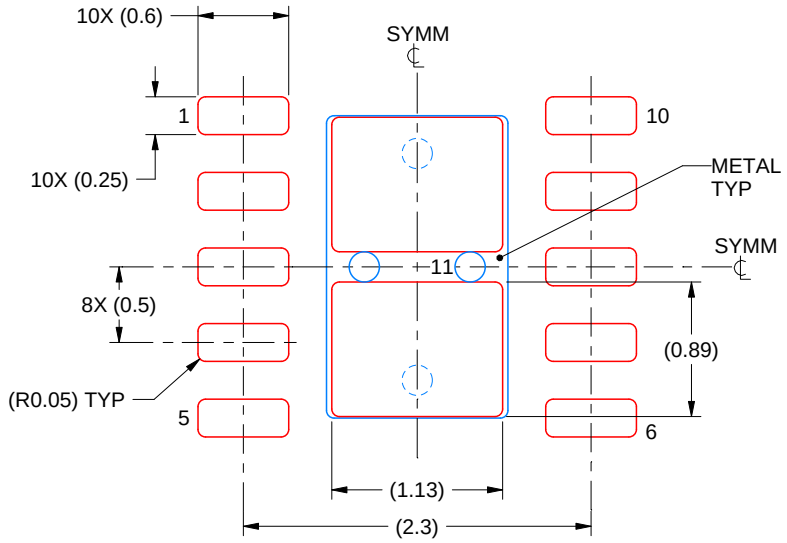
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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