TEXAS INSTRUMENTS
TPS3703
JAJSJ13B – MAY 2020 – REVISED NOVEMBER 2020

TPS3703 高精度過電圧および低電圧リセット IC、時間遅延および手動リセット搭載

1 特長

- 入力電圧範囲:1.7V～5.5V
- 低電圧誤動作防止 (UVLO):1.7V
- 低い静止電流:7µA (最大値)
- 高いスレッショルド精度:
  - ±0.25% (標準値)
  - ±0.7% (-40℃～+125℃)
- 固定ウィンドウのスレッショルド・レベル
  - 50mV 刻みで 500mV～1.3V
  - 1.5V、1.8V、2.5V、2.8V、2.9V、3.3V、5V
  - UV スレッショルドのみで利用可能
  - ±3% から ±7% までのウィンドウ許容範囲を使用可能
- 電圧スレッショルド・レベルをユーザーが変更可能
- 内部的なグリッチ耐性およびヒステリシス
- 固定時間遅延オプション:50µs、1ms、5ms、10ms、20ms、100ms、200ms
- 単一の外付けコンデンサで時間遅延をプログラム可能なオプション
- オープン・ドレイン、アクティブ Low の UV および OV モニタ
- $\overline{\text{RESET}}$ 電圧のラッチ出力モード

2 アプリケーション

- モーター・ドライブ
- ファクトリ・オートメーション / 制御
- ホーム・シアターおよびエンターテインメント
- グリッド・インフラストラクチャ
- データ・センターおよびエンタープライズ・コンピューティング

3 説明

TPS3703 デバイスは、統合された過電圧 (OV) および低電圧 (UV) の監視またはリセット IC で、業界でも最も小さい 6 ピンの DSE パッケージに搭載されています。この高精度電圧監視 IC は、低電圧電源レールで動作する、電源誤差の余地が小さいシステムに理想的です。スレッショルドのヒステリシスが小さいので、監視対象の電源電圧が通常の動作範囲内であるときに誤ってリセット信号が発生するのを防止します。内部的なグリッチ耐性およびノイズ・フィルタにより、ノイズの多い信号による誤ったリセットも回避されます。

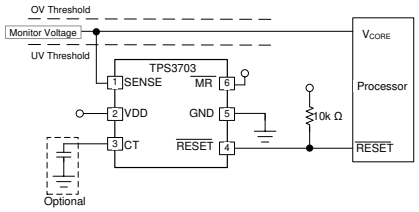
TPS3703 は、外付け抵抗なしで過電圧および低電圧リセットのスレッショルドを設定できるため、総合的な精度、コスト、ソリューション・サイズをさらに最適化でき、安全システムの信頼性も向上します。各デバイスの設計には 2 つのリセット遅延時間が設定されており、コンデンサ時間 (CT) ピンを使用してどちらかを選択できるほか、コンデンサを接続してリセット遅延を調整することもできます。SENSE 入力ピンと VDD ピンが別になっていることにより、高信頼性システムで求められる冗長性を実現できます。

このデバイスは、静止電流仕様がわずか 4.5µA です (標準値)。TPS3703 は、高精度の低電圧および過電圧監視を必要とする産業用アプリケーションおよびアプリケーションに適しています。

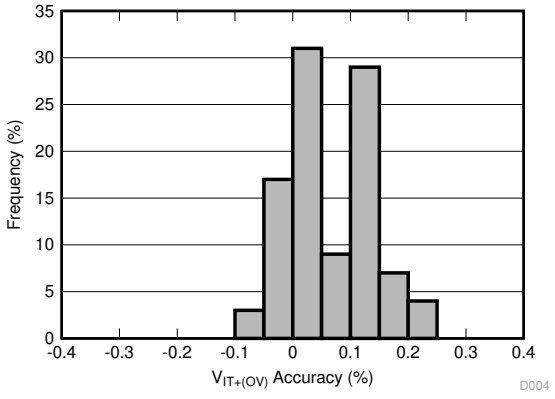
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS3703	WSON (6)	1.50mm × 1.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



過電圧および低電圧検出機能内蔵



過電圧精度の標準的な分散

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2020) to Revision B (November 2020)	Page
• Added Added V_{IT} < 800 mV threshold option to Electrical Characteristics table	6

5 Device Comparison

図 5-1 shows the device nomenclature of the TPS3703. For all possible voltages, window tolerance, time delays, and UV threshold options, see 表 12-1. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

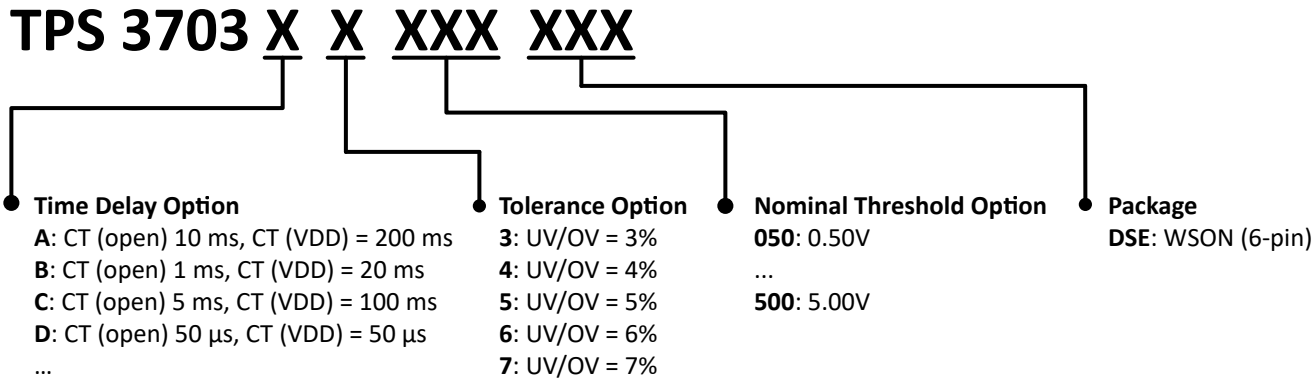


図 5-1. TPS3703 Device Nomenclature

6 Pin Configuration and Functions

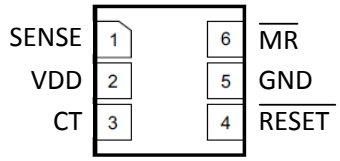


図 6-1. DSE Package
6-Pin WSON
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SENSE	I	Input for the monitored supply voltage rail. When the SENSE voltage goes above the overvoltage threshold or below the undervoltage threshold, the $\overline{\text{RESET}}$ pin is driven low. Connect to VDD pin if monitoring VDD supply voltage.
2	VDD	I	Supply voltage input pin. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.
3	CT	I	Capacitor time delay pin. The CT pin offers two fixed time delays by connecting CT pin to VDD or leaving it floating. Delay time can be programmed by connecting an external capacitor reference to ground.
4	$\overline{\text{RESET}}$	O	Active-low, open-drain output. This pin goes low when the SENSE voltage rises above the internally overvoltage threshold (V_{IT+}) or below the undervoltage threshold ($V_{IT–}$). See the timing diagram in 図 8-2 for more details. Connect this pin to a pull-up resistor terminated to the desired pull-up voltage.
5	GND	—	Ground
6	$\overline{\text{MR}}$	I	Manual reset (MR), pull this pin to a logic low ($V_{\overline{MR}\_L}$) to assert a reset signal . After the $\overline{\text{MR}}$ pin is deasserted the output goes high after the reset delay time(t_D) expires. $\overline{\text{MR}}$ can be left floating when not in use.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	6	V
Voltage	$V_{\overline{RESET}}$	–0.3	6	V
Voltage	V_{CT}	–0.3	6	V
Voltage	V_{SENSE}	–0.3	6	V
Voltage	$V_{\overline{MR}}$	–0.3	6	V
Current	$I_{\overline{RESET}}$		±40	mA
Temperature (2)	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(1)	±750	

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.7		5.5	V
V_{SENSE}	Input pin voltage	0		5.5	V
V_{CT}	CT pin voltage (1) (3)			V_{DD}	V
$V_{\overline{RESET}}$	Output pin voltage	0		5.5	V
$V_{\overline{MR}}$	$\overline{MR}$ pin Voltage (2)	0		5.5	V
$I_{\overline{RESET}}$	Output pin current	0.3		10	mA
T_J	Junction temperature (free-air temperature)	-40		125	℃

(1) CT pin connected to VDD pin requires a pullup resistor; 10 kΩ is recommended.
(2) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.
(3) The maximum rating is V_{DD} or 5.5 V, whichever is smaller.

7.4 Thermal Information

THERMAL METRIC[1]		TPS3703 DSE (WSON) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	86.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 1.7 V ≤ V_{DD} ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to V_{DD}, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at V_{DD} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.7		5.5	V
UVLO	Under Voltage Lockout[3]	V_{DD} falling below 1.7 V	1.2		1.7	V
V_{POR}	Power on reset voltage[2]	V_{OL}(max) = 0.25 V, I_{OUT} = 15 µA			1	V
$V_{IT+(OV)}$	Positive- going threshold accuracy		-0.7	±0.25	0.7	%
$V_{IT-(UV)}$	Negative-going threshold accuracy		-0.7	±0.25	0.7	%
V_{HYS}	Hysteresis Voltage[1]		0.3	0.55	0.8	%
$V_{IT+(OV)}$	Positive- going threshold accuracy	V_{IT} < 800 mV	-1		1	%
$V_{IT-(UV)}$	Negative-going threshold accuracy	V_{IT} < 800 mV	-1		1	%
V_{HYS}	Hysteresis Voltage[1]	V_{IT} < 800 mV	0.2		0.7	%
I_{DD}	Supply current	V_{DD} ≤ 5.5 V		4.5	7	µA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 5 V		1	1.5	µA
V_{OL}	Low level output voltage	V_{DD} = 1.7 V, I_{OUT} = 0.4 mA			250	mV
		V_{DD} = 2 V, I_{OUT} = 3 mA			250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA			250	mV
I_{LKG}	Open drain output leakage current	V_{DD} = $V_{\overline{RESET}}$ = 5.5 V			300	nA
$V_{\overline{MR}\_L}$	$\overline{MR}$ logic low input				0.3	V
$V_{\overline{MR}\_H}$	$\overline{MR}$ logic high input		1.4			V
V_{CT_H}	High level CT pin voltage		1.4			V
$R_{\overline{MR}}$	Manual reset Internal pullup resistance			100		KΩ
I_{CT}	CT pin charge current		337	375	413	nA
V_{CT}	CT pin comparator threshold voltage[4]		1.133	1.15	1.167	V

(1) Hysteresis is with respect of the tripoint ($V_{IT-(UV)}$, $V_{IT+(OV)}$).
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.
(3) $\overline{RESET}$ pin is driven low when V_{DD} falls below UVLO.
(4) V_{CT} voltage refers to the comparator threshold voltage that measures the voltage level of the external capacitor at CT pin.

7.6 Timing Requirements

At 1.7 V ≤ V_{DD} ≤ 5.5 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 10 kΩ to V_{DD}, $\overline{RESET}$ load = 10 pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at V_{DD} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_D	Reset time delay, TPS3703A, TPS3703E	CT = Open	7	10	13	ms
t_D	Reset time delay, TPS3703A, TPS3703E	CT = 10 kΩ to V_{DD}	140	200	260	ms
t_D	Reset time delay, TPS3703B, TPS3703F	CT = Open	0.7	1	1.3	ms
t_D	Reset time delay, TPS3703B, TPS3703F	CT = 10 kΩ to V_{DD}	14	20	26	ms
t_D	Reset time delay, TPS3703C, TPS3703G	CT = Open	3.5	5	6.5	ms
t_D	Reset time delay, TPS3703C, TPS3703G	CT = 10 kΩ to V_{DD}	70	100	130	ms
t_D	Reset time delay, TPS3703D, TPS3703H	CT = 10 kΩ to V_{DD} CT = Open		50		µs
t_{PD}	Propagation detect delay(1) (2)			15	30	µs
t_R	Output rise time(1) (3)			2.2		µs
t_F	Output fall time(1) (3)			0.2		µs
t_{SD}	Startup delay(4)			300		µs
$t_{GI\ (VIT-)}$	Glitch Immunity undervoltage $V_{IT-(UV)}$, 5% Overdrive(1)			3.5		µs
$t_{GI\ (VIT+)}$	Glitch Immunity overvoltage $V_{IT+(OV)}$, 5% Overdrive(1)			3.5		µs
$t_{GI\ (\overline{MR})}$	Glitch Immunity $\overline{MR}$ pin				25	ns
$t_{PD\ (\overline{MR})}$	Propagation delay from $\overline{MR}$ low to assert $\overline{RESET}$			500		ns
$t_{\overline{MR}\_W}$	$\overline{MR}$ pin pulse width duration to assert $\overline{RESET}$		1			µs
$t_{D\ (\overline{MR})}$	$\overline{MR}$ reset time delay			t_D		ms

(1) 5% Overdrive from threshold. Overdrive % = [V_{SENSE} - V_{IT}] / V_{IT}; Where V_{IT} stands for $V_{IT-(UV)}$ or $V_{IT+(OV)}$
(2) t_{PD} measured from threhold trip point ($V_{IT-(UV)}$ or $V_{IT+(OV)}$) to $\overline{RESET}$ V_{OL} voltage
(3) Output transitions from V_{OL} to 90% for rise times and 90% to V_{OL} for fall times.
(4) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least t_{SD} + t_D before the output is in the correct state.

7.7 Timing Diagrams

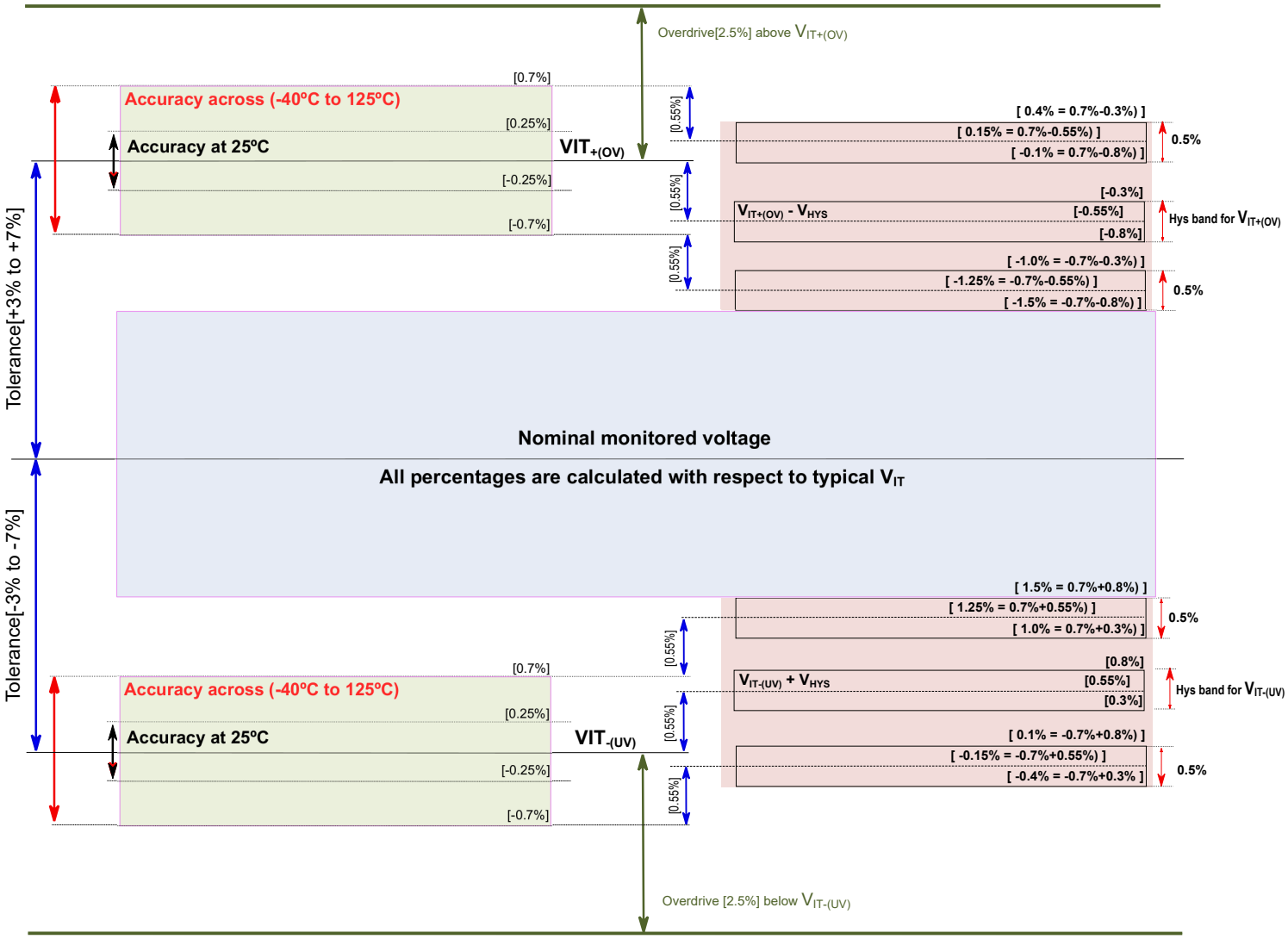


図 7-1. Voltage Threshold and Hysteresis Accuracy

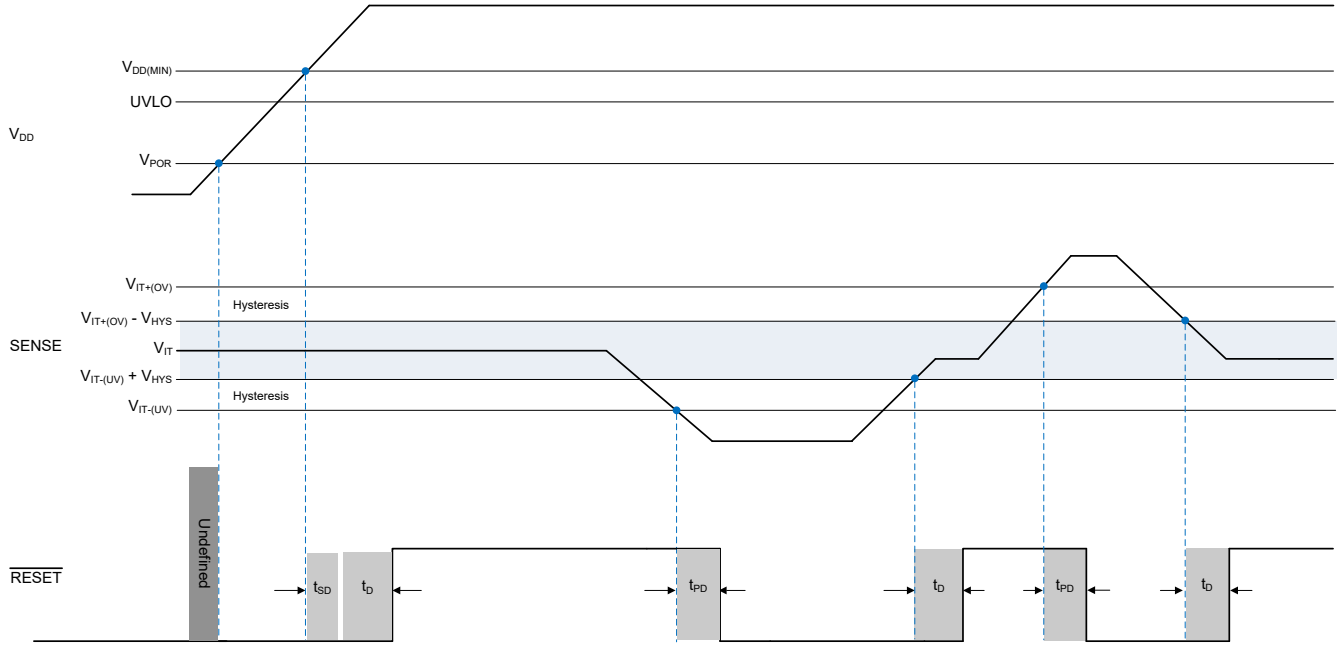
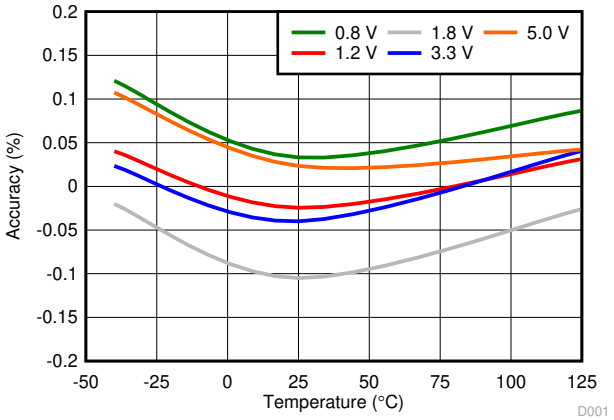


図 7-2. SENSE Timing Diagram

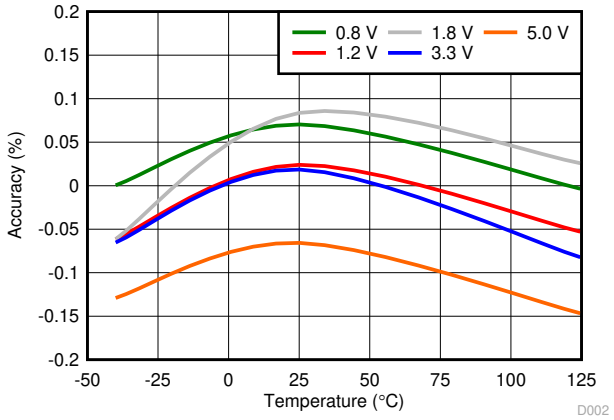
7.8 Typical Characteristics

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.



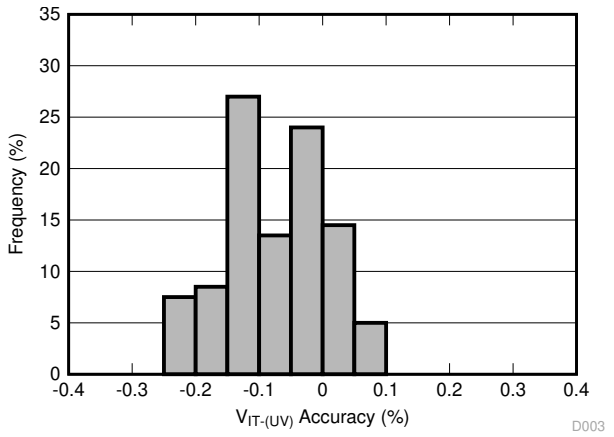
Tested across multiple voltage options

図 7-3. Undervoltage Accuracy vs Temperature



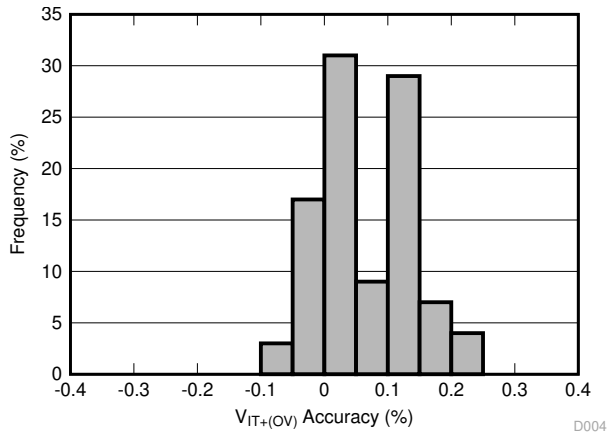
Tested across multiple voltage options

図 7-4. Overvoltage Accuracy vs Temperature



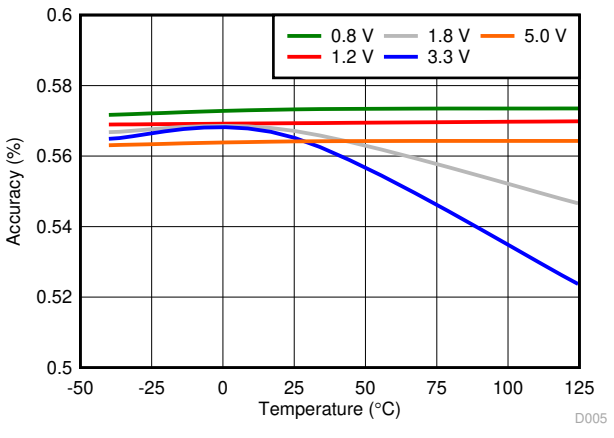
Sample Size of 100 TPS3703A7125 units

図 7-5. Undervoltage Accuracy Distribution



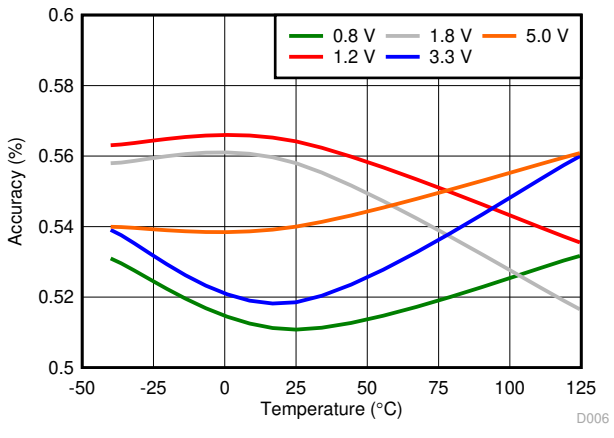
Sample Size of 100 TPS3703A7125 units

図 7-6. Overvoltage Accuracy Distribution



Tested across multiple voltage options

図 7-7. Undervoltage Hysteresis Voltage Accuracy vs Temperature

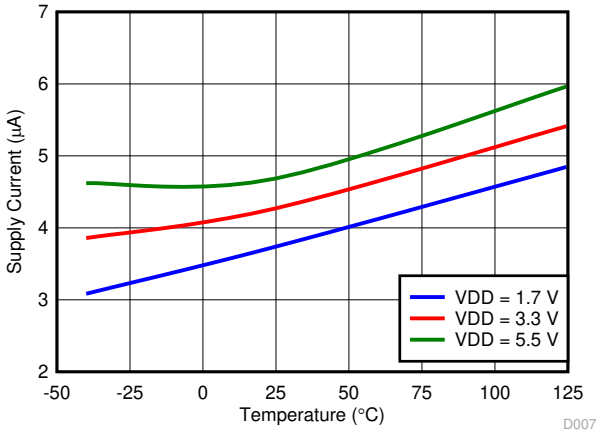


Tested across multiple voltage options

図 7-8. Overvoltage Hysteresis Voltage Accuracy vs Temperature

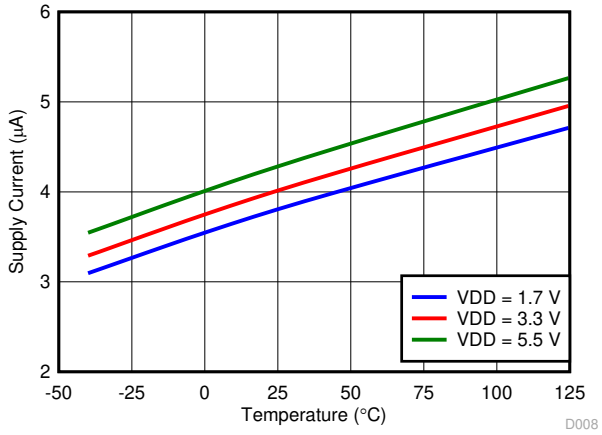
7.8 Typical Characteristics (continued)

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.



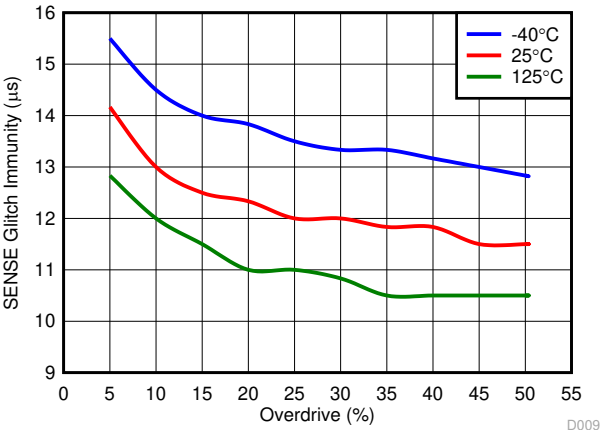
Output ($\overline{\text{RESET}}$ Pin) = High

図 7-9. Supply Current vs Temperature



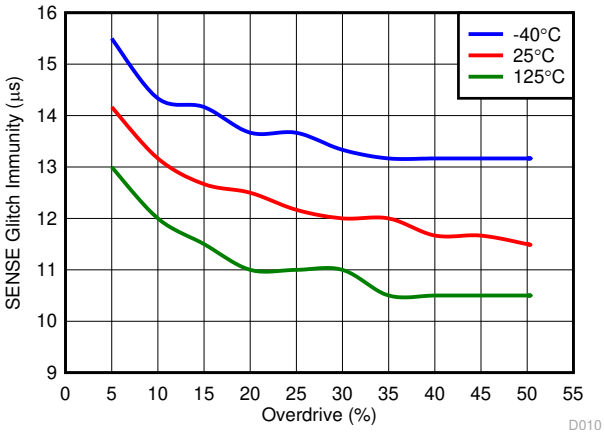
Output ($\overline{\text{RESET}}$ Pin) = Low

図 7-10. Supply Current vs Temperature



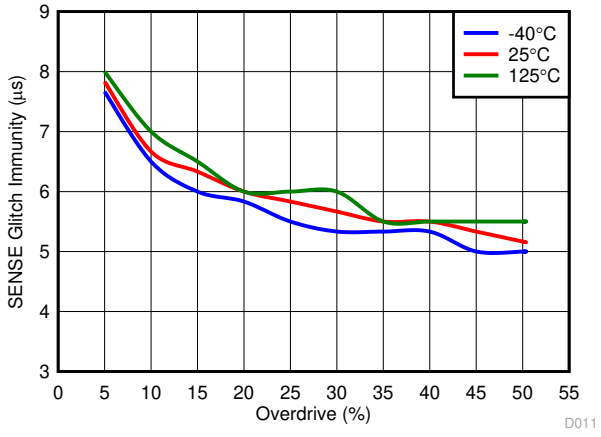
VDD = 1.7 V

図 7-11. SENSE Glitch Immunity (V_{IT-}) vs Overdrive



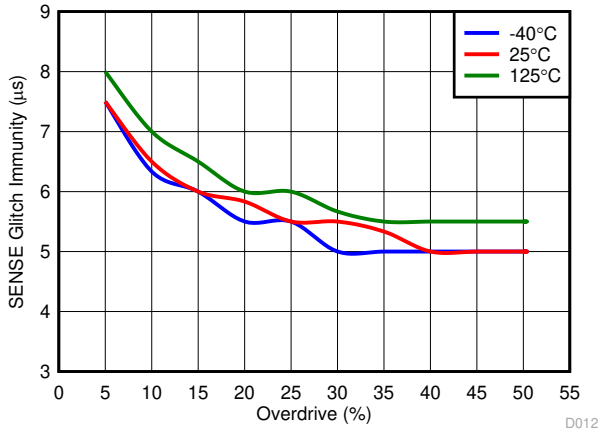
VDD = 1.7 V

図 7-12. SENSE Glitch Immunity (V_{IT+}) vs Overdrive



VDD = 5.5 V

図 7-13. SENSE Glitch Immunity (V_{IT-}) vs Overdrive

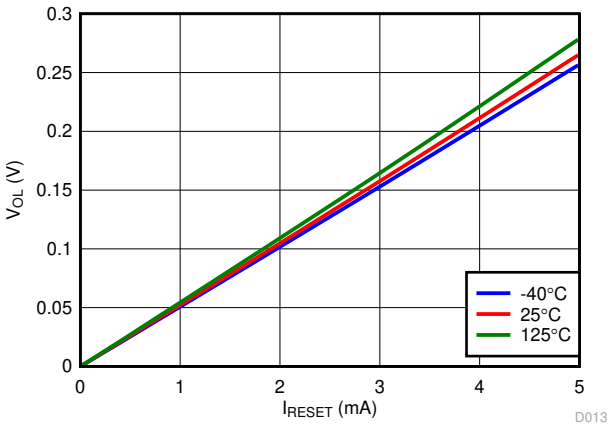


VDD = 5.5 V

図 7-14. SENSE Glitch Immunity (V_{IT+}) vs Overdrive

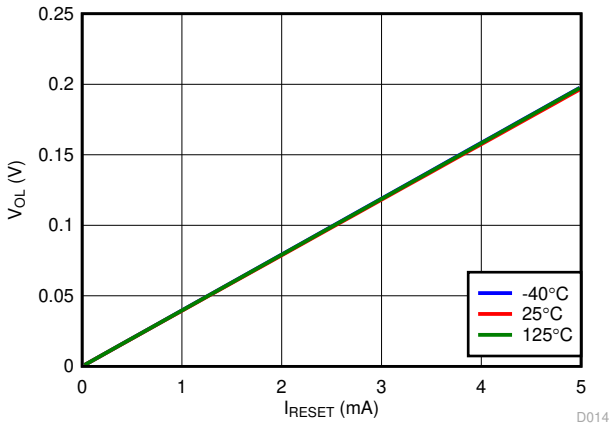
7.8 Typical Characteristics (continued)

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.



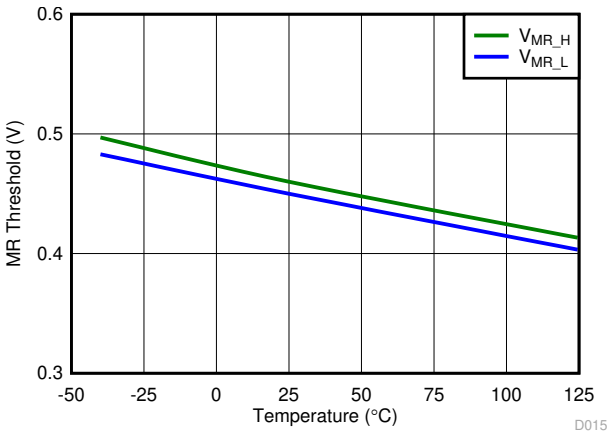
VDD = 1.7 V

図 7-15. Low-Level Output Voltage vs RESET current



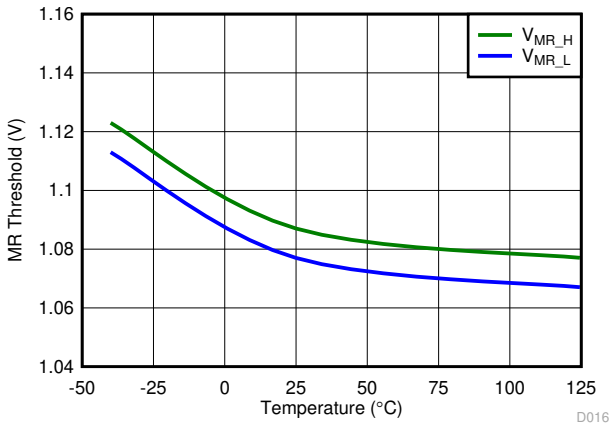
VDD = 5.5 V

図 7-16. Low-Level Output Voltage vs RESET current



VDD = 1.7 V

図 7-17. SET Threshold vs Temperature



VDD = 5.5 V

図 7-18. SET Threshold vs Temperature

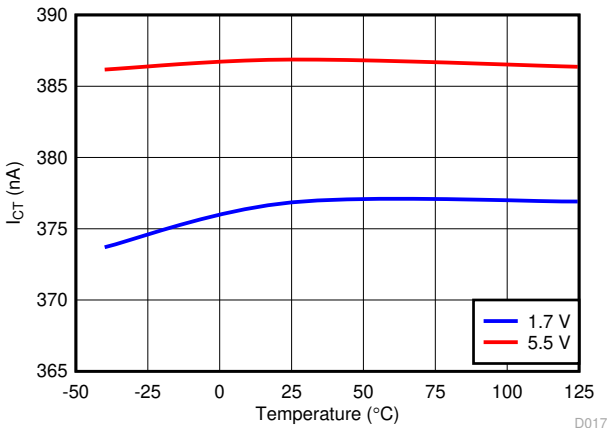


図 7-19. CT Current vs CT value

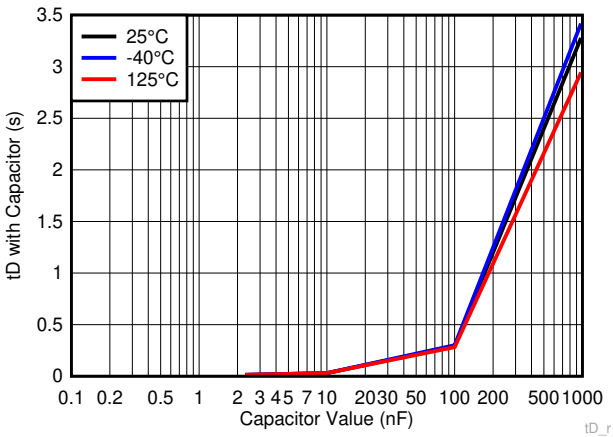


図 7-20. $\overline{\text{RESET}}$ Timeout vs CT Capacitor

7.8 Typical Characteristics (continued)

At T_J = 25°C, V_{DD} = 3.3 V, and R_{PU} = 10 kΩ, unless otherwise noted.

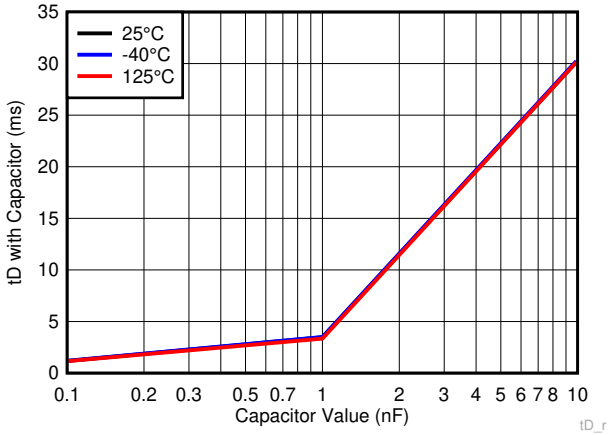


図 7-21. Timeout vs CT Capacitor (0.1 to 10 nF)

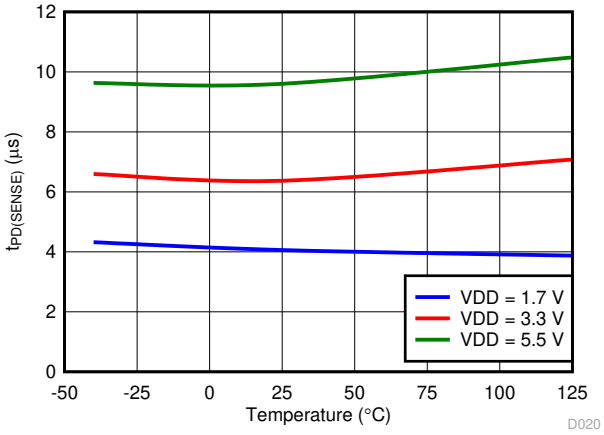


図 7-22. Detect Propagation Delay vs Temperature

8 Detailed Description

8.1 Overview

The TPS3703 family of devices combines two voltage comparators and a precision voltage reference for overvoltage and undervoltage detection. The TPS3703 features a highly accurate window threshold voltages (±0.7% over temperature) and a variety voltage threshold variants.

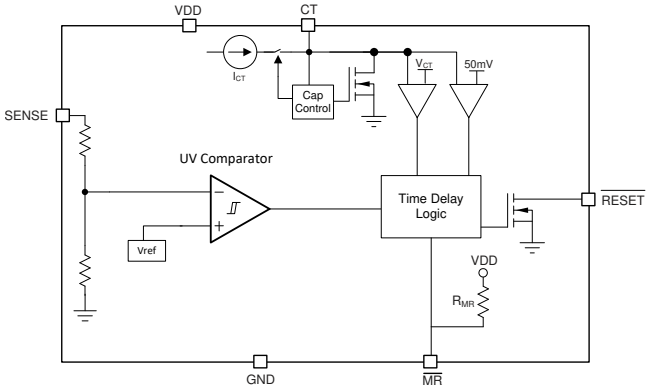
The TPS3703 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

TPS3703 version A, B and C has three time delay settings, two fixed by connecting CT pin to VDD through a resistor and leaving CT floating and a programmable time delay setting that only requires a single capacitor connected from CT pin to ground.

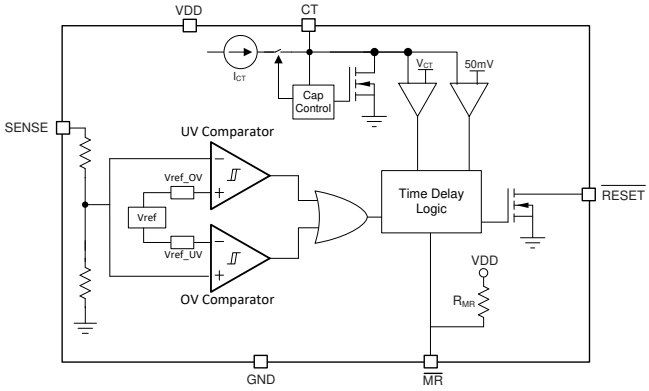
Manual Reset ($\overline{MR}$) allows for sequencing or hard reset by driving the $\overline{MR}$ pin below $V_{\overline{MR}\_L}$.

The TPS3703 is designed to assert active low output signals when the monitored voltage is outside the safe window. The relationship between the monitored voltage and the states of the outputs is shown in 表 8-1.

8.2 Functional Block Diagram



Undervoltage Only Version



Window Version

*For all possible voltages, window tolerance, time delays, and UV threshold options, see 表 12-1.

8.3 Feature Description

8.3.1 VDD

The TPS3703 is designed to operate from an input voltage supply range between 1.7 V to 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1-µF capacitor between the VDD pin and the GND pin.

V_{DD} needs to be at or above $V_{DD(MIN)}$ for at least the start-up delay (t_{SD}+ t_D) for the device to be fully functional.

8.3.2 SENSE

The TPS3703 combines two comparators with a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and ensures stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the SENSE input in order to reduce sensitivity to transient voltages on the monitored signal.

When monitoring VDD supply voltage, the SENSE pin can be connected directly to VDD. The output ($\overline{RESET}$) is high impedance when voltage at the SENSE pin is between upper and lower boundary of threshold.

8.3.3 $\overline{\text{RESET}}$

In a typical TPS3703 application, the $\overline{\text{RESET}}$ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator [such as a DC-DC converter or low-dropout regulator (LDO)].

The TPS3703 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current. These values are specified in セクション 7.5. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS3703 $\overline{\text{RESET}}$ pin.

表 8-1 describes the scenarios when the output ($\overline{\text{RESET}}$) is either asserted low or high impedance.

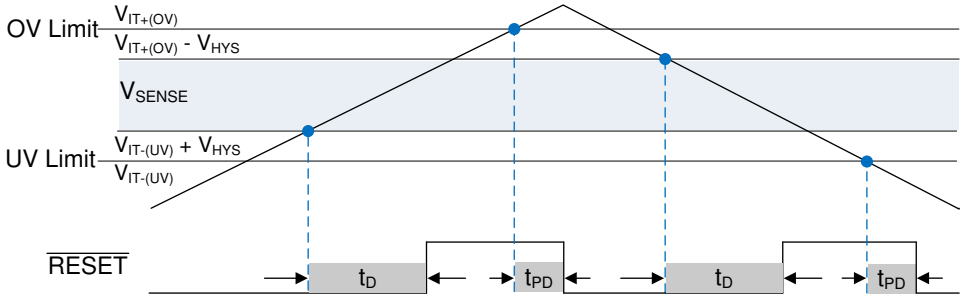


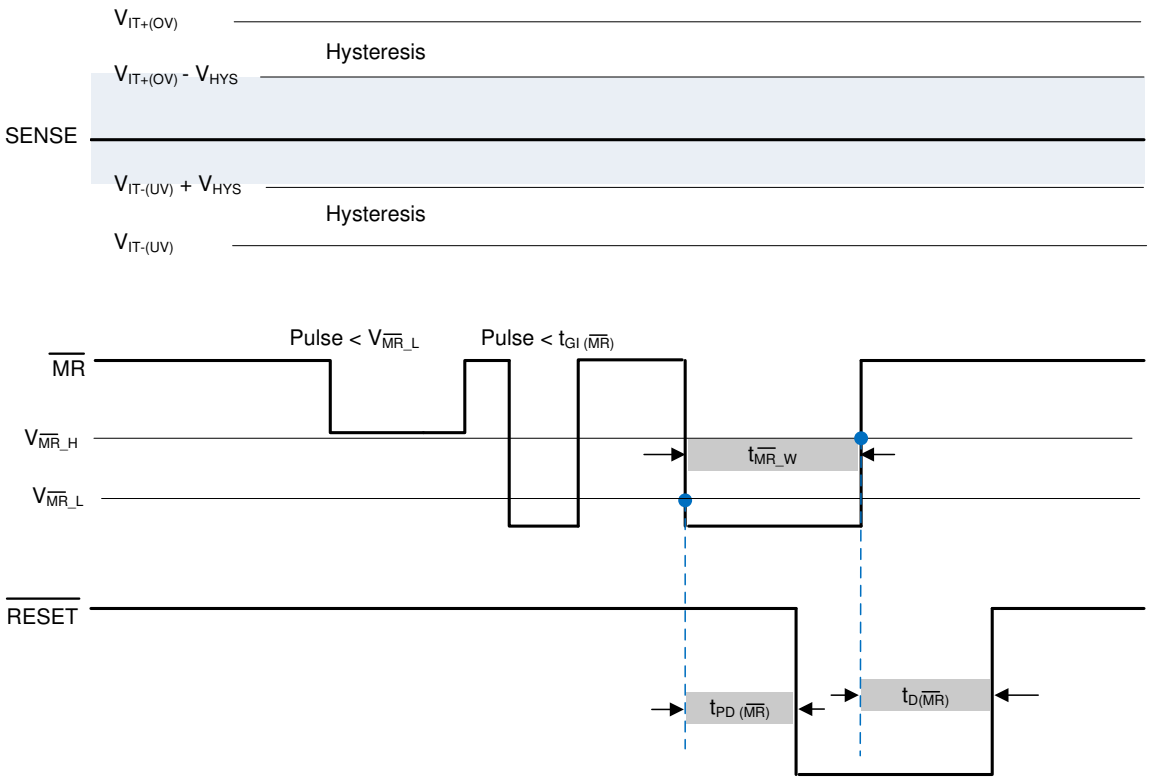
図 8-1. RESET output

8.3.4 Capacitor Time (CT)

The CT pin provides the user the functionality of both high-precision, factory-programmed, reset delay timing options and user-programmable, reset delay timing. The CT pin can be pulled up to V_{DD} through a resistor, have an external capacitor to ground, or can be left unconnected. The configuration of the CT pin is re-evaluated by the device every time the voltage on the SENSE line enters the valid window ($V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)}$). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CT pin. The sequence of events takes 450 µs to determine if the CT pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CT pin is being pulled up to VDD, then a pull-up resistor is required, 10 kΩ is recommended.

8.3.5 Manual Reset ($\overline{MR}$)

The manual reset ($\overline{MR}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to a logic high and the SENSE pin voltage is within a valid window ($(V_{IT-(UV)} < V_{SENSE} < V_{IT+(OV)})$, $\overline{RESET}$ is deasserted after the reset delay time (t_D). If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can either be connected to V_{DD} or left floating because the $\overline{MR}$ pin is internally pulled up to V_{DD}. 図 8-2 shows the relation between $\overline{MR}$ and $\overline{RESET}$.



A. $\overline{RESET}$ pulls up to VDD with 10 kΩ.
B. To initiate and continue time reset counter both conditions must be met $\overline{MR}$ pin above $V_{\overline{MR}\_H}$ or floating and V_{SENSE} between $V_{IT-(UV)}$ + V_{HYS} and $V_{IT+(OV)}$ - V_{HYS}
C. $\overline{MR}$ is ignored during output $\overline{RESET}$ low event

図 8-2. Manual Reset Timing Diagram

8.4 Device Functional Modes

表 8-1. Functional Mode Truth Table

DESCRIPTION	CONDITION	$\overline{MR}$ PIN	VDD PIN	OUTPUT ($\overline{RESET}$ PIN)
Normal Operation	$V_{IT-(UV)}$ < SENSE < $V_{IT+(OV)}$	Open or above $V_{\overline{MR}\_H}$	V_{DD} > $V_{DD(MIN)}$	High
Normal Operation (UV Only)	SENSE > $V_{IT-(UV)}$	Open or above $V_{\overline{MR}\_H}$	V_{DD} > $V_{DD(MIN)}$	High
Over Voltage detection	SENSE > $V_{IT+(OV)}$	Open or above $V_{\overline{MR}\_H}$	V_{DD} > $V_{DD(MIN)}$	Low
Under Voltage detection	SENSE < $V_{IT-(UV)}$	Open or above $V_{\overline{MR}\_H}$	V_{DD} > $V_{DD(MIN)}$	Low
Manual reset	$V_{IT-(UV)}$ < SENSE < $V_{IT+(OV)}$	Below $V_{\overline{MR}\_L}$	V_{DD} > $V_{DD(MIN)}$	Low
UVLO engaged	$V_{IT-(UV)}$ < SENSE < $V_{IT+(OV)}$	Open or above $V_{\overline{MR}\_H}$	V_{POR} < V_{DD} < UVLO	Low

8.4.1 Normal Operation (V_{DD} > $V_{DD(MIN)}$)

When the voltage on V_{DD} is greater than $V_{DD(MIN)}$ for approximately (t_{SD}+ t_D), the $\overline{RESET}$ output state will correspond to the SENSE pin voltage with respect to the threshold limits, when SENSE voltage is outside of threshold limits the $\overline{RESET}$ voltage will be low (V_{OL}).

8.4.2 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage but greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ pin will be held low , regardless of the voltage on SENSE pin.

8.4.3 Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) to internally pull the asserted output to GND, $\overline{RESET}$ signal is undefined and is not to be relied upon for proper device function.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Voltage Threshold Accuracy

Voltage monitoring requirements vary depending on the voltage supply tolerance of the device being powered. Due to the high precision of the TPS3703 (±0.7% Max), the device allows for a wider supply voltage margins and threshold headroom for tight tolerance applications.

For example, take a DC/DC regulator providing power to a core voltage rail of an MCU. The MCU has a tolerance of ±5% of the nominal output voltage of the DC/DC. The user sets an ideal voltage threshold of ±4% which allows for ±1% of threshold accuracy. Since the TPS3703 threshold accuracy is higher than ±1%, the user has more supply voltage margin which can allow for a relaxed power supply design. This gives flexibility to the DC/DC to use a smaller output capacitor or inductor because of a larger voltage window for voltage ripple and transients. There is also headroom between the minimum system voltage and voltage tolerance of the MCU to ensure that the voltage supply will never be in the region of potential failure of malfunction without the TPS3703 asserting a reset signal.

図 9-1 illustrates the supply undervoltage margin and accuracy of the TPS3703 for the example explained above. Using a low accuracy supervisor will eat into the available budget for the power supply ripple and transient response. This gives less flexibility to the user and a more stringent DC/DC converter design.

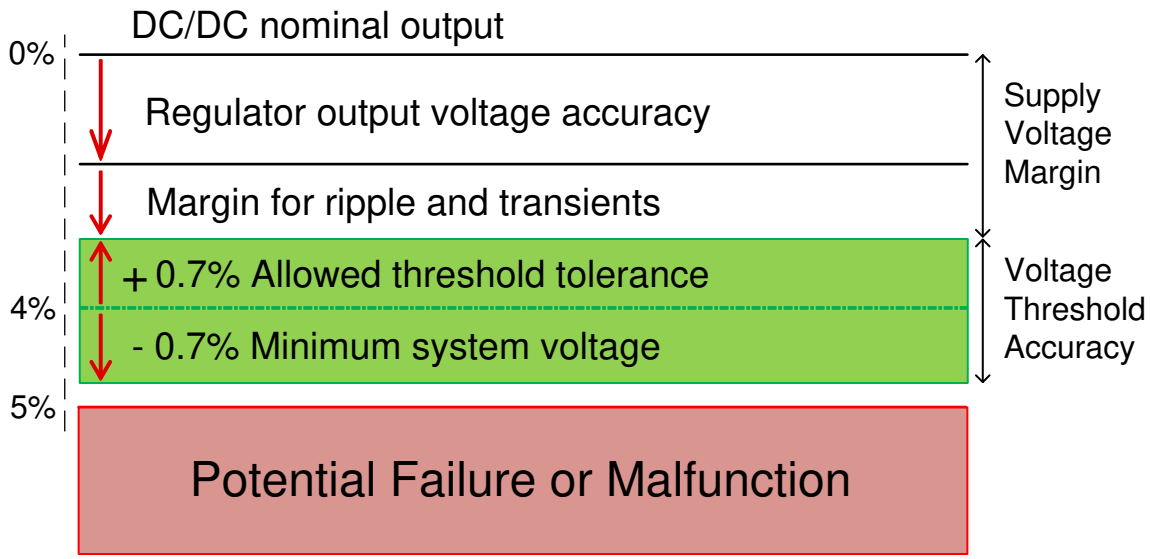


図 9-1. TPS3703 Voltage Threshold Accuracy

9.1.2 CT Reset Time Delay

The TPS3703 features three options for setting the reset delay (t_D): connecting a capacitor to the CT pin, connecting a pull-up resistor to VDD, and leaving the CT pin unconnected. 図 9-2 shows a schematic drawing of all three options. To determine which option is connected to the CT pin, an internal state machine controls the internal pulldown device and measures the pin voltage. This sequence of events takes 450 µs to determine which timing option is used. Every time the voltage on the SENSE line enters the valid window ($V_{IT-(UV)}$ + V_{HYS} < V_{SENSE} < $V_{IT+(OV)}$ -V_{HYS}, the state machine determines the CT option.

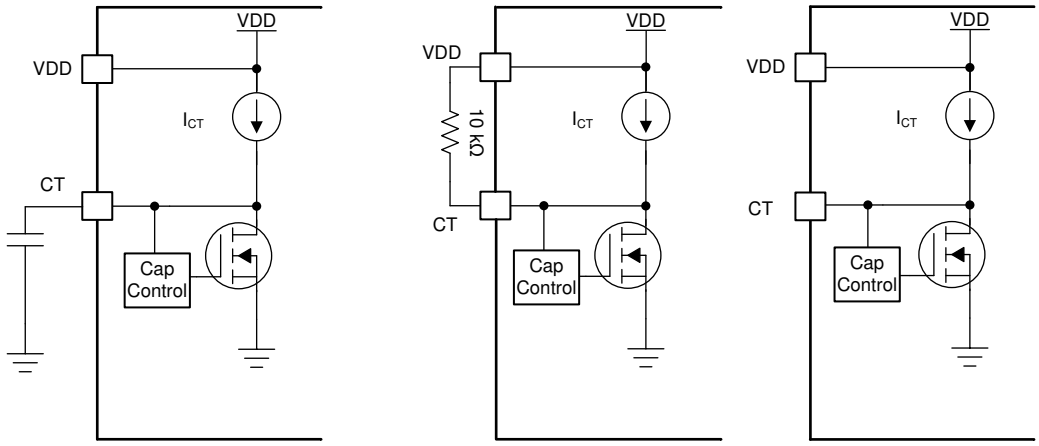


図 9-2. CT Charging Circuit

9.1.2.1 Factory-Programmed Reset Delay Timing

To use the factory-programmed timing options, the CT pin must either be left unconnected or pulled up to VDD through a 10 kΩ pull-up resistor. Using these options enables a high-precision reset delay timing, as shown in 表 9-1.

表 9-1. Reset Delay Time for Factory-Programmed Reset Delay Timing

VARIANT	RESET DELAY TIME (t_D)			VALUE
	CT = Capacitor to GND	CT = Floating	CT = 10 kΩ to VDD	
TPS3703A	Programmable t_D	10	200	ms
TPS3703B	Programmable t_D	1	20	ms
TPS3703C	Programmable t_D	5	100	ms
TPS3703D	N/A	50	50	µs

9.1.2.2 Programmable Reset Delay-Timing

The TPS3703 reset time delay is based on internal current source (I_{CT}) to charge external capacitor (C_{CT}) and read capacitor voltage with internal comparator. The minium value capacitor is 250 pF. There is no limitation on maximum capacitor the only constrain is imposed by the initial voltage of the capacitor, if CT cap is zero or near to zero then ideally there is no other constraint on the max capacitor. The typical ideal capacitor value needed for a given delay time can be calculated using 式 1, where C_{CT} is in nanofarads (nF) and t_D is in ms:

$$t_D = 3.066 \times C_{CT} + 0.5 \text{ ms} \quad (1)$$

To calculate the minimum and maximum-reset delay time use 式 2 and 式 3, respectively.

$$t_{D(min)} = 2.7427 \times C_{CT} + 0.3 \text{ ms} \quad (2)$$

$$t_{D(max)} = 3.4636 \times C_{CT} + 0.7 \text{ ms} \quad (3)$$

The slope of the equation is determined by the time the CT charging current (I_{CT}) takes to charge the external capacitor up to the CT comparator threshold voltage (V_{CT}). When $\overline{\text{RESET}}$ is asserted, the capacitor is discharged through the internal CT pulldown resistor. When the $\overline{\text{RESET}}$ conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor; when V_{CT} = 1.15 V, $\overline{\text{RESET}}$ is unasserted. Note that in order to minimize the difference between the calculated $\overline{\text{RESET}}$ delay time and the actual $\overline{\text{RESET}}$ delay time, use a use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. 表 9-2 lists the reset delay time ideal capacitor values for C_{CT}.

表 9-2. Reset Delay Time for Ideal Capacitor Values

C_{CT}	$\overline{\text{RESET}}$ DELAY TIME (t_D), TYPICAL
250 pF	1.27 ms
1 nF	3.57 ms
3.26 nF	10.5 ms
32.6 nF	100.45 ms
65.2 nF	200.40 ms
1uF	3066.50 ms

9.1.3 $\overline{\text{RESET}}$ Latch Mode

The TPS3703 features a voltage latch mode on the $\overline{\text{RESET}}$ pin when connecting the CT pin to common ground . A pull-down resistor is recommended to limit current consumption of the system. In latch mode, if the $\overline{\text{RESET}}$ pin is low or triggers low, the pin will stay low regardless if V_{SENSE} is within the acceptable voltage boundaries ($V_{IT-(UV)}$ < V_{SENSE} < $V_{IT+(OV)}$). To unlatch the device provide a voltage to the CT pin that is greater than the CT pin comparator threshold voltage, V_{CT}. The $\overline{\text{RESET}}$ pin will trigger high instantaneously without any reset delay. A voltage greater than 1.2 V to recommended to ensure a proper unlatch. Use a series resistance to limit current when an unlatch voltage is applied. For more information, セクション 9.2.2 gives an example of a typical latch application.

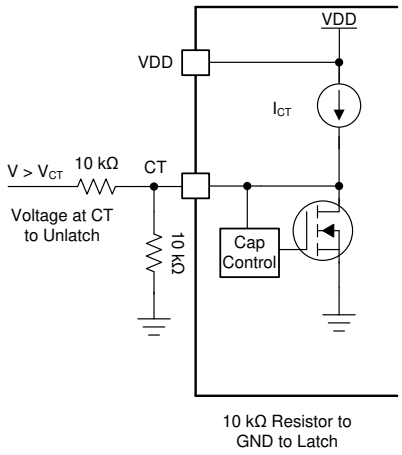


図 9-3. $\overline{\text{RESET}}$ Latch Circuit

9.1.4 Adjustable Voltage Thresholds

The TPS3703 0.7% maximum accuracy allows for adjustable voltage thresholds using external resistors without adding major inaccuracies to the device. In case that the desired monitored voltage is not available, external resistor dividers can be used to set the desired voltage thresholds. 図 9-4 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8V voltage threshold device such as the TPS3703B3080 because of the bypass mode of internal resistor ladder.

For example, consider a 2.0 V rail being monitored (V_{MON}) using the TPS3703B3080 variant. Using 式 4, R1 = 15 kΩ given that R2 = 10 kΩ, V_{MON} = 2 V, and V_{SENSE} = 0.8 V. This device is typically meant to monitor a 0.8 V rail with ±3% voltage thresholds. This means that the device undervoltage threshold ($V_{IT-(UV)}$) and overvoltage threshold ($V_{IT-(OV)}$) is 0.776 V and 0.824 V respectively. Using 式 4, V_{MON} = 1.94 V when V_{SENSE} = $V_{IT-(UV)}$. This can be denoted as V_{MON-}, the monitored undervoltage threshold where the device will assert a reset signal. Using 式 4 again, the monitored overvoltage threshold (V_{MON+}) = 2.06 V when V_{SENSE} = $V_{IT+(OV)}$. If a wider tolerance or UV only threshold is desired, use a device variant shown on 表 12-1 to determine what device part number matches your application.

$$V_{SENSE} = V_{MON} \times (R_2 \div (R_1 + R_2)) \quad (4)$$

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for design specifications. The internal sense resistance (R_{SENSE}) can be calculated by the sense voltage (V_{SENSE}) divided by the sense current (I_{SENSE}) as shown in 式 6. V_{SENSE} can be calculated using 式 4 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using 式 5.

$$I_{SENSE} = (V_{MON} - V_{SENSE}) \div R_1 - (V_{SENSE} \div R_2) \quad (5)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (6)$$

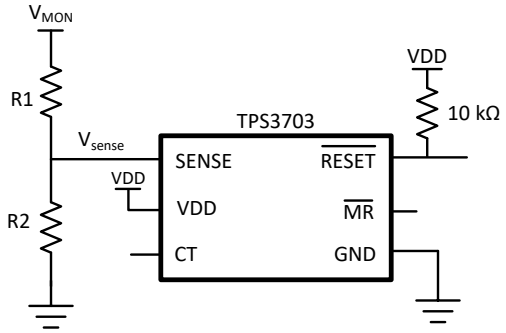


図 9-4. Adjustable Voltage Threshold with External Resistor Dividers

9.1.5 Immunity to SENSE Pin Voltage Transients

The TPS3703 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs ($\overline{RESET}$). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 7:

$$\text{Overdrive \%} = | (V_{SENSE} - (V_{IT-(UV)} \text{ or } V_{IT+(OV)})) / V_{IT} \text{ (Nominal)} \times 100\% | \quad (7)$$

where:

- V_{SENSE} is the voltage at the SENSE pin
- V_{IT} (Nominal) is the nominal threshold voltage
- $V_{IT-(UV)}$ and $V_{IT+(OV)}$ represent the actual undervoltage or overvoltage tripping voltage

9.1.5.1 Hysteresis

Overvoltage and undervoltage comparators include built-in hysteresis that provides noise immunity and ensures stable operation. For example if the voltage on the SENSE pin falls below $V_{IT-(UV)}$ or above $V_{IT+(OV)}$, then $\overline{RESET}$ is asserted (driven low), then when the voltage on the SENSE pin is between the positive and negative threshold voltages, $\overline{RESET}$ deasserts after the user-defined $\overline{RESET}$ delay time. 図 9-5 shows the relation between $V_{IT-(UV)}$,$V_{IT+(OV)}$ and hysteresis voltage (V_{HYS}).

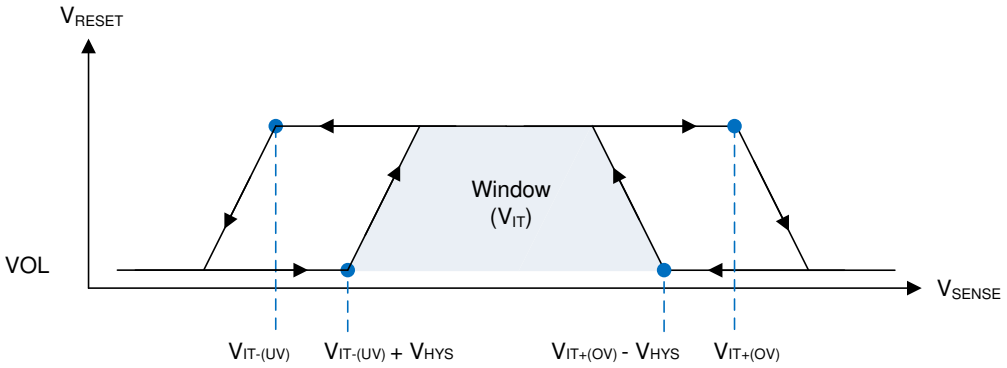


図 9-5. SENSE Pin Hysteresis

9.2 Typical Application

9.2.1 Design 1: Multi-Rail Window Monitoring for Microcontroller Power Rails

A typical application for the TPS3703 is shown in 図 9-6. The TPS3703 is used to monitor two PMIC voltage rails that powers the core and I/O voltage of the microcontroller that requires accurate reset delay and voltage supervision. It utilizes the TPS3703 to monitor the core voltage rail of a MCU similar to the circuit below.

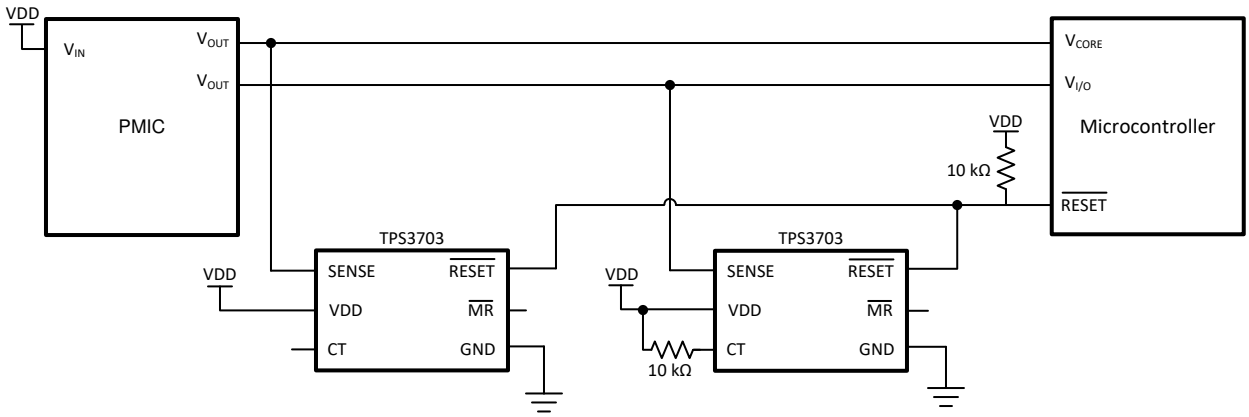


図 9-6. Two TPS3703 Monitoring Two Microcontroller Power Rails

9.2.1.1 Design Requirements

表 9-3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-$V_{I/O}$ nominal, with alerts if outside of ±8% of 3.3 V (including device accuracy), 200 ms reset delay	Worst case $V_{IT+(OV)}$ = 3.554 V (7.7%), Worst case $V_{IT–(UV)}$ = 3.046 V (-7.7%)
	1.2-V_{CORE} nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy), 10 ms reset delay	Worst case $V_{IT+(OV)}$ = 1.256 V (4.7%), Worst case $V_{IT–(UV)}$ = 1.144 V (-4.7%)
Output logic voltage	5-V CMOS	5-V CMOS
Maximum system supervision current consumption	50 µA	14 µA (7 µA Max each)

9.2.1.2 Detailed Design Procedure

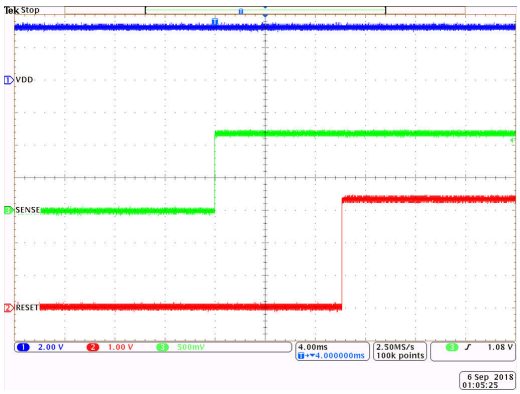
Determine which version of the TPS3703 best suits the monitored rail (V_{MON}) and window tolerances found on 表 12-1. The TPS3703 allows overvoltage and undervoltage monitoring for precise voltage supervision of common rails between 0.5 V and 5.0 V. This application calls for very tight monitoring of the rail with only ±5% of variation allowed on the 1.2V core rail. To ensure this requirement is met, the TPS3703 was chosen for its ±4% thresholds. The 3.3V I/O is more flexible and can operate up to 8% variance. Since the TPS3703 comes in various tolerance options, the ±7% thresholds can be chosen for this voltage rail. To calculate the worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$, the accuracy must also be taken into account. The worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$ can be calculated shown in 式 8 and 式 9 respectively:

$$V_{IT+(OV\text{-}Worst\ Case)} = V_{MON} \times (\%Threshold + 0.7\%) = 1.2 \times (+4.7\%) = 1.256\ V \quad (8)$$

$$V_{IT-(UV\text{-}Worst\ Case)} = V_{MON} \times (\%Threshold - 0.7\%) = 1.2 \times (-4.7\%) = 1.144V \quad (9)$$

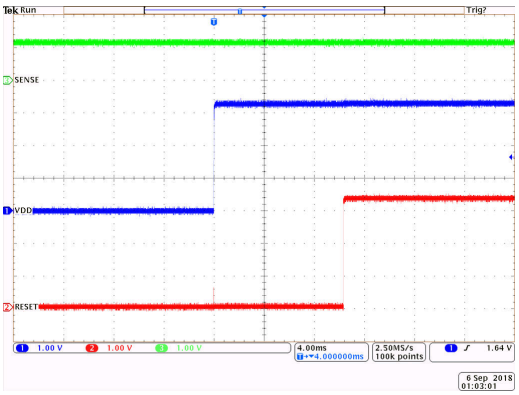
When the outputs switch to a high impedance state, the rise time of the $\overline{RESET}$ pin depends on the pull-up resistance and the capacitance on that node. Choose pull-up resistors that satisfy both the downstream timing requirements and the sink current required to have a V_{OL} low enough for the application; 10 kΩ to 1 MΩ resistors are a good choice for low-capacitive loads.

9.2.1.3 Application Curves



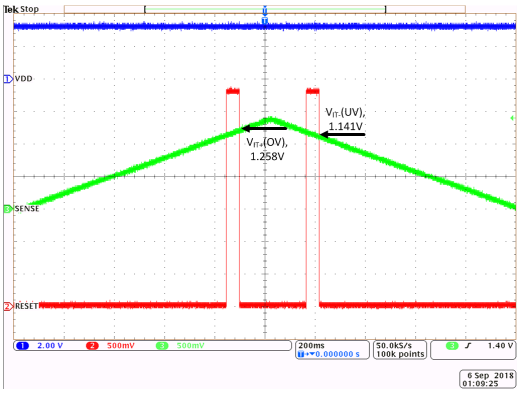
V_{SENSE} Start up from 0 V to 1.2 V, V_{DD} = 3.3 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

図 9-7. TPS3703 SENSE Start Up Function



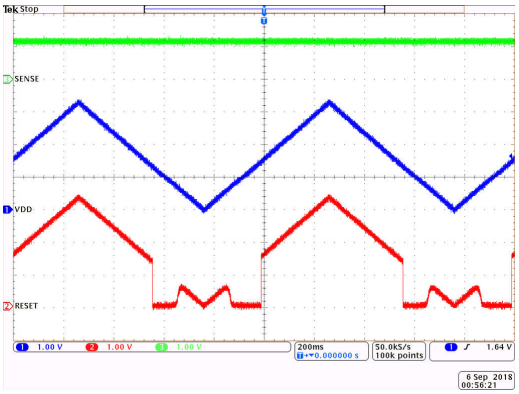
V_{DD} Start up from 0 V to 3.3 V, V_{SENSE} = 1.2 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

図 9-8. TPS3703 VDD Start Up Function



V_{SENSE} ramp from 0 V to 1.4 V, V_{DD} = 3.3 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

図 9-9. TPS3703 Overvoltage and Undervoltage Function



V_{DD} ramp from 0 V to 3.3 V, V_{SENSE} = 1.2 V, CT = OPEN
$V_{\overline{RESET}}$ = VDD = 3.3 V,TPS3703A4120

図 9-10. TPS3703 VDD Ramp Up Function

9.2.2 Design 2: $\overline{\text{RESET}}$ Latch Mode

Another typical application for the TPS3703 is shown in 図 9-11. The TPS3703 is used in a $\overline{\text{RESET}}$ latch output mode. In latch mode, once $\overline{\text{RESET}}$ driven logic low, it will stay low regardless of the sense voltage. If the $\overline{\text{RESET}}$ pin is low on start up, it will also stay low regardless of sense voltage.

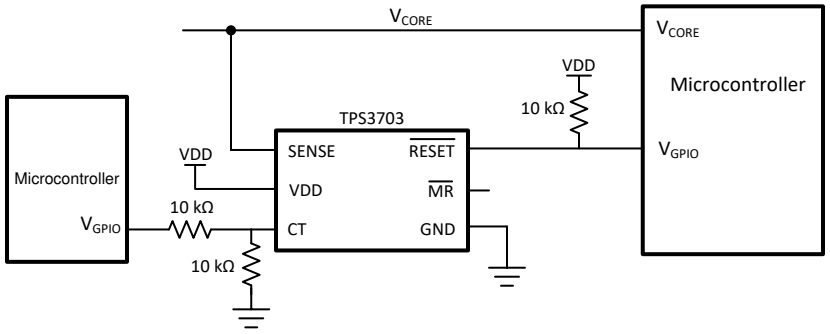


図 9-11. Window Voltage Monitoring with $\overline{\text{RESET}}$ Latch

9.2.2.1 Design Requirements

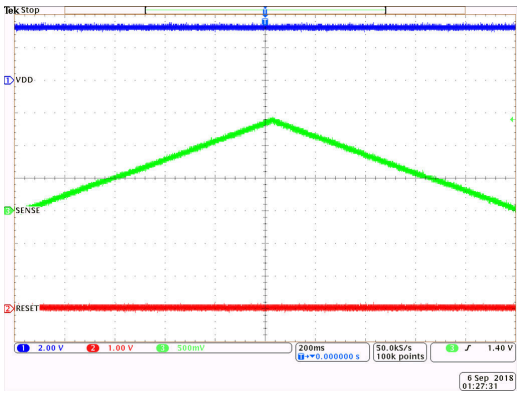
表 9-4. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored Rail	1.2-V_{CORE} nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy), Latch when $\overline{\text{RESET}}$ is low, until voltage is applied on CT pin.	Worst case $V_{IT+(OV)}$ = 1.256 V (4.7%), Worst case $V_{IT–(UV)}$ = 1.144 V (-4.7%)
Output logic voltage	5-V CMOS	5-V CMOS
Maximum device current consumption	15 µA	4.5 µA (Typ), 7 µA (Max)

9.2.2.2 Detailed Design Procedure

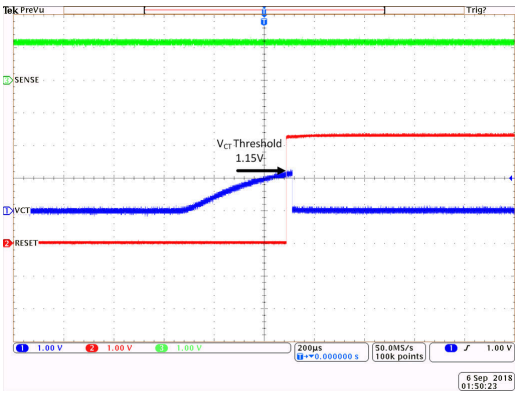
The $\overline{\text{RESET}}$ pin can be latched when the CT pin is connected to a common ground with a pull-down resistor. A 10 kΩ resistors is recommended to limit current consumption. To unlatch the device provide a voltage to the CT pin that is greater than the CT pin comparator threshold voltage, V_{CT}. A voltage greater than 1.15 V to recommended to ensure a proper unlatch. Use a series resistance to limit current when an unlatch voltage is applied. To go back into latch operation, disconnect the voltage on the CT pin. The $\overline{\text{RESET}}$ pin will trigger high instanously without any reset delay.

9.2.2.3 Application Curves



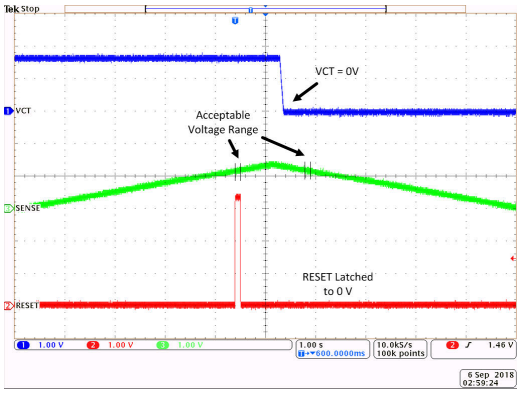
V_{SENSE} ramp from 0 V to 1.4V, V_{DD} = 3.3 V, V_{CT} = 0 V
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

図 9-12. TPS3703 SENSE Ramp Latch Function



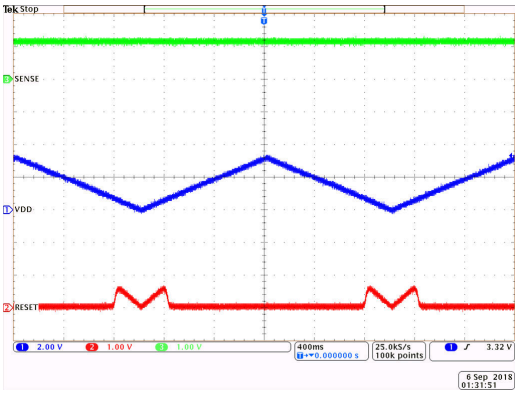
V_{CT} biased at least to 1.15 V , V_{SENSE} = 1.2 V
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

図 9-13. TPS3703 CT Bias Unlatch Function



V_{Sense} ramp from 0 V to 1.4 V , V_{DD} = 3.3 V, $V_{\overline{RESET}}$ = VDD
CT is pulled down after RESET is low, RESET becomes latched TPS3703A4120

図 9-14. TPS3703 Overvoltage and Undervoltage Latch Function



V_{DD} ramp up from 0 V to 3.3 V , V_{SENSE} = 1.2 V, CT = 0 V
$V_{\overline{RESET}}$ = VDD = 3.3 V, TPS3703A4120

図 9-15. TPS3703 VDD Ramp Latch Function

10 Power Supply Recommendations

10.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 1.7 V to 5.5 V. It has a 6-V absolute maximum rating on the VDD pin. It is good analog practice to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

11 Layout

11.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

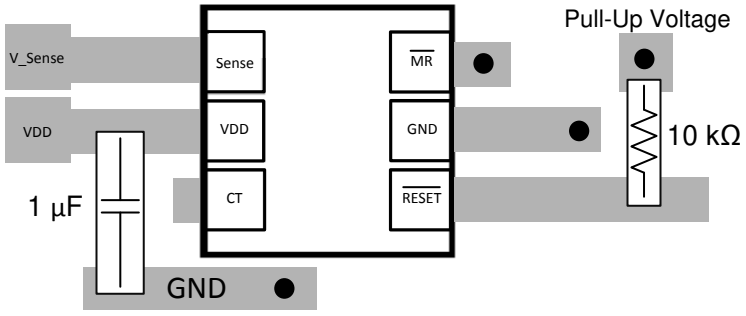


図 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

表 12-1 shows how to decode the function of the device based on its part number.

表 12-1. Device Naming Convention

DESCRIPTION		NOMENCLATURE	VALUE
		TPS3703	TPS3703
Time delay options: Every part has two fixed time delay and adjustable delay option via external capacitor part number	Window (OV & UV)	A	CT pin open = 10 ms, CT pin tied to VDD = 200 ms CT programable with external capacitor
		B	CT pin open = 1 ms, CT pin tied to VDD = 20 ms CT programable with external capacitor
		C	CT pin open = 5 ms, CT pin tied to VDD = 100 ms CT programable with external capacitor
		D	CT pin open = 50 µs, CT pin tied to VDD = 50 µs CT not programable
	UV only	E	CT pin open = 10 ms, CT pin tied to VDD = 200 ms CT programable with external capacitor
		F	CT pin open = 1 ms, CT pin tied to VDD = 20 ms CT programable with external capacitor
		G	CT pin open = 5 ms, CT pin tied to VDD = 100 ms CT programable with external capacitor
		H	CT pin open = 50 µs, CT pin tied to VDD = 50 µs CT not programable
Tolerance options: Trigger or threshold voltage as a percentage of the monitored threshold voltage		3	Window threshold from nominal value = OV : 3%; UV: –3%
		4	Window threshold from nominal value = OV : 4%; UV: –4%
		5	Window threshold from nominal value = OV : 5%; UV: –5%
		6	Window threshold from nominal value = OV : 6%; UV: –6%
		7	Window threshold from nominal value = OV : 7%; UV: –7%

表 12-1. Device Naming Convention (continued)

DESCRIPTION	NOMENCLATURE	VALUE
Nominal monitor threshold voltage option	050	0.50 V
	055	0.55 V
	060	0.60 V
	065	0.65 V
	070	0.70 V
	075	0.75 V
	080	0.80 V
	085	0.85 V
	090	0.90 V
	095	0.95 V
	100	1.00 V
	105	1.05 V
	110	1.10 V
	115	1.15 V
	120	1.20 V
	125	1.25 V
	130	1.30 V
	150	1.50 V
	180	1.80 V
	250	2.50 V
	280	2.80 V
	290	2.90 V
	330	3.30 V
	500	5.00 V
Package	DSE	WSON - 6 pin (1.5 mm × 1.5 mm)
Reel	R	Large reel

12.2 Documentation Support

12.2.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3703. The *TPS3703 evaluation module* (and *related user guide*) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore .

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.7 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3703A3250DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-45 to 125	LB	Samples
TPS3703A4080DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JQ	Samples
TPS3703A4110DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	IL	Samples
TPS3703A4330DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JU	Samples
TPS3703A5075DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JS	Samples
TPS3703A5085DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JR	Samples
TPS3703A5120DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	J7	Samples
TPS3703A5180DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JT	Samples
TPS3703A5330DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	J6	Samples
TPS3703A5500DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	J8	Samples
TPS3703A6330DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	JV	Samples
TPS3703A7330DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	K5	Samples
TPS3703B6050DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	J9	Samples
TPS3703F6050DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3703 :

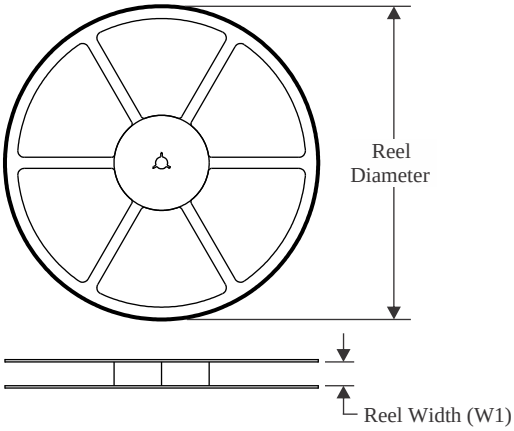
- Automotive : TPS3703-Q1

NOTE: Qualified Version Definitions:

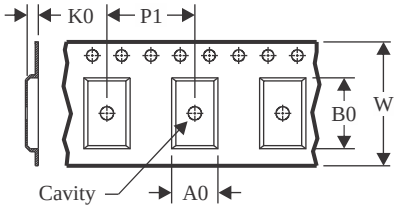
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

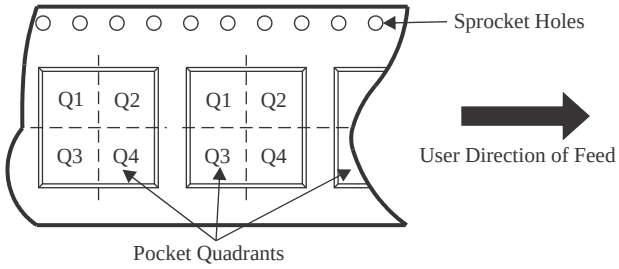


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

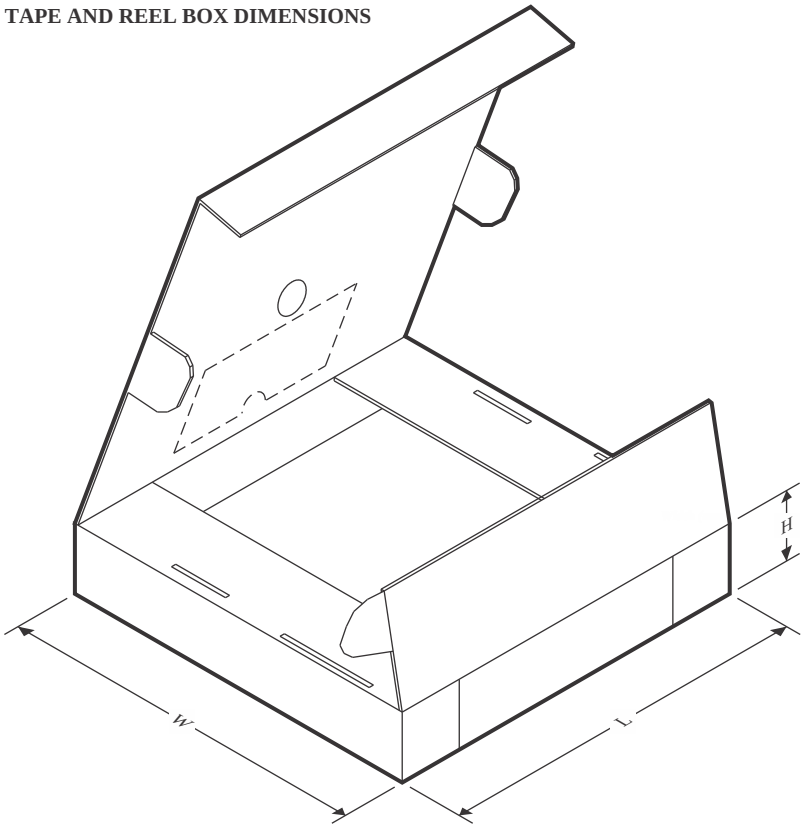


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3703A3250DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4080DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A4080DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4110DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A4110DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A4330DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5075DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5075DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A5085DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A5085DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5120DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5180DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5330DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5500DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A5500DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A6330DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3703A6330DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703A7330DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703A7330DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703B6050DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS3703B6050DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3703F6050DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3703A3250DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4080DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A4080DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4110DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A4110DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A4330DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5075DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5075DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A5085DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A5085DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5120DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5180DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5330DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5500DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A5500DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A6330DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703A6330DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703A7330DSER	WSON	DSE	6	3000	205.0	200.0	33.0

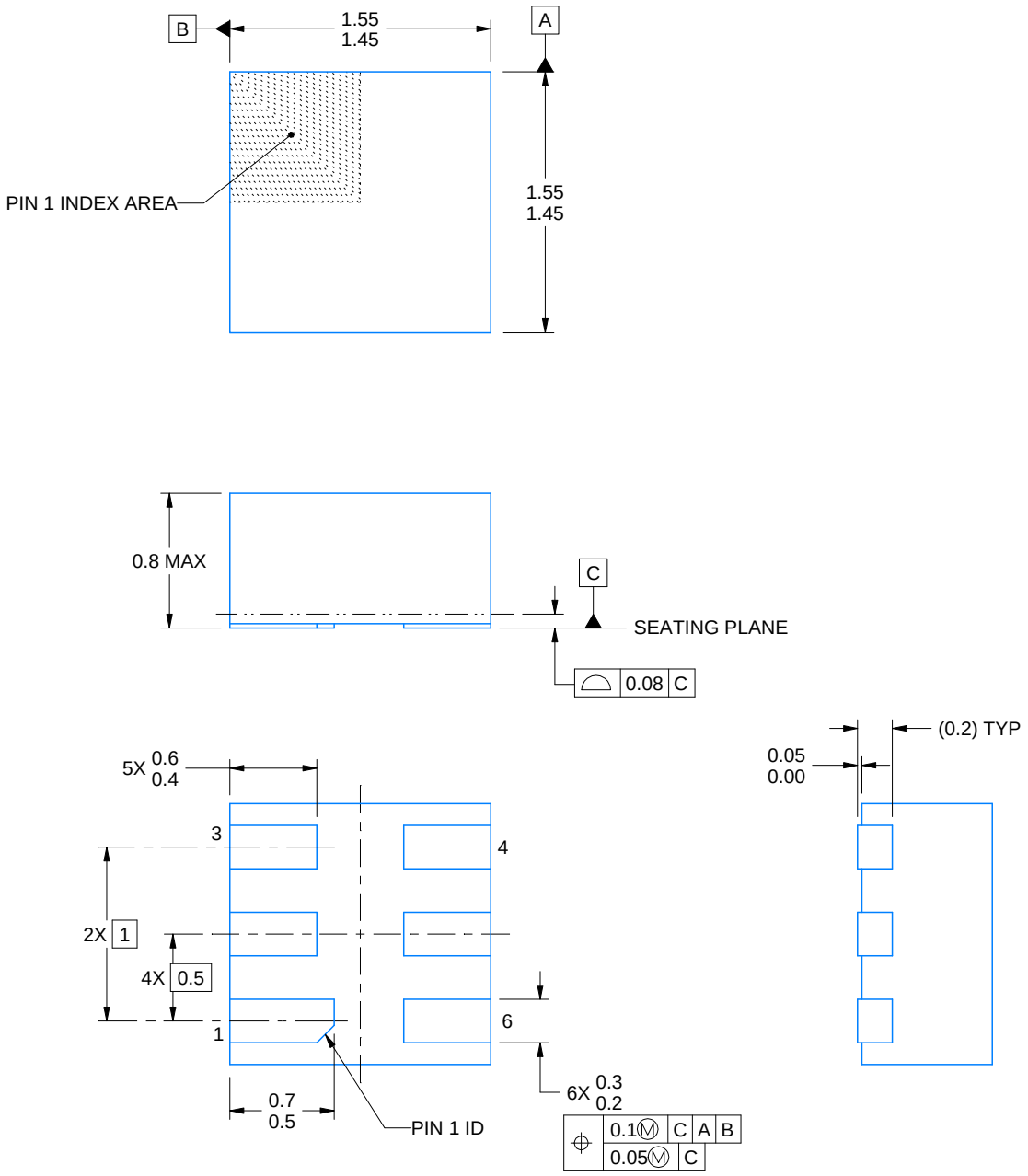
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3703A7330DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703B6050DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS3703B6050DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3703F6050DSER	WSON	DSE	6	3000	205.0	200.0	33.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

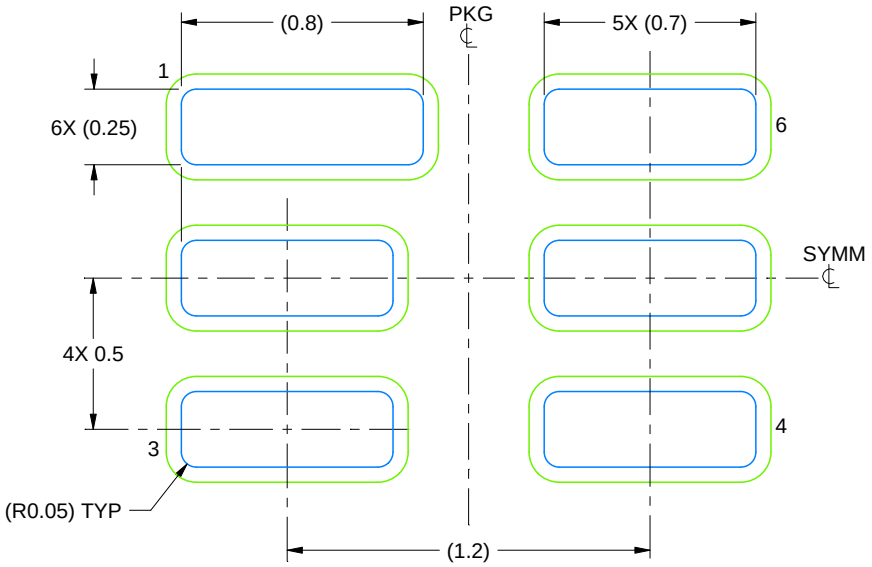
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

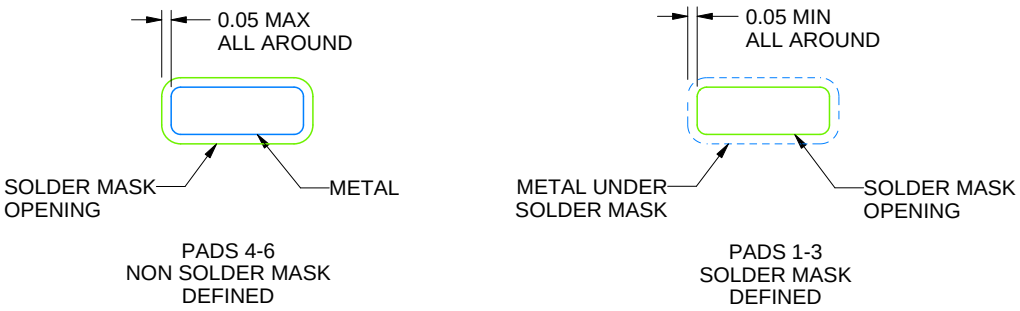
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

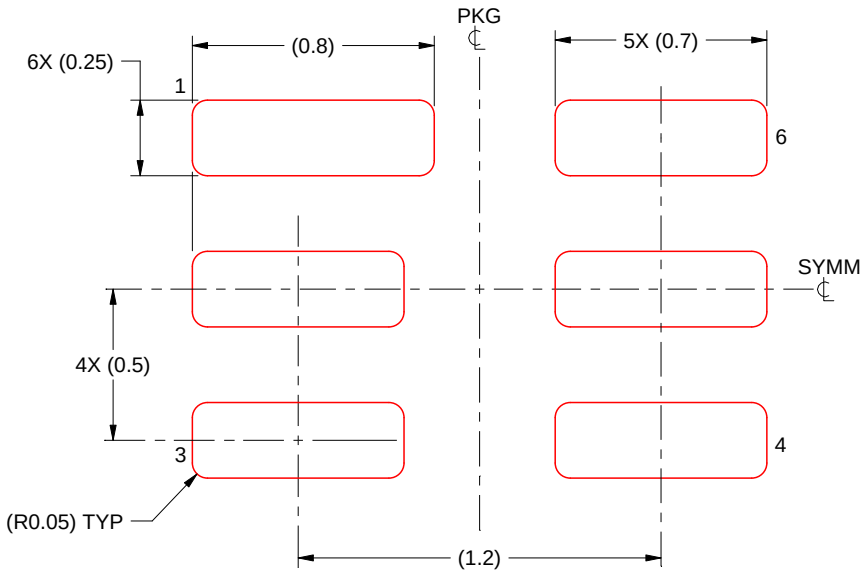
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265