TPS3704-Q1 車載対応、クワッド / トリプル / デュアル / シングル・チャネル、ウィンドウ形式または標準形式の電圧スーパーバイザ

1 特長

- ASIL-A 機能安全準拠
  - 機能安全アプリケーション向け開発
  - ISO 26262 システムの設計に役立つ資料
  - ASIL D までの決定論的能力
  - ASIL A までのハードウェア機能
- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1：-40℃～+125℃
- 1～4 チャネルで最新の SoC を監視
  - ±0.25% (標準値) の高いスレッショルド精度
  - ウィンドウ、UV、または OV 電圧監視用に各チャネルを構成
  - チャネルごとにウィンドウ許容範囲 [3%～11% (標準値*)] をプログラム可能
  - 可変バージョン用の使いやすい計算ツール
  - テキサス・インスツルメンツの各種プロセッサ (AM26x、AM62x、TDA4) のコアと GPIO の各レールを監視する目的で設計
- 低消費電力の小型ソリューション
  - 静止電流 5.5µA (標準値)
  - 小型 6 ピン SOT23 パッケージ (2.9mm × 1.6mm)
- 追加機能
  - 内蔵のヒステリシスにより、リセット時の誤トリップを防止：0.75% (標準値)
  - 23 の固定時間遅延オプション (20µs から 1200ms まで選択可能)
  - オープンドレインまたはプッシュプル出力トポロジを利用可能

2 アプリケーション

- 先進運転支援システム (ADAS)
- 車載用インフォテインメントおよびクラスタ
- HEV/EV
- ボディ・エレクトロニクスおよび照明

3 概要

TPS3704-Q1 は ASIL-A に準拠した低消費電力の高精度ウィンドウ (UV +OV) 電圧スーパーバイザであり、構成可能で、8 ピン (1.6mm × 2.9mm) の SOT-23 パッケージで供給されます。この高精度 (±0.25%) スーパーバイザは、クワッド、トリプル、デュアル、またはシングル チャネル オプションで供給されます。各チャネルは、対称型または非対称型にすることができる上限スレッショルドと下限スレッショルドの許容誤差により、過電圧 / 低電圧ウィンドウ検出を独自にカスタマイズできます。

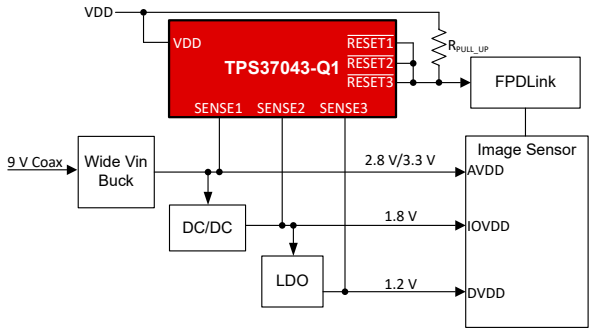
TPS3704-Q1 は高分解能で解高精度のスレッショルド検出を採用しており、低電圧の電源レールで動作し、電源許容誤差が狭いシステム向けに設計されています。また、低いスレッショルド ヒステリシスと固定のリセット遅延機能が組み込まれているため、複数の電圧レール監視中の誤ったリセット信号の発生が防止されます。

TPS3704-Q1 は、外付け抵抗なしで過電圧および低電圧リセットのスレッショルドを設定できるため、安全性システムの信頼性が向上し、精度、コスト、ソリューション サイズ全体が最適化されます。SENSEx ピンでは、柔軟性ある設計を目指し、外部抵抗のオプション使用がサポートされています。VDD ピンと SENSEx ピンは独立しており、VDD 以外のレール電圧を監視することや、プッシュ ボタン入力を使用することもできます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS3704-Q1	DDF (8 ピン SOT-23)	1.6mm × 2.9mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路

Table of Contents

4 Device Nomenclature

図 4-1 shows the device naming nomenclature to compare the different device variants. See 表 9-1 for a more detailed explanation. See 表 4-1 or 表 9-2 for the available device variants.

表 4-1. Device Threshold Table

ORDERABLE PART NAME	VARIANT(4)	NUM OF CHAN.	RESET TIME	SENSE1(2) (3)	SENSE2(2) (3)	SENSE3(2) (3)	SENSE4(2) (3)
TPS37042BJOFDDFRQ1	ADJ	2	10ms	0.8V (±4%)	0.8V (±4%)	-	-
TPS37042A3OFDDFRQ1	Fixed	2	10ms	3.3V (±5%)	1.2V (±5%)	-	-
TPS37042ZJOFDDFRQ1(1)	Fixed	2	10ms	1.95V (±4%)	3.8V (±6%)	-	-
TPS37043DJOFDDFR(1)	ADJ/Fixed	3	10 ms	3.3V (-11%)	1.2V (-11%)	0.8V (-8%)	-
TPS37043A4OFDDFRQ1	Fixed	3	10ms	2.8V (±5%)	1.8V (±5%)	1.2V (±5%)	-
TPS37043A8OFDDFRQ1	Fixed	3	10ms	3.3V (±5%)	1.8V (±5%)	1.0V (±5%)	-
TPS37043CPOFDDFRQ1(1)	ADJ/Fixed	3	10ms	3.3V (±4%)	0.75V (±4%)	0.8V (±3%)	-
TPS37043ZJOFDDFRQ1(1)	Fixed	3	10ms	0.95V (±4%)	1.35V (±4%)	1.8V (±4%)	-
TPS37043LJOFDDFRQ1(1)	ADJ	3	10ms	0.4V (±5%)	0.4V (±5%)	0.8V (±5%)	-
TPS37043CJOFDDFRQ1(1)	ADJ	3	10ms	0.8V (±6%)	0.8V (±6%)	0.8V (±6%)	-
TPS37043MJOFDDFRQ1(1)	ADJ	3	10ms	0.4V (±7%)	0.4V (±7%)	0.8V (±7%)	-
TPS37043A5OFDDFRQ1 (1)	Fixed	3	10ms	3.3V (±4%)	1.8V (±4%)	1.2V (±4%)	-
TPS37043BJOFDDFRQ1	ADJ	3	10ms	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)	-
TPS37044BJOFDDFR	ADJ	4	10 ms	0.8 V (±4%)	0.8 V (±4%)	0.8 V (±4%)	0.8 V (±4%)
TPS37044LJOJDDFR(1)	ADJ	4	35ms	0.4V (±5%)	0.4V (±5%)	0.8V (±5%)	0.8V (±5%)
TPS37044BJOFDDFRQ1	ADJ	4	10ms	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)
TPS37044CJOFDDFRQ1(1)	ADJ	4	10ms	0.8V (±6%)	0.8V (±6%)	0.8V (±6%)	0.8V (±6%)
TPS37044MJOFDDFRQ1(1)	ADJ	4	10ms	0.4V (±7%)	0.4V (±7%)	0.8V (±7%)	0.8V (±7%)
TPS37044A4OGDDFRQ1	Fixed	4	15ms	3.3V (±8%)	1.8V (±4%)	1.15V (±6%)	1.15V (±6%)

(1) Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options
(2) Listed percentage denotes window tolerance, see 図 6-1 for more information
(3) VIT threshold of 0.8V and 0.4V signifies an adjustable channel
(4) ADJ denotes an adjustable voltage threshold set by an external resistor divider, see Adjustable Voltage Thresholds for more information

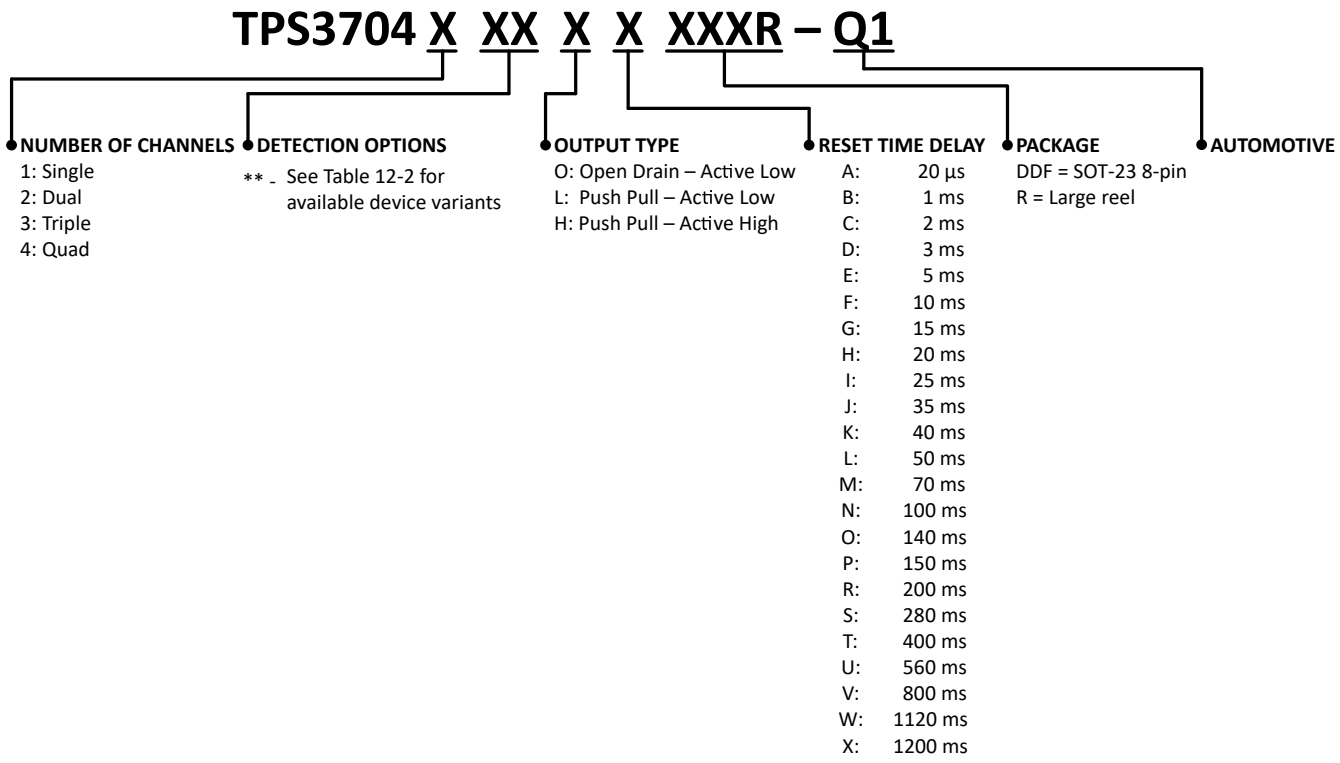


図 4-1. Device Naming Convention

5 Pin Configuration and Functions

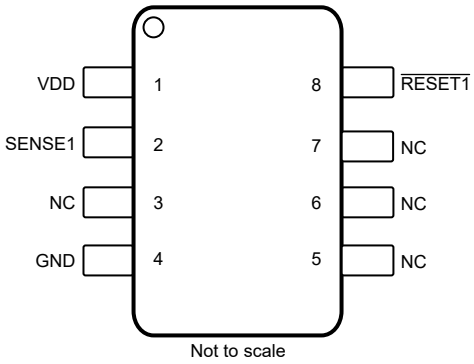


図 5-1. DDF Package
8-PIN SOT23
TPS37041-Q1 (Top View)

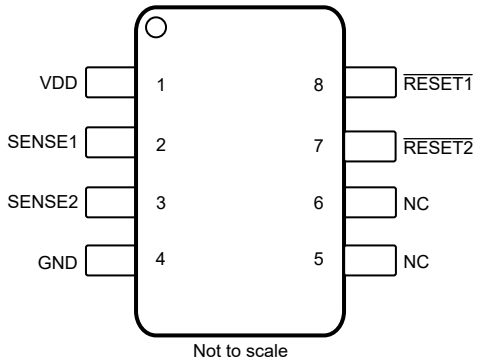


図 5-2. DDF Package
8-PIN SOT23
TPS37042-Q1 (Top View)

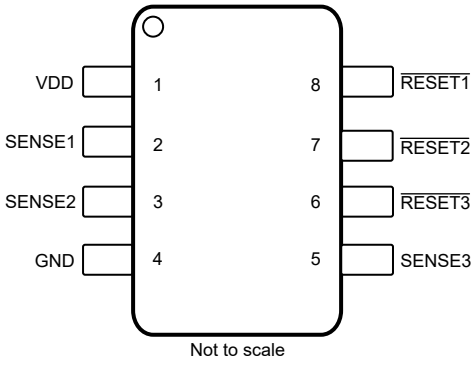


図 5-3. DDF Package
8-PIN SOT23
TPS37043-Q1 (Top View)

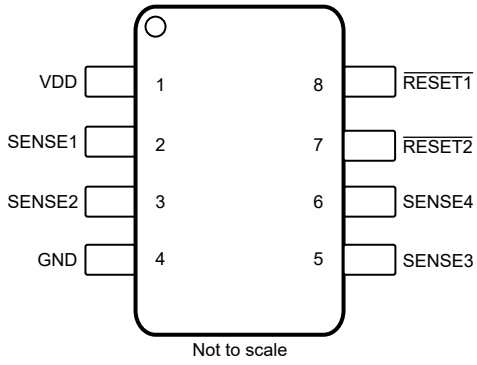


図 5-4. DDF Package
8-PIN SOT23
TPS37044-Q1 (Top View)

表 5-1. Pin Functions

PIN					I/O	DESCRIPTION
NAME	TPS37041-Q1	TPS37042-Q1	TPS37043-Q1	TPS37044-Q1		
VDD	1	1	1	1	I	Supply Input. Bypass with a 0.1-µF capacitor to GND.
SENSE1	2	2	2	2	I	Connect directly to a monitored voltage. $\overline{\text{RESET1}}$/RESET1 is asserted when SENSE1 falls outside of the window threshold. No external capacitor is required for this SENSE1 pin. For the TPS37044-Q1 (quad version) $\overline{\text{RESET1}}$/RESET1 asserts when either SENSE1 or SENSE2 fall outside of the window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. Leave this pin floating if not used.
SENSE2	—	3	3	3	I	Connect directly to a monitored voltage. $\overline{\text{RESET2}}$/RESET2 is asserted when SENSE2 falls outside of window threshold. No external capacitor is required for the SENSE2 pin. For the TPS37044-Q1 (quad version) $\overline{\text{RESET1}}$/RESET1 asserts when either SENSE1 or SENSE2 fall outside of the window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. Leave this pin floating if not used.
SENSE3	—	—	5	5	I	Connect directly to monitored voltage. $\overline{\text{RESET3}}$/RESET3 is asserted when SENSE3 falls outside of window threshold. No external capacitor is required for SENSE3 pin. For TPS37044-Q1 (quad version) $\overline{\text{RESET2}}$/RESET2 asserts when either SENSE3 or SENSE4 falls outside of window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. If the input pin is not being used, it can be left floating.
SENSE4	—	—	—	6	I	Connect directly to a monitored voltage. For TPS37044-Q1 (quad version) $\overline{\text{RESET2}}$/RESET2 asserts when either SENSE3 or SENSE4 fall outside of the window threshold. For noisy applications, placing a 10-nF to 100-nF ceramic capacitor close to this pin may be needed for optimum performance. Leave this pin floating if not used.
$\overline{\text{RESET1}}$	8	8	8	8	O	$\overline{\text{RESET1}}$/RESET1 asserts when SENSE1 falls outside of the overvoltage or undervoltage threshold window. $\overline{\text{RESET1}}$/RESET1 stays asserted for the reset timeout period after SENSE1 fall back within the window threshold. Active-low, open-drain reset output, requires an external pullup resistor. For the TPS37044-Q1, $\overline{\text{RESET1}}$/RESET1 asserts when either SENSE1 or SENSE2 falls outside of the window threshold. Leave this pin floating if not used. For the TPS37044F-Q1 option, any SENSEx channels that detect an overvoltage (OV) fault, this pin is asserted.
$\overline{\text{RESET2}}$	—	7	7	7	O	$\overline{\text{RESET2}}$/RESET2 asserts when SENSE2 falls outside of the overvoltage or undervoltage threshold window. $\overline{\text{RESET2}}$/RESET2 stays asserted for the reset timeout period after SENSE2 falls back within the window threshold. Active-low, open-drain reset output, requires an external pullup resistor. For the TPS37044-Q1, $\overline{\text{RESET2}}$/RESET2 asserts when either SENSE3 or SENSE4 fall outside of the window threshold. Leave this pin floating if not used. For the TPS37044F-Q1 option, any SENSEx channels that detect an undervoltage (UV) fault, this pin is asserted.
$\overline{\text{RESET3}}$	—	—	6	—	O	$\overline{\text{RESET3}}$/RESET3 asserts when SENSE3 falls outside of the overvoltage or undervoltage threshold window. $\overline{\text{RESET3}}$/RESET3 stays asserted for the reset timeout period after SENSE3 falls back within the window threshold. Active-low, open-drain reset output, requires an external pullup resistor. Leave this pin floating if not being used.
GND	4	4	4	4	—	Ground
NC	3,5,6,7	5,6	—	—	—	No connect

6 Specifications

6.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り) (1)

		最小値	最大値	単位
電圧	V_{DD}	-0.3	6.5	V
	V_{RESET1}、V_{RESET2}、V_{RESET3}	-0.3	6.5	V
	V_{SENSE1}、V_{SENSE2}、V_{SENSE3}、V_{SENSE4}	-0.3	6.5	V
電流	I_{RESET1}、I_{RESET2}、I_{RESET3}SINK		±20	mA
温度 (2)	連続総許容損失	「熱に関する情報」を参照		
	動作時の接合部温度、T_J	-40	150	℃
	自由気流での動作温度 (T_A)	-40	150	℃
	保管温度、T_{stg}	-65	150	℃

(1) 絶対最大定格 (AMR) を上回るストレスが加わった場合、デバイスに永続的な損傷が発生する可能性があります。これはストレスの定格のみに関するものであり、絶対最大定格において、または「推奨動作条件」に示された値を超える他のいかなる条件でも、本製品が正しく動作することを暗黙的に示すものではありません。AMR 定格の状態が長時間続くと、デバイスの信頼性に影響を与える可能性があります。

(2) このデバイスの消費電力は低いため、$T_J = T_A$ と想定されます。

6.2 ESD 定格

				値	単位
$V_{(ESD)}$	静電気放電	人体モデル (HBM)、ANSI/ESDA/JEDEC JS-001 準拠 (1)		±2000	V
		荷電デバイス・モデル (CDM)、AEC Q100-011 準拠		±750	

(1) AEC Q100–002 は、HBM ストレス試験を ANSI/ESDA/JEDEC JS–001 仕様に従って実施しなければならないと規定しています

6.3 推奨動作条件

		最小値	公称値	最大値	単位
V_{DD}	電源ピンの電圧	1.7		6.0	V
$V_{SENSE1、2、3、4}$	入力ピンの電圧	0		6.0	V
V_{RESET1}、V_{RESET2}、V_{RESET3}	出力ピン電圧	0		6.0	V
I_{RESET1}、I_{RESET2}、I_{RESET3} SINK	出力ピンの電流シンク	0.3		5	mA
T_A	自由気流での動作温度	-40		125	℃

6.4 Thermal Information

THERMAL METRIC (1)		TPS3704x-Q1	UNIT
		DDF	
		PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 電気的特性

1.7V ≤ V_{DD} ≤ 6.0V、、$\overline{RESETx}$ 電圧 ($V_{\overline{RESETx}}$) = 10kΩ から V_{DD}、$\overline{RESETx}$ 負荷 = 10pF、および自由気流での動作温度範囲 – 40℃～125℃ (特に記述のない限り)。代表値は T_A = 25℃、代表条件は V_{DD} = 3.3V。

パラメータ		テスト条件	最小値	標準値	最大値	単位
V_{DD}	電源電圧		1.7		6.0	V
UVLO	低電圧誤動作防止 (1)	V_{DD} が 1.7V 未満で下降する	1.2	1.4	1.6	V
$UVLO_{(HYS)}$	UVLO ヒステリシス (2)	V_{DD} が 1.7V 未満で上昇する		65		mV
V_{POR}	パワー オン リセット電圧 (3)	$V_{OL\ (MAX)}$ = 0.3V、I_{OUT} = 15µA			0.7	V
V_{IT} 範囲	スレッショルドのプログラミング範囲		0.4		5.55	V
$V_{IT-\ (UV)}$	UV 精度 (25℃)			0.1		%
$V_{IT+\ (OV)}$	OV 精度 (25℃)			0.1		%
TOL_min	許容誤差プログラミングの最小値			3		%
TOL_max	許容誤差プログラミングの最大値			11		%
THR RES Low	スレッショルドのプログラミング分解能 Low	V_{IT} ≤ 0.8V		20		mV / ステップ
THR RES Mid	スレッショルドのプログラミング分解能 Mid	0.8V < V_{IT} ≤ 4.0V		0.5		% / ステップ
THR RES High	スレッショルドのプログラミング分解能 High	V_{IT} > 4.0V		20		mV / ステップ
V_{IT}	許容誤差を含む絶対スレッショルドの精度	V_{IT} < 0.8V	-1.6		1.6	%
V_{IT}	許容誤差を含む絶対スレッショルドの精度	V_{IT} = 0.8V～5.55V	-1		1	%
V_{HYS}	V_{IT} < 0.80V		1.1	1.4	1.7	%
V_{HYS}	V_{IT} ≥ 0.80V		0.40	0.75	1	%
I_{DD}	TPS3704x	V_{DD} ≤ 6.0V		5.5	15	µA
I_{SENSEx}	入力電流、SENSEx ピン	V_{SENSEx} = 5.5V		1	2.5	µA
I_{SENSE_ADJ}	入力電流、SENSE ピン (バイパスの内部分圧抵抗) - 調整可能バージョン	V_{SENSEx} = 5.5V			350	nA
V_{OL}	Low レベル出力電圧	VDD = 1.7V、I_{SINK} = 0.4mA			300	mV
V_{OL}	Low レベル出力電圧	VDD = 2V、I_{SINK} = 3mA			300	mV
V_{OL}	Low レベル出力電圧	VDD = 6.0V、I_{SINK} = 5mA			300	mV
$I_{(lkg)}$	オープン ドレイン出力リーク電流	V_{DD} = $V_{\overline{RESETx}}$= 6.0V			350	nA

(1) V_{DD} が UVLO 未満になると、$\overline{RESETx}$ ピンは Low に駆動されます。
(2) ヒステリシスは、トリポイント ($V_{IT-\ (UV)}$、$V_{IT+\ (OV)}$) と関連しています。

(3) V_{POR} は、制御された出力状態の最小 V_{DD} 電圧レベルです。スルーレート = 100mV/µs

6.6 タイミング要件

1.7V ≤ V_{DD} ≤ 6.0V、、$\overline{RESETx}$ 電圧 ($V_{\overline{RESETx}}$) = 10kΩ から V_{DD}、$\overline{RESETx}$ 負荷 = 10pF、および自由気流での動作温度範囲 – 40℃～125℃ (特に記述のない限り)。代表値は T_A = 25℃、代表条件は V_{DD} = 3.3V。

パラメータ		テスト条件	最小値	公称値	最大値	単位
t_D	リセット解放時間遅延	固定遅延オプション t_D < 4ms、オーバードライブ = 10%	-40	t_D	40	%
t_D	リセット解放時間遅延	固定遅延オプション t_D > 5ms、オーバードライブ = 10%	-30	t_D	30	%
t_{PD}	伝搬検出遅延 (1)	固定遅延時間 t_D > 1ms、オーバードライブ 10%			10	µs
$t_{GI(VIT-)}$	グリッチ耐性低電圧 (5% オーバードライブ) (2)			2		µs
$t_{GI(VIT+)}$	グリッチ耐性過電圧 (5% オーバードライブ) (2)			2		µs
t_R	出力立ち上がり (プッシュプル) (2) (3)			25		ns
t_R	出力立ち上がり時間 (オープンドレイン) (2) (3)			2.2		µs
t_F	出力立ち下がり時間 (2) (3)			0.2		µs
t_{STRT}	スタートアップ遅延 (4)			1		ms

(1) スレッショルド トリップ ポイント ($V_{IT-(UV)}$ または $V_{IT+(OV)}$) から $\overline{RESETx}$ V_{OL} 電圧までの T_{PD} 測定値
(2) スレッショルドから 5% オーバードライブオーバードライブ % = [(V_{SENSEx} - V_{IT}) / V_{IT}]、ここでは V_{IT} は $V_{IT-(UV)}$ または $V_{IT+(OV)}$ を表します。
(3) 立ち上がり時間は V_{OL} から V_{OH} または ($V_{\overline{RESETx}}$)へ、立ち下がり時間は V_{OH} または ($V_{\overline{RESETx}}$) から V_{OL} へ出力が遷移します。
(4) パワーオン シーケンスの間、出力が適切な状態になる前に、V_{DD} が少なくとも t_{STRT} + t_D の間、$V_{DD(MIN)}$ 以上でなければなりません。VDD が $V_{DD(MIN)}$ と VPOR の間であるとき、$\overline{RESETx}$ ピンはアクティブになります。

6.7 Timing Diagrams

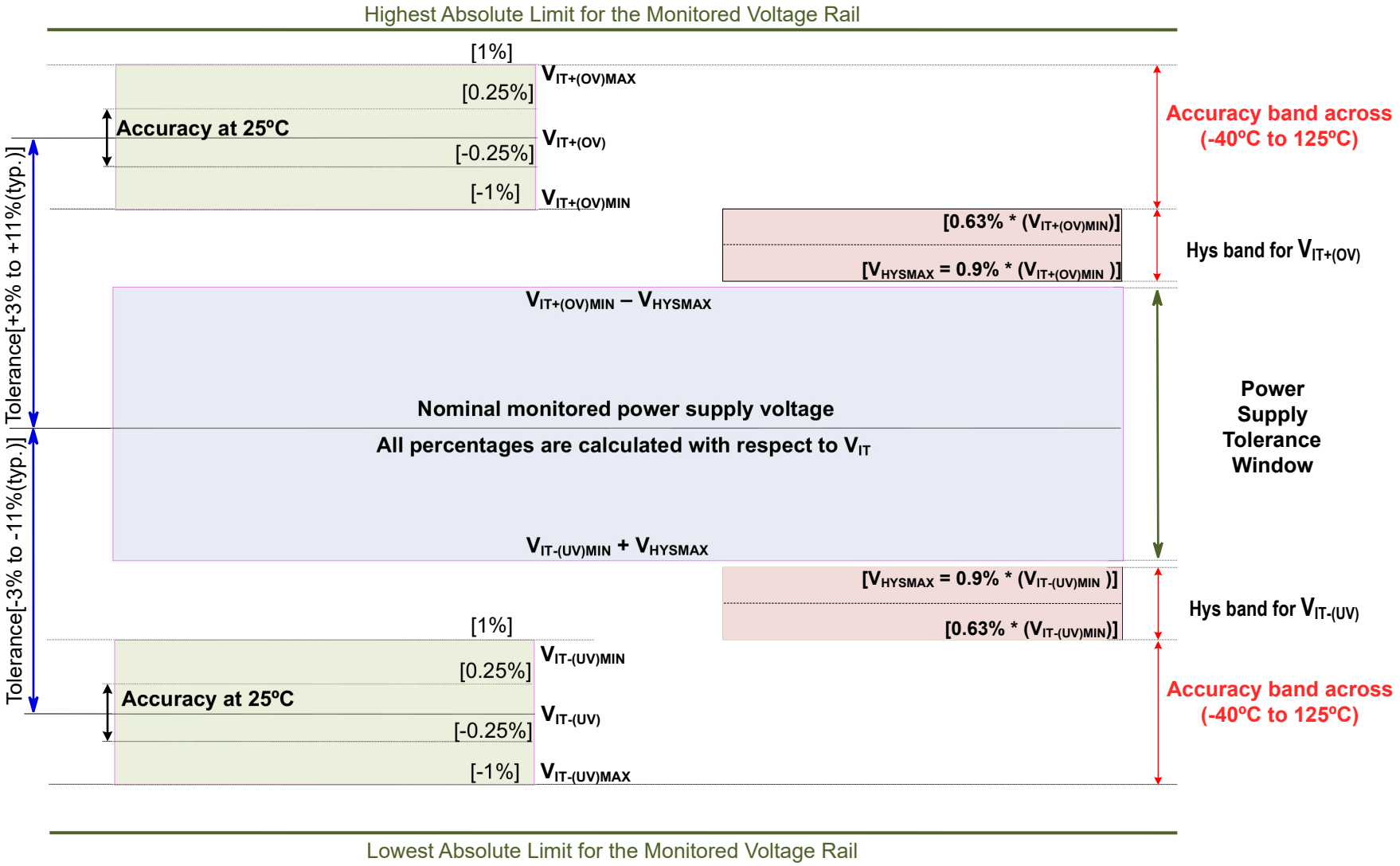
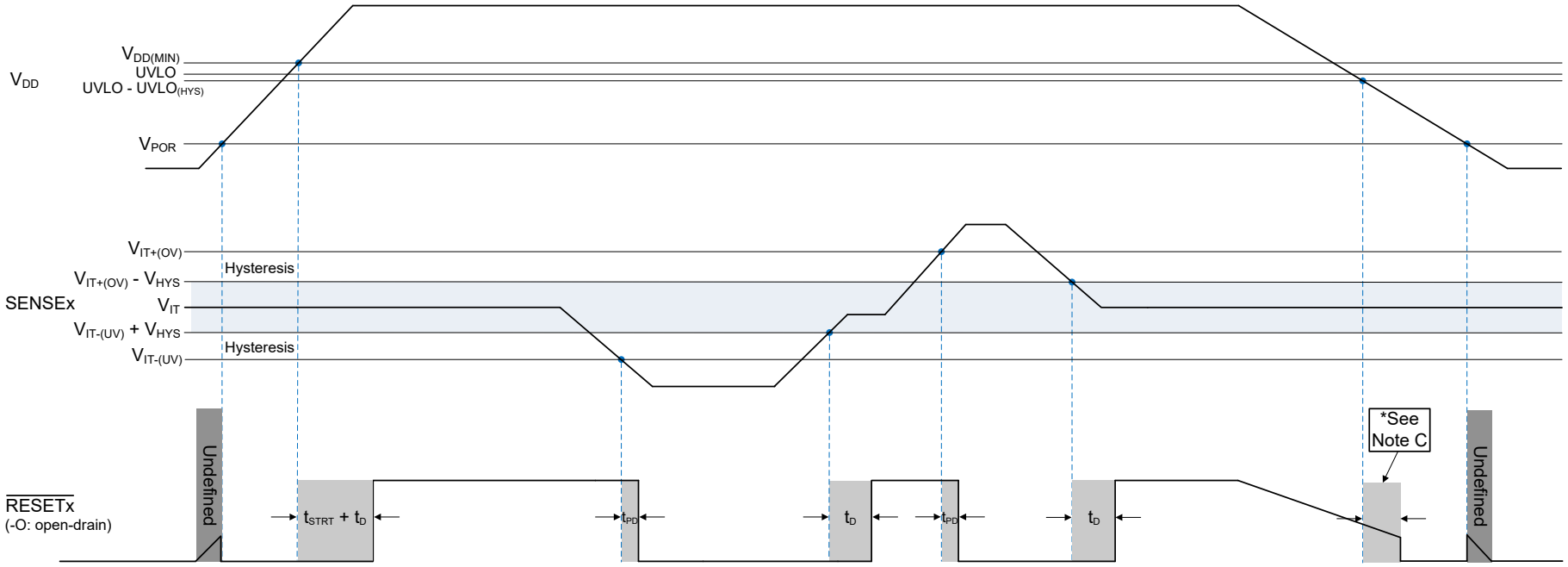


図 6-1. Voltage Threshold and Hysteresis Accuracy



A. Open-drain timing diagram assumes the $\overline{\text{RESETx}}$/RESETx pin is connected via an external pullup resistor to VDD.

B. Be advised that 図 6-2 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{PD}) time.

C. $\overline{\text{RESETx}}$/RESETx is asserted after a time delay, typical value of 100 µs, when VDD goes below the UVLO-$UVLO_{(HYS)}$ threshold.

図 6-2. SENSEx Timing Diagram

6.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.

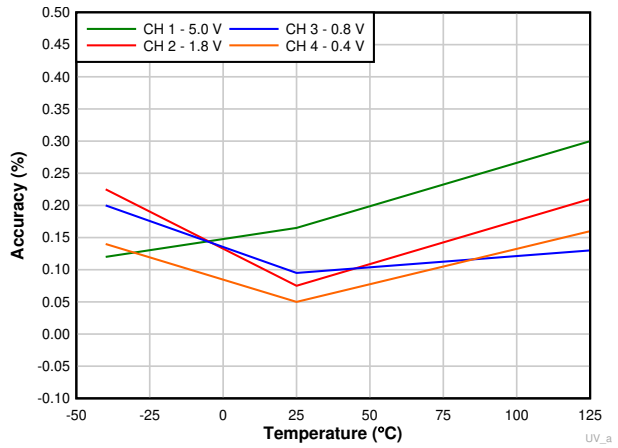


図 6-3. Undervoltage Accuracy vs Temperature

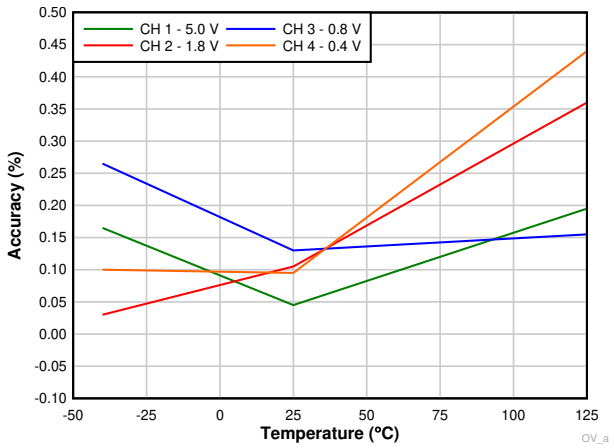


図 6-4. Overvoltage Accuracy vs Temperature

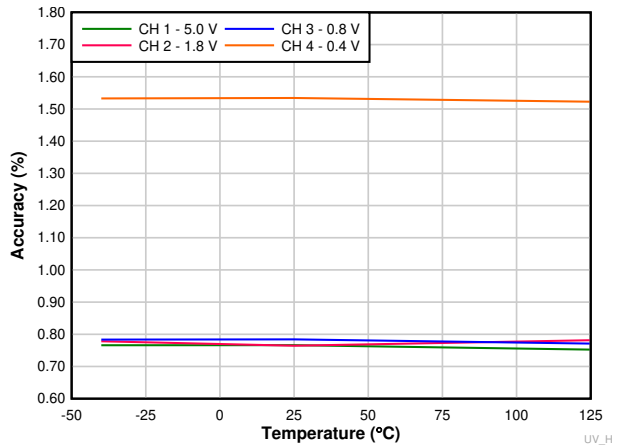


図 6-5. Undervoltage Hysteresis Voltage Accuracy vs Temperature

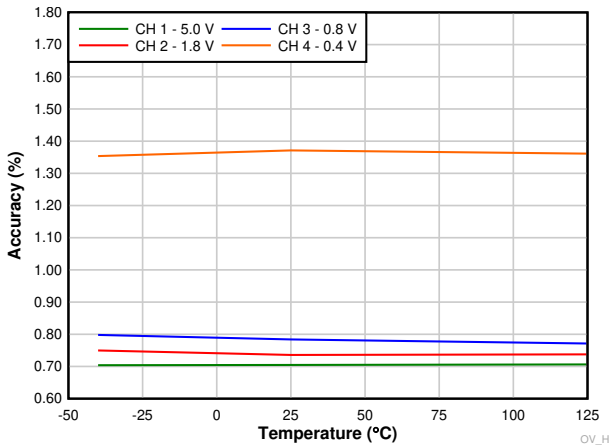
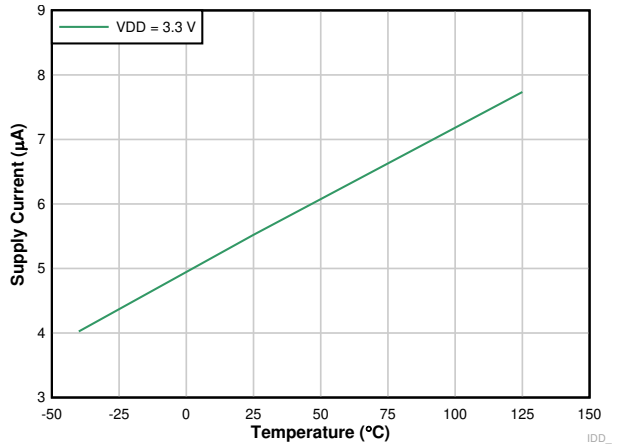
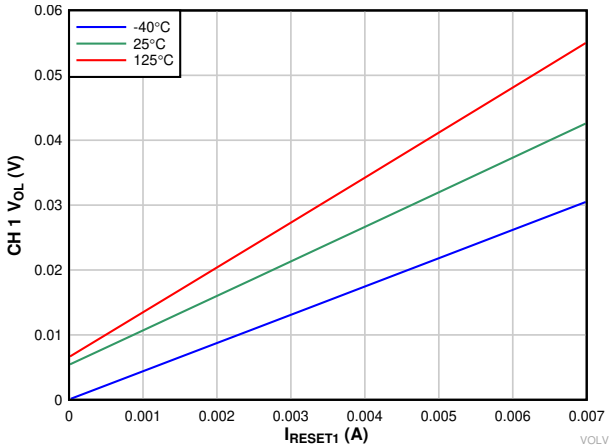


図 6-6. Overvoltage Hysteresis Voltage Accuracy vs Temperature



Output ($\overline{\text{RESET}}$x Pin) = High

図 6-7. Supply Current vs Temperature

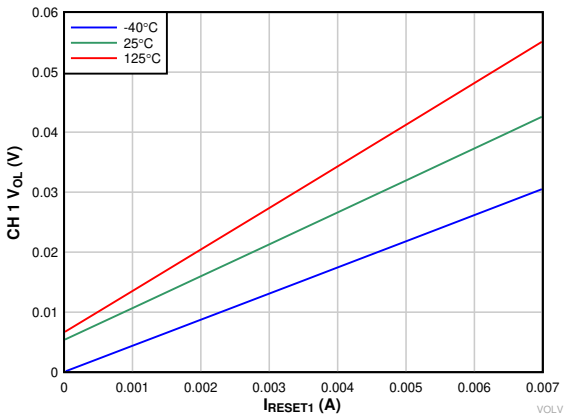


VDD = 1.7 V

図 6-8. Low-Level CH 1 Output Voltage vs $\overline{\text{RESET1}}$ Current

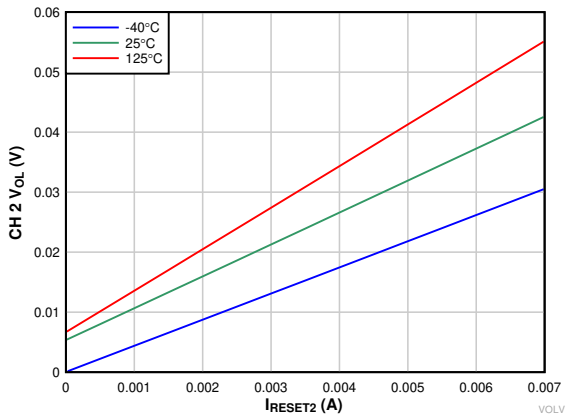
6.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull\text{-}upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.



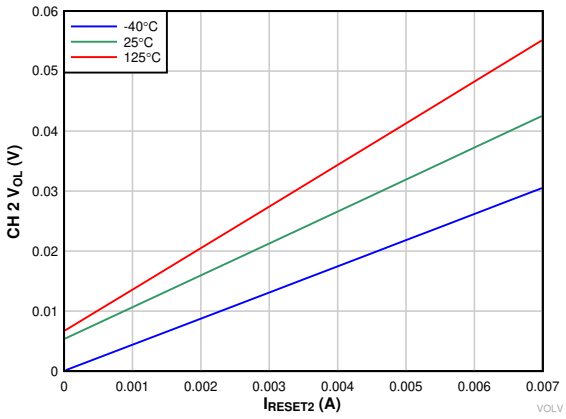
VDD = 5 V

図 6-9. Low-Level CH 1 Output Voltage vs $\overline{\text{RESET1}}$ Current



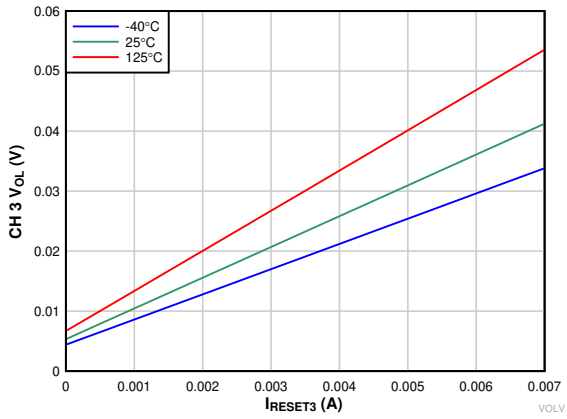
VDD = 1.7 V

図 6-10. Low-Level CH 2 Output Voltage vs $\overline{\text{RESET2}}$ Current



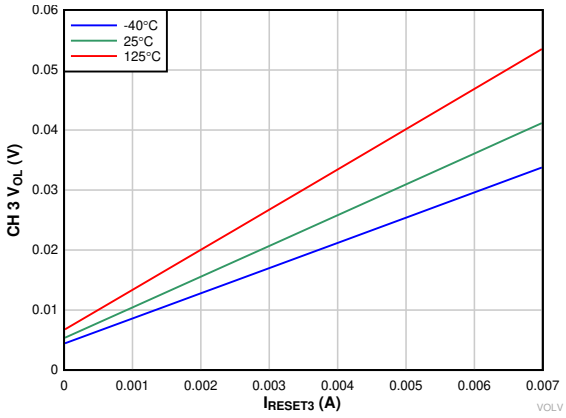
VDD = 5 V

図 6-11. Low-Level CH 2 Output Voltage vs $\overline{\text{RESET2}}$ Current



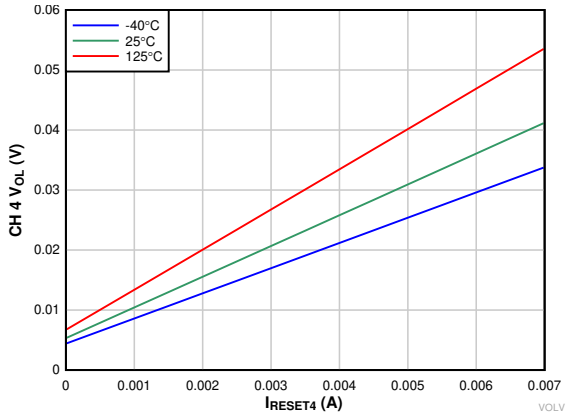
VDD = 1.7 V

図 6-12. Low-Level CH 3 Output Voltage vs $\overline{\text{RESET3}}$ Current



VDD = 5 V

図 6-13. Low-Level CH 3 Output Voltage vs $\overline{\text{RESET3}}$ Current

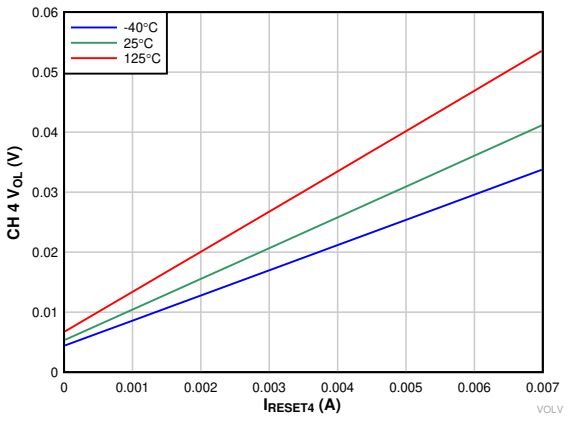


VDD = 1.7 V

図 6-14. Low-Level CH 4 Output Voltage vs $\overline{\text{RESET4}}$ Current

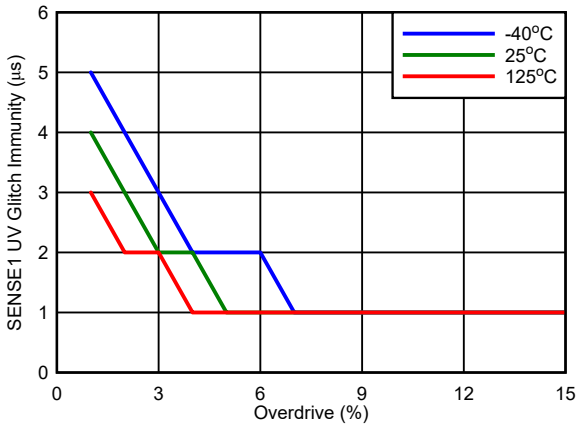
6.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.



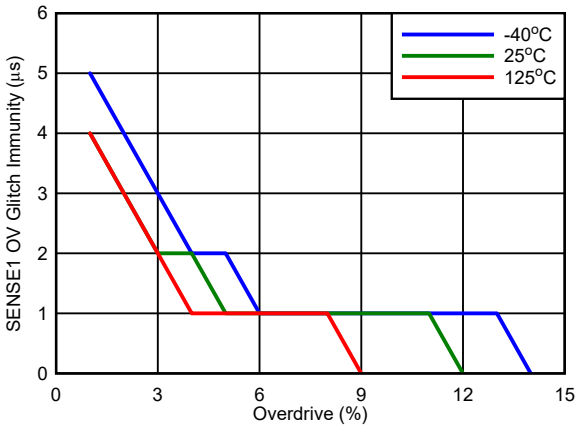
VDD = 5 V

図 6-15. Low-Level CH 4 Output Voltage vs $\overline{\text{RESET4}}$ Current



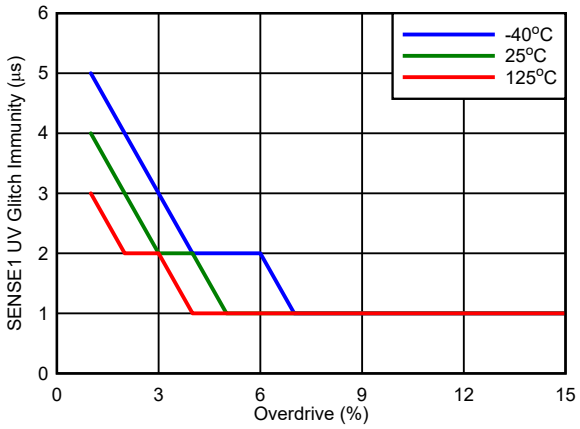
VDD = 1.7 V

図 6-16. SENSE1 Glitch Immunity (V_{IT-}) vs Overdrive



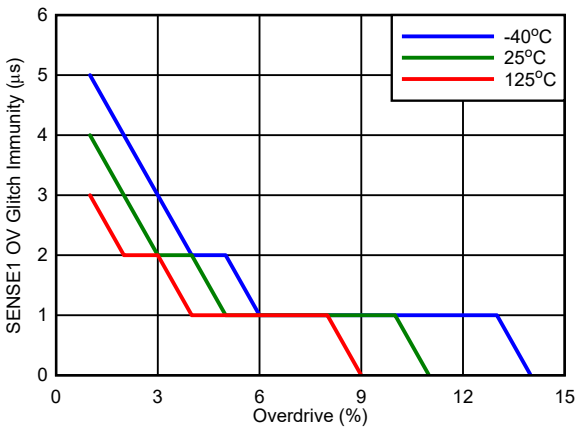
VDD = 1.7 V

図 6-17. SENSE1 Glitch Immunity (V_{IT+}) vs Overdrive



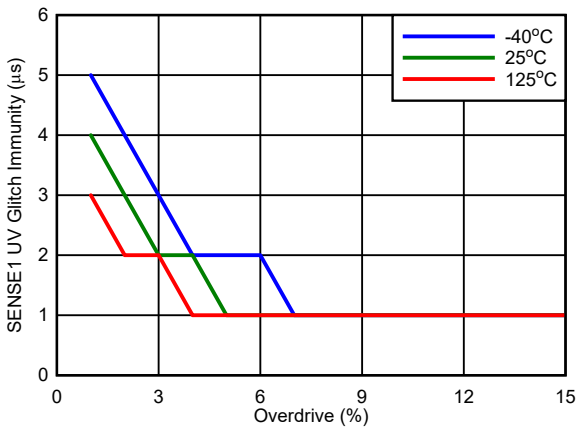
VDD = 3.3 V

図 6-18. SENSE1 Glitch Immunity (V_{IT-}) vs Overdrive



VDD = 3.3 V

図 6-19. SENSE1 Glitch Immunity (V_{IT+}) vs Overdrive



VDD = 5 V

図 6-20. SENSE1 Glitch Immunity (V_{IT-}) vs Overdrive

6.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3704x-Q1 device. Test conditions are T_A = 25°C, V_{DD} = 3.3 V, and $R_{pull-upx}$ = 10 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.

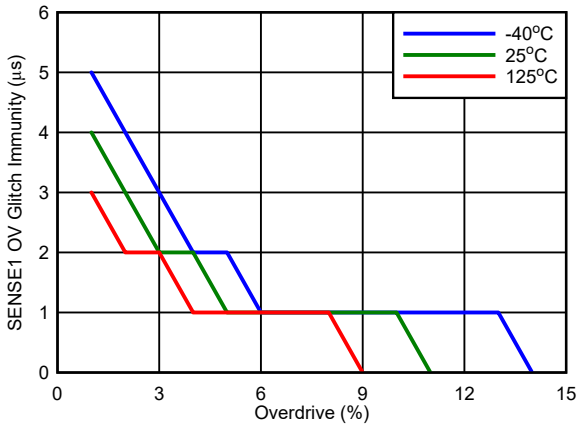


図 6-21. SENSE1 Glitch Immunity (V_{IT+}) vs Overdrive

7 Detailed Description

7.1 Overview

The TPS3704-Q1 (TPS37044-Q1, TPS37043-Q1, TPS37042-Q1, and TPS37041-Q1) is a family of quad, triple, dual, and single precision voltage supervisors where each channel has overvoltage and undervoltage detection capability. The TPS3704-Q1 features a highly accurate window threshold voltage where the upper and lower thresholds can be customized for symmetric or asymmetric tolerances. The reset signal for the TPS3704-Q1 is asserted, with a fault detection time delay (t_{PD} = 10 µs max), when the sense voltage is outside of the overvoltage and undervoltage thresholds.

The TPS3704-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors. The level of integration in the TPS3704-Q1 enables a total small solution size for any application.

The TPS3704-Q1 is able to monitor any voltage rail with high resolution (V_{IT} ≤ 0.8 V: 20-mV steps / V_{IT} > 0.8 V: 0.5% or 20-mV steps whichever is lower). Each channel in the TPS3704x-Q1 can be configured independently as a window, OV or UV supervisor. Also, the VIT threshold voltage for each channel can be asymmetric. For example, a channel that is configured as an overvoltage supervisor can be setup with a +5% tolerance whereas an undervoltage channel supervisor can be programmed with a -4% tolerance. If a window supervisor is configured, the voltage threshold tolerance can either be symmetrical or asymmetrical.

The TPS3704-Q1 device includes fixed reset time delay (t_D) options ranging from 20 µs to 1200 ms and can monitor up to four channels while maintaining an ultra-low I_Q current of 15 µA (maximum).

7.2 Functional Block Diagrams

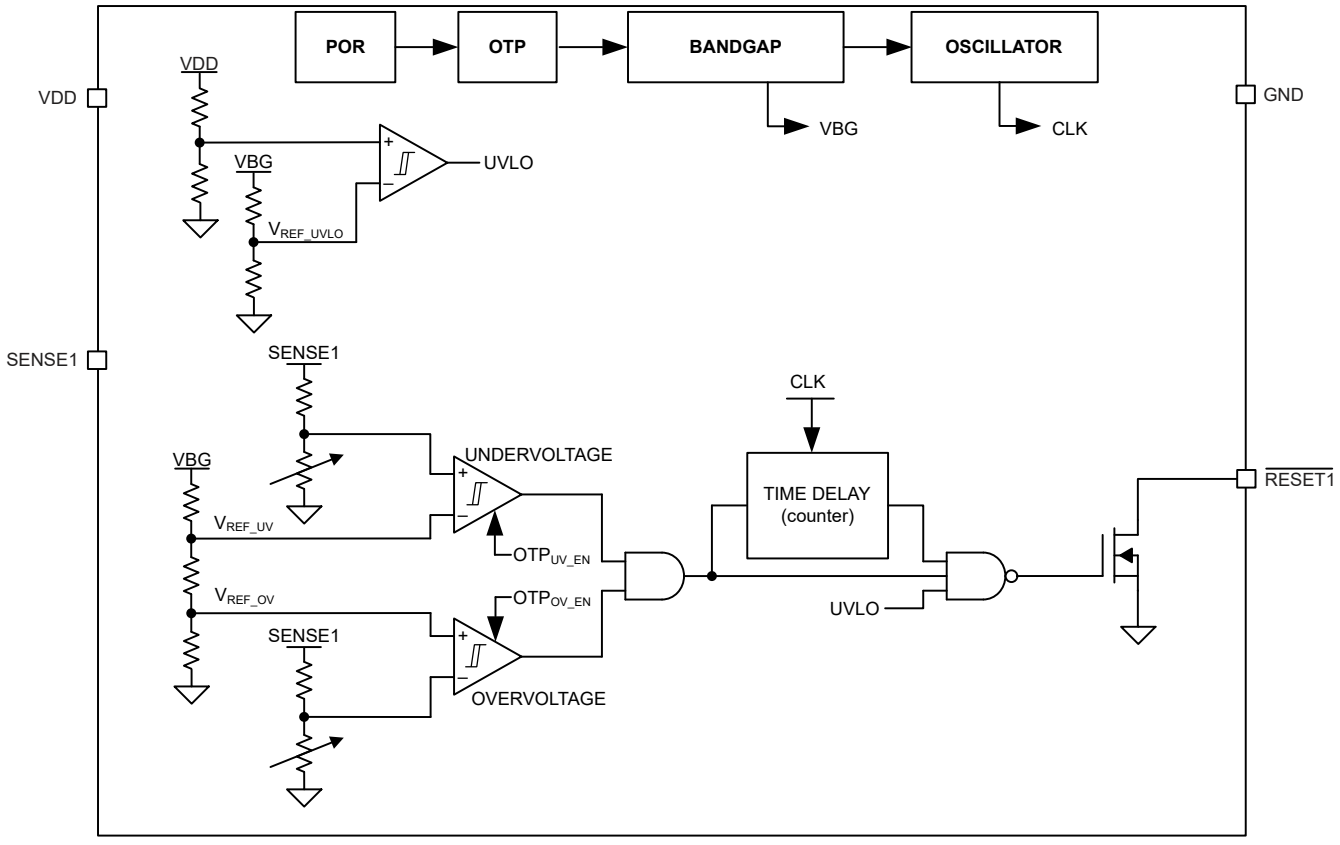


図 7-1. TPS37041-Q1 Single-Channel Functional Block Diagram

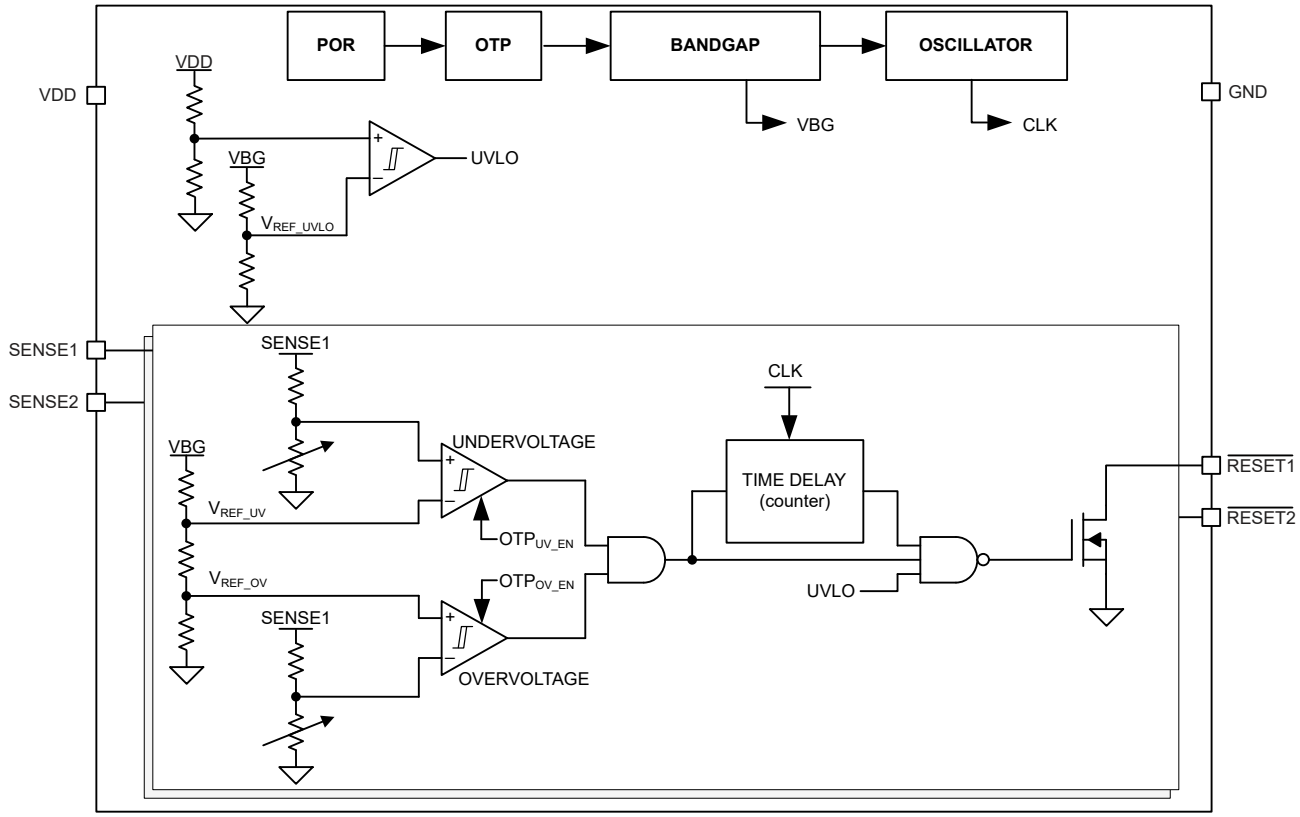


図 7-2. TPS37042-Q1 Dual-Channel Functional Block Diagram

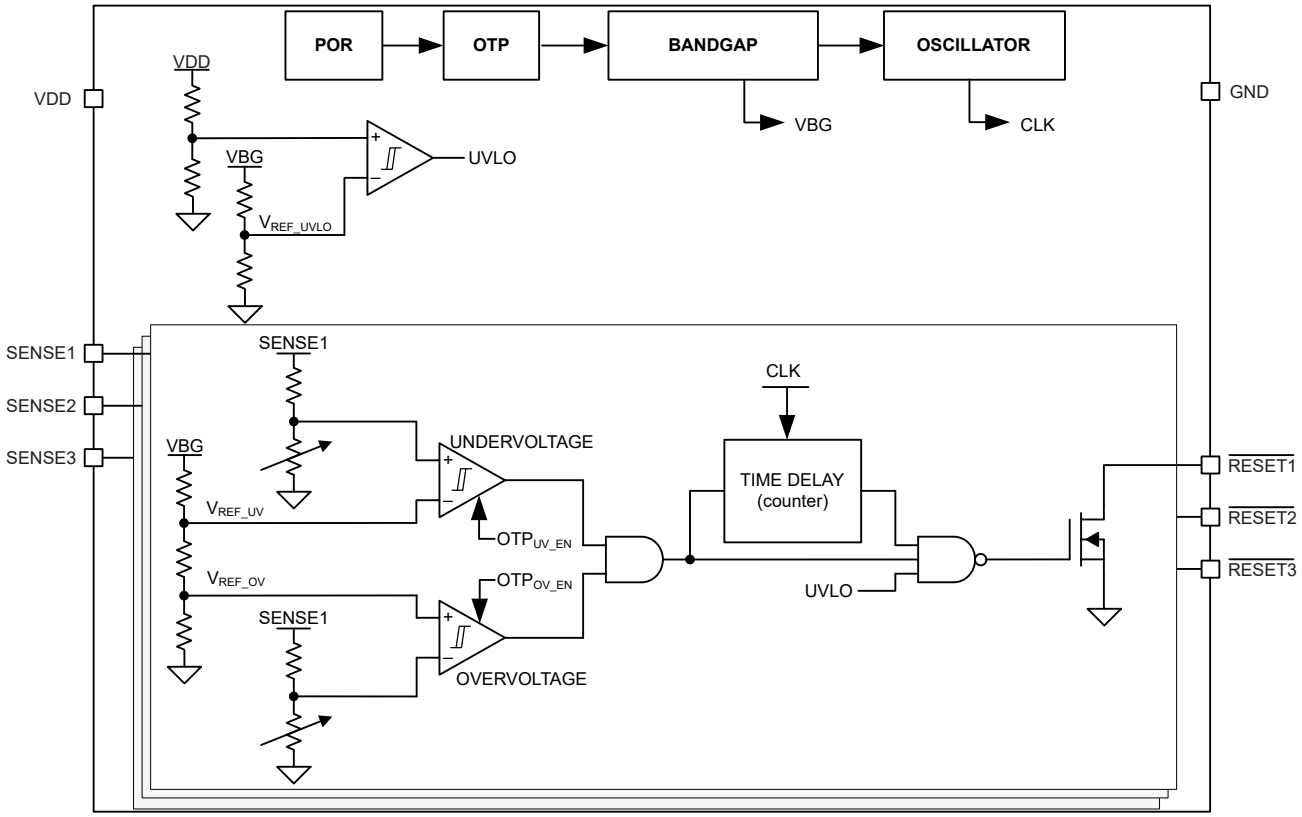


図 7-3. TPS37043-Q1 Triple-Channel Functional Block Diagram

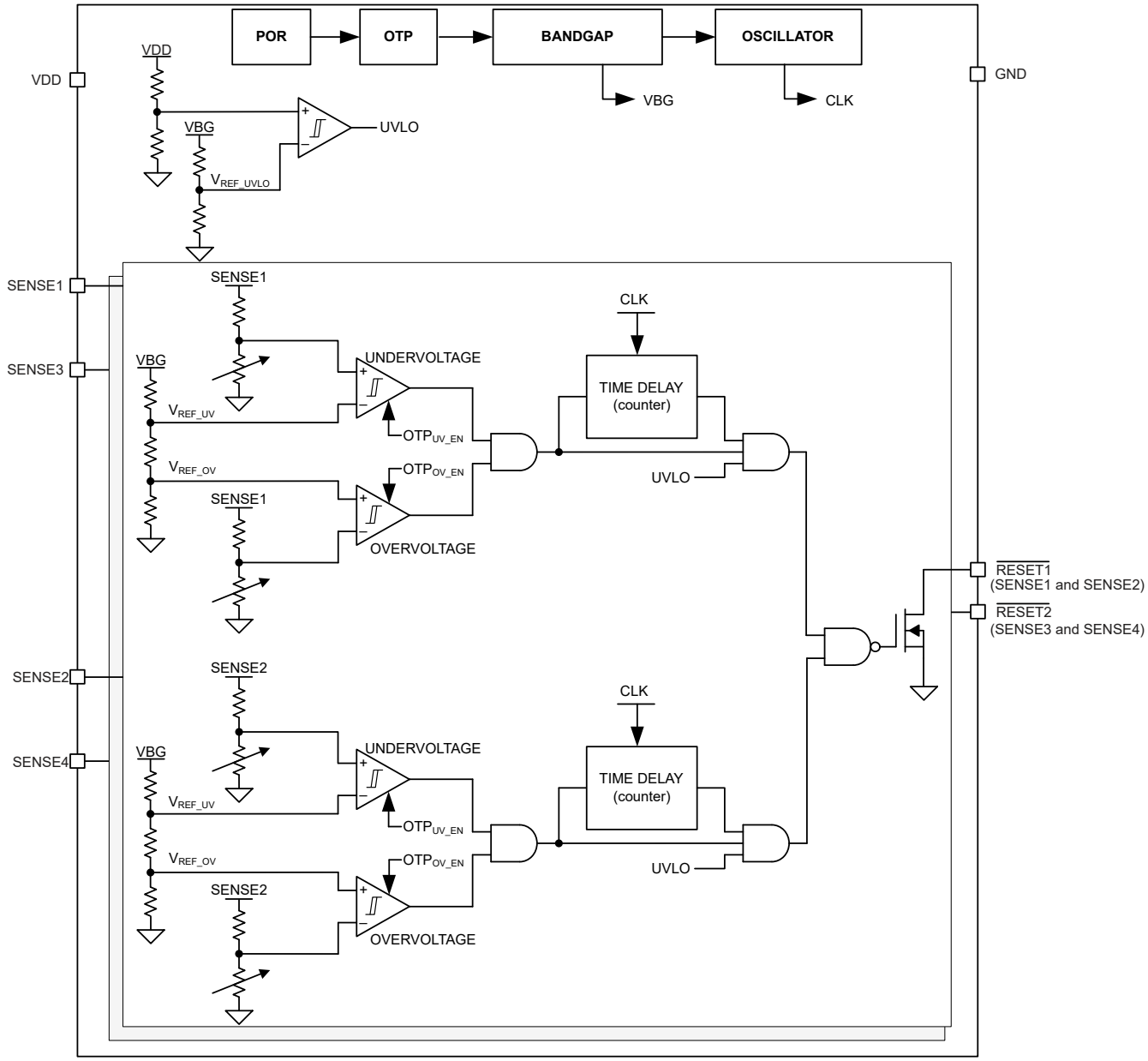


図 7-4. TPS37044-Q1 Quadruple-Channel Functional Block Diagram

*For available voltages, window tolerance, time delays, and UV/OV threshold options, see 表 9-2.

7.3 Feature Description

7.3.1 VDD

The TPS3704-Q1 is designed to operate from an input voltage supply range between 1.7 V to 6 V. The SENSEx pins are monitored by the internal comparator. VDD also functions as the supply for the internal band gap, internal regulator, state machine, buffers, and other control blocks. The reset signal is at a known state when VDD > V_{POR}. The undervoltage lockout forces the reset output to be asserted when VDD falls below the minimum VDD voltage.

The VDD capacitor is not required for this device; however, if the input supply is noisy, then good design practice is to place a 0.1-µF to 1-µF bypass capacitor between the VDD pin and the GND pin to make sure enough charge is available for the device to power up correctly. VDD must be at or above $V_{DD(MIN)}$ for start-up delay

(t_{STRT} + t_D) to begin and for the device to be fully functional.

7.3.2 SENSEx Input

The SENSEx input can vary from 0 V to 6 V, regardless of the device supply voltage used. The SENSEx pins are used to monitor critical voltage rails or push-button inputs. If the voltage on this pin drops below $V_{IT-(UV)}$ or goes above $V_{IT+(OV)}$, then $\overline{\text{RESETx}}$/RESETx is asserted. When the voltage on the SENSEx pin rises above the positive threshold voltage $V_{IT-(UV)}$ + V_{HYS} or goes below the negative threshold voltage $V_{IT+(OV)}$ - V_{HYS},

$\overline{\text{RESETx}}$/RESETx deasserts after the set $\overline{\text{RESETx}}$/RESETx delay time. The internal comparators have built-in hysteresis to make sure well-defined $\overline{\text{RESETx}}$/RESETx assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3704-Q1 combines comparators with a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. The TPS3704-Q1 is relatively immune to short transients on the SENSEx pin. Although not required in most cases, for noisy applications, good analog design practice is to place a 10-nF to 100-nF bypass capacitor at the SENSEx inputs to reduce sensitivity to transient voltages on the monitored signals.

7.3.2.1 Immunity to SENSEx Pins Voltage Transients

The TPS3704-Q1 is immune to short voltage transient spikes on the input SENSEx pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient.

Overdrive is defined by how much V_{SENSEx} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the $\overline{\text{RESETx}}$/RESETx outputs. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 1:

$$\text{Overdrive \%} = | (V_{SENSEx} - (V_{IT-(UV)} \text{ or } V_{IT+(OV)})) / V_{IT} \text{ (Nominal)} \times 100\% | \quad (1)$$

where:

- V_{SENSEx} is the voltage at the SENSEx pin
- V_{IT} (Nominal) is the nominal threshold voltage
- $V_{IT-(UV)}$ and $V_{IT+(OV)}$ represent the actual undervoltage or overvoltage tripping voltage

7.3.2.1.1 SENSEx Hysteresis

Overvoltage and undervoltage comparators include built-in hysteresis that provides noise immunity and ensures stable operation. For example, if the voltage on the SENSEx pin falls below $V_{IT-(UV)}$ or above $V_{IT+(OV)}$, then $\overline{\text{RESETx}}$/RESETx is asserted. When the voltage on the SENSEx pin is between the positive and negative threshold voltages, $\overline{\text{RESETx}}$/RESETx deasserts after the set $\overline{\text{RESETx}}$/RESETx delay time. 図 7-5 shows the relation between $V_{IT-(UV)}$,$V_{IT+(OV)}$ and the hysteresis voltage (V_{HYS}).

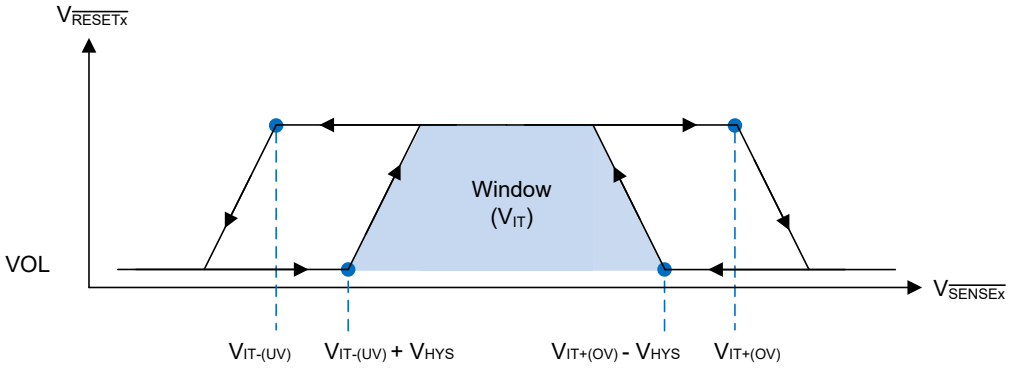


図 7-5. SENSEx Pin Hysteresis

7.3.3 $\overline{\text{RESETx}}$/RESETx

In a typical TPS3704-Q1 application, the $\overline{\text{RESETx}}$/RESETx output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the enable input of a voltage regulator [such as a DC/DC converter or low-dropout regulator (LDO)].

The TPS3704-Q1 has open-drain active low outputs that require an external pullup resistor to hold these lines high to the required voltage logic. Connect the external pullup resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To ensure proper voltage levels, give some consideration when choosing the external pullup resistor values. The external pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current. These values are specified in セクション 6.5. The open-drain output can be connected as a wired-OR logic with other $\overline{\text{RESETx}}$/RESETx open-drain pins.

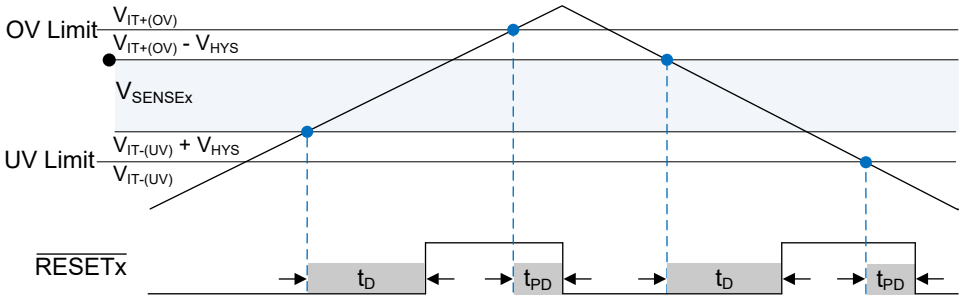


図 7-6. $\overline{\text{RESETx}}$ Output

7.4 Device Functional Modes

表 7-1. Functional Mode Truth Table

DESCRIPTION	CONDITION	VDD PIN	OUTPUT $\overline{\text{RESETx}}$ / (RESETx) PIN
Normal operation	$V_{IT-(UV)}$ < SENSEx < $V_{IT+(OV)}$	V_{DD} > $V_{DD(MIN)}$	High / (Low)
Normal operation (UV only)	SENSEx > $V_{IT-(UV)}$	V_{DD} > $V_{DD(MIN)}$	High / (Low)
Overvoltage detection	SENSEx > $V_{IT+(OV)}$	V_{DD} > $V_{DD(MIN)}$	Low / (High)
Undervoltage detection	SENSEx < $V_{IT-(UV)}$	V_{DD} > $V_{DD(MIN)}$	Low / (High)
UVLO engaged	$V_{IT-(UV)}$ < SENSEx < $V_{IT+(OV)}$	V_{POR} < V_{DD} < UVLO	Low / (High)

7.4.1 Normal Operation (V_{DD} > $V_{DD(MIN)}$)

When the voltage on V_{DD} is greater than $V_{DD(MIN)}$ for approximately (t_{STRT} + t_D), the $\overline{\text{RESETx}}$/RESETx output state corresponds to the SENSEx pin voltage with respect to the threshold limits. When SENSEx voltage is outside of threshold limits the $\overline{\text{RESETx}}$/RESETx voltage is asserted.

7.4.2 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage but greater than the power-on-reset voltage (V_{POR}), the $\overline{\text{RESETx}}$/RESETx pin is asserted, regardless of the voltage on the SENSEx pin.

7.4.3 Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) to internally pull the asserted output to GND, the $\overline{\text{RESETx}}$/RESETx signal is undefined and is not to be relied upon for proper device function.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Voltage Threshold Accuracy

Voltage monitoring requirements vary depending on the voltage supply tolerance of the device being powered. Because of the high precision of the TPS3704-Q1 (±1% max), the device allows for wider supply voltage margins and threshold headroom for tight tolerance applications.

For example, take a DC/DC regulator providing power to a core voltage rail of a microcontroller (MCU). The MCU has a tolerance of ±5% of the nominal output voltage of the DC/DC. The user sets an ideal voltage threshold of ±4%, which allows for ±1% of threshold accuracy. Because the TPS3704-Q1 threshold accuracy is ±1%, the user has more supply voltage margin, which can allow for a relaxed power supply design. This design gives flexibility to the DC/DC to use a smaller output capacitor or inductor because of a larger voltage window for voltage ripple and transients. There is also headroom between the minimum system voltage and voltage tolerance of the MCU to make sure that the voltage supply is never in the region of potential failure of malfunction without the TPS3704-Q1 asserting a reset signal.

図 8-1 shows the supply undervoltage margin and accuracy of the TPS3704-Q1 for the example explained in this section. Using a low accuracy supervisor cuts into the available budget for the power-supply ripple and transient response. This gives less flexibility to the user and a more stringent DC/DC converter design.

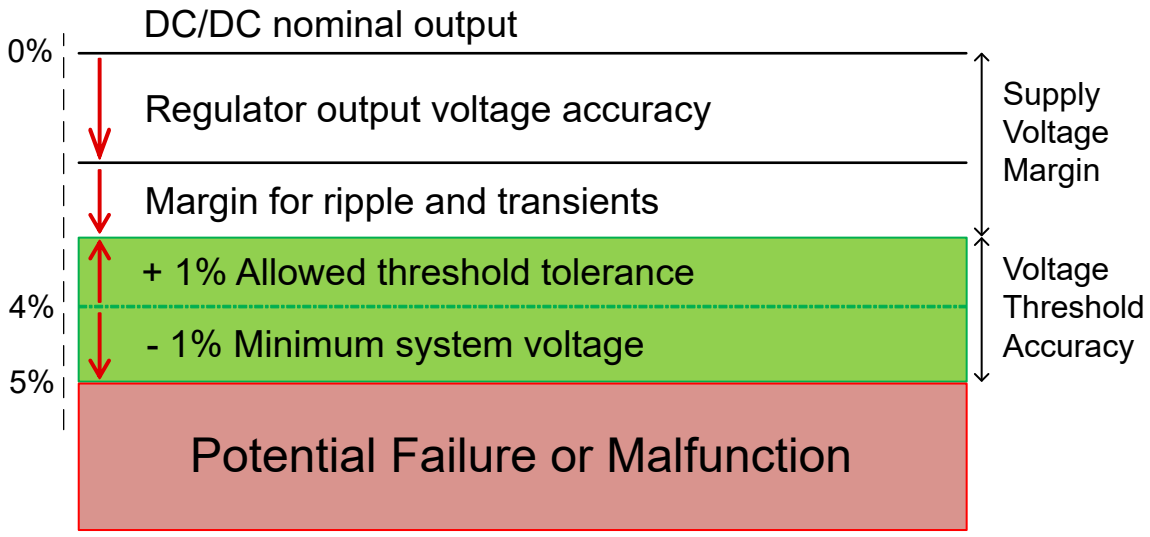


図 8-1. TPS3704-Q1 Voltage Threshold Accuracy

8.1.2 Adjustable Voltage Thresholds

The TPS3704-Q1 maximum accuracy (1%) allows for adjustable voltage thresholds using external resistors without adding major inaccuracies to the device. In case the desired monitored voltage is not available, external resistor dividers can be used to set the desired voltage thresholds. 図 8-2 illustrates an example of how to adjust the voltage threshold with external resistor dividers. For assistance in calulating the external resistors access the TPS3704 adjustable threshold voltage resistor calculator in the Design Tools and Simulation section of the TPS3704 product page. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using a voltage threshold device variant because of the bypass mode of the internal resistor ladder.

For example, consider a 2.0-V rail being monitored (V_{MON}) using the TPS37042BJOFDDFRQ1 variant. Using 式 2, R1 = 15 kΩ given that R2 = 10 kΩ, V_{MON} = 2 V, and V_{SENSE1} = 0.8 V. This device is typically meant to monitor a
0.8-V rail with ±4% voltage thresholds. This means that the device undervoltage threshold ($V_{IT-(UV)}$) and overvoltage threshold ($V_{IT+(OV)}$) is 0.768 V and 0.832 V, respectively. Using 式 2, V_{MON} = 1.92 V when V_{SENSE1} = $V_{IT-(UV)}$. This can be denoted as V_{MON-}, the monitored undervoltage threshold where the device asserts a reset signal. Using 式 2 again, the monitored overvoltage threshold (V_{MON+}) = 2.08 V when V_{SENSE1} = $V_{IT+(OV)}$. If a wider tolerance or UV only threshold is desired, use a device variant listed in
表 9-2 to determine which device part number matches which application.

$$V_{SENSE1} = V_{MON} \times (R_2 / (R_1 + R_2)) \quad (2)$$

There are inaccuracies that must be taken into consideration when adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE1 pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for design specifications. The internal sense resistance R_{SENSE1} can be calculated by the sense voltage V_{SENSE1} divided by the sense current I_{SENSE1} as shown in 式 4. V_{SENSE1} can be calculated using
式 2 depending on the resistor divider and monitored voltage. I_{SENSE1} can be calculated using 式 3.

$$I_{SENSE1} = [(V_{MON} – V_{SENSE1}) / R_1] – (V_{SENSE1} / R_2) \quad (3)$$

$$R_{SENSE1} = V_{SENSE1} / I_{SENSE1} \quad (4)$$

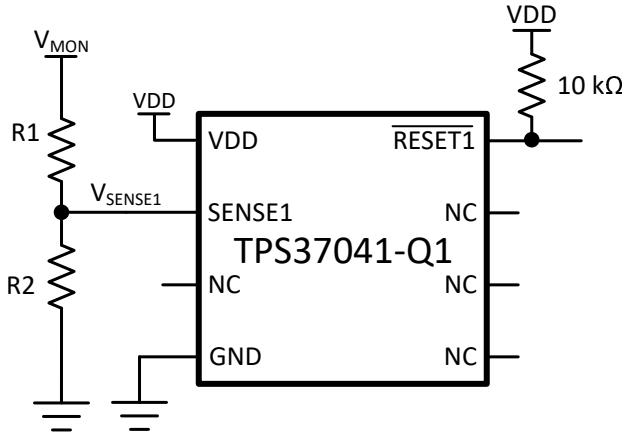


図 8-2. Adjustable Voltage Threshold With External Resistor Dividers

8.2 Typical Applications

8.2.1 Design 1: Multi-Rail Window Monitoring for Microcontroller Power Rails

図 8-3 show a typical application for the TPS37042-Q1. The TPS37042-Q1 is used to monitor two PMIC (Power Management IC) voltage rails that power the core and I/O voltage of the microcontroller that requires accurate reset delay and voltage supervision. The PMIC leverages the TPS37042-Q1 to monitor the core voltage rail of a MCU similar to the circuit below.

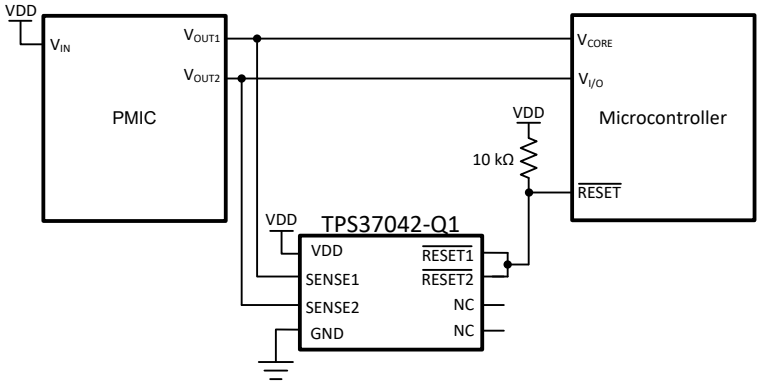


図 8-3. TPS37042-Q1 Dual-Channel Monitoring Two Microcontroller Power Rails

8.2.1.1 Design Requirements

表 8-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-$V_{I/O}$ nominal, with alerts if outside of ±8% of 3.3 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 3.533 V (7.06%) Worst case $V_{IT–(UV)}$ = 3.071 V (–6.94%)
	1.2-V_{CORE} nominal, with alerts if outside of ±5% of 1.2 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 1.2484 V (4.03%) Worst case $V_{IT–(UV)}$ = 1.1524 V (–3.97%)
Output logic voltage	5-V CMOS	5-V CMOS
Maximum system supervision current consumption	25 µA	5.5 µA (20 µA max)

8.2.1.2 Detailed Design Procedure

Determine which version of the TPS3704-Q1 best fits the monitored rail (V_{MON}) and window tolerances found on 表 9-2. The TPS3704-Q1 allows overvoltage and undervoltage monitoring for precise voltage supervision of common rails between 0.4 V and 5.5 V. This application calls for very tight monitoring of the rail with only ±5% of variation allowed on the 1.2-V_{CORE} rail. To make sure this requirement is met, the TPS37042-Q1 was chosen for its ±3% thresholds. The 3.3-$V_{I/O}$ is more flexible and can operate up to 8% variance. Because the TPS3704-Q1 comes in various tolerance options, the ±6% thresholds can be chosen for this voltage rail. To calculate the worst case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$, the accuracy must also be taken into account. The worst-case for $V_{IT+(OV)}$ and $V_{IT-(UV)}$ can be calculated shown in 式 5 and 式 6 respectively:

$$V_{IT+(OV\text{-}Worst\ Case)} = V_{MON} \times (1 + \%Threshold) \times (1 + \%Accuracy) = 1.2 \times (1.03) \times (1.01) = 1.2484\ V \quad (5)$$

$$V_{IT-(UV\text{-}Worst\ Case)} = V_{MON} \times (1 - \%Threshold) \times (1 - \%Accuracy) = 1.2 \times (0.97) \times (0.99) = 1.1524V \quad (6)$$

Hysteresis must also be taken into account when determining the OV and UV thresholds such that the release point after the fault is higher than the power-supply tolerance limits. See 図 6-1 for more details.

When the outputs switch to a high impedance state, the rise time of the $\overline{RESETx}$/RESETx pin depends on the pullup resistance and the capacitance on that node. Choose pullup resistors that satisfy both the downstream

timing requirements and the sink current required to have a V_{OL} low enough for the application; 10-kΩ to 1-MΩ resistors are a good choice for low-capacitive loads.

8.2.2 Design 2: Manual Self-Test Option for Enhanced Functional Safety Use Cases

図 8-4 displays a self-test scheme where a manual self-test function can be implemented. Any SENSEx pin can be reserved and used to trigger a fault to be observed at the output, thus pre-checking the TPS3704-Q1 for fault detection. Because the TPS3704-Q1 is functional safety compliant, it helps elevate applications like the automotive ADAS camera achieve ISO 26262 requirements and automotive safety integrity levels. This example uses a TPS37044F-Q1, configured for separate undervoltage and overvoltage (UV/OV) outputs where the SENSE4 thresholds are set at 5.5 V for OV and 2 V for UV.

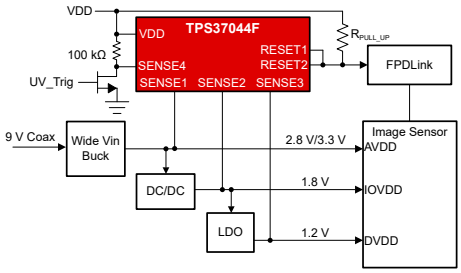


図 8-4. TPS37044F-Q1 Quad-Channel Monitoring With Manual Self-Test Option for Functional Safety

8.2.2.1 Design Requirements

表 8-2. Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored rails	3.3-V AVDD nominal, with alerts if outside of ±4% of 3.3 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 3.432 V (+4%) Worst case $V_{IT–(UV)}$ = 3.168 V (–4%)
	1.8-V IOVDD nominal, with alerts if outside of ±4% of 1.8 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 1.872 V (+4%) Worst case $V_{IT–(UV)}$ = 1.728 V (–4%)
	1.2-V DVDD nominal, with alerts if outside of ±4% of 1.2 V (including device accuracy), 10-ms reset delay	Worst case $V_{IT+(OV)}$ = 1.248 V (+4%) Worst case $V_{IT–(UV)}$ = 1.152 V (–4%)
SENSE4 (Self-test Option)	100-kΩ pullup resistor to VDD with NFET pulldown transistor to GND	UV_Trig = High - causing SENSE4 pin going low UV_Trig = Low - in normal operation
Output logic voltage	5-V CMOS	5-V CMOS
Max system IDD current	25 µA	5.5 µA (20 µA maximum)

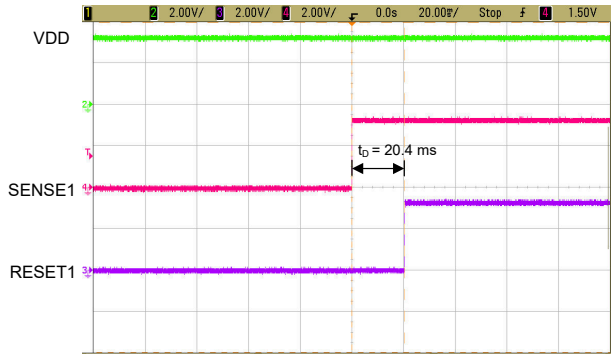
8.2.2.2 Detailed Design Procedure

図 8-4 shows a self-test scheme where a manual self-test function can be implemented. SENSE4 has an overvoltage (OV) threshold that is set at 5.5 V and the undervoltage (UV) threshold set at 2 V. SENSE4 can be connected via a 100-kΩ resistor to VDD. The self-test setup gives the added benefit of a built-in overvoltage detector for the rail powering the TPS37044F-Q1. From a functional safety perspective, a voltage supervisor cannot be considered reliable if the supervisor is operating outside its recommended operated limits.

To trigger a manual self-test, pull UV_Trig high to cause SENSE4 to be logic low, therefore triggering an undervoltage (UV) fault. The UV fault appears at $\overline{\text{RESET2}}$ as an asserted low signal. By tying both reset outputs to an NMI or interrupt input of the processor, this self-test option scheme serves as a purpose to ensure that $\overline{\text{RESET2}}$, of the TPS37044F-Q1 is operating properly. For more information on functional safety, see the Functional Safety Manual.

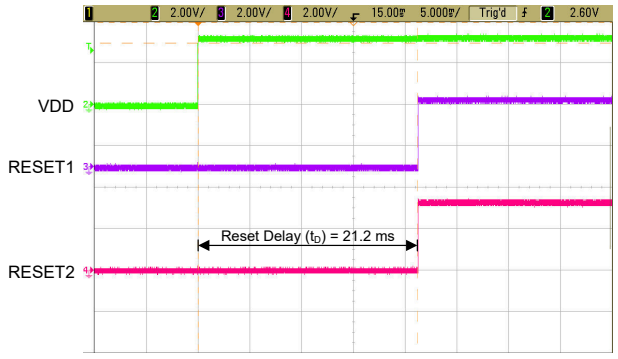
8.2.3 Application Curves

These application curves were taken with the TPS37044A7OHDDFRQ1 device on the TPS3704Q1EVM. Please see the TPS3704Q1EVM User Guide for more information.



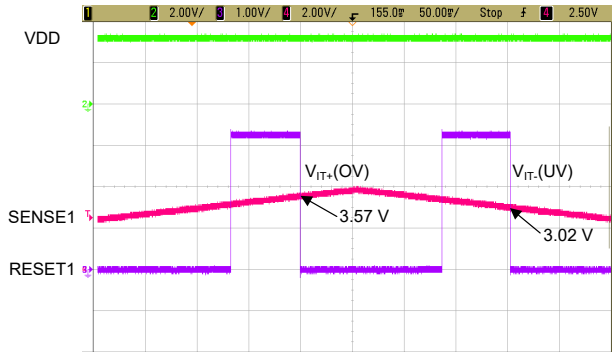
V_{SENSE1} start up 0 V to 3.3 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-5. TPS37044-Q1 SENSE1 Start-Up Function



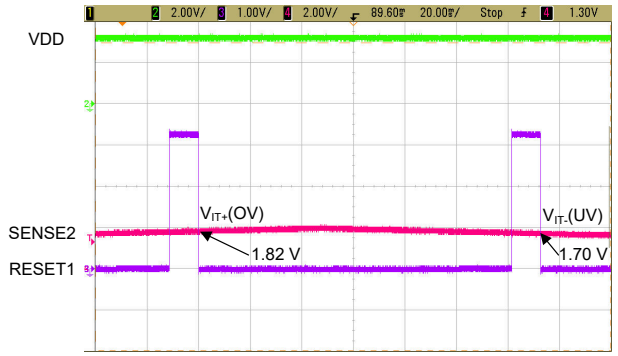
V_{DD} start up 0 V to 3.3 V, V_{SENSE1} = 3.3 V, V_{SENSE2} = 1.8 V, V_{SENSE3_4} = 1.15 V, $V_{\overline{RESET1\_2}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-6. TPS37044-Q1 VDD Start-Up Function



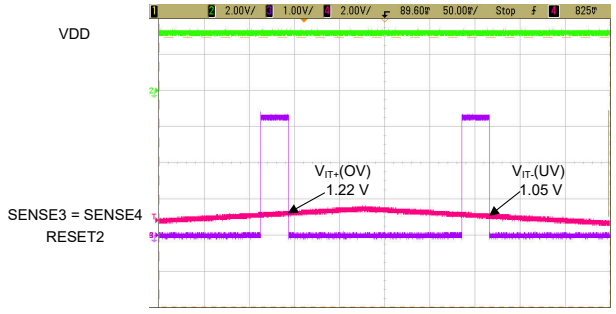
V_{SENSE1} ramp 0 V to 3.75 V, OV/UV Threshold = 3.3 V (±8%), V_{SENSE2} = 1.8 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-7. TPS37044-Q1 Overvoltage and Undervoltage Function



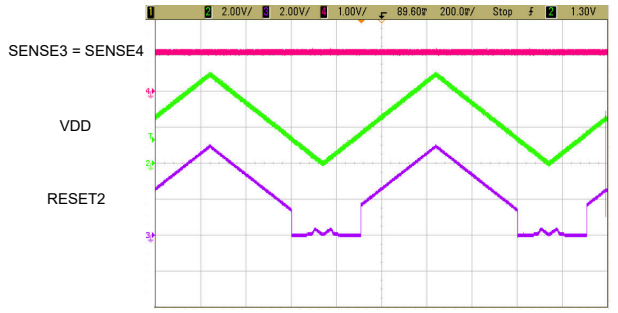
V_{SENSE2} ramp 0 V to 2 V, OV/UV Threshold = 1.8 V (+4%, -3.5%), V_{SENSE1} = 3.3 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-8. TPS37044-Q1 Overvoltage and Undervoltage Function



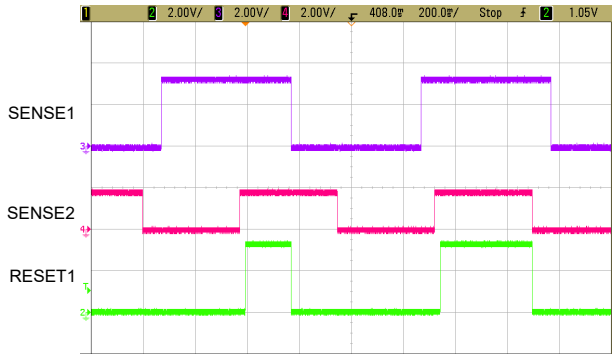
V_{SENSE3_4} ramp 0 V to 1.5 V, OV/UV Threshold = 1.15 V (+7.5%, -5.5%), V_{DD} = 3.3 V, $V_{\overline{RESET2}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-9. TPS37044-Q1 Overvoltage and Undervoltage Function



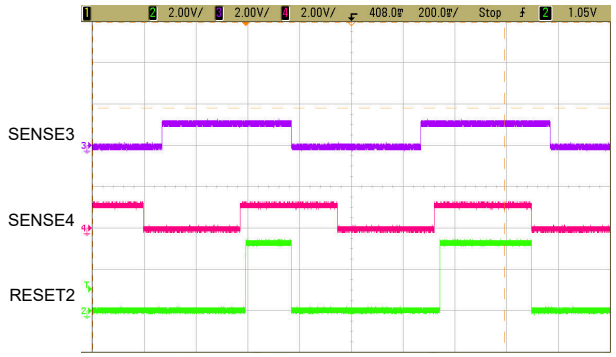
V_{DD} ramp 0 V to 5 V, V_{SENSE3_4} = 1.2 V, $V_{\overline{RESET2}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-10. TPS37044-Q1 VDD Ramp-Up Function



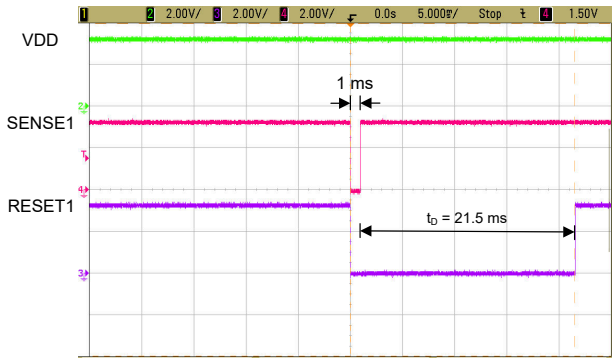
V_{SENSE1} toggling 0 V to 3.3 V [OV/UV Threshold = 3.3 V (±8%)], V_{SENSE2} toggling from 0 V to 1.8 V [OV/UV Threshold = 1.8 V (+4%, -3.5%)], V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-11. TPS37044-Q1 SENSE 1 and SENSE 2 Toggling



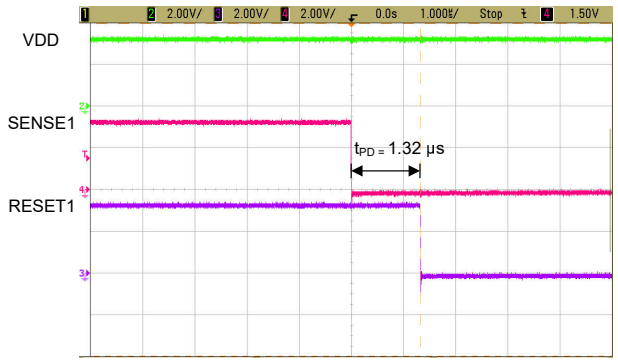
V_{SENSE3} toggling 0 V to 1.15 V [OV/UV Threshold = 1.15 V (+7.5%, -5.5%)], V_{SENSE4} toggling from 0 V to 1.15 V [OV/UV Threshold = 1.15 V (+7.5%, -5.5%)], V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-12. TPS37044-Q1 SENSE 3 and SENSE 4 Toggling



V_{SENSE1} = 3.3 V, V_{SENSE1} = 0 V via push-button for 1 ms, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ = 3.3 V, TPS37044A7OHDDFRQ1

図 8-13. TPS37044-Q1 SENSE1 Push-Button Monitoring Function With Reset Time Delay



V_{SENSE1} toggling from 3.3 V to 0 V, V_{DD} = 3.3 V, $V_{\overline{RESET1}}$ toggling from 3.3 V to 0 V, TPS37044A7OHDDFRQ1

図 8-14. TPS37044-Q1 SENSE1 Propagation Delay Function

8.3 Power Supply Recommendations

8.3.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 1.7 V to 5.5 V. This devise has a 6-V absolute maximum rating on the VDD pin. Good analog practice is to place a 0.1-µF to 1-µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage supply providing power to VDD is susceptible to any large voltage transients that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

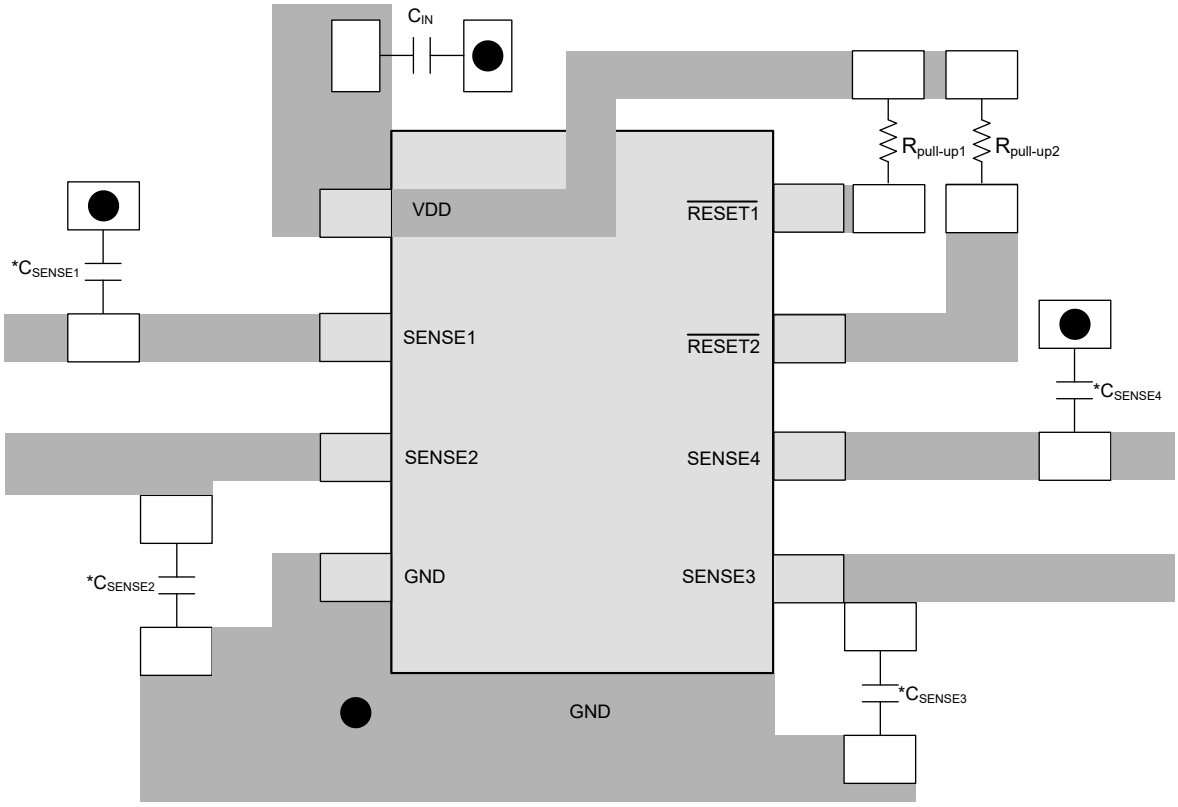
8.4 Layout

8.4.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.

- Avoid using long voltage traces to the sense pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- If SENSEx capacitors (C_{SENSEx}) are used, place capacitors as close as possible to the SENSEx pins to further improve noise immunity on the SENSEx pins. Placing a 10-nF to 100-nF capacitors between the SENSEx pins and GND can reduce the sensitivity to transient voltages on the monitored signal.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

8.4.2 Layout Example



● Vias used to connect pins for application-specific connections

*C_{SENSEx} capacitors can be added for improve noise immunity

図 8-15. Recommended Layout

9 Device and Documentation Support

9.1 Device Nomenclature

図 4-1 in セクション 4 and 表 9-1 describe how to decode the function of the device based on its part number listed in 表 9-2.

表 9-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Generic part number	TPS3704x-Q1	TPS3704x-Q1
Channel options	1	One-channel option
	2	Dual-channel option
	3	Triple-channel option
	4	Quad-channel option
Detection options	Ax, Bx, Cx,...	See 表 9-2
Variant code (output topology)	O	Open-drain, active-low
	L	Push-pull, active-low
	H	Push-pull, active-high
Reset time delay option	A	20-µs reset time delay
	B	1-ms reset time delay
	C	2-ms reset time delay
	D	3-ms reset time delay
	E	5-ms reset time delay
	F	10-ms reset time delay
	G	15-ms reset time delay
	H	20-ms reset time delay
	I	25-ms reset time delay
	J	35-ms reset time delay
	K	40-ms reset time delay
	L	50-ms reset time delay
	M	70-ms reset time delay
	N	100-ms reset time delay
	O	140-ms reset time delay
	P	150-ms reset time delay
	R	200-ms reset time delay
	S	280-ms reset time delay
	T	400-ms reset time delay
	U	560-ms reset time delay
	V	800-ms reset time delay
	W	1120-ms reset time delay
	X	1200-ms reset time delay
Package	DDF	SOT-23 8-pin (1.6 mm × 2.9 mm)
Reel	R	Large reel
Automotive version	Q1	Q100 AEC

表 9-2. Device Threshold Table

ORDERABLE PART NAME	VARIANT(4)	NUM OF CHAN.	RESET TIME	SENSE1(2) (3)	SENSE2(2) (3)	SENSE3(2) (3)	SENSE4(2) (3)
TPS37042BJOFDDFRQ1	ADJ	2	10ms	0.8V (±4%)	0.8V (±4%)	-	-
TPS37042A3OFDDFRQ1	Fixed	2	10ms	3.3V (±5%)	1.2V (±5%)	-	-
TPS37042ZJOFDDFRQ1(1)	Fixed	2	10ms	1.95V (±4%)	3.8V (±6%)	-	-
TPS37043DJOFDDFR(1)	ADJ/Fixed	3	10 ms	3.3V (-11%)	1.2V (-11%)	0.8V (-8%)	-
TPS37043A4OFDDFRQ1	Fixed	3	10ms	2.8V (±5%)	1.8V (±5%)	1.2V (±5%)	-
TPS37043A8OFDDFRQ1	Fixed	3	10ms	3.3V (±5%)	1.8V (±5%)	1.0V (±5%)	-
TPS37043CPOFDDFRQ1(1)	ADJ/Fixed	3	10ms	3.3V (±4%)	0.75V (±4%)	0.8V (±3%)	-
TPS37043ZJOFDDFRQ1(1)	Fixed	3	10ms	0.95V (±4%)	1.35V (±4%)	1.8V (±4%)	-
TPS37043LJOFDDFRQ1(1)	ADJ	3	10ms	0.4V (±5%)	0.4V (±5%)	0.8V (±5%)	-
TPS37043CJOFDDFRQ1(1)	ADJ	3	10ms	0.8V (±6%)	0.8V (±6%)	0.8V (±6%)	-
TPS37043MJOFDDFRQ1(1)	ADJ	3	10ms	0.4V (±7%)	0.4V (±7%)	0.8V (±7%)	-
TPS37043A5OFDDFRQ1 (1)	Fixed	3	10ms	3.3V (±4%)	1.8V (±4%)	1.2V (±4%)	-
TPS37043BJOFDDFRQ1	ADJ	3	10ms	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)	-
TPS37044BJOFDDFR	ADJ	4	10 ms	0.8 V (±4%)	0.8 V (±4%)	0.8 V (±4%)	0.8 V (±4%)
TPS37044LJOJDDFR(1)	ADJ	4	35ms	0.4V (±5%)	0.4V (±5%)	0.8V (±5%)	0.8V (±5%)
TPS37044BJOFDDFRQ1	ADJ	4	10ms	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)	0.8V (±4%)
TPS37044CJOFDDFRQ1(1)	ADJ	4	10ms	0.8V (±6%)	0.8V (±6%)	0.8V (±6%)	0.8V (±6%)
TPS37044MJOFDDFRQ1(1)	ADJ	4	10ms	0.4V (±7%)	0.4V (±7%)	0.8V (±7%)	0.8V (±7%)
TPS37044A4OGDDFRQ1	Fixed	4	15ms	3.3V (±8%)	1.8V (±4%)	1.15V (±6%)	1.15V (±6%)

(1) Preview, contact TI sales representatives or on TI's E2E forum for details and availability of other options
(2) Listed percentage denotes window tolerance, see 図 6-1 for more information
(3) VIT threshold of 0.8V and 0.4V signifies an adjustable channel
(4) ADJ denotes an adjustable voltage threshold set by an external resistor divider, see Adjustable Voltage Thresholds for more information

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (May 2022) to Revision B (August 2023)	Page
• 冗長な言い回しを簡潔にし、デバイスのスレッショルド表と計算ツールをハイライト表示	1
• ウィンドウ許容誤差の仕様に内容を明確にする文章を追加	1
• Addition of 表 4-1	3
• Clarifying text added to window tolerance specification in 図 6-1	11
• Addition of reference to adjustable threshold resistor calculator	24
• Orderable part name additions to 表 9-2	30

Changes from Revision * (March 2021) to Revision A (May 2022)	Page
• 量産データのリリース	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS37041BPLEDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1BPQE	Samples
TPS37042A3OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2A3FQ	Samples
TPS37042ZJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2ZJFQ	Samples
TPS37043A4OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3A4FQ	Samples
TPS37043A5OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3A5FQ	Samples
TPS37043A8OFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3A8FQ	Samples
TPS37043BJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3BJFQ	Samples
TPS37043CJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3CJFQ	Samples
TPS37043CPOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3CPFQ	Samples
TPS37043LJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3LJFQ	Samples
TPS37043MJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3MJFQ	Samples
TPS37043ZJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3ZJFQ	Samples
TPS37044A4OGDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4A4GQ	Samples
TPS37044BJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4BJFQ	Samples
TPS37044CJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4CJFQ	Samples
TPS37044MJOFDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4MJFQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3704-Q1 :

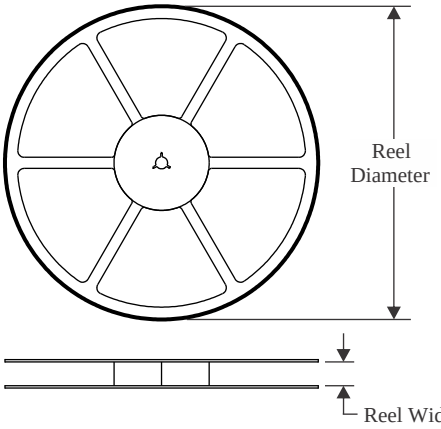
- Catalog : TPS3704

NOTE: Qualified Version Definitions:

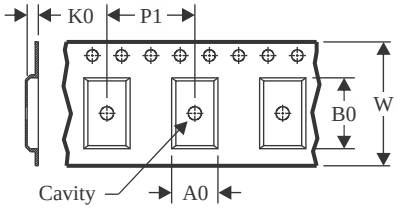
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

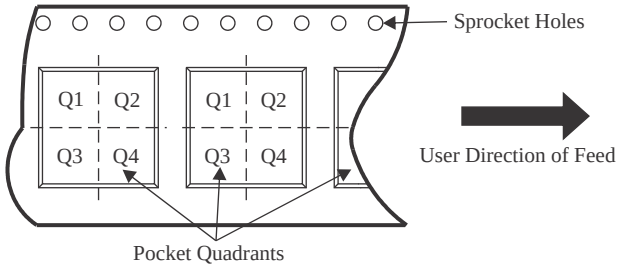


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

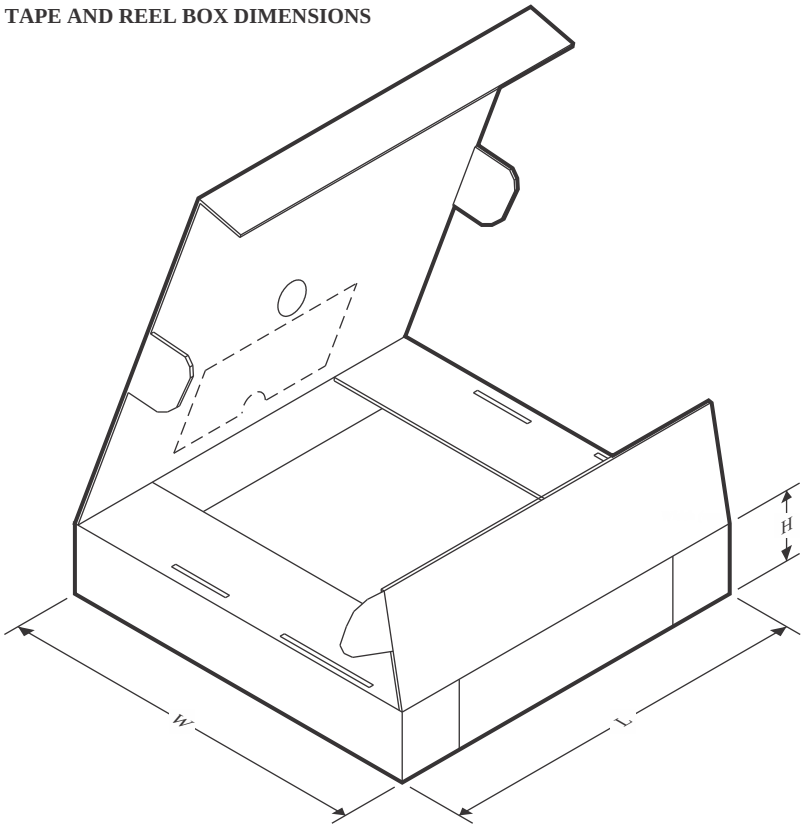


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS37041BPLEDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37042A3OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37042ZJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043A4OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043A5OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043A8OFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043CJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043CPOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS37043LJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043MJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37043ZJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37044A4OGDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37044BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37044CJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS37044MJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

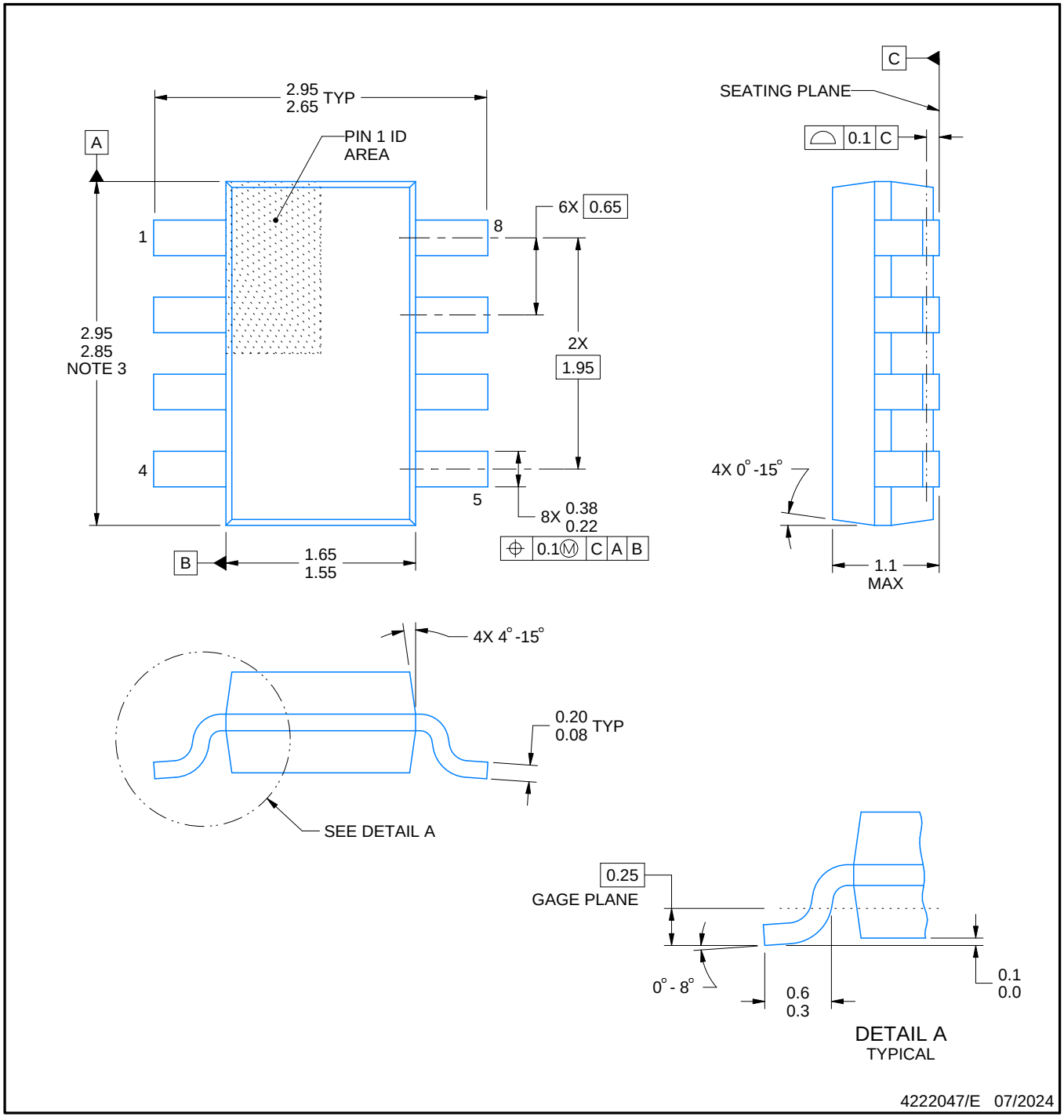
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS37041BPLEDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37042A3OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37042ZJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043A4OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043A5OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043A8OFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043CJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043CPOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043LJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043MJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37043ZJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37044A4OGDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37044BJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37044CJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS37044MJOFDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

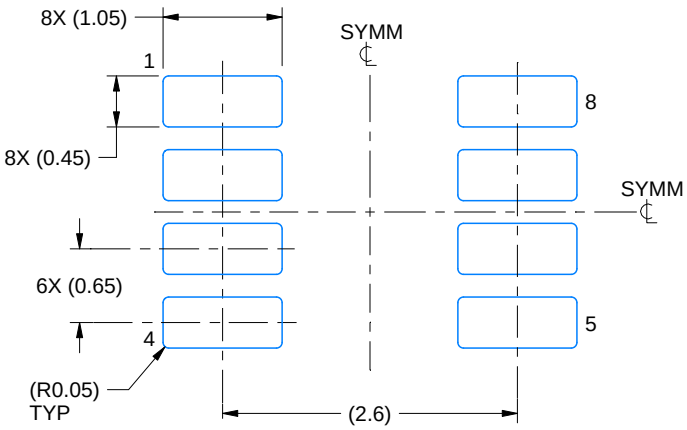
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

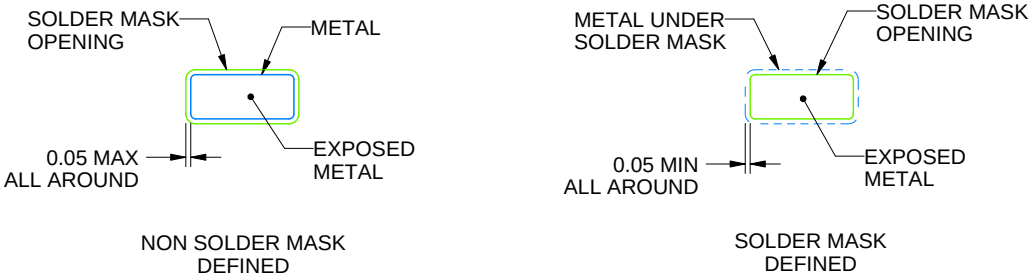


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

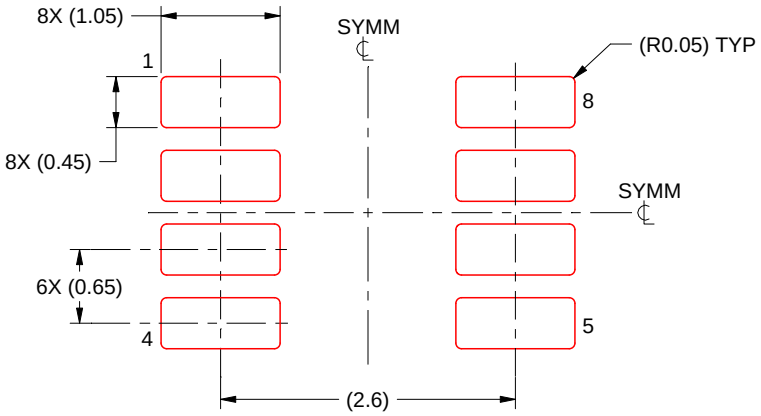
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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