

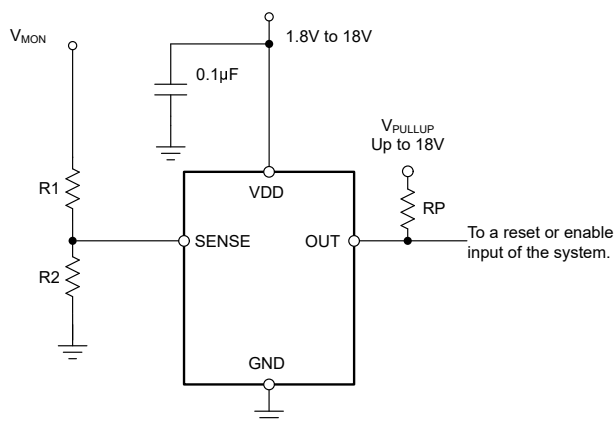
## TPS3710 広い入力電圧範囲の電圧検出器

### 1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1: 動作時周囲温度範囲  $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C6
- 広い電源電圧範囲:  $1.8\text{V} \sim 18\text{V}$
- スレッシュホールドを変更可能: 最小  $400\text{mV}$
- 高いスレッシュホールド精度:
  - $1.0\%$  過熱
  - $0.25\%$  の代表値
- 低い静止電流:  $5.5\mu\text{A}$  (標準値)
- オープンドレイン出力
- 内部ヒステリシス:  $5.5\text{mV}$  (標準値)
- 温度範囲:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
- パッケージ:
  - SOT-6
  - $1.5\text{mm} \times 1.5\text{mm}$  WSON-6

### 2 アプリケーション

- 産業用制御システム
- 組み込みコンピューティング モジュール
- DSP、マイクロコントローラ、マイクロプロセッサのアプリケーション
- ノート PC およびデスクトップ PC
- 携帯用およびバッテリー駆動の製品
- FPGA および ASIC アプリケーション



概略回路図

### 3 概要

TPS3710 は電源電圧範囲の広い電圧検出器で、 $1.8\text{V} \sim 18\text{V}$  の範囲で動作します。 $400\text{mV}$  の基準電圧と定格  $18\text{V}$  のオープンドレイン出力を内蔵する高精度のコンパレータにより、高精度の電圧検出を実現します。監視対象の電圧は、外付け抵抗を使用して設定することができます。

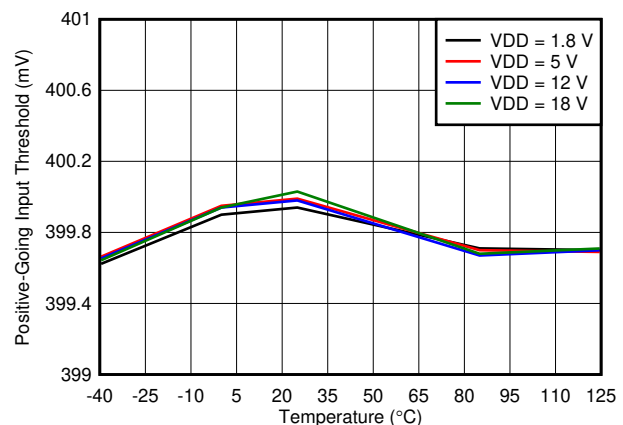
OUT ピンは、SENSE ピンの電圧が ( $V_{IT-}$ ) より低くなると LOW に駆動され、対応するスレッシュホールド ( $V_{IT+}$ ) より高い電圧に戻ると HIGH に復帰します。TPS3710 のコンパレータは、短時間のグリッチを除去するためヒステリシスが組み込まれているので、誤ったトリガが発生せずにデバイスは動作できます。

TPS3710 は 6 ピン SOT パッケージおよび  $1.5\text{mm} \times 1.5\text{mm}$  の 6 ピン WSON パッケージで供給され、 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$  の接合部温度範囲で動作が規定されています。

#### 製品情報

部品番号	パッケージ (1)	本体サイズ (公称) (2)
TPS3710	SOT (6)	$2.90\text{mm} \times 1.60\text{mm}$
	WSON (6)	$1.50\text{mm} \times 1.50\text{mm}$

- (1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。
- (2) パッケージ サイズ (長さ  $\times$  幅) は公称値であり、該当する場合はピンも含まれます。



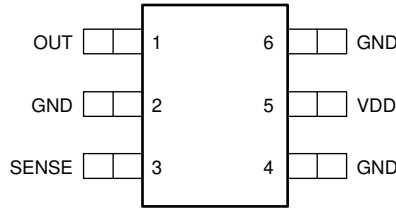
立ち上がり入カスレッシュホールド電圧 ( $V_{IT+}$ ) と温度との関係



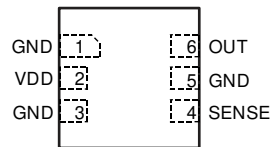
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## 4 Pin Configuration and Functions



**図 4-1. DDC Package  
6-Pin SOT  
Top View**



**図 4-2. DSE Package  
6-Pin WSON  
Top View**

**表 4-1. Pin Functions**

NAME	PIN		I/O	DESCRIPTION
	DDC	DSE		
GND	2, 4, 6	1, 3, 5	—	Connect all three pins to ground.
OUT	1	6	O	SENSE comparator open-drain output. OUT is driven low when the voltage at this comparator is below ( $V_{IT-}$ ). The output goes high when the sense voltage returns above the respective threshold ( $V_{IT+}$ ).
SENSE	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage ( $V_{IT-}$ ), OUT is driven low.
VDD	5	2	I	Supply voltage input. Connect a 1.8V to 18V supply to VDD to power the device. Good analog design practice is to place a 0.1 $\mu$ F ceramic capacitor close to this pin.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	VDD	-0.3	20	V
	OUT	-0.3	20	
	SENSE	-0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T <sub>J</sub>	-40	125	°C
	Storage, T <sub>stg</sub>	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground pin.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2500	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000		

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.8		18	V
V <sub>I</sub>	Input voltage	SENSE	0	6.5	V
V <sub>O</sub>	Output voltage	OUT	0	18	V

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3710		UNIT
		DDC (SOT)	DSE (WSON)	
		6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.5	128.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.3	153.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	11.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.8	157.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $1.8\text{V} < V_{DD} < 18\text{V}$  (unless otherwise noted). Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{DD} = 5\text{V}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$ Power-on reset voltage <sup>(1)</sup>	$V_{OLmax} = 0.2\text{V}$ , output sink current = $15\mu\text{A}$			0.8	V
$V_{IT+}$ Positive-going input threshold voltage	$V_{DD} = 1.8\text{V}$	396	400	404	mV
	$V_{DD} = 18\text{V}$	396	400	404	
$V_{IT-}$ Negative-going input threshold voltage	$V_{DD} = 1.8\text{V}$	387	394.5	400	mV
	$V_{DD} = 18\text{V}$	387	394.5	400	
$V_{hys}$ Hysteresis voltage (hys = $V_{IT+} - V_{IT-}$ )			5.5	12	mV
$I_{(SENSE)}$ Input current (at the SENSE pin)	$V_{DD} = 1.8\text{V}$ and $18\text{V}$ , $V_I = 6.5\text{V}$	-25	1	25	nA
$V_{OL}$ Low-level output voltage	$V_{DD} = 1.3\text{V}$ , output sink current = $0.4\text{mA}$			250	mV
	$V_{DD} = 1.8\text{V}$ , output sink current = $3\text{mA}$			250	
	$V_{DD} = 5\text{V}$ , output sink current = $5\text{mA}$			250	
$I_{lk(OD)}$ Open-drain output leakage-current	$V_{DD} = 1.8\text{V}$ and $18\text{V}$ , $V_O = V_{DD}$			300	nA
	$V_{DD} = 1.8\text{V}$ , $V_O = 18\text{V}$			300	
$I_{DD}$ Supply current	$V_{DD} = 1.8\text{V}$ , no load		5.5	11	$\mu\text{A}$
	$V_{DD} = 5\text{V}$		6	13	
	$V_{DD} = 12\text{V}$		6	13	
	$V_{DD} = 18\text{V}$		7	13	
UVLO Undervoltage lockout <sup>(2)</sup>	$V_{DD}$ falling	1.3		1.7	V

(1) The lowest supply voltage ( $V_{DD}$ ) at which output is active;  $t_{r(VDD)} > 15\mu\text{s/V}$ . Below  $V_{(POR)}$ , the output cannot be determined.

(2) When  $V_{DD}$  falls below UVLO, OUT is driven low. The output cannot be determined below  $V_{(POR)}$ .

## 5.6 Timing Requirements

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay <sup>(1)</sup>	$V_{DD} = 5V$ , 10mV input overdrive, $R_P = 10k\Omega$ , $V_{OH} = 0.9 \times V_{DD}$ , $V_{OL} = 400mV$ , see <a href="#">Figure 5-1</a>		18	$\mu s$
$t_{pd(LH)}$	Low-to-high propagation delay <sup>(1)</sup>	$V_{DD} = 5V$ , 10mV input overdrive, $R_P = 10k\Omega$ , $V_{OH} = 0.9 \times V_{DD}$ , $V_{OL} = 400mV$ , see <a href="#">Figure 5-1</a>		29	$\mu s$
$t_{d(start)}$	Start-up delay <sup>(2)</sup>			150	$\mu s$

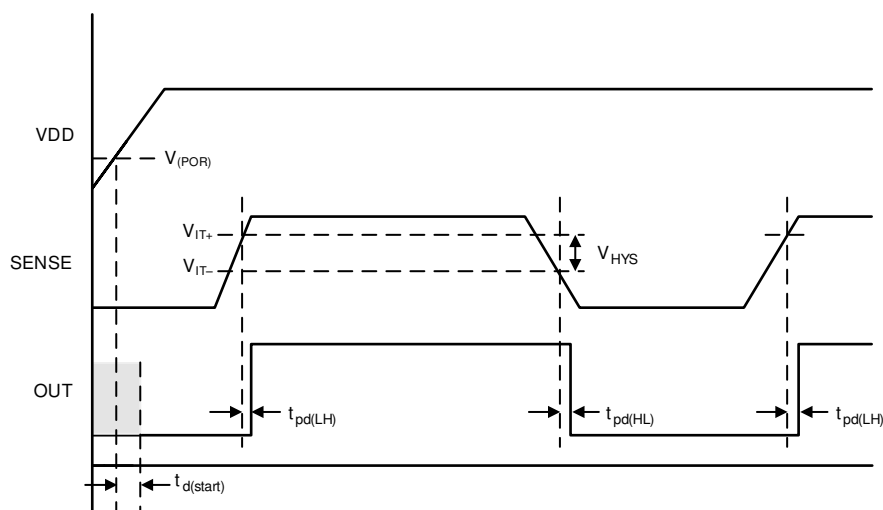
(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).

(2) During power on,  $V_{DD}$  must exceed 1.8V for at least 150 $\mu s$  before the output is in a correct state.

## 5.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

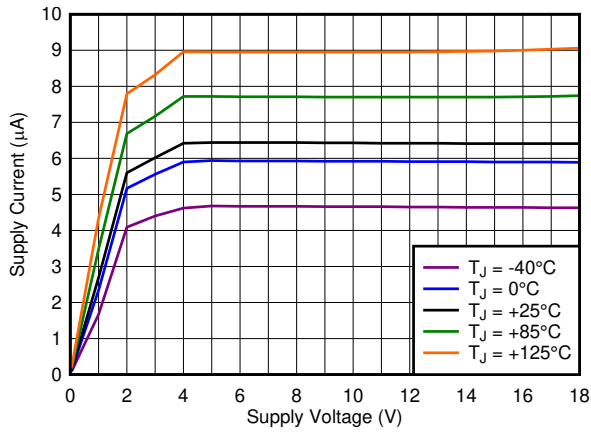
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output rise time	$V_{DD} = 5V$ , 10mV input overdrive, $R_P = 10k\Omega$ , $V_O = (0.1 \text{ to } 0.9) \times V_{DD}$			$\mu s$
$t_f$	Output fall time	$V_{DD} = 5V$ , 10mV input overdrive, $R_P = 10k\Omega$ , $V_O = (0.1 \text{ to } 0.9) \times V_{DD}$			$\mu s$



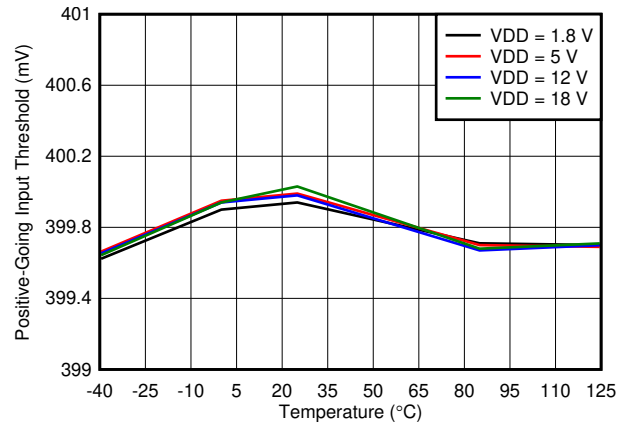
**Figure 5-1. Timing Diagram**

## 5.8 Typical Characteristics

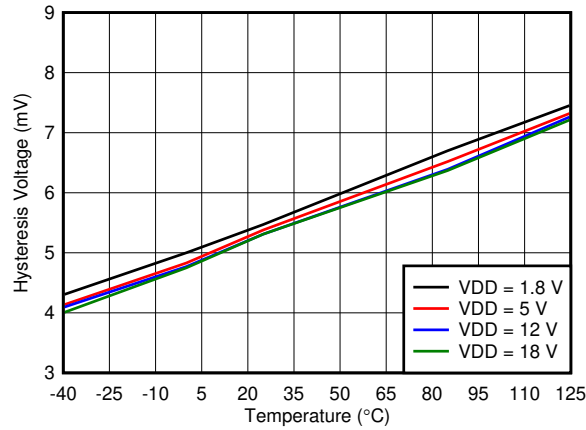
at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{V}$  (unless otherwise noted)



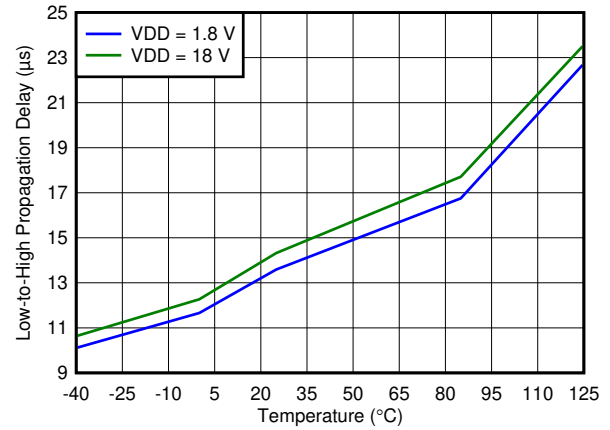
5-2. Supply Current ( $I_{DD}$ ) vs Supply Voltage ( $V_{DD}$ )



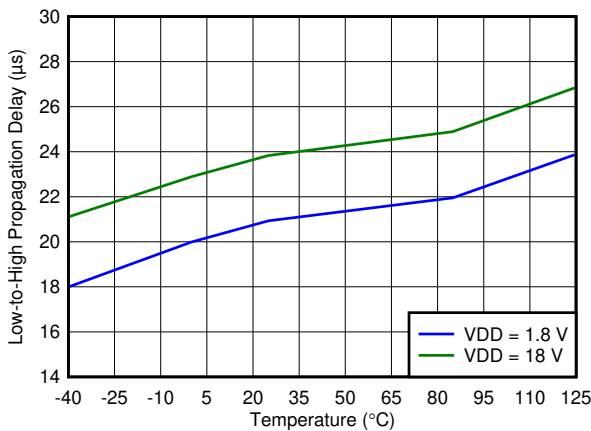
5-3. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature



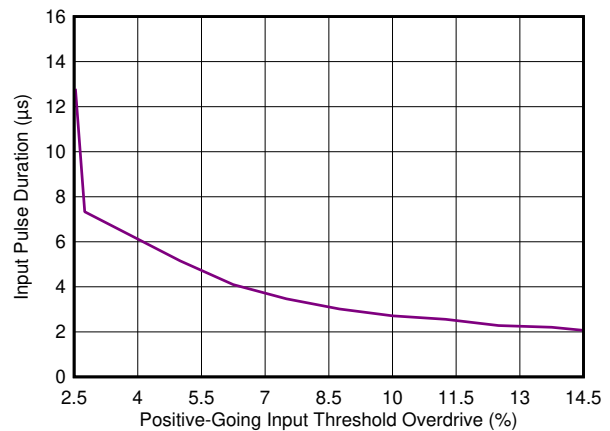
5-4. Hysteresis ( $V_{hys}$ ) vs Temperature



5-5. Propagation Delay vs Temperature (High-to-Low Transition at Sense)



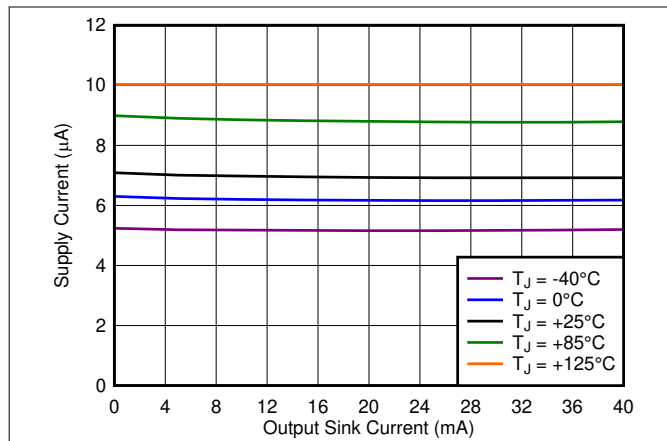
5-6. Propagation Delay vs Temperature (Low-to-High Transition at Sense)



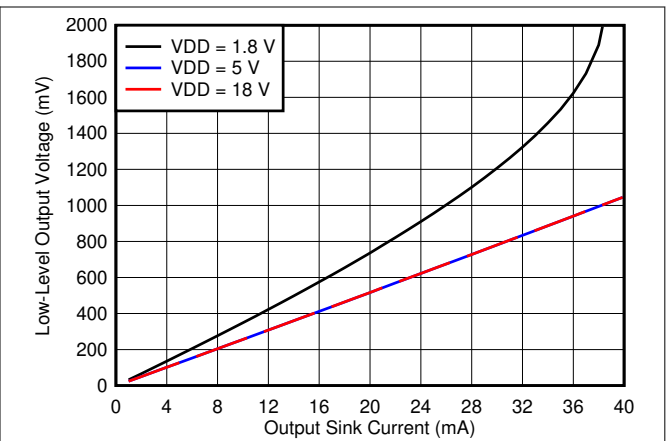
5-7. Minimum Pulse Width vs Threshold Overdrive Voltage

### 5.8 Typical Characteristics (continued)

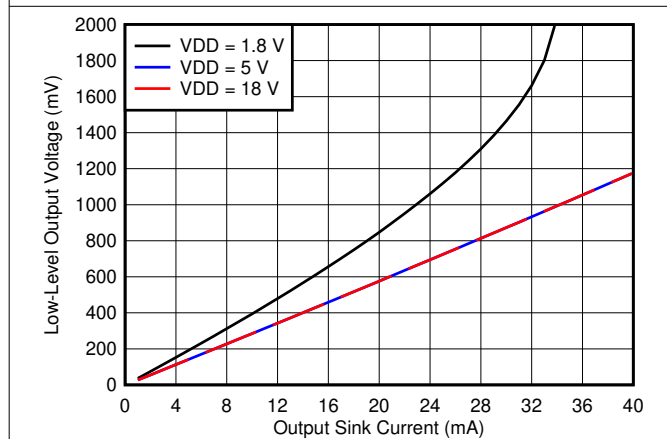
at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{V}$  (unless otherwise noted)



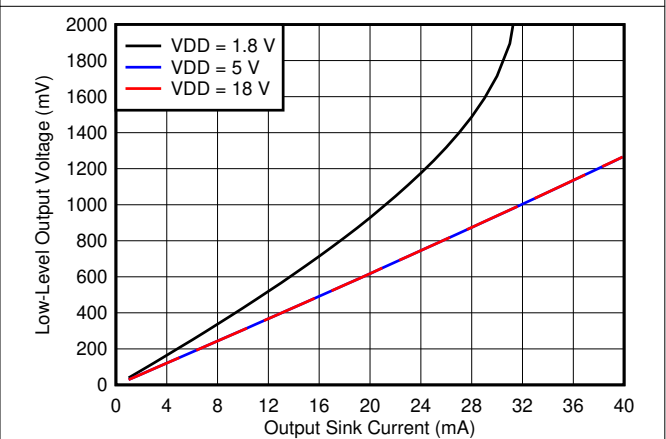
5-8. Supply Current ( $I_{DD}$ ) vs Output Sink Current



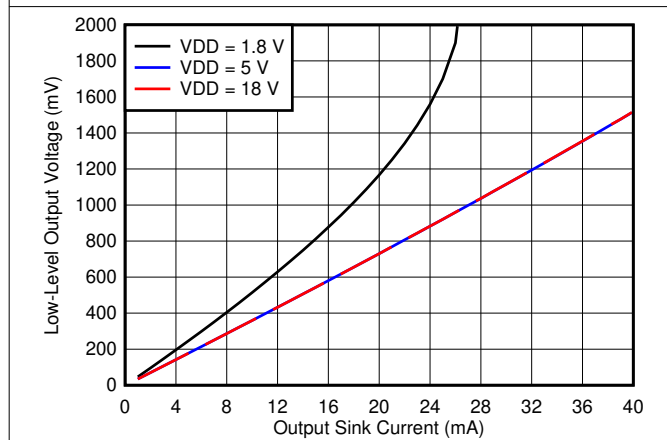
5-9. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $-40^\circ\text{C}$ )



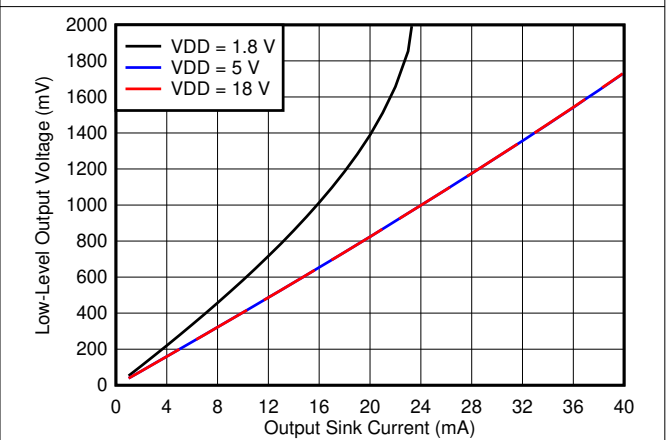
5-10. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $0^\circ\text{C}$ )



5-11. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $25^\circ\text{C}$ )



5-12. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $85^\circ\text{C}$ )



5-13. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $125^\circ\text{C}$ )



## 6 Detailed Description

### 6.1 Overview

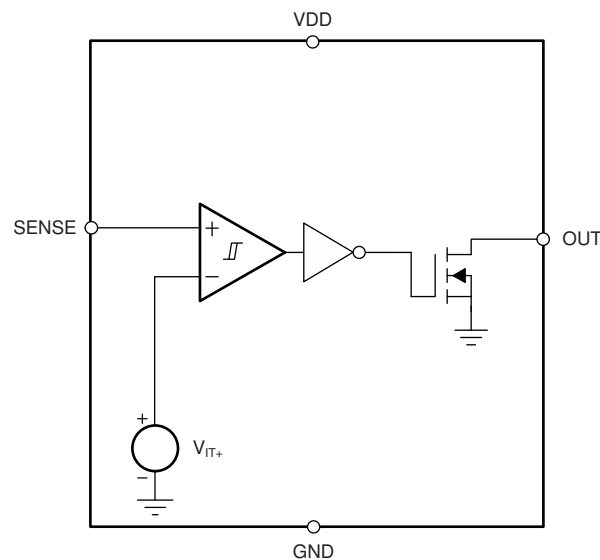
The TPS3710 provides precision voltage detection. The TPS3710 is a wide-supply voltage range (1.8V to 18V) device with a high-accuracy rising input threshold of 400mV (1% over temperature) and built-in hysteresis. The output is also rated to 18V, and can sink up to 40mA.

The TPS3710 asserts the output signal, as shown in 表 6-1. To monitor any voltage above 0.4V, set the input using an external resistor divider network. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

表 6-1. TPS3710 Truth Table

CONDITION	OUTPUT	STATUS
$SENSE > V_{IT+}$	OUT high	Output not asserted
$SENSE < V_{IT-}$	OUT low	Output asserted

### 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Input (SENSE)

The TPS3710 comparator has two inputs: one external input, and one input connected to the internal reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1nF to 10nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below ( $V_{IT-}$ ). When the voltage exceeds  $V_{IT+}$ , the output (OUT) goes to a high-impedance state; see [Figure 5-1](#).

### 6.3.2 Output (OUT)

In a typical TPS3710 application, the output is connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the output is connected to the enable input of a voltage regulator (such as a dc-dc converter or low-dropout regulator [LDO]).

The TPS3710 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TPS3710 output can be pulled up to 18V, independent of the device supply voltage.

[Table 6-1](#) and the [Section 6.3.1](#) describe how the output is asserted or deasserted. See [Figure 5-1](#) for a timing diagram that describes the relationship between threshold voltage and the respective output.

### 6.3.3 Immunity to Input-Pin Voltage Transients

The TPS3710 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see [Figure 5-7](#), *Minimum Pulse Width vs Threshold Overdrive Voltage*.

## 6.4 Device Functional Modes

### 6.4.1 Normal Operation ( $V_{DD} > UVLO$ )

When the voltage on  $V_{DD}$  is greater than 1.8V for at least 150 $\mu$ s, the OUT signal correspond to the voltage on SENSE as listed in [Table 6-1](#).

### 6.4.2 Undervoltage Lockout ( $V_{(POR)} < V_{DD} < UVLO$ )

When the voltage on  $V_{DD}$  is less than the device UVLO voltage, and greater than the power-on reset voltage,  $V_{(POR)}$ , the OUT signal is asserted regardless of the voltage on SENSE.

### 6.4.3 Power-On Reset ( $V_{DD} < V_{(POR)}$ )

When the voltage on  $V_{DD}$  is lower than the required voltage to internally pull the asserted output to GND ( $V_{(POR)}$ ), SENSE is in a high-impedance state and the OUT signal is undefined.

## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Application Information

The TPS3710 device is a wide-supply voltage comparator that operates over a  $V_{DD}$  range of 1.8V to 18V. The device has a high-accuracy comparator with an internal 400mV reference and an open-drain output rated to 18V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

#### 7.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$

The output is often tied to  $V_{DD}$  through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than  $V_{DD}$  to correctly interface with the reset and enable pins of other devices.

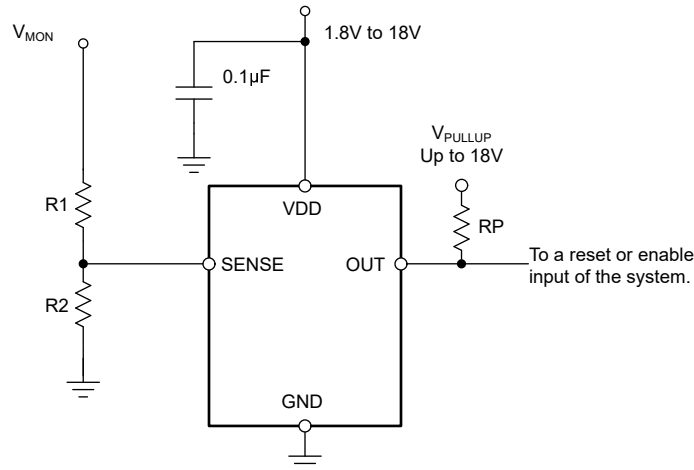
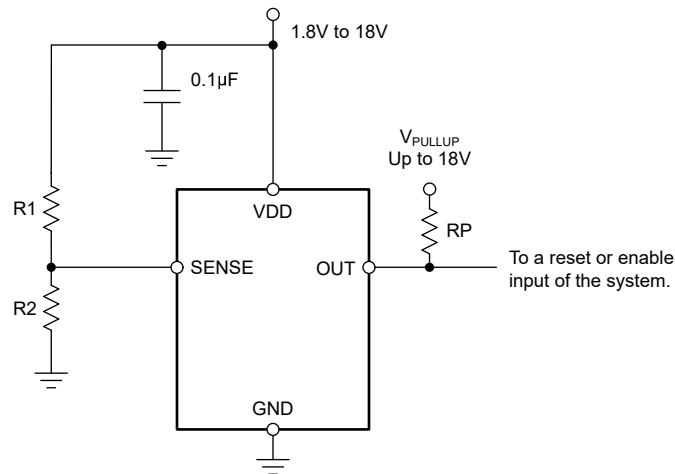


図 7-1. Interfacing to a Voltage Other Than  $V_{DD}$

### 7.1.2 Monitoring V<sub>DD</sub>

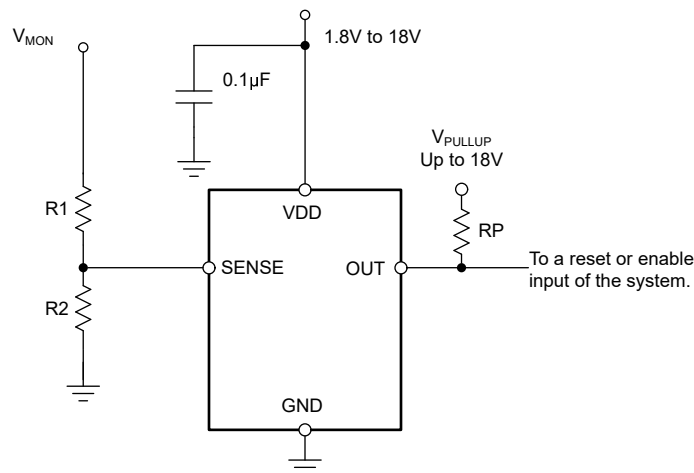
Many applications monitor the same rail that is powering V<sub>DD</sub>. In these applications the resistor divider is simply connected to the V<sub>DD</sub> rail.



**図 7-2. Monitoring the Same Voltage as V<sub>DD</sub>**

### 7.1.3 Monitoring a Voltage Other Than V<sub>DD</sub>

Some applications monitor rails other than the one that is powering V<sub>DD</sub>. In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.



NOTE: The input can monitor a voltage greater than maximum V<sub>DD</sub> with the use of an external resistor divider network.

**図 7-3. Monitoring a Voltage Other Than V<sub>DD</sub>**

## 7.2 Typical Application

The TPS3710 device is a wide-supply voltage comparator that operates over a  $V_{DD}$  range of 1.8 to 18V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

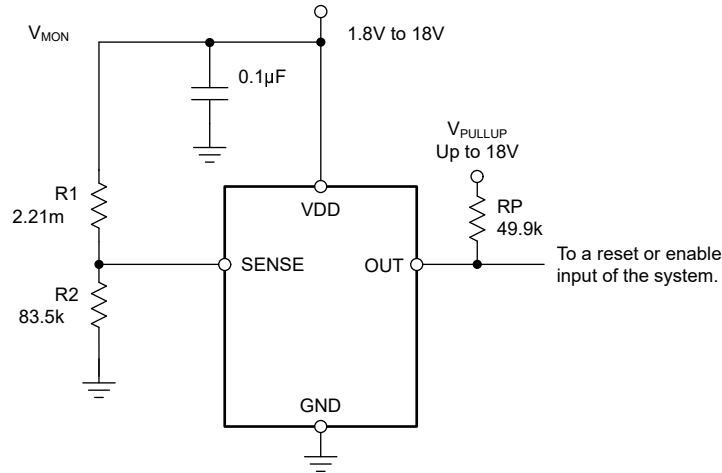


図 7-4. Wide VIN Voltage Monitor

### 7.2.1 Design Requirements

For this design example, use the values summarized in 表 7-1 as the input parameters.

表 7-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12V nominal rail with maximum falling threshold of 10%	$V_{MON(UV)} = 10.99V$ (8.33%)

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using 式 1 to determine  $V_{MON(UV)}$ .

$$V_{MON(UV)} = \left( 1 + \frac{R1}{R2} \right) \times V_{IT-} \quad (1)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$  is the target voltage at which an undervoltage condition is detected

Choose  $R_{TOTAL}$  ( $= R1 + R2$ ) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report [SLVA450, Optimizing Resistor Dividers at a Comparator Input](#), available for download from [www.ti.com](http://www.ti.com).

### 7.2.2.2 Pullup Resistor Selection

To make ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ( $I_{\text{kg(OD)}}$ ) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the [セクション 5.5](#).

Use [式 2](#) to calculate the value of the pullup resistor.

$$\frac{(V_{\text{HI}} - V_{\text{PU}})}{I_{\text{kg(OD)}}} \geq R_{\text{PU}} \geq \frac{V_{\text{PU}}}{I_{\text{O}}} \quad (2)$$

### 7.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1 $\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher value capacitor can be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

### 7.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1nF to 10nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

## 7.2.3 Application Curve

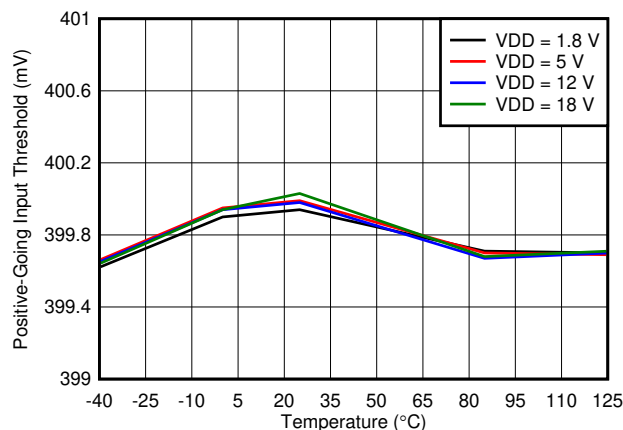


図 7-5. Rising Input Threshold Voltage ( $V_{\text{IT+}}$ ) vs Temperature

## 7.3 Do's and Don'ts

Do connect a 0.1 $\mu\text{F}$  decoupling capacitor from  $V_{\text{DD}}$  to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage ( $V_{\text{OL}}$ ).

## 7.4 Power-Supply Recommendations

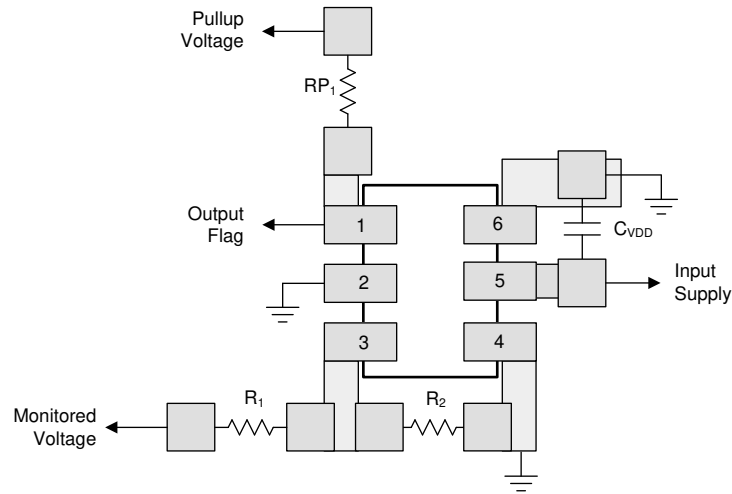
This device operates from an input voltage supply range between 1.8V and 18V.

## 7.5 Layout

### 7.5.1 Layout Guidelines

Placing a 0.1 $\mu$ F capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

### 7.5.2 Layout Example



**☒ 7-6. Layout Example**

## 8 Device and Documentation Support

### 8.1 Device Support

#### 8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT	DESCRIPTION
TPS3710yyyyz	yyy is package designator z is package quantity

### 8.2 Documentation Support

#### 8.2.1 Related Documentation

For related documentation, see the following:

[Optimizing Resistor Dividers at a Comparator Input](#)

### 8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 8.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision \* (October 2015) to Revision A (February 2024)

Page

- |  |   |
|--|---|
| ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....                       | 1 |
| ドキュメント全体で VDD ピンのコンデンサ値を 0.01uF から 0.1uF に変更して画像を更新..... | 1 |



## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3710DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11AO	<a href="#">Samples</a>
TPS3710DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11AO	<a href="#">Samples</a>
TPS3710DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1A	<a href="#">Samples</a>
TPS3710DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS3710 :**

- Automotive : [TPS3710-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3710DDCR	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3710DDCT	SOT-23-THIN	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3710DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS3710DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3710DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3710DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0
TPS3710DSEER	WSON	DSE	6	3000	200.0	183.0	25.0
TPS3710DSET	WSON	DSE	6	250	200.0	183.0	25.0

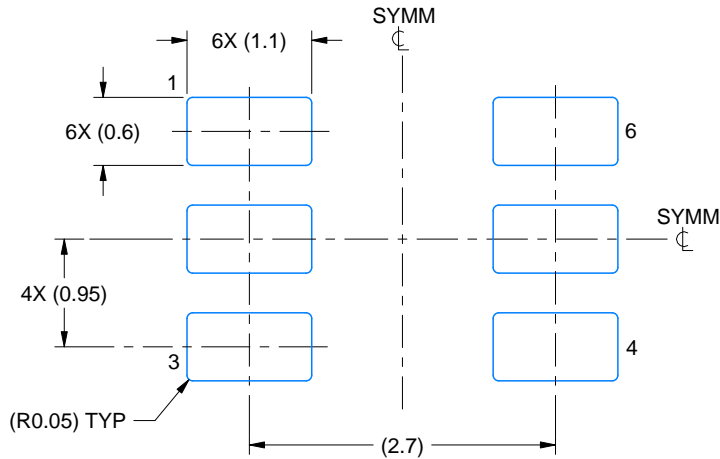


# EXAMPLE BOARD LAYOUT

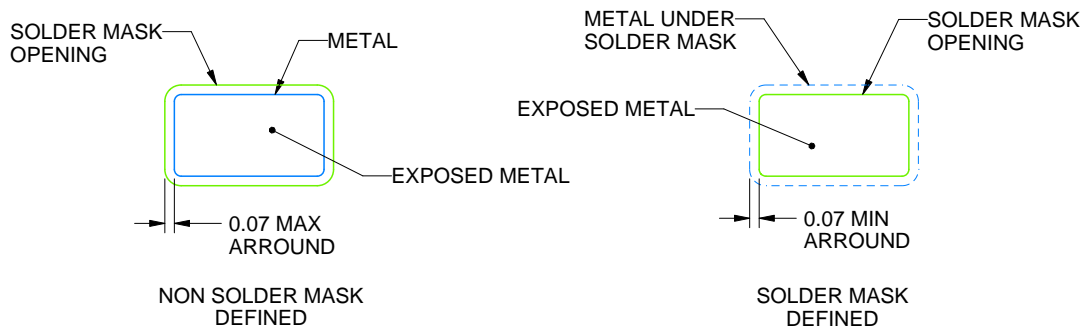
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDEMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

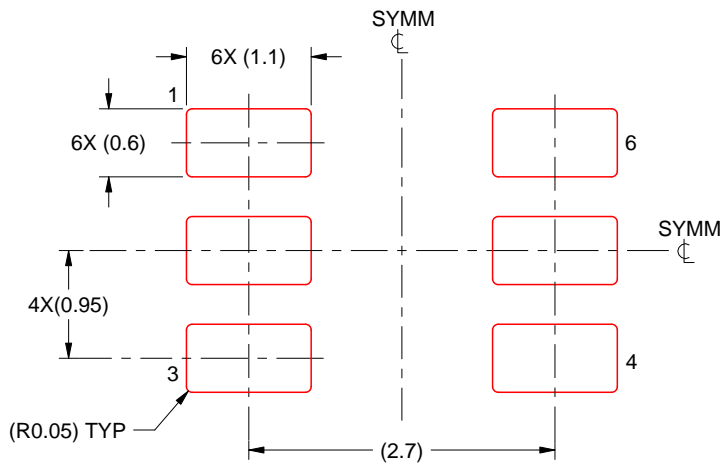


# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

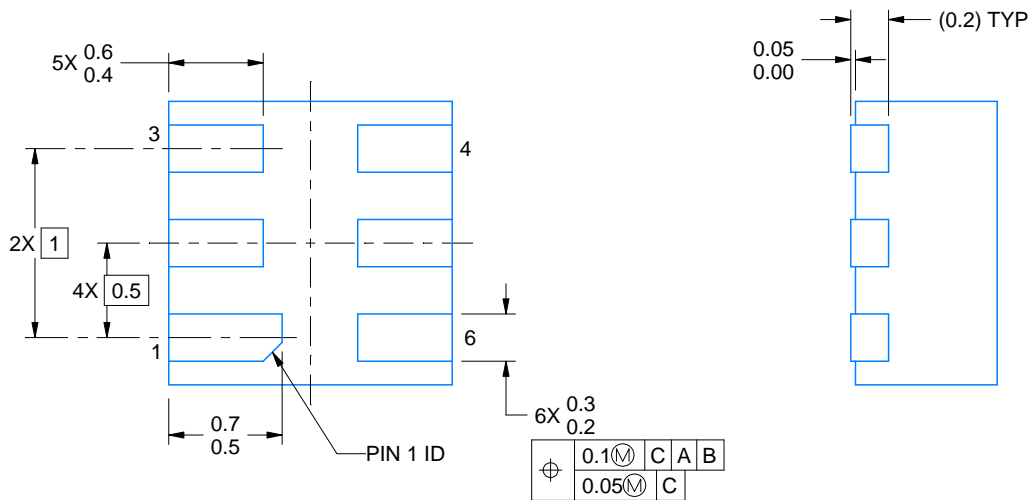
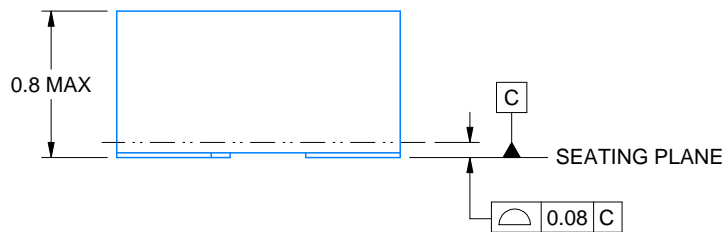
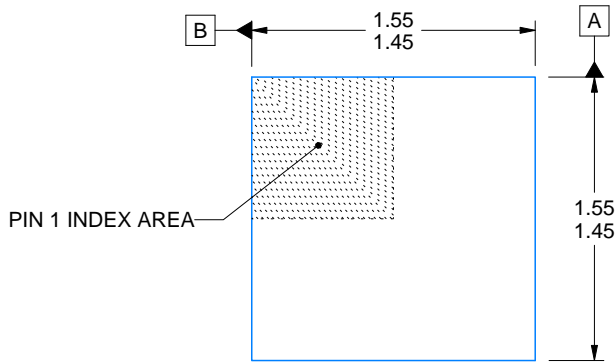
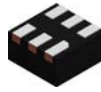


SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



4220552/B 01/2024

NOTES:

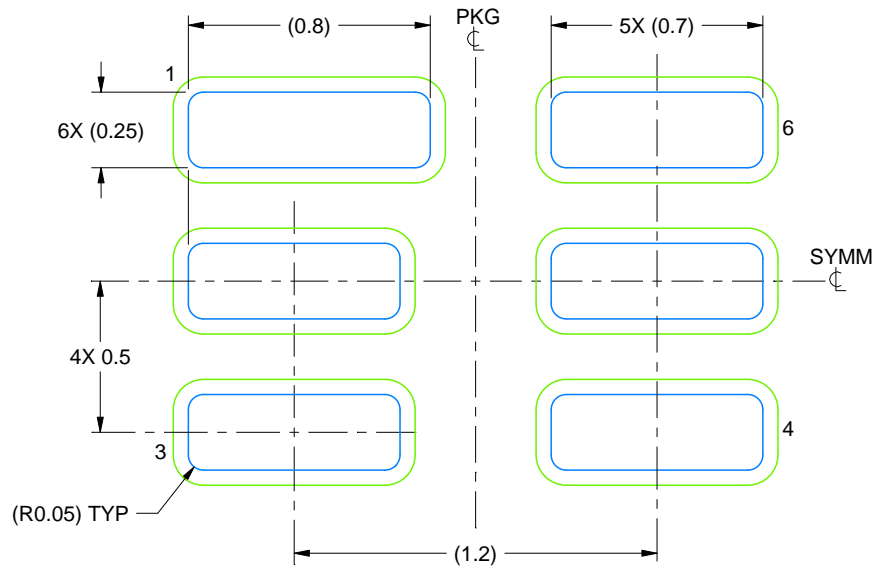
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

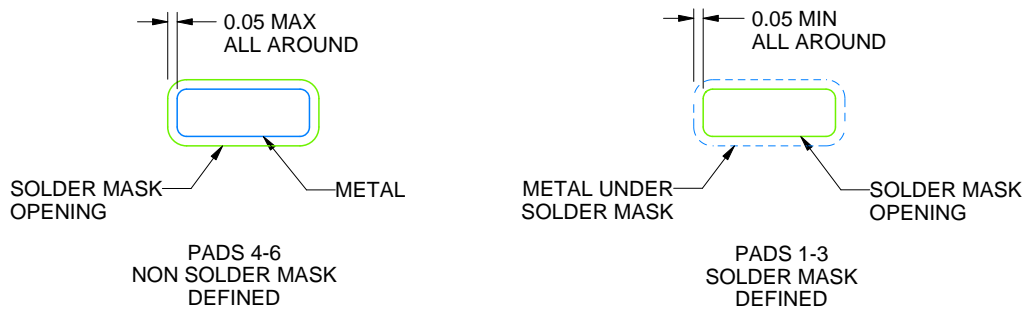
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

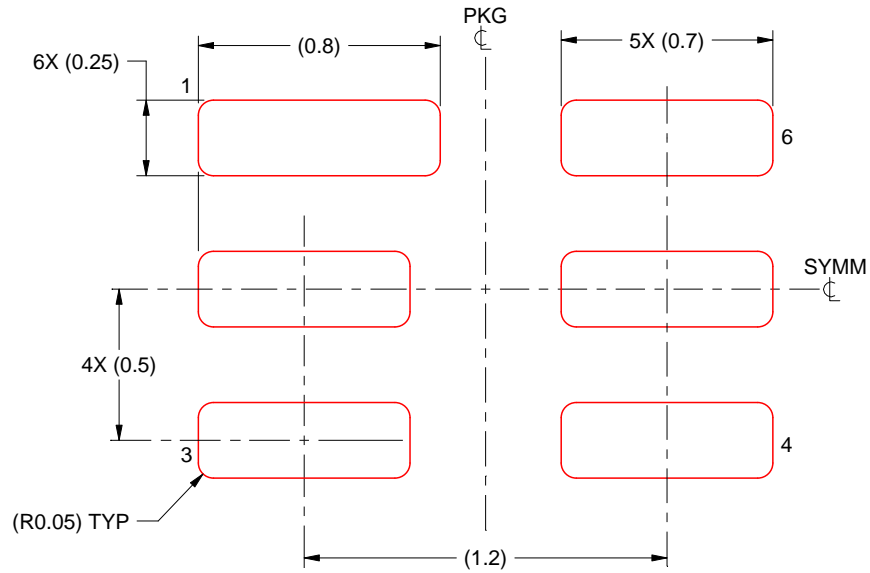
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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