

SGLS369A-AUGUST 2006-REVISED NOVEMBER 2006

FEATURES

- Controlled Baseline
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- 3-Pin SOT-23 Package
- Supply Current of 9 µA (Typical)
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION

The TPS3809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

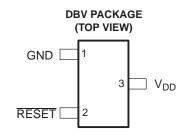
During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT} . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(typ)} = 200$ ms, starts after V_{DD} has risen above the V_{IT} . When the supply voltage drops below the V_{IT} , the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense V_{IT} set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TPS3809 devices are characterized for operation over a temperature range of –55°C to 125°C.

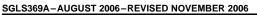


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- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator With Fixed Delay Time of 200 ms
- Pin-for-Pin Compatible With MAX 809

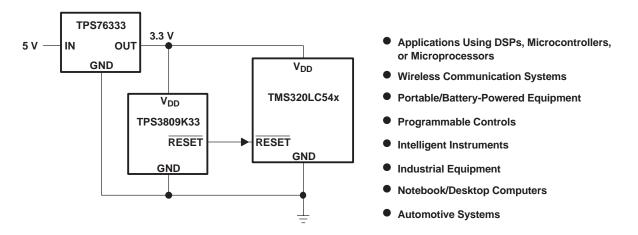


TPS3809L30-EP, TPS3809K33-EP, TPS3809I50-EP 3-PIN SUPPLY VOLTAGE SUPERVISORS





TYPICAL APPLICATIONS



AVAILABLE OPTIONS

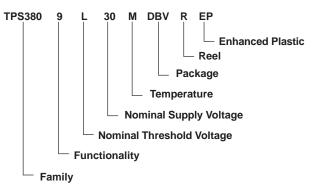
T _A	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
	TPS3809L30MDBVREP ⁽¹⁾	2.64 V	PLYM
–55°C to 125°C	TPS3809K33MDBVREP ⁽¹⁾	2.93 V	PLZM
	TPS3809I50MDBVREP ⁽¹⁾	4.55 V	PMAM

(1) The DBVR passive indicates tape and reel of 3000 parts.

FUNCTION/TRUTH TABLE

$V_{DD} > V_{IT}$	RESET
0	L
1	н

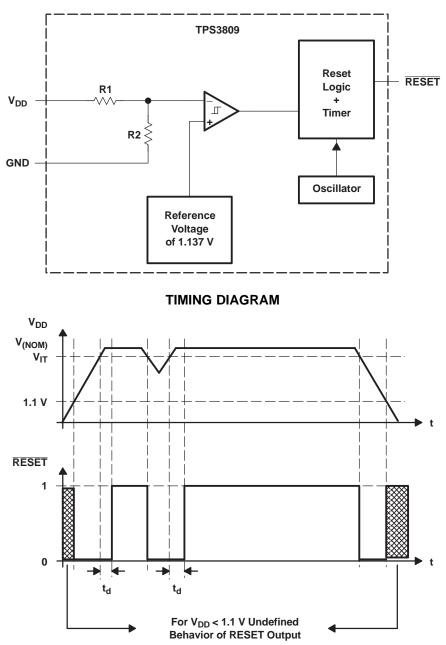
ORDERING INFORMATION



TPS3809L30-EP, TPS3809K33-EP, TPS3809I50-EP 3-PIN SUPPLY VOLTAGE SUPERVISORS

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FUNCTIONAL BLOCK DIAGRAM



TPS3809L30-EP, TPS3809K33-EP, TPS3809I50-EP 3-PIN SUPPLY VOLTAGE SUPERVISORS

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply voltage ⁽²⁾	V _{DD}		7	V
	Supply Voltage	All other pins	-0.3	7	v
I _{OL}	Maximum low output current			5	mA
I _{OH}	Maximum high output current			-5	mA
I _{IK}	Input clamp current	$V_l < 0 \text{ or } V_l > V_{DD}$		±20	mA
I _{OK}	Output clamp current	$V_{O} < 0 \text{ or } V_{O} > V_{DD}$		±20	mA
	Continuous total power dissipation		See Di	ssipation	Rating Table
T _A	Operating free-air temperature range		-55	125	°C
T _{stg}	Storage temperature range		-65	150	°C
	Soldering temperature			260	°C

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(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

Dissipation Ratings

PACKAGE	T _A < 25°C	DERATING FACTOR	T _A = 70°C	T _A = 85°C
	POWER RATING	ABOVE T _A = 25°C	POWER RATING	POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	6	V
T _A	Operating free-air temperature	-55	125	°C

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMET	ER	1	EST CONDITION	S	MIN	TY P	MAX	UNIT
			$V_{DD} = 2.5 V \text{ to } 6 V,$	I _{OH} = -500 μA		V _{DD} - 0.2			
	Link laurel euteurt :	ve låe ve	V _{DD} = 3.3 V,	$I_{OH} = -2 \text{ mA}$		V _{DD} - 0.4			V
V _{OH}	High-level output v	lage	$V_{DD} = 6 V,$	$I_{OH} = -4 \text{ mA}$		V _{DD} - 0.4			v
			V _{DD} = 6 V,	$I_{OH} = -4 \text{ mA},$	$T_A = 125^{\circ}C$	V _{DD} – 0.5			
			$V_{DD} = 2 V \text{ to } 6 V,$	I _{OL} = 500 μA				0.2	
V _{OL}	Low-level output v	oltage	V _{DD} = 3.3 V,	$I_{OL} = 2 \text{ mA}$				0.4	V
			V _{DD} = 6 V,	$I_{OL} = 4 \text{ mA}$				0.4	
	Power-up reset vo	ltage ⁽¹⁾	$V_{DD} \ge 1.1 V$,	I _{OL} = 50 μA				0.2	V
		TPS3809L30				2.58	2.6 4	2.7	
V _{IT-}	Negative-going input threshold voltage ⁽²⁾	TPS3809K33				2.87	2.9 3	2.99	V
	. enage	TPS3809150				4.45	4.5 5	4.65	
		TPS3809L30					35		
V _{hys}	Hysteresis	TPS3809K33					40		mV
		TPS3809I50					60		
	Supply ourrent		$V_{DD} = 2 V$,	Output unconnec	ted		9	12	
I _{DD}	Supply current		V _{DD} = 6 V,	Output unconnec	ted		20	25	μA
Ci	Input capacitance		$V_{I} = 0 V \text{ to } V_{DD}$				5		pF

The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 µs/V.
To ensure best stability of the threshold voltage, a bypass capacitor (0.1-µF ceramic) should be placed near the supply terminals.

Timing Requirements

 R_{L} = 1 MΩ, C_{L} = 50 pF, T_{A} = 25°C

	PARAMETER	TEST CONDITIONS	MIN MAX	UNIT
tw	Pulse width at V _{DD}	$V_{DD} = V_{IT-} + 0.2 \text{ V}, V_{DD} = V_{IT-} - 0.2 \text{ V}$	3	μs

Switching Characteristics

 R_L = 1 M Ω , C_L = 50 pF, T_A = 25°C

	PARAMET	ER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _d	Delay time	$V_{DD} \ge V_{IT-}$ + 0.2 V, See timing diagram	120	200	280	ms	
t _{PHL}	Propagation (delay) time, high- to low-level output	V _{DD} to RESET delay	$V_{IL} = V_{IT-} - 0.2 V,$ $V_{IH} = V_{IT-} + 0.2 V$		1		ms



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LOW-LEVEL OUTPUT VOLTAGE **HIGH-LEVEL OUTPUT VOLTAGE** vs VS LOW-LEVEL OUTPUT CURRENT **HIGH-LEVEL OUTPUT CURRENT** 2.75 6.5 $V_{DD} = 2.5 V$ $V_{DD} = 6 V$ 6.0 2.50 /OH – High-Level Output Voltage – V 5.5 VoL – Low-Level Output Voltage – V 2.25 5.0 2.00 4.5 -40°C T_A = 25°C T_A = 1.75 4.0 1.50 3.5 $T_A = \overline{0^{\circ}C}$ 3.0 T_A = 85°C 1.25 T_A = 85°C 2.5 T_A = 0°C 1.00 2.0 0.75 T_A =−40°C 1.5 0.50 1.0 T_A = 25°C 0.25 0.5 0.00 0.0 5.0 0.0 2.5 7.5 10.0 12.5 -10 -20 0 -30 -40 -50 IOL - Low-Level Output Current - mA IOH - High-Level Output Current - mA Figure 2. Figure 1. **HIGH-LEVEL OUTPUT VOLTAGE** NORMALIZED INPUT THRESHOLD VOLTAGE VS vs **HIGH-LEVEL OUTPUT CURRENT** FREE-AIR TEMPERATURE AT VDD 3.00 Normalized Threshold Voltage VIT (TA), VIT (25 $^\circ\text{C})$ 1.001 $V_{DD} = 2.5 V$ V_{DD} = 2.3 V 2.75 VOH – High-Level Output Voltage – V 1.000 2.50 2.25 0.999 2.00 T_A =−40°C 1.75 0.998 1.50 T_A = 0°C 1.25 0.997 1.00 T_A = 85°C 0.75 0.50 T_A = 25°C 0.996 0.25 0.995 0.00 0 -2 -4 -40 -20 20 40 60

TYPICAL CHARACTERISTICS

-10

0

T_A – Free-Air Temperature – °C

Figure 4.

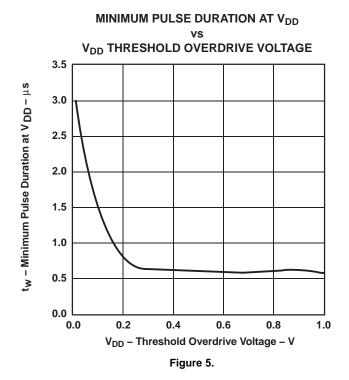
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IOH - High-Level Output Current - mA

Figure 3.

-8

TYPICAL CHARACTERISTICS (continued)





PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead finish/	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	Ball material	(3)		(4/5)	
TPS3809I50MDBVREP	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	(6) NIPDAU	Level-1-260C-UNLIM	-55 to 125	РМАМ	Samples
TPS3809K33MDBVREP	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLZM	Samples
TPS3809L30MDBVREP	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLYM	Samples
V62/06636-01XE	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLYM	Samples
V62/06636-02XE	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PLZM	Samples
V62/06636-03XE	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	PMAM	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



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OTHER QUALIFIED VERSIONS OF TPS3809-EP :

- Catalog: TPS3809
- Automotive: TPS3809-Q1

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3809I50MDBVREP	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809K33MDBVREP	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809L30MDBVREP	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3

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PACKAGE MATERIALS INFORMATION

22-Dec-2016



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3809I50MDBVREP	SOT-23	DBV	3	3000	182.0	182.0	20.0
TPS3809K33MDBVREP	SOT-23	DBV	3	3000	182.0	182.0	20.0
TPS3809L30MDBVREP	SOT-23	DBV	3	3000	182.0	182.0	20.0

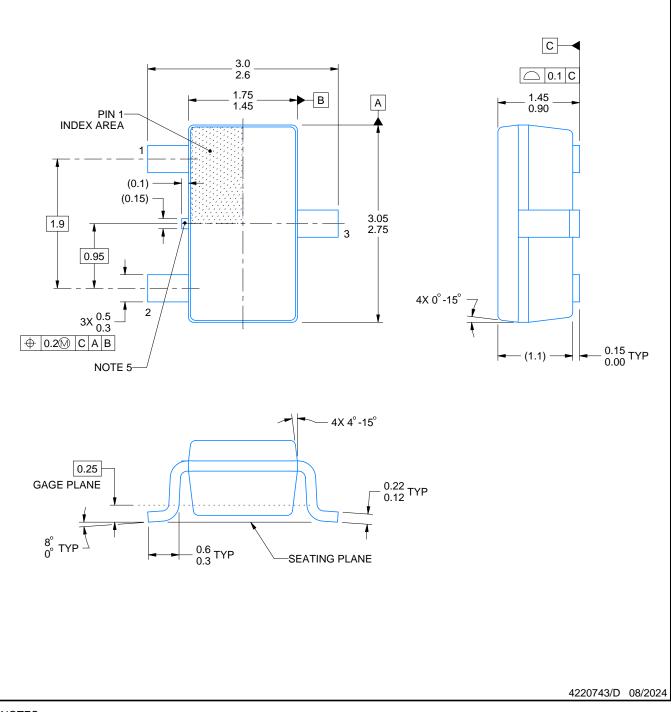
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PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. Refernce JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.

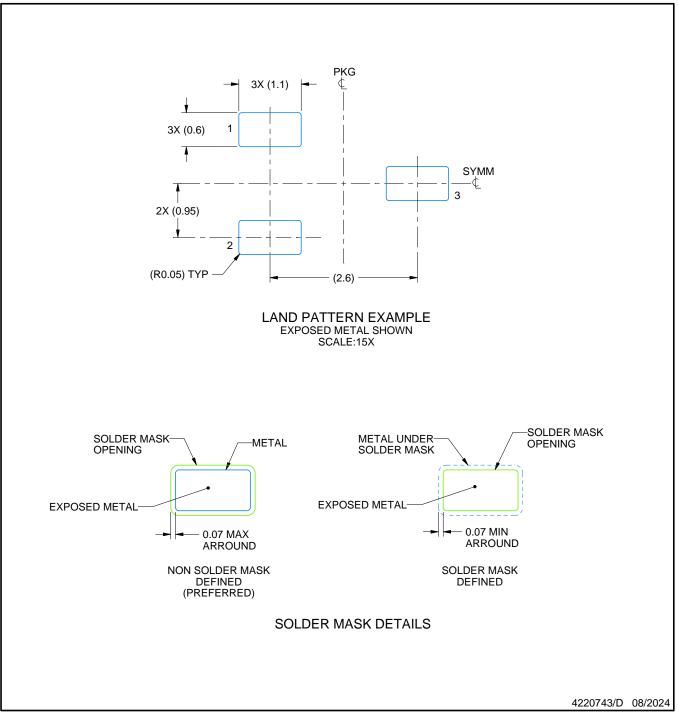


DBV0003A

EXAMPLE BOARD LAYOUT

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

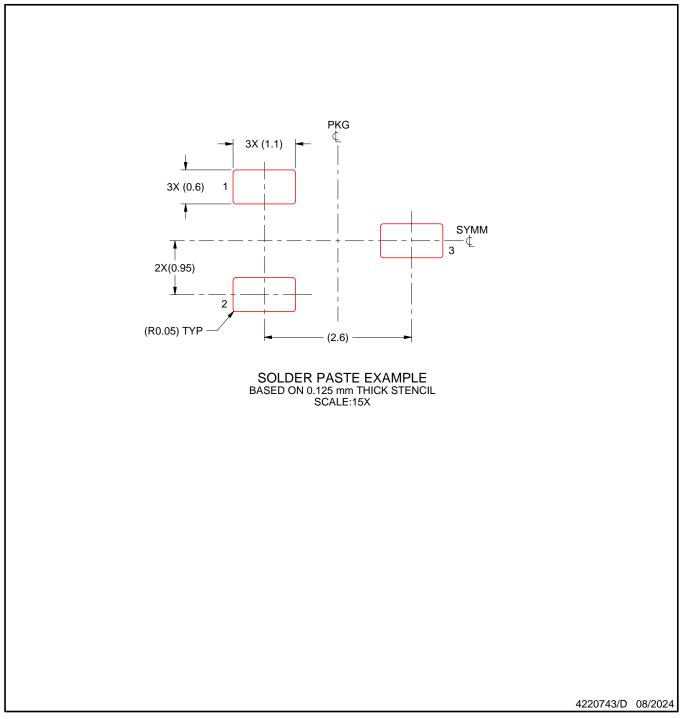


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EXAMPLE STENCIL DESIGN

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



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