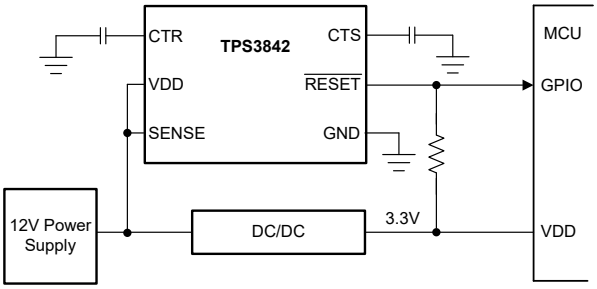
TPS3842 42V 小型、850nA 低電圧スーパーバイザ、プログラマブル遅延およびグリッチ除去機能付き

1 特長

- 広い電源電圧範囲:1.9V～42V
- VDD、SENSE、$\overline{\text{RESET}}$ は 42V 定格
- 低い静止電流:850nA (標準値)
- 高いスレッショルド精度:0.5% (標準値)
- 固定の内部スレッショルド電圧:2.7V～9.5V
- 可変電圧バリアント:0.7 V
- 遅延時間を CTR ピンによりコンデンサでプログラム可能
- グリッチ除去時間を CTS ピンによりコンデンサでプログラム可能
- オープン ドレイン、アクティブ Low 出力
- 温度範囲:-40℃～125℃
- 小型:SOT5X3 (DRL)

2 アプリケーション

- ファクトリ オートメーション
- モーター ドライブ
- 電力供給
- エンタープライズ システム
- グリッド インフラ



代表的なアプリケーション回路

3 概要

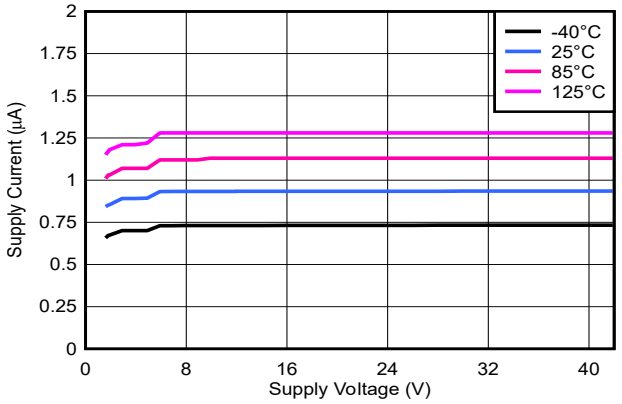
TPS3842 は、I_{DD} = 850nA、精度 0.5%、高速な検出時間を特長とする 42V 電圧検出器です。このデバイスは、12V/24V の電圧レールに直接接続して、低電圧 (UV) 状態を継続的に監視できます。TPS3842 はサイズの制約があるアプリケーション向けに小型の DRL パッケージで供給されています。SENSE ピンに組み込まれたヒステリシスは、電源電圧レール監視中のリセット信号の誤検出を防止します。1%、5%、10% のヒステリシス電圧を選択でき、設計の柔軟性により電圧過渡に対応できます。

SENSE は VDD から切り離されているため、VDD よりも高い電圧と低い電圧を監視できます。固定スレッショルド バリアントは、高精度の低 IQ 電圧監視を実現します。可変スレッショルド バリアントは、外付け抵抗により柔軟な低電圧スレッショルド設定を実現します。TPS3842 は、CTS ピンにより SENSE でコンデンサ プログラマブルなグリッチ除去機能および CTR ピンによりコンデンサ プログラマブルなリセット遅延タイミングを提供します。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
TPS3842	SOT5X3 (6)	1.20mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



電源電圧と電源電流との関係

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4 Device Comparison

Device Naming Convention shows some of the device naming nomenclature of the TPS3842. For a detailed breakdown of every device part number by features, thresholds, and analog out scale see 表 4-1 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.

表 4-1. Device Threshold Table

ORDERABLE PART NAME	THRESHOLD VOLTAGE	HYSTERESIS
TPS3842A011DRLR	700mV	1%
TPS3842A010DRLR	700mV	10%

1. Listed percentage denotes hysteresis tolerance, see セクション 6.5 for more information.
2. 700mV threshold with ADJ denotes an adjustable voltage threshold set by an external resistor divider, see セクション 7.3.1 for more information on how to set the threshold.

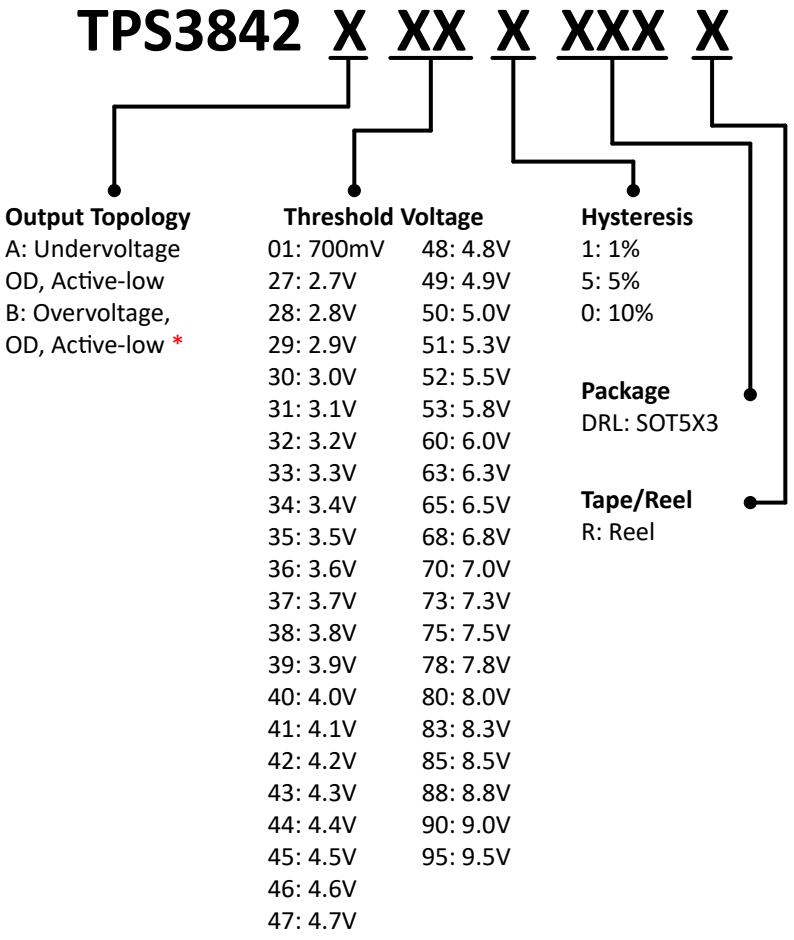

図 4-1. Device Naming Convention

1. Suffix 01 with V_{ITN} of 700mV corresponds to the adjustable variant, does not have internal voltage divider resistor ladder.

5 Pin Configuration and Functions

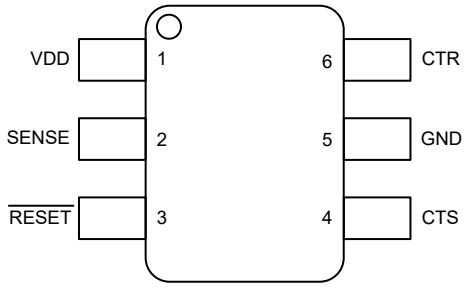

図 5-1. DRL Package
6-Pin SOT5X3
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT5X3		
VDD	1	I	Supply voltage pin.
SENSE	2	I	Sense input. Monitors input voltage based on internal voltage threshold. See セクション 7.3.1 for more details.
$\overline{\text{RESET}}$	3	O	Output reset signal. Connect $\overline{\text{RESET}}$ to pull up voltage using a pull up resistance.See セクション 7.3.4 for more details.
CTS	4	I	Sense time delay: Capacitor programmable sense delay: CTS pin offers a user adjustable sense delay time when asserting a reset condition. See セクション 7.3.2 for more details.
GND	5	—	Ground pin.
CTR	6	I	Reset time delay: User-programmable reset time delay for $\overline{\text{RESET}}$ pin. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See セクション 7.3.3 for more details.

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}, V_{SENSE}, $V_{\overline{RESET}}$	–0.3	50	V
Voltage	V_{CTR}, V_{CTS}	–0.3	5.5	V
Current	$I_{\overline{RESET}}$		±40	mA
Temperature (2)	Operating junction temperature, T_J	-55	150	°C
	Operating free-air temperature, T_A	-55	150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) As a result of the low dissipated power in this device, the operating temperature is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.9		42	V
V_{SENSE}	Sense pin voltage	0		42	V
V_{CTR}	CTR pin voltage			5	V
V_{CTS}	CTS pin voltage			5	V
$V_{\overline{RESET}}$	Output pin voltage	0		42	V
$I_{\overline{RESET}}$	Output pin current	0		10	mA
T_A	Junction temperature (free-air temperature)	-40		125	℃

6.4 Thermal Information

THERMAL METRIC(1)		TPS3842 DRL 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	153.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.9		42	V
V_{POR}	Power on reset voltage(1)	V_{OL}(max) = 0.25V, $I_{\overline{RESET}\ (Sink)}$ = 15µA			1.3	V
V_{ITN}	Negative-going threshold accuracy	Fixed internal threshold, V_{ITN} = 2.7V to 9.5V	-1.5	±0.5	1.5	%
V_{ITN}	Negative-going threshold accuracy	Adjustable internal threshold, V_{ITN} = 700mV	-1.5	±0.5	1.5	%
V_{HYS}	Hysteresis Voltage(2)	1% Variant	0.5	1	1.5	%
V_{HYS}	Hysteresis Voltage(2)	5% Variant	4.5	5	5.5	%
V_{HYS}	Hysteresis Voltage(2)	10% Variant	9.5	10	10.5	%
I_{DD}	Supply current	VDD = 12V, $\overline{RESET}$ = Not asserted		0.85	1.9	µA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = V_{ITN}, Adjustable version			25	nA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 12V, Fixed versions		1.35	2.5	µA
V_{OL}	Low level output voltage	1.9V ≤ V_{DD} < 42V, $I_{\overline{RESET}\ (Sink)}$ = 0.5mA			300	mV
I_{LKG}	Open drain output leakage current	V_{DD} = $V_{\overline{RESET}}$ = 12V			300	nA

(1) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.
(2) Hysteresis is with respect of the tripoint V_{ITN}.

6.6 Timing Requirements

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
$t_{GI\ (VITN)}$	Glitch Immunity undervoltage $V_{IT-(UV)}$, 20% Overdrive(1)	CTS = Open		5		µs

(1) 20% Overdrive from threshold. Overdrive % = [V_{SENSE} - V_{ITN}] / V_{ITN}

6.7 Switching Characteristics

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_{CTR}	Reset time delay	CTR = Open		250		µs
t_{CTR}	Reset time delay	CTR = 0.1uF		285.8		ms
t_{CTR}	Reset time delay	CTR = 3.3uF		9.43		s
t_{PD}	Propagation detect delay(1) (2)	CTS = Open, ADJ Vth		7		µs
t_{PD}	Propagation detect delay(1) (2)	CTS = Open, Fixed Vth		9		µs
t_{CTS}	Sense time delay	CTS = 0.1uF		300		ms
t_{SD}	Startup delay(3)			300		µs

(1) 20% Overdrive from threshold. Overdrive % = [V_{SENSE} - V_{ITN}] / V_{ITN}
(2) t_{PD} measured from threhold trip point (V_{ITN}) to $\overline{RESET}$ V_{OL} voltage
(3) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least t_{SD} + t_D + t_{CTR} before the output is in the correct state.

6.8 Timing Diagram

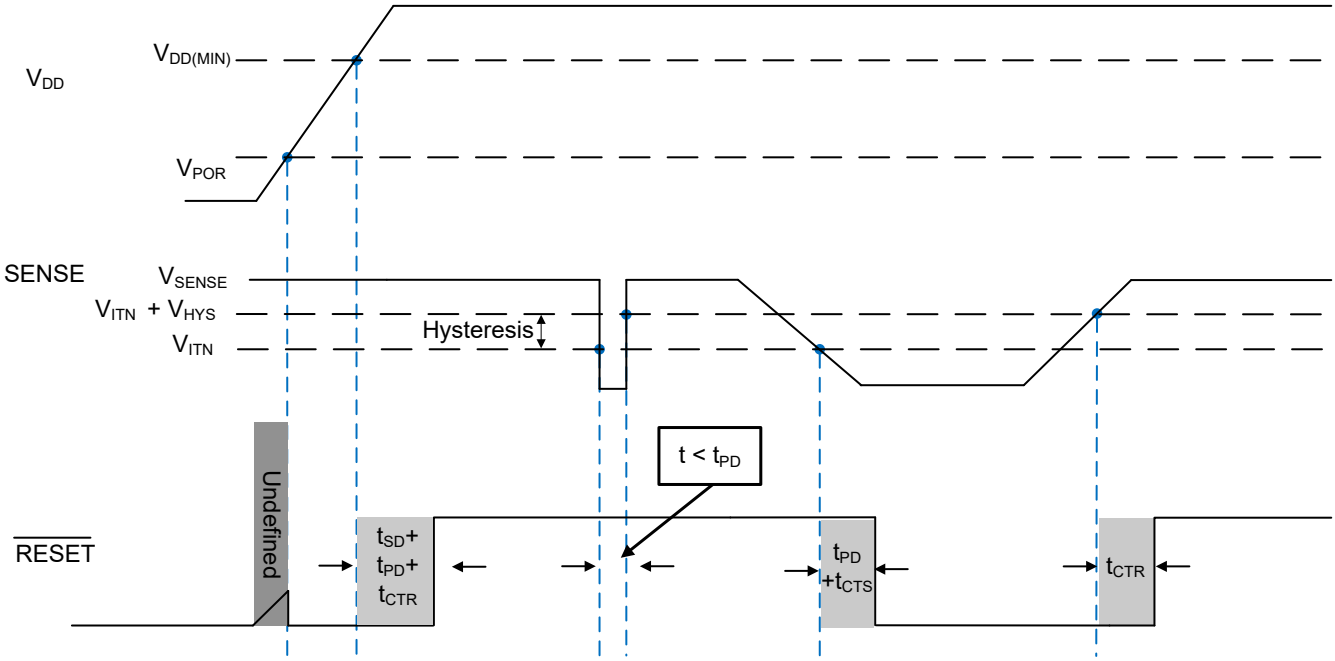

図 6-1. Timing Diagram

6.9 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3V, R_{RESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

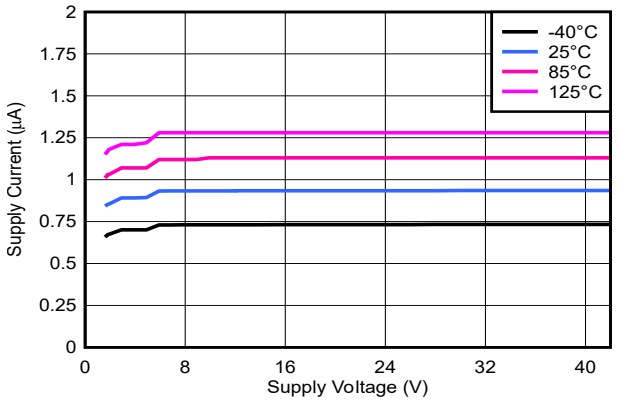

図 6-2. Supply Current vs Supply Voltage

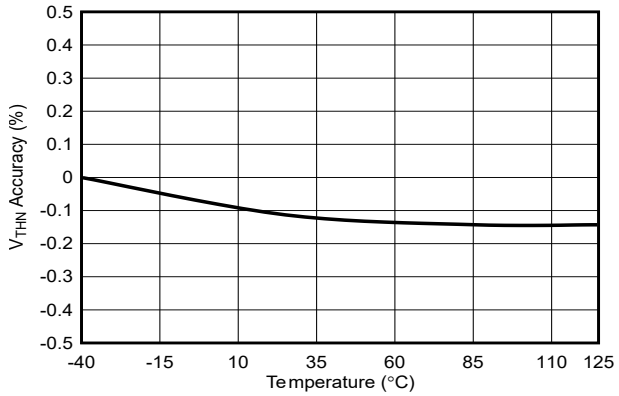

図 6-3. V_{THN} Accuracy vs Temperature

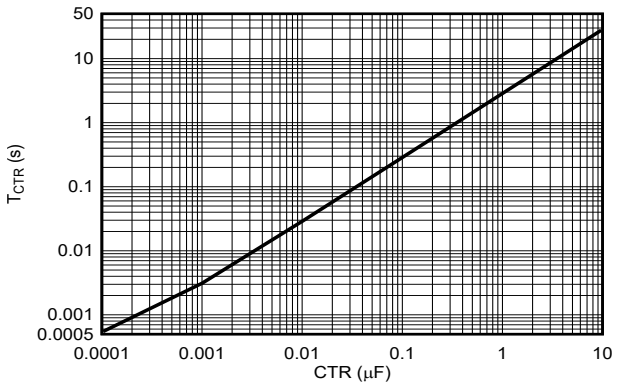

図 6-4. T_{CTR} vs CTR

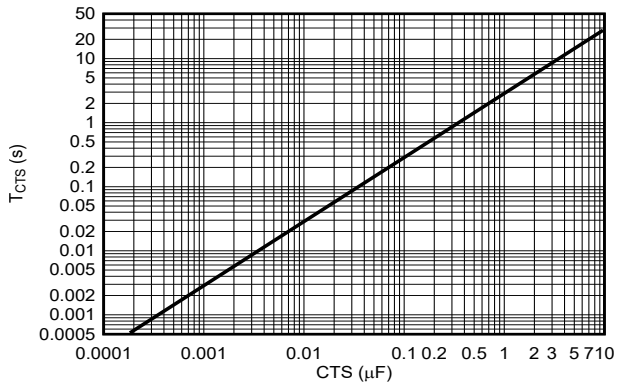

図 6-5. T_{CTS} vs CTS

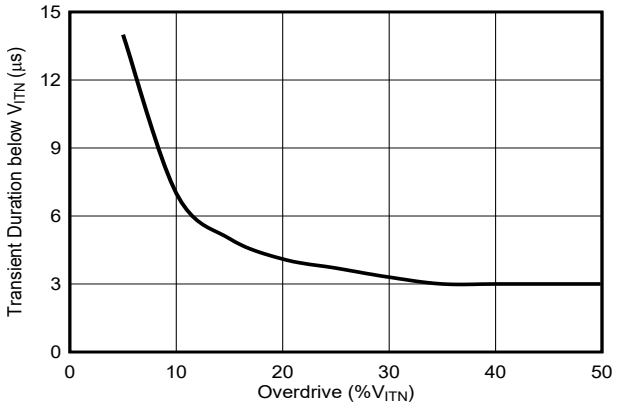

図 6-6. Transient Duration at Sense vs Sense Threshold Overdrive Voltage (CTS = Open)

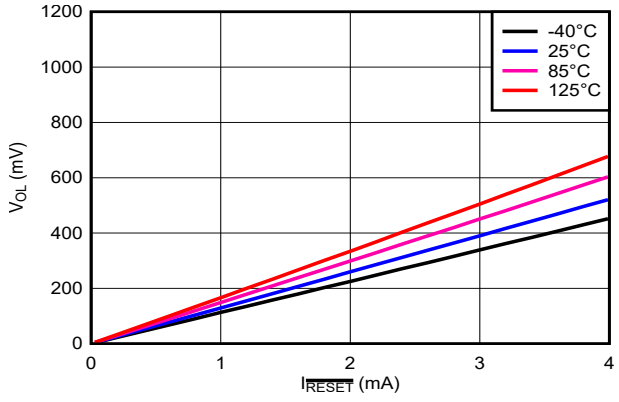

図 6-7. RESET Current (Sink) vs V_{OL} (V_{DD} = 3.3V)

6.9 Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3V, R_{RESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

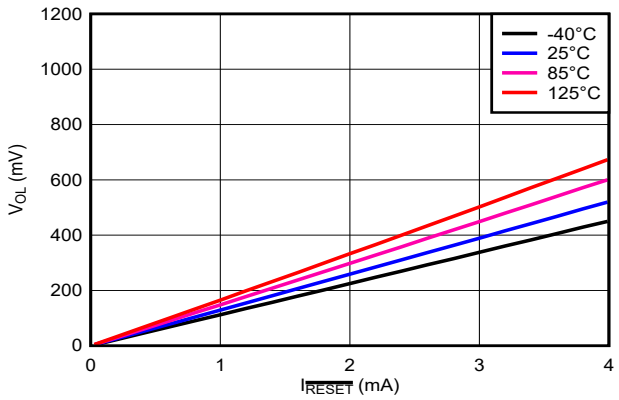

図 6-8. RESET Current (Sink) vs V_{OL} (V_{DD} = 12V)

7 Detailed Description

7.1 Overview

The TPS3842 high voltage supervisor product family is designed to assert a $\overline{\text{RESET}}$ signal when the SENSE pin voltage drops below V_{ITN} and stays below V_{ITN} for user defined time. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time until after SENSE voltages returns above the respective threshold and hysteresis.

VDD, SENSE and $\overline{\text{RESET}}$ pins can support 42V continuous operation. All VDD, SENSE, and $\overline{\text{RESET}}$ voltage levels can be independent of each other. The TPS3842 features capacitor programmable sense time delay (CTS) to set a minimum duration of a undervoltage event before $\overline{\text{RESET}}$ is asserted. CTS feature also functions as a programmable de-glitch to avoid false resets. The TPS3842 also features a capacitor programmable reset time delay (CTR) to set a minimum duration of $\overline{\text{RESET}}$ assertion after a undervoltage event recovers.

7.2 Functional Block Diagrams

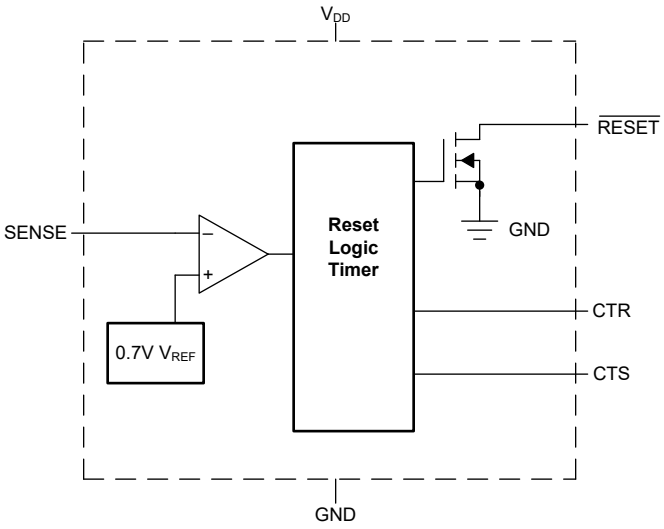

図 7-1. Adjustable-Voltage Version

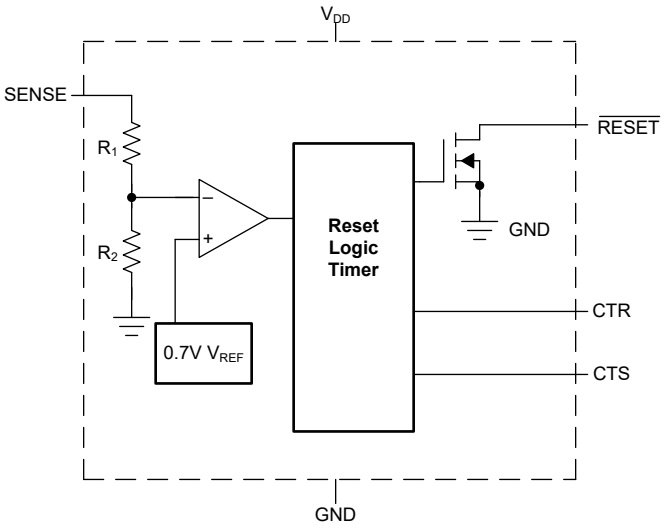

図 7-2. Fixed-Voltage Version

7.3 Feature Description

A broad range of voltage threshold and hysteresis options are available for the TPS3842, allowing this device to be used in a wide array of applications. Reset threshold voltages can be factory-set from adjustable 0.7V or fixed from 2.7V to 9.5V. The adjustable variant can be set to any voltage above 0.7V using an external resistor divider. Connecting a capacitor between CTR and GND allows the designer to select any reset delay period up to 10µF. Connecting a capacitor between CTS and GND allows the designer to select any sense delay period up to 10µF.

7.3.1 SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{ITN} for a t_{PD}+t_{CTS} time interval, then $\overline{RESET}$ is asserted. The comparator has a built-in hysteresis to suppress unintended $\overline{RESET}$ assertions and de-assertions. For noisy envirionments, good analog design practice is to put a 1nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics or leaverage the CTS feature to set a minimum fault time interval before $\overline{RESET}$ is asserted.

図 7-3 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 700mV threshold option when using an external resistor divider. The variant bypasses the internal resistor ladder for higher accuracy when using external resistors.

For example, consider a 12V rail, V_{MON}, being monitored for undervoltage (UV) using of the TPS3842A011DRLR variant, as shown in 図 7-3. The monitored UV threshold, denoted as V_{MON-}, is the desired voltage where the device asserts the reset. For this example V_{MON-} = 5.8V. To assert an undervoltage reset the voltage at the sense pin, V_{SENSE}, needs to be equal to the input threshold negative, V_{ITN}. For this example variant V_{SENSE} = V_{ITN} = 0.7V. Using R_1 and R_2 the correlation between V_{MON-} and V_{SENSE} can be seen in 式 1. Assuming R_1 = 100kΩ, and R_2 can be calculated as R_2 = 13.7kΩ.

$$V_{SENSE} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (1)$$

The TPS3842 hysteresis depends on the configuration selected. For the reset signal to become deasserted, V_{MON} must go above V_{ITN} + V_{HYS}. For this example variant a 1% voltage threshold hysteresis was selected. Therefore, V_{MON} equals 5.858V when the reset signal becomes deasserted. If a 10% hysteresis option was instead used, V_{MON} equals 6.38V when the reset signal becomes deasserted.

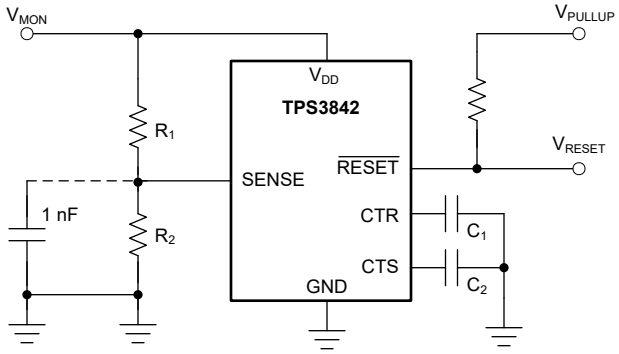

図 7-3. Using the TPS3842A011DRLR to Monitor a User-Defined Threshold Voltage

7.3.1.1 SENSE Hysteresis

TPS3842 device offers built-in hysteresis around the UV threshold to avoid erroneous $\overline{RESET}$ deassert. The hysteresis (V_{HYS}) is opposite to the threshold voltage for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

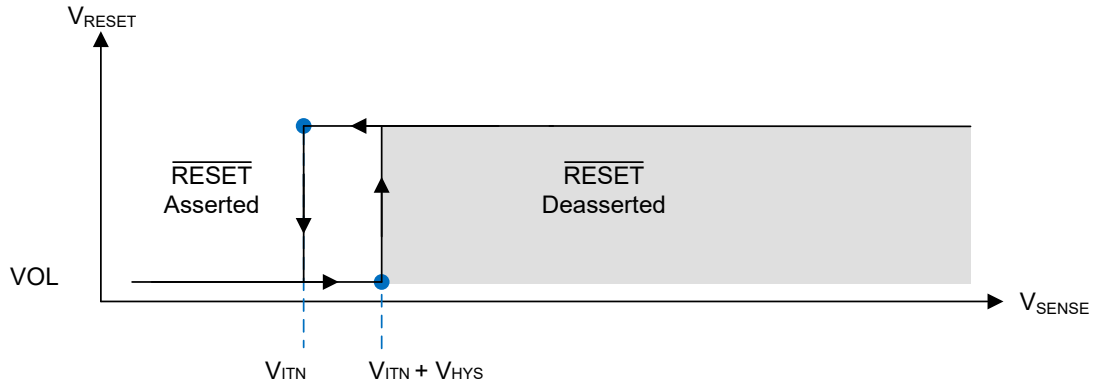

図 7-4. Hysteresis (Undervoltage Active-Low)

表 7-1. Common Adjustable Hysteresis Lookup Table

Part Number	DEVICE HYSTERESIS OPTION
TPS3842Axx**1**DRLR	1%
TPS3842Axx**5**DRLR	5%
TPS3842Axx**0**DRLR	10%

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is (V_{ITN} + V_{HYS}). Hysteresis is dependent on the device V_{ITN} including V_{ITN} accuracy and deviations.

Undervoltage (UV)

V_{ITN} = 700mV

Voltage Hysteresis (V_{HYS}) = 1% = V_{ITN} x 1% = 7mV

Release Voltage = V_{ITN} + V_{HYS} = 707mV

7.3.2 Selecting the SENSE Delay Time

TPS3842 has adjustable sense time delay with external capacitors.

- A capacitor on CTS programs the minimum fault time interval before $\overline{\text{RESET}}$ is asserted.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{PD} in セクション 6.6.
- Parasitic capacitance on the CTS pin counts as CTS capacitance and increases t_{CTS}.

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS\_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by 式 2.

$$t_{CTS\ (typ)} = 2.858 \times C_{CTS\_EXT\ (typ)} \quad (2)$$

$t_{CTS\ (typ)}$ = is given in seconds (s)

$C_{CTS\_EXT\ (typ)}$ = is given in microfarads (µF)

The sense delay varies according to the external capacitor (C_{CTS_EXT}). The minimum and maximum variance due to the constant is show in 式 3 and 式 4:

$$t_{CTS\ (max)} = 3.715 \times C_{CTS\_EXT\ (max)} \quad (3)$$

$$t_{CTS\ (min)} = 2 \times C_{CTS\_EXT\ (min)} \quad (4)$$

Make sure there is enough time for the capacitor to fully discharge when a voltage fault occurs to prevent the CTS capacitor from having charge before the next fault. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip earlier or later near the threshold.

* Leakages on the capacitor can effect accuracy of sense time delay.

7.3.3 Selecting the RESET Delay Time

TPS3842 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time.
- Parasitic capacitance on the CTR pin counts as CTR capacitance and increases t_{CTR}.

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR\_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by 式 5.

$$t_{CTR\ (typ)} = 2.858 \times C_{CTR\_EXT\ (typ)} \quad (5)$$

$t_{CTR\ (typ)}$ = is given in seconds (s)

$C_{CTR\_EXT\ (typ)}$ = is given in microfarads (µF)

The reset delay varies according to the external capacitor (C_{CTR_EXT}). The minimum and maximum variance due to the constant is show in 式 6 and 式 7:

$$t_{CTR\ (max)} = 3.715 \times C_{CTR\_EXT\ (max)} \quad (6)$$

$$t_{CTR\ (min)} = 2 \times C_{CTR\_EXT\ (min)} \quad (7)$$

Having a too large of a capacitor value (>10µF) can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{RESET}$ active.

* Leakages on the capacitor can effect accuracy of reset time delay.

7.3.4 RESET Output

$\overline{RESET}$ (active low) denoted with a bar above the pin label. $\overline{RESET}$ remains high voltage (V_{OH}, deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation above the threshold boundary and VDD voltage is above VDD(min). If SENSE falls below V_{ITN} for a time period longer than t_{PD}+t_{CTS}, $\overline{RESET}$ is asserted, driving the $\overline{RESET}$ pin to a low impedance.

Once SENSE is above V_{ITN} + V_{HYS}, a delay circuit (CTR) is enabled that holds $\overline{RESET}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{RESET}$ pin goes to a high impedance state.

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. $\overline{RESET}$ supports pull-up voltages up to 42V and is independent of VDD and SENSE voltages.

To select the right pull-up resistor, consider system V_{OH} and the Open-Drain Leakage Current (I_{LKG}) provided in the electrical characteristics to set the maximum pull-up resistor value. Low pull-up resistor values increase the amount of current through the internal open-drain output. The current through the open-drain output must be lower than the $I_{\overline{RESET}}$ of the device.

7.4 Device Functional Modes

表 7-2. Truth Table

SENSE > V_{ITN}	$\overline{RESET}$	VDD
0	L	VDD > VDD(min)
1	H	VDD > VDD(min)
0 or 1	L	VDD(min) > VDD > V_{POR}

7.4.1 Normal Operation (V_{DD} > $V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by the voltage on the SENSE pin.

- The $\overline{RESET}$ signal corresponds to the voltage on SENSE relative to V_{ITN}.

7.4.2 Above Power-On Reset but Less Than $V_{DD(min)}$ (V_{POR} < V_{DD} < $V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted and low impedance regardless of the voltage on the SENSE pin.

7.4.3 Below Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) needed to internally pull the asserted output to GND, $\overline{RESET}$ is undefined.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.2 Typical Application

A typical application of the TPS3842 used to monitor a 12V power rail is shown in 図 8-1. The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pullup resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below V_{POR}, but this characteristic is normally not a problem because most microprocessors do not function below this voltage.

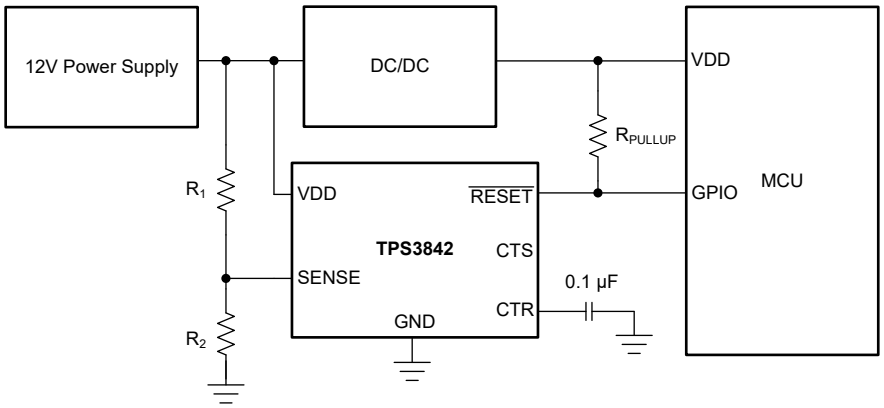

図 8-1. Typical Application of the TPS3842 Monitoring a 12V Power Supply

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Voltage Threshold	Typical UV voltage threshold 9.5V
Output logic	Open-Drain
SENSE delay	< 0.2ms
$\overline{\text{RESET}}$ delay	300ms

8.2.2 Detailed Design Procedure

The TPS3842 utilizes high-voltage SENSE and V_{DD} inputs to monitor a 12V power supply for undervoltage. In this design example TPS3842A011DRLR is used.

The negative-going threshold voltage, V_{ITN}, is set by the device variant. In this example, the nominal supply voltage from the power supply is 12V. Setting a undervoltage threshold of 9.5V (approximately 20% under 12V) makes sure that the device resets before supply voltage violates the allowed boundary. The adjustable voltage variant is chosen and R_1 and R_2 are adjusted to meet the threshold. Assuming R_2 equal to 10kΩ and R_1 is calculated as 125kΩ. For additional information on selecting resistor values see セクション 7.3.1. TPS3842 also supports fixed voltage threshold variants. Threshold voltage decoding can be found in Device Decoder.

8.2.2.1 Meeting the Sense and Reset Delay

The TPS3842 features both reset assertion (sense) delay, t_{CTS}, and reset deassertion (reset) delay, t_{CTR}. セクション 7.3.2 and セクション 7.3.3 show how to set the timings for the capacitor-programmable delays. The application requires less than 0.2ms sense delay, thus no capacitor is used and CTS is left open. The application requires greater than 300ms reset delay, thus a 0.1µF capacitor is used.

8.2.3 Application Curve

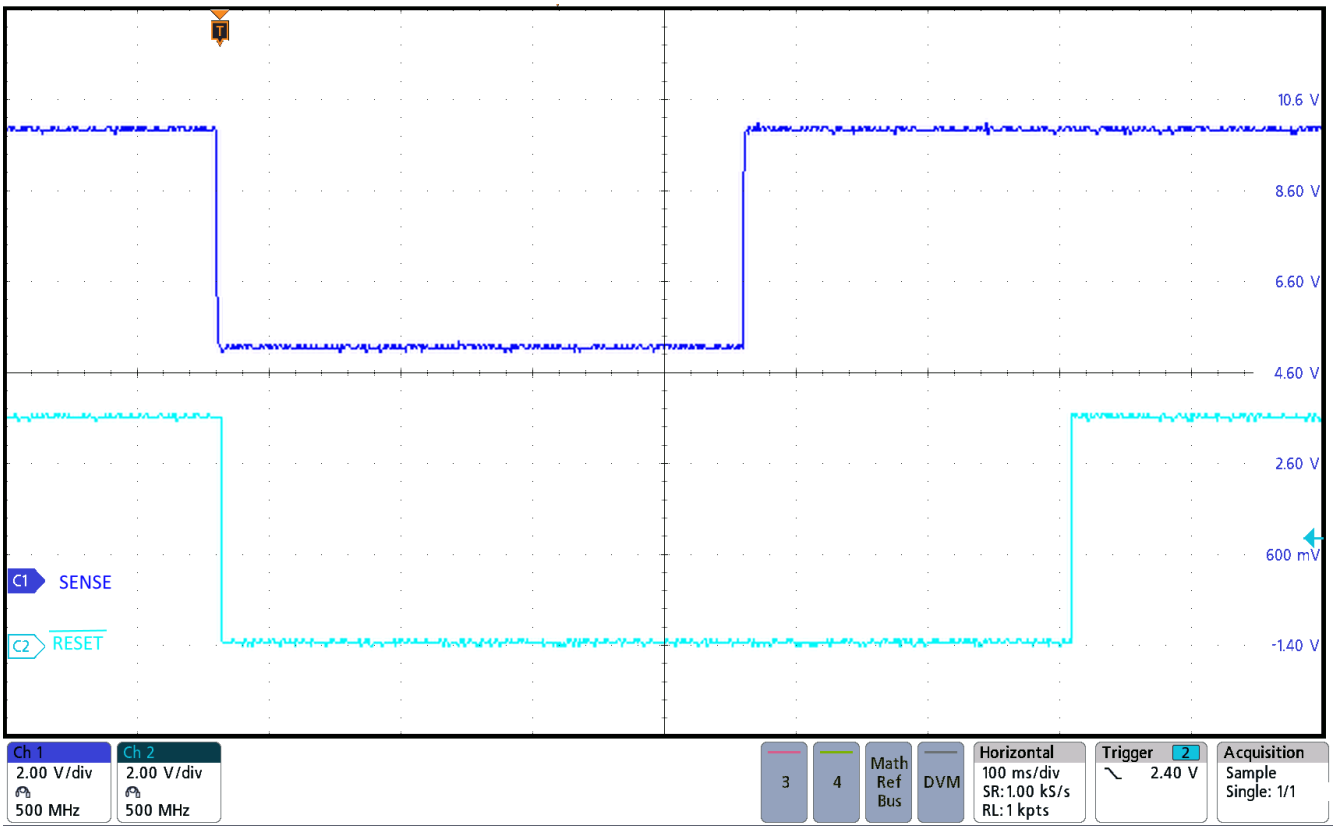

図 8-2. TPS3842 Detecting Undervoltage Fault and $\overline{\text{RESET}}$ Recovery

8.2.4 Power Supply Recommendations

TPS3842 is designed to operate from an input supply with a V_{DD} voltage between 1.9V (minimum operation) to 42V (maximum operation). Good analog design practice recommends placing a minimum 0.1µF ceramic capacitor as near as possible to the V_{DD} pin.

8.2.5 Layout

8.2.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1µF ceramic capacitor as near as possible to the VDD pin.
- For noisy envirionments and to improve noise immunity on the SENSE pins, an optional 1nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. An alternative to improve noise immunity is to use the CTS feature.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance to not affect the t_{PD} or t_{CTR}.
- Place the pull-up resistors on $\overline{\text{RESET}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible.

- Do not have high voltage metal pads or traces closer than 20mils (0.5mm) to the low voltage metal pads or traces.

8.2.5.2 Layout Example

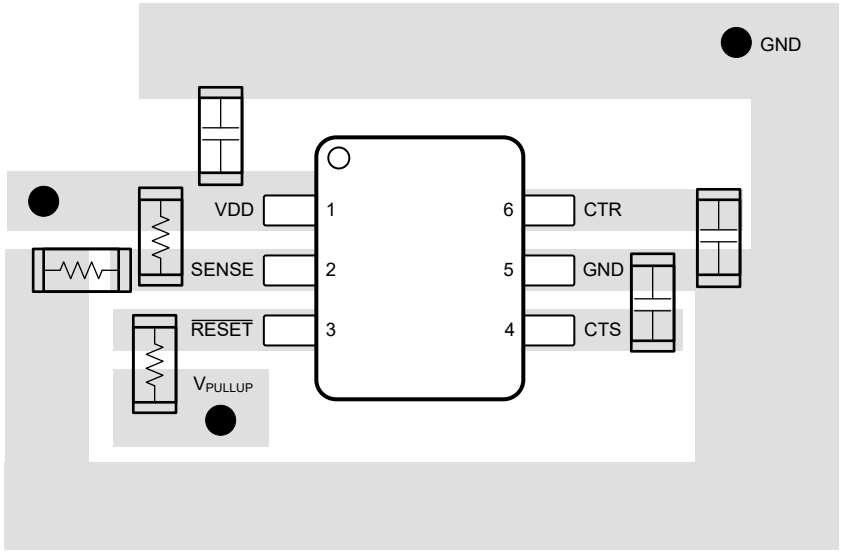

図 8-3. TPS3842 Reccomended Layout

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2024) to Revision A (August 2024)	Page
• 量産データのリリース	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3842A010DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A010	Samples
TPS3842A011DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A011	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3842 :

- Automotive : TPS3842-Q1

NOTE: Qualified Version Definitions:

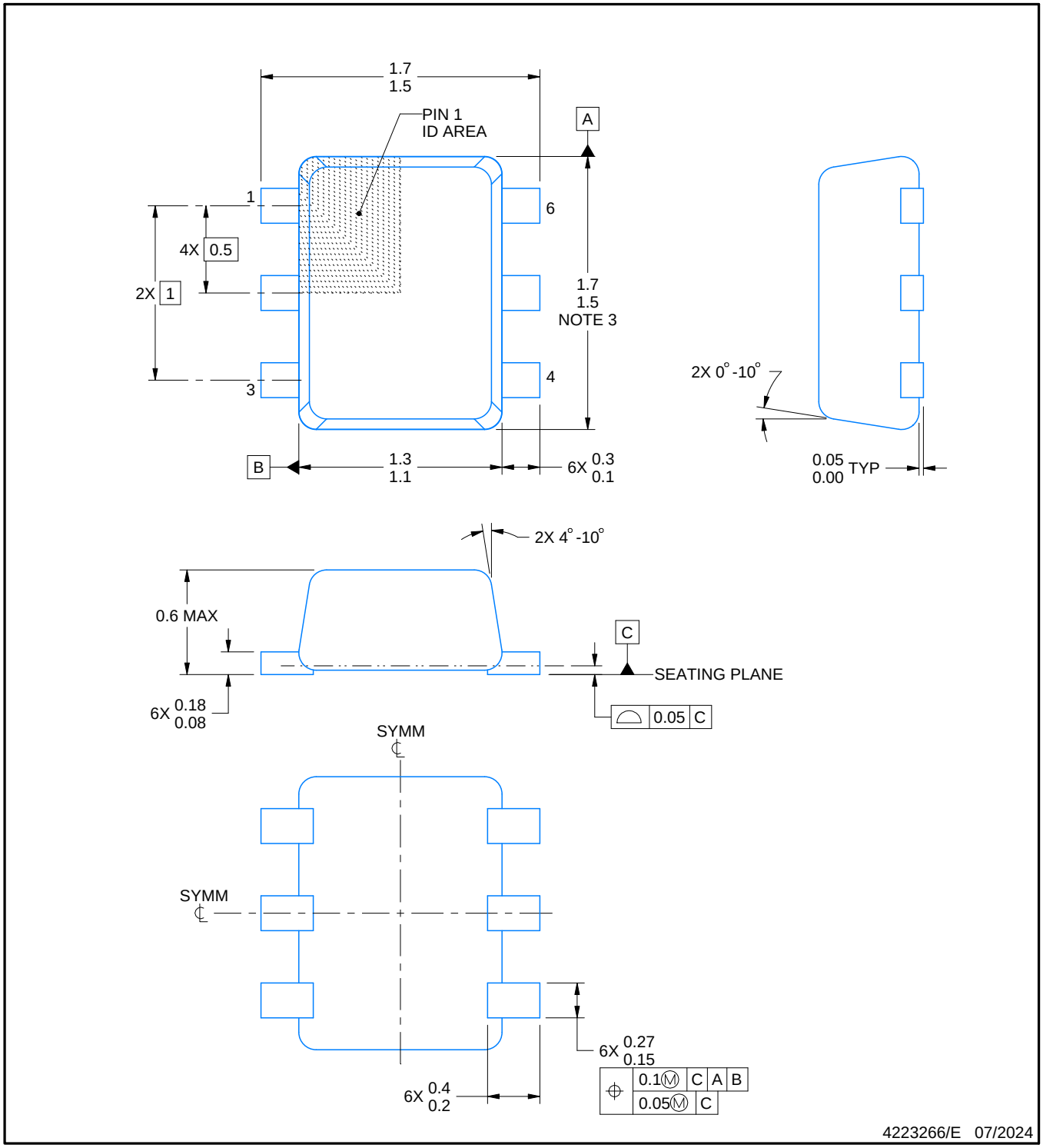
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

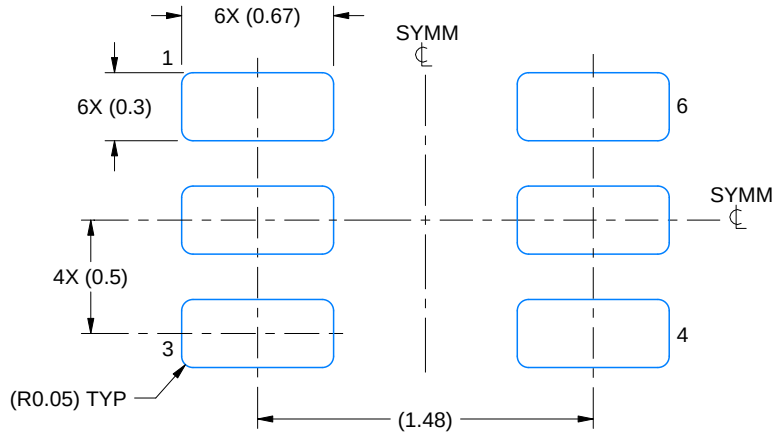
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

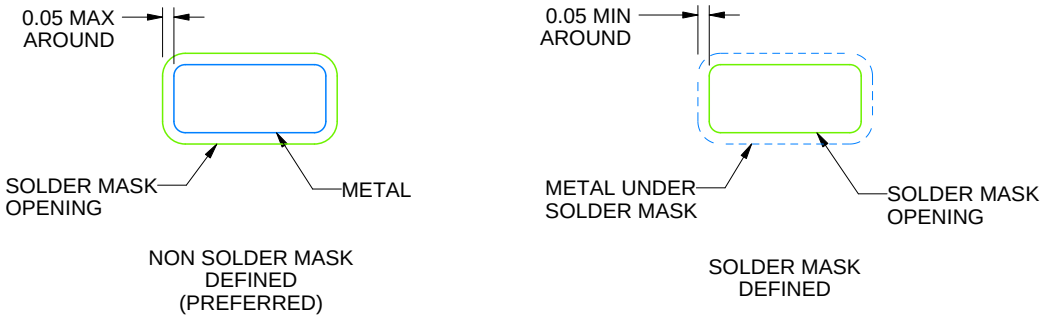
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X

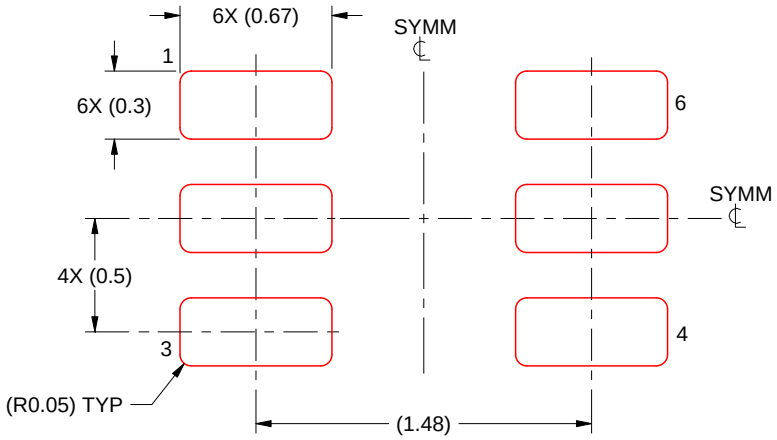


SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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