TEXAS INSTRUMENTS
TPS4810-Q1
JAJSOG7 – JANUARY 2024

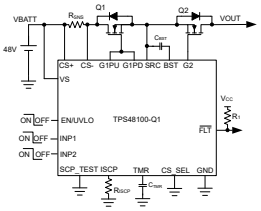
TPS4810-Q1 短絡保護および診断機能搭載、100V、車載用、低 I_Q、バック ツー バック MOSFET スマート ハイサイド ドライバ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～+125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 3.5V～80 の入力範囲 (絶対最大定格 100V)
- 最低 –65V までの逆入力保護
- 345µA の電流能力を持つ内蔵 11V チャージ ポンプ
- 低い静止電流:35µA (動作時)
- 低シャットダウン電流 (EN/UVLO = Low):1.5µA
- 個別の制御入力 (INP1、INP2) でのバック ツー バック MOSFET 駆動用の 2 つの強力なゲートドライバ (2A ソースおよびシンク)
- 外付けの Rsense または可変遅延 (TMR) 付き MOSFET VDS センシングを使用する、可変短絡保護 (ISCP)
- ハイサイドまたはローサイドの電流検出構成 (CS_SEL)
- 短絡フォルト時のフォルト表示 ($\overline{FLT}$)、チャージ ポンプ低電圧、入力低電圧、短絡コンパレータの診断 (SCP_TEST)
- 調整可能な入力低電圧誤動作防止 (UVLO)
- TPS1210-Q1 とピン互換

2 アプリケーション

- 車載用 48V リチウムイオン バッテリ管理システム
- DC/DC コンバータ
- 車載用パワー ディストリビューション ボックス
- コードレス電動工具



個別の放電および充電 FET 制御付き BMS ブレーカ

3 概要

TPS48100-Q1 は、保護および診断機能を備えた、100V、低 I_Q、スマート ハイサイド ドライバです。本デバイスは 3.5V～80V の広い動作電圧範囲を持っているため、12V、24V、および 48V システムの設計に適しています。このデバイスは、最低 –65V の負の電源電圧に耐えられ、この電圧から負荷を保護できます。

コモン ソース構成でバック ツー バック MOSFET を駆動するために、独立した制御入力 (INP1、INP2) を備えた 2 つの強力な 2A (ソースとシンク) ゲートドライバを備えています。強力な GATE 駆動により、大電流システム設計で並列 MOSFET を使用した電力スイッチングが可能になります。

このデバイスは、可変短絡保護機能を備えています。自動リトライおよびラッチオフ フォルト動作は設定可能です。電流検出は、外付けの検出抵抗、または MOSFET VDS センシングのいずれかを使用して実行できます。CS_SEL ピン入力を使用して、ハイサイドまたはローサイドの電流検出抵抗構成が可能です。このデバイスは、SCP_TEST 入力の外部制御を使用した、内蔵の短絡コンパレータを診断する機能も備えています。

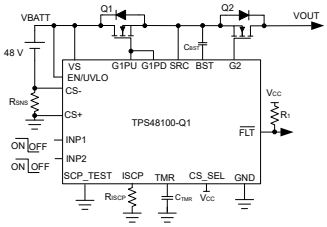
動作時の静止電流 (35µA、標準値) が低いため、常時オンのシステム設計が可能になります。EN/UVLO が Low で、静止電流が 1.5µA (標準値) まで低減します。

TPS48100-Q1 は、19 ピンの VSSOP パッケージで供給されます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ (公称) (2)
TPS48100-Q1	DGX (VSSOP、19)	5.1mm × 3.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



ローサイド電流検出付き BMS ブレーカ

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4 Pin Configuration and Functions

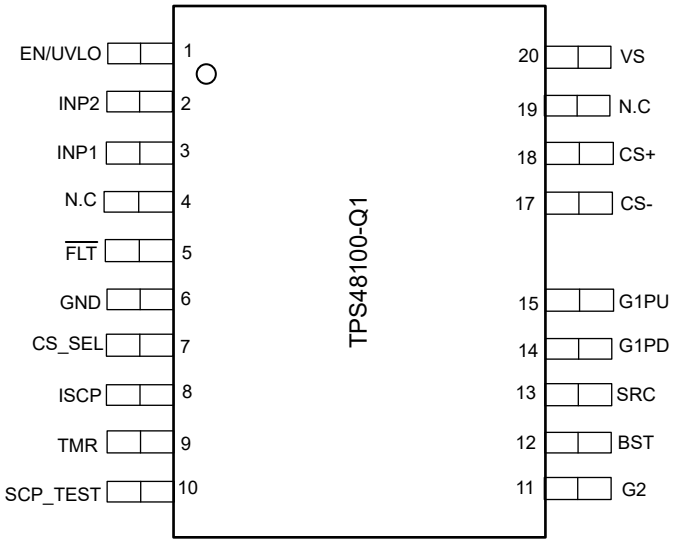

図 4-1. DGX Package, 19-Pin VSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
EN/UVLO	1	I	EN/UVLO Input. A voltage on this pin above 1.24V enables normal operation. Forcing this pin below 0.3V shuts down the device reducing quiescent current to approximately 1.5µA. Optionally connect to the input supply through a resistive divider to set the undervoltage lockout. When EN/UVLO is left floating an internal pull down of 100nA pulls EN/UVLO low and keeps the device in shutdown state.
INP2	2	I	Input signal for external charge FET control. CMOS compatible input reference to GND that sets the state of G2 pin. INP2 has an internal weak pull down of 100nA to GND to keep G2 pulled to SRC when INP2 is left floating.
INP1	3	I	Input signal for external discharge FET control. CMOS compatible input reference to GND that sets the state of G1PD and G1PU pins. INP1 has an internal weak pull down of 100nA to GND to keep G1PD pulled to SRC when INP1 is left floating.
N.C	4	—	No connect.
$\overline{\text{FLT}}$	5	O	Open drain fault output. This pin asserts low during short circuit fault, charge pump UVLO, input UVLO, and during SCP comparator diagnosis. If $\overline{\text{FLT}}$ feature is not desired then connect it to GND.
GND	6	G	Connect GND to system ground.
CS_SEL	7	I	Current sense select input. Connect this pin to ground to activate high side current sense. Drive this pin to > 2V to activate low side current sensing. CS_SEL has an internal weak pull down of 100nA to GND.

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表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ISCP	8	I	Short circuit detection setting. A resistor across ISCP to GND sets the short circuit current comparator threshold. If short-circuit protection feature is not desired then connect CS+, CS–, and VS pins together. Also connect ISCP and TMR pins to GND.
TMR	9	I	Fault timer input. A capacitor across TMR pin to GND sets the times for fault turn-off. Leave it open for fastest setting. Leave this pin open for fastest response setting. If short-circuit protection feature is not desired then connect CS+, CS–, and VS pins together. Also, connect ISCP and TMR pins to GND.
SCP_TEST	10	I	Internal short circuit comparator (SCP) diagnosis input. When SCP_TEST is driven low to high with INP1 pulled high, the internal SCP comparator operation is checked. $\overline{FLT}$ goes low and G1PD gets pulled to SRC if SCP comparator is functional. Connect SCP_TEST pin to GND if this feature is not desired. SCP_TEST has an internal weak pull down of 100nA to GND.
G2	11	O	Charging FET gate drive output. It has 1.69A peak source and 2A sink capacity. Leave the G2 pin floating if the G2 drive functionality is unused.
BST	12	O	High side bootstrapped supply. An external capacitor with a minimum value of > $Q_{g(tot)}$ of the external FET must be connected between this pin and SRC.
SRC	13	O	Source connection of the external FET.
G1PD	14	O	High current gate driver pull-down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET.
G1PU	15	O	High current gate driver pull-up. This pin pulls up to BST. Connect this pin to G1PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on.
CS–	17	I	Current sense negative input
CS+	18	I	Current sense positive input.
N.C	19	—	No connect.
VS	20	P	Supply pin of the controller.

(1) I = Input, O = Output, I/O = Input and Output, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	VS, CS+, CS– to GND	–65	100	V
	SRC to GND	–65	100	V
	G1PU, G1PD, G2, BST to SRC	–0.3	19	V
	ISCP, TMR, SCP_TEST to GND	–0.3	5.5	V
	EN/UVLO, INP1, INP2, CS_SEL to GND, $V_{(VS)}$ > 0 V	–1	70	V
	EN/UVLO, INP1, INP2, CS_SEL to GND, $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(70 + $V_{(VS)}$)	V
	CS+ to GND, $V_{(VS)}$ > 0 V	–0.3	70	V
	CS+ to GND, $V_{(VS)}$ ≤ 0 V	$V_{(VS)}$	(100 + $V_{(VS)}$)	V
	CS+ to CS–	–1	100	V
Output pins	$\overline{FLT}$ to GND	–1	20	V
	G1PU, G1PD, G2, BST to GND	–65	112	V
Sink current	$I_{(\overline{FLT})}$		10	mA
	$I_{(CS+)}$ to $I_{(CS–)}$, 1 msec	–100	100	mA
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN/UVLO, VS, SCP_TEST, G2)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	VS to GND	3.5		80	V
	EN/UVLO, INP1, INP2, CS_SEL to GND	0		65	V
	SCP_TEST to GND	0		5	V
Output pins	$\overline{FLT}$ to GND	0		15	V
External capacitor	VS, SRC to GND	22			nF
	BST to SRC	0.1			µF
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

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5.4 Thermal Information

THERMAL METRIC(1)		TPS4810-Q1 DGX 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

T_J = –40 °C to +125°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VS	Operating input voltage		3.5		80	V
$I_{(Q)}$	Total system quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		35		µA
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V		1.5		µA
ENABLE, UNDERVOLTAGE LOCKOUT (EN/UVLO), SHORT CIRCUIT COMPARATOR TEST (SCP_TEST) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising			1.24		V
$V_{(UVLOF)}$	UVLO threshold voltage, falling			1.14		V
$V_{(ENR)}$	Enable threshold voltage for low Iq shutdown, rising				1.02	V
$V_{(ENF)}$	Enable threshold voltage for low Iq shutdown, falling		0.3			V
$V_{(SCP\_TEST)}$	SCP test mode rising threshold				1.02	V
$V_{(SCP\_TEST)}$	SCP test mode rising threshold		0.3			V
$I_{(EN/UVLO)}$	Enable input leakage current	$V_{(EN/UVLO)}$ = 48 V		180		nA
CHARGE PUMP (BST–SRC)						
$V_{(BST-SRC\_ON)}$	Charge Pump turn on voltage	$V_{(EN/UVLO)}$ = 2 V	10			V
$V_{(BST-SRC\_OFF)}$	Charge Pump turn off voltage	$V_{(EN/UVLO)}$ = 2 V			11.8	V
$V_{(BST\_UVLOR)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, rising	$V_{(EN/UVLO)}$ = 2 V			9.5	V
$V_{(BST\_UVLOF)}$	$V_{(BST-SRC)}$ UVLO voltage threshold, falling	$V_{(EN/UVLO)}$ = 2 V	7.2			V
$I_{(SRC)}$	SRC pin leakage current	$V_{(EN/UVLO)}$ = 2 V, $V_{(INP1)}$ = $V_{(INP2)}$ = 0 V		1		µA
GATE DRIVER OUTPUTS (G1PU, G1PD, G2)						
$I_{(G1PU)}$	Peak Source Current			1.69		A
$I_{(G2)}$	G2 Peak Source Current			1.69		A
$I_{(G1PD)}$	Peak Sink Current			2		A
$I_{(G2)}$	G2 Peak Sink Current			2		A
$V_{(G1\_GOOD)}$	VGS Good Threshold for G1 Gate Drive			7.5		V
SHORT CIRCUIT PROTECTION (ISCP)						

5.5 Electrical Characteristics (続き)

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCP)}$	SCP threshold	$R_{(ISCP)}$ = 145 kΩ	240	300	360	mV
		$R_{(ISCP)}$ = 32.5 kΩ		75		mV
		$R_{(ISCP)}$ = 15 kΩ		40		mV
DELAY TIMER (TMR)						
$I_{(TMR\_SRC\_CB)}$	TMR source current			80		µA
$I_{(TMR\_SRC\_FLT)}$	TMR source current			2.2		µA
$I_{(TMR\_SNK)}$	TMR sink current			2.5		µA
$V_{(TMR\_SC)}$				1.1		V
$V_{(TMR\_LOW)}$				0.2		V
$N_{(A\text{-}R\ Count)}$				32		
INPUT CONTROLS (INP1, INP2), CURRENT SENSE SELECT (CS_SEL) & FAULT FLAG ($\overline{FLT}$)						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance			70		Ω
$V_{(INP1\_H)}$, $V_{(INP2\_H)}$, $V_{(CS\_SEL\_H)}$					2	V
$V_{(INP1\_L)}$, $V_{(INP2\_L)}$, $V_{(CS\_SEL\_L)}$			0.8			V

5.6 Switching Characteristics

T_J = –40 ℃ to +125℃. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V, $V_{(SRC)}$ = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{G1PU(INP1\_H)}$	INP1 turn on propogation Delay	INP1 ↑ to G1PU ↑, C_L = 47 nF		1		µs
$t_{G2(INP2\_H)}$	INP2 turn on propogation Delay	INP2 ↑ to G2 ↑, C_L = 47 nF		5		µs
$t_{G1PD(INP1\_L)}$	INP1 turn off propogation Delay	INP1 ↓ to G1PD ↓, C_L = 47 nF		1		µs
$t_{G2(INP2\_L)}$	INP2 turn off propogation Delay	INP2 ↓ to G2 ↓, C_L = 47 nF		5		µs
$t_{PD(UVLO\_OFF)}$	UVLO turn off propogation Delay	UVLO ↓ to G1PD ↓, C_L = 47 nF		7.5		µs
$t_{PD(IFLT\_OFF)}$	Hard short-circuit protection propogation Delay	$V_{(CS+-CS-)}$ ↑ $V_{(SCP)}$ to G1PD ↓, C_L = 47 nF, $C_{(TMR)}$ = Open		4		µs
t_{SC_PUS}	Short circuit protection propogation delay during power up with output short circuit	$C_{(TMR)}$ = Open			10	µs

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6 Parameter Measurement Information

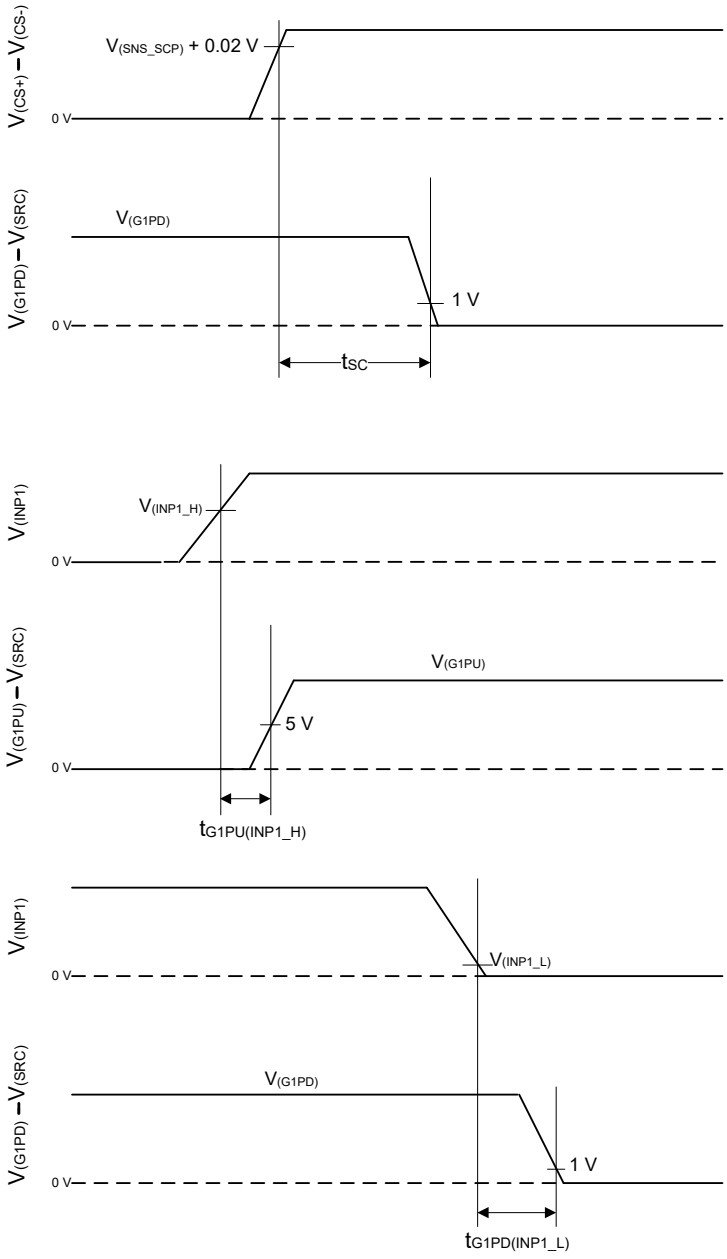


図 6-1. Timing Waveforms

7 Detailed Description

7.1 Overview

The TPS48100-Q1 is a 100V low IQ smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V–80V, the device is suitable for 12V, 24V, and 48V system designs. The device can withstand and protect the loads from negative supply voltages down to –65V.

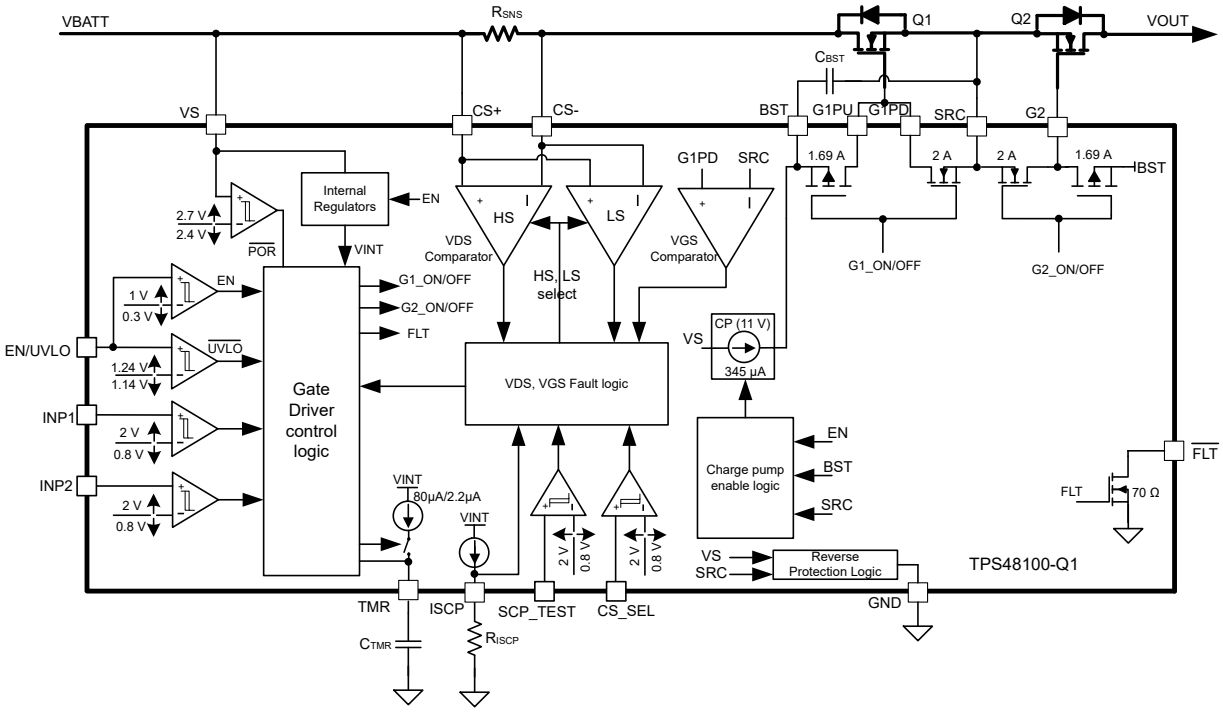
It has two strong 1.69A and 2A peak source and sink gate drivers with separate control inputs (INP1, INP2) to drive back to back MOSFETs in common source configuration. Strong GATE driving enables power switching using parallel FETs in high current system designs.

The device provides configurable short circuit protection using ISCP and TMR pins for adjusting the threshold and response time, respectively. Auto-retry and latch-off fault behavior can be configured. With TPS48100-Q1, current sensing can be done either by an external sense resistor or by MOSFET VDS sensing by using CS+ and CS– pins. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. Diagnosis of the integrated short circuit comparator is possible using external control on SCP_TEST input.

The device indicates fault ($\overline{FLT}$) on open drain output during short-circuit, charge pump undervoltage, and input undervoltage conditions.

Low quiescent current 35µA (typical) in operation enables always ON system designs. Quiescent current reduces to 1.5µA (typical) with EN/UVLO low.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Charge Pump and Gate Driver Output (VS, G1PU, G1PD, G2, BST, SRC)

図 7-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses two strong 1.69A/2A peak source/sink gate drivers enabling paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 11V, 345µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, C_{BST} that is placed across the gate driver (BST and SRC).

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the C_{BST} capacitor. After the voltage across C_{BST} crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The device has a 1V (typical) UVLO hysteresis to ensure chattering less performance during initial GATE turn ON. Choose C_{BST} based on the external FET Q_G and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches 11.8V, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to 10V typically at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between 11.8V and 10V as shown in the 図 7-2.

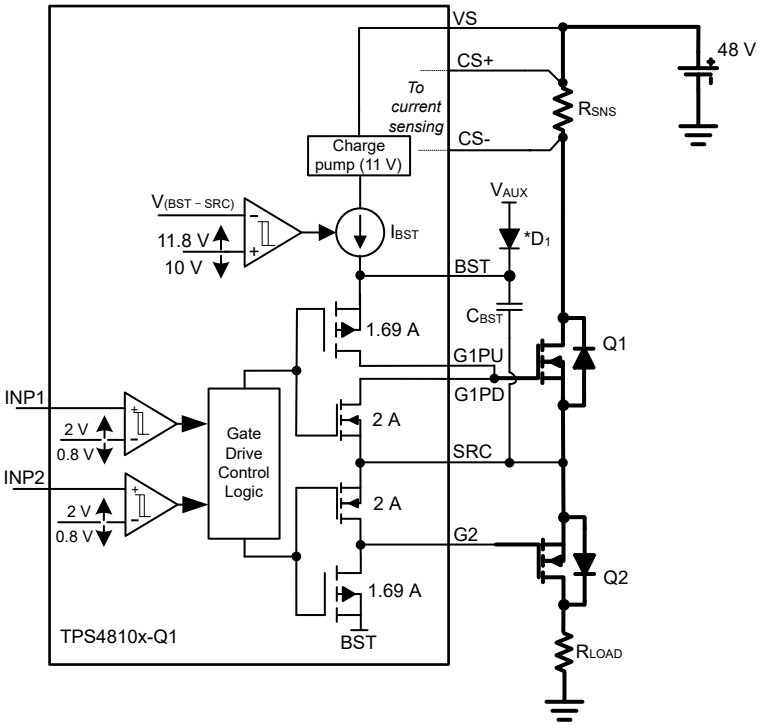

図 7-1. Gate Drivers

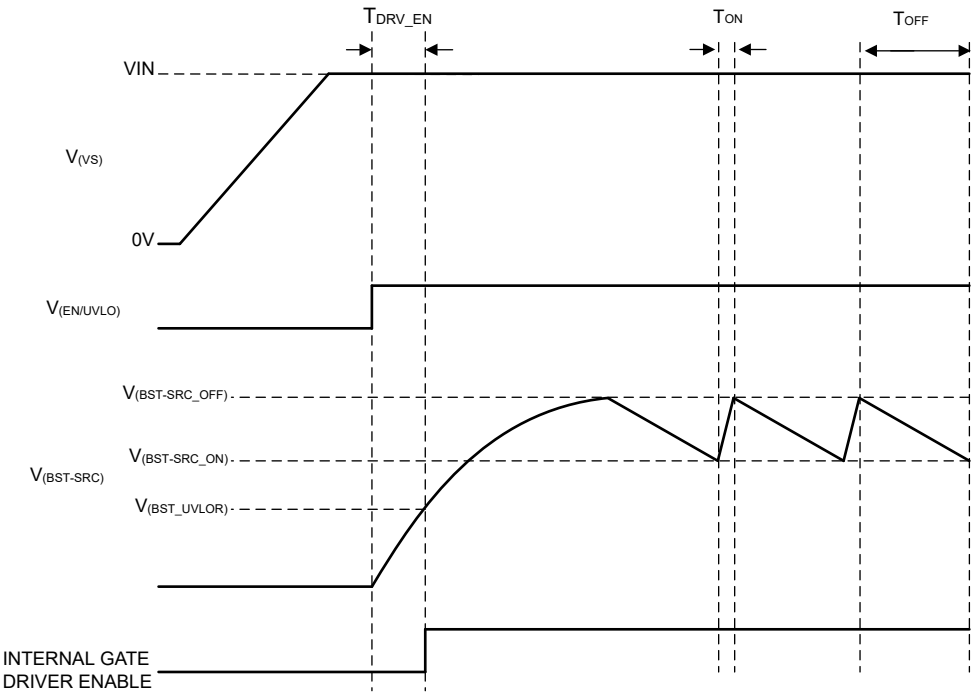

図 7-2. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay:

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{345\ \mu A} \quad (1)$$

Where,

C_{BST} is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 9.5V (max).

If T_{DRV_EN} needs to be reduced then pre-bias BST terminal externally using an external V_{AUX} supply through a low leakage diode D_1 as shown in 図 7-3. With this connection, T_{DRV_EN} reduces to 400µs. TPS48100-Q1 application circuit with external supply to BST is shown in 図 7-3.

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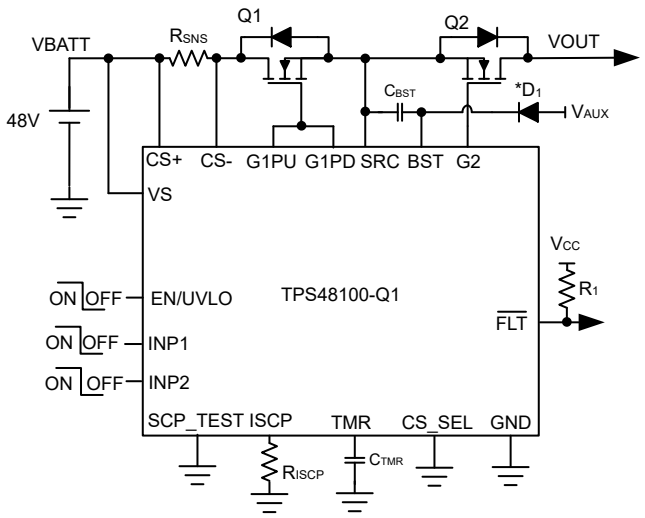

図 7-3. TPS48100-Q1 Application Circuit With External Supply to BST

注

V_{AUX} can be supplied by external regulated supply ranging between 8V and 18V.

7.3.2 Capacitive Load Driving Using FET Gate (G1PU, G1PD) Slew Rate Control

For limiting inrush current during turn-ON of the external FET (Q1) with capacitive loads, use R_1, R_2, C_1 as shown in 図 7-4. The R_1 and C_1 components slow down the voltage ramp rate at the gate of Q1 FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

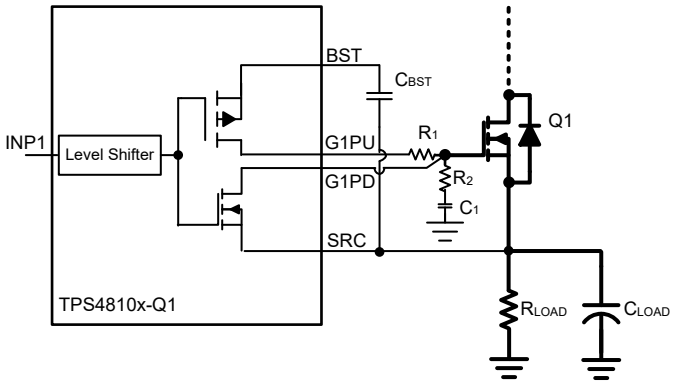

図 7-4. Inrush Current Limiting Using G1 Gate Drive

Use the 式 2 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \quad (2)$$

$$C_1 = \frac{0.63 \times V_{(BST\ -\ SRC)} \times C_{LOAD}}{R_1 \times I_{INRUSH}} \quad (3)$$

Where,

C_{LOAD} is the load capacitance.

VBATT is the input voltage and T_{charge} is the charge time.

$V_{(BST-SRC)}$ is the charge pump voltage (11V),

Use a damping resistor R_2 (approximately 10Ω) in series with C_1. 式 3 can be used to compute required C_1 value for a target inrush current. A 100kΩ resistor for R_1 can be a good starting point for calculations.

Connecting G1PD pin of TPS48100-Q1 directly to the gate of the Q1 FET ensures fast turn-OFF without any impact of R_1 and C_1 components.

C_1 results in an additional loading on C_{BST} to charge during turn-ON. Use below equation to calculate the required C_{BST} value:

$$C_{BST} = \frac{Q_{g(total)}}{\Delta V_{BST}} + 10 \times C_1 \quad (4)$$

Where,

$Q_{g(total)}$ is the total gate charge of the FET,

ΔV_{BST} (1V typical) is the ripple voltage across BST to SRC pins.

7.3.3 Short-Circuit Protection

The TPS48100-Q1 feature adjustable short circuit protection. The threshold and response time can be adjusted using R_{ISCP} resistor and C_{TMR} capacitor respectively. The device senses the voltage across CS+ and CS– pins.

These pins can be connected across an external high and low side current sense resistor (R_{SNS}) or across the FET drain and source terminals for FET RDSON sensing as shown in 図 7-5, 図 7-6 and 図 7-7 respectively.

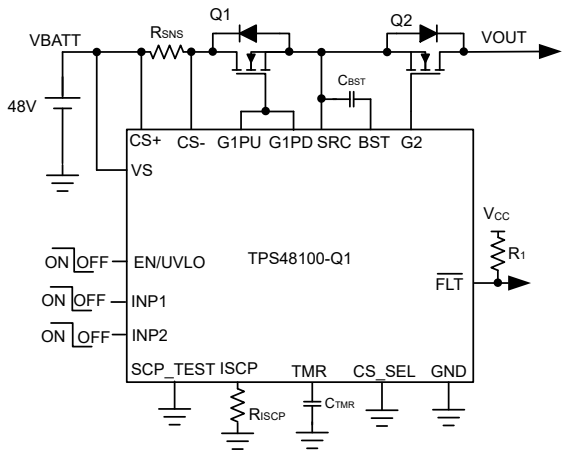

図 7-5. TPS48100-Q1 Application Circuit With External Sense Resistor RSNS Based High Side Current Sensing

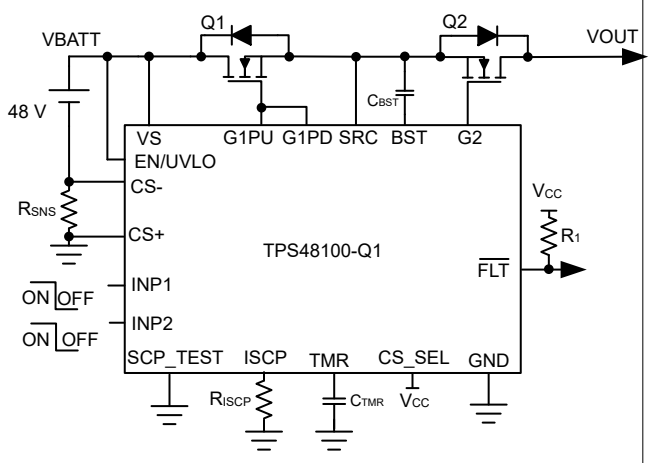

図 7-6. TPS48100-Q1 Application Circuit With External Sense Resistor RSNS Based Low Side Current Sensing

ADVANCE INFORMATION

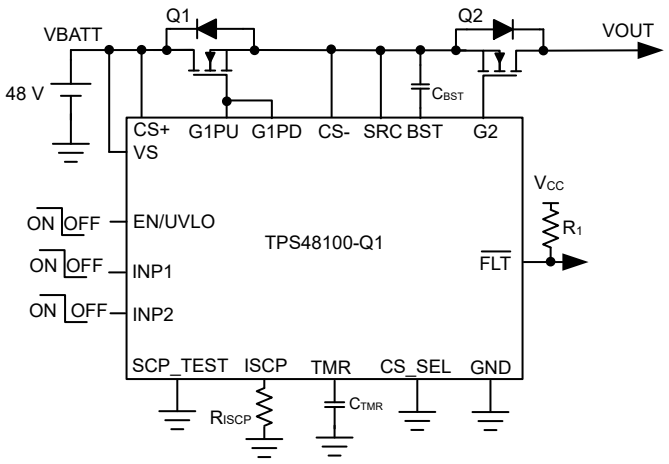

図 7-7. TPS48100-Q1 Application Circuit with MOSFET RDSON Based Current Sensing

Set the short-circuit detection threshold using an external R_{ISCP} resistor across ISCP and GND pins. Use 式 5 to calculate the required R_{ISCP} value:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 10\ mV\right)}{2\ \mu A} \quad (5)$$

Refer to 式 9 in Application Limitations section for update in equation in final revision of IC.

Where,

R_{SNS} is the current sense resistor value or the FET R_{DSON} value.

I_{SC} is the desired short circuit current level.

The short circuit protection response is fastest with no C_{TMR} cap connected across TMR and GND pins.

With device powered ON and EN/UVLO, INP pulled high, During Q1 turn ON, first VGS of external FET Q1 (G1 gate drive) is sensed by monitoring the voltage across G1PD to SRC. Once G1PD to SRC voltage raises above $V_{(G1\_GOOD)}$ threshold which ensures that the external FET is enhanced, then the SCP comparator output is monitored. If the sensed voltage across CS+ and CS– exceeds the short-circuit set point (V_{SCP}), G1PD pulls low to SRC and $\overline{FLT}$ asserts. Subsequent events can be set either to be auto-retry or latch off as described in following sections.

VGS of external FET (Q1) is only monitored when CS_SEL is pulled low. VGS of external FET (Q1) is not monitored for low side current sensing as shown in 図 7-6.

7.3.3.1 Short-Circuit Protection With Auto-Retry

The C_{TMR} programs the short-circuit protection delay (t_{SC}) and auto-retry time (t_{RETRY}). Once the voltage across CS+ and CS– exceeds the set point, the C_{TMR} starts charging with 80µA pull-up current.

After C_{TMR} charges to $V_{(TMR\_SC)}$, G1PD pulls low to SRC and $\overline{FLT}$ asserts low providing warning on impending FET turn OFF. Post this event, the auto-retry behavior starts. The C_{TMR} capacitor starts discharging with 2.5µA pulldown current. After the voltage reaches $V_{(TMR\_LOW)}$ level, the capacitor starts charging with 2.2µA pullup. After 32 charging-discharging cycles of C_{TMR} the FET turns ON back and $\overline{FLT}$ de-asserts.

The device retry time (t_{RETRY}) is based on C_{TMR} for the first time as per 式 7 .

Use 式 6 to calculate the C_{TMR} capacitor to be connected across TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{SC}}{1.1} \quad (6)$$

Where,

I_{TMR} is internal pull-up current of 80µA.

t_{SC} is desired short-circuit response time.

The fastest t_{SC} is with no C_{TMR} cap connected.

$$t_{RETRY} = 22.7 \times 10^6 \times C_{TMR} \quad (7)$$

If the short-circuit pulse duration is below t_{SC} then the FET remains ON and C_{TMR} gets discharged using internal pull down switch.

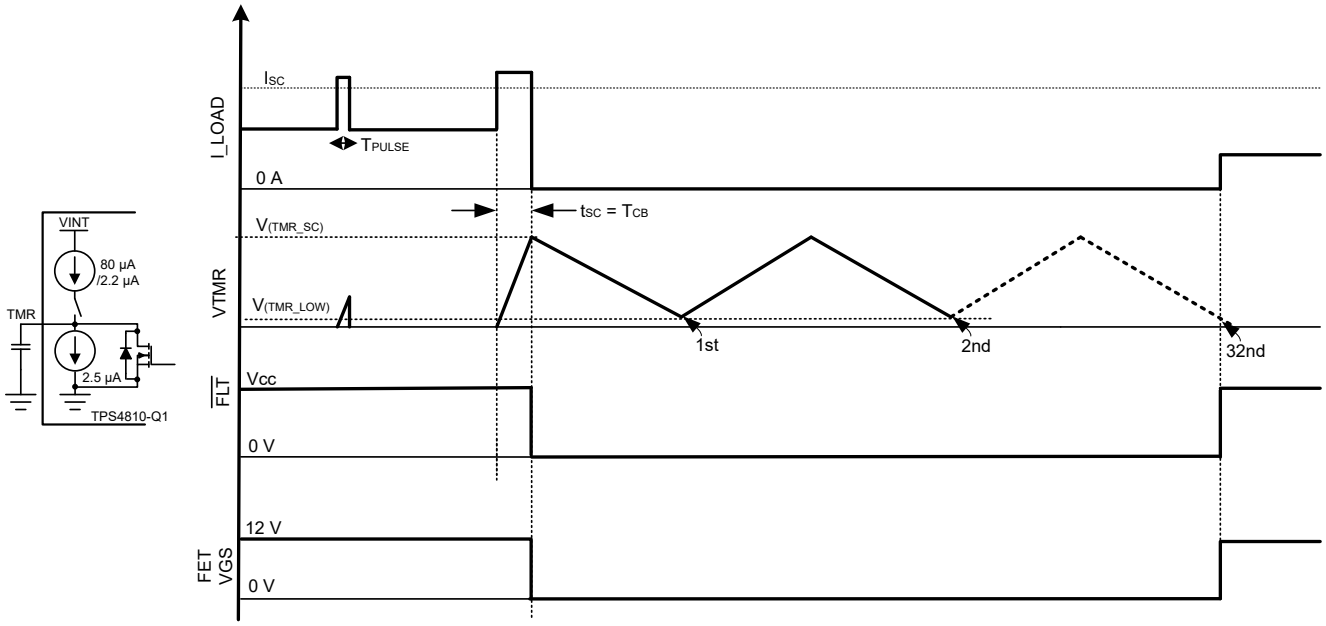

図 7-8. Short-Circuit Protection With Auto-Retry

7.3.3.2 Short-Circuit Protection With Latch-Off

Connect an approximately 100kΩ resistor across C_{TMR} as shown in 図 7-9. With this resistor, during the charging cycle, the voltage across C_{TMR} gets clamped to a level below $V_{(TMR\_SC)}$ resulting in a latch-off behavior and $\overline{FLT}$ asserts low at same time.

Use 式 8 to calculate C_{TMR} capacitor to be connected between TMR and GND for R_{TMR} = 100kΩ.

$$C_{TMR} = \frac{t_{SC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.1}{R_{TMR} \times 80\ \mu A}}\right)} \quad (8)$$

Where,

I_{TMR} is internal pull-up current of 80µA.

t_{SC} is desired short-circuit response time.

Toggle INP1 or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS\_PORF)}$ to reset the latch. At low edge, the timer counter is reset and C_{TMR} is discharged. G1PU pulls up to BST when INP1 is pulled high.

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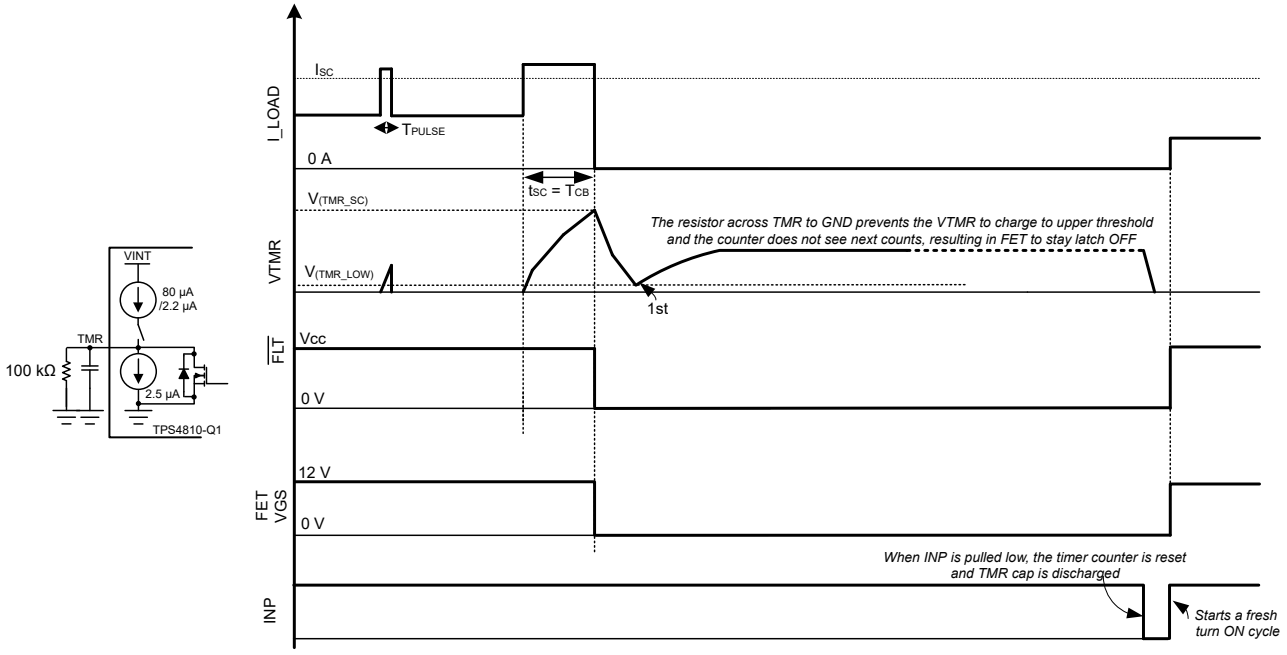

図 7-9. Short-Circuit Protection With Latch-Off

7.3.4 Undervoltage Protection (UVLO)

TPS48100-Q1 has an accurate undervoltage protection (< ±2%) using EN/UVLO pin providing robust protection. Connect a resistor ladder as shown in 図 7-10 for undervoltage protection threshold programming.

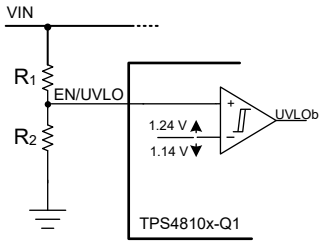

図 7-10. Programming Undervoltage Protection

7.3.5 Reverse Polarity Protection

The TPS48100-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults occur during installation and maintenance of the end equipment. The device is tolerant to reverse polarity voltages down to –65V both on input and on the output.

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems the output negative voltage level is limited by the output side TVS or a diode.

7.3.6 Short-Circuit Protection Diagnosis (SCP_TEST)

In the safety critical designs, short-circuit protection (SCP) feature and its diagnosis is important.

The TPS48100-Q1 features the diagnosis of the internal short circuit protection. When SCP_TEST is driven low to high then, a voltage is applied internally across the SCP comparator inputs to simulate a short circuit event.

The comparator output controls the gate drive (G1PU/G1PD) and also the $\overline{FLT}$. If the gate drive goes low (with initially being high) and $\overline{FLT}$ also goes low then it indicates that the SCP is good otherwise it is to be treated as SCP feature is not functional.

If the SCP_TEST feature is not used, then connect SCP_TEST pin to GND.

7.3.7 TPS48100-Q1 as a Simple Gate Driver

図 7-11 shows application schematics of TPS48100-Q1 as a simple gate driver in load connect-disconnect switch driving back-to-back FETs topology. The short-ciruit protection feature is disabled.

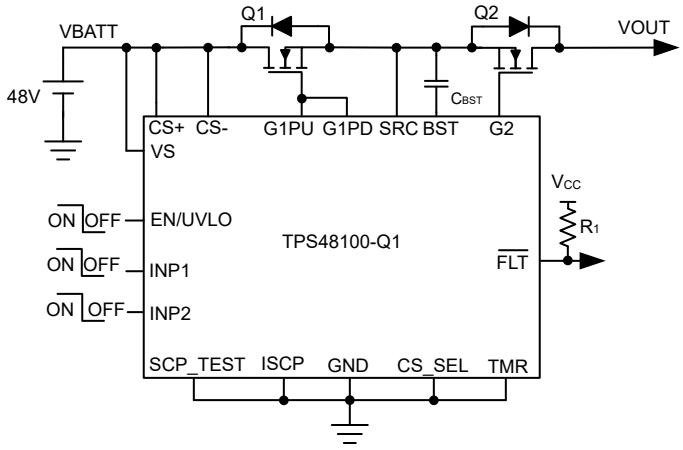

図 7-11. TPS48100-Q1 Application Circuit for Simple Gate Driver

7.4 Device Functional Modes

The TPS48100-Q1 has two modes of operation. Active mode and low IQ shutdown mode.

If the EN/UVLO pin voltage is greater than $V_{(ENR)}$ rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers, all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled below $V_{(ENF)}$ falling threshold, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The gate drive and external FETs turn OFF. The TPS48100-Q1 consumes low IQ of 1.5µA (typical) in this mode.

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8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPS48100-Q1 is a 100V, low IQ, smart high side driver with protection and diagnostics. The TPS48100-Q1 device architecture is design to drive and control back-to-back N-Channel MOSFETs independently in common source configuration with separate control inputs (INP1, INP2), which makes TPS48100-Q1 a competitive choice to realize circuit breaker in battery management system (BMS). The strong (2A) GATE drivers enable switching parallel MOSFETs in high current applications, such as circuit breaker in powertrain (DC/DC converter), driving loads in power distribution unit, circuit breaker in 12V, 48V BMS, and so forth.

The TPS48100-Q1 device provides configurable short-circuit protection using ISCP and TMR pins for adjusting the threshold and response time, respectively. Auto-retry and latch-off fault behavior can be configured. By using CS+ and CS– pins, current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. The device also features diagnosis of the internal short-circuit comparator using external control on SCP_TEST input.

The following design procedure can be used to select the supporting component values based on the application requirement.

8.1.1 Application Limitations

8.1.1.1 Short-Circuit Protection Delay

In application designs with high side current sense configurations as shown in 図 7-5 and 図 7-7 with C_{TMR} = Open, the short-circuit protection delay during power up with output short circuited does not match the specified maximum value of 10µs.

Testing has shown that the actual short-circuit protection delay during power up by EN/UVLO signal is approximately 70µs. This increase in protection delay still allows for the TPS48100-Q1 to operate as designed, but results in larger power dissipation in the external MOSFET during output short-circuit scenario.

A design fix must be included in the final version of the IC.

8.1.1.2 Short-Circuit Protection Threshold

The minimum short-circuit protection threshold is limited to 30mV.

A design update is planned in the final revision of the IC to extend the minimum threshold down to 20mV. Due to the design update there will be a change of R_{ISCP} resistor formula and the revised formula will be as per the 式 9:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 19\ mV\right)}{2\ \mu A} \tag{9}$$

Lowest SCP threshold setting will be limited to 20mV.

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8.2 Typical Application: Circuit Breaker in Battery Management System (BMS) using Low Side Current Sense

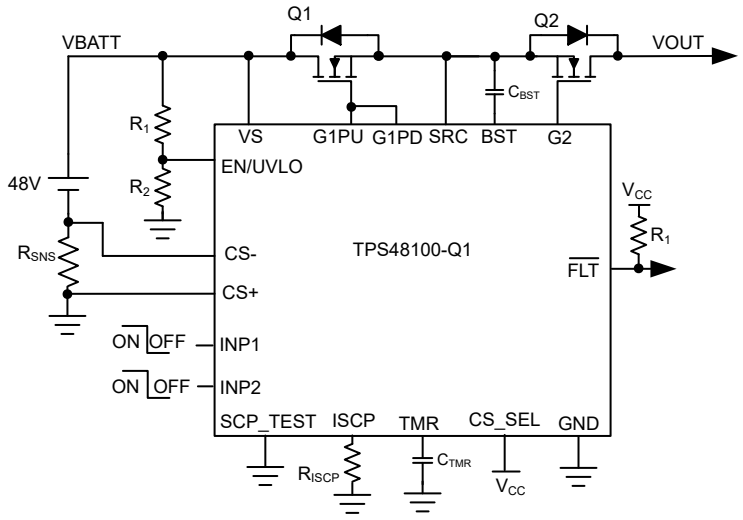

図 8-1. Typical Application Schematic: BMS Circuit Breaker With Low Side Current Sense

8.2.1 Design Requirements

The following table shows the design parameters for this application example.

表 8-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{IN}	48V
Undervoltage lockout set point, VIN_{UVLO}	24V
Maximum load current, I_{OUT}	25A
Short-circuit protection threshold, I_{SC}	40A
Short-circuit protection delay (t_{SC})	1ms
Fault response	Auto-retry
Current sensing	Low-side

8.2.2 Detailed Design Procedure

Selection of Current Sense Resistor, R_{SNS}

The recommended range of the overcurrent protection threshold voltage, $V_{(SCP)}$, extends from 30mV to 300mV. Values near the low threshold of 30mV can be affected by the system noise. Values near the upper threshold of 300mV can cause high power dissipation in the current sense resistor. To minimize both the concerns, 40mV is selected as the short-circuit protection threshold voltage. Use the following equation to calculate the current sense resistor, R_{SNS}.

$$R_{SNS} = \frac{V_{(SCP)}}{I_{SC}} \quad (10)$$

The next smaller available sense resistor 1mΩ, 1% is chosen.

To improve signal to noise ratio or for better short-circuit protection accuracy, higher short-circuit protection threshold voltage, $V_{(SCP)}$ can be selected.

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Programming the Short-Circuit Protection Threshold – R_{ISCP} Selection

The R_{ISCP} sets the short-circuit protection threshold. Use the following equation to calculate the value.

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{SNS} - 10\ mV\right)}{2\ \mu A} \quad (11)$$

To set 30A as short-circuit protection threshold, R_{ISCP} value is calculated to be 15kΩ.

Choose the closest available standard value: 15kΩ, 1%.

Refer to 式 9 in セクション 8.1.1 for updated equation in final revision of IC.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components cannot be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

Programming the Short-Circuit Protection Delay – C_{TMR} Selection

For the design example under discussion, overcurrent transients are allowed for 1ms duration. This short-circuit protection delay, t_{SC} can be set by selecting appropriate capacitor C_{TMR} from TMR pin to ground. Use the following equation to calculate the value of C_{TMR} to set 1ms for t_{SC}.

$$C_{TMR} = \frac{80\ \mu \times t_{SC}}{1.1} = 72.72\ nF \quad (12)$$

Choose closest available standard value: 82nF, 10%.

Selection of MOSFETs, Q_1 and Q_2

For selecting the MOSFET Q_1 and Q_2 important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON-resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 60V as the maximum application voltage, MOSFETs with V_{DS} voltage rating of 80V is designed for this application.

The maximum V_{GS} TPS4810-Q1 can drive is 13V, so a MOSFET with 15V minimum V_{GS} rating must be selected.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred.

Based on the design requirements, IAUS200N08S5N023 is selected and the ratings are:

- 80V $V_{DS(MAX)}$ and 20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 2.3mΩ typical at 10V V_{GS}
- Maximum MOSFET $Q_{g(total)}$ is 110nC

Selection of Bootstrap Capacitor, C_{BST}

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 345µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving two IAUS200N08S5N023 MOSFETs.

$$C_{BST} = \frac{Q_{g(total)}}{1\,V} = 220\,nF \quad (13)$$

Choose closest available standard value: 220nF, 10%.

Setting the Undervoltage Lockout

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider network of R_1 and R_2 connected between VS, EN/UVLO and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving 式 14.

$$V_{(UVLOR)} = \frac{R_2}{(R_1 + R_2)} \times VIN_{UVLO} \quad (14)$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for R_1 and R_2. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{12})$ must be chosen to be 20 times greater than the leakage current of UVLO pin.

From the device electrical specifications, $V_{(UVLOR)}$ = 1.24V. From the design requirements, VIN_{UVLO} is 6.5V. To solve the equation, first choose the value of R_1 = 470kΩ and use 式 14 to solve for R_2 = 24.9kΩ. Choose the closest standard 1% resistor values: R_1 = 470kΩ, and R_2 = 24.9kΩ.

8.2.3 Application Curves

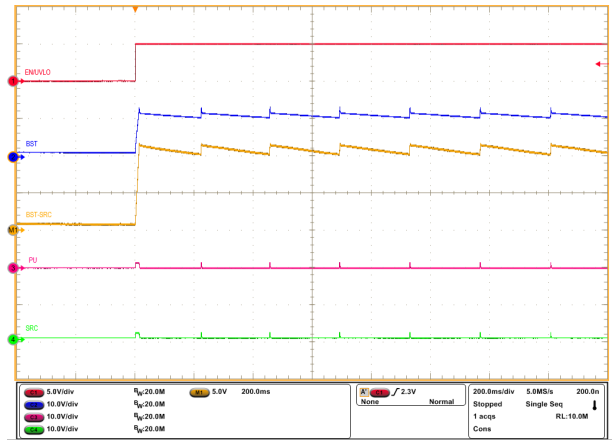

図 8-2. Start-Up Profile of Bootstrap Voltage With INP1 = INP2 = GND and C_{BST} = 470nF

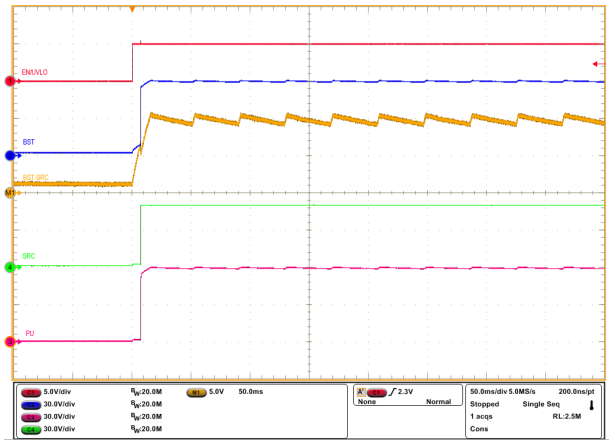

図 8-3. Start-Up Profile of Bootstrap Voltage With INP1 = INP2 = HIGH and C_{BST} = 470nF

ADVANCE INFORMATION

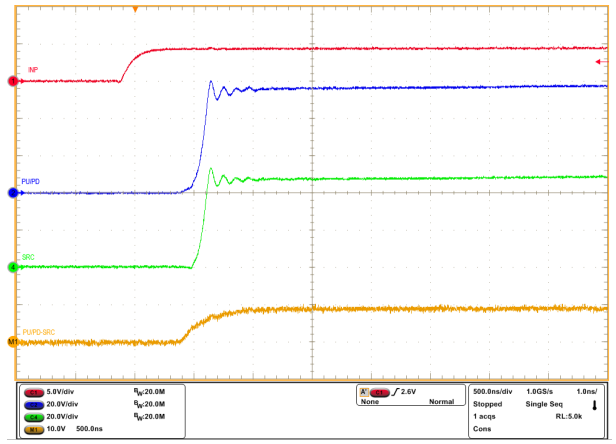

図 8-4. Turn-ON Response of TPS48100-Q1 for INP1 -> LOW to HIGH and C_{BST} = 470nF

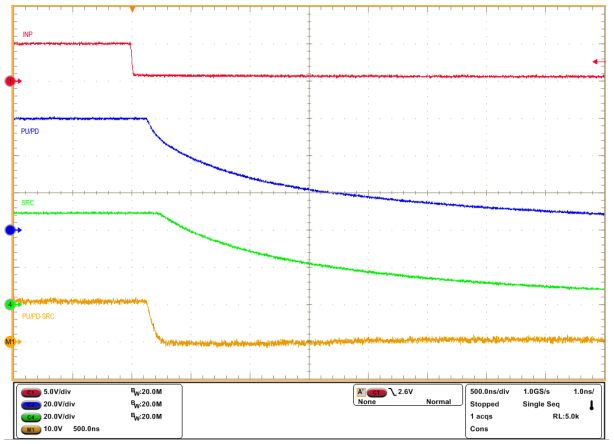

図 8-5. Turn-OFF Response of TPS48100-Q1 for INP1 -> HIGH to LOW and C_{BST} = 470nF

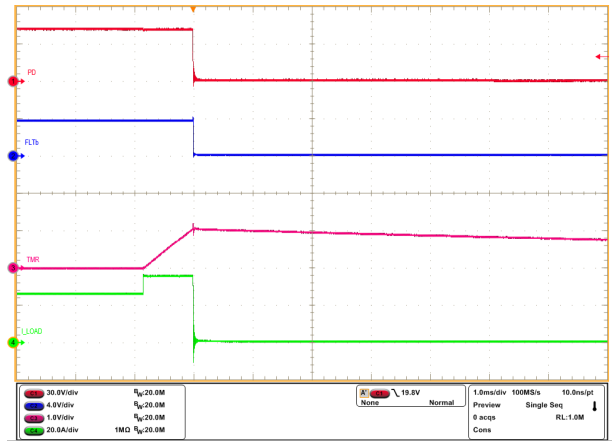

図 8-6. Overcurrent Response of TPS48100-Q1 for a Load Step From 25A to 35A With 30A Overcurrent Protection Setting

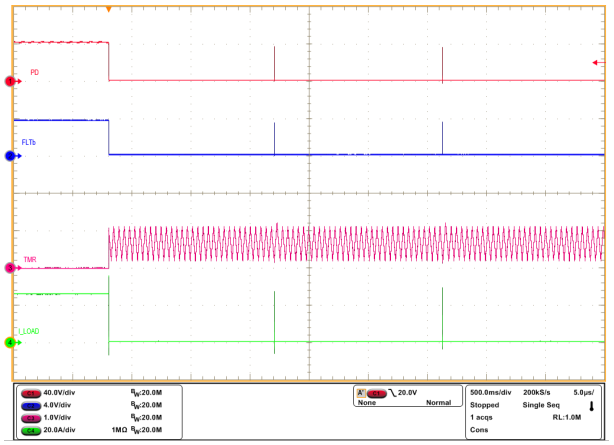

図 8-7. Auto-Retry Response of TPS48100-Q1 for an Overcurrent Fault

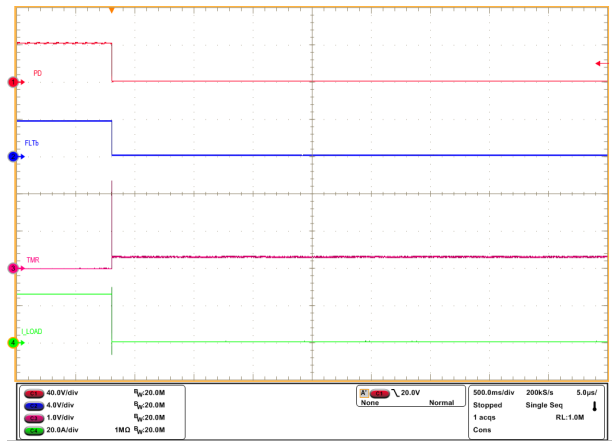

図 8-8. Latch-Off Response of TPS48100-Q1 for an Overcurrent Fault

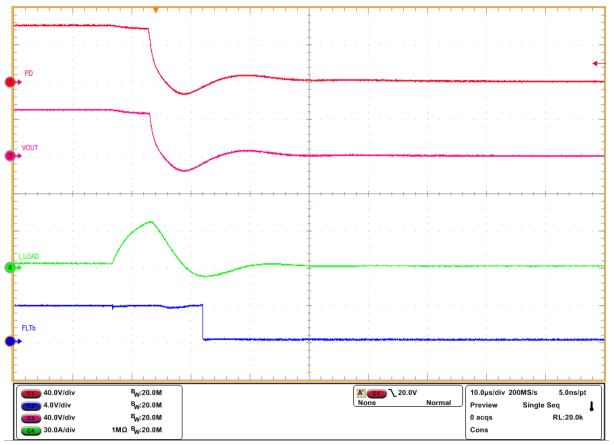

図 8-9. Output Short-Circuit Response of TPS48100-Q1 Device

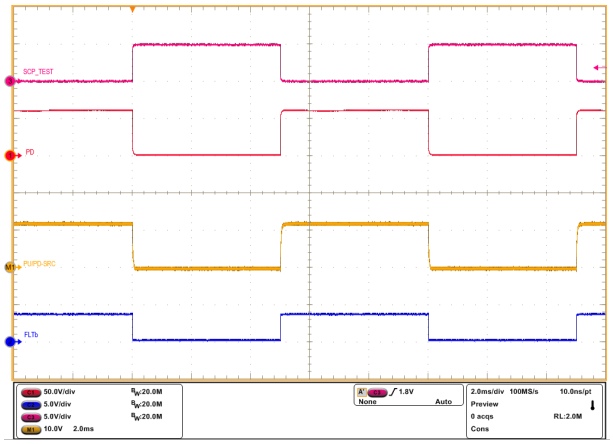

図 8-10. Short-Circuit Protection Diagnosis Test Response of TPS48100-Q1

8.3 Power Supply Recommendations

When the external MOSFETs turn-OFF during the conditions such as INP1 control, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS4810-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to specified operation. If the input power supply source is noisy with transients, then TI recommends to place a R_{VS} – C_{VS} filter between the input supply line and VS pin to filter out the supply noise. TI recommends R_{VS} value around 100Ω.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor (R_{SNS}) and tweak the values during test in the real system. The RC filter components must not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

The following figure shows the circuit implementation with optional protection components.

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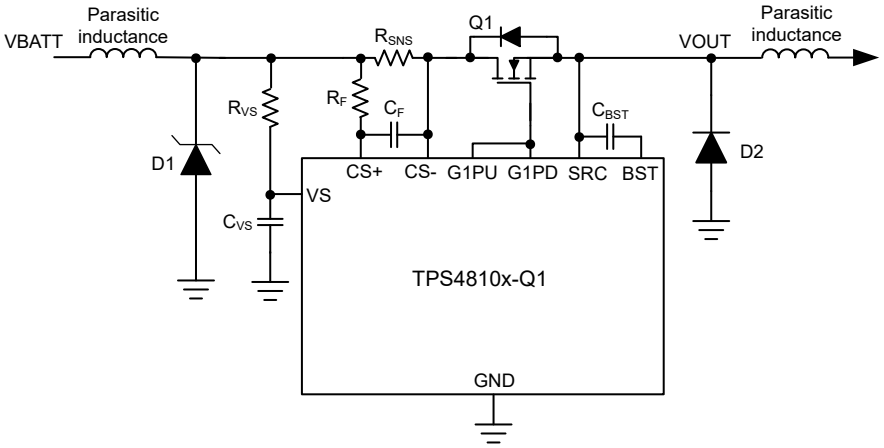

図 8-11. Circuit Implementation With Optional Protection Components For TPS4810-Q1

8.4 Layout

8.4.1 Layout Guidelines

- Place the sense resistor (R_{SNS}) close to the TPS4810x-Q1 and then connect R_{SNS} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- Choose a 0.1µF or higher value ceramic decoupling capacitor between VS terminal and GND for all the applications. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- Make the high-current path from the board input to the load, and the return path, parallel and close to each other to minimize loop inductance.
- Place the external MOSFETs close to the controller GATE drive pins (G1PU/PD and G2) such that the GATE of the MOSFETs are close to the controller GATE drive pins and forms a shorter GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- Place the external boot-strap capacitor close to BST and SRC pins to form very short loop.
- Connect the ground connections for the various components around the TPS4810x-Q1 directly to each other, and to the TPS4810x-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

ADVANCE INFORMATION

8.4.2 Layout Example

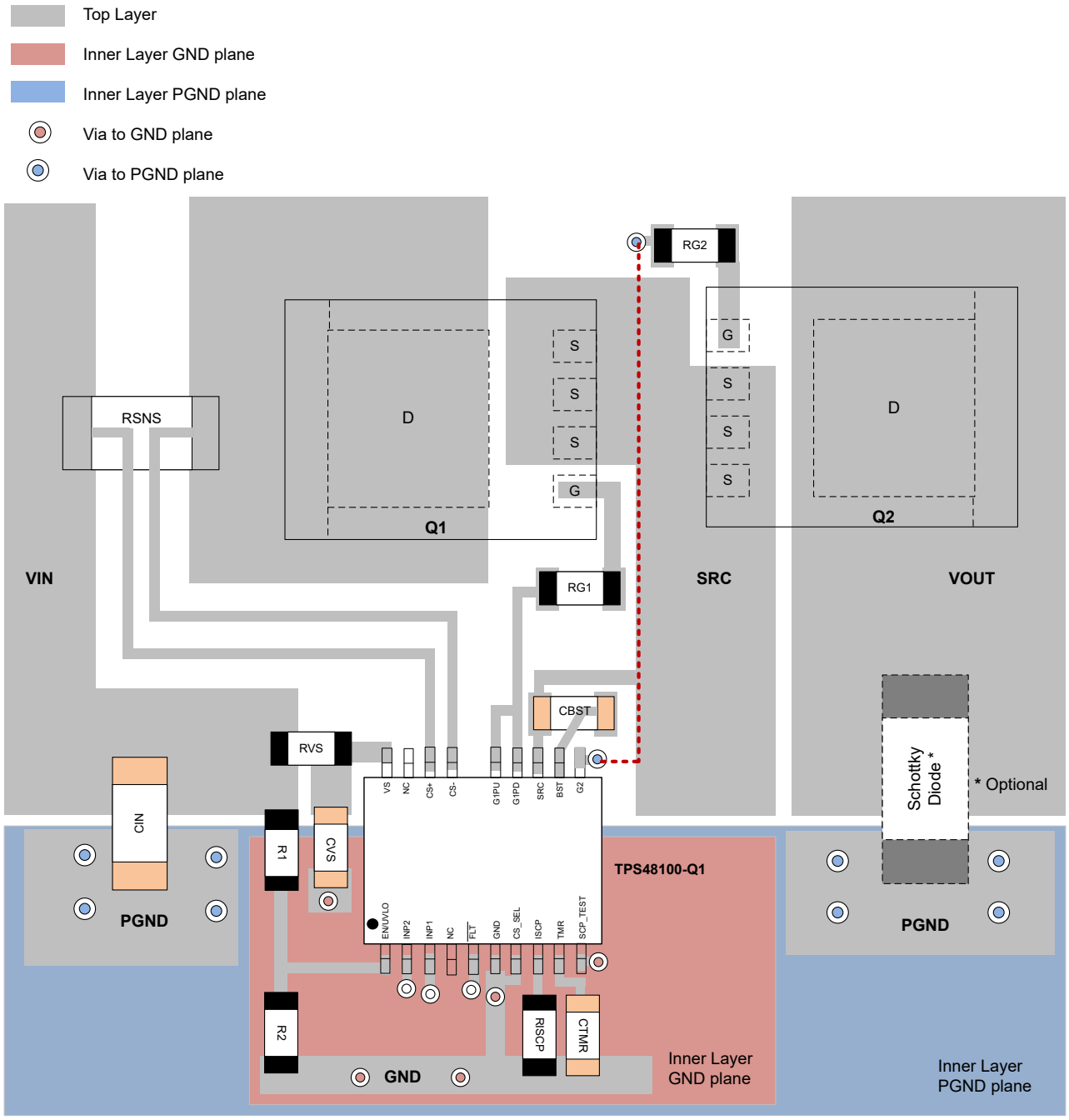

図 8-12. Typical PCB Layout Example for TPS4810-Q1 With B2B MOSFETs

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.3 Trademarks

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9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS48100QDGXRQ1	ACTIVE	VSSOP	DGX	19	5000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

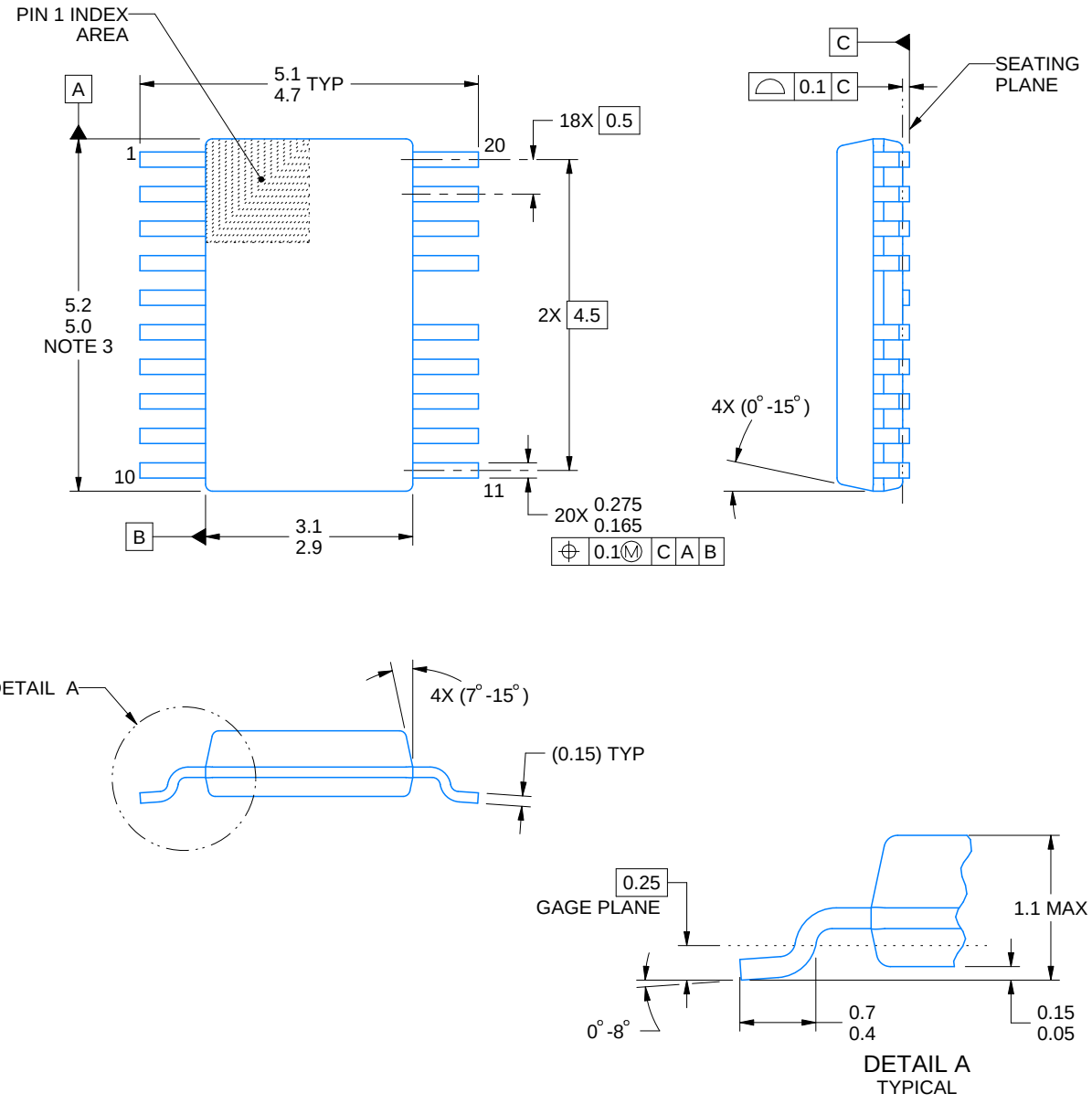
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGX0019A

VSSOP - 1.1 mm max height

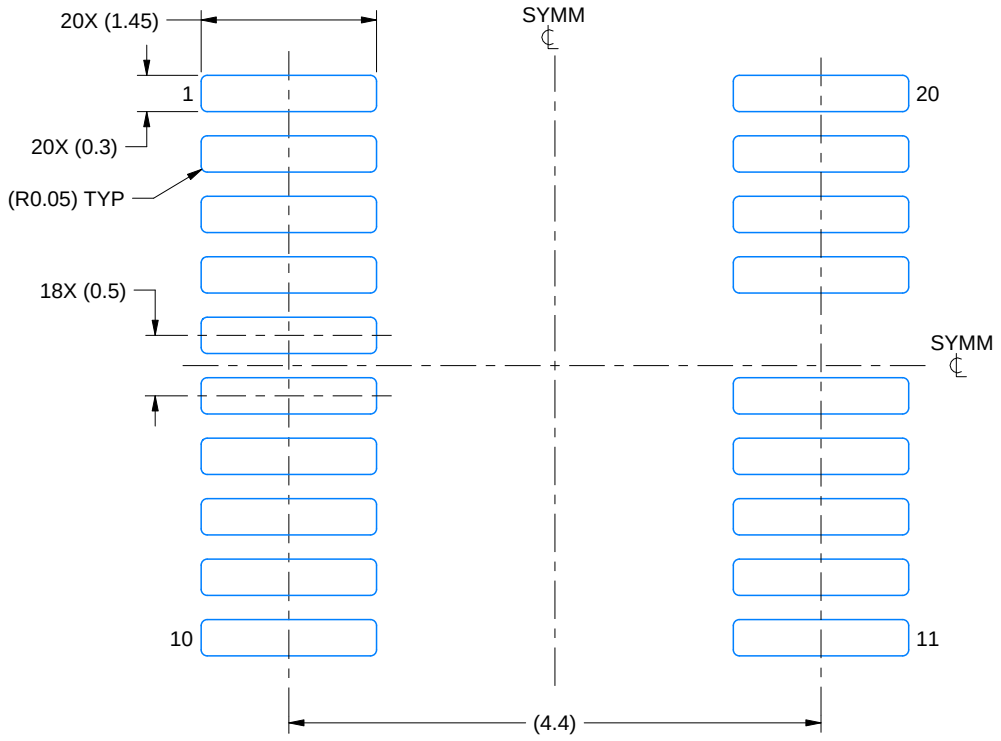
SMALL OUTLINE PACKAGE



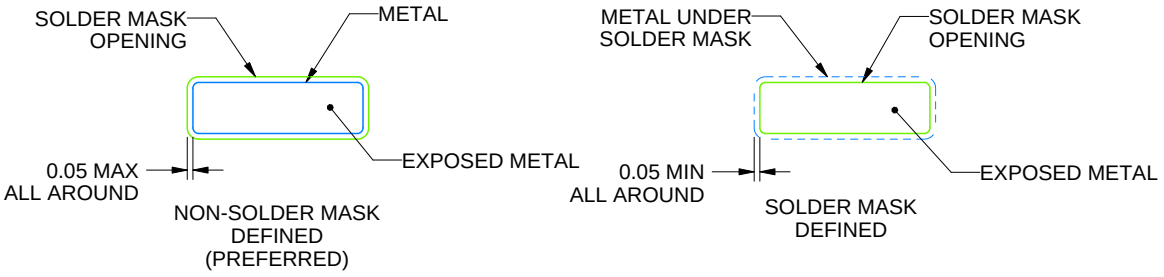
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

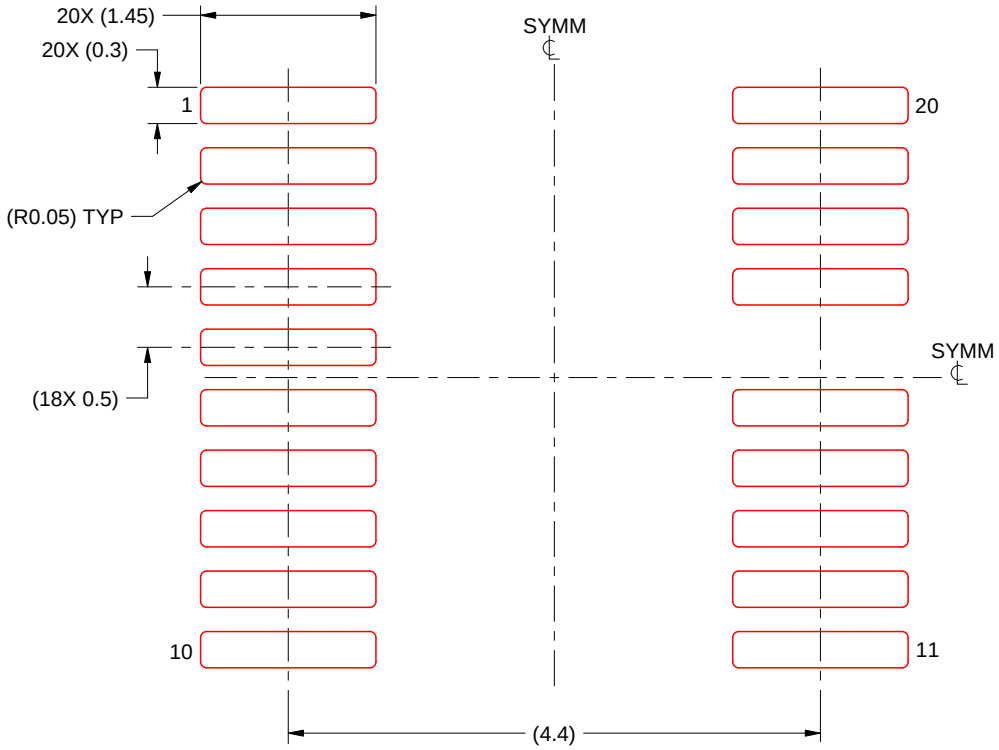


SOLDER MASK DETAILS

4226944/A 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226944/A 07/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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