TEXAS INSTRUMENTS
TPS51383, TPS51384
JAJSK76 – SEPTEMBER 2022

TPS51383 および TPS51384 100mA LDO を搭載した 4.5V～24V 入力、8A の同期整流降圧コンバータ

1 特長

- 4.5V～24V の入力電圧範囲
- 3.36V の出力電圧 (TPS51383)
- スイッチ・オーバー機能付きの 3.3V、100mA LDO (TPS51383)
- 1.82V の出力電圧 (TPS51384)
- スイッチ・オーバー機能付きの 1.8V、100mA LDO (TPS51384)
- 22mΩ および 11mΩ の MOSFET を内蔵
- 8A の連続 I_{OUT} をサポート
- 低い静止電流：80µA
- 25℃で ±1% のリファレンス電圧精度
- -40℃～125℃で ±1.5% のリファレンス電圧精度
- D-CAP3™ 制御モードによる高速過渡応答
- POSCAP およびすべての MLCC 出力コンデンサをサポート
- 出力放電機能
- 軽負荷時に PSM モードと OOA モードを選択可能
- パワー・グッド・インジケータにより出力電圧を監視
- ラッチ付きの出力 OV および UV 保護
- ラッチなしの UVLO および OT 保護
- サイクル単位の過電流保護
- 出力放電機能を内蔵
- 小型の 2.00mm × 3.00mm HotRod™ QFN パッケージ

2 アプリケーション

- ノート PC およびデスクトップ PC
- ウルトラブック、タブレット
- TV および STB、ポイント・オブ・ロード (POL)
- 分散電源システム

3 概要

TPS51383 および TPS51384 はモノリシックな 8A 同期整流降圧コンバータで、適応型オン時間 D-CAP3 制御モードが搭載されています。低 $R_{DS(on)}$ のパワー MOSFET を内蔵して高効率を実現しており、必要な外付け部品数が最小限なので、容積の制約が厳しい電力システムでも簡単に使えます。特長として、高精度のリファレンス電圧、高速な負荷過渡応答、軽負荷効率を実現する自動スキップ・モード動作、25kHz を超えるスイッチング周波数を使用する OOA 軽負荷動作、良好なラインおよび負荷レギュレーションを実現する D-CAP3 制御モードがあり、外部補償は不要です。

TPS51383 は、3.36V 固定、$8A_{MAX}$ の出力と、スイッチ・オーバー機能を備えた 3.3V、$100mA_{MAX}$ の LDO 出力を提供します。TPS51384 は、1.82V 固定、$8A_{MAX}$ の出力と、スイッチ・オーバー機能を備えた 1.8V、$100mA_{MAX}$ の LDO 出力を提供します。TPS51383 と TPS51384 はどちらも超低静止電流機能を備えているため、システムのスタンバイ・モードでバッテリ寿命を延長できます。

TPS5138x は放熱特性の優れた 12 ピン QFN パッケージで供給され、-40℃～125℃の接合部温度で動作するよう設計されています。

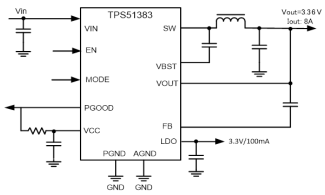
パッケージ情報

型番	パッケージ(1)	本体サイズ (公称)
TPS51383	RJN (VQFN-HR、12)	2.00mm × 3.00mm
TPS51384		

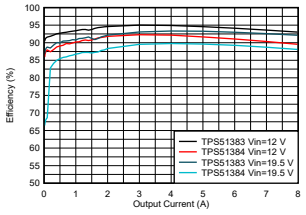
(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

製品情報

型番	固定出力	LDO OUTPUT
TPS51383	3.36V	3.3V
TPS51384	1.82V	1.8V



TPS51383 の代表的なアプリケーション



TPS51383 の効率曲線

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4 Revision History

DATE	REVISION	NOTES
September 2022	*	Initial release

5 Pin Configuration and Functions

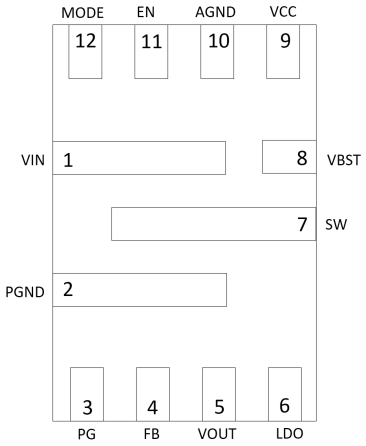


図 5-1. RJN Package 12-Pin VQFN-HR Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
PGND	2	G	Power ground terminal for the internal power FET.
PG	3	O	Open Drain Power Good Indicator. This pin is asserted low if output voltage is out of PG threshold, overvoltage or if the device is under thermal shutdown, EN shutdown or during soft start.
FB	4	I	FB pin can be used for feedforward compensation to improve load transient performance.
VOUT	5	I	Output voltage sense pin of buck converter. Connect this pin to the positive terminal of the output capacitor that is closest to the load.
LDO	6	O	100-mA LDO output pin for powering external devices even when EN is low (but Vin is >UVLO). Decouple with a minimum 4.7-uF, 10-V X7R capacitor.
SW	7	O	Switch node terminal. Connect the output inductor to this pin.
VBST	8	I	Supply input for the high-side MOSFET gate drive. Connect the bootstrap capacitor between VBST and SW.
VCC	9	O	5-V internal VCC LDO output. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 1-µF capacitor.
AGND	10	G	Ground of internal analog circuitry. Connect AGND to PGND at a single point close to AGND.
EN	11	I	Enable pin of buck converter. EN pin is a digital input pin, pull up to enable the converter, pull down to disable. Internal pulldown if EN pin is floating.
MODE	12	I	Mode selection pin. Connect MODE pin to VCC, or pull above 0.8 V for OOA mode operation, connect MODE to AGND or float for Power Save Mode. Internal pulldown if MODE pin is floating.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	28	V
Input voltage	VBST	-0.3	34	V
Input voltage	VBST - SW	–0.3	6	V
Input voltage	EN, FB, MODE, VOUT	–0.3	6	V
Output voltage	SW (10ns transient)	–4	28	V
Output voltage	SW	–1.0	28	V
Output voltage	PG, LDO	–0.3	6	V
Output voltage	VCC	0	6	V
Voltage	PGND,AGND	–0.3	0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	VIN	4.5		24	V
Input voltage range	VBST	-0.1		29.5	V
Input voltage range	VBST – SW	–0.1		5.5	V
Input voltage range	EN, FB, MODE, VOUT	–0.3		5.5	V
Output voltage range	SW	-1.0		24	V
Output voltage range	PG, VCC, LDO	–0.1		5.5	V
Output current range	I_{OUT}			8	A
LDO output current	LDO (V_{VIN} ≥ 5.2 V)			100	mA
T_J		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE		UNIT
		RJNR (QFN, JEDEC)	RJNR (QFN, TI EVM)	
		12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.7	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.1	Not Applicable (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.7	Not Applicable (2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	3.7	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC(1)		DEVICE		UNIT
		RJNR (QFN, JEDEC)	RJNR (QFN, TI EVM)	
		12 PINS	12 PINS	
ψ_{JB}	Junction-to-board characterization parameter	18.4	18.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal simulation setup is not applicable to a TI EVM layout.

6.5 Electrical Characteristics

MODE connected to AGND, V_{EN} = 3.3V; T_J = –40°C to +125°C, Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)						
VIN	Input voltage range	VIN	4.5		24	V
I_{VIN}	VIN Supply Current (Quiescent)	V_{VIN} = 12 V, No load, V_{EN} = 3.3 V, non-switching		80		µA
I_{INSDN}	VIN Shutdown Current	V_{VIN} = 12 V, No load, V_{EN} = 0 V, PG open		55		µA
UVLO						
$V_{VCC\ UVLO\_R}$	V_{CC} Under-Voltage Lockout	V_{VCC} rising		4.2	4.42	V
$V_{VCC\ UVLO\_F}$	V_{CC} Under-Voltage Lockout	V_{VCC} falling	3.65	3.85		V
$V_{VCC\ UVLO\_H}$	V_{CC} Under-Voltage Lockout	Hysteresis V_{CC} voltage		450	650	mV
ENABLE (EN), MODE						
V_{EN_R}	EN Threshold High-level	V_{EN} rising		1.31	1.5	V
V_{EN_F}	EN Threshold Low-level	V_{EN} falling	1.0	1.13		V
V_{EN_H}	EN Threshold Low-level	Hysteresis		180		mV
I_{EN}	EN Pull down Current	V_{EN} = 0.8 V	1.3	2.3		uA
$V_{IL;MODE}$	Low-Level Input Voltage at MODE Pin		0.4			V
$V_{IH;MODE}$	High-Level Input Voltage at MODE Pin				0.8	V
I_{MODE}	MODE Pull down Current	V_{MODE} = 0.8 V	1.3	2.3	3.5	uA
VCC						
V_{VCC}	VCC Output Voltage	V_{VIN} > 5.2 V, I_{VCC} ≤ 1 mA	4.85	5	5.15	V
OUTPUT VOLTAGE (VOUT)						
V_{VOUT}	VOUT voltage (TPS51384)	T_J=25°C	1.802	1.82	1.838	V
	VOUT Voltage (TPS51384)	-40 °C ≤ T_J ≤125°C	1.793	1.82	1.847	V
V_{VOUT}	VOUT Voltage (TPS51383)	T_J=25°C	3.326	3.36	3.394	V
	VOUT Voltage (TPS51383)	-40 °C ≤ T_J ≤125°C	3.30	3.36	3.42	V
DUTY CYCLE and FREQUENCY CONTROL						
f_{SW}	Switching frequency	CCM operation	480	600	720	kHz
$t_{ON(min)}$	Minimum ON pulse width	T_J = 25°C		65	75	ns
$t_{OFF(min)}$	Minimum OFF pulse width	T_J = 25°C			190	ns
t_{OOA}	OOA operation period	V_{MODE} = V_{VCC}		30	50	µs
SOFT-START						
t_{SS}	Internal fixed softstart		0.55	1	1.35	ms
POWER SWITCHES (SW)						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C		22		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C		11		mΩ
BOOT CIRCUIT						
CURRENT LIMIT						
I_{OCL}	Low-side valley current limit	Valley current limit on LS FET	9.5	11	12.5	A
I_{NOCL}	Low-side negative current limit	Sinking current limit on LS FET		3.9		A

6.5 Electrical Characteristics (continued)

MODE connected to AGND, V_{EN} = 3.3V; T_J = –40°C to +125°C, Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP Trip Threshold		117	120	123	%
t_{OVPDLY}	OVP Prop deglitch			20		µs
t_{OVPDLY}	OVP latch-off Prop deglitch			256		µs
V_{UVP}	UVP Trip Threshold		55	60	65	%
t_{UVPDLY}	UVP Prop deglitch			256		µs
POWER GOOD (PG)						
t_{PGDLY}	PG Start-Up delay	PG from low to high		500		µs
t_{PGDLY}	PG delay time when V_{FB} rising (fault)	PG from high to low		20		µs
t_{PGDLY}	PG delay time when V_{FB} falling (fault)	PG from high to low		28		µs
V_{PGTH}	PG Threshold when V_{FB} falling (fault)	V_{FB} falling (fault), percentage of V_{FB}	79	85	89	%
V_{PGTH}	PG Threshold when V_{FB} rising (good)	V_{FB} rising (good), percentage of V_{FB}	86	90	94	%
V_{PGTH}	PG Threshold when V_{FB} rising (fault)	V_{FB} rising (fault), percentage of V_{FB}	116	120	124	%
V_{PGTH}	PG Threshold when V_{FB} falling (good)	V_{FB} falling (good), percentage of V_{FB}	109	115	119	%
I_{PGMAX}	PG Sink Current	V_{PG} = 0.5 V		50		mA
I_{PGLK}	PG Leak Current	V_{PG} = 5.5 V			1	µA
OUTPUT DISCHARGE						
R_{DIS}	Discharge resistance	T_J = 25°C, V_{EN} = 0 V		160		Ω
SWITCH-OVER LDO OUTPUT (LDO)						
V_{LDO}	LDO output voltage (TPS51383)	V_{EN} = 0 V, V_{IN} ≥ 4.5 V	3.24	3.3	3.36	V
V_{LDO}	LDO output voltage (TPS51384)	V_{EN} = 0 V, V_{IN} ≥ 4.5 V	1.773	1.8	1.827	V
$V_{LOADREG}$	LDO load regulation	V_{EN} = 0 V, I_{LDO} = 80 mA, V_{IN} ≥ 5.2 V	-0.5		0.5	%
I_{LDO}	LDO current limit	V_{EN} = 0 V, V_{IN} ≥ 5.2 V	100	170	240	mA
R_{LDOSW}	VOUT switch-over FET on resistance (TPS51383)	V_{VIN} ≥ 5.2 V, V_{EN} = 3.3 V, V_{OUT} = 3.3 V, I_{LDO} = 50 mA		0.8	2.1	Ω
R_{LDOSW}	VOUT switch-over FET on resistance (TPS51384)	V_{VIN} ≥ 5.2 V, V_{EN} = 3.3 V, V_{OUT} = 1.8 V, I_{LDO} = 50 mA		0.5	1	Ω
R_{LDOSW}	VOUT switch-over FET on resistance (TPS51383)	V_{VIN} = 4.5 V, V_{EN} = 3.3 V, V_{OUT} = 3.3 V, I_{LDO} = 50 mA		1.7	2.65	Ω
R_{LDOSW}	VOUT switch-over FET on resistance (TPS51384)	V_{VIN} = 4.5 V, V_{EN} = 3.3 V, V_{OUT} = 1.8 V, I_{LDO} = 50 mA		0.6	1.3	Ω
V_{BYPON}	VOUT switch-over turn on voltage	V_{EN} = 3.3 V		98		%
V_{BYPOFF}	VOUT switch-over turn off voltage	V_{EN} = 3.3 V		96		%
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold			165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			20		°C

(1) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.6 Typical Characteristics

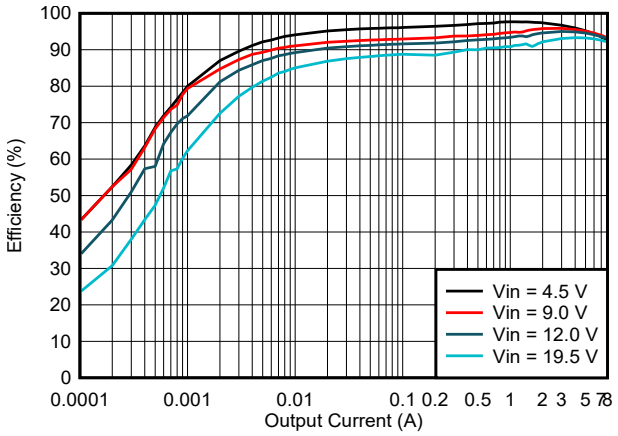


図 6-1. TPS51383 PSM Efficiency

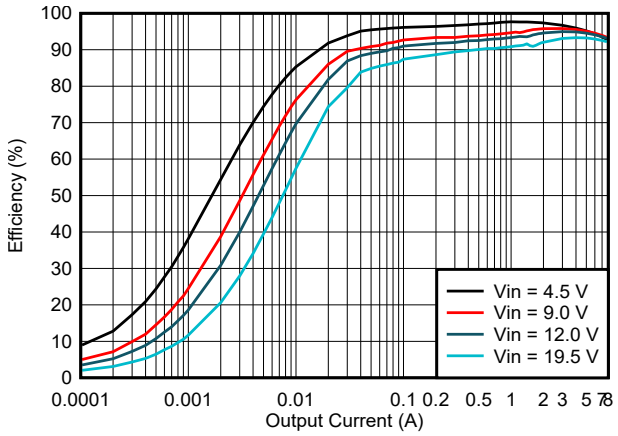


図 6-2. TPS51383 OOA Efficiency

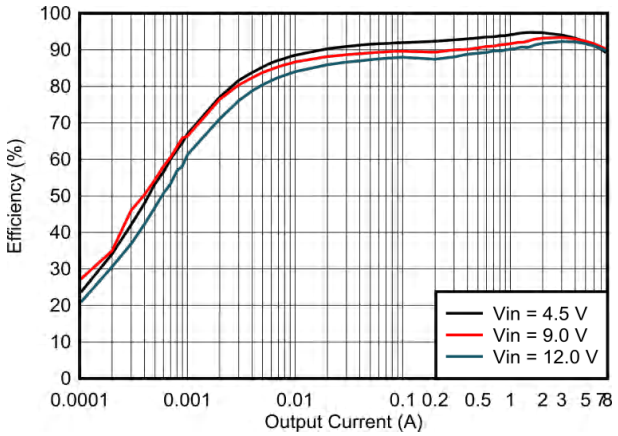


図 6-3. TPS51384 PSM Efficiency

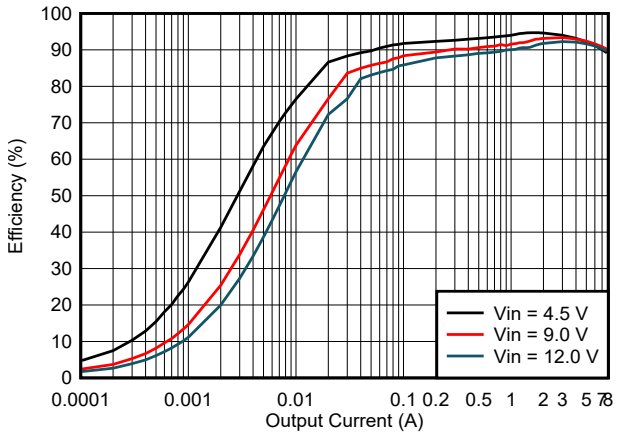


図 6-4. TPS51384 OOA Efficiency

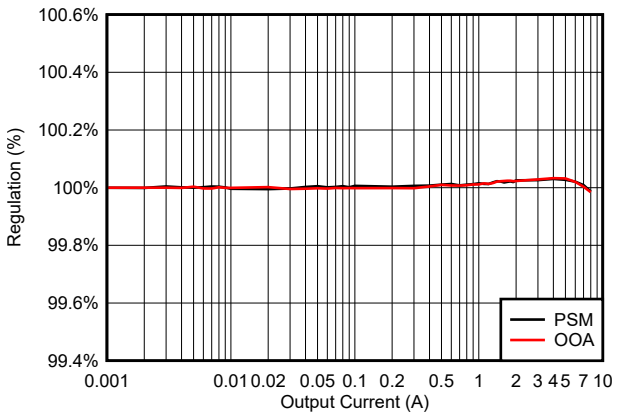


図 6-5. TPS51383 Load Regulation

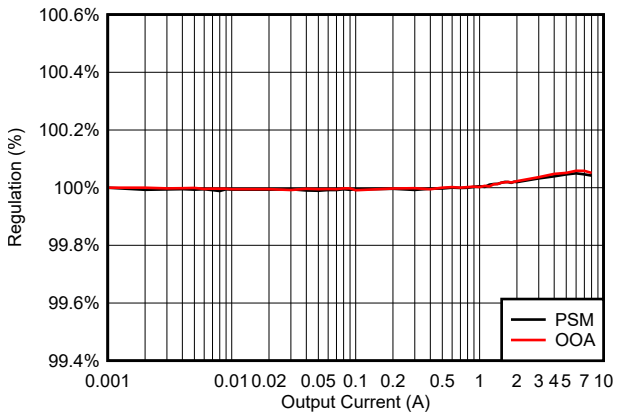


図 6-6. TPS51384 Load Regulation

6.6 Typical Characteristics (continued)

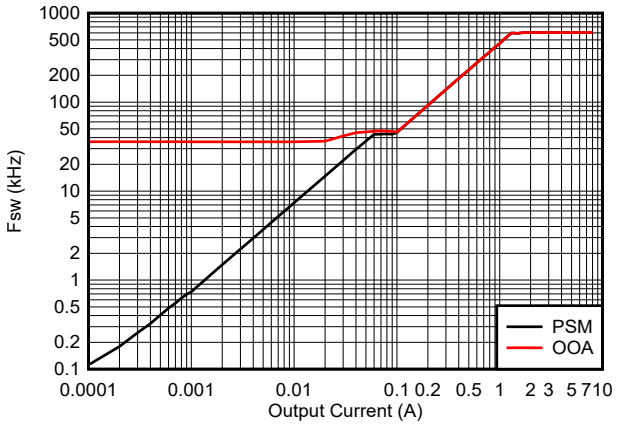


図 6-7. TPS51383 Fsw vs Iout

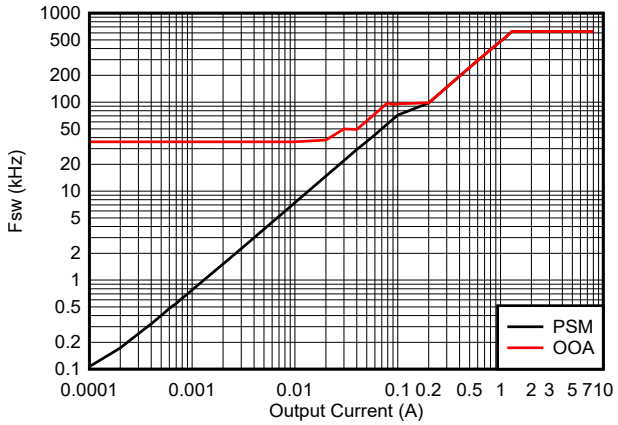


図 6-8. TPS51384 Fsw vs Iout

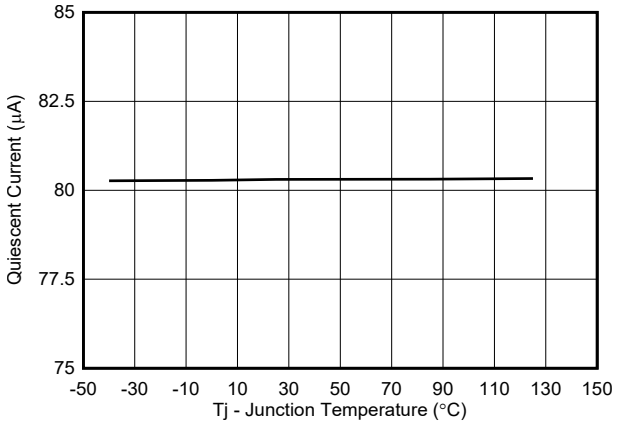


図 6-9. Quiescent Current vs Temperature

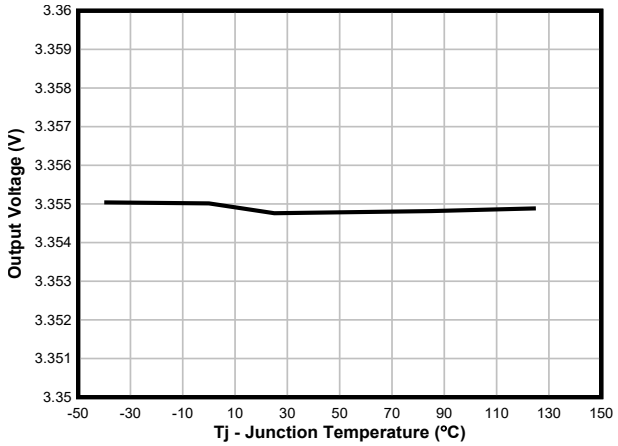


図 6-10. Output Voltage vs Temperature

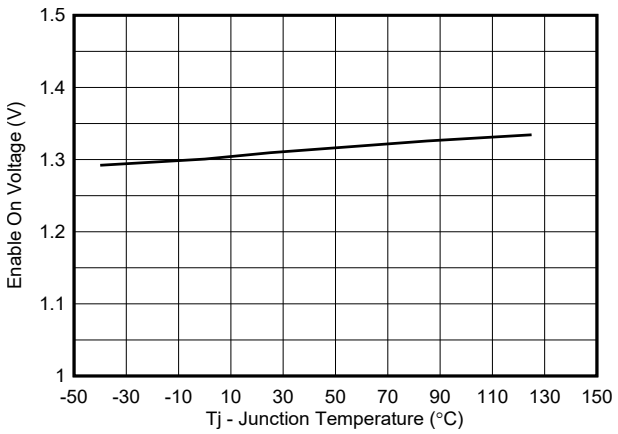


図 6-11. Enable On Voltage vs Temperature

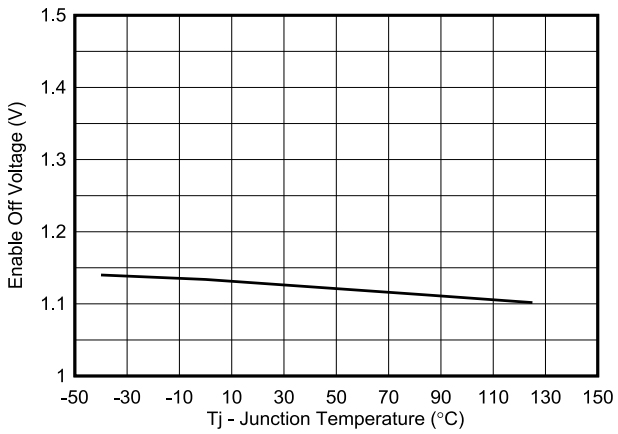


図 6-12. Enable Off Voltage vs Temperature

6.6 Typical Characteristics (continued)

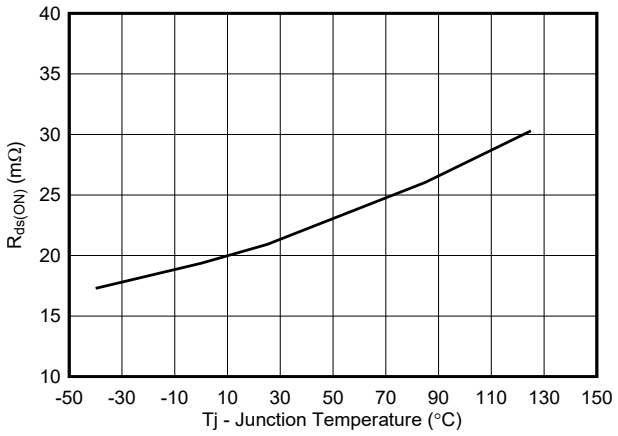


図 6-13. High-side $R_{DS(on)}$ vs Temperature

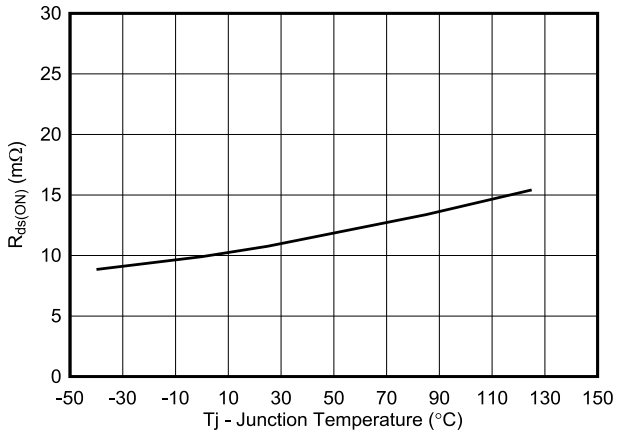


図 6-14. Low-side $R_{DS(on)}$ vs Temperature

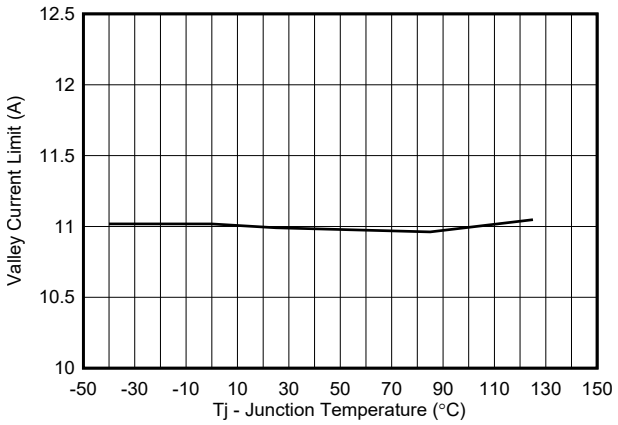


図 6-15. Valley Current Limit vs Temperature

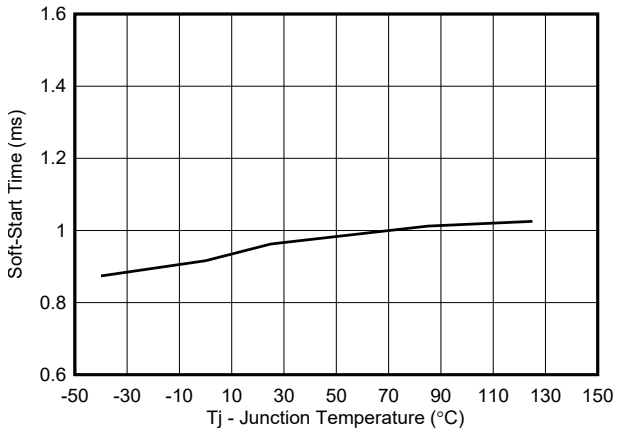


図 6-16. Soft-Start Time vs Temperature

7 Detailed Description

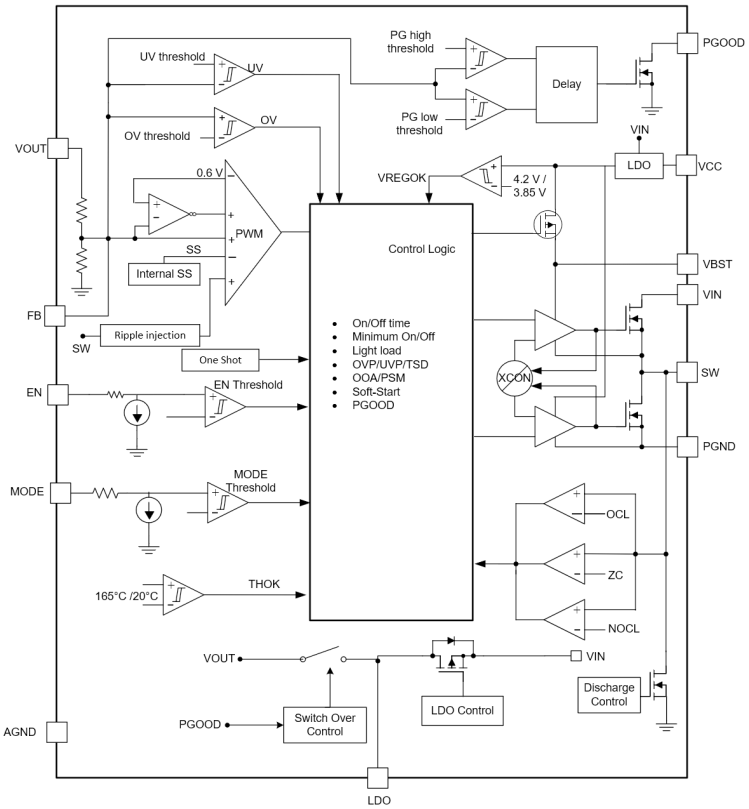
7.1 Overview

The TPS51383 and TPS51384 are synchronous step-down buck converters that can operate from 4.5-V to 24-V input voltage (V_{IN}). TPS51383 features fixed 3.36-V output, and TPS51384 features fixed 1.82-V output. Both devices have integrated 22-mΩ and 11-mΩ integrated MOSFETs enable high efficiency up to 8-A output current. D-CAP3 control mode provides fast transient response without external compensation components and an accurate feedback voltage. The D-CAP3 control mode topology also provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition. DCM allows the TPS51383 and TPS51384 to maintain high efficiency at light loads, and Out Of Audio (OOA) function maintains a minimum of 25-kHz switching frequency that is above audible range (20 Hz – 20 kHz). D-CAP3 control mode allow the use of low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The TPS51383 and TPS51384 have 5-V internal VCC LDO that creates bias for all internal circuitry. The undervoltage lockout (UVLO) circuit monitors the VCC pin voltage to protect the internal circuitry from low input voltages. Both devices have an internal pulldown current source on the EN pin, require external pullup circuit to enable buck converter. Both devices feature MODE pin dynamic change, which allows the device to change state between OOA Mode and PSM Mode dynamically by toggling MODE pin high or low. TPS51383 and TPS51384 have fixed 600-kHz switching frequency and fixed 1-ms soft start.

TPS51383 features 3.36-V fixed output and a build in 3.3-V, 100-mA LDO. TPS51384 features 1.82-V fixed output and a build in 1.8-V, 100-mA LDO. The LDO is designed for powering external circuits that require constant power even when switching regulator is off (Vin > UVLO, EN = LOW). When the buck converter is ready, PGood is pulled high, and the buck output replaces the LDO output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control Mode

The TPS51383 and TPS51384 operates using the adaptive on-time PWM control with a proprietary D-CAP3 control mode which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle, the high side MOSFET is turned on for an on-time set by an internal one shot timer. This on-time is set based on the converter input voltage, output voltage, and the pseudo-fixed frequency hence this type of control topology is called an adaptive on-time control. The one shot timer resets and turns on again after the feedback voltage (V_{FB}) falls below the internal reference voltage (V_{REF}). An internal ramp is generated which is fed to the FB pin to simulate the output voltage ripple. This action enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode topology.

The TPS51383 and TPS51384 includes an error amplifier that makes the output voltage very accurate. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used is a low pass L-C circuit. This L-C filter has double pole that is described in the following equation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is optimized to provide fast transient response performance and also give an consideration to meet the stability requirement with typical external L-C filter. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-fifth of the switching frequency (F_{SW}).

7.3.2 VCC LDO

The VCC pin is the output of the internal 5.0-V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VCC pin must be bypassed with a minimum 1-µF, 10-V X5R rated capacitor. The UVLO circuit monitors the VCC pin voltage and disables the output when VCC falls below the UVLO threshold.

7.3.3 Soft Start

TPS51383 and TPS51384 feature fixed internal 1-ms softstart. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Enable Control

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold which is around 1.31 V, the device starts switching and when the EN pin voltage falls below the turn-off threshold which is around 1.13V it stops switching.

7.3.5 Power Good

The Power Good (PGOOD) pin is an open drain output. After the FB pin voltage is between 90% and 115% of the internal reference voltage (V_{REF}) the PGOOD is de-asserted and floats after a 500-µs de-glitch time. TI recommends a pullup resistor of 100 kΩ to pull it up to VCC. The PGOOD pin is pulled low when the FB pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold or in an event of thermal shutdown or during the soft-start period.

7.3.6 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 256 us. In this type of valley detect control, the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. This protection is a latch function, fault latching can be re-set by EN going low or VIN power cycling.

7.3.7 100-mA LDO with Switch Over

TPS51383 includes a 3.3-V, 100-mA standby linear regulator. TPS51384 includes a 1.8-V, 100-mA standby linear regulator. The 100-mA LDO is intended mainly as an auxiliary supply for the notebook system during standby mode. When the Buck converter output voltage becomes higher than 98% of VOUT and the PGOOD is high, the internal LDO is switched over to VOUT by the internal MOSFET. This action helps reduce the power loss from the LDO. The LDO pin must be bypassed with a 10-V, X5R rated or better ceramic capacitor with minimum 4.7-uF capacitance, placed as close to the LDO pin as possible.

7.3.8 UVLO Protection

Undervoltage Lock Out protection (UVLO) monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.9 Overvoltage Protection

TPS51383 and TPS51384 detect overvoltage and undervoltage conditions by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and output is discharged after a wait time of 20 us. When the OV fault comparator has been tripped for 256 us, the part latches off. When the overvoltage condition is removed, output remains latched until EN is toggled to low then high, or the power cycling VIN.

7.3.10 Output Voltage Discharge

TPS51383 and TPS51384 have a 160-ohm discharge switch that discharges the output V_{OUT} through the Vout pin during any event of fault like output overvoltage, output undervoltage, TSD, or if VCC voltage is below the UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

7.3.11 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 165°C) the device shuts off. This protection is a non-latch protection. The device re-starts switching when the temperature goes below the thermal shutdown threshold and 20°C hysterisis.

7.4 Device Functional Modes

7.4.1 MODE Pin

TPS51383 and TPS51384 have a MODE pin that can be used to toggle mode of the device by pulling it high (> 0.8 V) or low (< 0.4 V). When the MODE pin is pulled high, it enables the converter to operate in Out-of-Audio™ (OOA) mode. When the MODE pin is pulled low or float, the converter goes into Power Save Mode (PSM). The MODE pin can be toggled dynamically, even when the converter is in operation.

7.4.2 Out-Of-Audio™ Mode

Out-of-Audio (OOA) mode is a unique control feature that maintains minimum switching frequency of 25 kHz at light load conditions where regular discontinuous conduction mode cause switching frequency to drop into audible range (20 Hz – 20 kHz), to prevent switching frequency to be audible.

7.4.3 Power Save Mode (PSM)

The TPS51383 and TPS51384 can be placed in power save mode by floating the MODE pin or pulling the MODE pin low (< 0.4 V).

8 Application and Implementation

注

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8.1 Application Information

The schematic shows a typical application for TPS51383. This design converts an input voltage range of 4.5 V to 24 V down to 3.36 V with a maximum output current of 8 A.

8.2 Typical Application

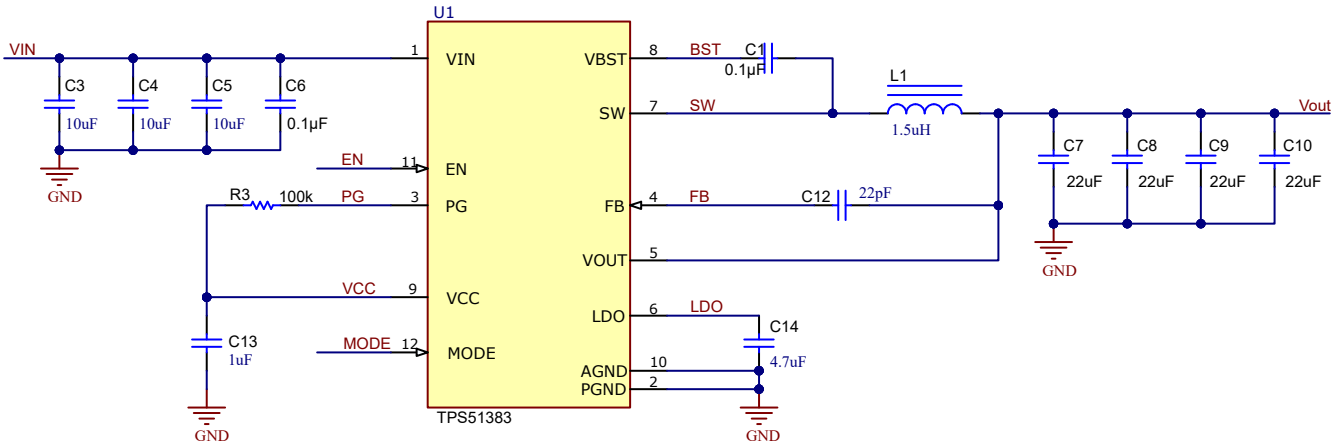

図 8-1. Application Schematic

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			3.36		V
I_{OUT}	Output current				8	A
V_{IN}	Input voltage		4.5	19	24	V
$V_{OUT(ripple)}$	Output voltage ripple			24		$mV_{(P-P)}$
F_{SW}	Switching frequency			600		kHz
Operating Mode		Float MODE pin		PSM		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See 表 8-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 式 2 and 式 3. Make sure that the inductor is rated to handle these currents.

$$I_{L(rms)}=\sqrt{\left(I^2_{OUT}+\frac{1}{12}\times\left(\frac{V_{OUT}\times\left(V_{IN(max)}-V_{OUT}\right)}{V_{IN(max)}\times L_{OUT}\times F_{SW}}\right)^2\right)} \quad (2)$$

$$I_{L(peak)}=I_{OUT}+\frac{I_{OUT(ripple)}}{2} \quad (3)$$

During transient, short-circuit conditions the inductor current can increase up to the current limit of the device, so choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.2 Output Capacitor Selection

After selecting the inductor the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 8-2

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$

表 8-2. Recommended Component Values

V_{OUT} (V)	C_{ff} (pF)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(Range)}$ (µF)
3.36	22	600	2.2	44-500
		600	1.5	44-500
1.82	NA	600	1.5	44-500
		600	1.0	44-500

8.2.2.1.3 Input Capacitor Selection

The minimum input capacitance required is given in 式 4.

$$C_{IN(min)}=\frac{I_{OUT}\times V_{OUT}}{V_{INripple}\times V_{IN}\times F_{SW}} \quad (4)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 22 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 式 5 below:

$$I_{CIN(rms)}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN(min)}}\times\frac{\left(V_{IN(min)}-V_{OUT}\right)}{V_{IN(min)}}} \quad (5)$$

8.2.3 Application Curves

V_{IN} = 19 V, T_a = 25°C unless otherwise specified.

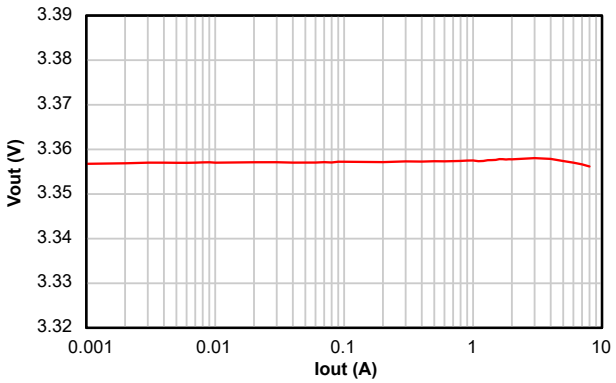

図 8-2. Load Regulation

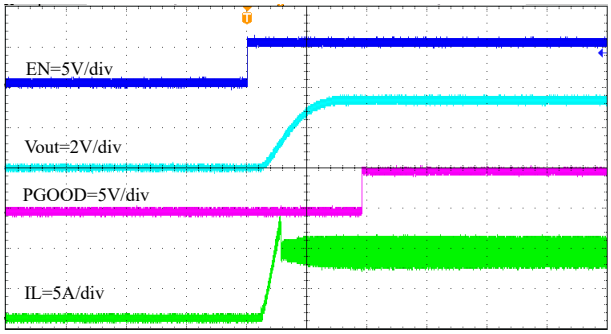

図 8-3. Start-up Relative to EN Rising

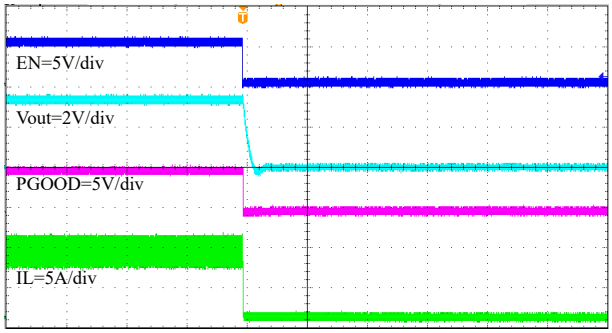

図 8-4. Shutdown Relative to EN Falling

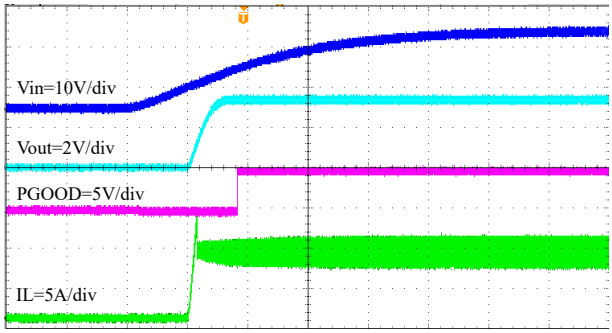

図 8-5. Start-up Relative to Vin Rising

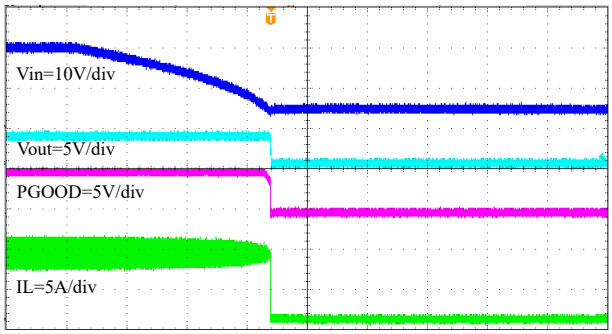

図 8-6. Shutdown Relative to Vin Falling

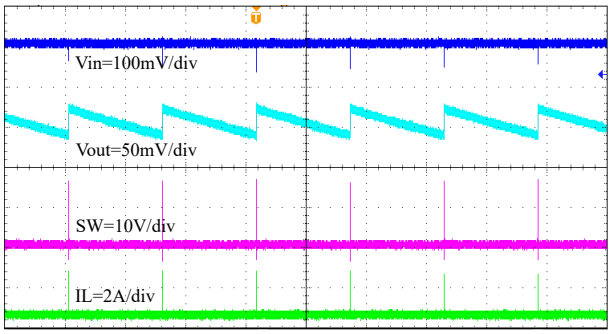

図 8-7. PSM Mode Output Voltage Ripple, Iout = 0 A

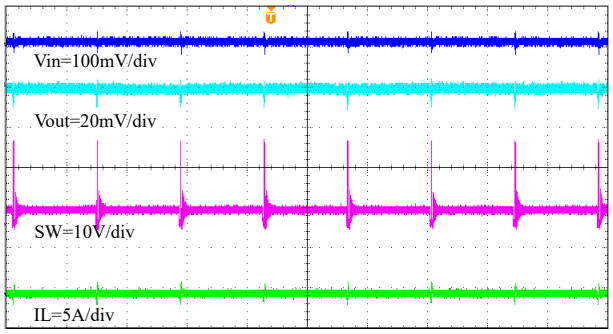

図 8-8. OOA Mode Output Voltage Ripple, Iout = 0 A

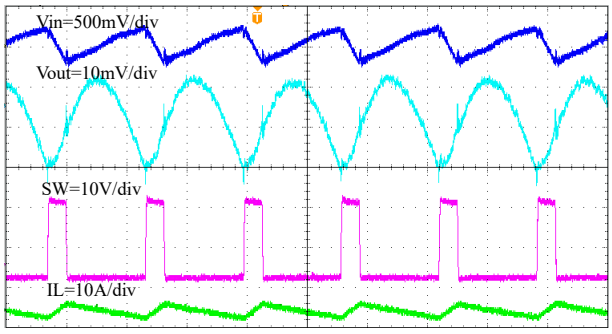

図 8-9. Output Voltage Ripple, Iout = 8 A

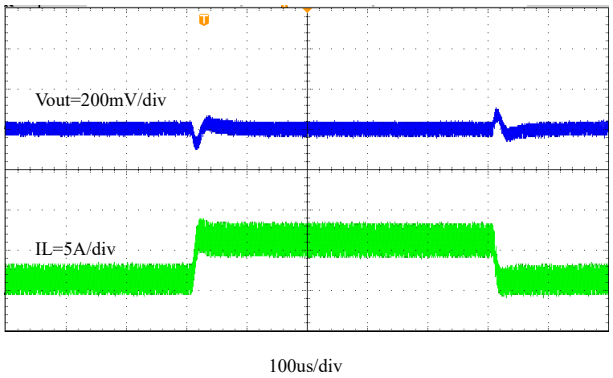

図 8-10. Transient Response, 1.6 A to 6.4 A with 2.5 A/us SR

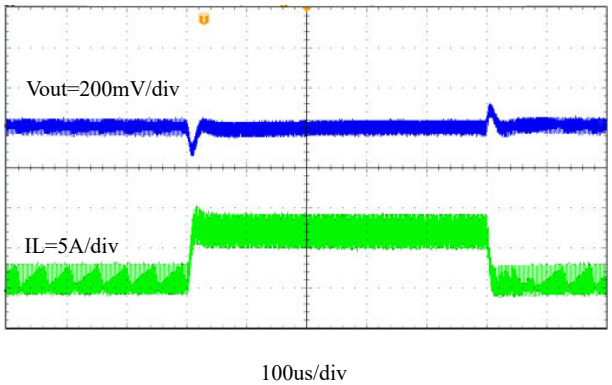

図 8-11. Transient Response, 0.8 A to 7.2 A with 2.5 A/us SR

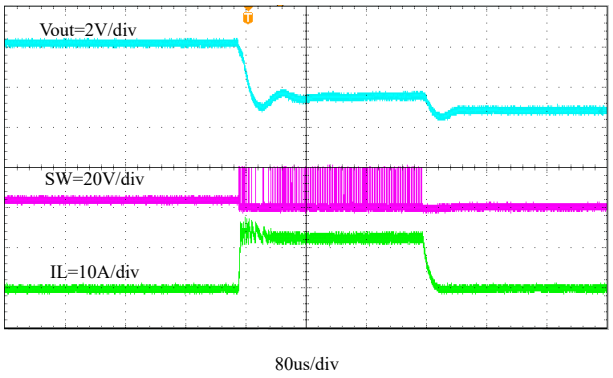

図 8-12. Normal Operation to Output Hard Short

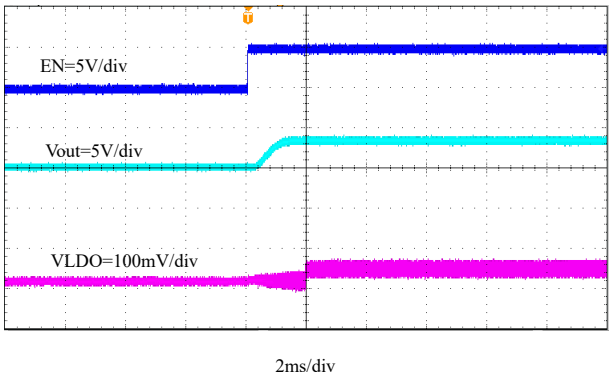

図 8-13. LDO Switch Over

8.3 Power Supply Recommendations

The TPS51383 and TPS51384 are intended to be powered by a well regulated DC voltage. The input voltage range is 4.5 V to 24 V. TPS51383 and TPS51384 are buck converters. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS51383 and TPS51384 circuit, TI recommends some additional input bulk capacitance. Typical values are 22 µF to 88 µF.

8.4 Layout

8.4.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane.
- Recommend having a small bypass capacitor on VIN side of the IC. Place the capacitor as close to IC as possible.
- FB and VOUT traces must be routed away from the noisy switch node.
- VIN and VOUT traces must be wide to reduce the trace impedance.

8.4.2 Layout Example

Top Side Layout shows the recommended top side layout.

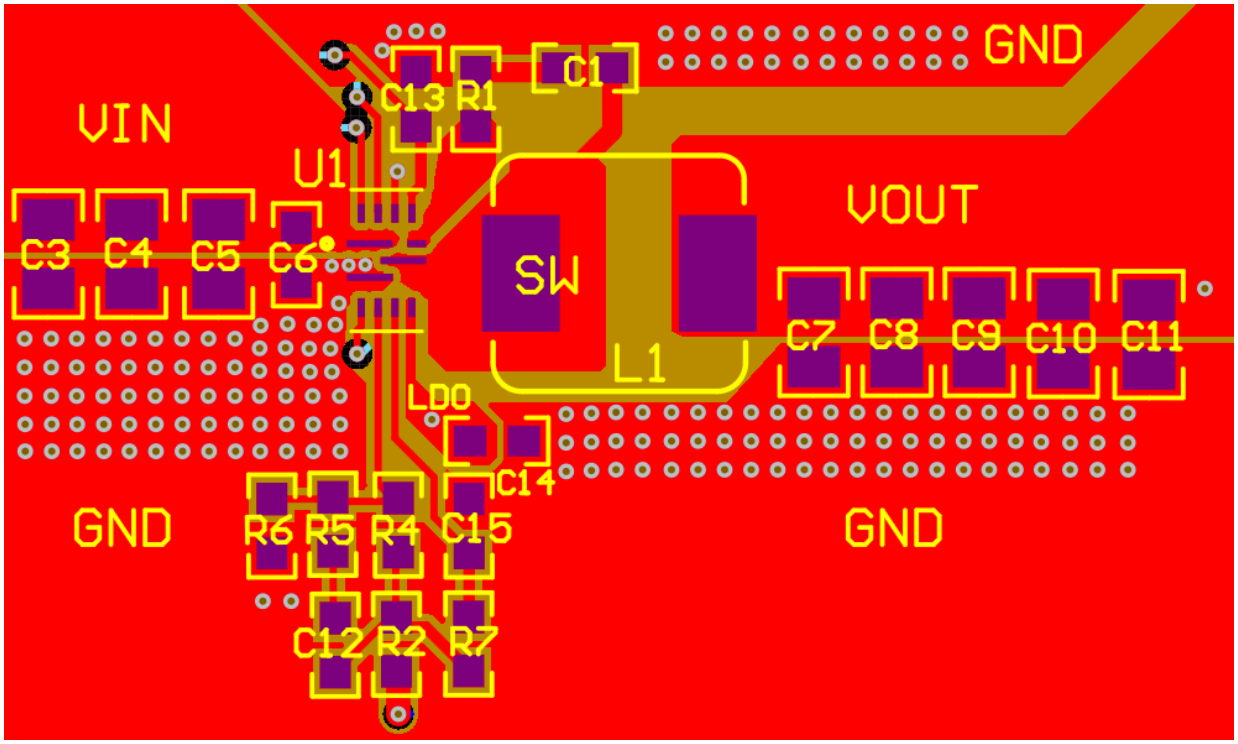

図 8-14. Top Side Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51383RJNR	ACTIVE	VQFN-HR	RJN	12	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	51383	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

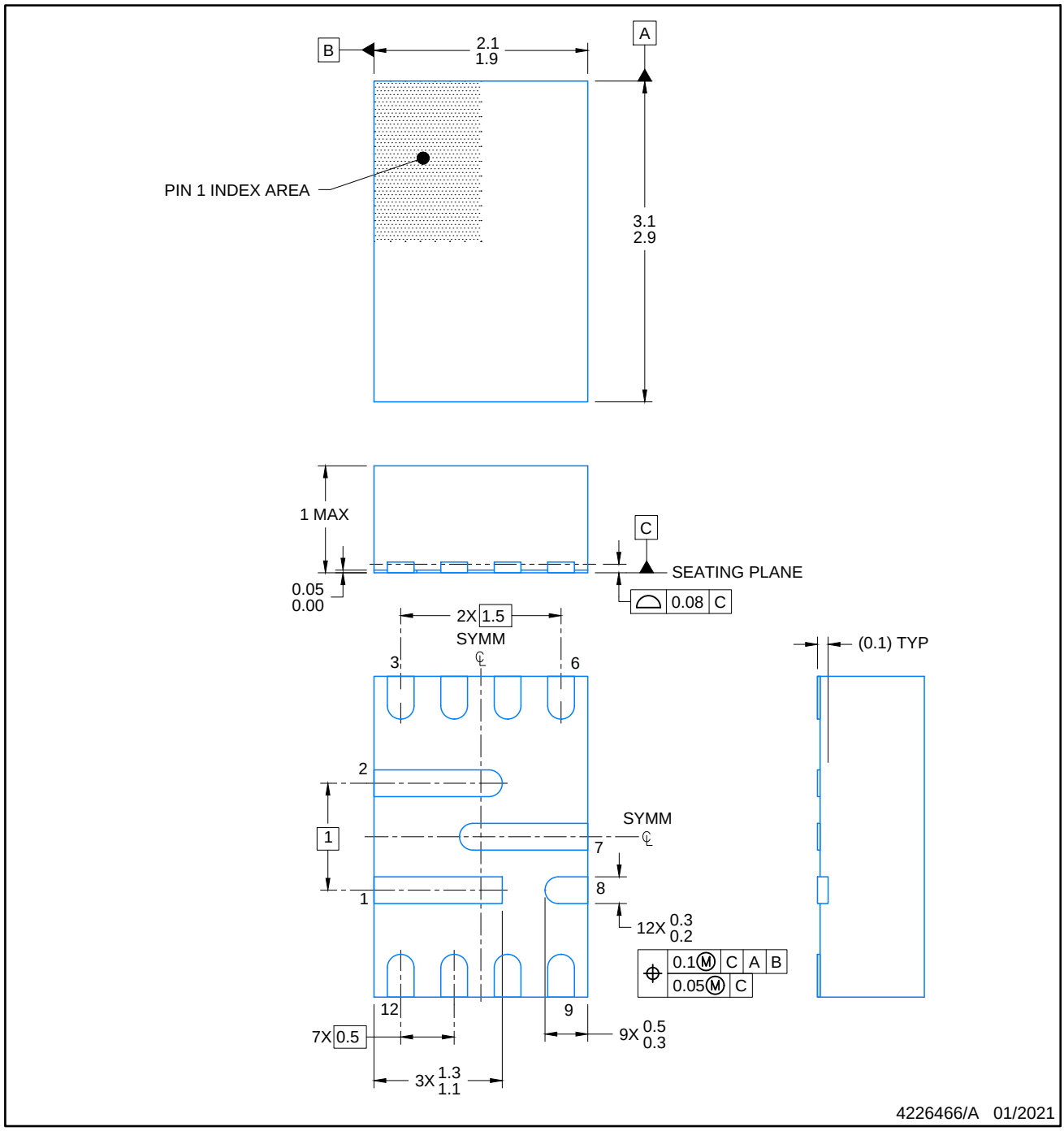
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RJN0012A

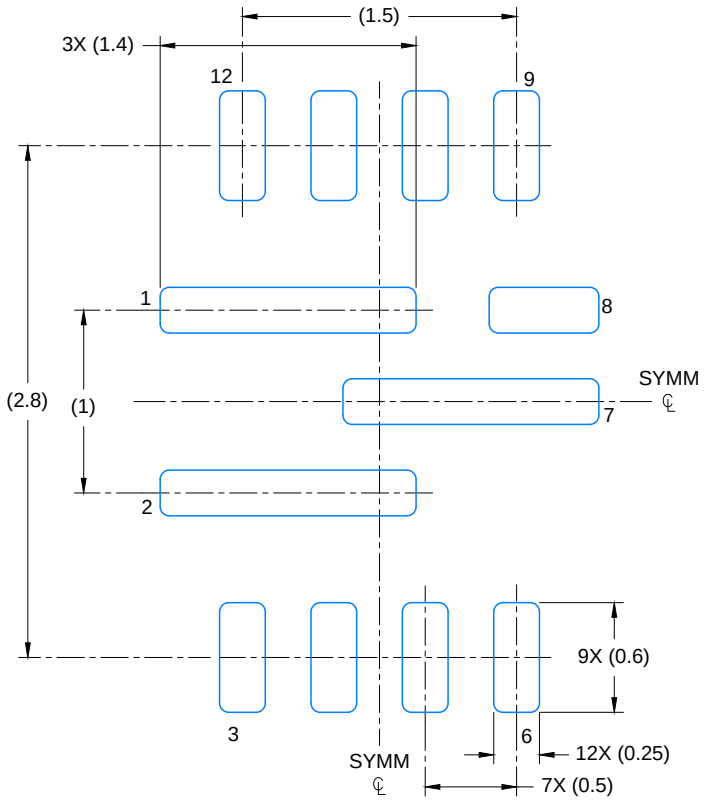
VQFN-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

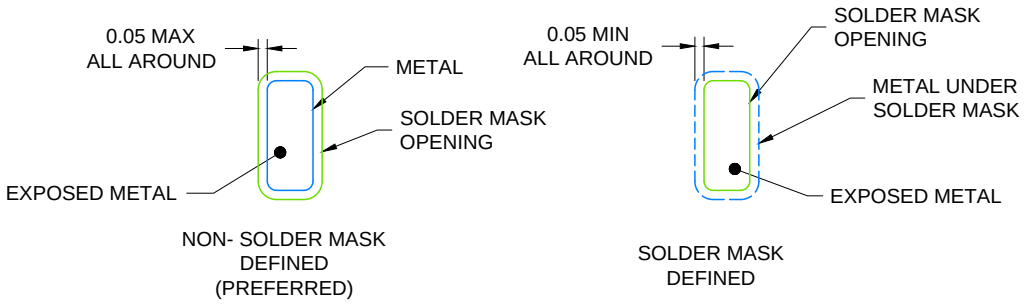


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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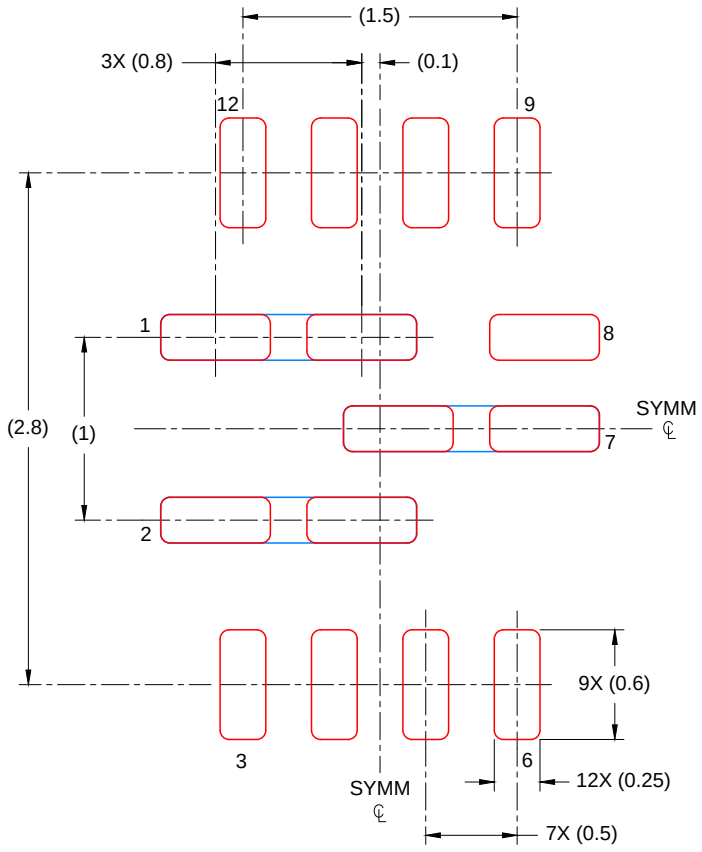
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
PINS 1,2,7: 86%
SCALE: 25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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