TPS53014 4.5V～28V 入力、D-CAP2™ の同期整流降圧コントローラ

1 特長

- D-CAP2™モード制御
  - 高速過渡応答
  - ループ補償に外付け部品が不要
  - セラミック出力コンデンサに対応
- **初期精度が高い基準電圧** (±1%)
- **広い入力電圧範囲**：4.5V～28V
- **出力電圧範囲**：0.77V～7.0V
- **ローサイド $R_{DS(ON)}$ の無損失電流センシング**
- **調整可能なソフト・スタート**
- **シンクなしのプリバイアス付きソフト・スタート**
- 500kHz のスイッチング周波数
- **サイクル単位の過電流制限制御**
- **自動スキップ Eco-mode™ により、軽負荷時の効率を向上**
- OCL、OVP、UVP、UVLO、TSD 保護
- **昇圧 PMOS スイッチ内蔵の適応型ゲート・ドライバ**
- **温度補償された** OCP：4000ppm/°C
- 10 ピン VSSOP

2 アプリケーション

- **広範なアプリケーション向けの低消費電力システムのポイント·オブ·ロード（POL）レギュレーション**
  - デジタル・テレビ用電源
  - ネットワーク・ホーム・ターミナル
  - デジタル・セットトップ・ボックス (STB)
  - DVD プレーヤー / レコーダー
  - ゲーム機など

3 概要

TPS53014 はシングル、適応型オン時間の D-CAP2™ モード、同期整流降圧コントローラです。TPS53014 を使うと、各種最終機器の電源バス・レギュレータを、コスト効果が高く、外付け部品数の少ない、低スタンバイ電流のソリューションで設計できます。TPS53014 の主制御ループは、外部補償部品なしで非常に高速な過渡応答が得られる D-CAP2 モード制御を使用しています。適応型オン時間制御により、高負荷時の PWM モードと、軽負荷時の Eco-mode™動作との間をシームレスに移行できます。Eco-mode により、TPS53014 は軽負荷時に高い効率を維持できます。また TPS53014 は、POSCAP や SP-CAP など等価直列抵抗 (ESR) の低い出力コンデンサにも、ESR の非常に低いセラミック・コンデンサにも対応できます。このデバイスは 4.5V～28V の入力電圧、0.77V～7V の出力電圧に対応しており、使いやすく高効率で動作します。

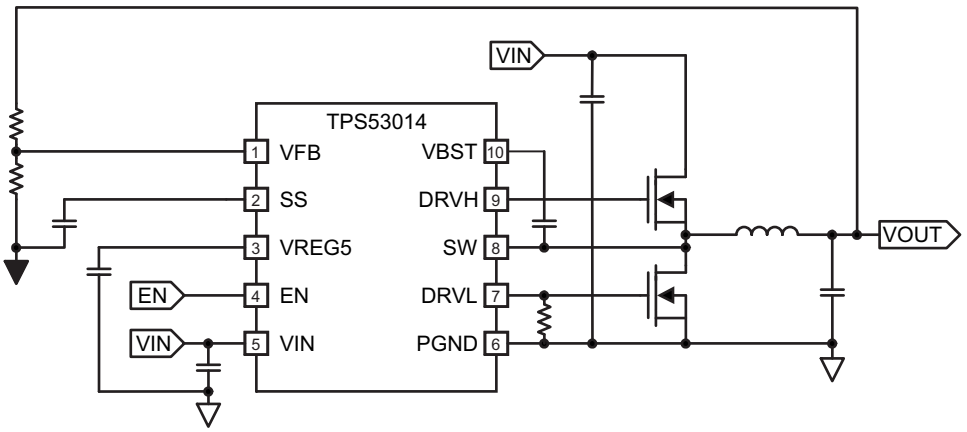
TPS53014 は、3mm×3mm の 10 ピン VSSOP (DGS) パッケージで供給され、-40°C～+85°C の周囲温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS53014	DGS (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



目次

4 改訂履歴

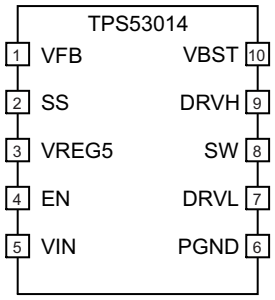
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2012年5月発行のものから更新 **Page**

- 編集上の変更のみ、技術的変更点なし、コンテンツを最新の TI データシート標準に合わせて更新 ... 1

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	VSSOP-10		
VFB	1	I	D-CAP2 feedback input. Connect to output voltage with resistor divider.
SS	2	O	Soft start programming pin. Connect capacitor from SS pin to GND to program soft start time.
VREG5	3	O	Output of 5-V linear regulator and supply for MOSFET driver. Bypass to GND with a minimum 4.7-μF high quality ceramic capacitor. VREG5 is active when EN is asserted high.
EN	4	I	Enable. Pull High to enable converter.
VIN	5	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum 0.1-μF high quality ceramic capacitor.
PGND	6	I	System ground.
DRVL	7	O	Low-side N-Channel MOSFET gate driver output. PGND referenced driver switches between PGND(OFF) and VREG5(ON).
SW	8	I/O	Switch node connections for both the high-side driver and over current comparator.
DRVH	9	O	High-side N-channel MOSFET gate driver output. SW referenced driver switches between SW(OFF) and VBST(ON).
VBST	10	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from VBST to SW. An internal diode is connected between VREG5 and VBST

6 Specifications

6.1 Absolute Maximum Ratings

Operating under free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Input voltage range	VIN, EN	–0.3 to 30	V
	VBST	–0.3 to 36	
	VBST - SW	–0.3 to 6	
	VFB	–0.3 to 6	
	SW	–0.3 to 30	
	SW (10 nsec transient)	–3.0 to 30	
Output voltage range	DRVH	–2 to 36	V
	DRVH - SW	–0.3 to 6	
	DRVL, VREG5, SS	–0.3 to 6	
	PGND	–0.3 to 0.3	
T_A	Operating ambient temperature range	–40 to 85	°C
T_{STG}	Storage temperature range	–55 to 150	°C
T_J	Junction temperature range	–40 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	28	V
Input voltage range	VBST	–0.1	33.5	V
	VBST - SW	–0.1	5.5	
	VFB	–0.1	5.5	
	EN	–0.1	28	
	SW	–1.0	28	
Output Voltage range	DRVH	–1.0	33.5	V
	DRVH - SW	–0.1	5.5	
	DRVL, VREG5, SS	–0.1	5.5	
	PGND	–0.1	0.1	
T_A	Operating free-air temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

6.3 Thermal Information

THERMAL METRIC(1)		TPS53014 DGS (10 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	172.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	93.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) 従来および新しい熱測定値の詳細については、『*Semiconductor and IC Package Thermal Metrics*』アプリケーション・レポート (SPRA953)を参照してください。

6.4 Electrical Characteristics

over recommended free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN Supply current	VIN current, T_A = 25°C, EN = 5V, V_{VFB} = 0.8V, V_{SW} = 0 V		660		µA
I_{VINSDN}	VIN Shutdown current	VIN current, T_A = 25°C, No Load , V_{EN} = 0V, VREG5 = OFF		6.0		µA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{VFBTHL}	VFB Threshold voltage	T_A = 25°C , V_{OUT} = 1.05 V	765.3	773.0	780.7	mV
TC_{VFB}	VFB Temperature coefficient	Relative to T_A = 25°C (1)	-140		140	ppm/°C
I_{VFB}	VFB Input current	VFB = 0.8V, T_A = 25°C	-150	-10	100	nA
VREG5 OUTPUT						
V_{VREG5}	VREG5 Output voltage	T_A=25°C, 6 V < V_{IN} < 28 V, I_{VREG5} = 5 mA		5.1		V
I_{VREG5}	Output current	VIN = 5.5V, V_{VREG5} = 4.0V, T_A = 25°C		120		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50mA, T_A = 25°C		3.2	4.7	Ω
		Sink, I_{DRVH} = 50mA, T_A = 25°C		1.4	2.4	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50mA, T_A = 25°C		6.9	8.2	Ω
		Sink, I_{DRVL} = 50mA, T_A = 25°C		0.8	1.7	
T_D	Dead time	DRVH-low to DRVL-on (1)		15		ns
		DRVL-low to DRVH-on (1)		20		
INTERNAL BOOST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5-VBST}$, I_F = 10mA, T_A = 25°C		0.1	0.2	V
SOFT START						
I_{ssc}	SS Charge current	VSS = 0V , T_A = 25°C	-7.36	-6.4	-5.44	µA
I_{ssd}	SS Discharge current	VSS = 0.5V , T_A = 25°C	4.5	5.0		mA
TC_{ISSC}	I_{SSC} Temperature coefficient	Relative to T_A = 25°C	-4.5		4.5	nA/°C
UVLO						
$V_{UVVREG5}$	VREG5 UVLO threshold	VREG5 Rising		4.0		V
		Hysteresis		0.3		
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.6			V
V_{ENL}	EN L-level threshold voltage				0.5	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	450	900	kΩ
CURRENT SENSE						
I_{TRIP}	TRIP Source current	V_{DRVL} = 0.1V, T_A = 25°C	14.3	15	15.8	µA
TC_{VTRIP}	V_{TRIP} Temperature coefficient	Relative to T_A = 25°C		4000		ppm/°C
V_{OCL}	Current limit threshold	R_{TRIP} = 75kΩ, T_A = 25°C	234	336	424	mV
		R_{TRIP} = 27kΩ, T_A = 25°C	121	174	220	
		R_{TRIP} = 6.8kΩ, T_A = 25°C	35	50	63	
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{OUT} = 1.05 V (1)		250		ns
$T_{OFF(MIN)}$	Minimum off time	V_{IN} = 4.5 V, V_{VFB} = 0.7 V, T_A = 25°C		230		ns

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect voltage	115%	120%	125%	
T_{OVPDEL}	Output OVP propagation delay				10	µs
V_{UVP}	Output UVP trip threshold	UVP detect voltage	63%	68%	73%	
T_{UVPDEL}	Output UVP delay			1		ms
T_{UVPEN}	Output UVP enable delay	UVP enable delay / soft start time	X1.4	X1.7	X2.0	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		25		

6.5 Typical Characteristics

V_{IN} = 12 V, T_A= 25°C (unless otherwise noted)

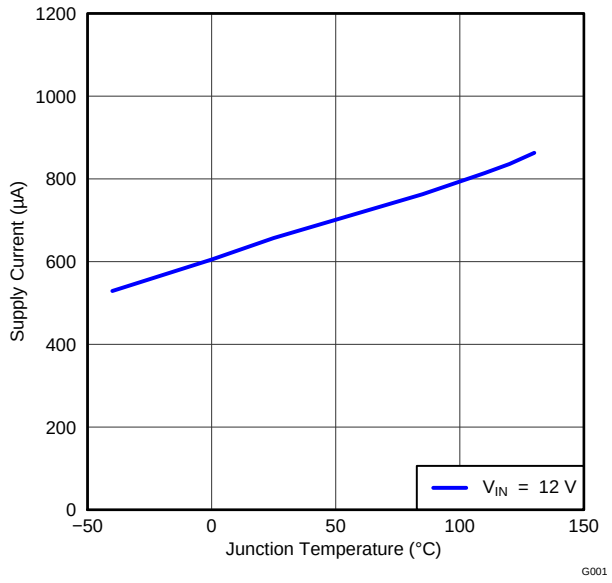


図 1. VIN Supply Current vs Junction Temperature

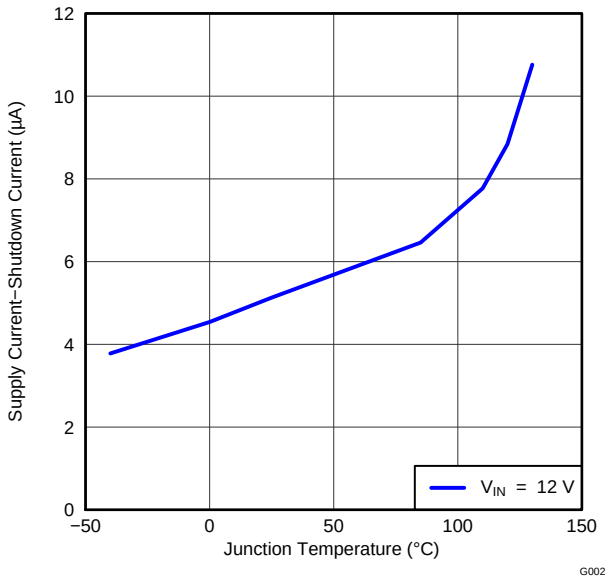


図 2. VIN Shutdown Current vs Junction Temperature

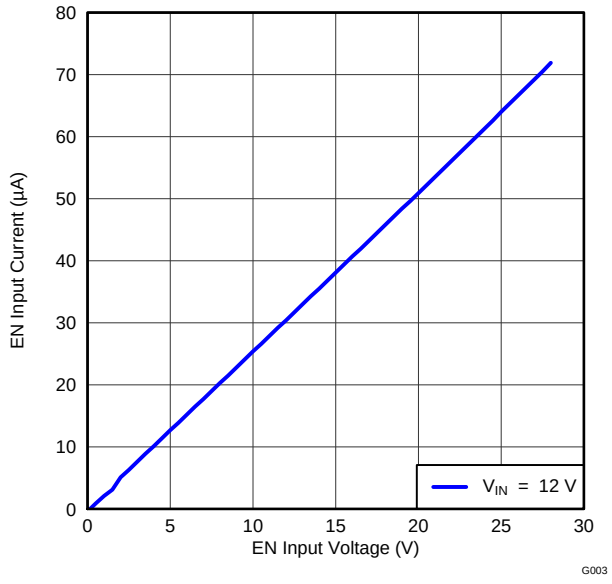


図 3. En Input Current Vs En Input Voltage

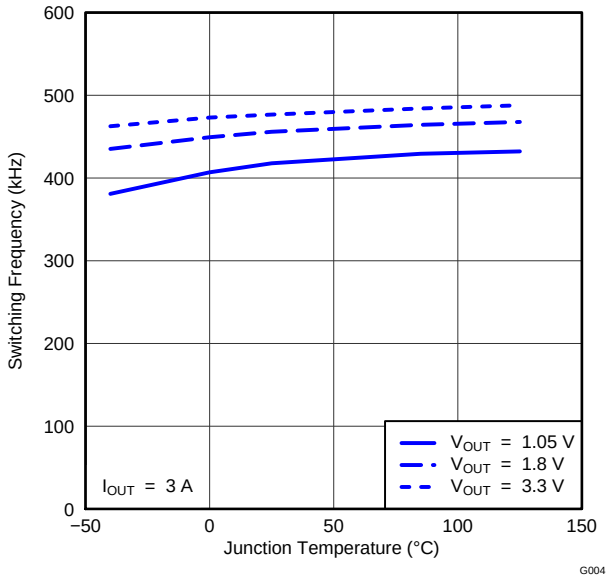


図 4. Switching Frequency vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V, T_A= 25°C (unless otherwise noted)

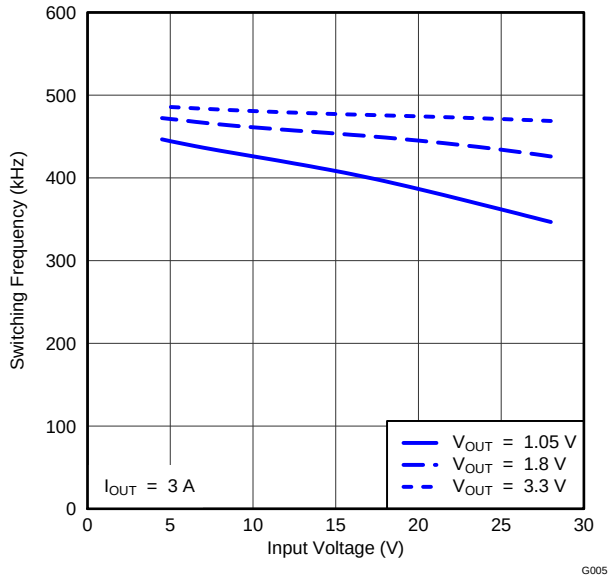


図 5. Switching Frequency vs Input Voltage

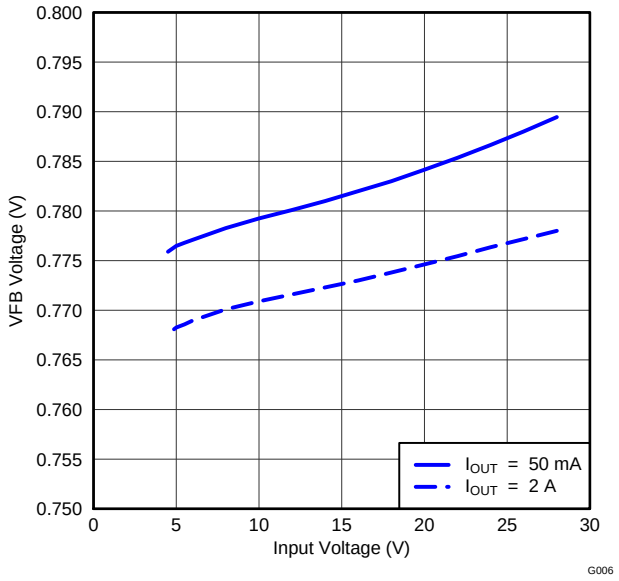


図 6. Vfb Voltage vs Input Voltage

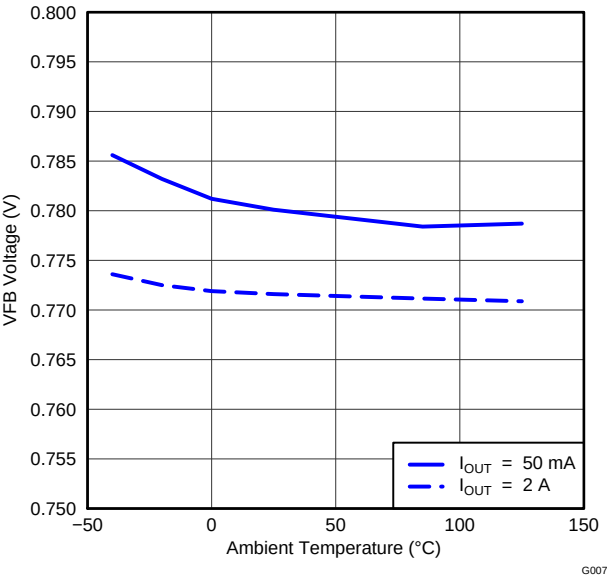


図 7. Vfb Voltage vs Ambient Temperature

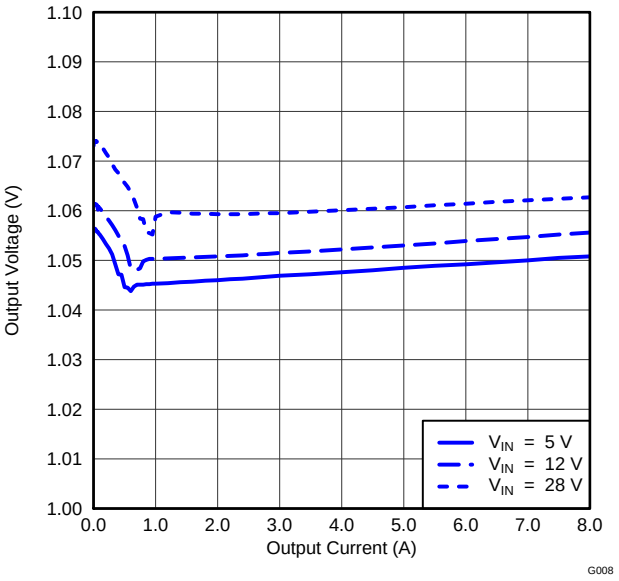


図 8. Load Regulation

Typical Characteristics (continued)

V_{IN} = 12 V, T_A= 25°C (unless otherwise noted)

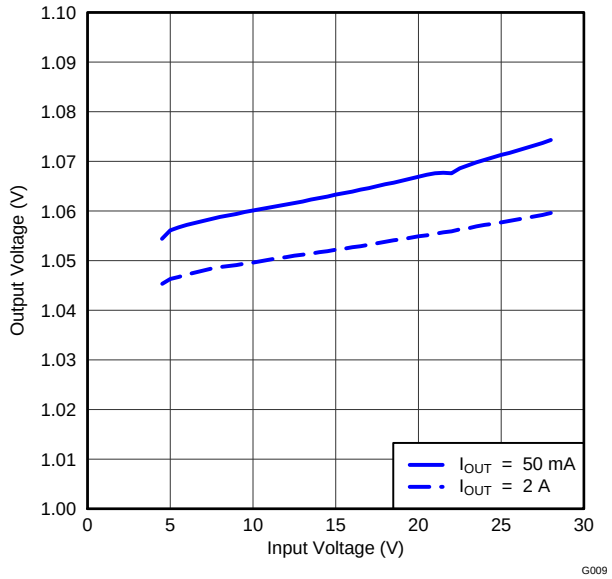


図 9. Line Regulation

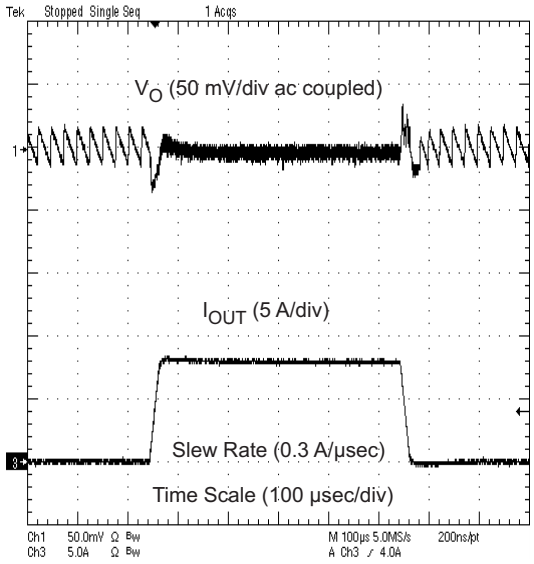


図 10. Transient Response

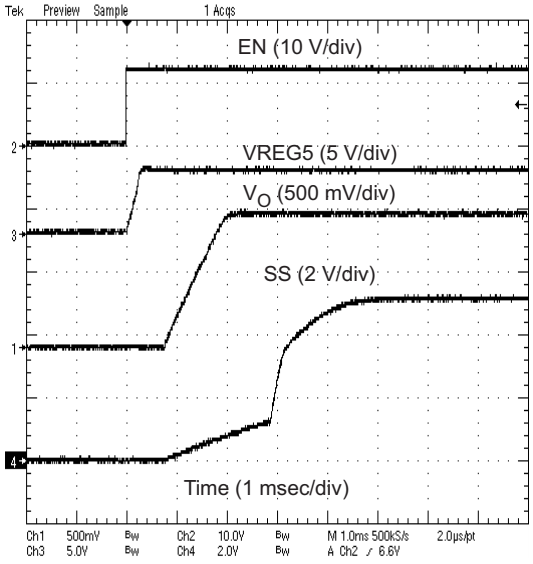


図 11. Start Up Waveforms

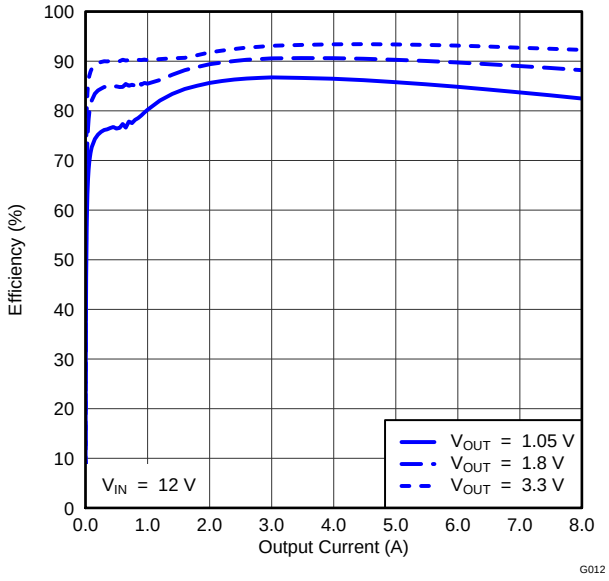


図 12. Efficiency

Typical Characteristics (continued)

V_{IN} = 12 V, T_A= 25°C (unless otherwise noted)

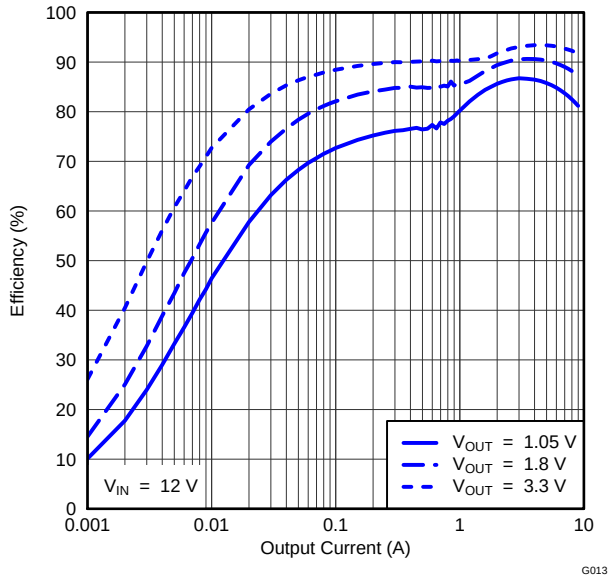


図 13. Light Load Efficiency

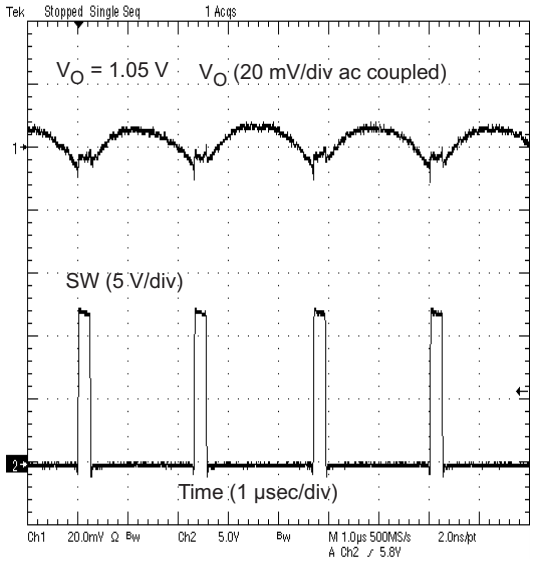


図 14. Output Voltage Ripple, I_{OUT} = 8 A

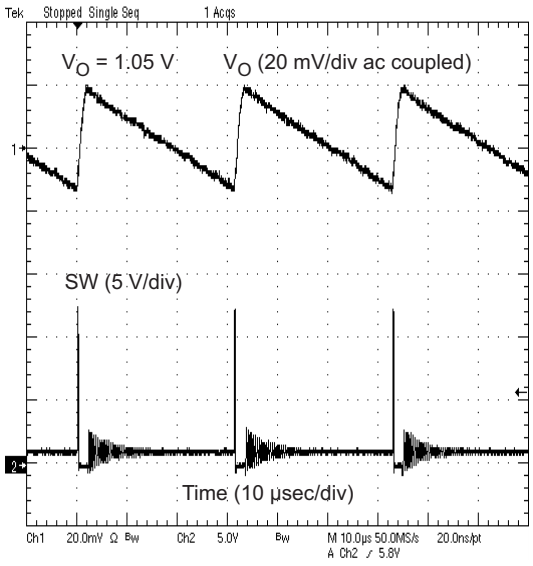


図 15. Output Voltage Ripple, I_{OUT} = 50 mA

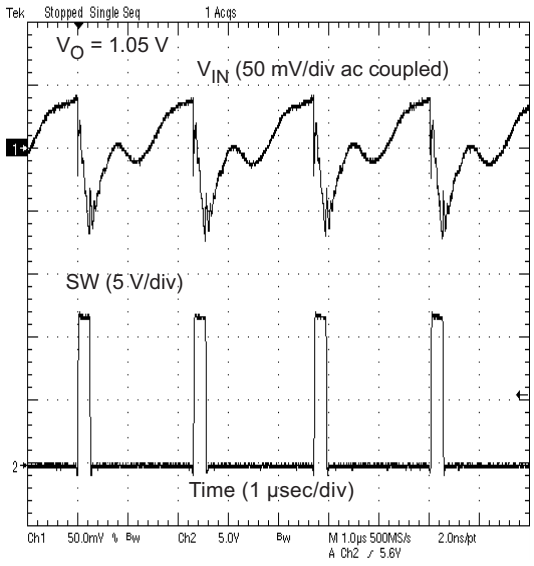


図 16. Input Voltage Ripple, I_{OUT} = 8 A

Typical Characteristics (continued)

V_{IN} = 12 V, T_A= 25°C (unless otherwise noted)

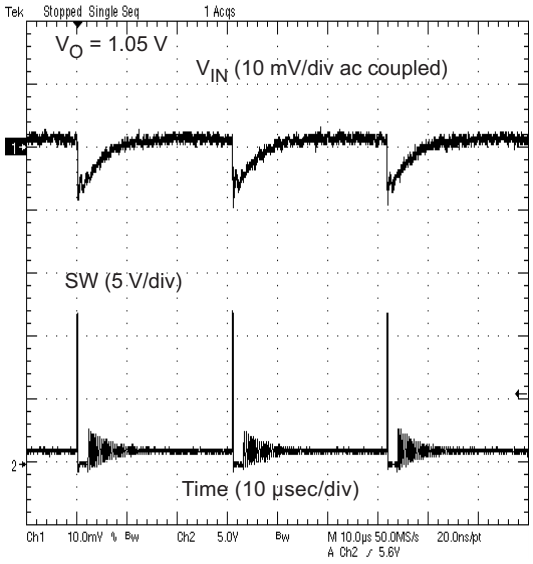


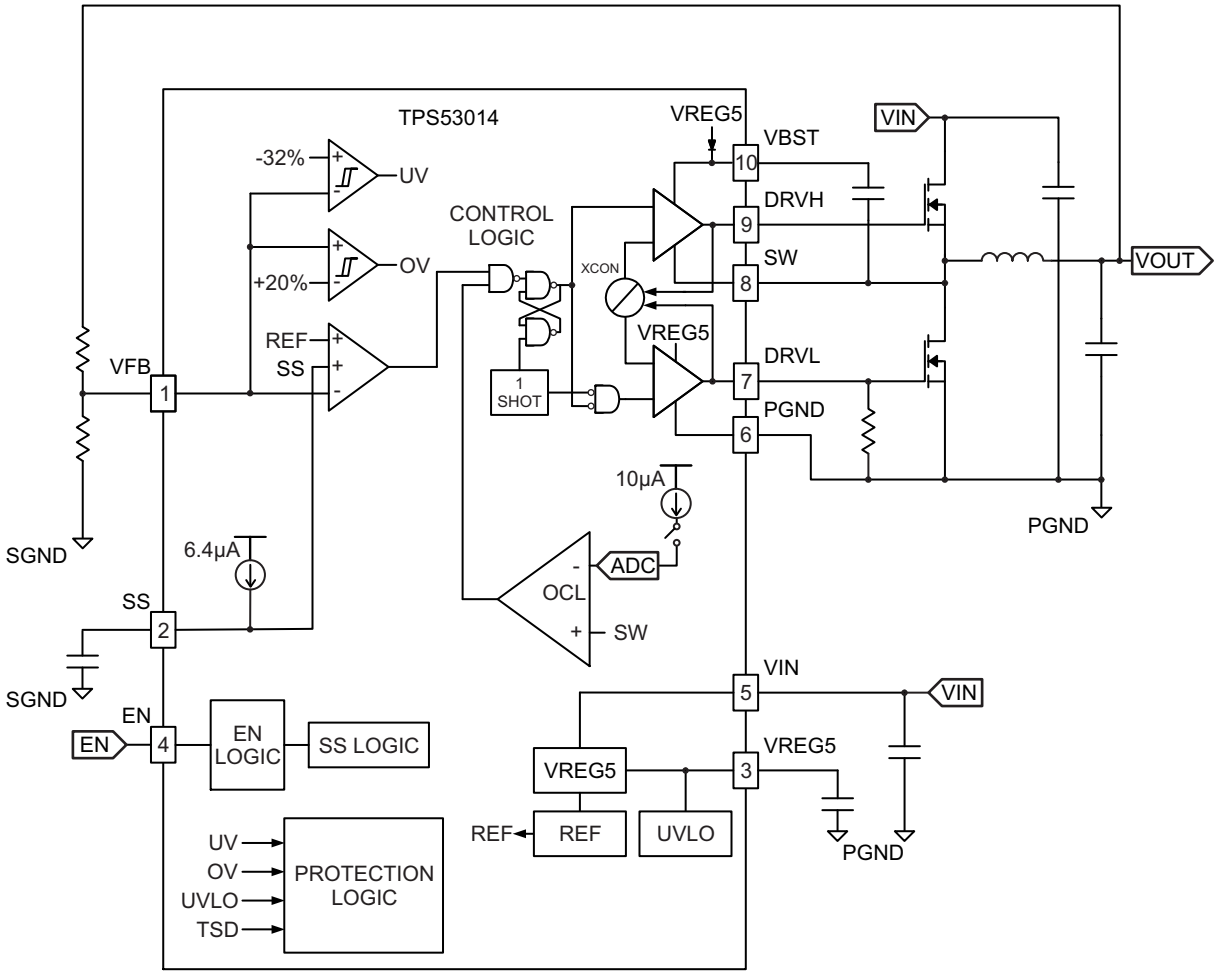
図 17. Input Voltage Ripple, I_{OUT} = 50 mA

7 Detailed Description

7.1 Overview

The TPS53014 is single synchronous step-down (buck) controller. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the required amount of output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS53014 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ control mode. D-CAP2™ control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. At the beginning of each cycle, the high-side MOSFET is turned on. this MOSFET is turned off when the internal timer expires. This timer is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

Feature Description (continued)

7.3.2 Auto-Skip Eco-Mode™ Control

The TPS53014 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point where its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost half as is was in the continuous conduction mode because it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation IOX(LL) current can be calculated in 式 1 with 500kHz used as fsw.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Drivers

TPS53014 contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SW referenced, VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to Gate Charge (Q_g @ V_{gs} = 5V) times Switching frequency (fsw). To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

7.3.4 5-Volt Regulator

The TPS53014 has an internal 5V Low-Dropout (LDO) Regulator to provide a regulated voltage for all both drivers and the ICs internal logic. A high-quality 4.7µF or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator.

7.3.5 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6.4-µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in 式 2. VFB voltage is 0.773 V and SS pin source current is 6.4-µA.

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times VFB(V)}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.773\ V}{6.4 \mu A} \quad (2)$$

The TPS53014 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than internal feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (VO) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

7.3.6 Overcurrent Protection

TPS53014 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53014 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, a resister should be connected between DRVL and PGND. The recommended values are given in表 1.

表 1. OCL Resistor Values

RESISTER VALUE (kΩ)	V_{trip} (V)
6.8	0.050
11	0.087
18	0.125
27	0.174
39	0.224
56	0.274
75	0.336

I_{OCL} is determined by 式 3.

$$I_{OCL} = \left(\frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \right) + \frac{V_{TRIP}}{R_{DS(ON)}} \quad (3)$$

The trip voltage is set between 0.05 V to 0.336 V over all operational temperature, including the 4000ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the overcurrent limit, the voltage will begin to drop. If the over-current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53014 will shut down.

7.3.7 Over/Undervoltage Protection

TPS53014 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 120% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53014 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately 1.7 × T_{ss} after power-on. The OVP and UVP latch off is reset when EN goes low.

7.3.8 UVLO Protection

TPS53014 has under voltage lock out protection (UVLO) that monitors the voltage of VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF. The UVLO is non-latch protection.

7.3.9 Thermal Shutdown

TPS53014 monitors its temperature. If the temperature exceeds the threshold value (typically 150°C), the device shuts off. When the temperature falls below the threshold, the IC starts again. When VIN starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is kept lower than 150°C. As long as VIN rises, T_J must be kept less than 110°C.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

A typical application schematic is shown in 図 18.

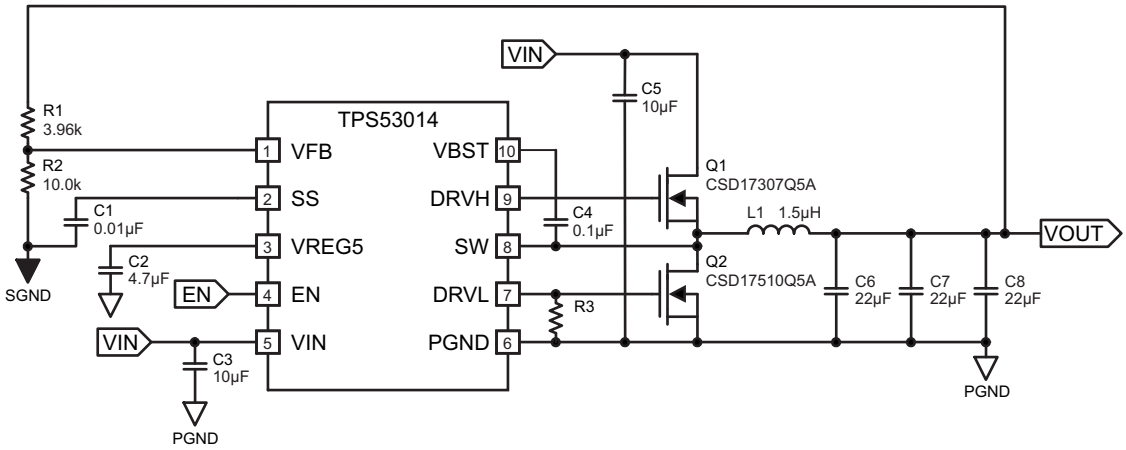


図 18. Application Schematic

8.1.1 Detailed Design Procedure

8.1.1.1 Component Selection

8.1.1.1.1 Inductor

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. 式 4 can be used to calculate te value for L_{OUT}.

$$L_{OUT} = \frac{V_{IN(MAX)} - V_{OUT}}{I_{L(RIPPLE)} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (4)$$

The inductors current ratings needs to support both the RMS (thermal) current and the peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L(RIPPLE)} = \frac{V_{IN(MAX)} - V_{OUT}}{L_{OUT} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} \quad (5)$$

$$I_{L(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L(RIPPLE)} \quad (6)$$

$$I_{L(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times I_{L(RIPPLE)}^2} \quad (7)$$

Note:

The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

Typical Application (continued)

8.1.1.1.2 Output Capacitor

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Ceramic output capacitors with X5R dielectric or better are recommended .

$$C_{OUT} = \frac{I_{L(RIPPLE)}}{8 \times V_{OUT(RIPPLE)}} \times \frac{1}{f_{SW}} \tag{8}$$

$$C_{OUT} = \frac{\Delta I_{LOAD}{}^{2}}{2 \times V_{OUT} \times \Delta V_{OS}} \times L_{OUT} \tag{9}$$

$$C_{OUT} = \frac{\Delta I_{LOAD}{}^{2}}{2 \times K \times \Delta V_{US}} \times L_{OUT} \tag{10}$$

Where:

$$K = (V_{IN} - V_{OUT}) \times \frac{T_{ON}}{T_{ON} - T_{OFF(MIN)}}$$

- ΔV_{OS} = The allowable amount of overshoot voltage in load transition
- ΔV_{US} = The allowable amount of undershoot voltage in load transition
- $T_{OFF(MIN)}$ = Minimum off time (11)

Select the capacitance value greater than the largest value calculated from 式 8, 式 9 and 式 10. The minimum recommended output capacitance is 44 μF.

8.1.1.1.3 Input Capacitor

The TPS53014 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-μF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.1.1.1.4 Bootstrap Capacitor

The TPS53014 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-μF high-quality ceramic capacitor is recommended. The capacitor voltage rating should be greater than 10 V.

8.1.1.1.5 VREG5 Capacitor

The TPS53014 requires that the VREG5 regulator is bypassed. A minimum 4.7-μF high-quality ceramic capacitor must be connected between the VREG5 and PGND for proper operation. The capacitor voltage rating should be greater than 10 V.

8.1.1.1.6 Choose Output Voltage Resistors

The output voltage is set with a resistor divider from output voltage node to the VFB pin. TI recommends using 1% tolerance or better resistors. Select R2 between 10 kΩ and 100 kΩ and use 式 12 to calculate R1.

$$R1 = \left(\frac{V_{OUT}}{V_{VFB}} - 1 \right) \times R2 \tag{12}$$

9 Layout

9.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Place the input capacitor close to the top switching FET. Keep the output current loop as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (VFB) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

10 デバイスおよびドキュメントのサポート

10.1 ドキュメントの更新通知を受け取る方法

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10.2 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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10.4 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53014DGS	LIFEBUY	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	53014	
TPS53014DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 85	53014	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

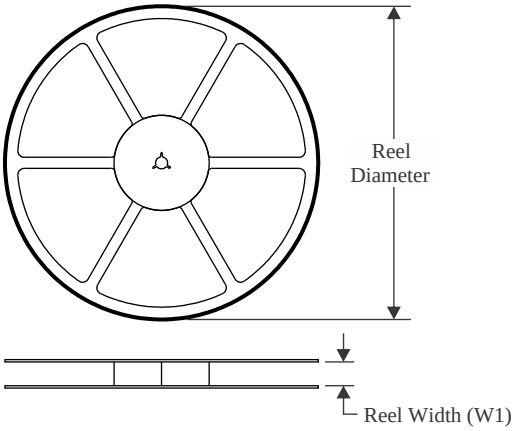
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

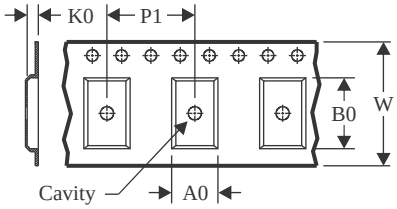
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

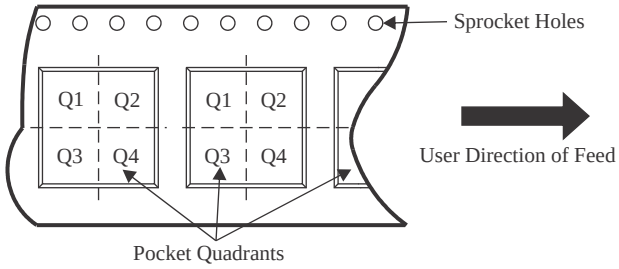


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

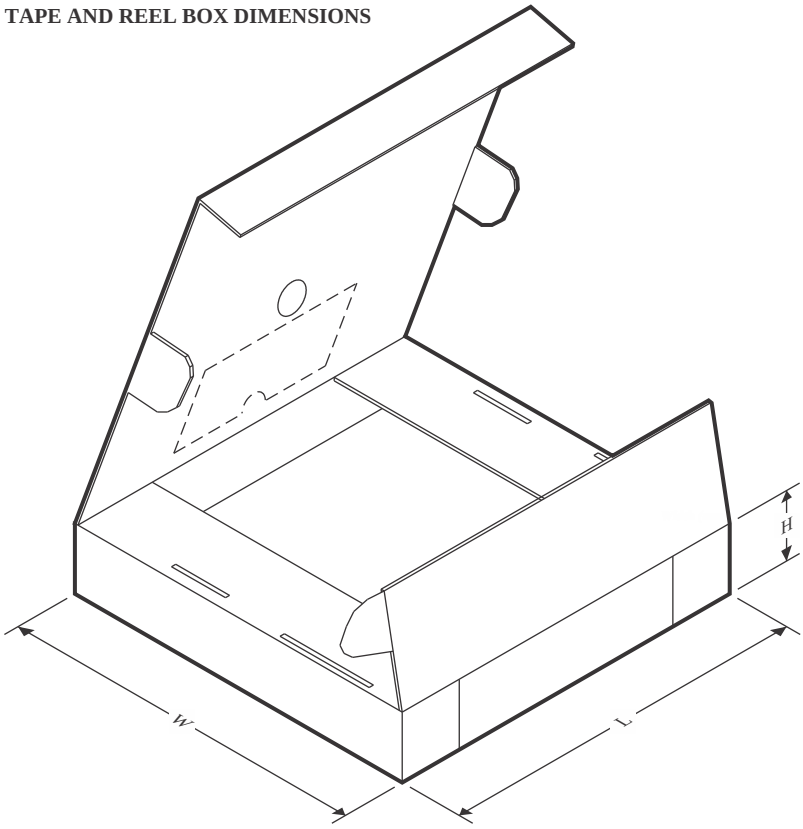
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53014DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

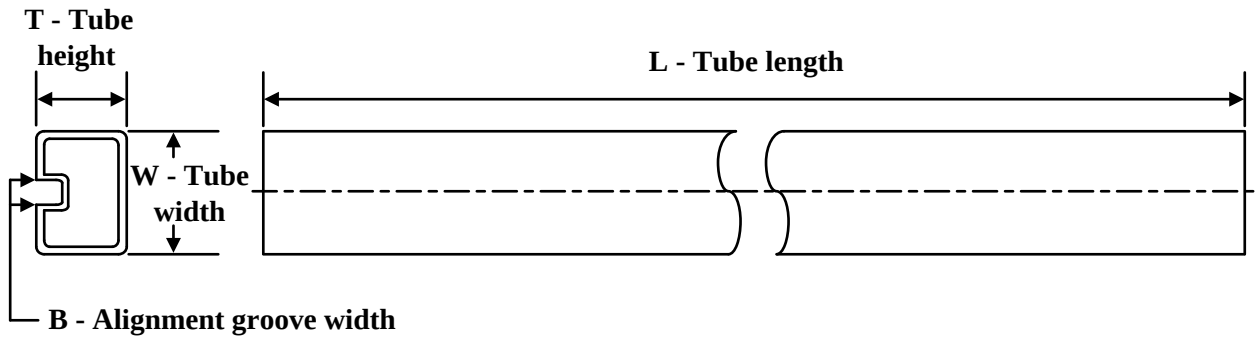
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53014DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

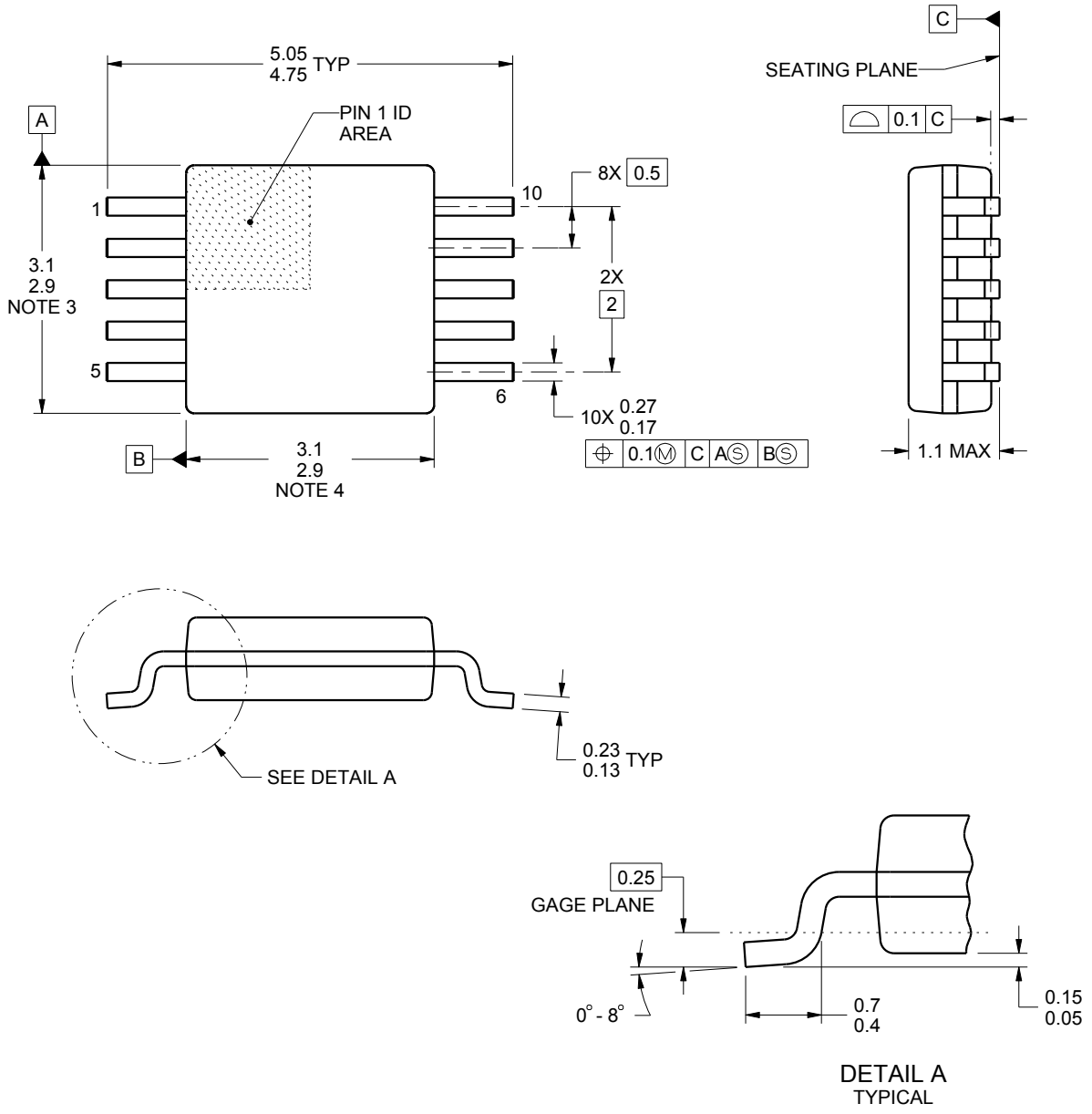
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS53014DGS	DGS	VSSOP	10	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGS0010A

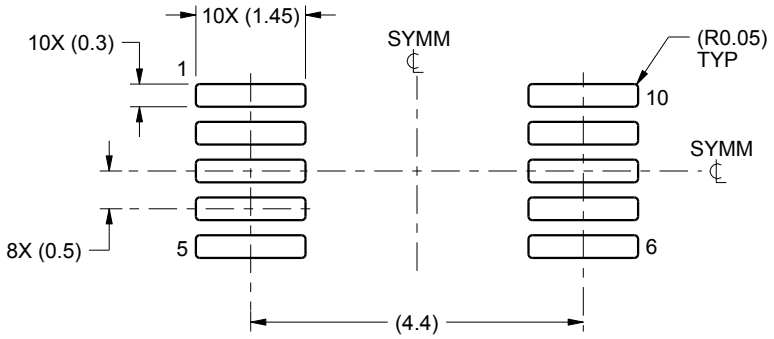
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

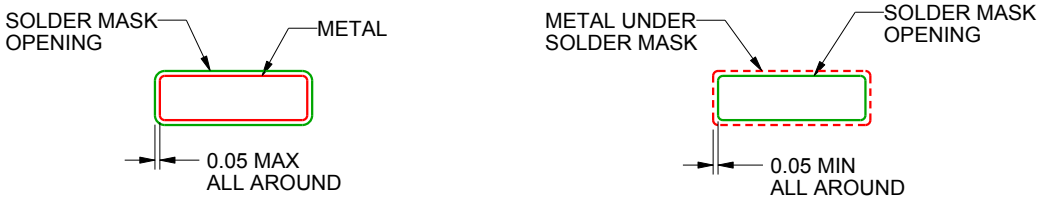


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

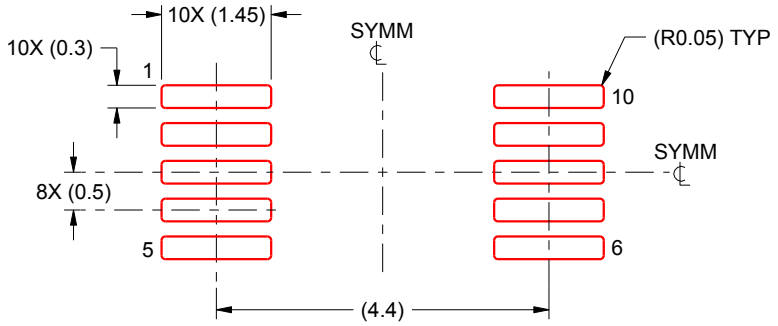


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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